2007-2008 PhD Qualifying Examination

Professor Yoshio Nishi

1. Please explain basic C-V characteristics of silicon MOS capacitor with p-type substrate measured at low enough frequency and at high enough frequency at room temperature. You can ignore any series resistances in gate electrode contact and substrate contact.

2. What would happen if you do the same measurements at 600K and at 50K for (a) highly doped substrate, (b) lightly doped substrate? Please assume the acceptor doping concentrations in the substrates are uniform for both cases.

3. If the silicon MOS capacitor has very high density of interface states (traps) at the middle of silicon forbidden gap, how would the C-V curve change, and why? You can assume it is acceptor-like interface states, and substrate silicon is p-Type.