Date: Wed, 01 Mar 2006 22:45:39 -0800
To: Diane Shankle <shankle@ee.Stanford.EDU>
From: Simon Wong <wong@ee.Stanford.EDU>
Subject: Re: Reminder Quals Question 2006

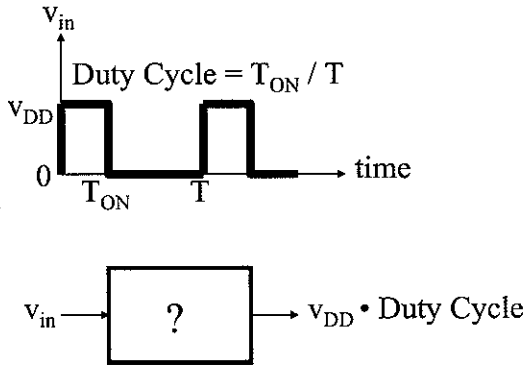
Simon Wong,

Given the layout of a circuit, identify each layer, the transistor, connection and determine the circuit.
Answer : first circuit is a CMOS inverter, 2nd circuit is a CMOS cascode amplifier

At 08:58 AM 3/1/2006, you wrote:

> Hi,
>
> Reminder!
>
> Please send me your Quals question.
>
> Thanks and Enjoy Your Day,
> Diane

2009 Qualifying Exam
Simon Wong




1. Design a circuit such that with the periodic input waveform shown, the output is approximately a DC voltage of $V_{DD}$ • Duty Cycle.

   A low pass filter with bandwidth << 1/T;

   Possible Answers :

   R-C low pass filter with $2\Pi RC >> T$

   R-L low pass filter with $2\Pi L/R >> T$

   L-C filter with $2\Pi(LC)^{1/2} >> T$
   (Except for the peaking at resonant frequency, this filter has a low-pass behavior.)

2. If the output has to drive a heavy load (e.g., 1A), how will you modify the circuit ?

   Possible Answers :

   R-C low pass filter will not be appropriate as the small load resistance will increase the effective bandwidth.

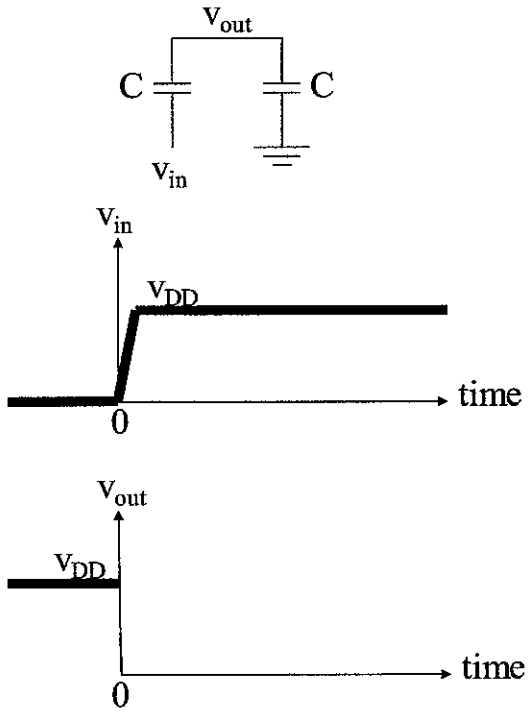
   R-L low-pass filter will be fine, but the small load resistance will decrease the effective bandwidth.

   L-C filter will not be significantly affected by the load resistance. The peaking will be reduced.

   Add a unity gain voltage buffer that is capable of driving the heavy load.

2010 Qualifying Exam
Simon Wong

1. Sketch $V_{out}$.
   Ans: final $V_{out} = 1.5\ V_{DD}$
2. What is initial total stored energy ? What is final total stored energy ?
   Ans: initial $E = CV_{DD}^2$; final $E = 1.25CV_{DD}^2$
3. If C can be varied, what is the maximum final $V_{out}$ ?
   Ans: $C_{left} >> C_{right}$; maximum final $V_{out} = 2\ V_{DD}$
4. Modify the circuit to achieve final $V_{out} = 3\ V_{DD}$.
   Many possible solutions including the following :
   $C_{left} >> C_{right}$; insert a diode between the 2 C, drive the bottom plate of the right C to $V_{DD}$.



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Simon Wong

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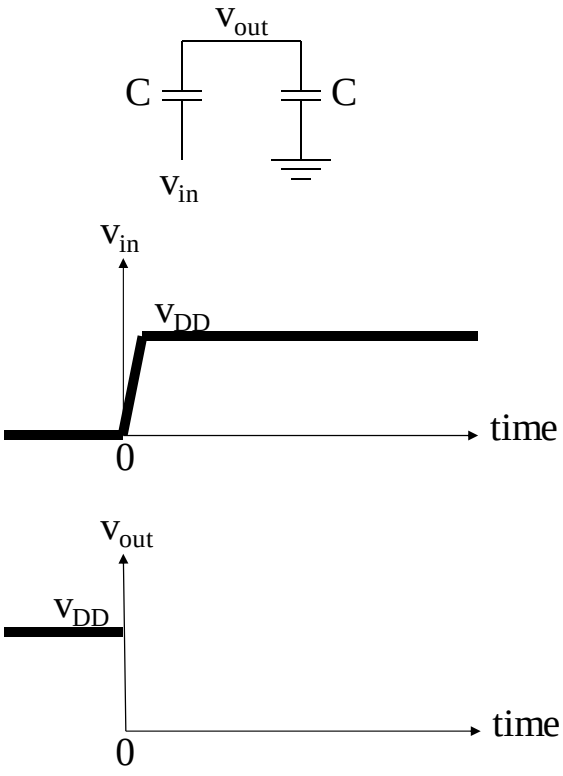

2013 Qualifying Exam
Simon Wong

An n-channel MOSFET with $V_{TH} = 0.5V$, $V_G = 1V$, $V_S = 0V$, sketch $I_D$ versus $V_D$.

Why does $I_D$ saturate ?
Channel pinches off near the drain.

Will $I_D$ stay saturated at very high $V_D$ ?
No, at high $V_D$, $I_D$ will increase rapidly.

What is the mechanism responsible for the rapid increase in $I_D$ ?
There are at least 4 possible mechanisms:

1. Darin-induced-barrier-lowering, also known as punch through
2. Avalanche (in the channel) induced breakdown
3. Drain-substrate junction breakdown
4. Drain-gate oxide breakdown

The dominant mechanism depends on the channel length, gate oxide thickness, and doping levels in the junction, channel and substrate.

How can you distinguish which mechanism is responsible for the rapid increase in $I_D$ ?
Measure all currents, $I_D$, $I_S$, $I_G$, and $I_{SUB}$. Assume the device has been destroyed yet.

1. Drain-induced-barrier-lowering
   $I_D \cong I_S, I_G \cong 0, I_{SUB} \cong 0$
2. Avalanche induced breakdown
   $I_D \cong I_S, I_G \cong 0, I_{SUB} \neq 0$ but $<< I_D$
3. Drain-substrate junction breakdown
   $I_D \cong I_{SUB}, I_S < I_D, I_G \cong 0$
4. Drain-gate oxide breakdown
   $I_D \cong I_G, I_S < I_D, I_{SUB} \cong 0$