computer Architecture

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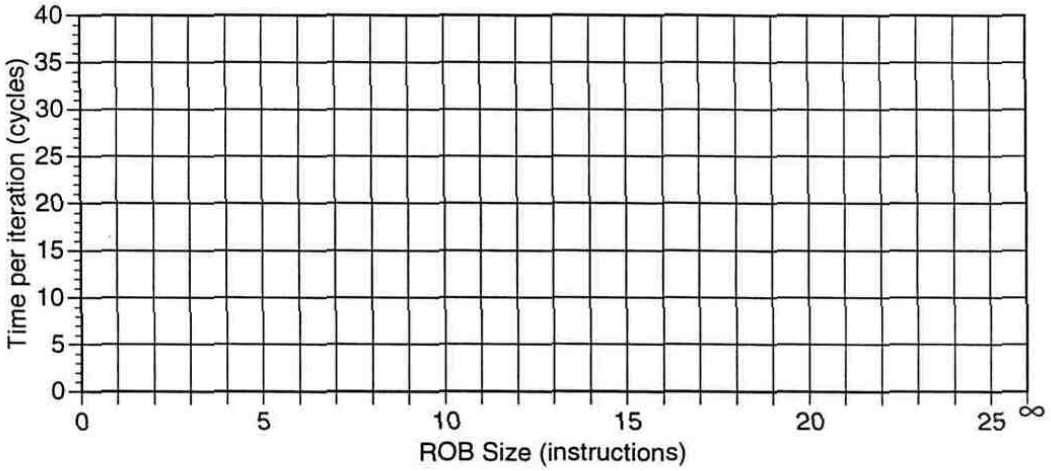
1. What's a non-blocking cache (NBC)?
2. How does it improve AMAT?
3. What do you need in processor and memory system to make a NBC most effective?
4. Fill in the graph below? (assume a pipelined memory system)

```
for (i = 0; i < 1000; i +=2)
      B[i] = B[i] + C[i] + B[i+1] + C[i+1]; /* all arrays are 4-byte
                                              integers */

        top:  LD   R1, B[i]
              LD   R2, C[i]
              ADD R3, R1, R2
              LD   R4, B[i+1]
              ADD  R5, R3, R4
              LD   R6, C[i+1]
              ADD R7, R5, R6
              ST   R7, B[i]
              3 instrs to update i, B[i], C[i]
              BLT R8, #1000, top
```



Assumptions

1. fully associative non-blocking data cache, initially empty
2. 8 byte cache line size
3. write back, write allocate
4. 10 cycle miss penalty
5. single issue fully pipelined processor
6. perfect branch prediction