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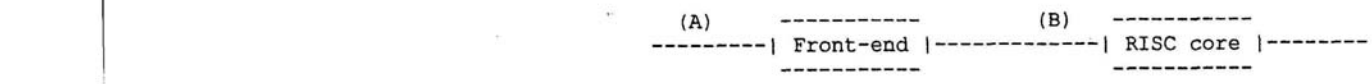
Modern CISC processors (e.g. the superscalar Pentium 4 or Athlon designs) are not as CISC as they used to be. Often, a RISC core lies at the heart of the processor and a "front-end" translates a CISC instruction to a sequence of one or more RISC-like micro-instructions.



1) Designers of CISC processors are faced with the decision of placing an instruction cache a location (A) or at location (B). Discuss the advantages and disadvantages of each alternative, particularly with respect to wide superscalar microarchitectures.

A particular CISC processor has a cache only at location (A). Its RISC core could achieve CPI of 1.0, if it was given a steady stream of micro-instructions. However, the front-end takes 5 cycles (unpipelined) to translate a CISC instruction. On the average, each CISC instruction translates to 3 RISC microinstructions.

A (B) cache is proposed as an alternative. On a hit, this cache can produce 1 translation per cycle. Misses take 12 cycles. What hit rate would you need for the (B) cache in order to operate the RISC core at its peak performance? What speedup does this give you over the original processor with the cache in location (A)?

Tip: assume that both alternatives have sufficient buffering at proper locations in order to stream-line execution.