X-Sender: horowitz@vlsi.stanford.edu
Mime-Version: 1.0
Date: Wed, 21 Jan 1998 13:08:24 -0800
To: shankle@ee.stanford.edu
From: Mark Horowitz <horowitz@ee.stanford.edu>
Subject: Quals questions
Status:

Computer Architecture

We would like to build a logic block that detects when the 32 or 64 bit operand is equal to zero.

1. What logic function is this?
   NOR

2. How would you implement this using static logic gates
   Looking for NOR-NAND tree. pseudo nMOS was an interesting answer too, but then asked about using std cells to get tree solution

Show the students a simple datapath diagram for a simple processor. Zero detect is placed after a 3-1 mux for bypass (inputs from Regfile, ALU out, and cache memory). The mux has a flop in it. Say that the delay of the zero detect unit is too slow, and that you need the output right after the clock edge.

3. How can you get the output earlier
   Triplicate the unit and move it to the inputs of the mux

4. What assumptions are you making by moving the unit
   There is excess time in the regfile, alu and memory paths

5. You ask the Regfile designer whether there is spare time, and he say no. Can you get the same effect a different way?
   Store a 33 or 65 bit that indicating whether the value is zero, since you must have computed it already on the path that created the value.