Date: Wed, 1 Mar 2006 17:22:45 -0800
From: "Subhasish Mitra" <subh.mitra@gmail.com>
To: "Diane Shankle" <shankle@ee.Stanford.EDU>
Subject: Re: Reminder Quals Question 2006

Hi Diane,

Here are the questions.
-Subhasish

Suppose you have a system where bits are coming in serially, 1 bit at each clock cycle. With each bit coming in, you create a binary number where the last received bit is treated as the Least Significant Bit (LSB) and so on. For example, suppose that everything is initialized to 0. The first bit that comes in is 1 – the number is 1; the second bit received is 0, so the number is now "10" = 2; the third bit received is 1, so the new number in the third cycle is "101" = 5, and so on. At each clock cycle the system output is 1 if and only if the number at that clock cycle is divisible by 7.

Create a state diagram for the corresponding sequential circuit.

What is the minimum number of states you can have?

How will you implement a similar circuit for which we want to find out if the number at each clock cycle is divisible by 28?

What happens if we want to find out if the number at each clock cycle is prime?

On 3/1/06, Diane Shankle <shankle@ee.stanford.edu> wrote:
> Hi,
>
> Reminder!
>
> Please send me your Quals question.
>
> Thanks and Enjoy Your Day,
> Diane
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