Robert Dutton
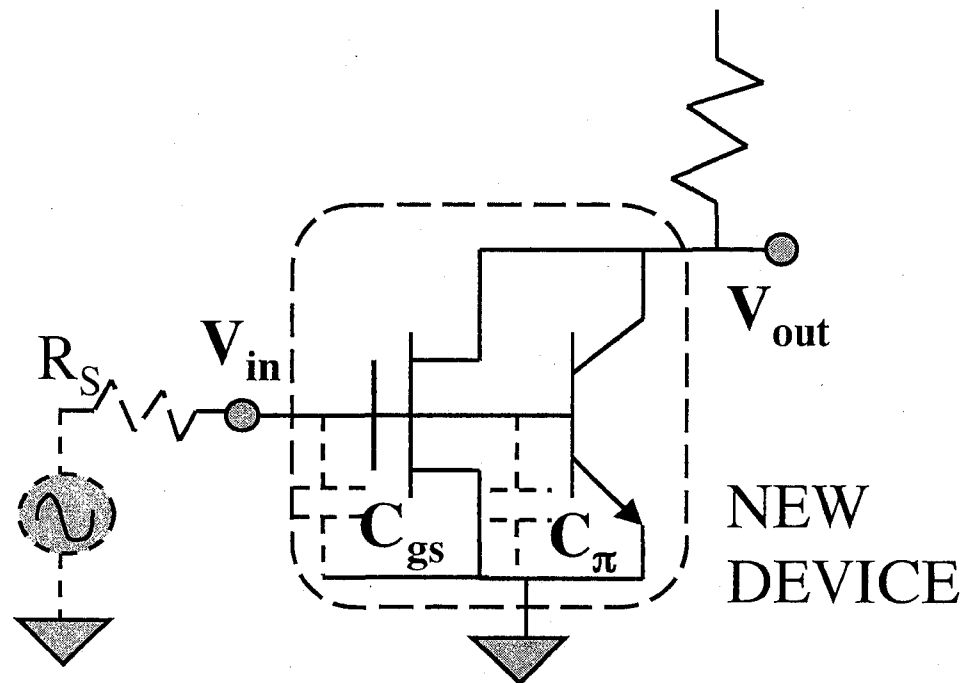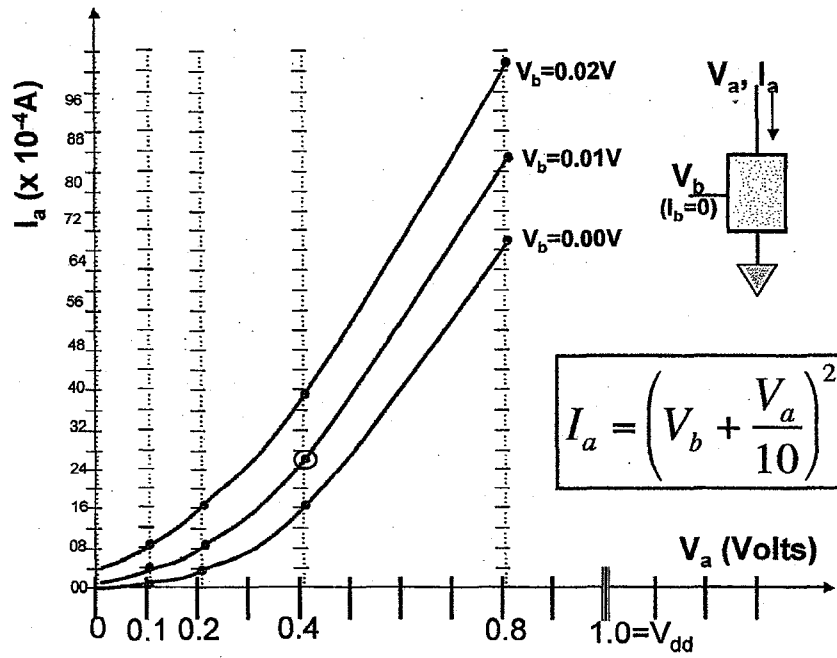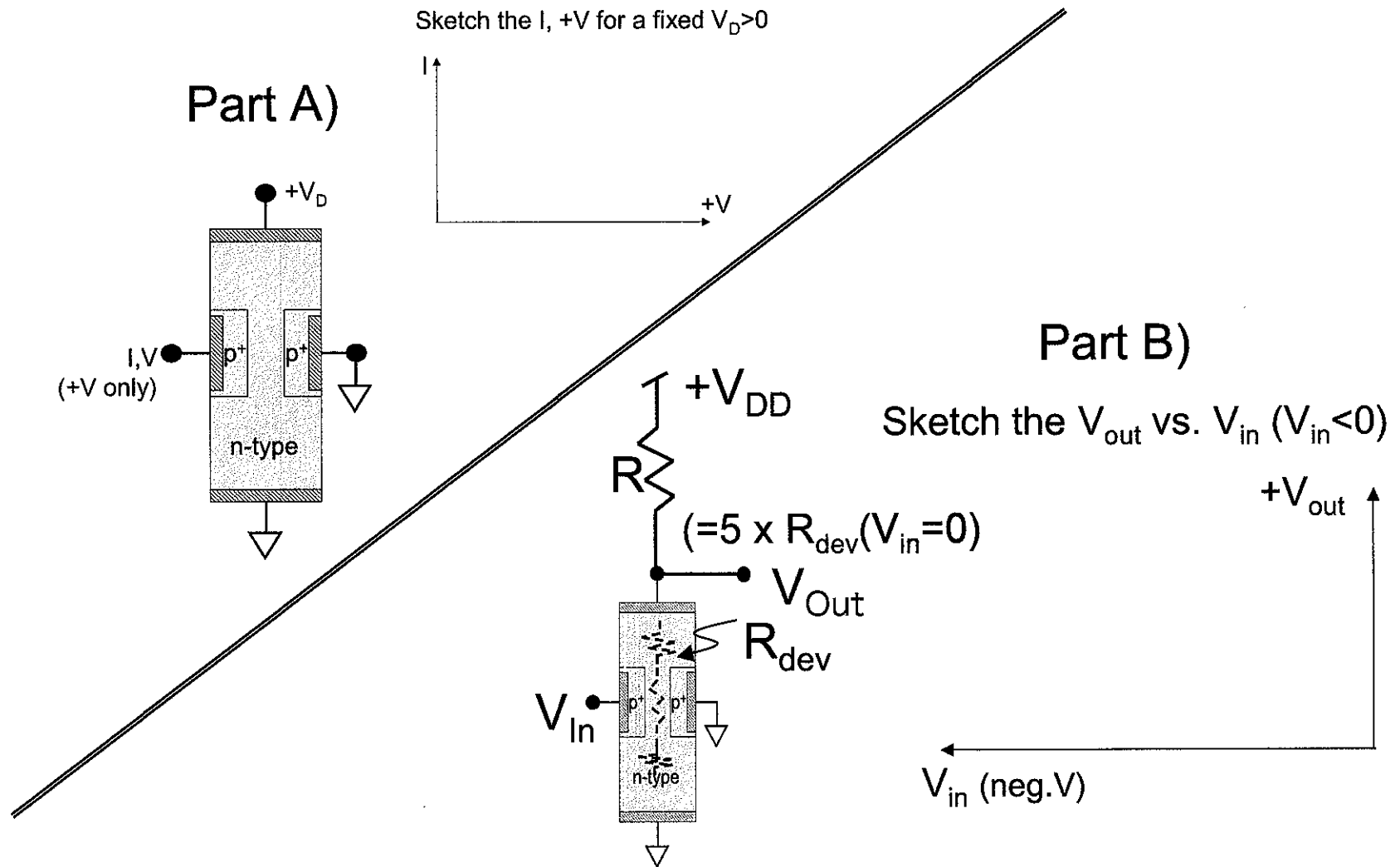
A device technologist has created a NEW DEVICE-- part MOS, part BJT--with "drive current" given by: $I_{Drive}=I_D(MOS)+I_C(BJT)$. The schematic is as follows.


To achieve maximum small-signal (ac)voltage gain, at what operating point should we bias the NEW DEVICE? What is the ac gain and bandwidth?

I_a ($\times 10^{-4}$A)

96
88
80
72
64
56
48
40
32
24
16
08
00

V_b=0.02V
V_b=0.01V
V_b=0.00V

V_a, I_a

V_b
(I_b=0)

$$I_a = \left(V_b + \frac{V_a}{10}\right)^2$$

V_a (Volts)

0   0.1 0.2   0.4   0.8   1.0=V_{dd}

Sketch the I, +V for a fixed $V_D > 0$

I

+V

Part A)

+V_D

I,V
(+V only)

p⁺   p⁺

n-type

Part B)

Sketch the V_{out} vs. V_{in} ($V_{in} < 0$)

+V_{DD}

R

(=5 x $R_{dev}(V_{in}=0)$)

V_{Out}

R_{dev}

V_{In}
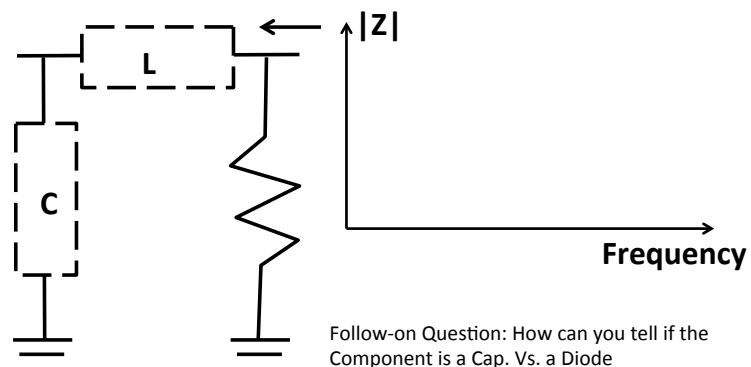
p⁺   p⁺

n-type

+V_{out}

V_{in} (neg.V)

After discussion of Parts A) and B) there were follow-on questions (not included here) dealing with different terminal connections and bias conditions for Part A) and how to "optimized" the device performance in Part B)
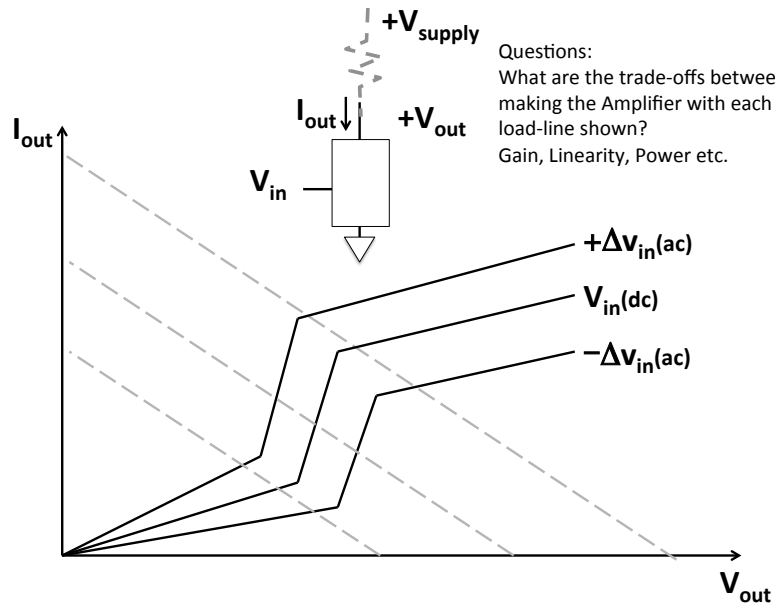
Choices For Components:
R, L, C, Diode

|Z|

Frequency

L

C

Choices For Components:
R, L, C, Diode

L

C

|Z|

Frequency
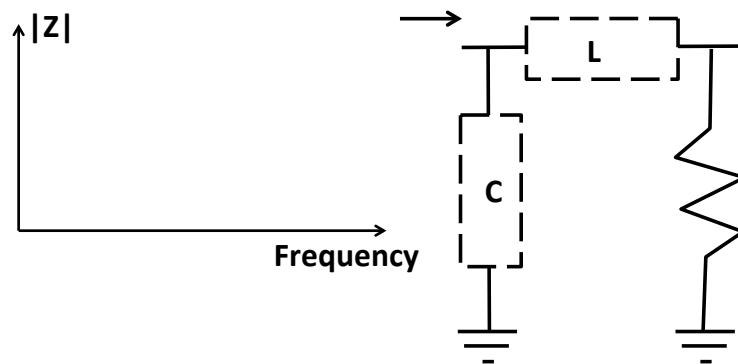
Follow-on Question: How can you tell if the
Component is a Cap. Vs. a Diode

$+V_{supply}$

I_{out} $+V_{out}$

V_{in}

I_{out}

V_{out}

$+\Delta v_{in}(ac)$

$V_{in}(dc)$

$-\Delta v_{in}(ac)$

Questions:
What are the trade-offs between making the Amplifier with each load-line shown?
Gain, Linearity, Power etc.

The digital world deals with "1" and "0" so...why do we need to consider the amplification of signals? (What does amplification mean and why do we need it?)

What does an amplifier do and how does it work?

Suppose the world only had ideal switches with series resistance as shown. How would that work from a digital time-domain perspective? (Explain what your amplifier would do)

$+$

C

V_{in}

$-$

R

$V_{in} > |V_T|$
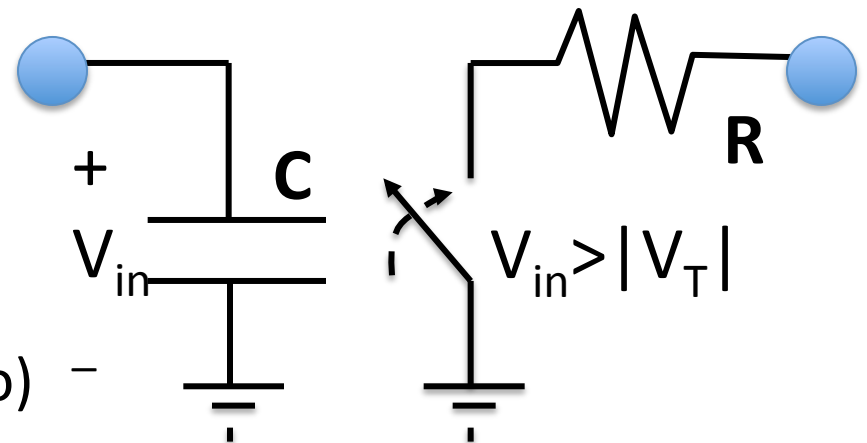
What would you do if we want to amplify current? (How would you do it?)