To: "Diane J. Shankle" <shankle@sierra.stanford.edu>
Subject: Re: Quals Questions
In-Reply-To: Your message of Mon, 14 Feb 94 16:02:10 -0800.
<CMM.0.90.0.761270530.shankle@Sierra.Stanford.EDU>
Date: Tue, 15 Feb 94 10:21:42 PST
From: Mark Horowitz <horowitz@chroma.Stanford.EDU>

Here is my quals question:

Area: Digital Design

Question:

You need to design a priority encoder. This is a block that has n inputs (where n is around 32) and n outputs. One only output is allowed to be high at anytime, and should correspond to the highest priority input that is asserted. Assume that the highest priority input is connected to the MSB of the encoder, and the lowest priority input is connected to the LSB.

Examples of a 4 bit priority encoder:

In	1111	0101	0011	0000
Out	1000	0100	0010	0000

How would you design this circuit?

Answer:

There is no right answer. I am more interested in the process of getting a solution. Most often people come up with a single gate for each output. The fanin of this gate grows with the number of inputs, so this is not a great answer. There is also a ripple-carry like solution which is very dense, but slow. Good students go through both of these, and then synthesize a solution is like a ripple-carry, but is faster using some block based approach.

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