8; Wed, 3 Mar 93 08:35:48 PST
Received: by chroma.Stanford.EDU (5.57/Ultrix3.0-C)
        id AA22838; Wed, 3 Mar 93 08:35:47 -0800
Message-Id: <9303031635.AA22838@chroma.Stanford.EDU>
To: "Diane J. Shankle" <shankle@sierra.stanford.edu>
Cc: horowitz@chroma.stanford.edu
Subject: Re: Last Chance
In-Reply-To: Your message of Tue, 02 Mar 93 13:32:53 -0800.
             <CMM.0.90.0.731107973.shankle@Sierra.Stanford.EDU>
Date: Wed, 03 Mar 93 08:35:47 PST
From: Mark Horowitz <horowitz@chroma.stanford.edu>

architecture

Quals Question:

1. You are designing a computer and need to build a function unit that checks to see if the value on the source bus is zero. How would you build the function unit in CMOS?

Answer:
There are two ways of solving this problem. No matter which you choose I would ask for the other answer as well.

Tne circuit that is needed is a 32 input NOR gate, since its output will be 1 only if all the inputs are zero. This can be built by using a precharged gate will 32 parallel transistors, a precharge pullup, and a single pulldown device. For this gate to work, the inputs must be stable when the evaluate transistor turns on. A pseudo nMOS gate, with a single pMOS static load and 32 pulldown nMOS devices would be ok for this part of the problem as well.

The other solution is to use static CMOS gates. Since there is a series stack of transistors that is proportional to the number of inputs, each gate must have a limited fanin. Let's set the fanin to be 2. One can use a tree to build a 32 input out of 2 input gates. The first layer is 16 2input NOR gates. Since the outputs are inverted, the next stage must be NOR with inverted inputs, which are NAND gates. There are 8 or these gates. The next level in the tree is then 4 NOR gates, and this is followed by 2 NAND gates, and the final NOR gate. The key was to realize that you need to flip from NORs to NANDs to handle the inversions.

2. How does the delay of these structures scale with the number of inputs.

For the precharge gate, the resistance of the worst-case pulldown is constant. The cap of the output node will increases linearly with the number of inputs, since each additional input adds some diffusion cap to the output node.

In the tree, the critical path is the depth of the tree. This is log2 of the number of inputs. Thus, since the delay of all the 2input gates should be similar, the delay is proportional to the log2 of the number of inputs.

3. Which of the two structures is faster? Does the answer depend on the number of inputs?

ince the precharge gate's delay increases linearly with n, and the
ree is log(n), the tree must be faster for large n. The key question
s which is faster for small n. I was interested in how students
ttacked this problem. The precharge gate will be faster, since it has
ewer transistors, and that means less input and output capacitance.
o the right anwer is the precharge gate is faster at small n and the
ree is faster for large n.

. Does the answer to question 3 give you an idea of how to build a
aster 32 input NOR?

ure, replace the NOR gates in the tree with precharge gates. This
ould allow you to increase the fanin of these gates, and shorten the
epth of the tree while maintaining the same gate delay. The NAND
ates in the tree invert the output of the precharge gates, so the
nputs to the NAND gates are monotonically rising signals.

To: "Diane J. Shankle" <shankle@sierra.stanford.edu>
Subject: Re: Quals Questions
In-Reply-To: Your message of Mon, 14 Feb 94 16:02:10 -0800.
<CMM.0.90.0.761270530.shankle@Sierra.Stanford.EDU>
Date: Tue, 15 Feb 94 10:21:42 PST
From: Mark Horowitz <horowitz@chroma.Stanford.EDU>

Here is my quals question:

Area: Digital Design

Question:

You need to design a priority encoder. This is a block that has n inputs (where n is around 32) and n outputs. One only output is allowed to be high at anytime, and should correspond to the highest priority input that is asserted. Assume that the highest priority input is connected to the MSB of the encoder, and the lowest priority input is connected to the LSB.

Examples of a 4 bit priority encoder:

In	1111	0101	0011	0000
Out	1000	0100	0010	0000

How would you design this circuit?

Answer:

There is no right answer. I am more interested in the process of getting a solution. Most often people come up with a single gate for each output. The fanin of this gate grows with the number of inputs, so this is not a great answer. There is also a ripple-carry like solution which is very dense, but slow. Good students go through both of these, and then synthesize a solution is like a ripple-carry, but is faster using some block based approach.

R>

To: shankle@ee.Stanford.EDU
Cc: darlene@mojave.Stanford.EDU
Subject: Quals Question.
Date: Sun, 19 Mar 95 13:20:46 PST
From: Mark Horowitz <horowitz@chroma.Stanford.EDU>

Computer Architecture

Here was my quals question:

The question was really to see how students handled dealing with an element that they had not seen before -- a relay. To help them out, I started out with more familar material, CMOS switch logic.

1. Using CMOS switches build a XOR gate

There are many ways to approach this problem, and I didn't really care which was chosen. The easiest is to build the gate from two switches that form a 2:1 mux. The top switch connects when the input A is true and the bottom switch connects when the input A is false. The top switch connects to B_b and the bottom switch connects to B. One could have built the gate out of a 4:1 mux too.

2. Using CMOS switches build an AND gate

Here the best solution is to use the same 2:1 mux solution used above. The top switch connects to B and the bottom switch connects to Gnd. Most students choose to build an AND gate using 4 switches -- two series devices connected to Vdd, and two parallel devices connected to Gnd.

3. Actually I was not really interested in using CMOS switches. I really want to build logic gates out of relays. A relay is an electro-mechanical device, where a current creates a magnetic field which pulls a cylinder into a coil and mechanically changes the switches. The input goes to the coil (one end is connected to Gnd), and this relay has one normally connected switch, and one switch which is normally not connected (so there are 5 terminals to this device). In terms of abstract switches, how would you represent this element?

This relay is a GREAT device. It basically consists of two ideal switches, on connects when the input is 1 (the normally not connected) and the other connects when the input is 0 (the normally connected switch). This means that the relay is like a package of an nMOS and a pMOS transistor. But unlike transistors, there is no problem with threshold drops.

4. Using this relay as a basic element please make an XOR gate. (I allow them to use inverted signals at first, but the final solution can have only the true value of signals)

Since the relay contain both type of switches, connecting the switch outputs together forms a 2:1 mux. Using another relay it is easy to make an inverter to form B_b from B.

5. Now build an AND gate.

Again use the 2:1 mux and connect B to the normally not connected switch, and connect Gnd to the normally connected switch. (The latter connection is not really needed, see the following questions)

6. In logic built out of CMOS switches the output is not allowed to be left floating. Why?

If an output is left floating, it with retain the previous value, becuase the inputs of CMOS switches do not take input current. To prevent building a latch, you need to make sure that the output is always driven.

7. In logic built out of relays, are floating outputs ok? Why or why not?

Since relays are activated by current, a 1 must be a path that can supply current. If the output is left floating, there will not be a path for current. Thus, a floating output is the same as a zero. For relays there is not need to drive a zero value. It is ok just to leave the output floating.

Professor Mark Horowitz

Build a decoder for a 256 x 256 memory. The address lines A0 - A7 (and their complements, A0_b - A7_b) are available.

The only components that you can use in your design are inverters and 2 input NAND gates, and 2 input NOR gates.

1. What logic would you use to build the decoder?
   If they have problems with that, suggest that they look at a single wordline first — WL0, and derive the logic function for this WL. If they build a full tree at each gate, need to ask, whether they can share logic ...

2. Having done the logic, how would you layout this design?
   Look for people worrying about the wires. Clearly the final NAND inverter should be next to the wordline, but so should the next level, unless you want to double the wire tracks

3. Assume that inverters would like to have a fanout of 4, and NAND and NOR gates would like to have a fanout of 3. Also assume that each memory cell contributes 10fF to the wordline load. Using these assumptions find the rough sizes of the gates in your decoder (you can measure the gate's size by its input capacitance).

X-Sender: horowitz@vlsi.stanford.edu
Mime-Version: 1.0
Date: Wed, 21 Jan 1998 13:08:24 -0800
To: shankle@ee.stanford.edu
From: Mark Horowitz <horowitz@ee.stanford.edu>
Subject: Quals questions
Status:

Computer Architecture

We would like to build a logic block that detects when the 32 or 64 bit operand is equal to zero.

1. What logic function is this?
NOR

2. How would you implement this using static logic gates
Looking for NOR-NAND tree. pseudo nMOS was an interesting answer too, but then asked about using std cells to get tree solution

Show the students a simple datapath diagram for a simple processor. Zero detect is placed after a 3-1 mux for bypass (inputs from Regfile, ALU out, and cache memory). The mux has a flop in it. Say that the delay of the zero detect unit is too slow, and that you need the output right after the clock edge.

3. How can you get the output earlier
Triplicate the unit and move it to the inputs of the mux

4. What assumptions are you making by moving the unit
There is excess time in the regfile, alu and memory paths

5. You ask the Regfile designer whether there is spare time, and he say no. Can you get the same effect a different way?
Store a 33 or 65 bit that indicating whether the value is zero, since you must have computed it already on the path that created the value.

X-Sender: horowitz@vlsi.stanford.edu
Date: Sat, 16 Jan 1999 01:07:52 -0800
To: shankle@ee.stanford.edu
From: Mark Horowitz <horowitz@stanford.edu>
Subject: Quals question:
Cc: horowitz@vlsi.Stanford.EDU
Mime-Version: 1.0

Computer Architecture and logic design

We will be looking at the question of wire delay in an IC. To solve this problem we will model delay using simple RC models.

I present the student with an example wire 1u wide, and 1mm long. It has a resistance of 100ohms and a capacitance of .13pF

1. How does the resistance and capacitance of the wire vary with length
   (both are linear)
2. How does the delay vary with length
   (quadratic)
3. What is the delay of a 10mm wire.
   1/2 RC = 650ps

4. If that is too large how could you reduce it?
   wire wider, repeaters

5. Shown on the board is how the capacitance of the wire varies with width. At 1u = .13pF, 2u=.16pF, 3u=.19pF. Does this data make sense? What does the extrapolated value of 0.1pF at zero width represent?
   Makes sense. 0.1pF is the fringe capacitance

6. Roughly how much faster can you make the wire by making it wider?
   4 times

7. Why does adding buffers speed up the wire?
   breaks the increasing resistance with length

8. What parameters should you optimize in a wire with repeaters to minimize delay.
   distance between inverters and the inverter size

9. Write the delay equation for one segment of a buffered wire

RC delay model, repeater, fringe capacitance, buffer

X-Sender: horowitz@vlsi.stanford.edu
Date: Mon, 24 Jan 2000 23:41:10 -0800
To: Diane Shankle <shankle@ee.stanford.edu>
From: Mark Horowitz <horowitz@stanford.edu>
Subject: Re: Reminder: Quals Questions were due on Friday, 1/21/200

Here is my quals question

We are looking at a machine that has variable length instructions. Assume that the top two bits indicate the instruction length. 0- indicates 2B instruction, 10 is 4B and 11 is 5bytes.

1. Show the logic for the length decoder. (it has 3 outputs)

2. Show the logic for getting the instruction data aligned for the next instruction decode

3. Assume you want to build a machine that can issue three instructions each cycle. Show how you would connect 3 instruction decoders to the register that contains the instruction bytes. Don't worry about delay, but show the critical path

4. Now assume that decoding the instruction length is complex, like in the x86 instruction set. What techniques could you use to speed up the implementation. You have as much hardware as you need.

5. Would making the long instructions 6 bytes make the decoding easier?

X-Sender: horowitz@vlsi.stanford.edu
Date: Thu, 15 Feb 2001 11:01:41 -0800
To: Diane Shankle <shankle@ee.stanford.edu>
From: Mark Horowitz <horowitz@stanford.edu>
Subject: Re: Quals Question 2001

Quals questions:

Assume we want to generate a field specifier for a 64 bit machine. This is a unit that generates all constants that have a contiguous sequence of '1'. How many bits would it take? How would you encode it.

We encode the constant using the starting and ending location of the string of '1's. How would you build the hardware to decode this. You can use a normal decoder or a thermometer decoder.

How would you build a thermometer decoder. Don't worry about speed at first, just get the logic right.

How might you make the decoder faster. Can you estimate its speed?

At 10:43 AM 2/15/01 -0800, you wrote:

> I am still waiting for you to submit your Quals Question either by hard copy
> or email.
> Please try to submit by 2/23/01.
>
> Happy Thursday,
> Diane

X-Sender: horowitz@vlsi.stanford.edu
Date: Wed, 13 Mar 2002 22:26:46 -0800
To: shankle@ee.Stanford.EDU
From: Mark Horowitz <horowitz@Stanford.EDU>
Subject: Quals question (finally)
Cc: penny Chumley <penny@csl.Stanford.EDU>

The quals question was based on building the interface to a dot-matrix display

1. Assume you have an array of 8x128 lights. If you had a wire to control each light how many wires would you need?

1024

2. Clearly that is too many wires. If we want to reduce the wires what can we do?

Need to use memory in the display, and use the fact that the eye is slow. So scan out image a column at a time. This will take 8 wires (one for each row) and either 7 wires for the columns (decode locally), or just two wires -- one for the clock and one for reseting the counter.

3. Now assume that I want to have an analog display rather than just turing the lights on or off. How could I do that?

Simplest solution is to drive an analog voltage on each row line. The light on that row's amplitude will be set but that control.

4. Assume that the actual picture elements are intrinsically digital. Can we still create an analog display?

Sure, use pulse width modulation. Pulse the row so the pulse width is proportional to the desired intensity

5. How does the clock on my desk work?

X-Sender: horowitz@vlsi.stanford.edu
Date: Thu, 06 Feb 2003 16:31:04 -0800
To: Diane Shankle <shankle@ee.Stanford.EDU>
From: Mark Horowitz <horowitz@Stanford.EDU>
Subject: Re: Quals Question 2003

Quals question:

Have a picture of an inverter driving a capacitor to Gnd. Also on the board is a simple model of the current through a transistor, Ids= k(Vgs -Vtheff)

Look at the power supply current, where does the current flow?
What is the energy comsumed in this circuit
Capacitor is lossless. Where is the power dissipated
Write an equation for delay
Can you reduce the supply and not change the delay?
To minimize power, what should the threshold be?
What is the ratio of the static to dynamic power?

At 10:23 AM 1/31/03 -0800, you wrote:

> Quals Question 2003
>
> Please send a copy of your Quals Question or you can email the question.
> Thanks,
> Diane Shankle
> Packard 165
> MC:9505
> (650) 723-3194
> Fax:(650) 723-1882

Date: Fri, 27 Jan 2006 21:43:25 -0800
To: Diane Shankle <shankle@ee.Stanford.EDU>
From: Mark Horowitz <horowitz@stanford.edu>
Subject: Re: Quals Meeting Time Change Please see below!

Quals questions:

Basic setup: We have a new type of transistor called QMOS, which has no leakage current when it is off, and roughly the same one resistance as a normal MOS device when turned on. The big advantage of QMOS is that it operates at 100mV, and nicely turns on when Vg is about 30mV. The downside is that to conduct current a nano-structure must move a nano distance and that takes 1-2ns. So the current is delayed by this amount of time. The input cap is 2fF/u, and assume the output resistance is 10K/sq.

Is this technology interesting? Why?

How should you think about logic design if this is your implementation technology. What are the rules of thumb you should use? What kinds of logic gates should you build?

Mark

At 04:23 PM 1/27/2006, you wrote:

> Quals Meeting
> Tuesday, January 31st.
> 4:30 P.M.
> CIX-X AUD
>
> Coffee,Tea and Cookies will be served before the meeting.
>
> Please send me a copy of your Quals Question either by email or a
> hard copy to the address listed below!
>
> Happy Friday,
> Diane
>
> --
>
> Any other questions feel free to call me!
>
> Diane Joan Shankle
> Tel: (650) 723-3194
> FAX: (650) 723-1882
> shankle@ee.stanford.edu
> Stanford University
> Electrical Engineering
> Student Services
> Packard Building Rm. 177
> Stanford,CA 94305-9505
> http://www-ee.stanford.edu

Quals Questions 2007

From: Mark Horowitz <horowitz@stanford.edu>

Here was my quals question:

Basic setup: I am asking people how to build the bypass network for a simple processor. This is looking for them to understand what operations are required, and then to explore how to build the comparison networks and then the priority encoder

If the value is available early, why isn't it written back when it is created

In a 5 stage pipeline, how many value need to be bypassed.

What does the input mux look like ? Does it depend on the register file design?

You need to create the control logic for the mux. What logic needs to be performed

Design both the match logic, and the priority encoder

What happens if the machine has a fixed zero register

How does the complexity change with increasing issue width?

Mark Horowitz

I have a clock in my office that uses an oscillating wand with LEDs on it that it uses to display the time. It contains a microcontroller that runs the clock.

1. How would you use the controller to control the freq and amplitude of the wand oscillator.

2. How do you sync the timing of the display to the position of the wand (where does the sensor need to be place).

3. Please make the timing of the dots on the display all the same size.

Mark Horowitz

I have a clock in my office that uses an oscillating wand with LEDs on it that it uses to display the time. It contains a microcontroller that runs the clock.

1. How would you use the controller to control the freq and amplitude of the wand oscillator.

2. How do you sync the timing of the display to the position of the wand (where does the sensor need to be place).

3. Please make the timing of the dots on the display all the same size.

EE Quals Questions 2012 - Mark Horowitz

The goal of this question was to get to a point where the student did not know the answer off the top of their head, and needed to figure it out. It did not matter much where the point occurred, the score really depended on how the student solved a new problem.

This question is going to look at the hardware needed to compress a video stream.

1. Video consists of a stream of picture. Often motion estimation is used to compress frames. Why is estimating motion useful in compression?

2. Show a picture of an image block (8x8 pixels) being compared against many different 8x8blocks of pixels. Ask about the trade-off in choosing the size of the comparison region.

3. The actually computation is a funny one. It is not a squared error metric $(a-b)^{\hat{}2}$, but rather the sum of absolute differences |a-b|. What practical reasons might have favored this metric

4. If you create an implementation on a simple processor, it runs to slowly, and takes too mch energy. What can you change, to either the hardware or the algorithm, to make this computation more efficient.

Mark