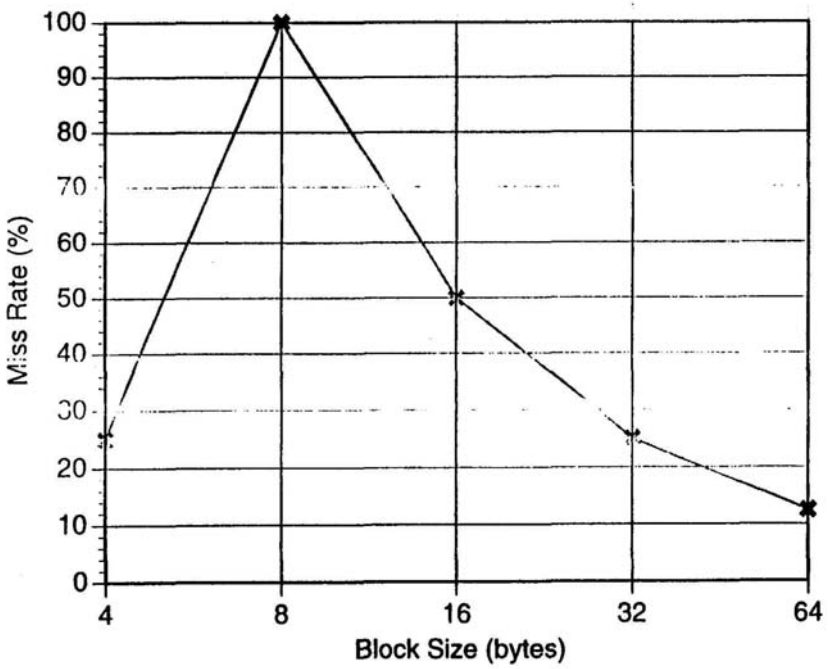
Cache

16384 bytes
Fully associative
LRU replacement

Application

```
int x[8192], y, i, j; /* 4 byte integers */

for (i = 0; i < 4; i++)
   for (j = 0; j < 8192; j += 2)
        y = x[j];
```



Q: Graph the miss rate vs. block size for the cache and application.
A: Shown on graph

Q: What types of locality are being exploited at the various block sizes?
A: 4B-temporal, 8B-none, 16B–64B-spatial

Q: What types of misses occur at the at the various block sizes? Use 3-Cs model
A: 4B-compulsory, 8B–64B-compulsory, capacity. No conflict misses.

Q: Which block size provides the best performance? Assume 4B wide refill bus.
A: Depends on latency (LA) and bandwidth (BW) of cache refill. To achieve higher performance with a 64B block than with a 4B block: LA > 60B/BW.