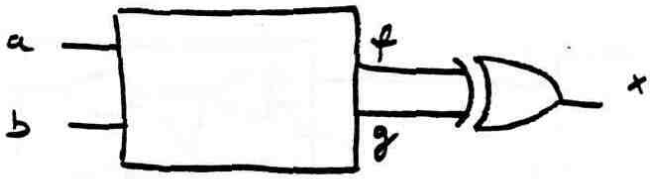
PH.D. QUALIFYING EXAMINATION 1994 / SOLUTIONS

Topic: Logic design and Boolean algebra

NOTE: We are dealing with combinational circuits only.

1) An engineer claims correctly that he can replace the XOR gate in the circuit below by a NAND gate.
Can you give an example of a circuit that can fit in the box?



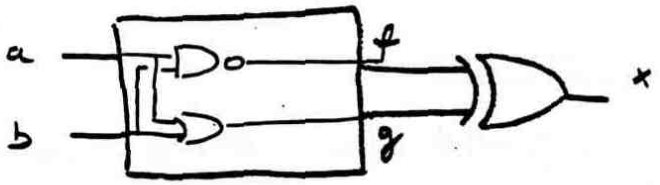
Compare XOR to NAND

a	b	XOR	NAND
0	0	0	1
0	1	1	1
1	0	1	1
1	1	0	0

XOR differs from NAND on input pattern 00

The network in the box should not yield 00

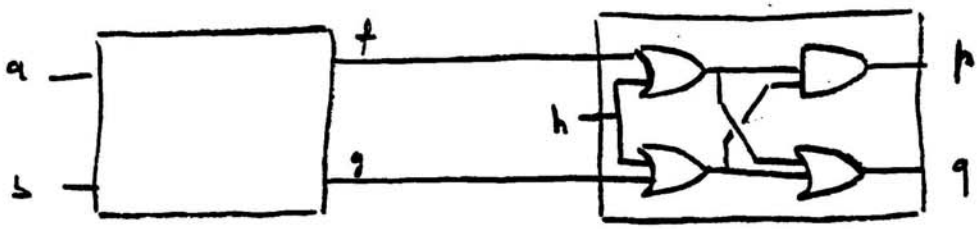
Example



2) Is the circuit in the box unique?
How can you characterize the class of circuits that fit the box?
Hint: consider functions f(a,b) and g(a,b).

$$f + g = 1$$

3) The circuit in the box is driving another circuit as shown below. What are the possible output patterns in terms of variables (p,q)?



$$p = (f+h)(g+h) = fg + h$$
$$q = (f+h)+(g+h) = f + g + h$$

Since $f + g = 1 \implies q = 1$

p can be $1, 0$

Output vectors are $\begin{bmatrix}1\\0\end{bmatrix}$ $\begin{bmatrix}0\\1\end{bmatrix}$

4) Assume that f and g can take any value, what are the possible output vectors?

Vector $\begin{bmatrix}0\\0\end{bmatrix}$ is possible when all inputs are 0

Vector $\begin{bmatrix}1\\0\end{bmatrix}$ is NOT possible because

$$fg + h = 1 \implies f + g + h = 1$$

Date: Wed, 1 Mar 2006 17:22:45 -0800
From: "Subhasish Mitra" <subh.mitra@gmail.com>
To: "Diane Shankle" <shankle@ee.Stanford.EDU>
Subject: Re: Reminder Quals Question 2006

Hi Diane,

Here are the questions.
-Subhasish

Suppose you have a system where bits are coming in serially, 1 bit at each clock cycle. With each bit coming in, you create a binary number where the last received bit is treated as the Least Significant Bit (LSB) and so on. For example, suppose that everything is initialized to 0. The first bit that comes in is 1 – the number is 1; the second bit received is 0, so the number is now "10" = 2; the third bit received is 1, so the new number in the third cycle is "101" = 5, and so on. At each clock cycle the system output is 1 if and only if the number at that clock cycle is divisible by 7.

Create a state diagram for the corresponding sequential circuit.

What is the minimum number of states you can have?

How will you implement a similar circuit for which we want to find out if the number at each clock cycle is divisible by 28?

What happens if we want to find out if the number at each clock cycle is prime?

On 3/1/06, Diane Shankle <shankle@ee.stanford.edu> wrote:
> Hi,
>
> Reminder!
>
> Please send me your Quals question.
>
> Thanks and Enjoy Your Day,
> Diane
>

Here are my Quals 07 questions.

Thanks

We use a number system S where the positions represent
1, -2, 4, -8, and so on, and each entry can be 0 or 1.
1. How will you convert a number in S to binary without converting to decimal?
2. How about binary to S without converting to decimal?
3. How will you add two numbers in the S system without going through the binary system?
4. Is there a problem with the S system?
5. Are all numbers in the S system unique?

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2009 Qualifying Exam Questions
S. Mitra

1.What is the difference between a combinational and a sequential circuit?
2. Consider a ripple carry adder with an End Around Carry (i.e., last carry out fed back into first carry in). Is this a combinational or a sequential circuit? Under what circumstances?
3. Given an arbitrary circuit with feedback loops, how will you analyze whether the circuit is combinational or not?
4. How will you perform static timing analysis for the ripple carry adder with End Around Carry feedback?
5. Can you extend such a static timing analysis methodology for general designs?

S. Mitra

2010 EE Qualifying Exam Questions

1. What is the difference between a latch and a flip-flop?

2. Helped student draw a gate-level MUX and a simple D-latch out of that MUX. OUT = OR(A, B), A = AND (D, CLK), B = AND (OUT, E), E = NOT(CLK) Does the above circuit work correctly? Why not?

3. How will you fix it?

4. Suppose that you are given a flip-flop-based FSM. I claim that you can automatically convert the circuit into one where there are no flip-flops / clk or any sequential element (i.e., replace each flip-flop by a wire) without changing the combinational logic function. How can you do that? Assume that for each gate there is a single delay value associated with that gate.

5. You can have trillions of paths if you plan on path delay balancing. What's a scalable way to do this?

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Name

Start time

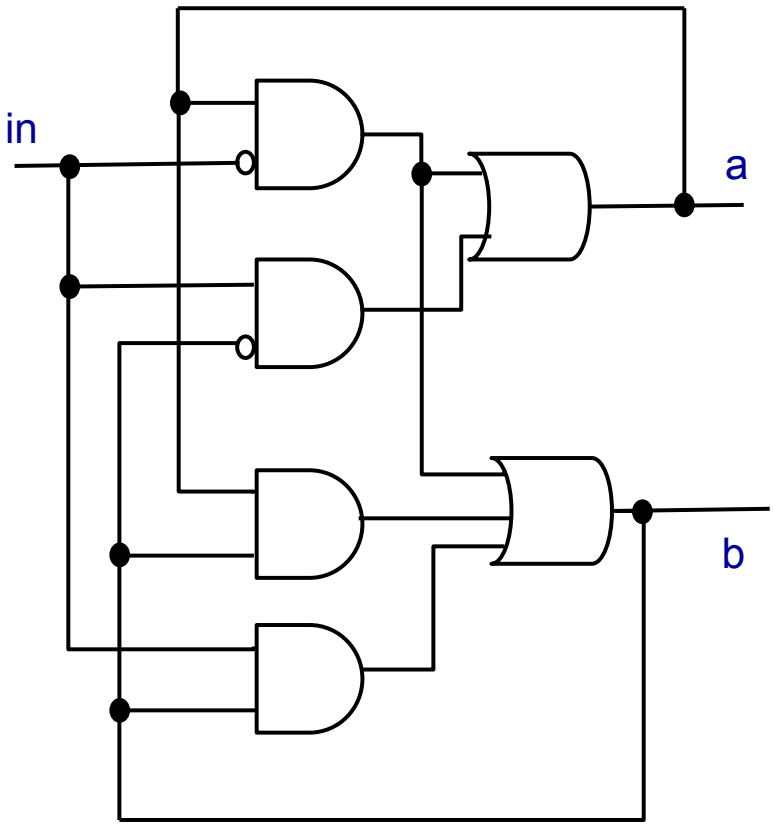
1. What are hazards in a logic circuit?

2. Is there a hazard problem for output “a” of the circuit below?

3. If yes, please fix it. If not, why not?

4. Is there any other hazard problem in this circuit? Which ones? What’s the fix? Is it possible to fix those problems without inserting delays?

Name



State	Code b a	Next in = 0	Next in = 1
A	0 0	(A)	B
B	0 1	C	(B)
C	1 1	(C)	D
D	1 0	A	(D)

Truth table for a

b a \ in	0	1
0 0		1
0 1	1	1
1 1	1	
1 0		

Truth table for b

b a \ in	0	1
0 0		
0 1	1	
1 1	1	1
1 0		1