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To: "Diane J. Shankle" <shankle@sierra.stanford.edu>
Cc: horowitz@chroma.stanford.edu
Subject: Re: Last Chance
In-Reply-To: Your message of Tue, 02 Mar 93 13:32:53 -0800.
<CMM.0.90.0.731107973.shankle@Sierra.Stanford.EDU>
Date: Wed, 03 Mar 93 08:35:47 PST
From: Mark Horowitz <horowitz@chroma.stanford.edu>

Quals Question: architecture

1. You are designing a computer and need to build a function unit that checks to see if the value on the source bus is zero. How would you build the function unit in CMOS?

Answer:
There are two ways of solving this problem. No matter which you choose I would ask for the other answer as well.

The circuit that is needed is a 32 input NOR gate, since its output will be 1 only if all the inputs are zero. This can be built by using a precharged gate will 32 parallel transistors, a precharge pullup, and a single pulldown device. For this gate to work, the inputs must be stable when the evaluate transistor turns on. A pseudo nMOS gate, with a single pMOS static load and 32 pulldown nMOS devices would be ok for this part of the problem as well.

The other solution is to use static CMOS gates. Since there is a series stack of transistors that is proportional to the number of inputs, each gate must have a limited fanin. Let's set the fanin to be 2. One can use a tree to build a 32 input out of 2 input gates. The first layer is 16 2input NOR gates. Since the outputs are inverted, the next stage must be NOR with inverted inputs, which are NAND gates. There are 8 or these gates. The next level in the tree is then 4 NOR gates, and this is followed by 2 NAND gates, and the final NOR gate. The key was to realize that you need to flip from NORs to NANDs to handle the inversions.

2. How does the delay of these structures scale with the number of inputs.

For the precharge gate, the resistance of the worst-case pulldown is constant. The cap of the output node will increases linearly with the number of inputs, since each additional input adds some diffusion cap to the output node.

In the tree, the critical path is the depth of the tree. This is log2 of the number of inputs. Thus, since the delay of all the 2input gates should be similar, the delay is proportional to the log2 of the number of inputs.

3. Which of the two structures is faster? Does the answer depend on the number of inputs?