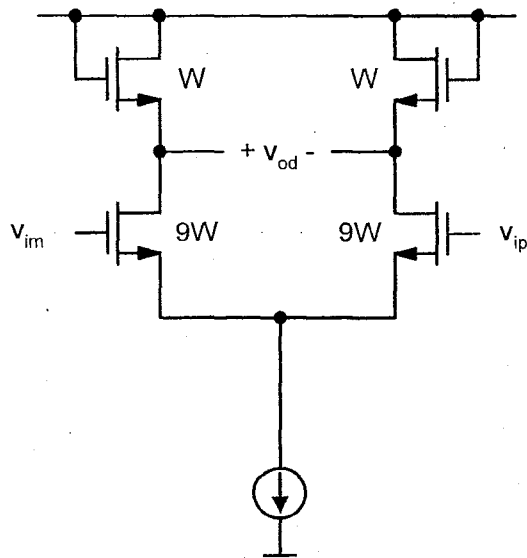
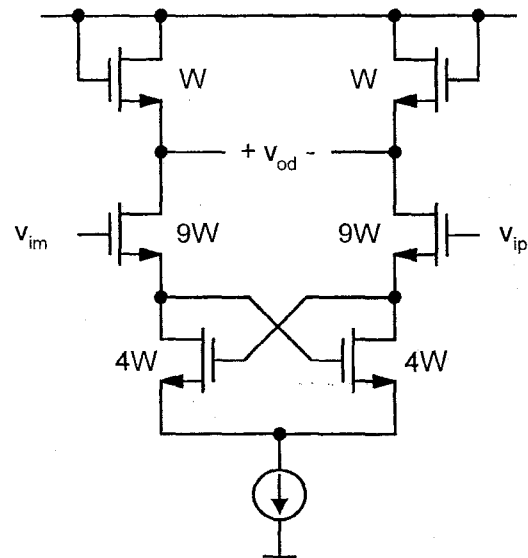


In the circuits below, neglect second order effects such as finite output resistance and body effect and assume ideal square law behavior. All devices have the same channel length and operate in the forward active region.



(a)



(b)

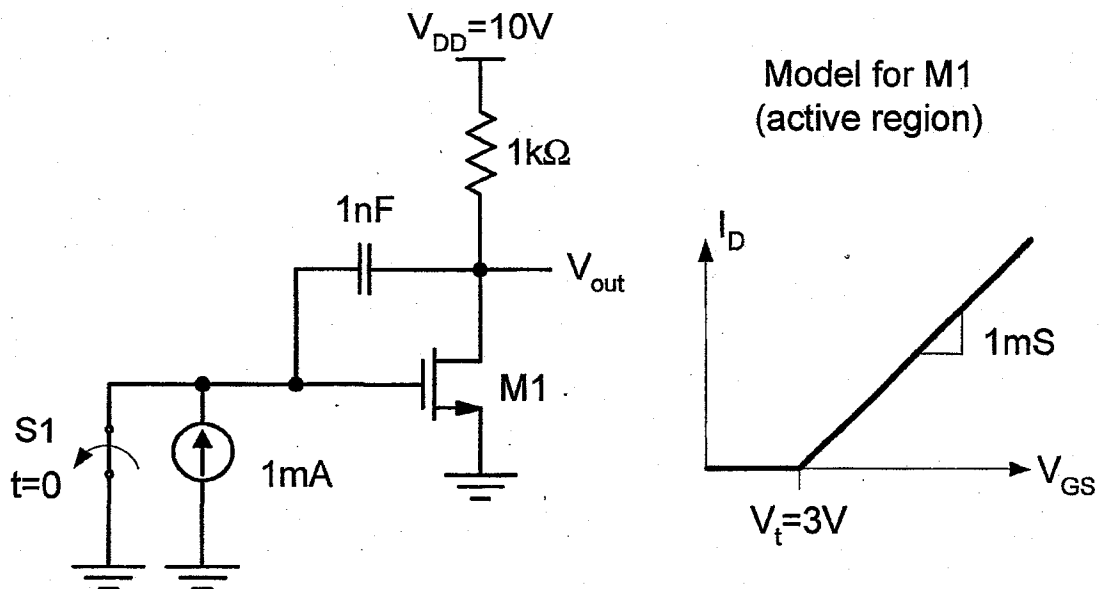
- What is the low frequency differential voltage gain in the above circuits?
- Discuss potential issues, subtleties and disadvantages of circuit (b).

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Neglect all capacitances, except the explicitly drawn 1nF capacitor. S1 is an ideal switch; it is closed for $-\infty < t < 0$ and open for $t \geq 0$.

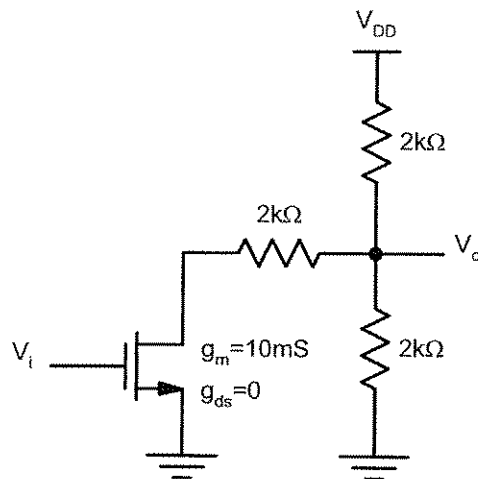
Sketch $V_{out}(t)$, calculate and mark pertinent breakpoints.



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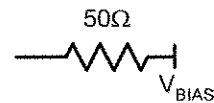
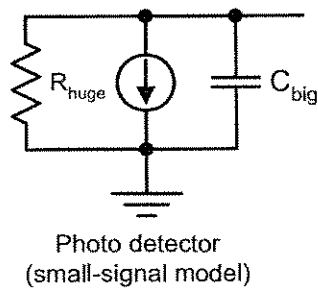
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For the circuit below, calculate the low-frequency small-signal gain $A = v_o/v_i$. The MOS device is biased such that it operates in the active region.



Design a broadband circuit that interfaces a photo detector (as shown below) to a 50Ω load. The detector provides a short circuit current on the order of $100\mu\text{A}$; the desired voltage swing across the load is on the order of 100mV .

Available components: transistors, resistors, capacitors and independent voltage and current sources for biasing (no ideal op-amps). Provide a first-order expression for the bandwidth of your circuit.

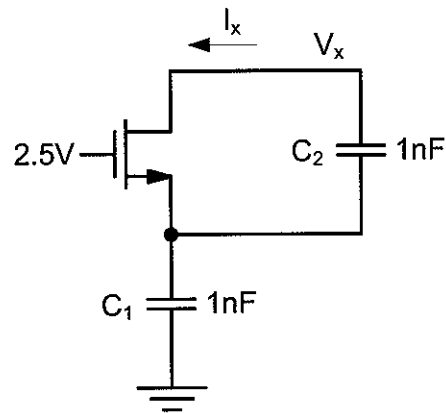


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For the circuit below, sketch V_x and I_x versus time. Annotate pertinent break points and slopes.

At $t=0$, the initial voltages across C_1 and C_2 are 1V and 3V, respectively. Device parameters:
 $V_t=0.5V$, $\mu C_{ox}W/L = 1mA/V^2$.



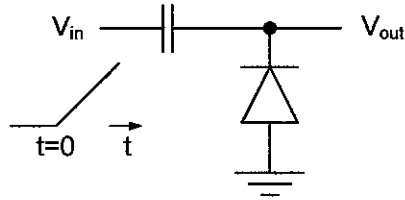
Consider a CMOS circuit in which the features and voltages are scaled by a factor S such that all electric fields remain constant. For this case, it can be shown that all performance parameters of the circuit improve by a factor of S^k .

Determine the values of k that apply to integration density, speed and energy per operation.

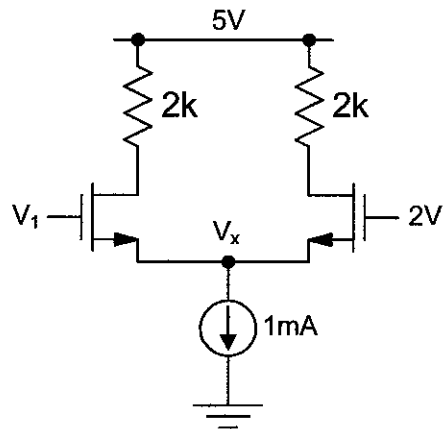
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1. The circuit below is driven by a voltage ramp that increases linearly with time. Sketch (qualitatively) $V_{out}(t)$, assuming $V_{out}(0) = 0V$.



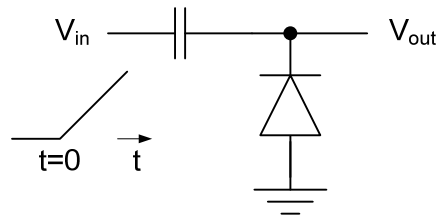
2. For the circuit below, sketch the voltage V_x as a function of V_1 , ranging from 0...5V. The MOSFETs obey the ideal square law equation with $\mu C_{ox} W/L = 4\text{mA/V}^2$, and $V_t = 1\text{V}$.



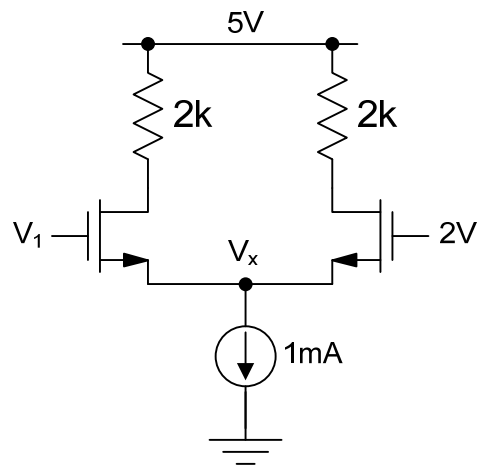
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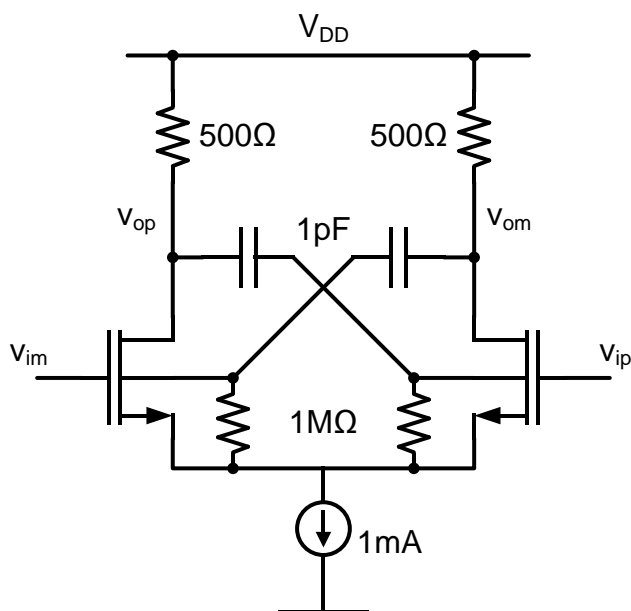
1. The circuit below is driven by a voltage ramp that increases linearly with time. Sketch (qualitatively) $V_{\text{out}}(t)$, assuming $V_{\text{out}}(0) = 0\text{V}$.



2. For the circuit below, sketch the voltage V_x as a function of V_1 , ranging from 0...5V. The MOSFETs obey the ideal square law equation with $\mu C_{ox}W/L = 4\text{mA/V}^2$, and $V_t = 1\text{V}$.



In the circuit below, all MOSFETs obey the ideal square law equations. The transistors are sized such that $|V_{GS}-V_t| = 200 \text{ mV}$. The backgate transconductance is $g_{mb} = 0.2 g_m$. Ignore all device capacitances.



1. Sketch the frequency response (magnitude only) of the differential small-signal voltage gain $(v_{op}-v_{om})/(v_{ip}-v_{im})$.
2. Is this circuit stable? Discuss in terms of gain and phase margin, as applicable.
3. Can this circuit work with the 1-pF decoupling capacitors shorted? Discuss potential issues.