Question 2

Consider a cache for a FIFO queue in a network switch, router or network interface card, built from the same SRAM and DRAM.

(a) Explain how it works.

(b) How large does the block size, *b*, need to be so that it won't overflow?

(c) How about *c*, so that the "head cache" won't underflow?

(d) What problems do we run into if we want to build a cache for *N* FIFO queues, instead of just 1?