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Computer Architecture and Logic design

We will be looking at the question of wire delay in an IC. To solve this problem we will model delay using simple RC models.

I present the student with an example wire 1u wide, and 1mm long. It has a resistance of 100ohms and a capacitance of .13pF

1. How does the resistance and capacitance of the wire vary with length
   (both are linear)
2. How does the delay vary with length
   (quadratic)
3. What is the delay of a 10mm wire.
   1/2 RC = 650ps

4. If that is too large how could you reduce it?
   wire wider, repeaters

5. Shown on the board is how the capacitance of the wire varies with width. At 1u = .13pF, 2u=.16pF, 3u=.19pF. Does this data make sense? What does the extrapolated value of 0.1pF at zero width represent?
   Makes sense. 0.1pF is the fringe capacitance

6. Roughly how much faster can you make the wire by making it wider?
   4 times

7. Why does adding buffers speed up the wire?
   breaks the increasing resistance with length

8. What parameters should you optimize in a wire with repeaters to minimize delay.
   distance between inverters and the inverter size

9. Write the delay equation for one segment of a buffered wire

RC delay model, repeater, fringe capacitance, buffer