Quals Questions 2007

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Here was my quals question:

Basic setup: I am asking people how to build the bypass network for a simple processor. This is looking for them to understand what operations are required, and then to explore how to build the comparison networks and then the priority encoder

If the value is available early, why isn't it written back when it is created

In a 5 stage pipeline, how many value need to be bypassed.

What does the input mux look like ? Does it depend on the register file design?

You need to create the control logic for the mux. What logic needs to be performed

Design both the match logic, and the priority encoder

What happens if the machine has a fixed zero register

How does the complexity change with increasing issue width?