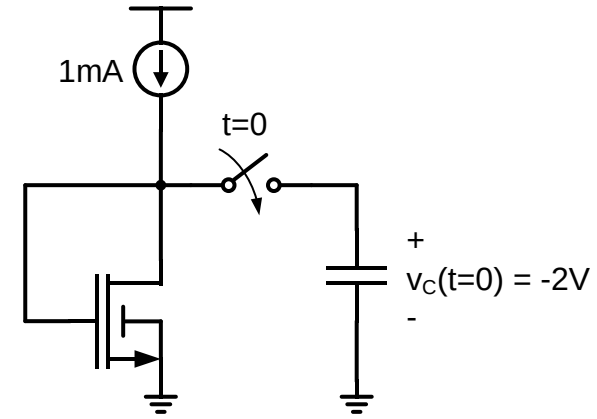
Name:	Stanford EE Quals 2015 Murmann

Sketch $v_C(t)$ versus time. Ignore the capacitance of the MOSFET and assume that it obeys the ideal square law model.



The op-amp in the circuit below has a DC gain of 80dB and two left half plane poles at 1 rad/s.

a) Sketch the magnitude of the circuit's loop gain.
b) Is this circuit stable? If yes, what is its phase margin assuming RC = 10ms?