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Date: Mon, 24 Jan 2000 23:41:10 -0800
To: Diane Shankle <shankle@ee.stanford.edu>
From: Mark Horowitz <horowitz@stanford.edu>
Subject: Re: Reminder: Quals Questions were due on Friday, 1/21/200

Here is my quals question

We are looking at a machine that has variable length instructions. Assume that the top two bits indicate the instruction length. 0- indicates 2B instruction, 10 is 4B and 11 is 5bytes.

1. Show the logic for the length decoder. (it has 3 outputs)

2. Show the logic for getting the instruction data aligned for the next instruction decode

3. Assume you want to build a machine that can issue three instructions each cycle. Show how you would connect 3 instruction decoders to the register that contains the instruction bytes. Don't worry about delay, but show the critical path

4. Now assume that decoding the instruction length is complex, like in the x86 instruction set. What techniques could you use to speed up the implementation. You have as much hardware as you need.

5. Would making the long instructions 6 bytes make the decoding easier?