2007 PhD Quals Question, James Harris

1. Si MOSFET

A. Can you sketch the cross-section of a MOSFET?
B. Below your sketch, can you sketch the energy band diagram at thermal equilibrium with no gate or drain voltage?
C. Using a different color, can you show how the band diagram is changed if I apply a sufficient gate bias to reach inversion under the channel?
D. Can you now show how the band diagram is changed when I apply a drain bias?
E. Draw the drain I-V characteristic and briefly describe the 2 or 3 most important regions of the I-V characteristic and how these are related to the three band diagrams you've sketched.

2. Single Electron Transistor

The above characteristics look pretty useful, so I'm going to SNF and fabricate some of these devices. I go down to the e-beam system to make very small gate length devices and find my line drawing skills are pretty good, but my alignment skills are somewhat lacking and so I have produced a series of devices in which the gate length is less than the source-drain spacing, so draw that on the cross-section schematic of your earlier device to make sure we are both clear what kind of device my inept skills have produced.

A. Would this device work by the normal processes by which we describe MOSFETs? Why not?
B. If I apply a gate bias, can I still create an inversion layer under the gate of this device?
C. Is there anything different about the inversion layer in this device and the normal MOSFET?
D. If I apply a drain bias to this device, would I expect to get any drain current? By what mechanism?
E. I made 25 of these devices in SNF with gate lengths from 100nm down to 5 nm and they all had the same degree of mis-alignment at source and drain, i.e., the barriers at each end were all exactly the same. As I measure the drain I-V characteristics of these devices, would I expect to see anything different about the characteristics as the gate length became shorter and shorter?
F. What do you imagine the characteristics might look like compared to the normal MOSFET characteristics and what would this be due to?
G. If I said that I measured a voltage step of 25mV for the tunneling of a SINGLE electron onto the inversion layer island of my device, how might you go about estimating how small such an island would have to be?