# Quals Question
# Prof. Olukotun

Computer Architecture

Q: What are precise exceptions?

A: All instructions before exception PC have been execute d and have modified machine state
All instructions following exception PC are unexecuted
The instructions following the exception PC are restartable

Q: Give an example instruction that must be handled precisely

A: Page fault

Q: How do you implement precise interrupts in a simple instruction pipeline that has in-order instruction completion?

A: Post exception in a status register that can be checked at a common commit point. At the commit point in the execution pipeline all interrupts must have occurred but the state to the machine must not have been modified. In a DLX style pipeline this point is just before the write-back stage.

Q: How do you implement precise interrupts in a machine that has out-of-order instruction completion?

A: A possible answer is use a reorder buffer.

Q: How does the reorder buffer work?

The reorder buffer is FIFO queue that is placed between the output of the functional units and the write-back port of the register file. It keeps the register file in a precise state. The entries of the reorder buffer are en queued when instructions are issued. Each entry contains the following fields: destination register, result value, PC, interrupt status, valid. Instructions are removed from the head of the queue when they have valid result values after they have written back their results. Exceptions are checked for an instruction when the instruction reaches the head of the queue. If an instruction causes an exception all entries behind it in the reorder buffer are discarded and do not write back their results. Bypassing of result values from the reorder buffer is required for maximum performance.