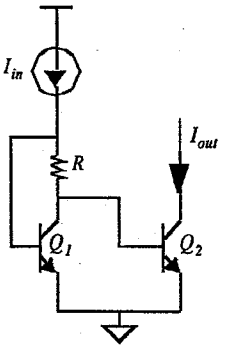
Name: Tom Lee **Solutions** Ph.D. Qualifying Examination 2007

STANFORD UNIVERSITY
Department of Electrical Engineering

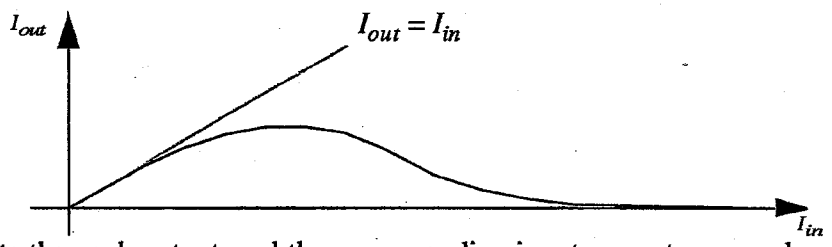
Bob Widlar is often considered to be the father of analog IC design. The following current source is but one of his many ingenious circuits (from the LM101A op-amp):

Assume that all components are ideal.



Plot the output current as a function of input current. Label any features of relevance.

Ans: A couple of quick observations enable a rough sketch. First, $V_{BE2} < V_{BE1}$ for any nonzero I_{in}. So, $I_{out} < I_{in}$ for all $I_{in} > 0$. There is a range of I_{in} (to be defined later) over which the drop across R is negligible, and thus over which I_{out} is approximately equal to I_{in}. But, the drop across R grows linearly, while V_{BE1} grows only logarithmically. So, V_{BE2} eventually decreases. At very high I_{in} the drop across R is large enough that V_{BE2} is essentially zero (V_{CEsat1} could be taken as ideally zero), and the output current heads to zero. The corresponding plot therefore looks roughly like this:



To compute the peak output, and the corresponding input current, we need an equation or two:

$$\left(I_{in}R = V_{BE1} - V_{BE2} = V_T \ln\frac{I_{in}}{I_{out}}\right) \Rightarrow I_{out} = I_{in}\exp\left(-\frac{I_{in}R}{V_T}\right). \qquad \text{(EQ 1)}$$

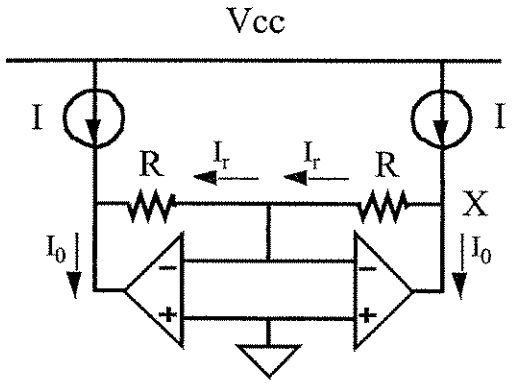
This equation is readily solved for the coordinates of the peak: $I_{in} = V_T/R$, $I_{out} = V_T/eR$. This circuit, known as a *peaking current source*, is useful because its output current is independent of input current (to first order), provided that the nominal input current is set to V_T/R. The circuit then produces an output current that is a factor of e smaller than that nominal value, even if the input current should deviate a bit from the nominal. Several may be combined to broaden the flatness, in a manner similar to filter design. Finally, the same topology functions for MOS implementations, although the numbers differ.

SOLUTIONS to Prof. Tom Lee's Ph.D. Qualifying Exam Question, 2008

Recall that an ideal operational transconductance amplifier (OTA) is simply a voltage-controlled current source (i.e., a transconductor, hence the name), in which the transconductance, bandwidth, output impedance and output voltage range are all infinite, and the input currents are zero.

Suppose we connect two identical, ideal OTAs in the following configuration:

FIGURE 1. OTA circuit



The two current sources shown are simply static (DC) sources.

What is the (small-signal) resistance seen between node "X" and ground? (As with most problems, there are many, many ways to solve this one. If you need a hint, consider exploiting the circuit's topological symmetry).

SOLUTION: We first make a couple of quick observations: The DC current sources can be removed right away for small-signal analysis. Next, the inverting terminals are at ground potential, given the assumptions of ideal OTA properties. Also, the matched OTAs are controlled by equal voltages, so their output currents match as well (labeled I_0). Finally, the current flowing in the two resistors must also be equal, because no current flows into the inverting terminals of the OTAs. These three observations allow a rapid deduction of the answer.

To discover resistances, the canonical method is to **drive the port in question with a source**, compute the response, and simply take the ratio of voltage to current. Here, suppose we arbitrarily drive node X with a test current source I_T. This current splits in an initially unknown way between the right-hand resistor and the OTA output. Call the current through the former I_r and that through the latter I_0. Now, the left-hand resistor carries the **same current** I_r. The left-hand OTA's output current is thus also I_r, because the left-hand resistor's (small-signal) current can only go through the OTA. So we now know that $I_r = I_0 = I_T/2$. That is, the test current applied at X splits *equally* between the resistor and the OTA. The voltage induced at node X is thus simply $(I_T/2)R$, because the other end of R is connected to a virtual ground. The equivalent load seen at X is just the ratio of voltage induced to current supplied, and is thus **R/2.**

So, what about the hint? Another way to solve this problem is to apply a differential excitation (say, I/2 into X, and I/2 out of its counterpart on the left-hand side), and then a common-mode excitation (I/2 into both nodes). The perfect symmetry of excitation and circuit in each case facilitates analysis. One need only sum the individual voltages induced at X. This method requires more steps, but depends much less on intuition, because the symmetry of the circuit AND excitations allows you to use the time-honored tricks of folding or bisecting, etc. to compute the induced voltages with a simplified circuit.

Common mistakes: The following is a partial list of widespread errors:

Almost everyone chose to retain the static DC current sources when computing small-signal resistance. Failure to remove these sources unnecessarily clutters derivations, and inhibits getting to the answer. When doing small-signal analysis, do yourself a favor and begin by setting all independent sources to their zero value.

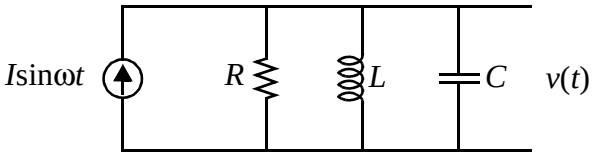
Many students also didn't understand how to identify when something has symmetry. Yes, this *circuit by itself* is symmetrical, but adding the *excitation* required to investigate resistance introduces an asymmetry (the question asks for the single-ended resistance). So, you can't fold or bisect *first*, and *then* compute resistances. This error was disappointingly common. Study the alternate solution method above for an example of how to exploit symmetry.

Another common error was to hand-wave the OTA into irrelevance by saying "it's ideal, with infinite output impedance, so no current flows out of it." The OTA is a *dependent current source*, and is connected here in a feedback loop. Impedances can be modified in non-obvious ways. To avoid tripping up, just *measure* the impedance, as asked. There's no need to guess (and you shouldn't, if your circuit intuition is weak).

Another surprising error was the random grounding of the inverting inputs. Yes, it's a virtual ground, but the key word is *virtual*. It's not a real ground. The virtual ground's potential is indeed zero volts. However, arbitrarily adding a wire from this node to real ground then introduces a spurious branch through which currents can flow. It also deactivates the OTA (you've turned off the control voltage). Make sure you understand when and when not adding a wire to ground is correct.

Consider the following circuit:

FIGURE 1. Parallel *RLC* circuit



Assume that the current source has an amplitude of 1A and a frequency of 1rad/s. Assume also that the inductance is 1H and that the resistance is 1kΩ.

a) Suppose that the capacitance is 1F. Sketch the steady-state voltage $v(t)$. Identify the amplitude and frequency (or period). What is the average power dissipated in R?

The component values are chosen to produce a resonance at 1rad/s, at which the inductive and capacitive impedances cancel to contribute a net infinite impedance. The 1A current thus flows through the 1kΩ resistor to produce a 1kV-amplitude sinusoidal v(t). The average dissipation in the resistor is just $I^2R/2$= 500W.

***Common mistake*:** Many students immediately and mechanically started writing node equations and Laplace transformed them (or wrote differential equations and tried solving them directly), instead of thinking about the problem a bit first.

b) Now suppose that, starting from $t = 0$, the capacitance instantaneously decreases by 1% at the voltage extrema. Sketch the voltage $v(t)$, assuming that the capacitance returns to its nominal value at each zero crossing. Make reasonable assumptions/approximations.

Capacitive charge cannot change instantaneously if currents are finite (as they are here). Since Q=CV and Q is continuous, a discontinuous change in C must be balanced by a discontinuous change in V. Here, a drop in C implies a jump in V; the capacitor's voltage therefore increases by an amount Q/ΔC (or ~1%) at each extremum, growing without bound. This behavior is exploited in the parametric amplifier*, of which a child's swing is an example.*

At the zero-crossings of v(t), the capacitive charge is zero, so there is no change in capacitor voltage there.

***Common mistake*:** Many students attempted to deduce the behavior using concepts of shifts in resonant frequency. Now, resonant phenomena are evident only over the order of Q cycles (where Q here is 1000), so deducing circuit responses to perturbations occurring on a per-cycle basis (and here, more often than that) is somewhat of an unnatural act for a resonance-based approach.