Professor Mark Horowitz

Build a decoder for a 256 x 256 memory. The address lines A0 - A7 (and their complements, A0_b - A7_b) are available.

The only components that you can use in your design are inverters and 2 input NAND gates, and 2 input NOR gates.

1. What logic would you use to build the decoder?
   If they have problems with that, suggest that they look at a single wordline first — WL0, and derive the logic function for this WL. If they build a full tree at each gate, need to ask, whether they can share logic ...

2. Having done the logic, how would you layout this design?
   Look for people worrying about the wires. Clearly the final NAND inverter should be next to the wordline, but so should the next level, unless you want to double the wire tracks

3. Assume that inverters would like to have a fanout of 4, and NAND and NOR gates would like to have a fanout of 3. Also assume that each memory cell contributes 10fF to the wordline load. Using these assumptions find the rough sizes of the gates in your decoder (you can measure the gate's size by its input capacitance).