

Since the precharge gate's delay increases linearly with n , and the tree is $\log(n)$, the tree must be faster for large n . The key question is which is faster for small n . I was interested in how students attacked this problem. The precharge gate will be faster, since it has fewer transistors, and that means less input and output capacitance. So the right answer is the precharge gate is faster at small n and the tree is faster for large n .

Does the answer to question 3 give you an idea of how to build a faster 32 input NOR?

Yes, replace the NOR gates in the tree with precharge gates. This could allow you to increase the fanin of these gates, and shorten the depth of the tree while maintaining the same gate delay. The NAND gates in the tree invert the output of the precharge gates, so the inputs to the NAND gates are monotonically rising signals.