Date: Fri, 27 Jan 2006 21:43:25 -0800
To: Diane Shankle <shankle@ee.Stanford.EDU>
From: Mark Horowitz <horowitz@stanford.edu>
Subject: Re: Quals Meeting Time Change Please see below!

Quals questions:

Basic setup: We have a new type of transistor called QMOS, which has no leakage current when it is off, and roughly the same one resistance as a normal MOS device when turned on. The big advantage of QMOS is that it operates at 100mV, and nicely turns on when Vg is about 30mV. The downside is that to conduct current a nano-structure must move a nano distance and that takes 1-2ns. So the current is delayed by this amount of time. The input cap is 2fF/u, and assume the output resistance is 10K/sq.

Is this technology interesting? Why?

How should you think about logic design if this is your implementation technology. What are the rules of thumb you should use? What kinds of logic gates should you build?

Mark

At 04:23 PM 1/27/2006, you wrote:

> Quals Meeting
> Tuesday, January 31st.
> 4:30 P.M.
> CIX-X AUD
>
> Coffee,Tea and Cookies will be served before the meeting.
>
> Please send me a copy of your Quals Question either by email or a
> hard copy to the address listed below!
>
> Happy Friday,
> Diane
>
> --
>
> Any other questions feel free to call me!
>
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