Fabian

Quals Question 2000, Pease

1. Why is the semiconductor industry spending $B's on shrinking the features of IC's?
2. How do the speed and energy dissipated per clock cycle vary with linear dimensions (vertical and horizontal) when the speed is limited by the interconnect load (in a CMOS inverter ckt.)?
3. Why does the energy dissipated per clock cycle not depend upon the resistance when it is only in the resistance that energy is dissipated?
4. By driving the interconnect with a slow ramp instead of a step function can we lower the energy dissipated/clock cycle below CV^2?
5. What fundamental factors (i.e. NOT lithography) limit how far we scale down dimensions of IC's?