To: shankle@ee.Stanford.EDU
Cc: darlene@mojave.Stanford.EDU
Subject: Quals Question.
Date: Sun, 19 Mar 95 13:20:46 PST
From: Mark Horowitz <horowitz@chroma.Stanford.EDU>

Computer Architecture

Here was my quals question:

The question was really to see how students handled dealing with an element that they had not seen before -- a relay. To help them out, I started out with more familar material, CMOS switch logic.

1. Using CMOS switches build a XOR gate

There are many ways to approach this problem, and I didn't really care which was chosen. The easiest is to build the gate from two switches that form a 2:1 mux. The top switch connects when the input A is true and the bottom switch connects when the input A is false. The top switch connects to B_b and the bottom switch connects to B. One could have built the gate out of a 4:1 mux too.

2. Using CMOS switches build an AND gate

Here the best solution is to use the same 2:1 mux solution used above. The top switch connects to B and the bottom switch connects to Gnd. Most students choose to build an AND gate using 4 switches -- two series devices connected to Vdd, and two parallel devices connected to Gnd.

3. Actually I was not really interested in using CMOS switches. I really want to build logic gates out of relays. A relay is an electro-mechanical device, where a current creates a magnetic field which pulls a cylinder into a coil and mechanically changes the switches. The input goes to the coil (one end is connected to Gnd), and this relay has one normally connected switch, and one switch which is normally not connected (so there are 5 terminals to this device). In terms of abstract switches, how would you represent this element?

This relay is a GREAT device. It basically consists of two ideal switches, on connects when the input is 1 (the normally not connected) and the other connects when the input is 0 (the normally connected switch). This means that the relay is like a package of an nMOS and a pMOS transistor. But unlike transistors, there is no problem with threshold drops.

4. Using this relay as a basic element please make an XOR gate.
(I allow them to use inverted signals at first, but the final solution can have only the true value of signals)

Since the relay contain both type of switches, connecting the switch outputs together forms a 2:1 mux. Using another relay it is easy to make an inverter to form B_b from B.

5. Now build an AND gate.

Again use the 2:1 mux and connect B to the normally not connected switch, and connect Gnd to the normally connected switch. (The latter connection is not really needed, see the following questions)

6. In logic built out of CMOS switches the output is not allowed to be left floating. Why?

If an output is left floating, it with retain the previous value,