

EE Quals 2015

Computer architecture and digital design

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Question 1

Draw a 1-bit full adder from 2-input logic gates.

Question 2

Show how you can create a 32bit adder from your 1bit full adder building block.

Question 3

Draw/describe other ways to create a 32-bit adder from a 1bit full adder.

Describe the gate-count/delay tradeoff for each design.