2010 EE Qualifying Exam Questions

1. What is the difference between a latch and a flip-flop?

2. Helped student draw a gate-level MUX and a simple D-latch out of that MUX.
OUT = OR(A, B), A = AND (D, CLK), B = AND (OUT, E), E = NOT(CLK)
Does the above circuit work correctly? Why not?

3. How will you fix it?

4. Suppose that you are given a flip-flop-based FSM. I claim that you can automatically convert the circuit into one where there are no flip-flops / clk or any sequential element (i.e., replace each flip-flop by a wire) without changing the combinational logic function. How can you do that? Assume that for each gate there is a single delay value associated with that gate.

5. You can have trillions of paths if you plan on path delay balancing. What's a scalable way to do this?