The Dark Age of Memory Corruption Mitigations in the Spectre Era

Andrea Mambretti, IBM Research Europe - Zurich
Alexandra Sandulescu, Google (formerly: IBM Research Europe - Zurich)

About us

Andrea Mambretti

System Security Research @ IBM Research Europe - Zurich

PhD in Cybersecurity @ Northeastern University, Boston

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Alexandra Sandulescu

Security @ Google

(work done previously at IBM Research Europe - Zurich)

Background - transient execution

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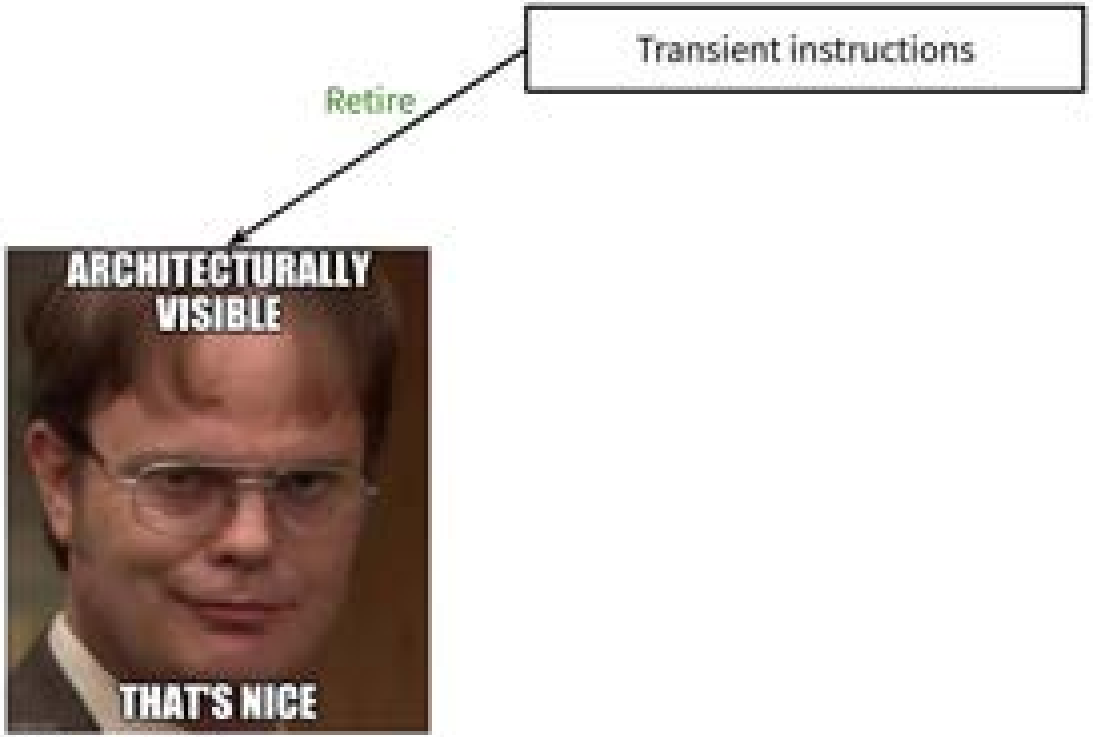

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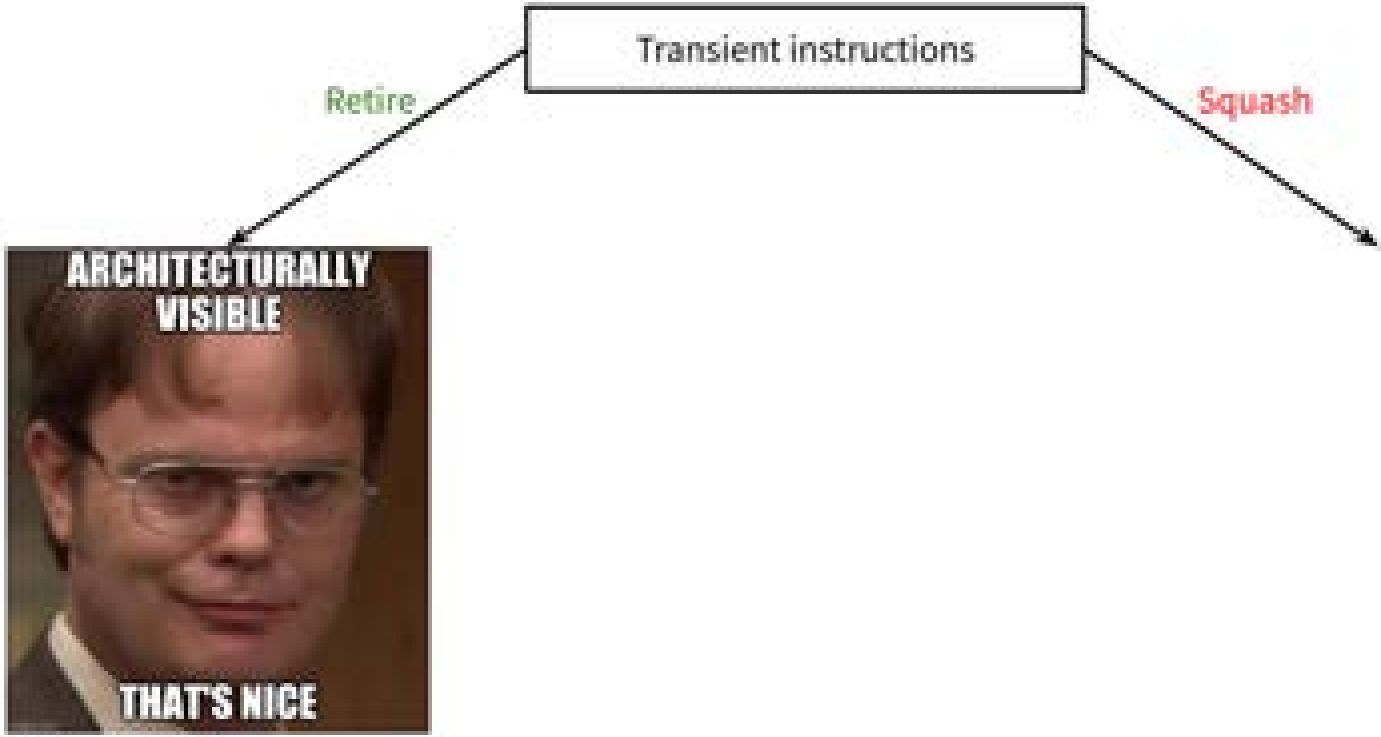

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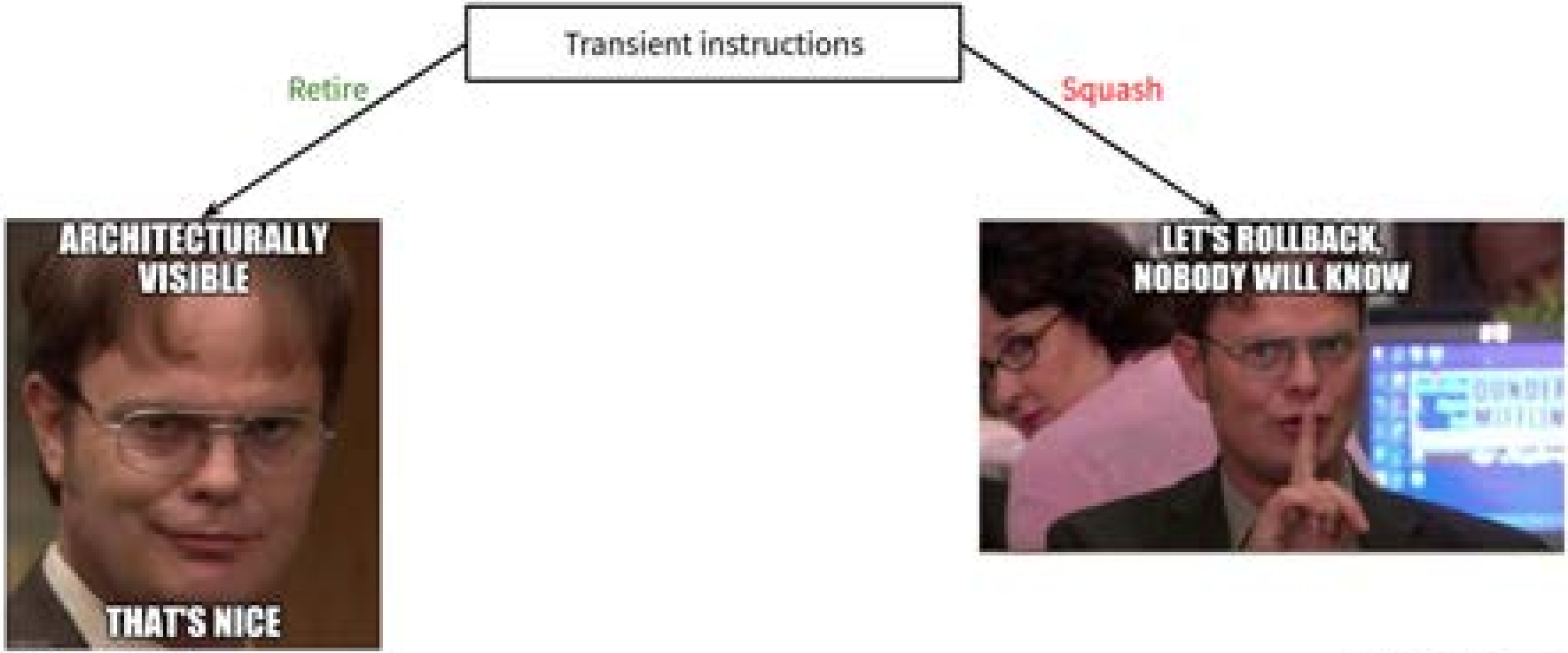

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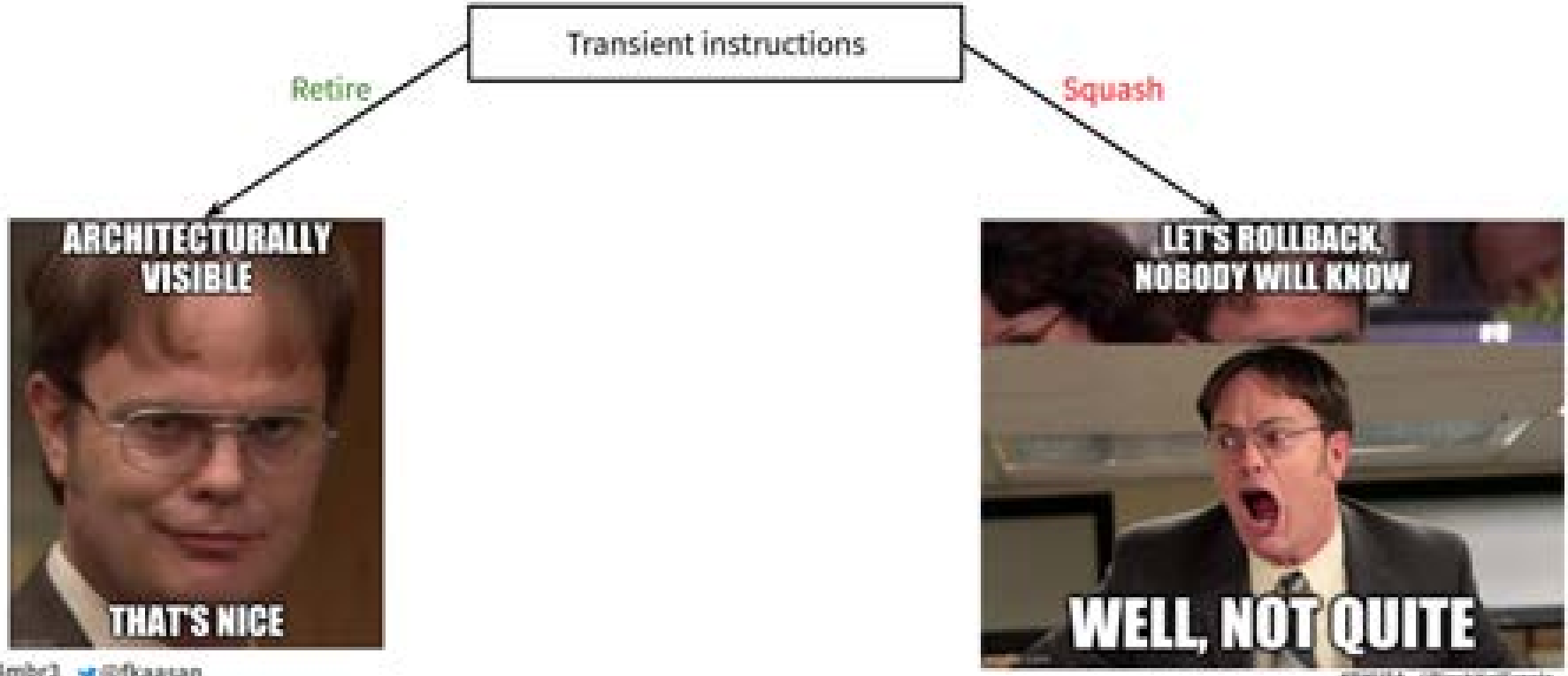

Background - transient execution attacks

Transient instructions

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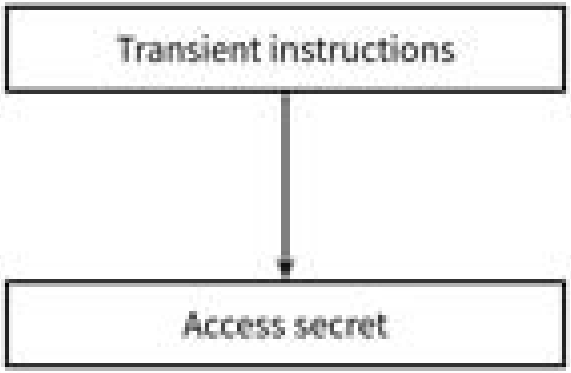

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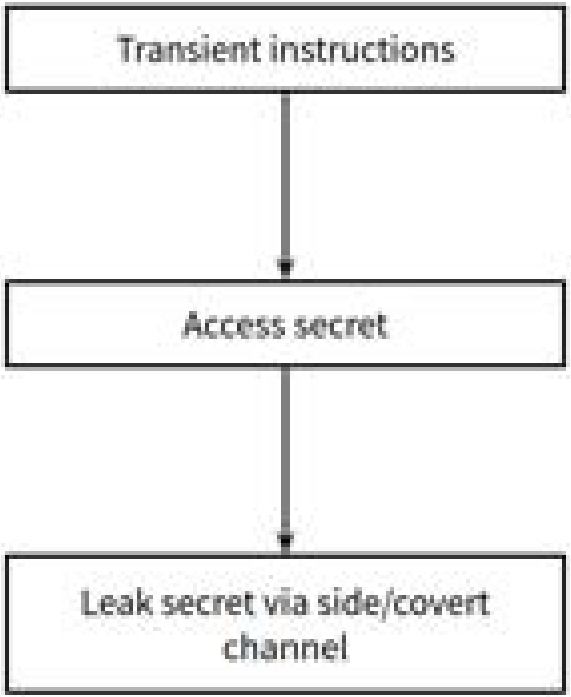

Threat model for Speculative Execution Attacks (SEAs)

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int array1[size_array1];
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if (x < size_array1) {
   array1[x] = val;
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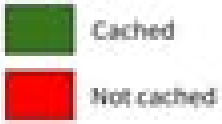


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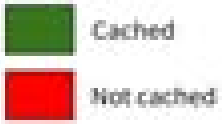


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Speculative Execution Trigger

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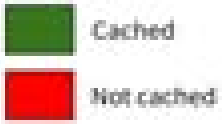


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return;
```

Speculative overflow if x out of bound

saved RET
saved RBP
....
array1[size_array1 - 1]
array1[...]
....
array1[1]
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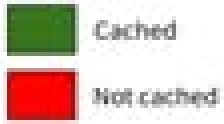


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Speculative overflow if x out of bound

val
saved RBP
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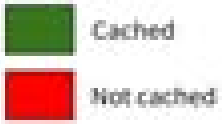


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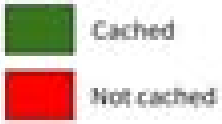


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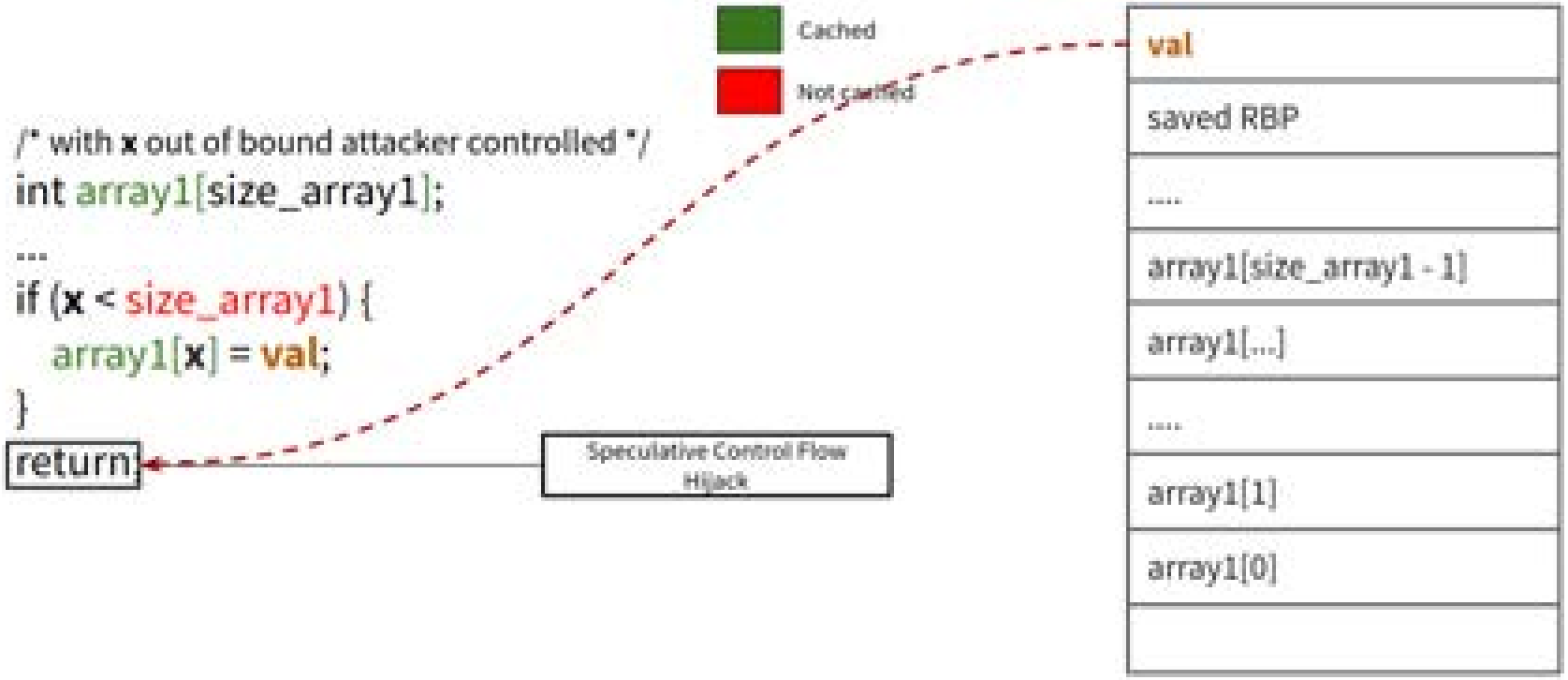

SPEculative ARchitectural control flow hijacks (SPEAR)

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SPEculative CFH

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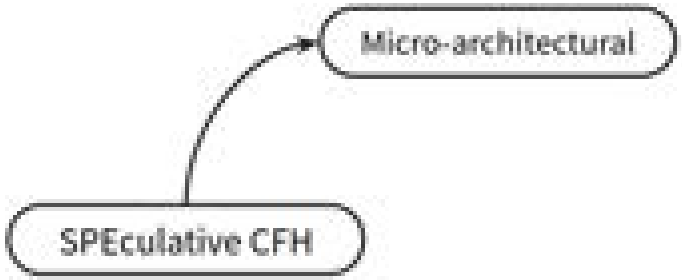

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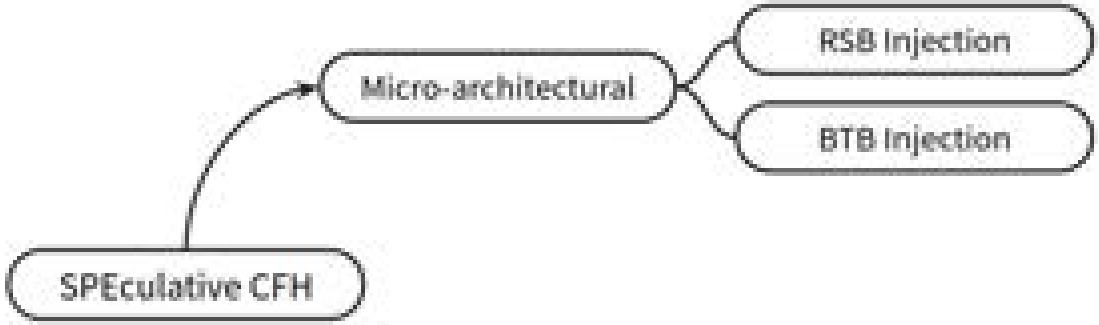

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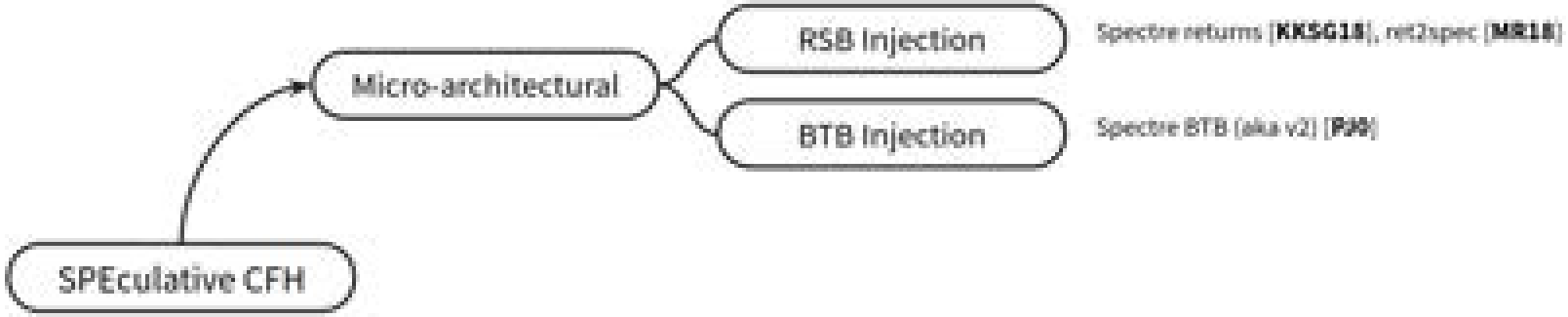

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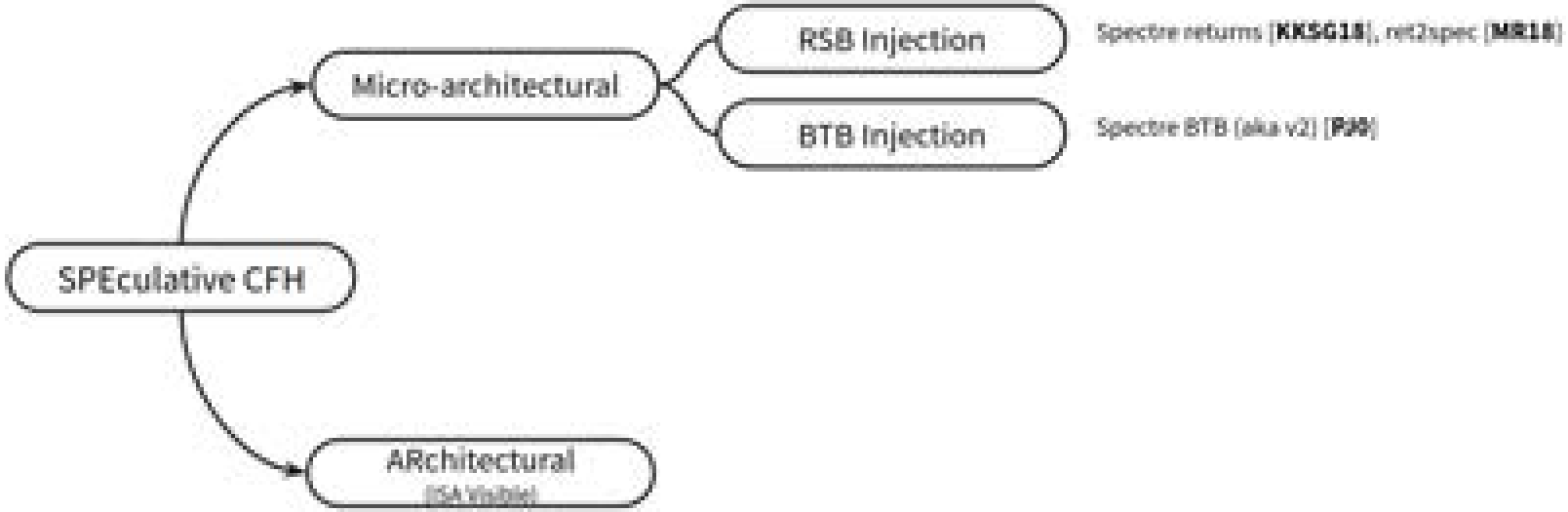

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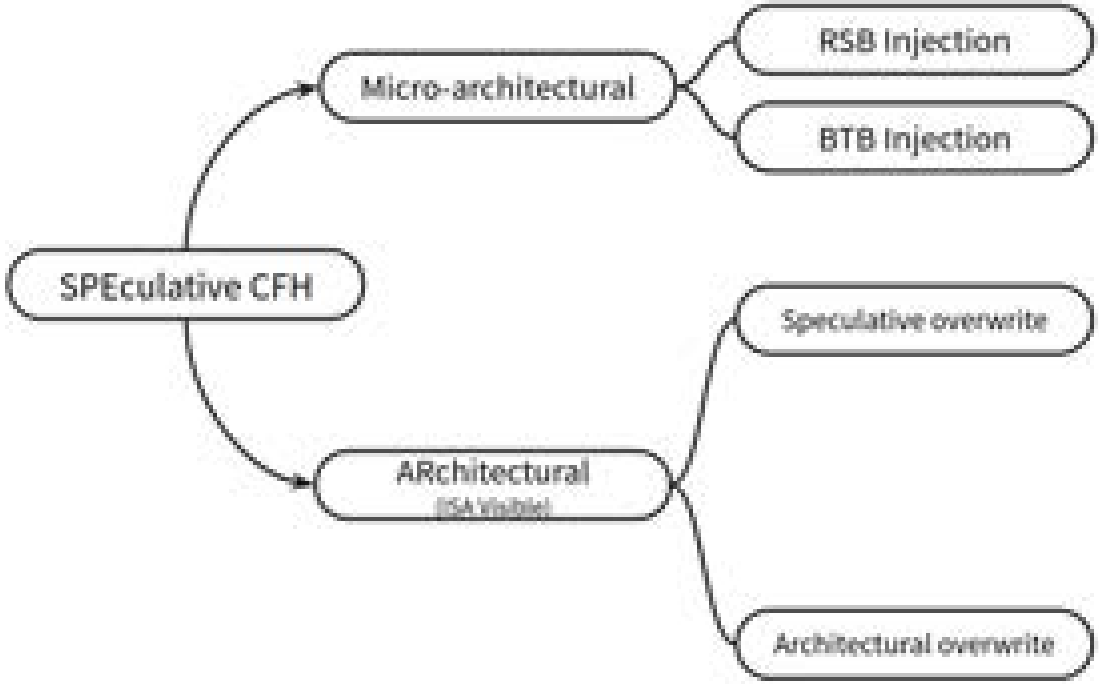

Spectre returns [**KKSG18**], ret2spec [**MR18**]

Spectre BTB (aka v2) [**PJ0**]

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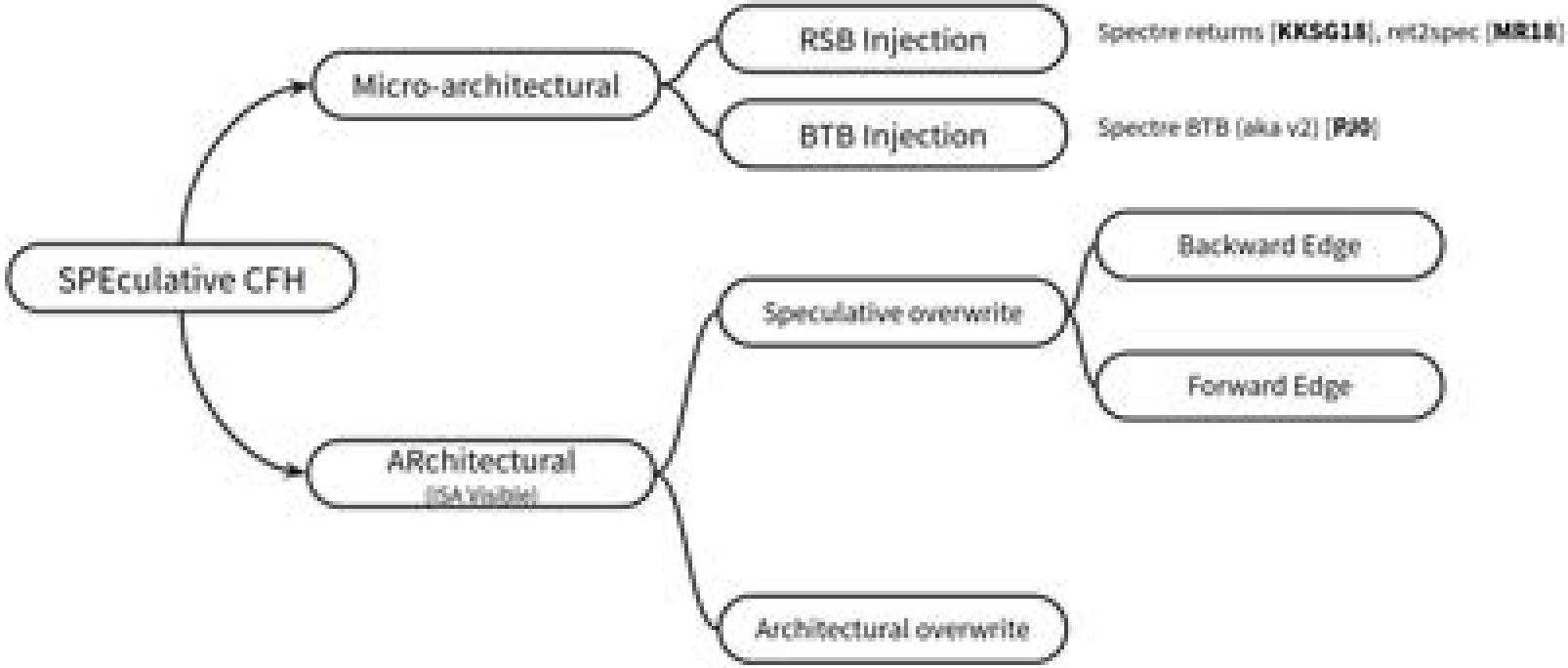

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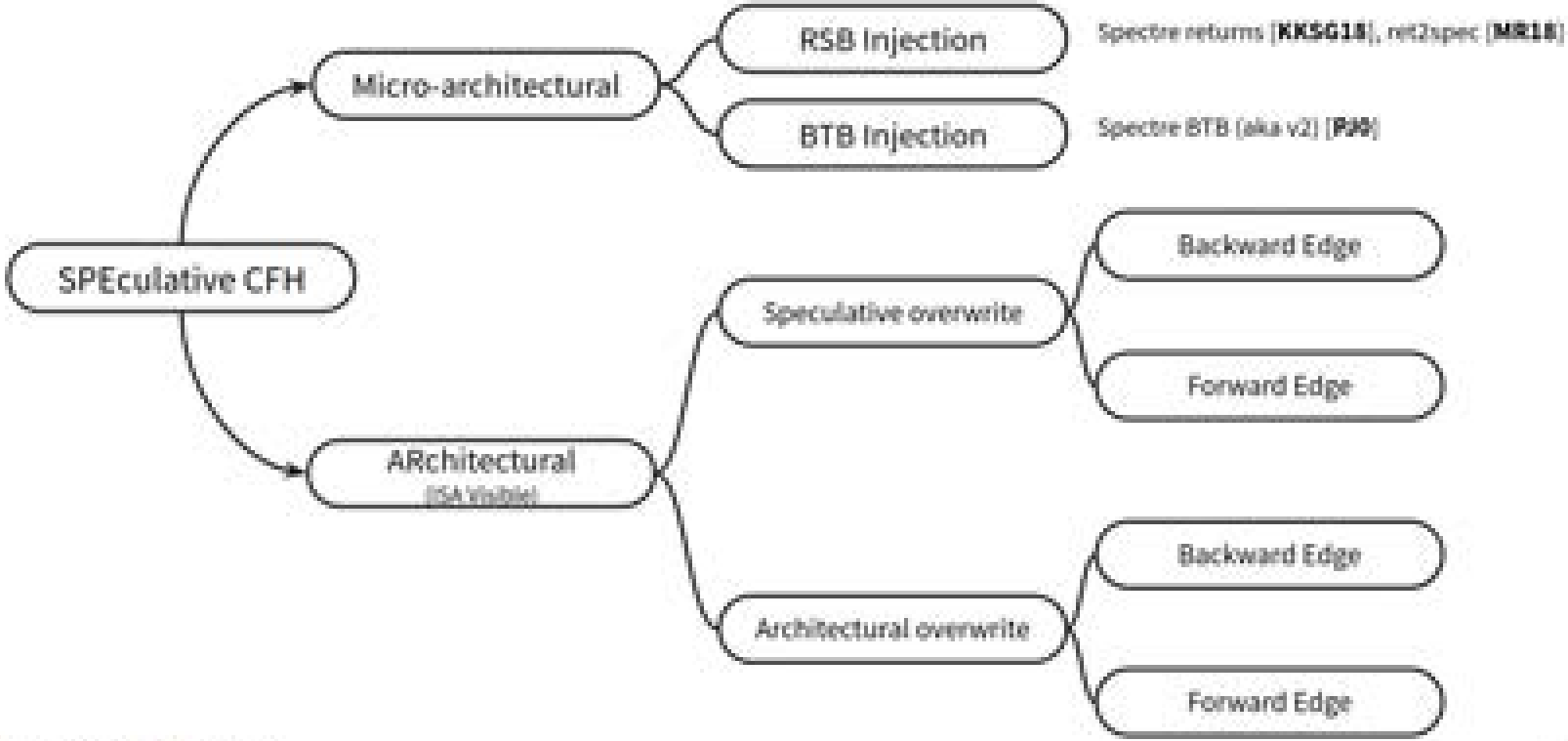

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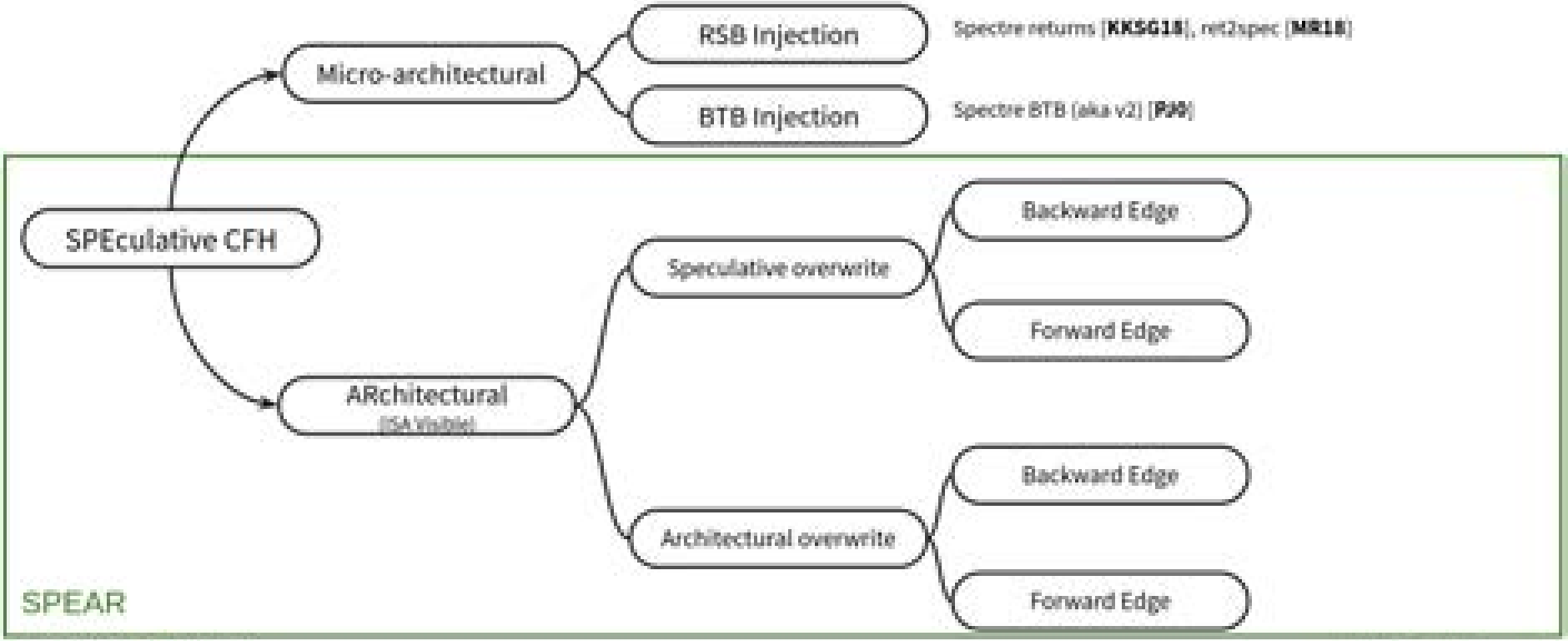

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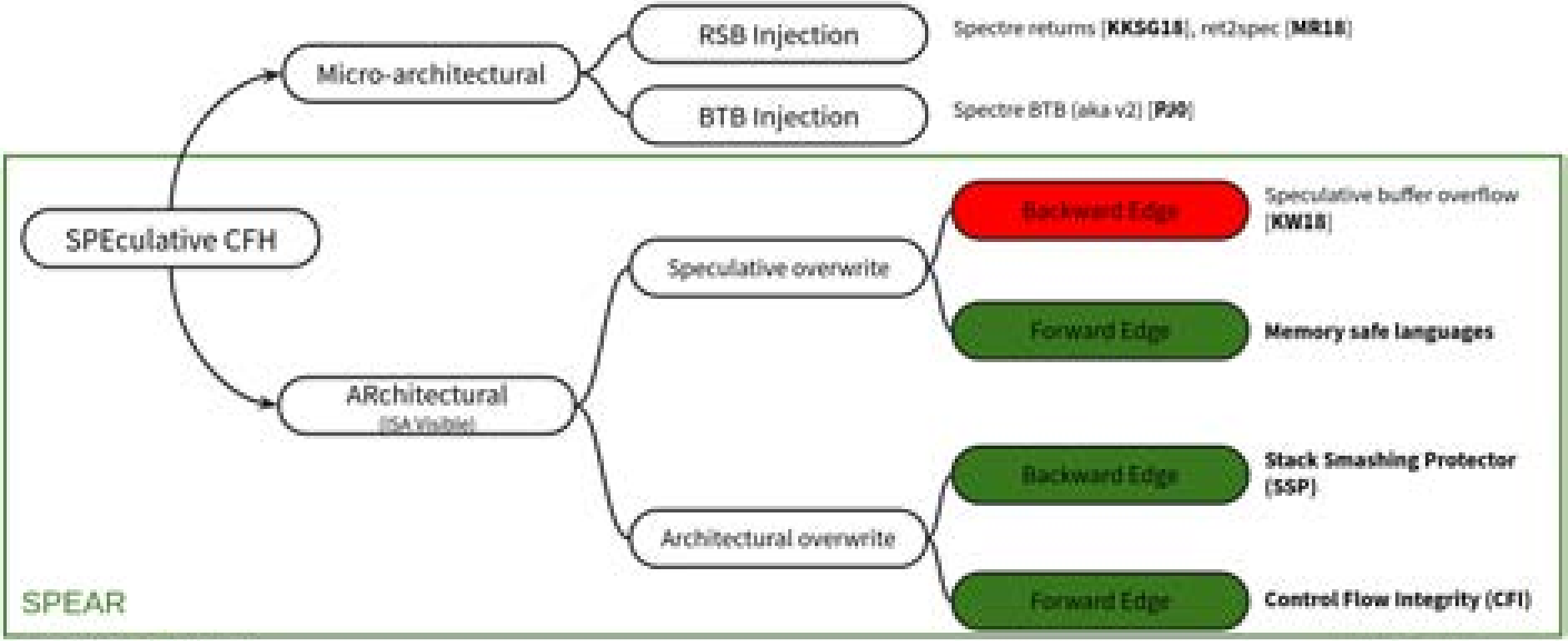

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3       mov QWORD[stored_ret], rax
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6   ;   (Attacker Controlled)
7       mov rax, QWORD[target]
8       mov [rsp], rax
9
10  ; Evict RET Value Copy
11      clflush [stored_ret]
12      lfence
13
14  ; Backward Edge Integrity Check
15  ;   (Speculation Trigger)
16      mov rax, [rsp]
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20  ; Backward Edge Hijack
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Test architectural overwrite backward edge

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	Architectural		Speculative	
Family	*Fwd*	*Bwd*	*Fwd*	*Bwd*
Intel Broadwell	99.5	94.9	99.5	98.7
Intel Skylake	97.6	98.3	98.2	92.1
Intel Coffee Lake	99.8	98.1	99.7	99.4
Intel Kabylake	99.5	95.9	100	99.5
AMD Ryzen	100	100	100	100

Success rates in % of our tests

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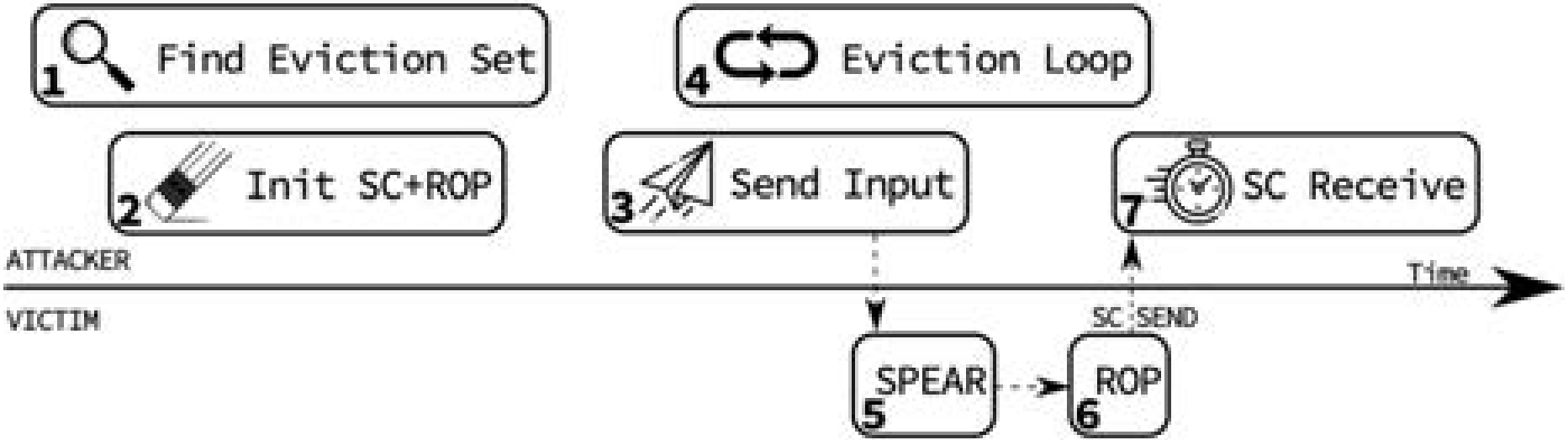

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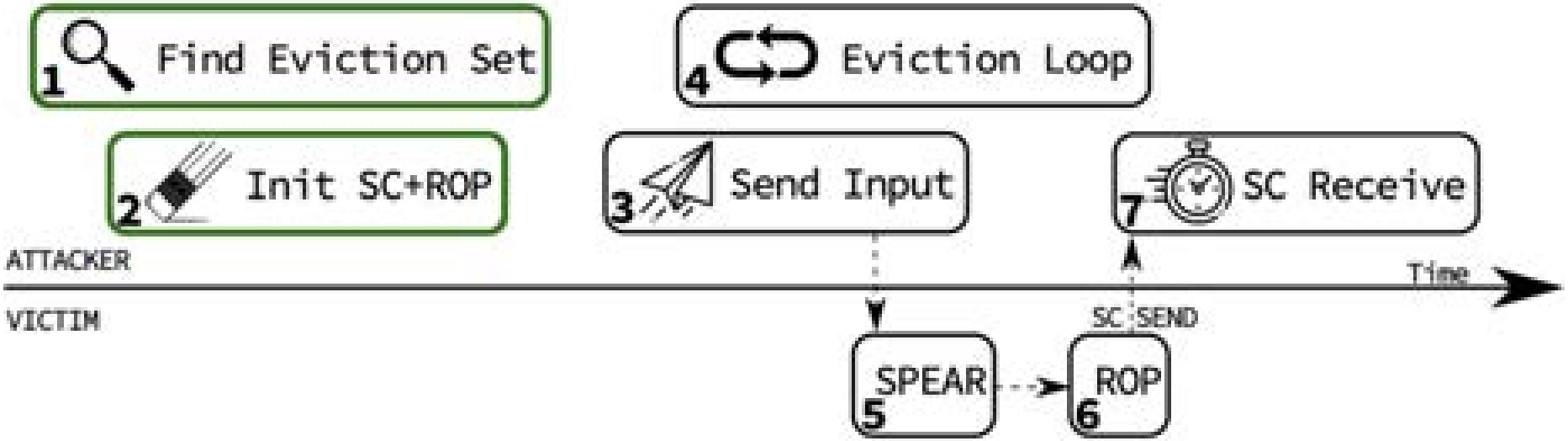

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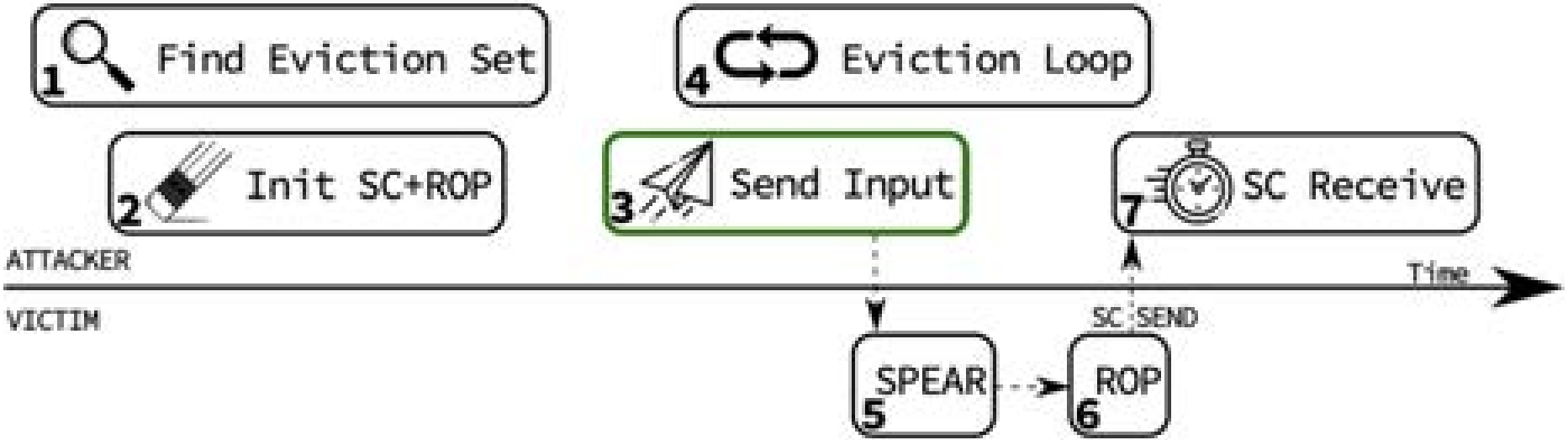

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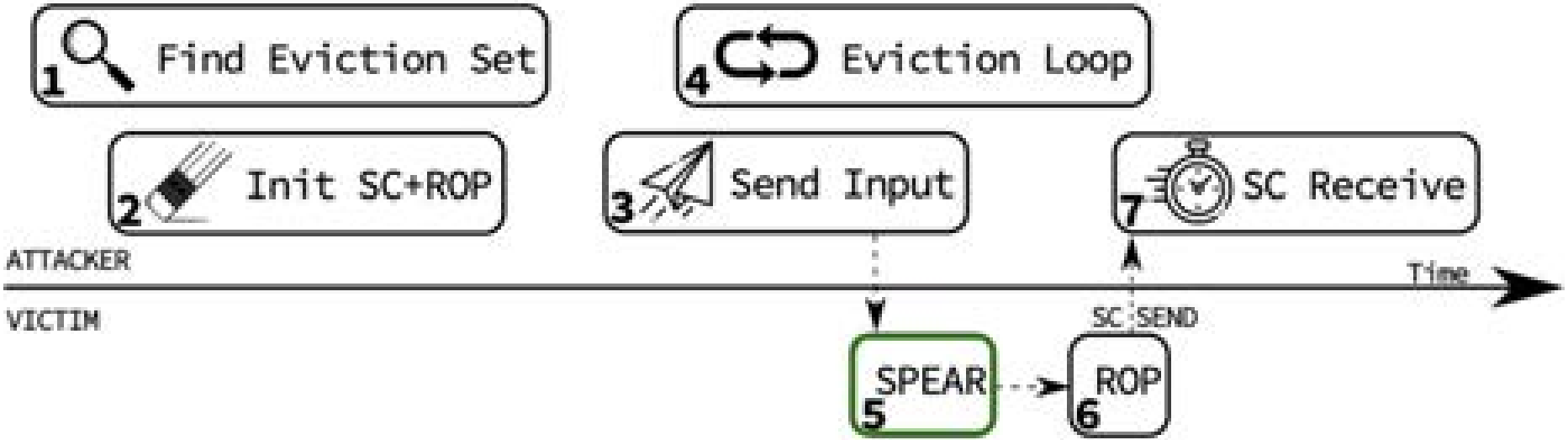

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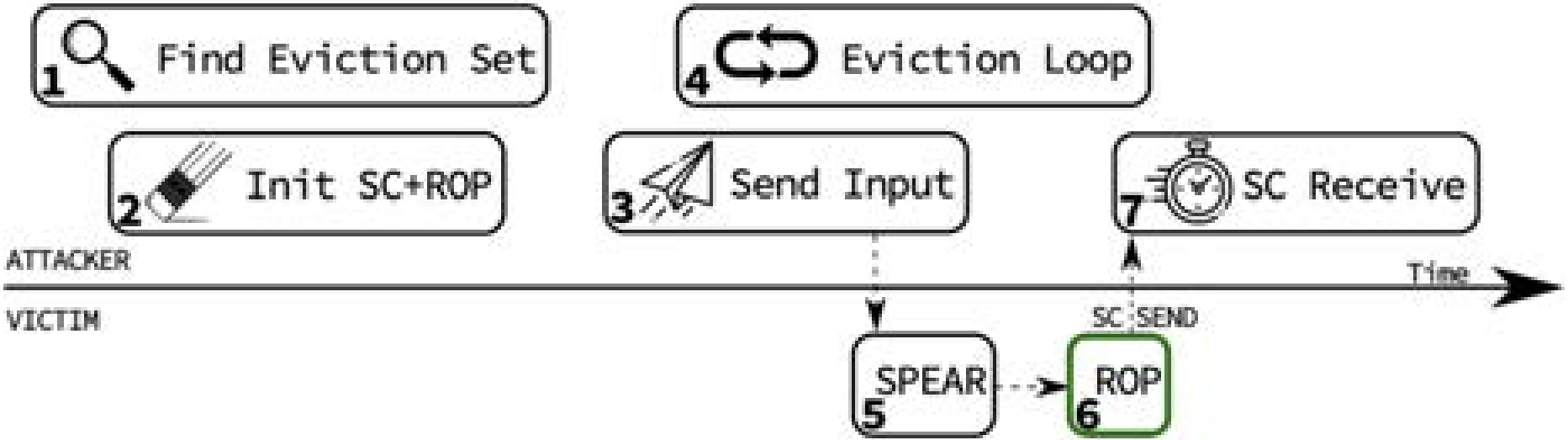

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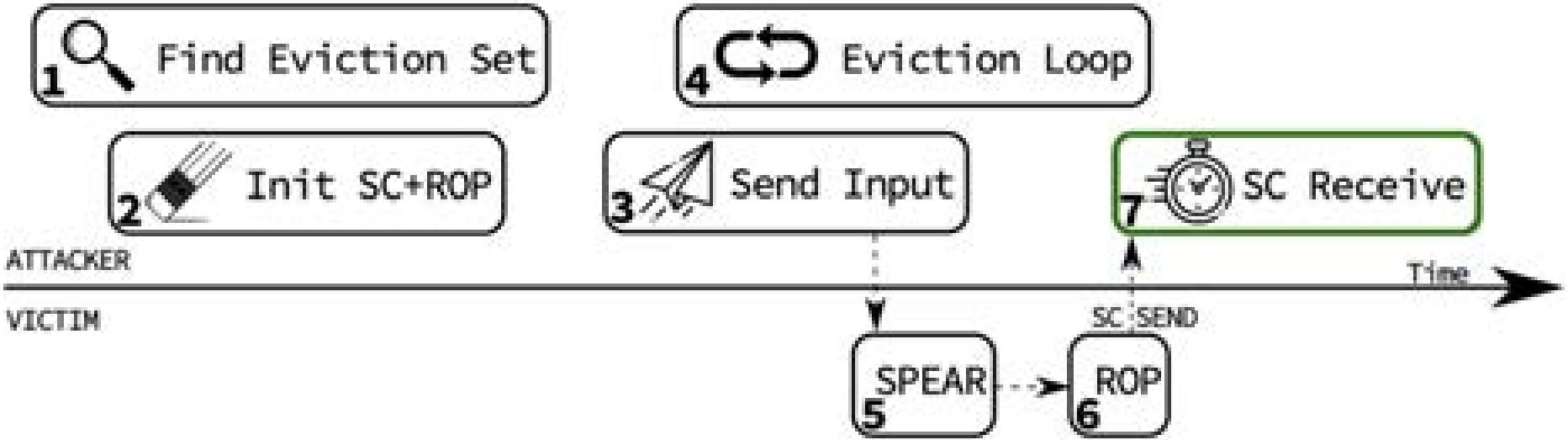

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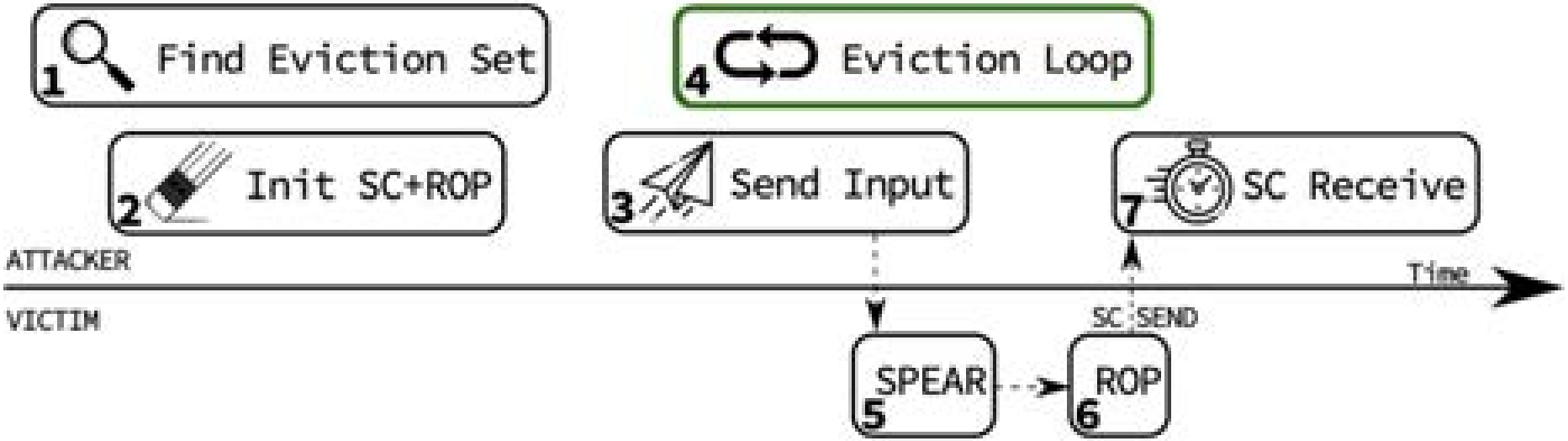

Attacking Stack Smashing Protection (SSP)

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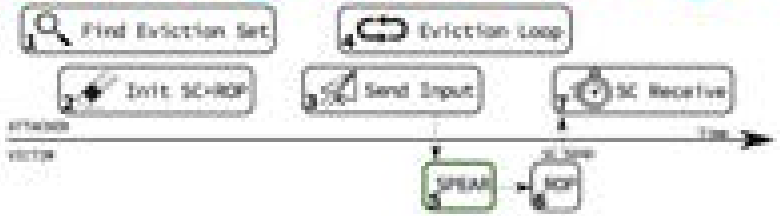

Attacking Stack Smashing Protection (SSP)

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void f() {
   char buf[size];
   memcpy(buf, src, src_size);
   if (!ok(canary)) {
      abort();
   }
   return;
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Stack buffer overflow

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```

Stack buffer overflow

ROP gadget
saved RBP
canary
....
buf[size - 1]
....
buf[1]
buf[0]

Attacker controlled

Not cached

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Speculative execution trigger

Attacker controlled

Not cached

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```
; Store canary on stack
      mov rbx, QWORD[fs:0x28]
      mov QWORD[stack_canary], rbx

; Function body

; Check for corrupted canary
      mov rbx, QWORD[stack_canary]
      xor QWORD[fs:0x28], rbx
      je exit
      call __stack_chk_fail

exit:
   ; Epilogue
      ret
```

Attacking Stack Smashing Protection (SSP)

```
void f() {
   char buf[size];
   memcpy(buf, src, src_size);
   if (!ok(canary)) {
      abort();
   }
   return;
}
```

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Speculative control flow hijack
architectural edge overwrite

Attacker controlled

Not cached

Attacking Stack Smashing Protection (SSP)

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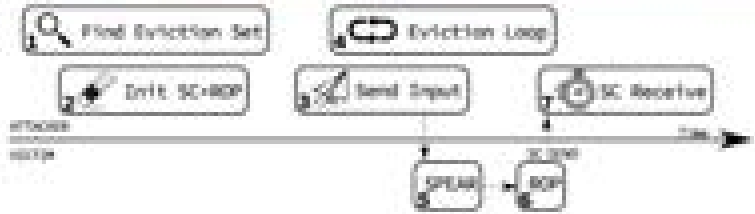
Canary eviction

Canary eviction



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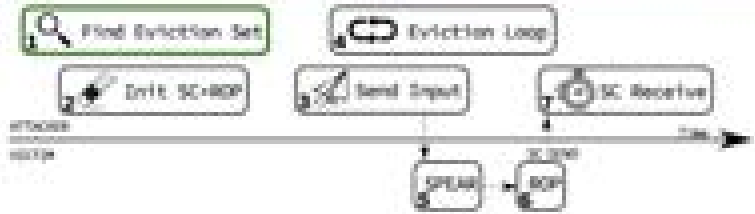

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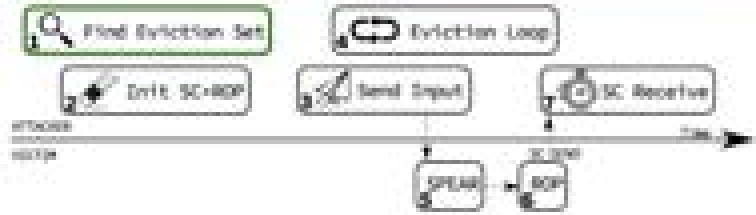

Attacker Program

Attacker Program

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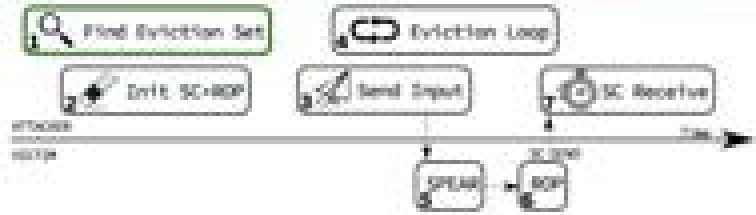

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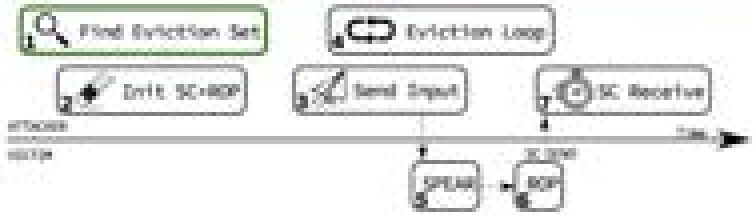

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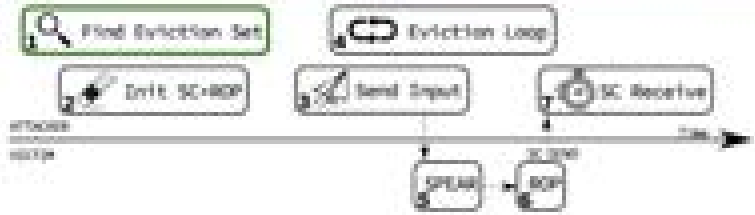

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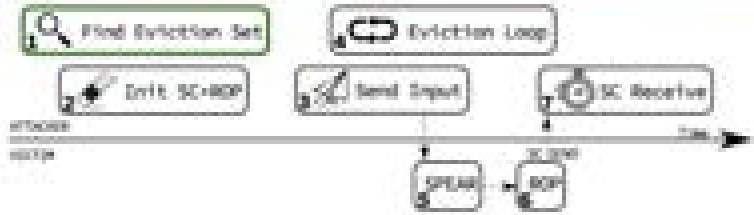

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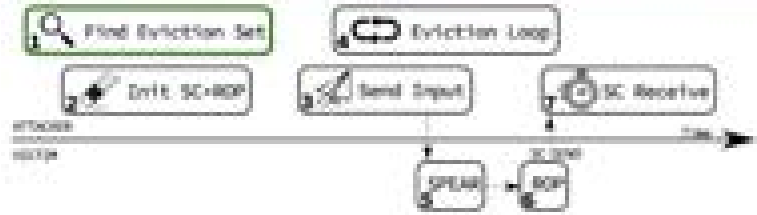

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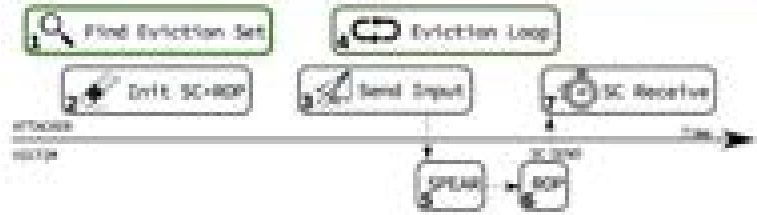

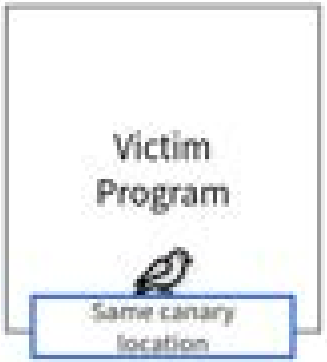

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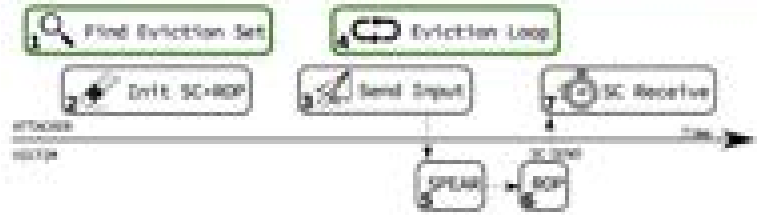

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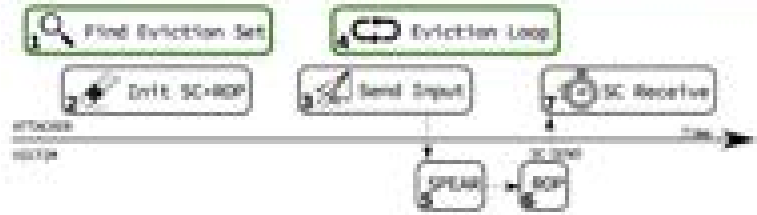
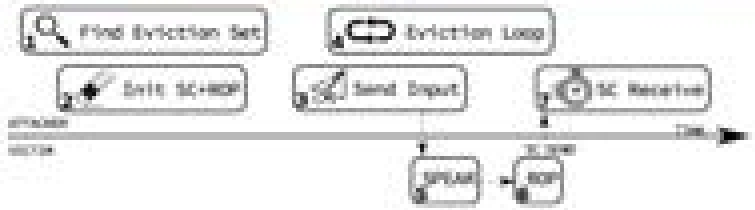


Not cached

Speculative ROP

Speculative ROP



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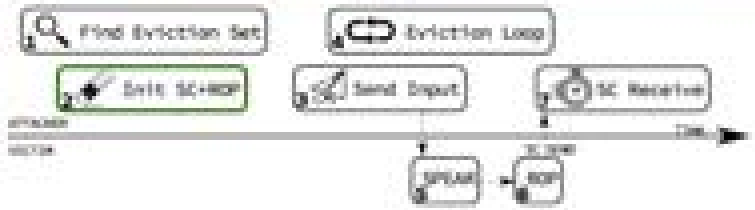

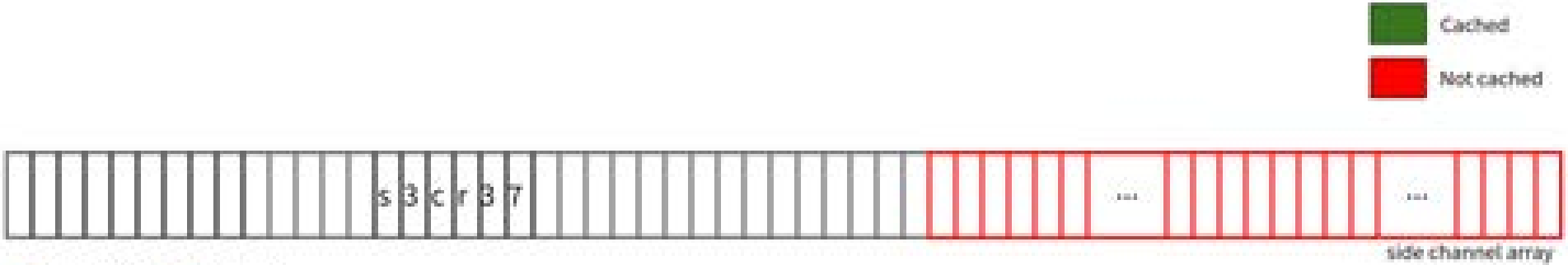

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    mov rax, BYTE[victim_addr]
    ret

; Compute side-channel array entry
    shl rax, 8
    ret

; Add side-channel array base
    add rax, base_address
    ret

; Access side-channel array entry
;   (Side-channel Send Signal)
    mov rax, QWORD[rax]
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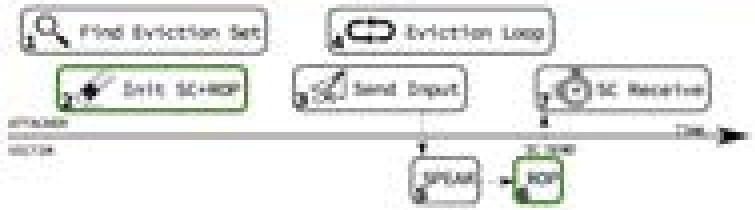
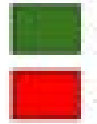
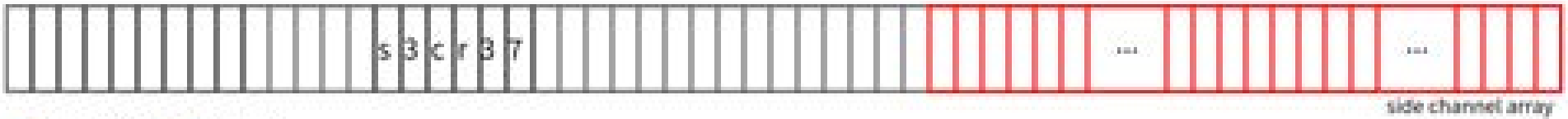
```







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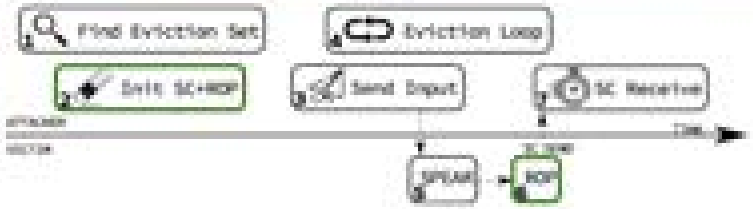

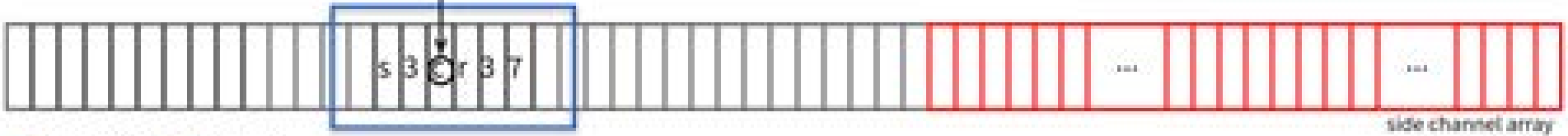

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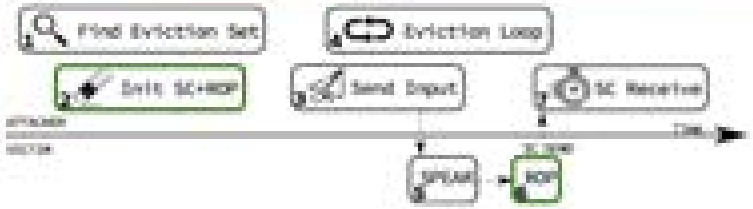

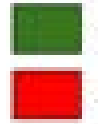

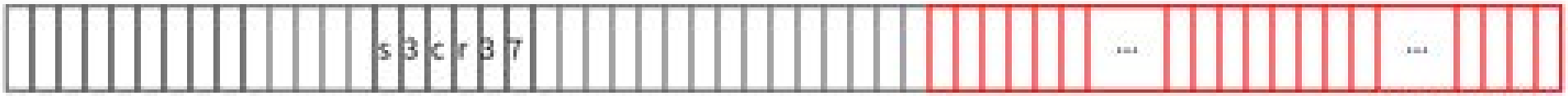

side channel array

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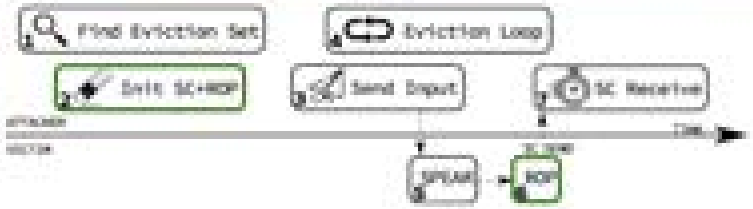

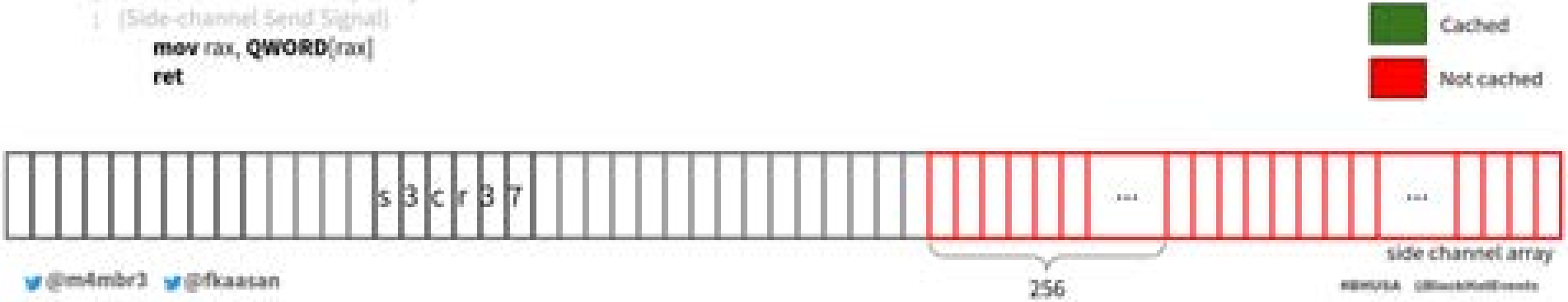

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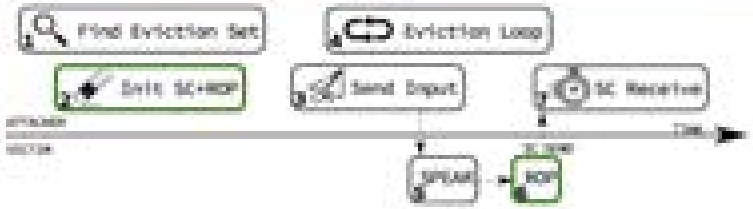
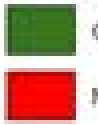
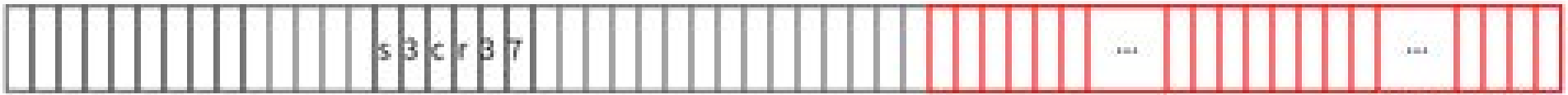
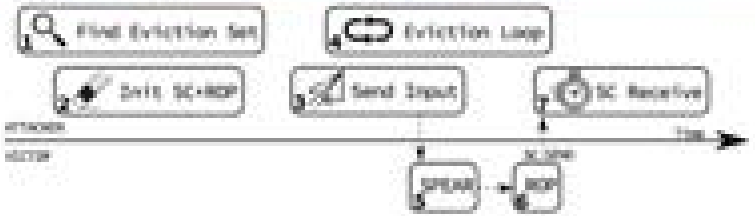






Arbitrary memory read with a side-channel

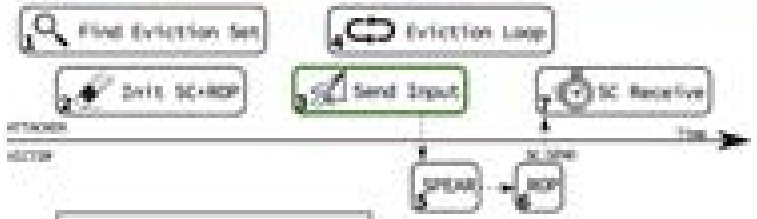


Arbitrary memory read with a side-channel

Attacker Program

Victim Program

Arbitrary memory read with a side-channel



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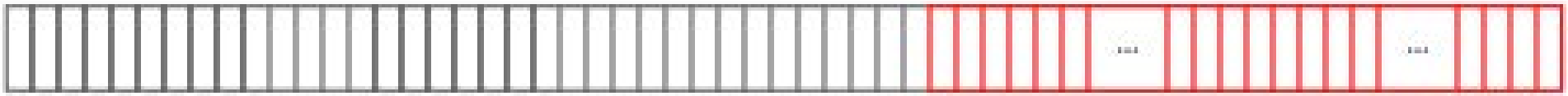

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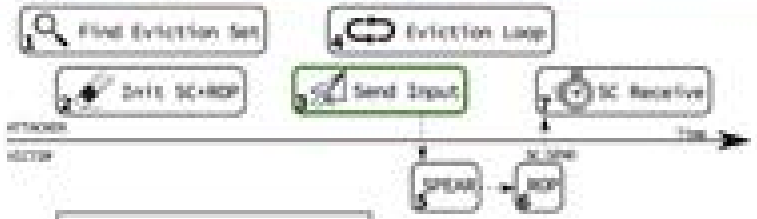

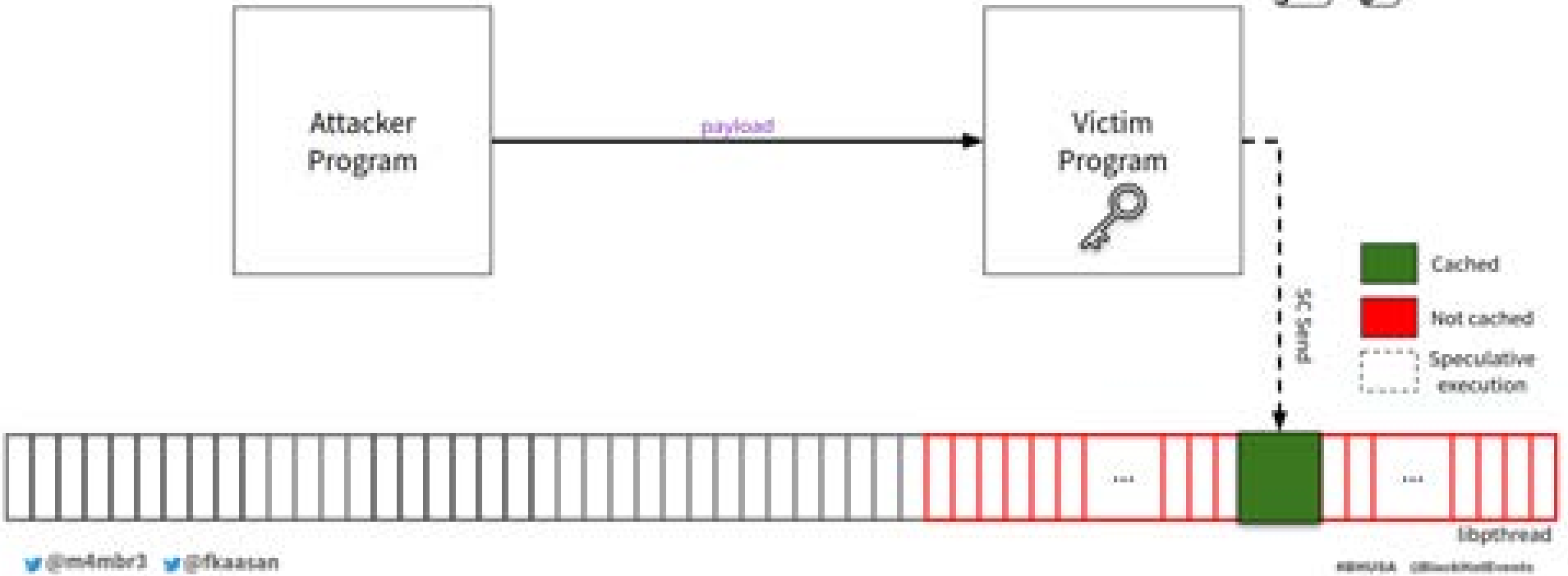

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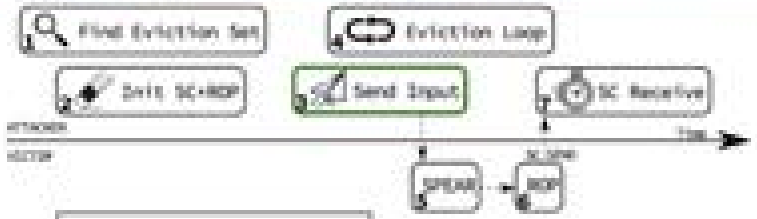

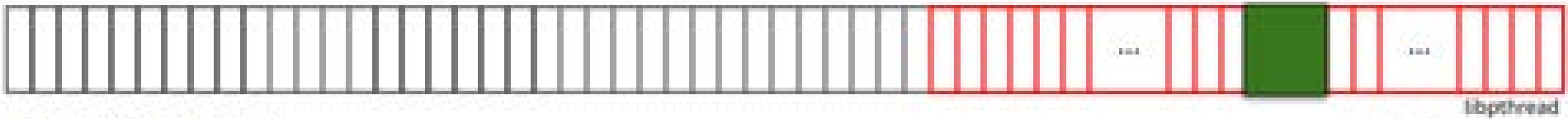

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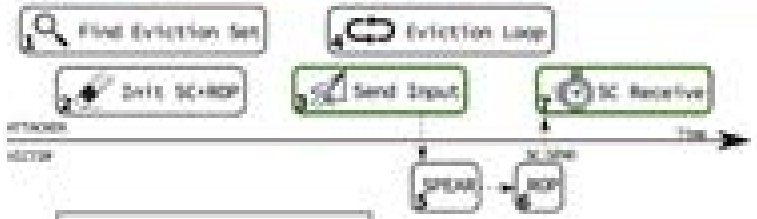

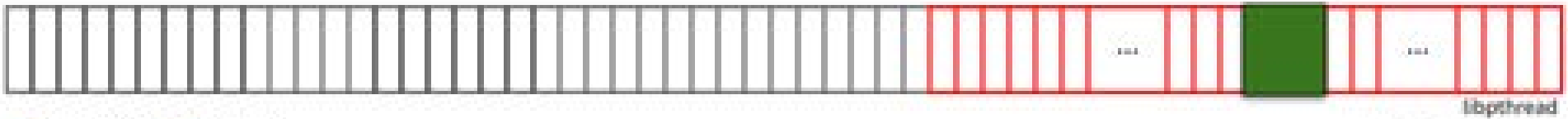

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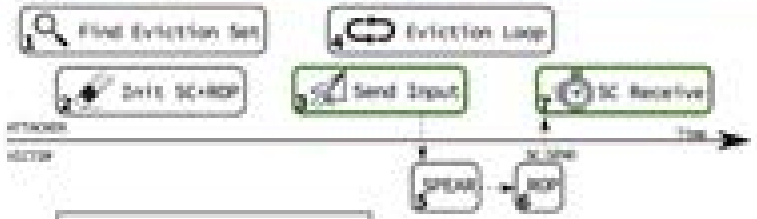

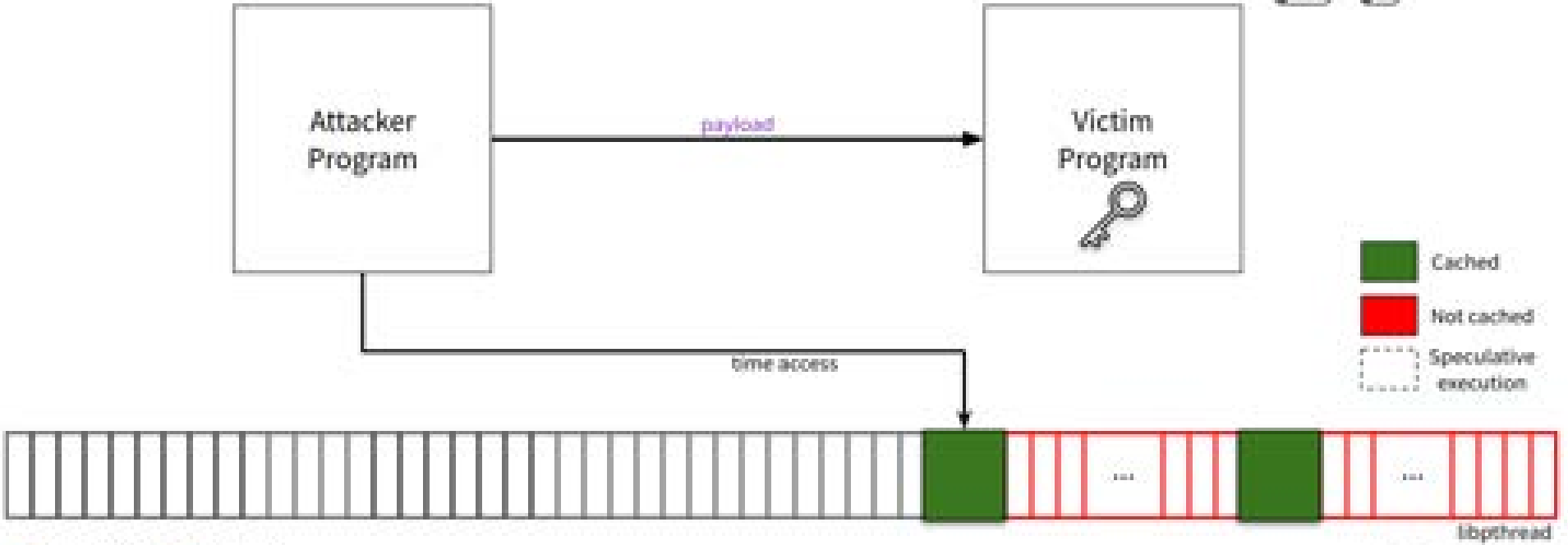

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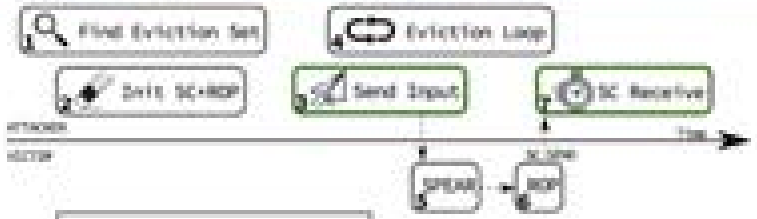

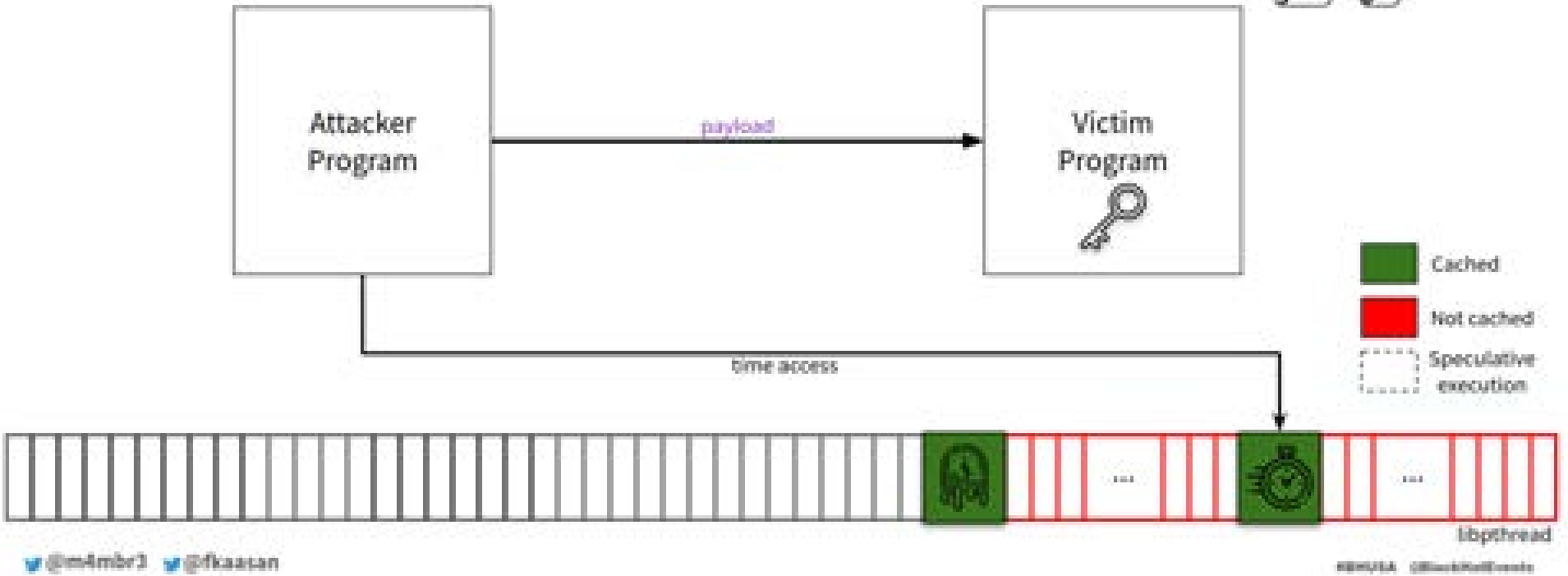

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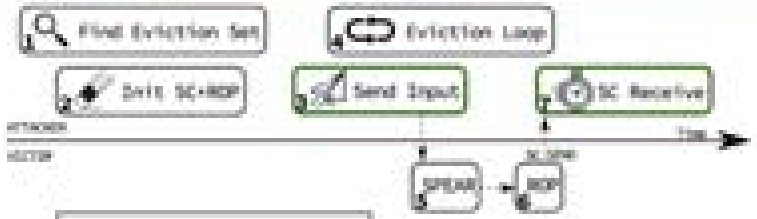

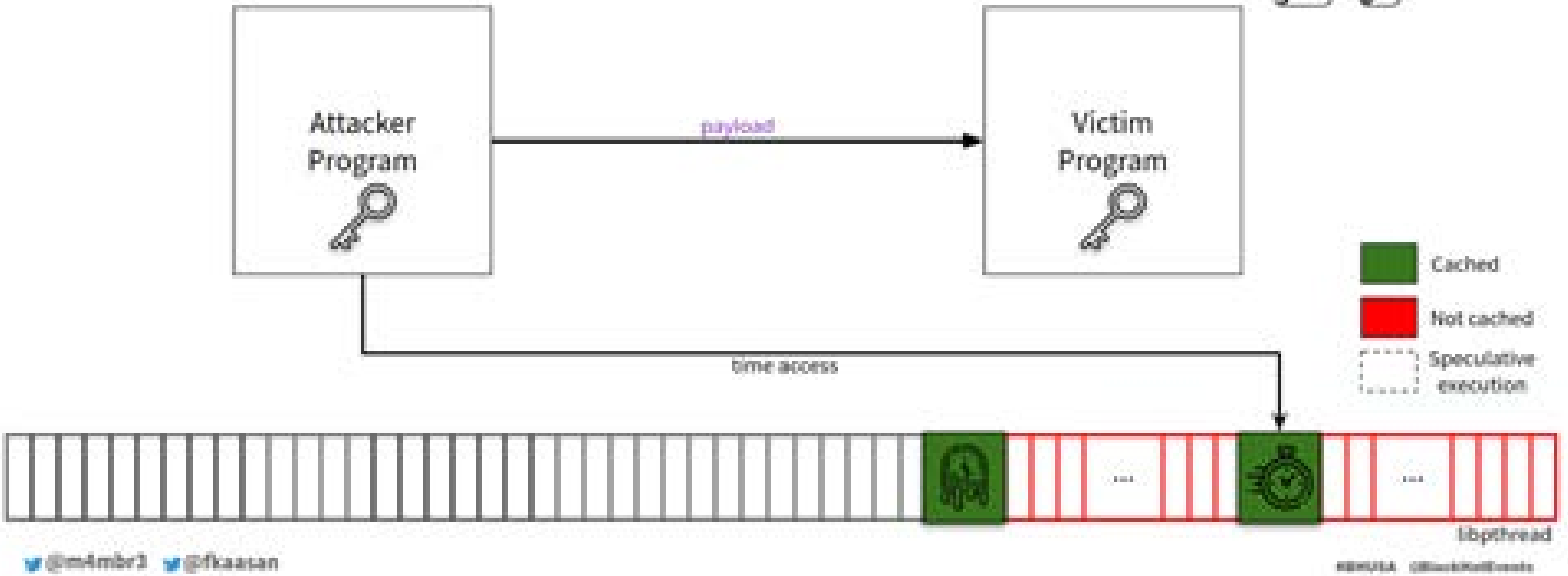

Results

Local arbitrary victim memory read

Leak rate for 2-digits sized secret: **0.3 Bytes per second**

100 attack runs per byte to reduce noise (shared library as side-channel array)

Works on Intel **Skylake** and **Coffee Lake** with all Spectre mitigations enabled

Slight success rate change between Ubuntu 16.04 and Ubuntu 20.04

Discussion about attack optimization and better synchronization are in our paper

Other SPEAR case - memory safe languages

[1] https://github.com/golang/go/wiki/Spectre

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More details in our EuroSP 2021 paper: https://arxiv.org/abs/2003.05503

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Examples:

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These mitigations require instrumentation of the application

Some compiler pass already exists (e.g., LLVM Speculative Load Hardening)

Generally, they are very hard to apply due to the trade-off coverage/overhead

Examples:

Fencing instructions like **lfence** or **mfence**

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Only available in future iterations of CPUs

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SEAs are a significant research and industry challenge for the next decade (tools, attacks and defences)

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