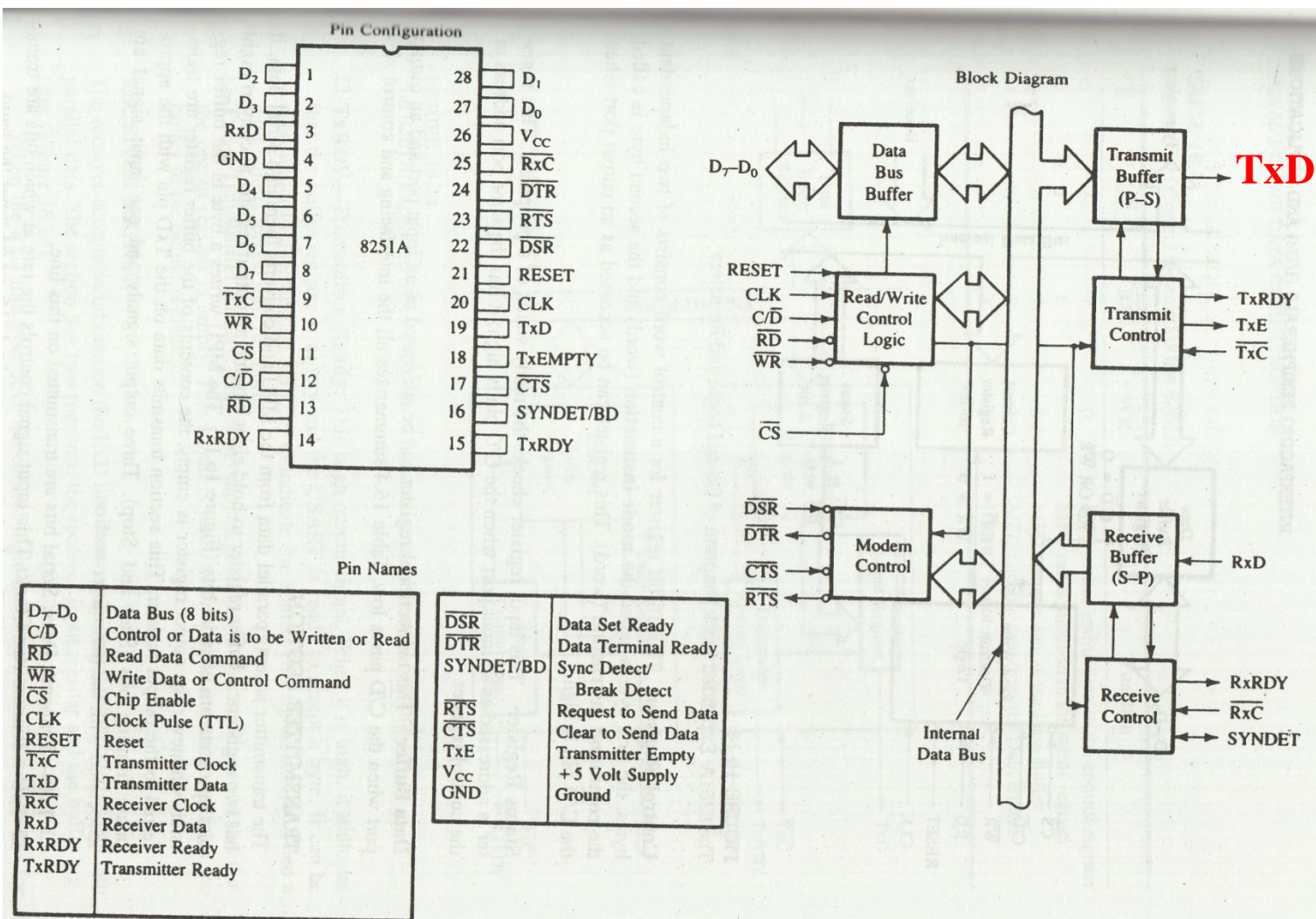


# **8251-Programmable Communication Interface (8251-PCI)**





**FIGURE 16.12**

The 8251A: Block Diagram, Pin Configuration, and Description

SOURCE: Intel Corporation, *Connectivity* (Santa Clara, Calif.: Author, 1993), p. 2-2.

# Features

- ✓ The 8251 is a programmable chip designed for **synchronous** and **asynchronous serial data communication**
- ✓ The INTEL 8251 is the industry standard Universal Synchronous/Asynchronous Receiver/Transmitter (**USART**) designed for data communications
- ✓ The 8251 is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique
- ✓ The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission
- ✓ Simultaneously, it can receive serial data streams and convert them into parallel data character for the CPU
- ✓ The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU



# Description

The block diagram includes five section

- ✓ Read/write Control Logic
- ✓ Transmitter
- ✓ Receiver
- ✓ Data Bus Buffer and
- ✓ Modem Control



# Read/Write Control Logic

The control logic interfaces the chip with the processor, determines the functions of the chip according to the control word in its register, and monitors the data flow



# Transmitter

The transmitter section converts a parallel word received from the processor into serial bits and transmits them over the TxD line to a peripheral



# Receiver

The transmitter section receives serial bits from a peripheral, converts them into a parallel word, and transfers the word to the  $\mu\text{P}$



# Modem Control

The modem control is used to establish data communication through modems over telephone lines





# Data Buffer

This bidirectional register can be addressed as an input and an output port when the  $\mathbf{C/\bar{D}}$  pin is low

## Control/Data pin ( $\mathbf{C/\bar{D}}$ ):

When this signal is high, the control register or the status register is addressed; when it is low, the data buffer is addressed. The control register and the status register are differentiated by  $\overline{RD}$  and  $\overline{WR}$  signals respectively.



# Control Register

This 16-bit register for a control word consists of two independent bytes; the first byte is called **Mode Instruction (Word)** and the second byte is called the **Command Instruction (Word)**. This register can be accessed as an output port when the  $\text{c}/\overline{\text{D}}$  pin is high



# Status Register

This input register checks the ready status of a peripheral. This register is addressed as an input port when the **C/ $\bar{D}$**  pin is high. It has the same port address as the control register



# Initialization of 8251

To implement serial communication, 8085 must inform 8251 of all the details, such as mode, baud, stop bits, parity etc. Therefore prior to data transfer, a set of control words must be loaded into 16-bit control register of the 8251. In addition, 8085 must check the readiness of a peripheral by reading the status register. The control words are divided into two formats: mode word and command word.

*(Please see page number 547 to refer the format of Control Word and Status Word Format)*



# NEXT CLASS

**8237**



# THANK YOU

