Serial form of Data Vs Parallel Form of Data

- ✓ Data may be available in Parallel form or Serial form.
- ✓ Multi bit data is said to be in parallel form when all the bits are available (accessible) simultaneously.
- ✓ The data is said to be in serial form when data bits appear sequentially (one after another in time) at a single terminal.
- ✓ Data may also be transferred in parallel form or in serial form.

Data Transmission Serial/Parallel

- ✓ Parallel data transfer is the simultaneous transmission of all bits of data from one device to another.
- ✓ Serial data transfer is the transmission of one bit of data at time from one device to another.
- ✓ Serial data must be transmitted under the synchronization of a clock, since clock provides the means to specify the time at which each new bit is sampled

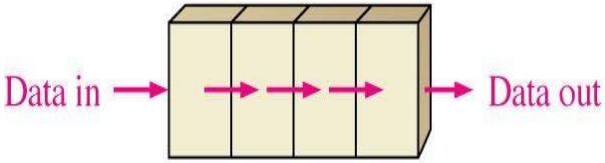
Register

- ✓ As a flip flop can store only one bit of data, a 0 or a 1, it is referred as a single bit register.
- ✓ When more bits of data are to be stored, a number of FFs used.
- ✓ A register is a set of FFs used to store binary data.
- ✓ The storage capacity of a register is the number of bits (1s and 0s) of digital data it can retain.
- ✓ A register may have output data either in serial form or in parallel form.

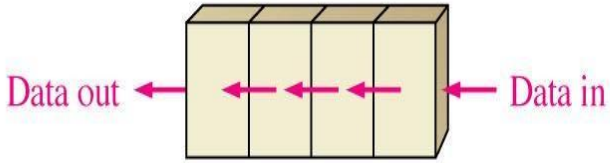
Shift Register

- ✓ A shift register is a very important digital building blocks. It has innumerable applications.
- ✓ Shift registers are a type of logic circuits closely related to counters.
- ✓ They are used basically for storage and transfer of digital data.
- ✓ The basic difference between a shift register and a counter is that, a shift register has no specified sequence of states whereas a counter has a specified sequence of states.

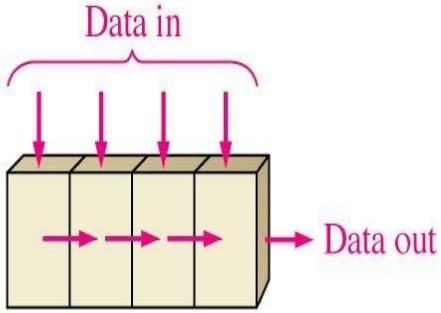
Basic Data Movements in Shift Registers



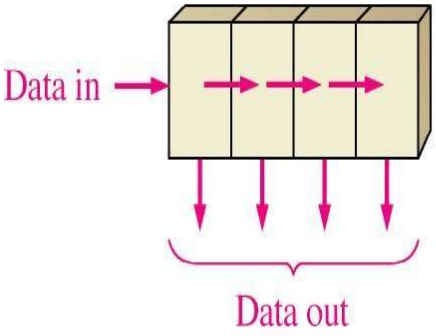
(a) Serial in/shift right/serial out



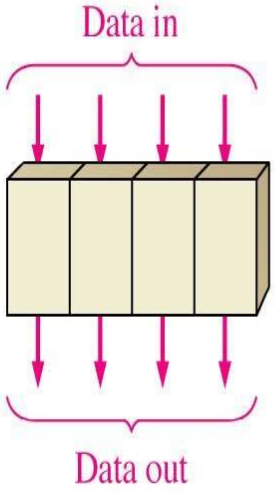
(b) Serial in/shift left/serial out



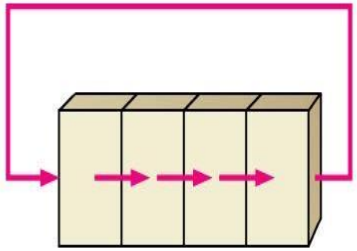
(c) Parallel in/serial out



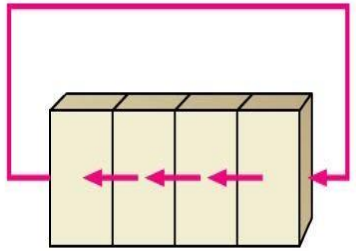
(d) Serial in/parallel out



(e) Parallel in/parallel out



(f) Rotate right

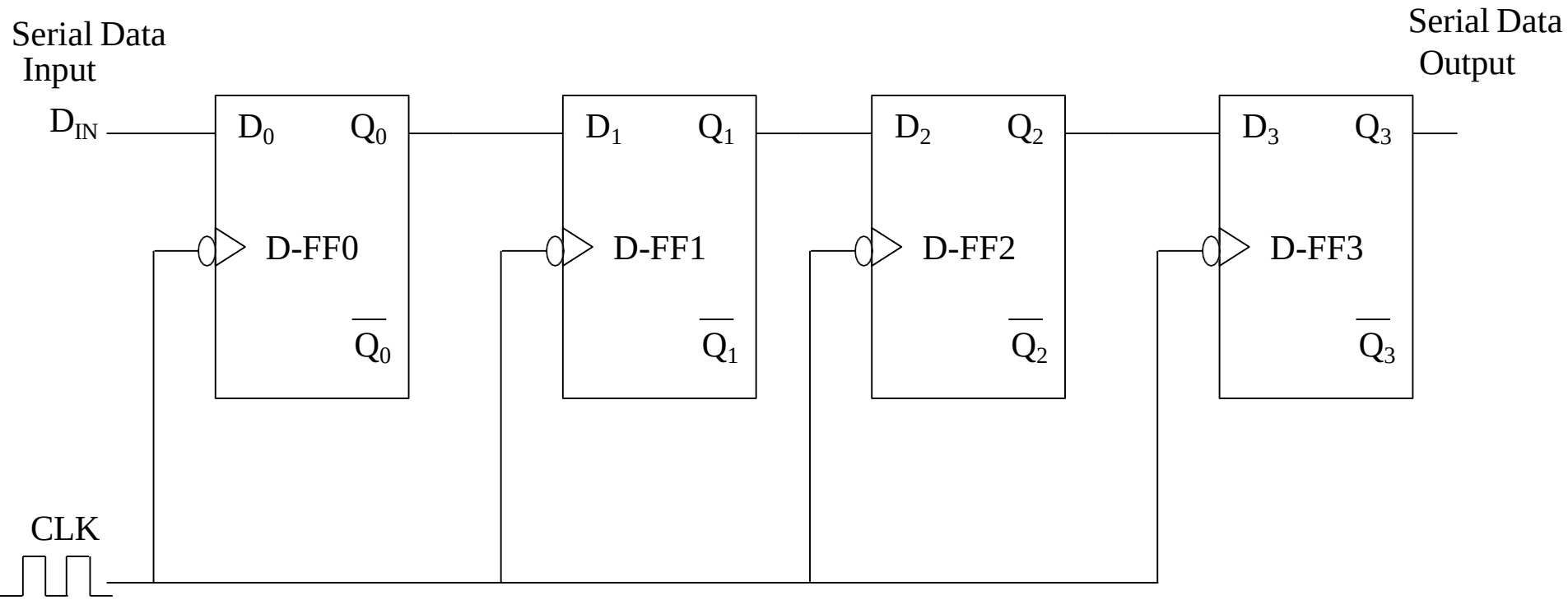


(g) Rotate left

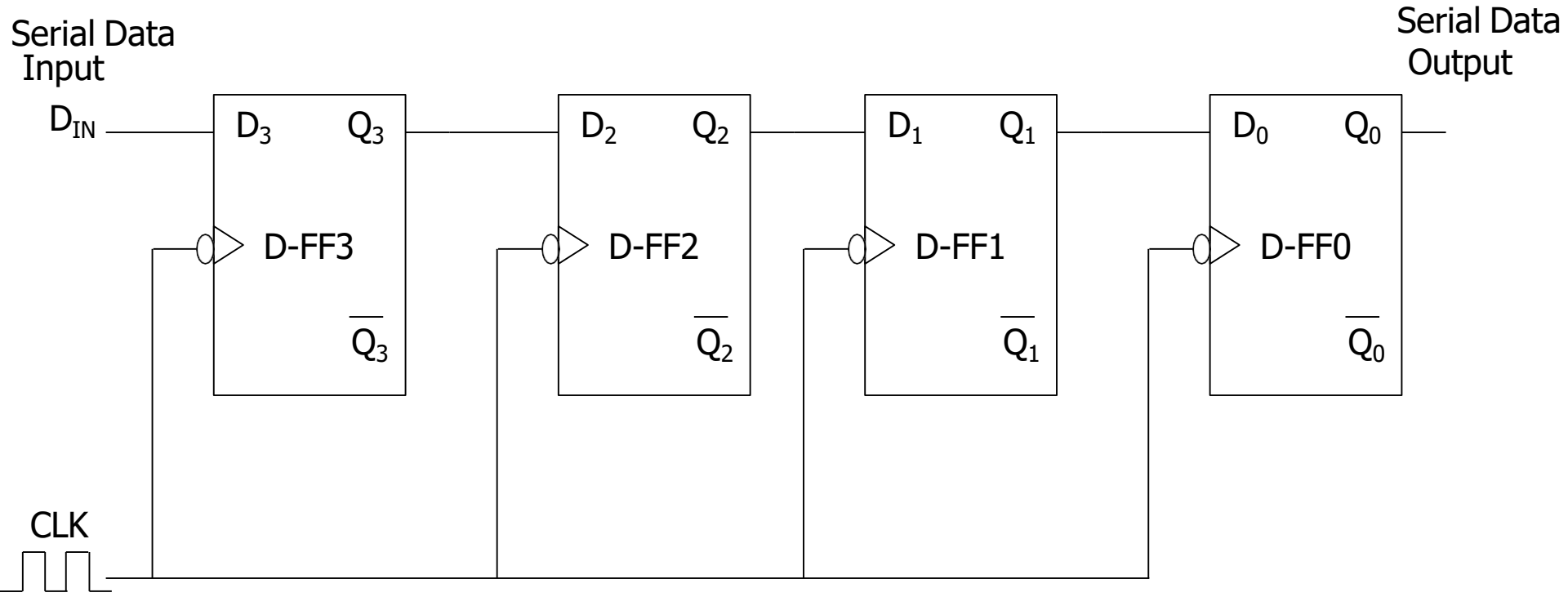
Types of Shift Registers

- ✓ SISO – Serial In Serial Out Shift Register
- ✓ SIPO – Serial In Parallel Out Shift Register
- ✓ PISO – Parallel In Serial Out Shift Register
- ✓ PIPO – Parallel In Parallel Out Shift Register
- ✓ Bi-directional Shift Register
- ✓ Universal Shift Register

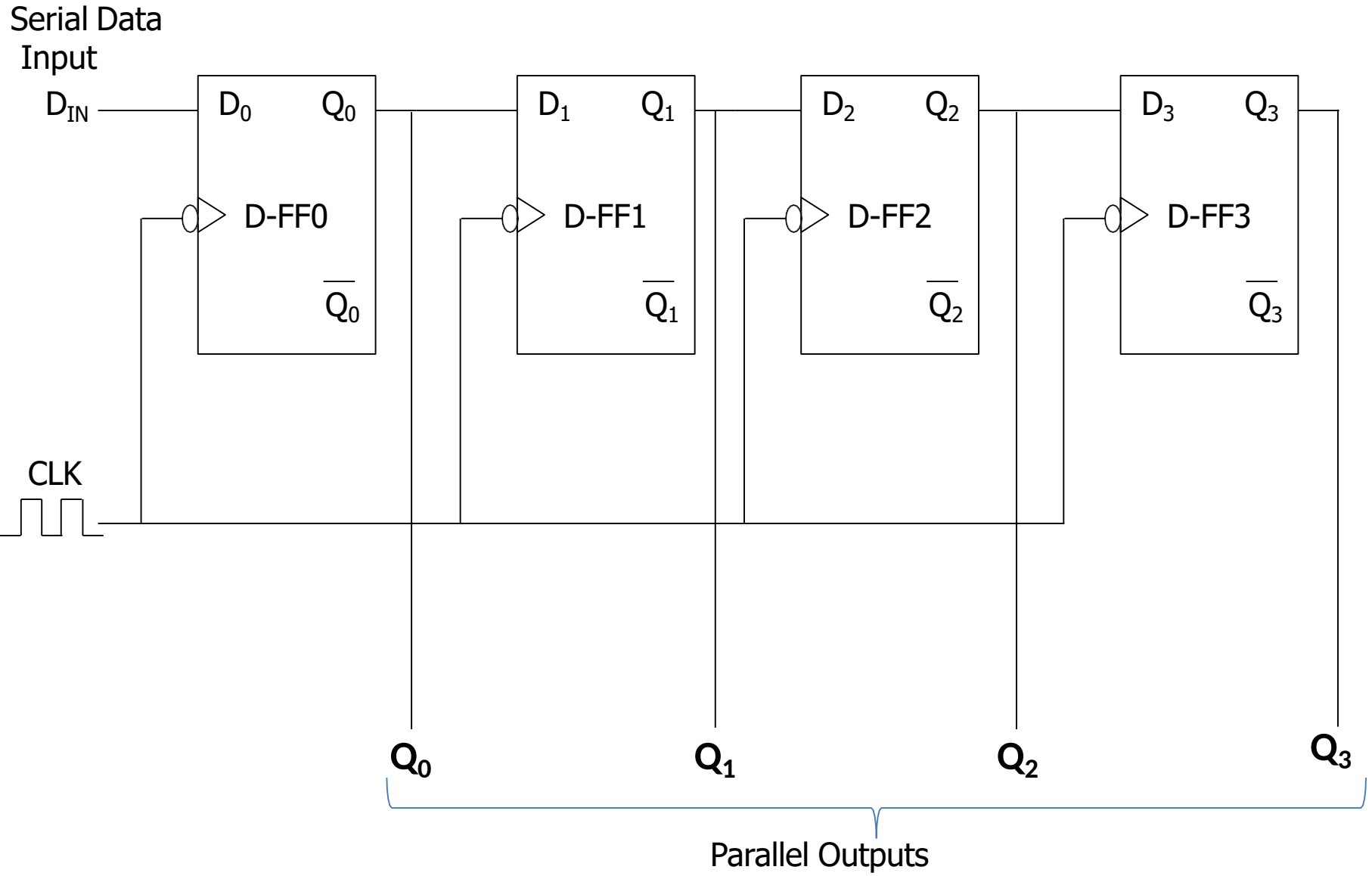
SISO – Serial In Serial Out Shift Register (Shift Left)



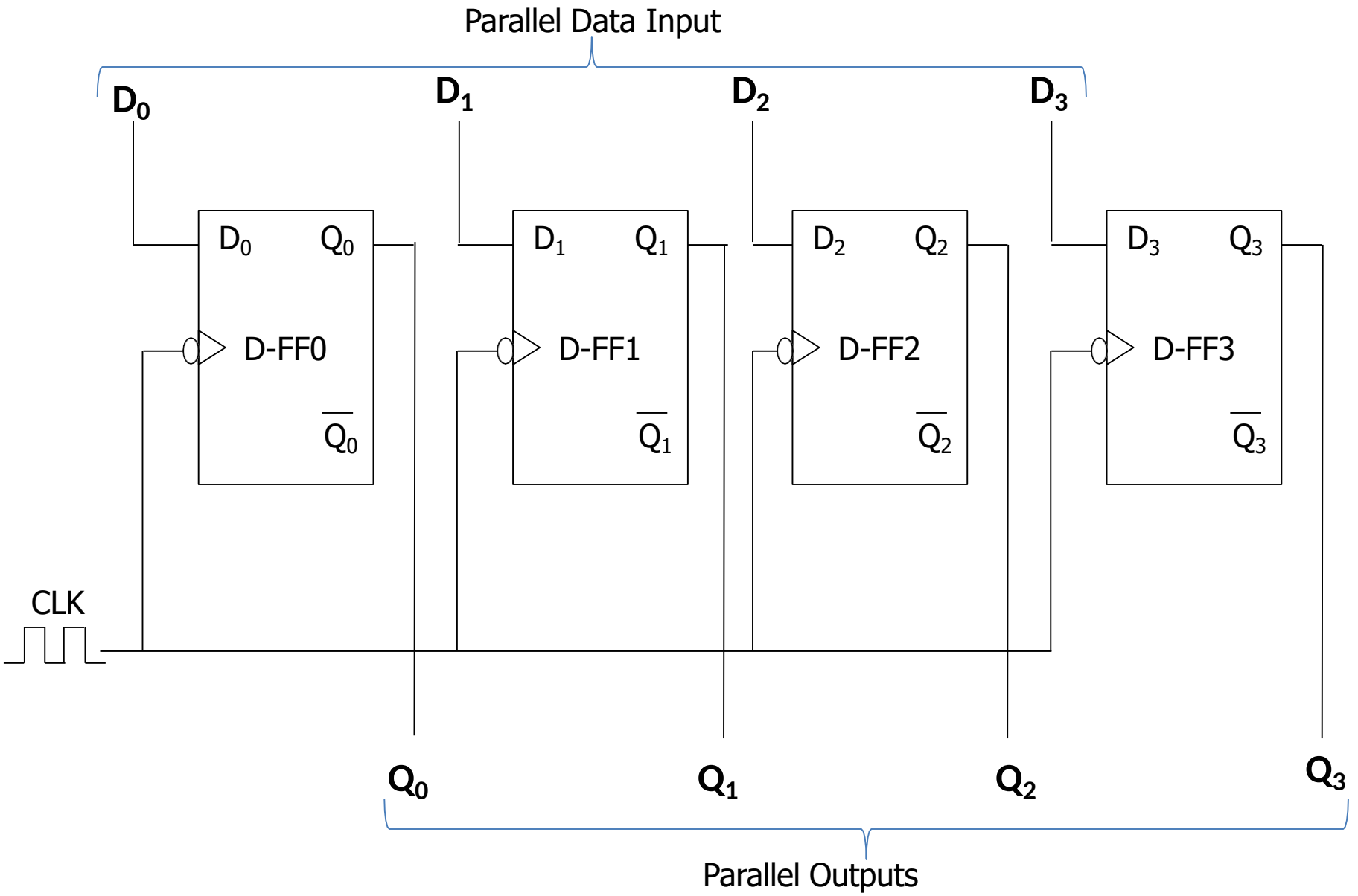
SISO – Serial In Serial Out Shift Register (Shift Right)



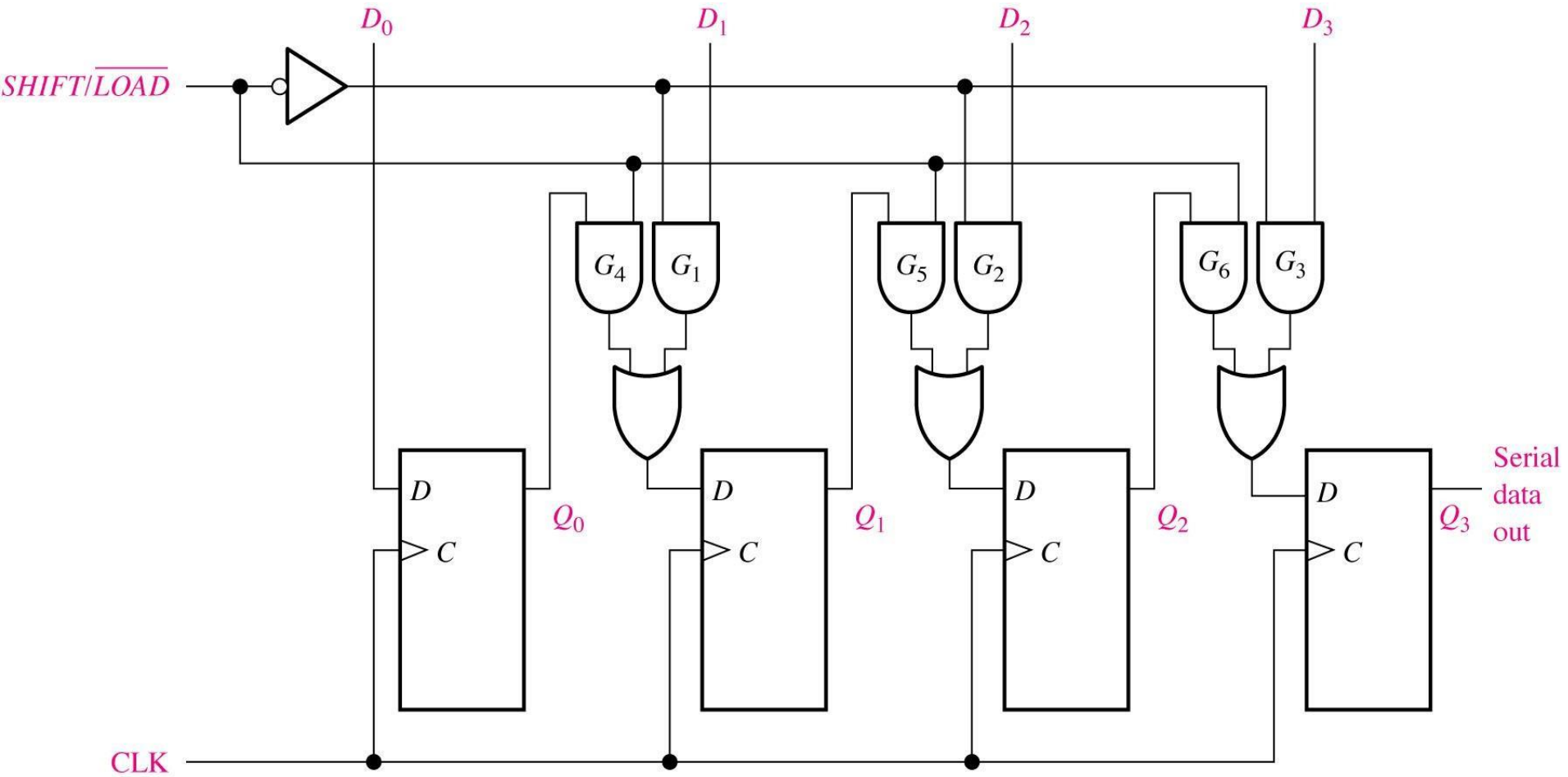
SIPO – Serial In Parallel Out Shift Register



PIPO – Parallel In Parallel Out Shift Register



PISO – Parallel In Serial Out Shift Register



PISO – Parallel In Serial Out Shift Register

Load Mode:

- ✓ When the *Shift* / $\overline{Load}$ line is Low, the AND gates G1, G2 and G3 become active. They will pass D1, D2, and D3 bits to the corresponding Flip Flops.
- ✓ On the low going edge of clock, the binary inputs D0, D1, D2 and D3 will get loaded into corresponding flip flops. Thus parallel loading takes place.

PISO – Parallel In Serial Out Shift Register

Shift Mode:

- ✓ When the *Shift* / $\overline{Load}$ line is High, the AND gates G1, G2 and G3 become inactive. Hence parallel loading of data becomes impossible.
- ✓ But AND gates G4, G5 and G6 become active. Therefore the shifting of data from left to right bit by bit on application of clock pulses
- ✓ Thus the parallel in serial out operation takes place

Shift register:

- A register capable of shifting its binary information either to the right or to the left.
- The logical configuiration of shift register consists of a chain of flipflop connected in cascade.
- A flipflop receives a common clock pulse which causes the shift from one stage to another.

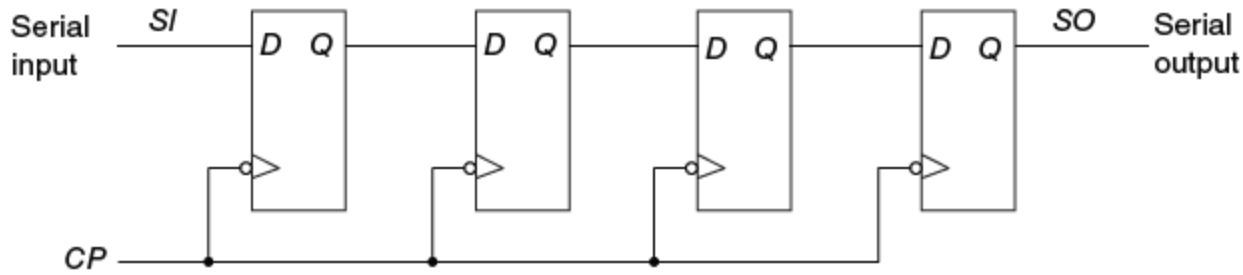
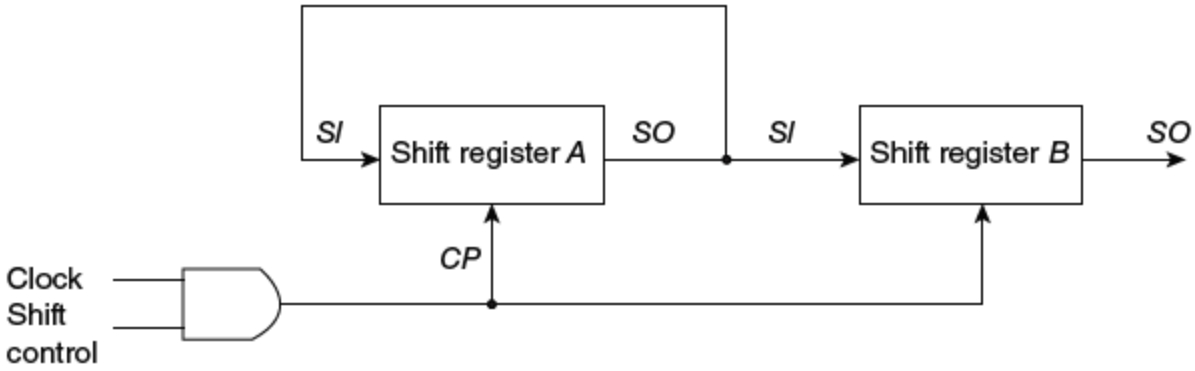


Figure 7-7 Shift register

Serial transfer:

- A digital system is said to be operate in a serial mode when information is transferred one bit at a time.
- The content of one register is transferred to another by shifting the bit from one register to another.
- The serial transfer of information from register A to register B is is done with shift register as shown in block diagram.
- The serial output of register A (S0) goes to serial input of register A (Si) of register B
- To prevent the loss of information stored in the source register, the A register is made to circulate the information by connecting the serial output to the input terminal.



(a) Block diagram

- Assume the binary content of A before the shift is 1011 and that of B is 0010.
- The serial transfer from A to B will occur in 4 steps as shown in table.
- After the first pulse T1 the rightmost bit of A is shifted into the leftmost bit of B and at the same time , this bit is circulated into the leftmost position of A.
- Once the bit of A and B are shift to right, the previous serial output from B is lost.

Timing pulse	Shift register A	Shift register B							Serial output of B
Initial value	1	0	1	1	0	0	1	0	0
After T_1	1	1	0	1	1	0	0	1	1
After T_2	1	1	1	0	1	1	0	0	0
After T_1	0	1	1	1	0	1	1	0	0
After T_4	1	0	1	1	1	0	1	1	1

- Ring counter:

- A type of counter in which the output of the last flipflop is connected as an input to the first flipflop is known as Ring Counter.
- The input is shifted between the flipflops n ing shape so it is called as ring counter.
- A ring counter is a synchronous counter.

- Johnson counter:
- Johnson counter as a reverse ring counter. In other words, feedback from the last flipflop is fed inversly to the data input of the first flipflop.
- For example for a D- flipflop shift register, the Q’ output of the last flipflop is fed to the D input of the first flipflop.
- The Mod of the johnson counter is ‘2n’, n is the bit size of the counter.Mod is the maximum number of states a counter can obtain.

- Advantages:

- More output as compared to ring counter.
- It has the same number of flip flop but it can count twicw the number of states the ring counter can count.
- It count the data in the continuous loop.
- It only needs half the number of flip flops compared to the standard ring counter for the same MOD.

- Disadvantages:

- Only 8 of the 15 states are being used.
- It doesnt count in binary sequence.

Arithmetic and Logic unit:

Q) Define ALU with block diagram.

- An arithmetic Logic unit (ALU) multi-operation, combinational logic digital function.
- It can perform a set of basic operation and a set of logic operation.
- Figure below shows the block diagram of 4 bit ALU. The four bit data input from 'A' are combined with 4 input from 'B' to generate 8 operation at the F output.

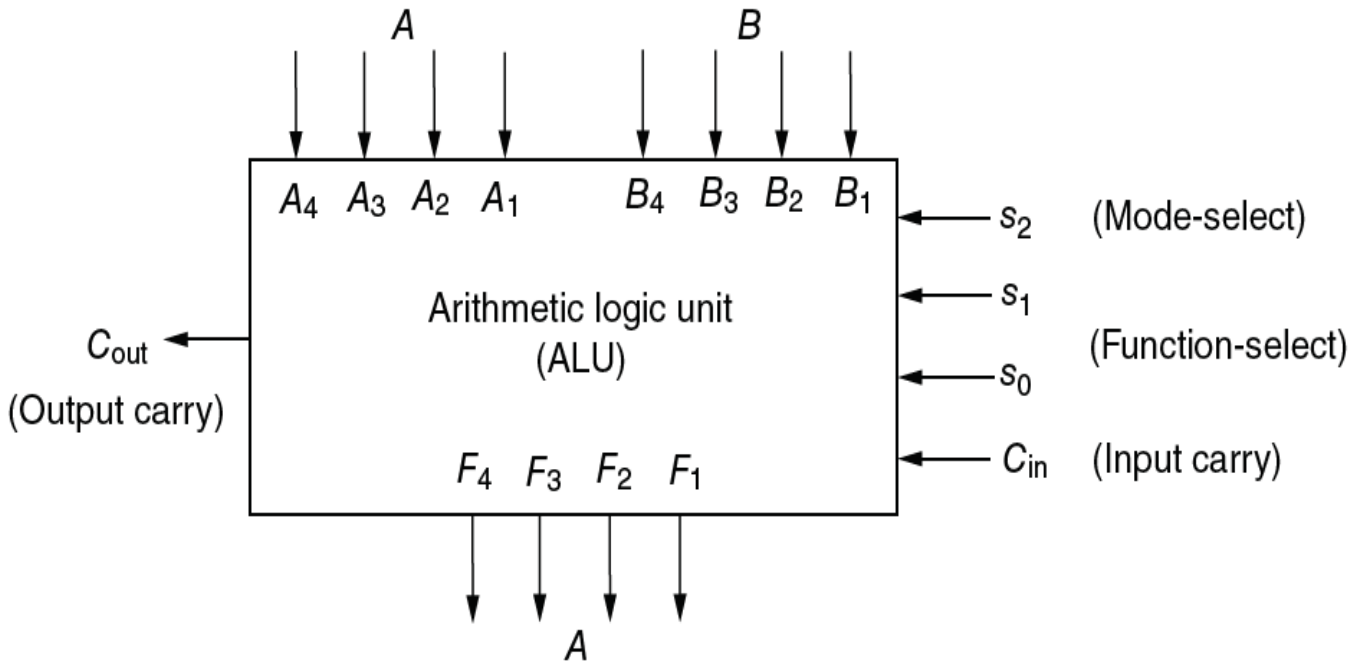


Figure 9-5 Block diagram of a 4-bit ALU

- Selection line s_2 is used for mode select to distinguish between arithmetic and logic operation.
- Selection line s_1 and s_0 specify the particular arithmetic or logic operation to be generated.
- With three selection variable, it is possible to specify four arithmetic operation and four logic operation.
- The input and output carries have meaning only during an arithmetic operation.
- The fourth selection variable c_{in} can

Design of Arithmetic circuit:

Q)Draw an arithmetic circuit logic diagram with function table that perform 8 different operation.

- The basic component of arithmetic section of ALU is a parallel adder.
- A parallel adder is constructed with number of flipflop. By controlling the data input to the parallel adder, it is possible to obtain 8 different types of arithmetic operation.

1. **Addition:** Arithematic addition is

2. **Addition with carry:** with c_{in} =1 in addition.
3. **A plus 1's complement of B:** By complementing all the bit of input B with c_{in}=0.
4. **Subtraction:** By making cin = 1, it is possible to add 1 to the A plus 1's complement of B which produces the sum of A plus 2's complement of B. This operation is similar to subtraction if input carry is discarded.
5. **Transfer A:** if we force all the bit of B terminal to 0 then it transfers input A into output F.
6. **Increament A:** By making c_{in} = 1 and all bit of B terminal to 0, we obtain F= A+1 which is increament of A.
7. **Decreament A:** If we insert all the bit of B terminal to with c_{in} = 0 then this produce a

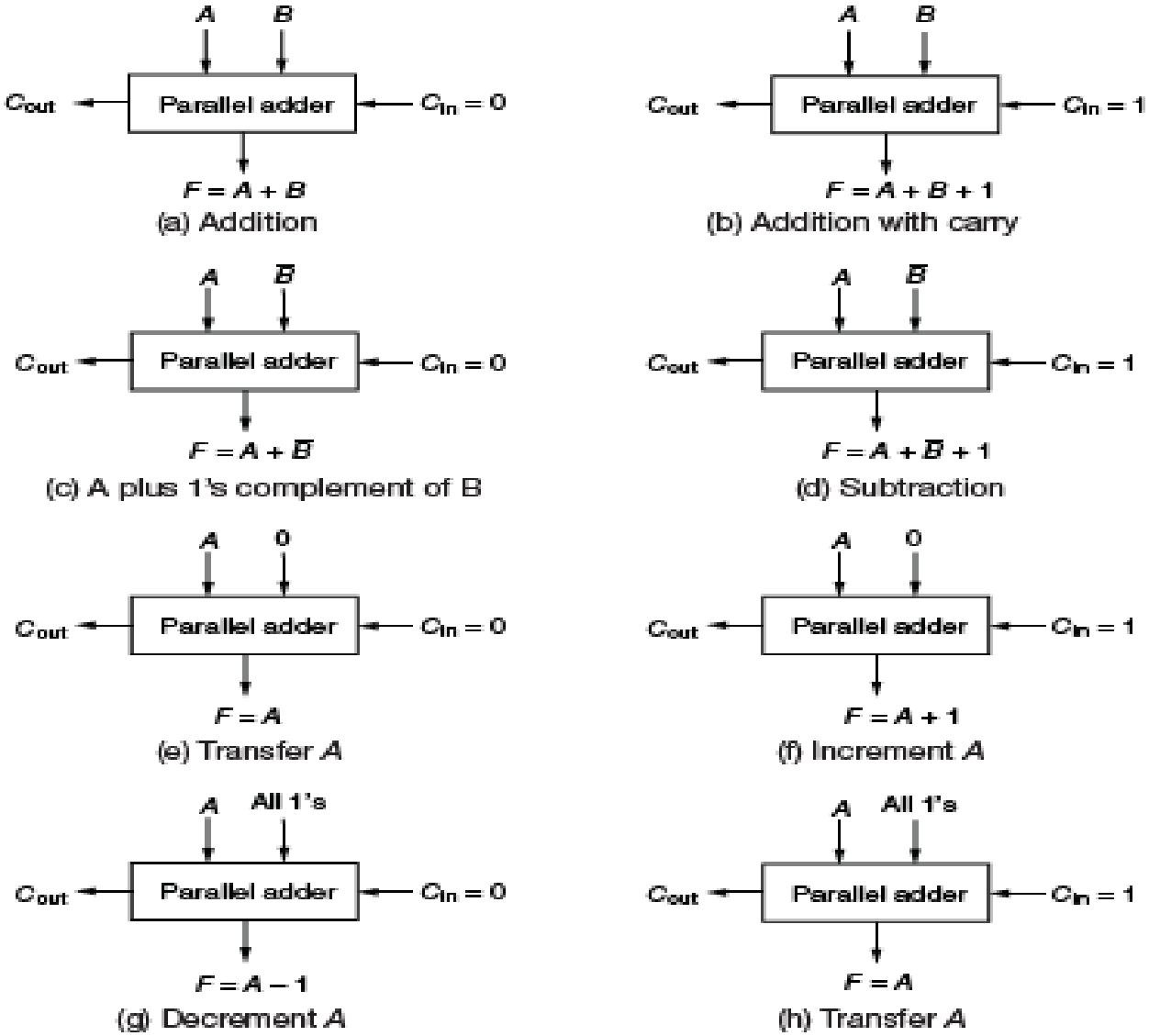


Figure 9-6 Operations obtained by controlling one set of inputs to a parallel adder

Function table for the arithmetic circuit:

Function select			Y equals	Output equals	Function
s_1	s_0	C_{in}			
0	0	0	0	$F = A$	Transfer A
0	0	1	0	$F = A + 1$	Increment A
0	1	0	B	$F = A + B$	Add B to A
0	1	1	B	$F = A + B + 1$	Add B to A plus 1
1	0	0	$\overline{B}$	$F = A + \overline{B}$	Add 1's complement of B to A
1	0	1	$\overline{B}$	$F = A + \overline{B} + 1$	Add 2's complement of B to A
1	1	0	All 1's	$F = A - 1$	Decrement A
1	1	1	All 1's	$F = A$	Transfer A

When s_1s_0= 0(
y_i =0
When s_1s_0= 0'
y_i= B_i
When s_1s_0= 1(
y_i= B_i'
When s_1s_0= 1'
y_i= all 1's

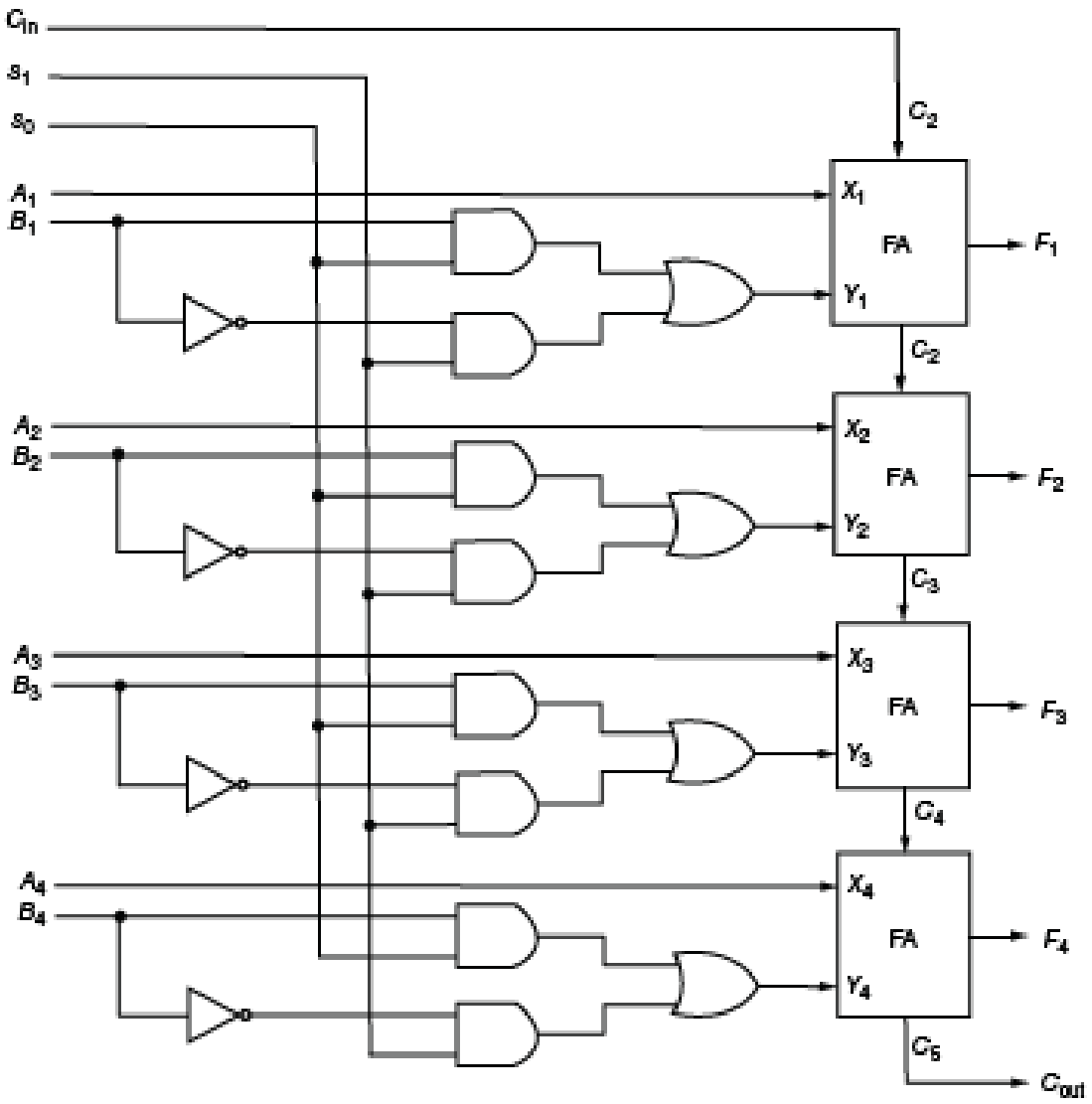
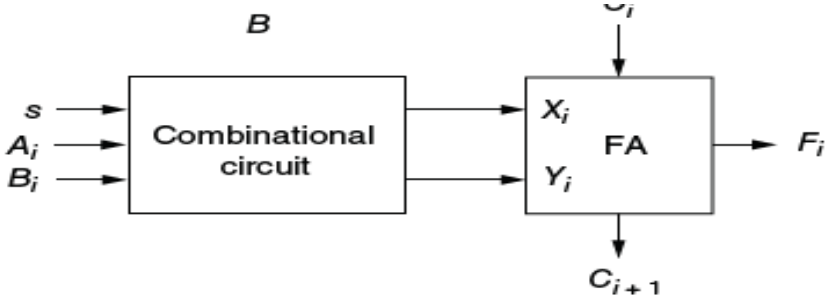


Figure 9-8 Logic diagram of arithmetic circuit

Q) Design an adder/ subtractor circuit with one selection variable and two input A and B, when s=0 the circuit performs A+B. when S=1 the circuit performs A-B by taking the 2's complement of B

The arithmetic circuit and truth table for given condition will be as:

s	X_i	Y_i	C_{in}
0	A_i	B_i	0
1	A_i	B'_i	1



(b) Specifying combinational circuit

s	A_i	B_i	X_i	Y_i
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

$X_i = A_i$

$Y_i = B_i \oplus s$

$C_{in} = s$

(c) Truth table and simplified equations

Figure 9.9 Derivation of an adder/subtractor circuit

When s=0 xi and yi for each full adder must be equal to the external input Ai and Bi Respectively. When s =1, xi = Ai and yi = Bi'. The input carry must be equal to value of s.

The logic diagram will be as:

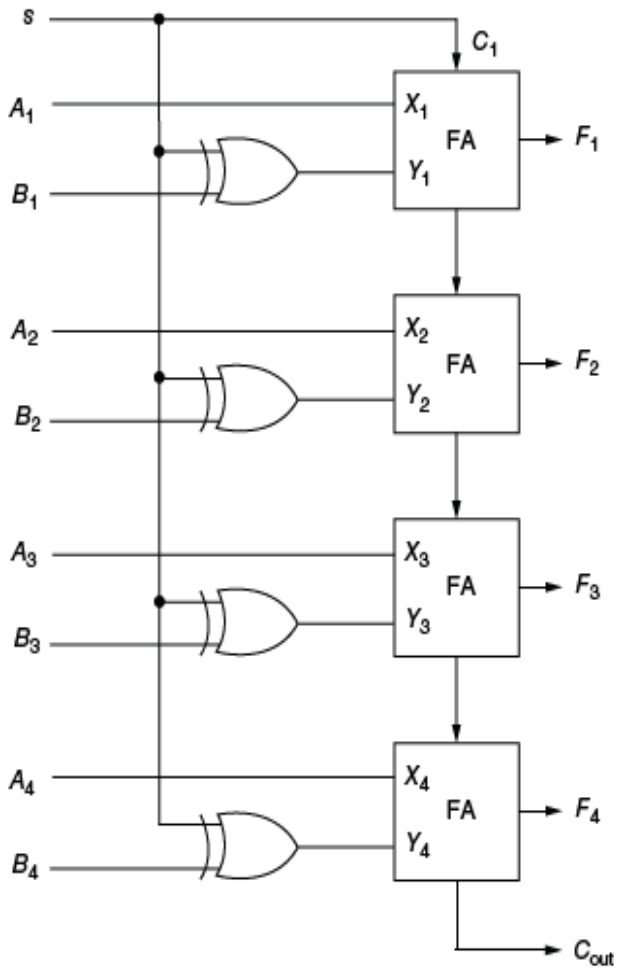


Figure 9-10 4-bit adder/subtractor circuit

Shift register:

- A register capable of shifting its binary information either to the right or to the left.
- The logical configuiration of shift register consists of a chain of flipflop connected in cascade.
- A flipflop receives a common clock pulse which causes the shift from one stage to another.

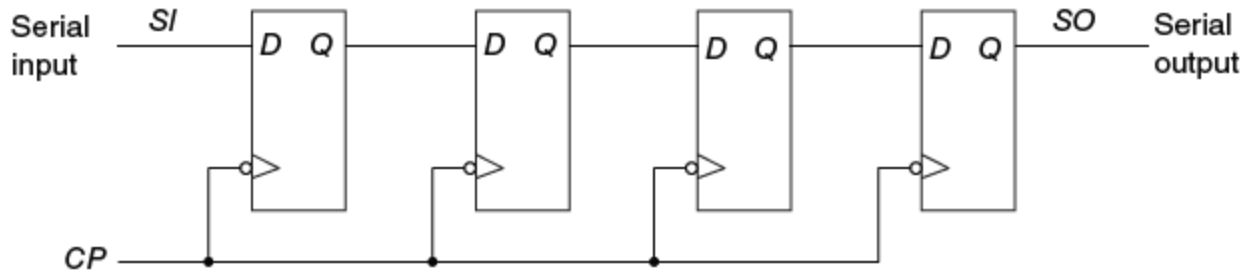
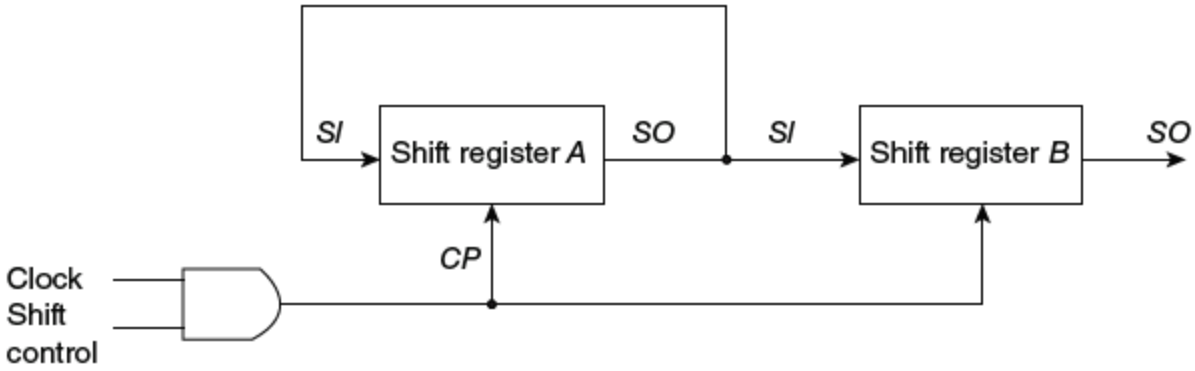


Figure 7-7 Shift register

Serial transfer:

- A digital system is said to be operate in a serial mode when information is transferred one bit at a time.
- The content of one register is transferred to another by shifting the bit from one register to another.
- The serial transfer of information from register A to register B is is done with shift register as shown in block diagram.
- The serial output of register A (S0) goes to serial input of register A (Si) of register B
- To prevent the loss of information stored in the source register, the A register is made to circulate the information by connecting the serial output to the input terminal.



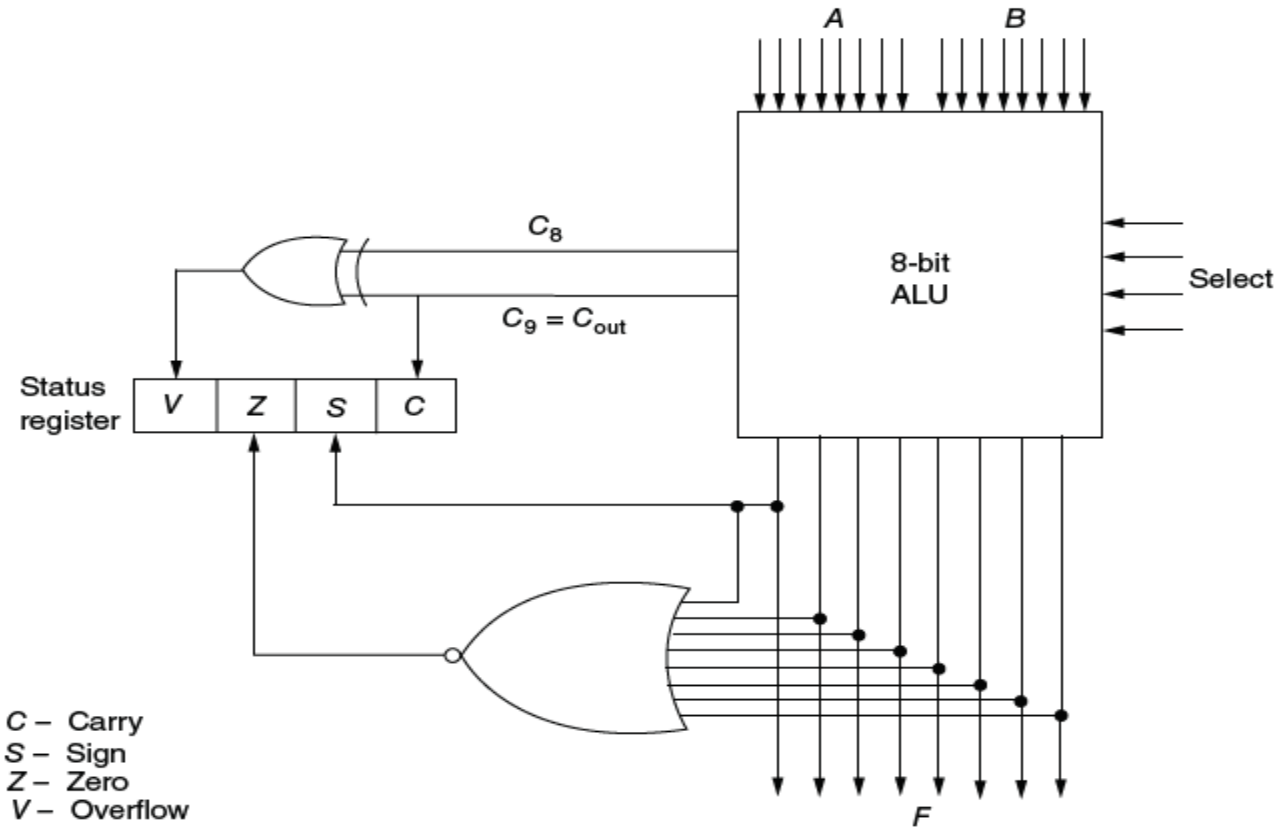
(a) Block diagram

- Assume the binary content of A before the shift is 1011 and that of B is 0010.
- The serial transfer from A to B will occur in 4 steps as shown in table.
- After the first pulse T1 the rightmost bit of A is shifted into the leftmost bit of B and at the same time , this bit is circulated into the leftmost position of A.
- Once the bit of A and B are shift to right, the previous serial output from B is lost.

Timing pulse	Shift register A	Shift register B							Serial output of B
Initial value	1	0	1	1	0	0	1	0	0
After T_1	1	1	0	1	1	0	0	1	1
After T_2	1	1	1	0	1	1	0	0	0
After T_1	0	1	1	1	0	1	1	0	0
After T_4	1	0	1	1	1	0	1	1	1

Status register:

Figure below shows the block diagram of an 8 bit Alu with a 4 bit status register.



- The four status bits or flag bits are symbolized by C , S , Z and V.
- The bit are set or cleared as a result of an operation performed in the ALU.

1. Bit C is set if the output carry of the ALU is 1. It is cleared if the output carry is 0.
2. Bit S is set if the highest-order bit of the result in the output of the ALU (the sign bit) is 1. It is cleared if the highest-order bit is 0.
3. Bit Z is set if the output of the ALU contains all 0's, and cleared otherwise. $Z = 1$ if the result is zero, and $Z = 0$ if the result is nonzero.
4. Bit V is set if the exclusive-OR of carries C_8 and C_9 is 1, and cleared otherwise. This is the condition for overflow when the numbers are in sign-2's-complement representation (see Section 8-6). For the 8-bit ALU, V is set if the result is greater than 127 or less than -128.