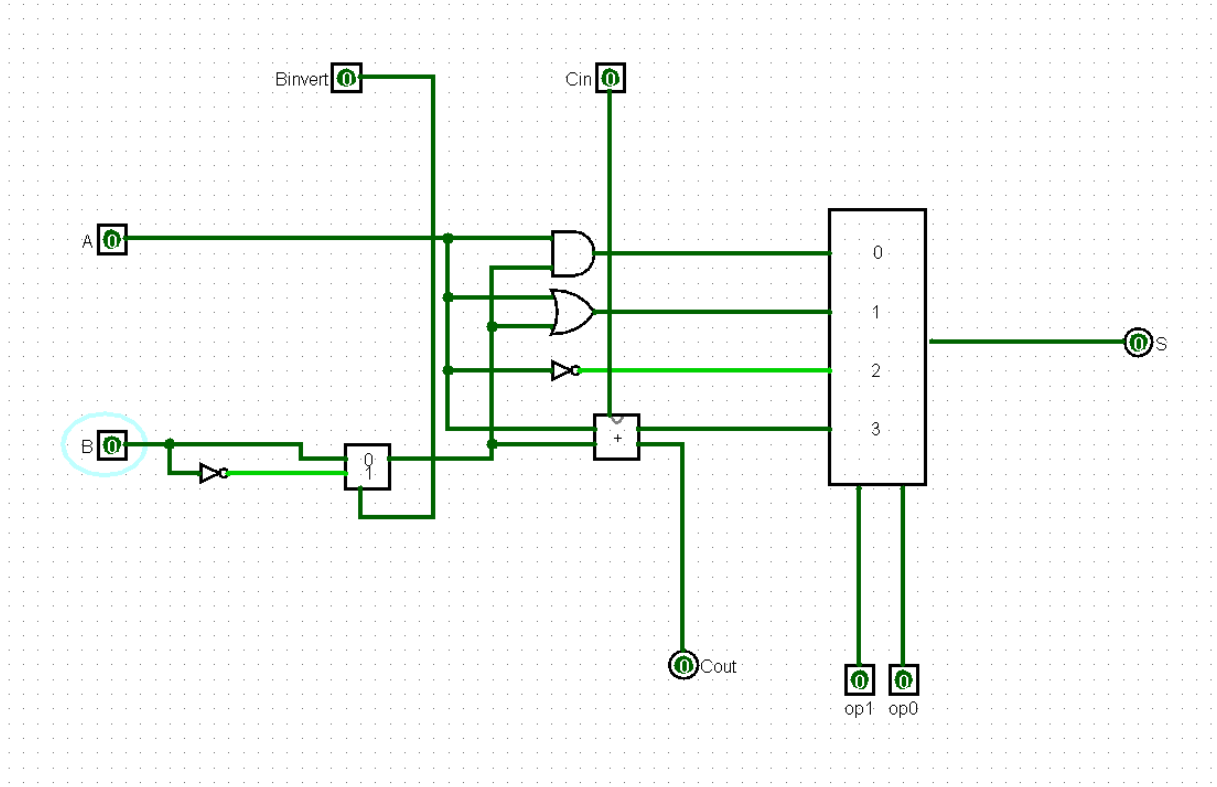
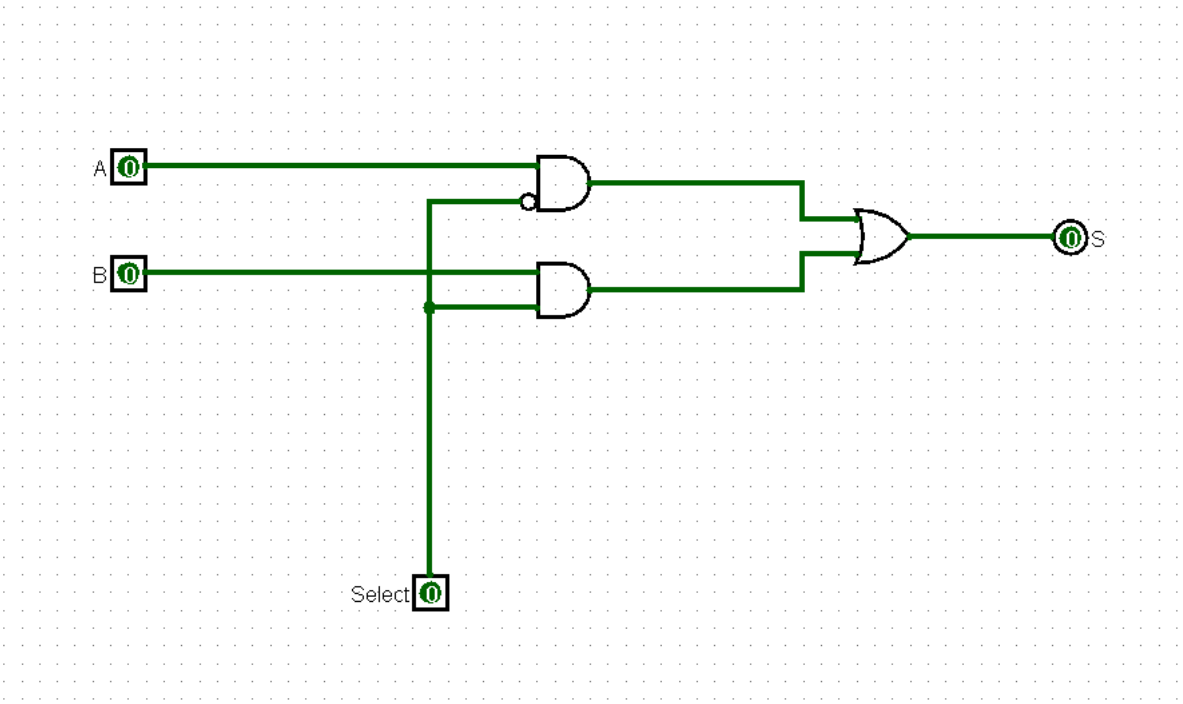
Arquitetura de Computadores 2 - Relatório 03

Grupo : Filipe Arthur, Henrique Augusto, Lucas Diniz

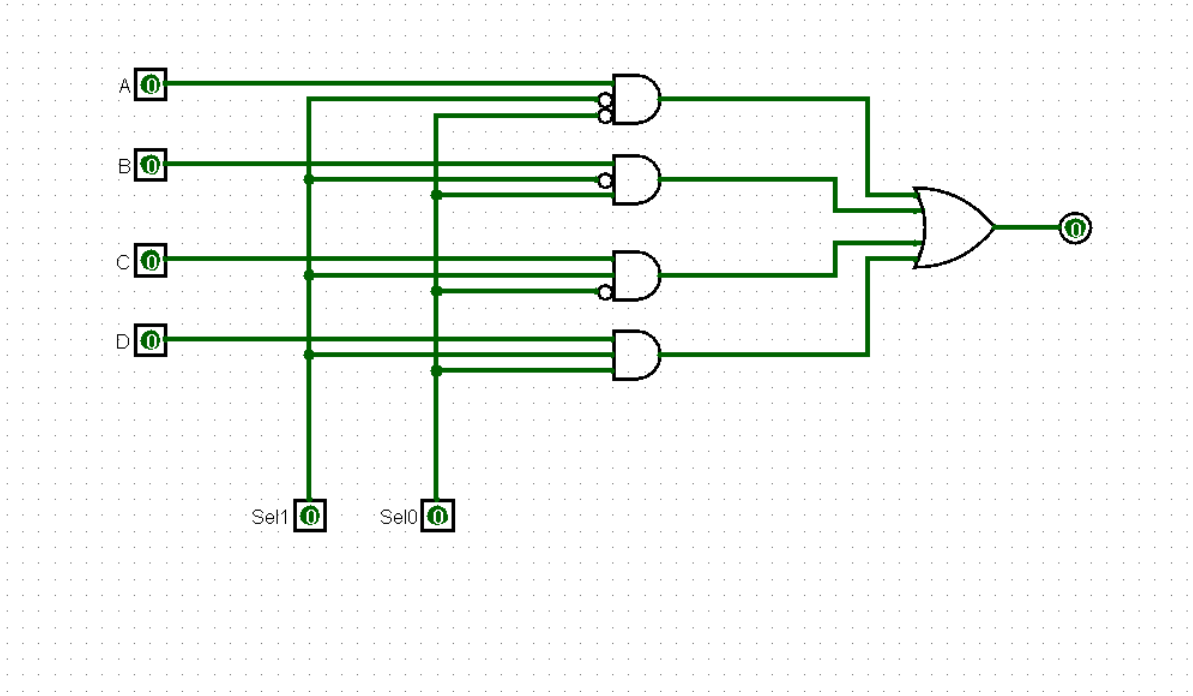
ALU 1 bit (Logisim)



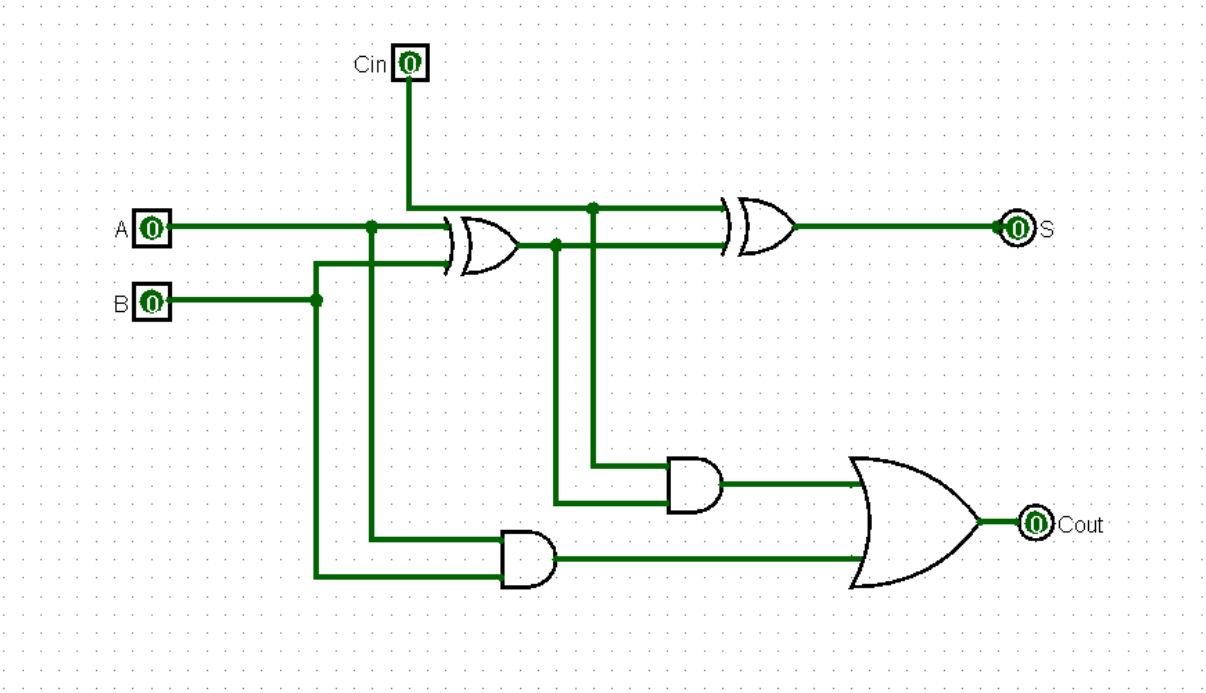
MUX 1 bit de seleção (Logisim)



MUX 2 bits de seleção (Logisim)

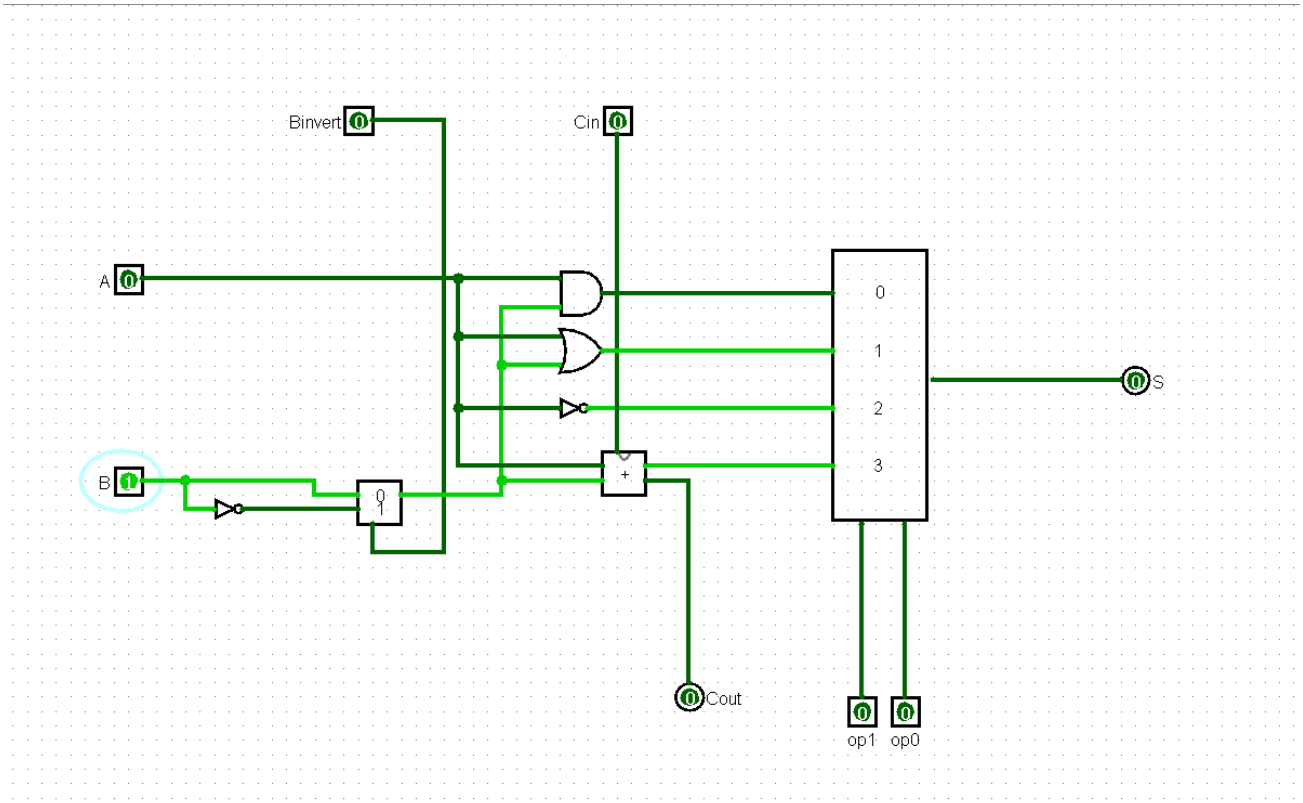


Somador completo 1 bit (Logisim)

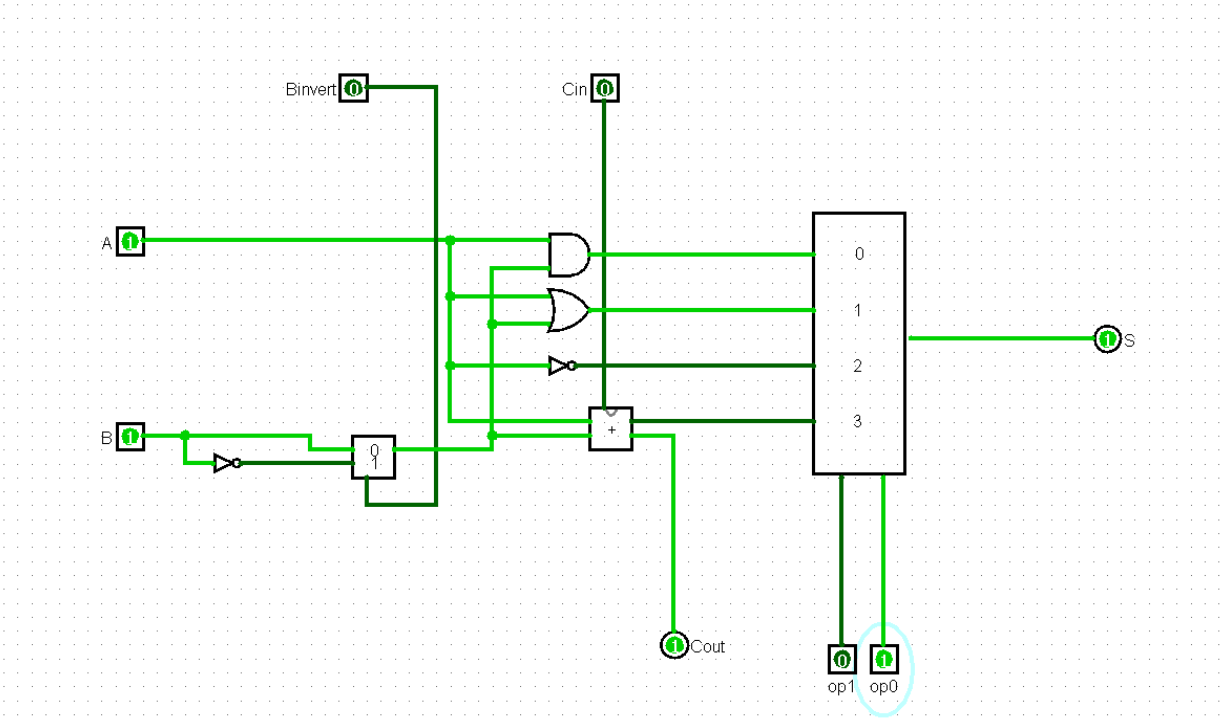


Teste do algoritmo :

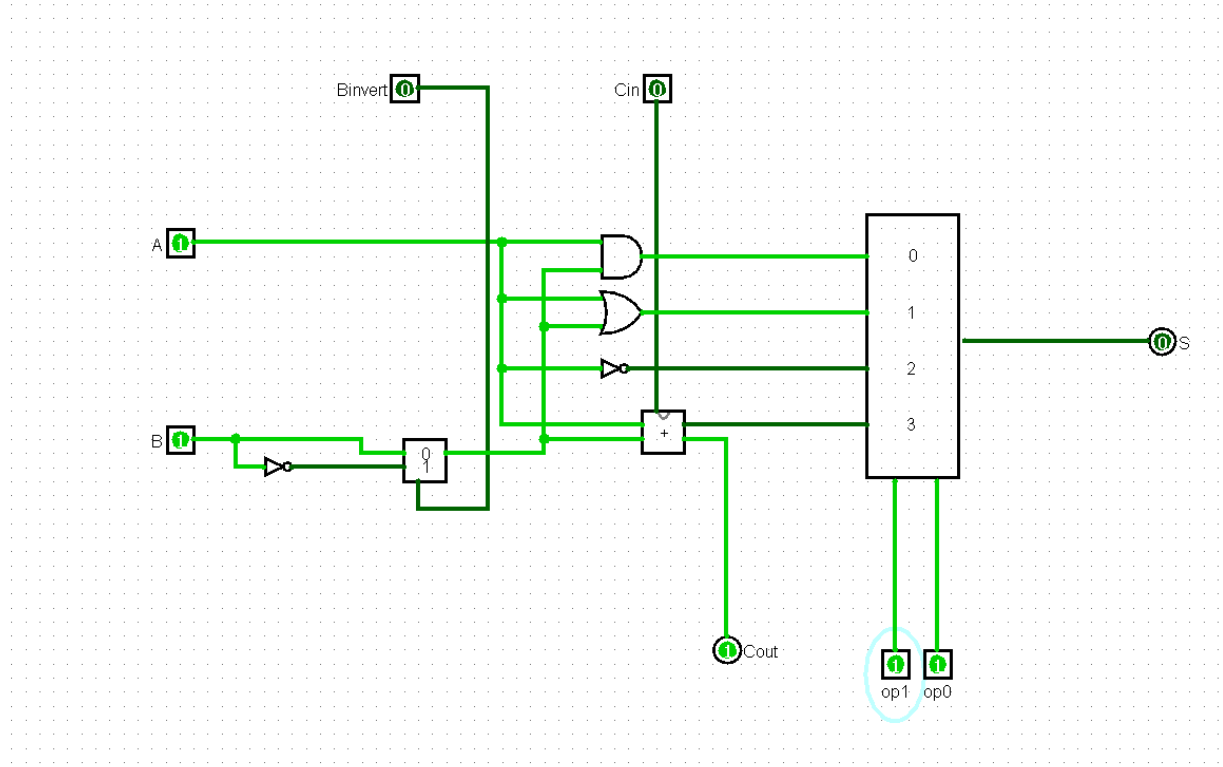
A=0;
B=1;
AND(A,B);



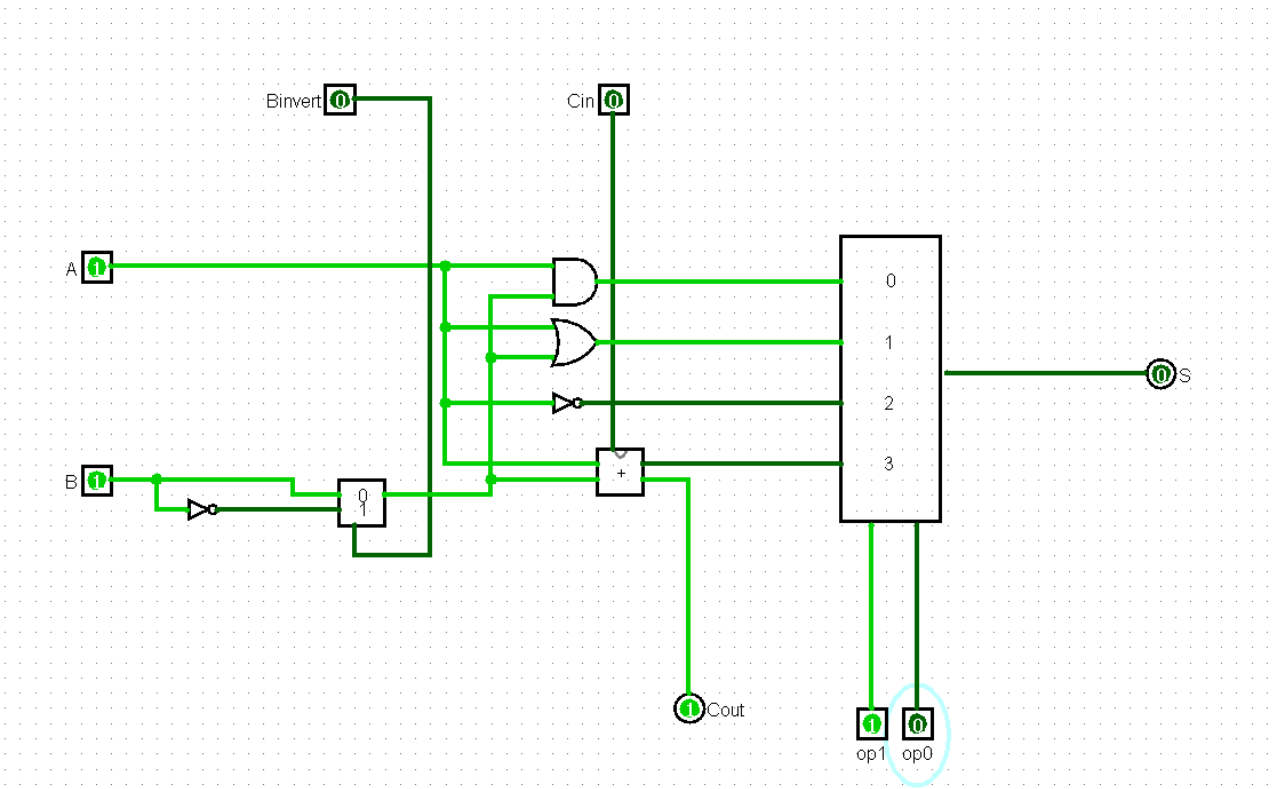
A=1;
B=1;
OR(A,B);



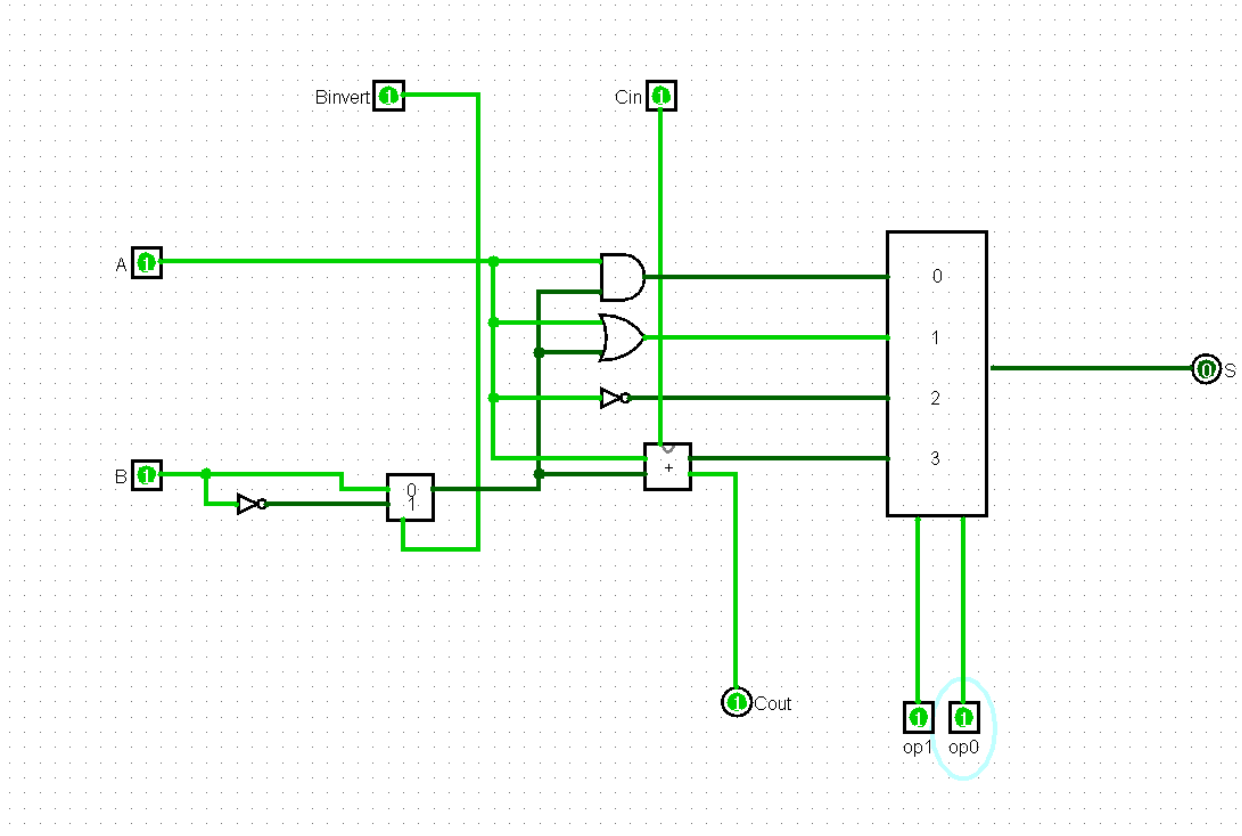
SOMA(A,B);



NOT(A);


Binvert
Cin
A
B
0
1
2
3
S
Cout
op1
op0

SOMA (A,-B);


Binvert
Cin
A
B
0
1
2
3
S
Cout
op1
op0

ALU de 4 bits (Logisim)

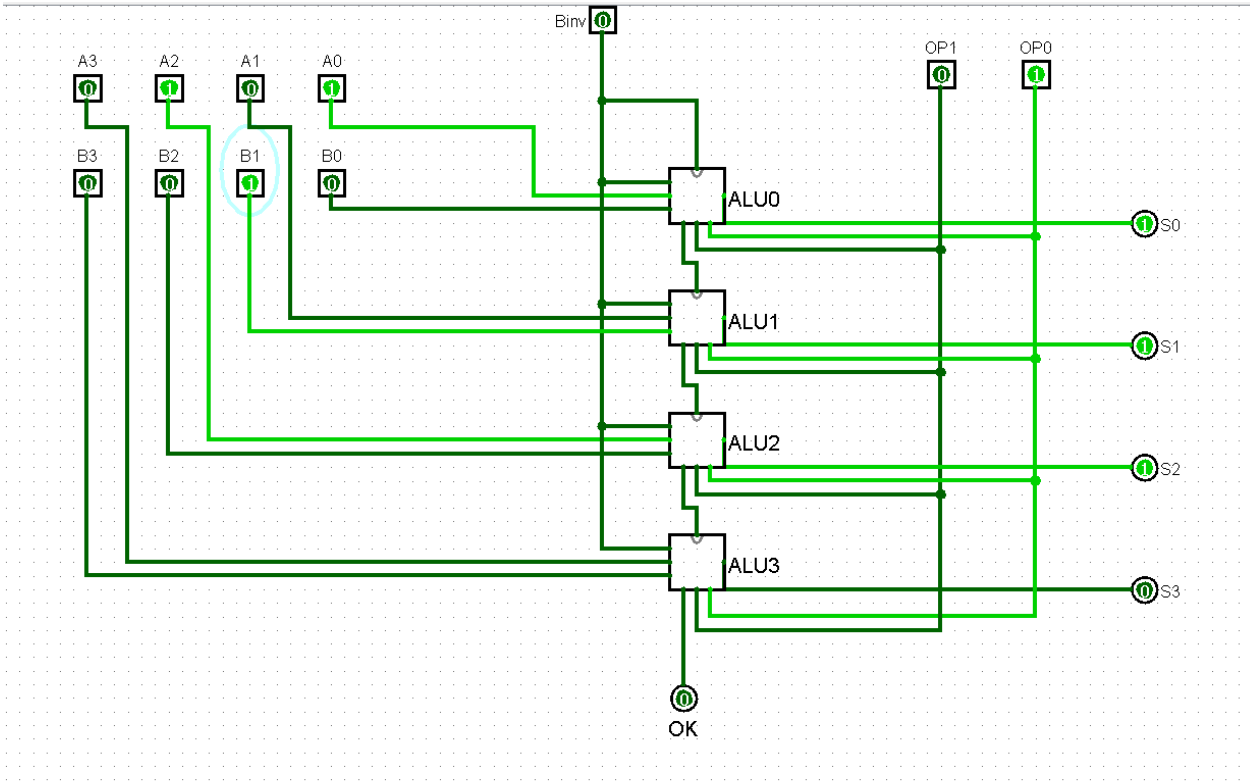


Tabela verdade ALU

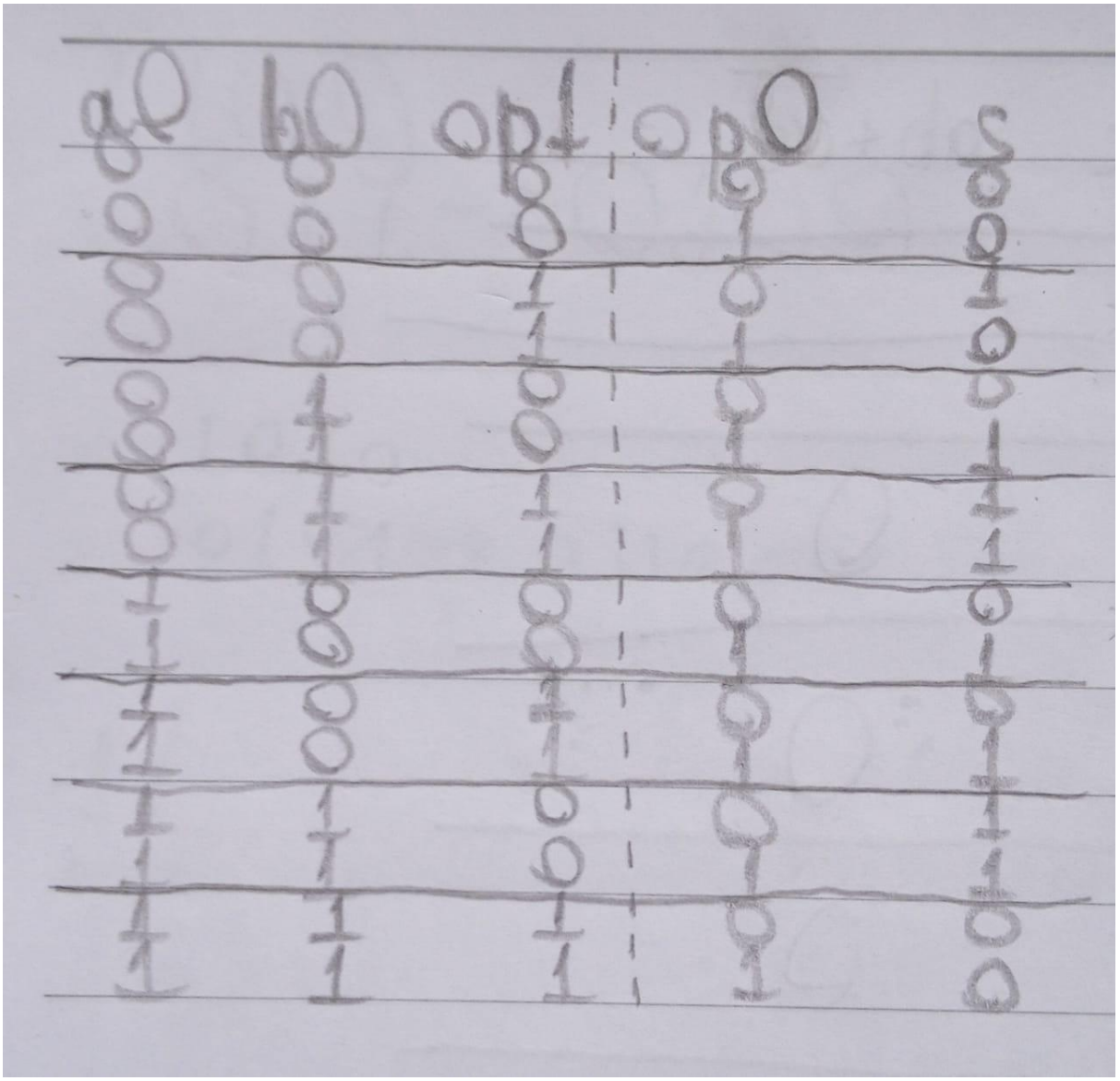
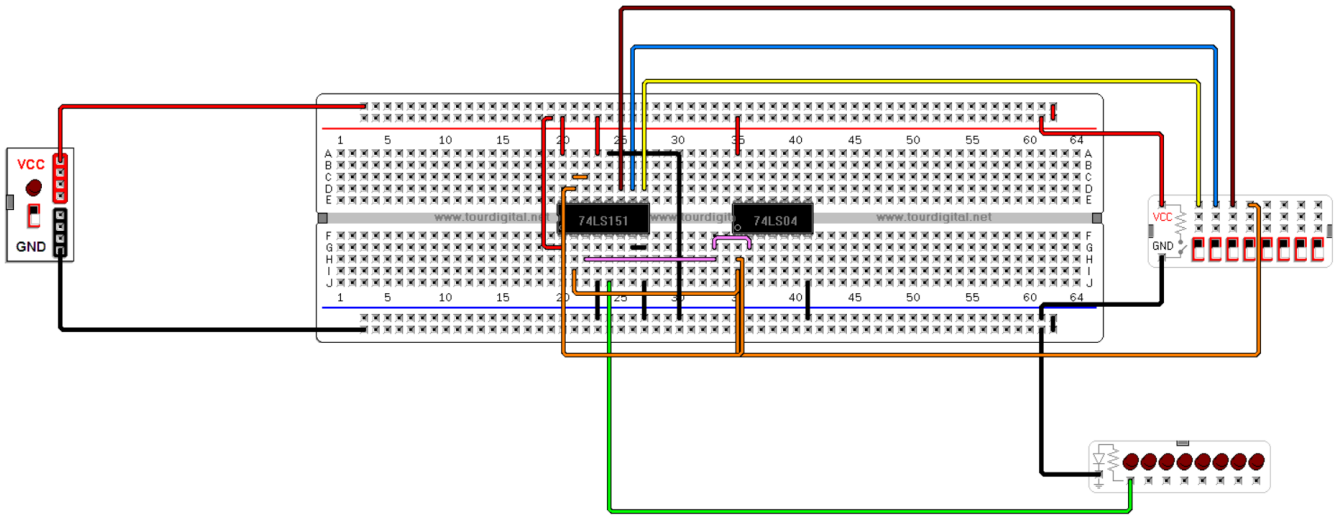


Tabela do algoritmo

A	B	C
Instrução Realizada	Binário	Val. Hexa
And (a,b)	10 01 00	24
Or (a,b)	00 00 11	3
NAND (a,b)	00 01 01	5
XOR (a,b)	00 01 10	6

Circuito ALU (Simulador 97)



Entrada a0 : Fio amarelo
Entrada b0 : Fio azul
Entrada op1 : Fio marrom
Entrada op0 : Fio laranja
op0 negado : Fio rosa
Saída S : Fio verde
Vcc : Fio vermelho
Gnd : Fio preto