EE141-Spring 2012 Digital Integrated Circuits

Instructor: Jan Rabaey

WeFr 9am-10:30am
254 Sutardja-Dai Hall

ADMINISTRATIVIA

What is this class all about?

- **Introduction to digital integrated circuit design engineering**
  - Key concepts needed to be a good digital IC designer
  - Design creativity
- **Models that allow reasoning about circuit behavior**
  - Allow analysis and optimization of the circuit's performance, power, cost, etc.
  - Understanding circuit behavior is key to making sure it will actually work
- **Teach you how to make sure your circuit works**
  - Do you want your transistor to be the one that screws up a 1 billion transistor chip?

What will you learn?

- Understanding, designing, and optimizing digital circuits for various quality metrics:
  - Performance (speed)
  - Power dissipation
  - Cost
  - Reliability

Detailed Topics

- CMOS devices and manufacturing technology
- CMOS gates
- Combinational and sequential circuits
- Arithmetic building blocks
- Interconnect
- Memories
- Propagation delay, noise margins, power
- Timing and clocking
- Design methodologies

Practical Information

- Instructor
  - Prof. Jan Rabaey

    563 Cory Hall, 643-3986, jan at eecs

    Office hours: We 10:30pm-noon
- TAs:
  - Rikky Muller, rikky at eecs (OH: TBD)
  - Wen Li, wenli at eecs (OH: TBD)
- Reader:
  - TBD

Discussions and Labs

- Discussion sessions
  - Mo 4-5pm, (521 Cory)
- Labs (125 Cory)
  - Mo 1-4pm (Rikky)
  - Th 2-5pm (Wen)
  - Machines to left of double doors, with larger monitors
- Please choose one lab session and stick with it!

Class Organization

- 9-10 assignments
- One design project (with multiple phases)
- Labs: 5 software
- 2 midterms, 1 final
  - Midterm 1: Fr Febr 17
  - Midterm 2: Fr March 23
  - Final: Mo May 7, 7-10pm!

Course Information

- Basic Source of Information: bspace (ee141 Spring 2012)
  - Class and lecture notes
  - Assignments and solutions
  - Lab and project information
  - Exams
  - Many other goodies …
  - Everyone enrolled should have access – let us know if you need to be added

Print only what you need: Save a tree!

Course Information

- For interactions between faculty, GSIs and fellow students – we are joining the social networking age

This term we will be using **Piazza** for class discussion. The system is highly catered to getting you help fast and efficiently from classmates, the TA, and myself. Rather than emailing questions to the teaching staff, I encourage you to post your questions on Piazza.
If you have any problems or feedback for the developers, email **team@piazza.com**.

Find our class page at:
http://www.piazza.com/berkeley/spring2012/ee141.
(make sure to register ASAP if you don't want to miss all the action)

Some Important Announcements

- Can work together on homework
  - But you must turn in your own solution
- Lab reports due 1 week after the lab session
- Project is done in groups
- No late assignments
  - Solutions available shortly after due date/time
- Don't even think about cheating!

Grading Policy

- Homeworks: 10%
- Labs: 10%
- Projects: 20%
- Midterms: 30%
- Final: 30%

Class Material

- Textbook: "Digital Integrated Circuits – A Design Perspective", 2nd ed, by J. Rabaey, A. Chandrakasan, B. Nikolic
- Class notes: bSpace
- Lab Reader: bSpace
- Check web page for the availability of tools

Class Capturing

- Class is being captured for a

Course Webcast

- All lectures streamed life
- Also available in archive
- Check: http://webcast.berkeley.edu/courses.php
- However: Live experience has advantages

Software

- Cadence
  - Widely used in industry
  - Online tutorials and documentation
- HSPICE and Spectre for simulation

Getting Started

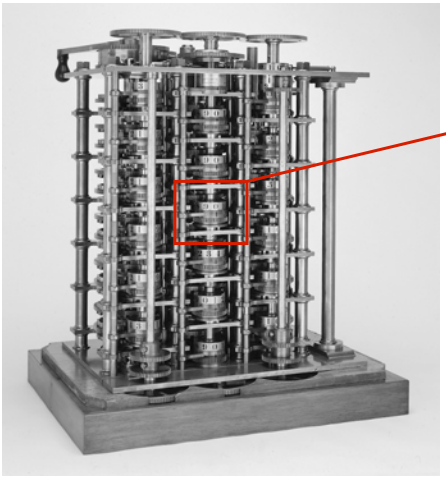
- Assignment 1: Getting SPICE to work – see web-page
- Due Wednesday, February 1, 5pm
- NO discussion sessions or labs this week.
- First discussion session on Monday
- First software lab in Week 3
- Make-up lecture time TBA!

Digital Integrated Circuits – From The Past to the Present

Introduction

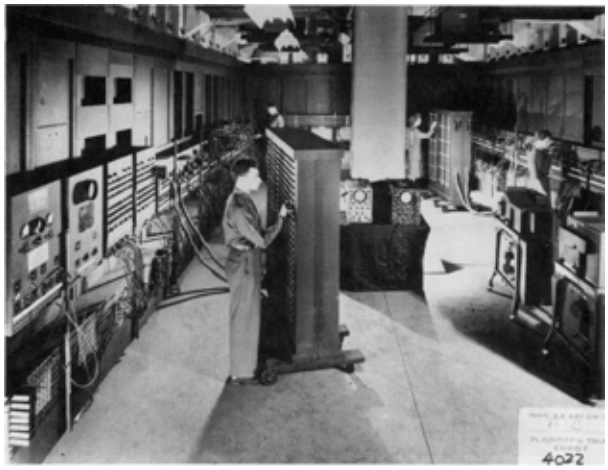
- Digital Integrated Circuit Design: The Past, The Present and The Future
  - What made Digital IC design what it is today
  - Why is designing digital ICs different today than it was before?
  - Will it change in the future?

The First Computer

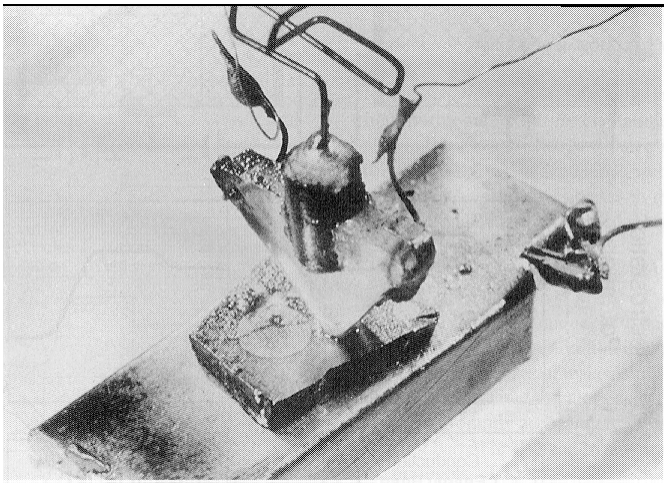


- The Babbage Difference Engine
  - 25,000 parts
  - cost: £17,470

ENIAC - The First Electronic Computer (1946)

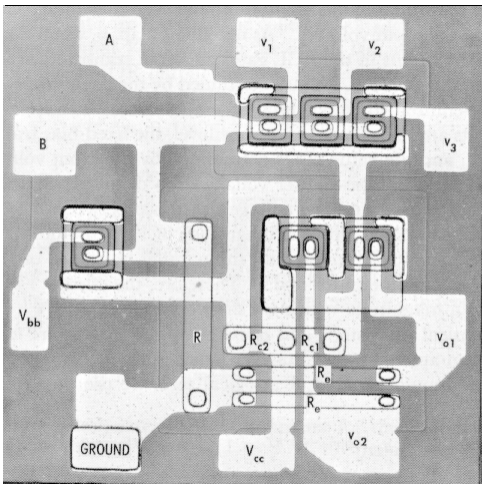


The Transistor Revolution



First transistor
Bell Labs, 1948

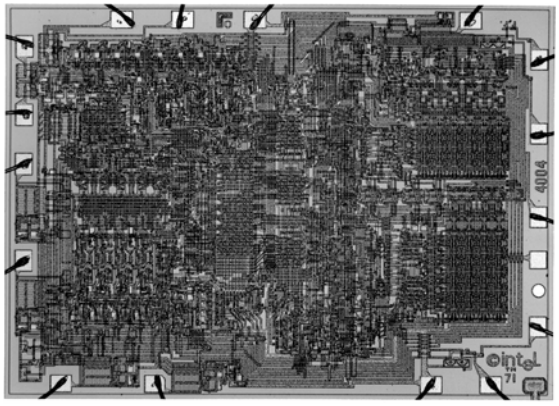
The First Integrated Circuits



Bipolar logic
1960's

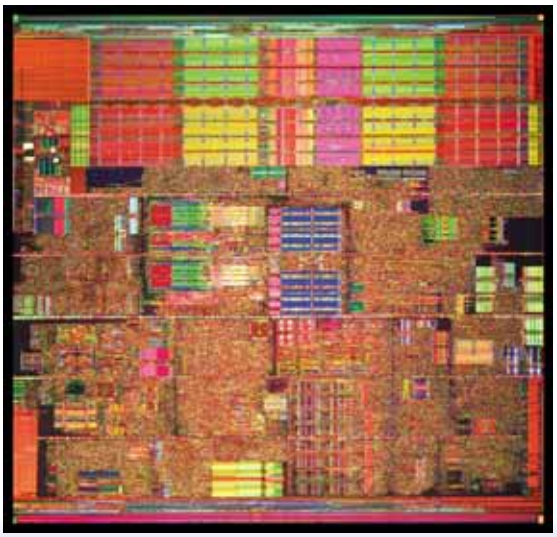
ECL 3-input Gate
Motorola 1966

Intel 4004 Microprocessor



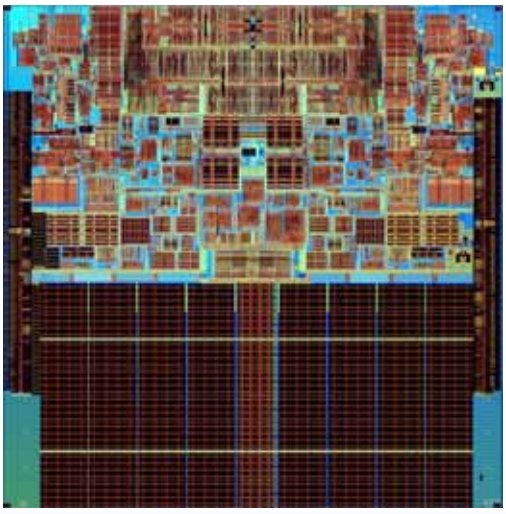
Intel, 1971.
2,300 transistors (12mm^2)
740 KHz operation
(10μm PMOS technology)

Intel Pentium 4 Microprocessor



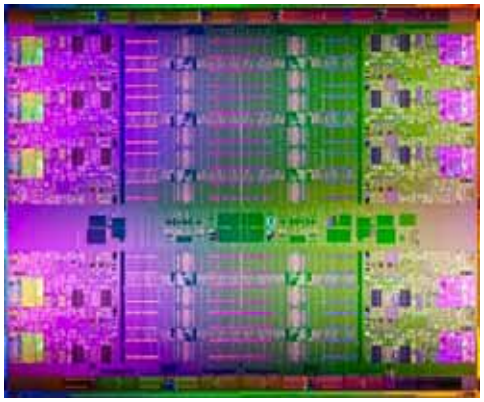
Intel, 2005.
125,000,000 transistors
(112mm^2)
3.8 GHz operation
(90nm CMOS technology)

Intel Core 2 Microprocessor



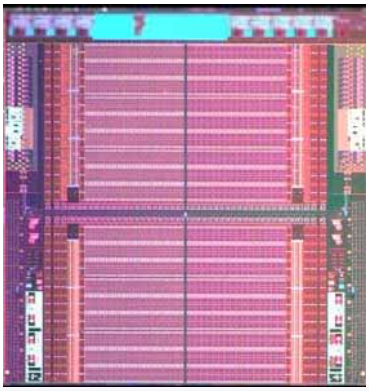
Intel, 2006.
291,000,000 transistors
(143mm^2)
3 GHz operation
(65nm CMOS technology)

Intel Xeon (E7-8800)

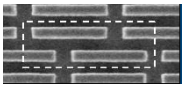


Intel, 2011.
2,600,000,000 transistors
(513mm^2)
2.4 GHz operation
(32nm CMOS technology)

Intel 22 nm Test Chip (2009)

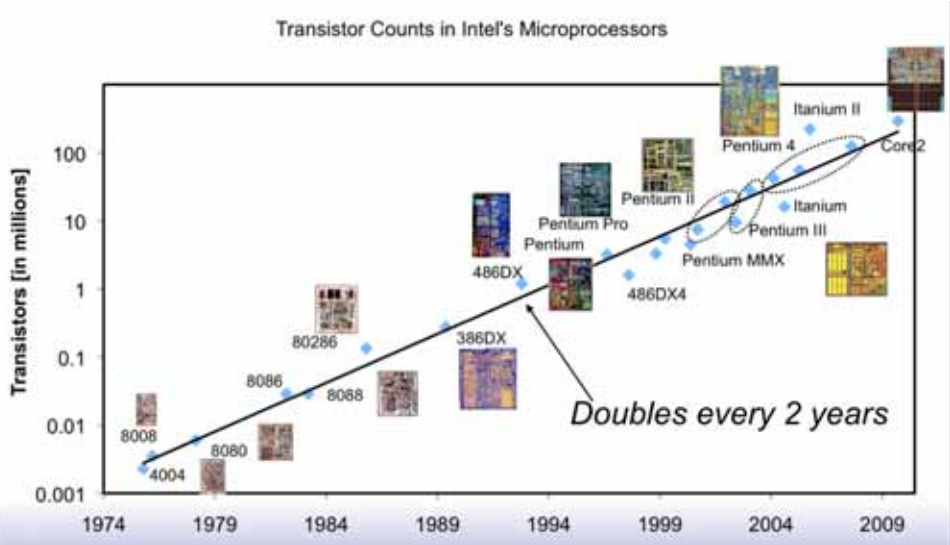


Intel, ~2009.
2,900,000,000 transistors
364Mb memory array

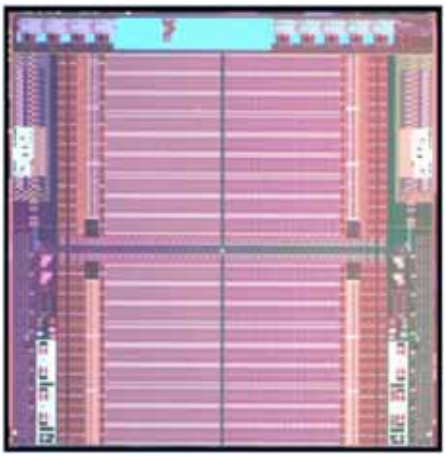


0.092μm^2 SRAM cell

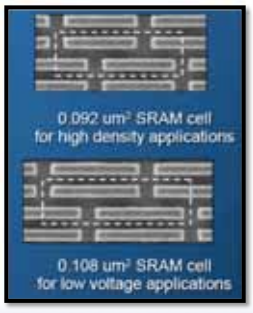
Transistor Counts



Intel SRAM Prototype Chip (2009)



- 22 nm
- 364 Mbyte SRAM
- > 2.9 Billion Transistors
- 3rd generation high-k + metal gate

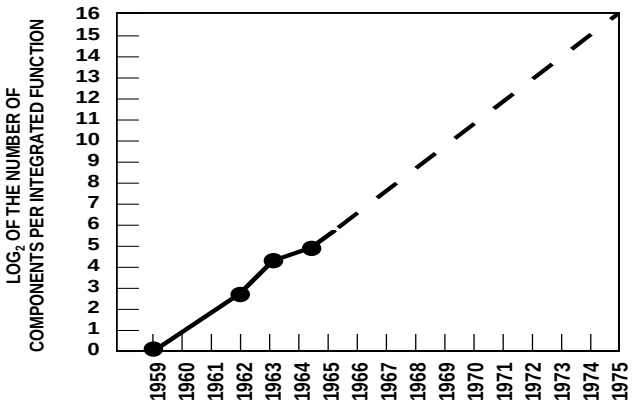


Moore's Law

Moore's Law

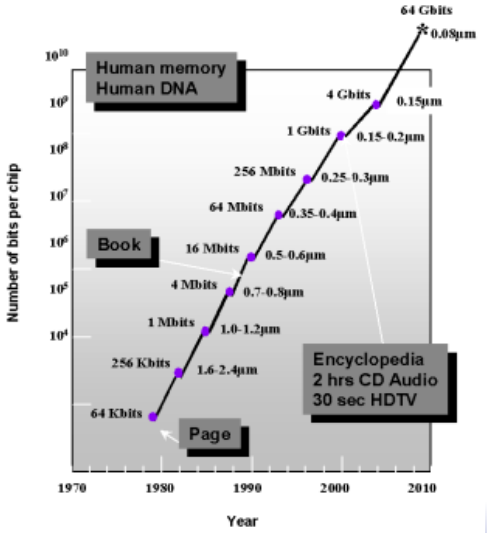
- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

Moore's Law

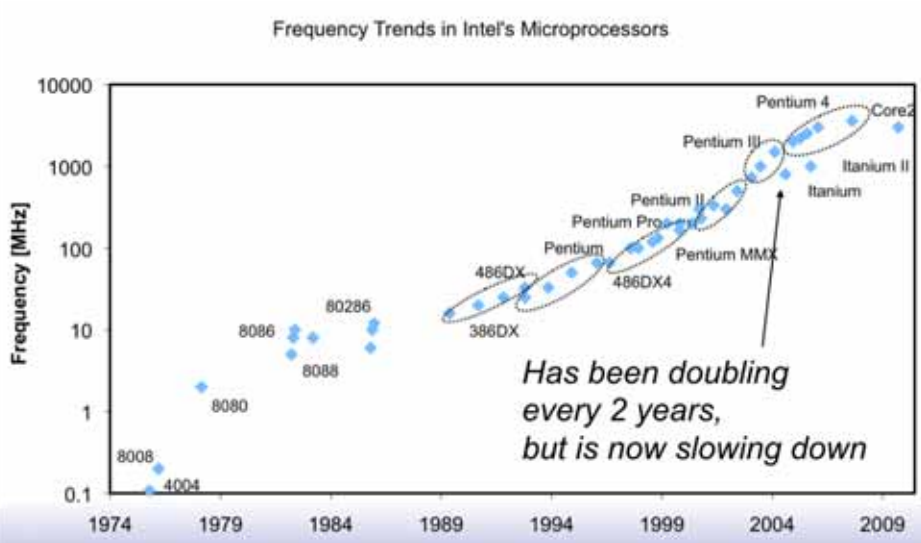


Electronics, April 19, 1965.

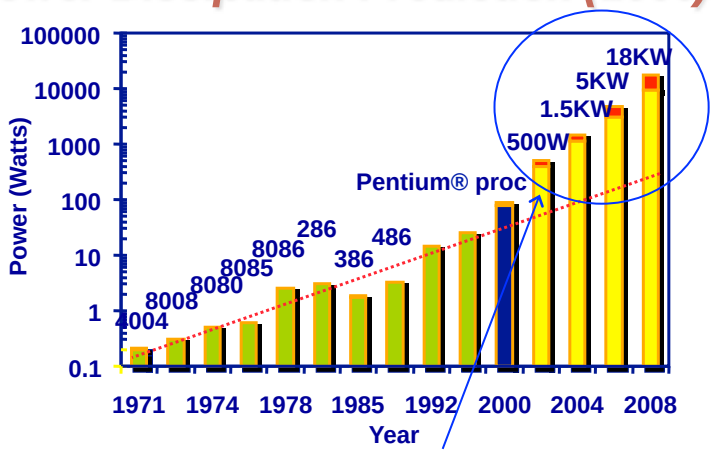
Evolution in Complexity



Frequency



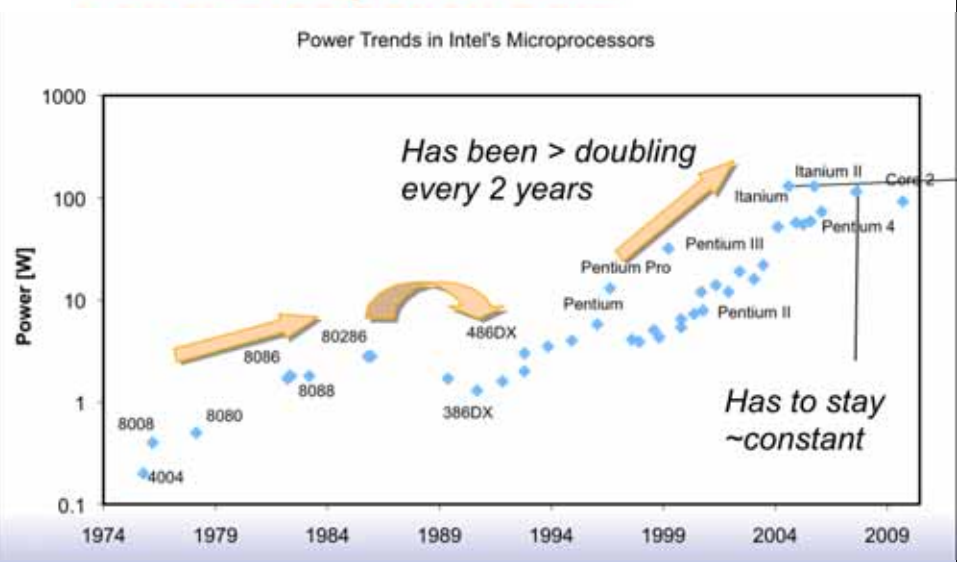
Power Dissipation Prediction (2000)



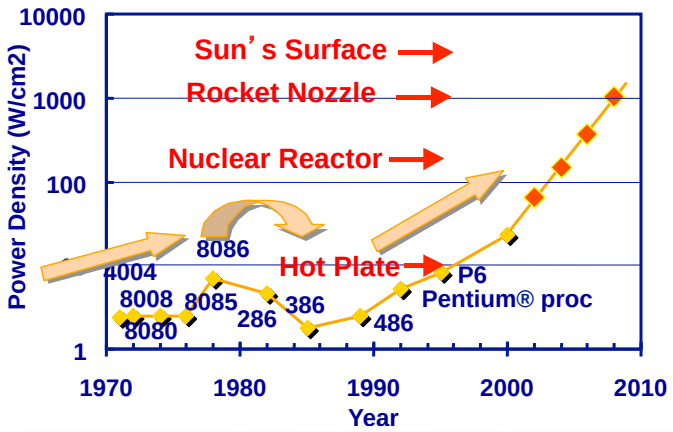
- Did this really happen?

Courtesy, Intel

Power Dissipation Data



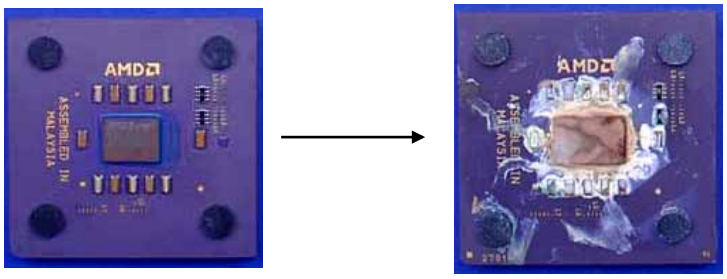
Cause: Power Density



S. Borkar

Power density too high for cost-effective cooling

Not enough cooling...



*Pictures from http://www.tomshardware.com/2001/09/17/hot_spot/

Moving Forward

Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Not Only Microprocessors

Cell Phone

Digital Cellular Market (Phones Shipped)

	1996	1997	1998	1999	2000
Units	48M	86M	162M	260M	435M

(data from Texas Instruments)

Challenges in Digital Design

∝ DSM

"Microscopic Problems"
- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

∝ 1/DSM

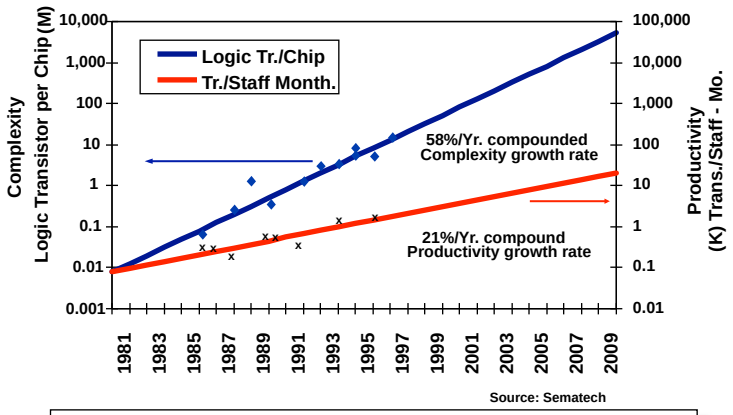
"Macroscopic Issues"
- Complexity
- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

Everything Looks a Little Different

?

…and There's a Lot of Them!

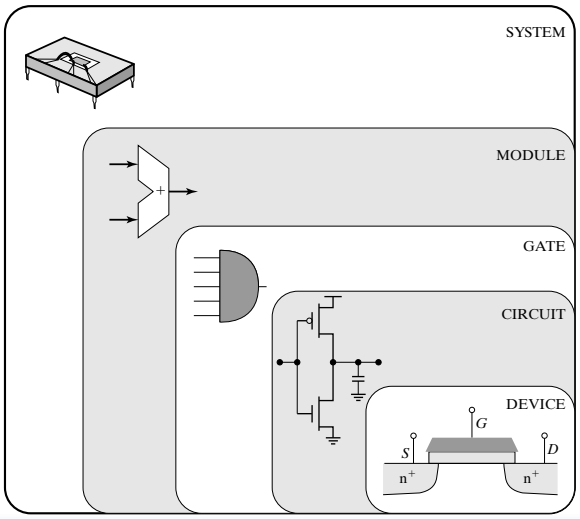
Productivity Trends



Complexity outpaces design productivity

Courtesy, ITRS Roadmap

Design Abstraction Levels



Next Lecture

- Introduce basic metrics for design of integrated circuits – how to measure cost, delay, power, etc.