EE141-Spring 2012 Digital Integrated Circuits

Lecture 14
Memory

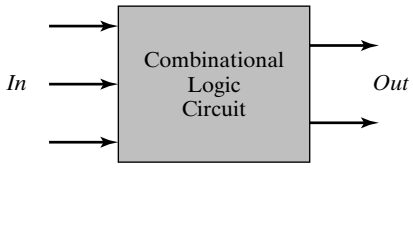
Administrativia

logic depth

- Homework 6 due March 16.
- Project Phase 1 due on March 21. global critical path
- Midterm 2 on March 23!
- Prepare to get buzzed.

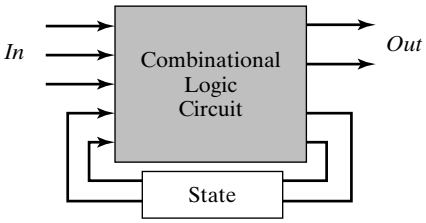
Registers and Memory

Combinational vs. Sequential Logic



(a) Combinational

Output = *f*(*In*)



(b) Sequential

Output = *f*(*In, Previous In*)

Registers versus Memory

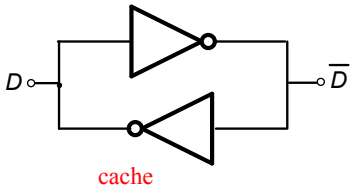
不同的内存单元核心都是一样的，对于总体的操作，布尔方程应该一样。

面积变得重要
外围硬件共享
记忆单元可以
save area

Memory - Introduction

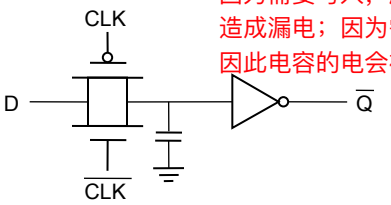
Storage Mechanisms

Static



cache

Dynamic



RAM

会漏电：
因为需要写入，所以需要接一个晶体管控制，这个会造成漏电；因为需要读取，即接入一个输出晶体管，因此电容的电会被消耗。

Semiconductor Memory Classification

Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory ROM
Random Access	Non-Random Access	Erasable Programmable ROM	
static SRAM	FIFO	EPROM	Mask-Programmed
DRAM dynamic	LIFO	E^2PROM	Programmable (PROM)
	Shift Register	Electrically Erasable Programmable ROM	
	CAM contents addressable memory	FLASH	

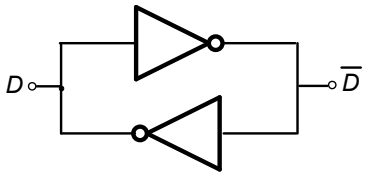
FLASH写入速度慢（这就是为什么不是主要memory的原因）但是读取速度快。所以也可以叫 Fast Read Slow Write memory。

Random Access Memories (RAM)

- STATIC (SRAM)
  - Data stored as long as supply is applied
  - Larger (6 transistors/cell)
  - Fast
  - Differential (usually)
- DYNAMIC (DRAM)
  - Periodic refresh required
  - Smaller (1-3 transistors/cell)
  - Slower
  - Single Ended

Memory - SRAM

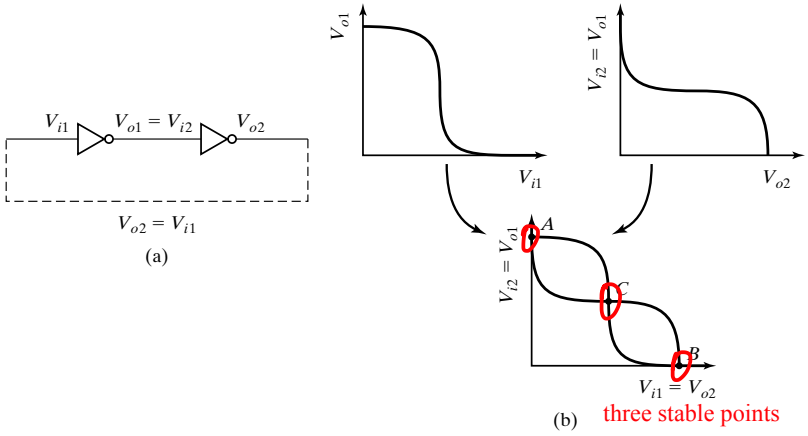
Basic Static Memory Element



- If D is high, D_b will be driven low
  - Which makes D stay high
- Positive feedback

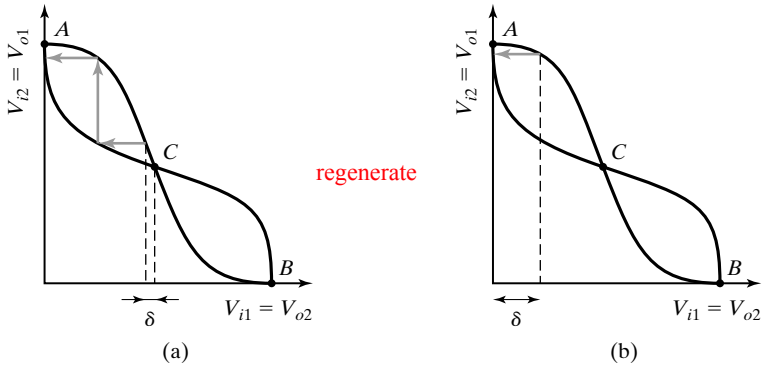
不会处于稳定态，会在0和1之间快速变换

Positive Feedback: Bi-Stability



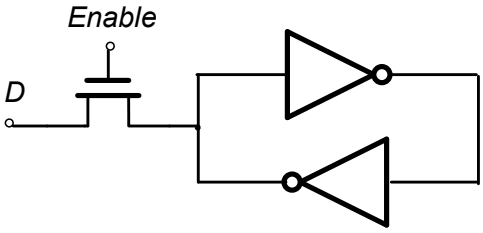
three stable points

Meta-Stability



Gain should be larger than 1 in the transition region

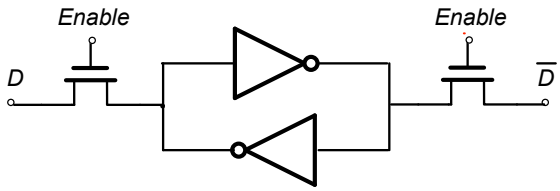
Writing into a Cross-Coupled Pair



Access transistor must be able to overpower the feedback

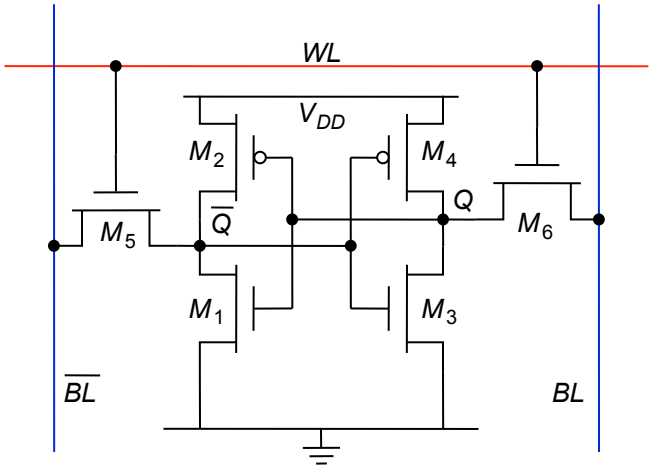
Writing a "1"

Memory Cell



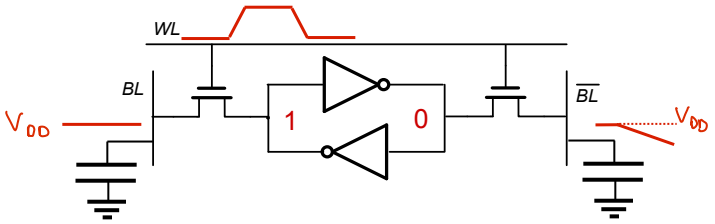
Complementary data values are written (read) from two sides

6-Transistor CMOS SRAM Cell



SRAM Operation - Read

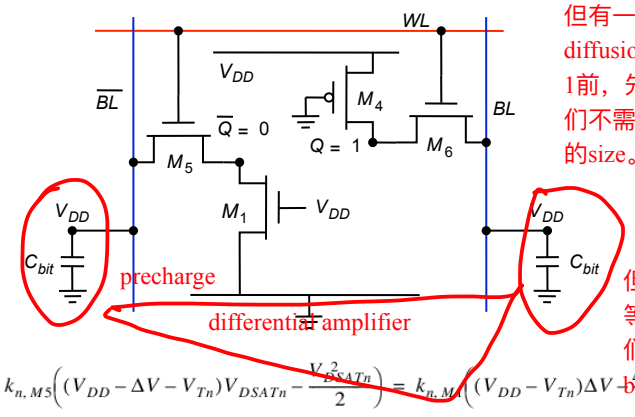
Read



- Q_b will get pulled up when WL first goes high
  - Reading the cell should not destroy the stored value

在对SRAM进行写操作时，其中一条bitline置为0，另一条置为1，或者相反。
在对SRAM进行读操作时，两条bitline都要对电容进行预充电。

CMOS SRAM Analysis (Read)



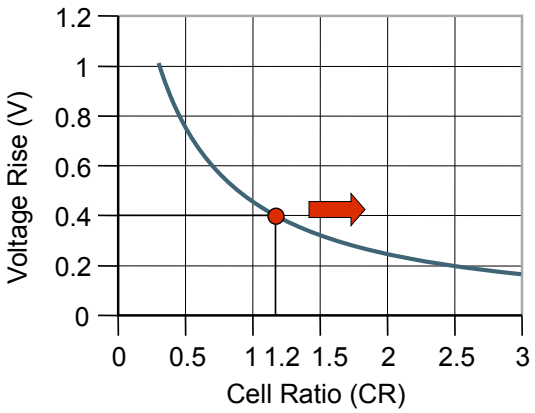
但有一个问题，当一条bitline连接的cell比较多时diffusion capcitror的值会比较大。所以在WL变为1前，先对bitline那些电容进行预充电。这时候我们不需要再担心PMOS的size，只需要关心NMOS的size。

precharge
但是，其中一条bitline需要漫长的放电，如果我们等待它完全放完电，这将会使delay很高，因此我们可以添加一个differential amplifier去比较两条bitline的电压值，然后输出VDD或者VSS！

$$k_{n,M5}\left((V_{DD}-\Delta V-V_{Tn})V_{DSATn}-\frac{V_{DSATn}^2}{2}\right)=k_{n,M1}\left((V_{DD}-V_{Tn})\Delta V-\frac{\Delta V^2}{2}\right)$$

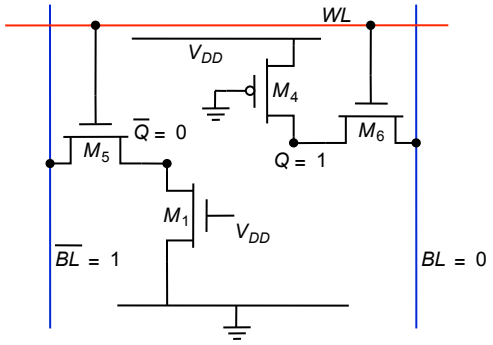
$$\Delta V=\frac{V_{DSATn}+CR(V_{DD}-V_{Tn})-\sqrt{V_{DSATn}^2(1+CR)+CR^2(V_{DD}-V_{Tn})^2}}{CR}$$

CMOS SRAM Analysis (Read)



$$CR=\frac{W_1/L_1}{W_5/L_5}$$

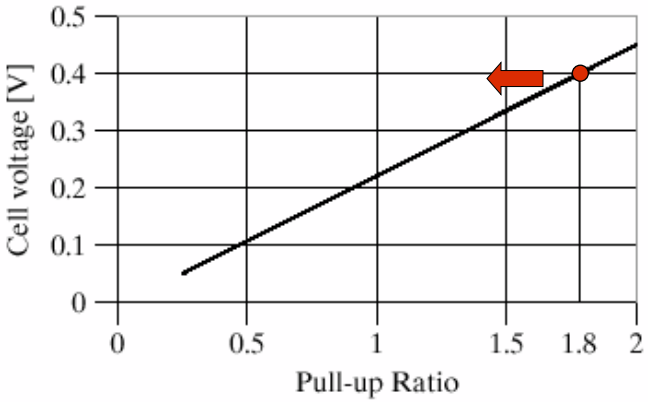
CMOS SRAM Analysis (Write)



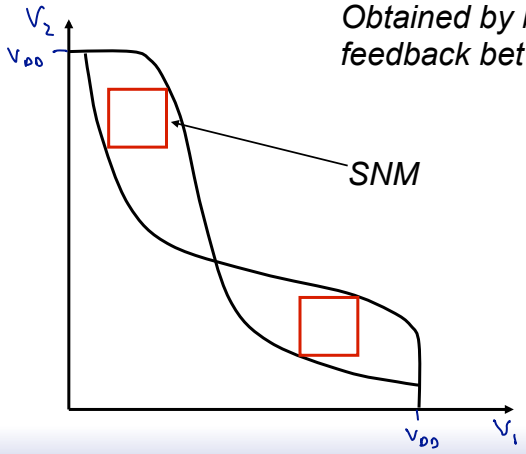
$$k_{n,M6}\left((V_{DD}-V_{Tn})V_Q-\frac{V_Q^2}{2}\right)=k_{p,M4}\left((V_{DD}-|V_{Tp}|)V_{DSATp}-\frac{V_{DSATp}^2}{2}\right)$$

$$V_Q = V_{DD}-V_{Tn}-\sqrt{(V_{DD}-V_{Tn})^2-2\frac{\mu_p}{\mu_n}PR\left((V_{DD}-|V_{Tp}|)V_{DSATp}-\frac{V_{DSATp}^2}{2}\right)},$$

CMOS SRAM Analysis (Write)

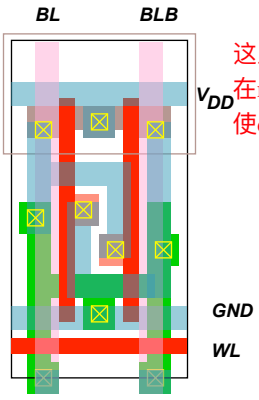


Read Static Noise Margin



Obtained by breaking the feedback between the inverters

6T-SRAM — Layout

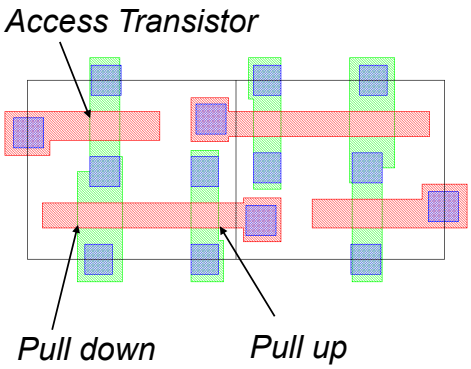


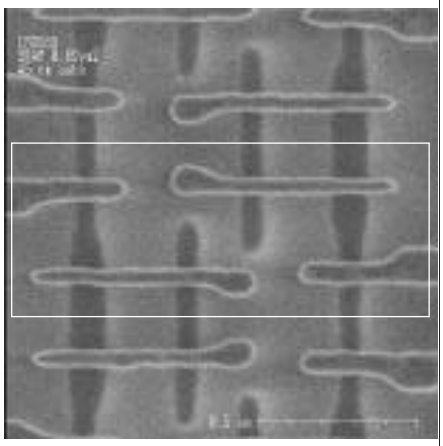
这里的PMOS不一定是NMOS的两倍大，在memory cell的设计中，我们要尽可能使device小

Compact cell
- Bitlines: M2
- Wordline: bootstrapped in M3

65nm SRAM

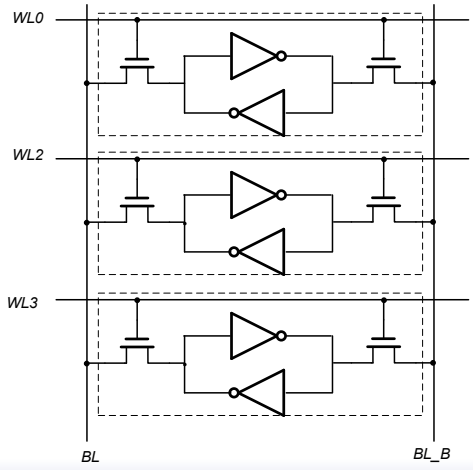
- ST/Philips/Motorola





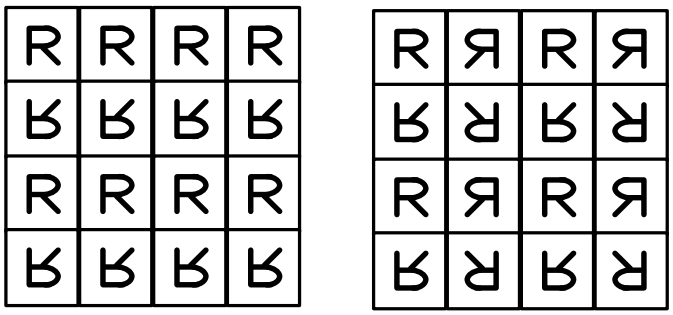
SRAM Column

存在外围电路帮助这个电路进行读取或者写入操作。

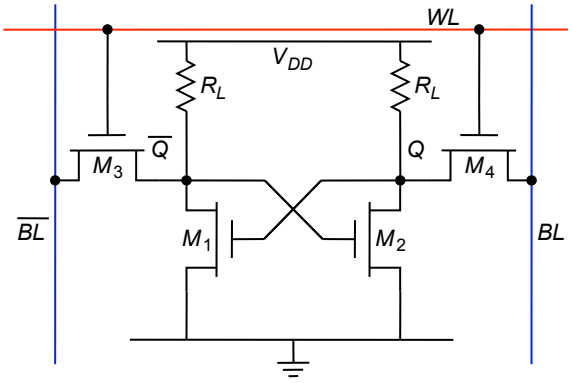


SRAM Array Layout

这种矩阵设计有助于通过共享内存单元的某些元素从而减少节省面积。



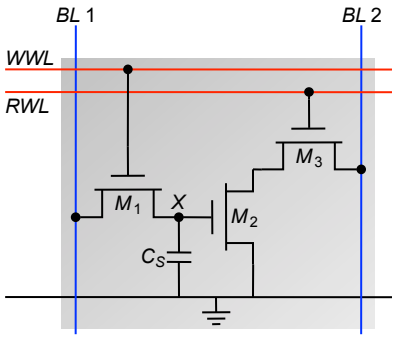
Resistive Pull-Ups

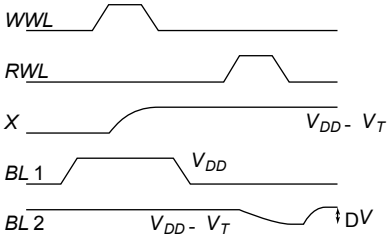


Static power dissipation -- Want R_L large
Bit lines precharged to V_{DD} to address t_p problem

Memory - DRAM

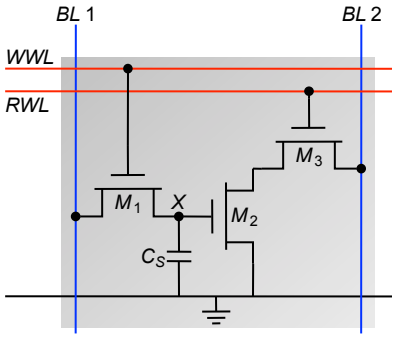
3-Transistor DRAM Cell

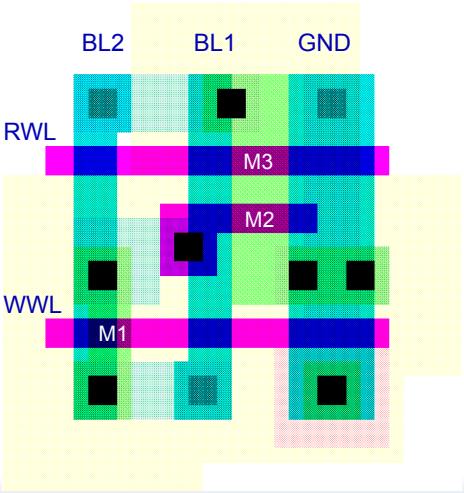




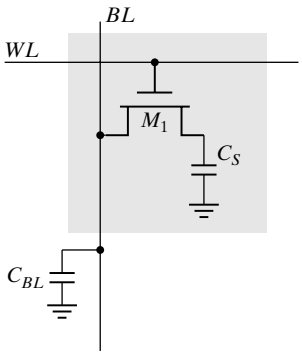
No constraints on device ratios
Reads are non-destructive
Value stored at node X when writing a "1" = V_{WWL}-V_{Tn}

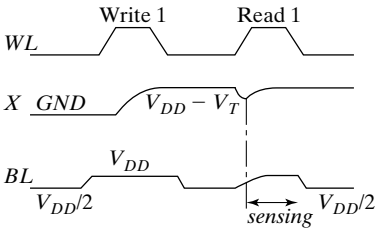
3T DRAM Layout





1-Transistor DRAM Cell



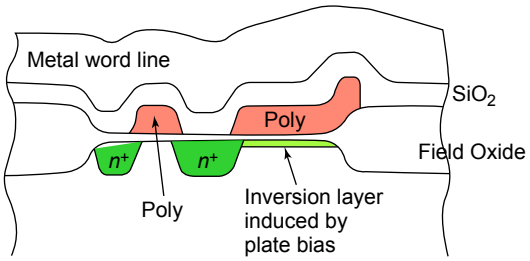


Write: C S is charged or discharged by asserting WL and BL.
Read: Charge redistribution takes places between bit line and storage capacitance

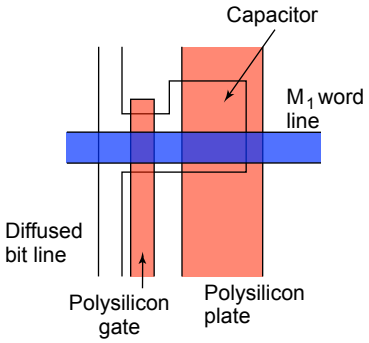
$$\Delta V = V_{BL} - V_{PRE} = V_{BIT} - V_{PRE} \frac{C_S}{C_S + C_{BL}}$$

Voltage swing is small; typically around 250 mV.

1T DRAM Cell



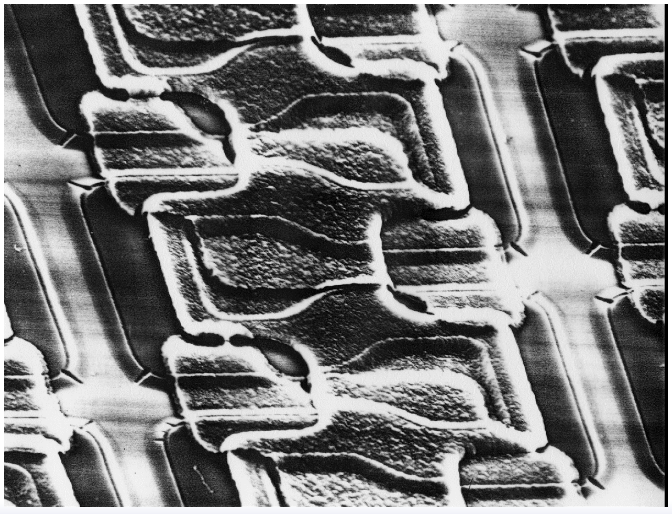
Cross-section



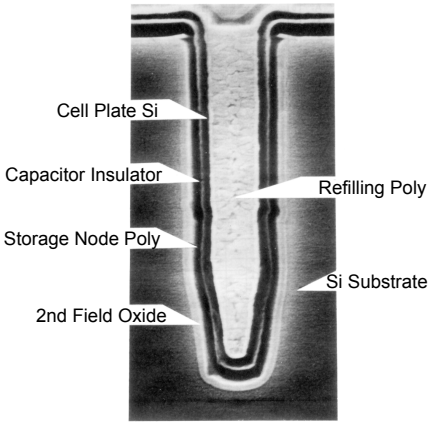
Layout

Uses Polysilicon-Diffusion Capacitance
Expensive in Area

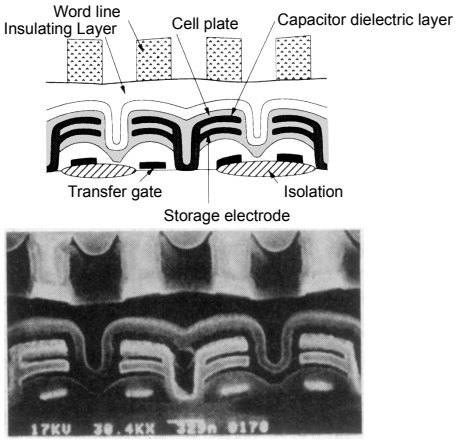
Micrograph of 1T DRAM



Advanced 1T DRAM Cells



Trench Cell



Stacked-capacitor Cell