EE141-Spring 2012 Digital Integrated Circuits

Lecture 3
Metrics (Cntd)
IC Manufacturing

Administrativia

- Labs start next week – be prepared
- Homework #1 is due next Wednesday

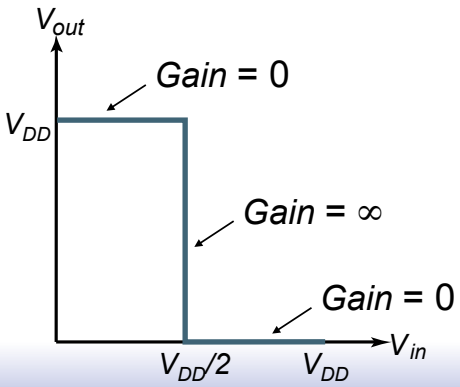
Design Metrics: Reliability

Noise and Digital Systems

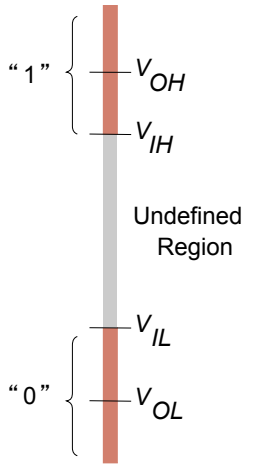
- Circuit needs to works despite "analog" noise
  - Digital gates can reject noise
  - This is actually how digital systems are defined
- Digital system is one where:
  - Discrete values mapped to analog levels and back
  - All the elements (gates) can reject noise
    - For "small" amounts of noise, output noise is less than input noise
  - Thus, for sufficiently "small" noise, the system acts as if it was noiseless

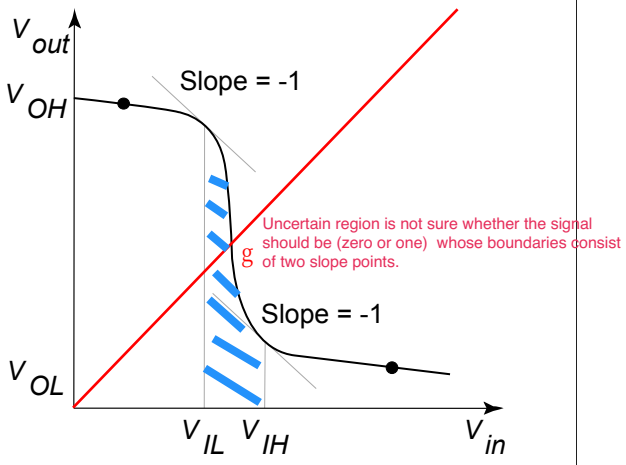
Noise Rejection

- To see if a gate rejects noise
  - Look at its DC voltage transfer characteristic (VTC)
  - See what happens when input is not exactly 1 or 0
- Ideal digital gate:
  - Noise needs to be larger than $V_{DD}/2$ to have any effect on gate output

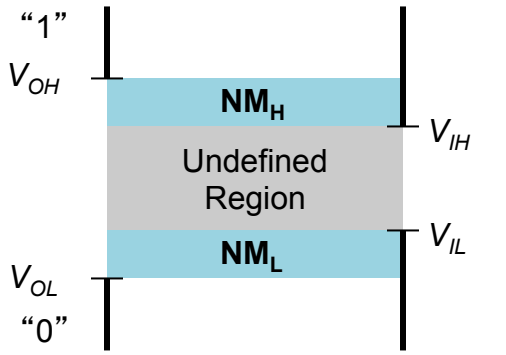


Voltage Mapping





Definition of Noise Margins

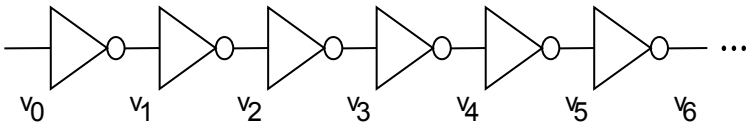


Noise margin high:
$NM_H = V_{OH} - V_{IH}$

Noise margin low:
$NM_L = V_{IL} - V_{OL}$

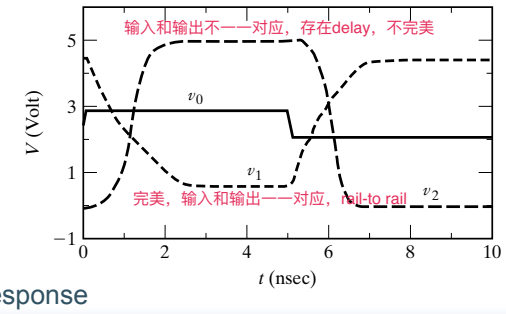
nature noise suppression or regeneration：噪声对输入的干扰使得反相器的输出和没有噪声干扰时相比，变得更好了。如果是理想的反相器（指gain=0），噪声的加入甚至对输出没影响，或者讲输出时会被消除。然而模拟电路的放大器会使输入的噪声越来越大。这也是数字电路为什么如此强大的原因。

Digital Gate Noise Reduction: Regenerative Property



A chain of inverters

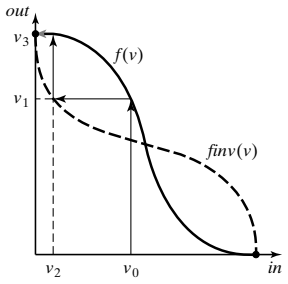
上一个门的输出是下一个门的输入。



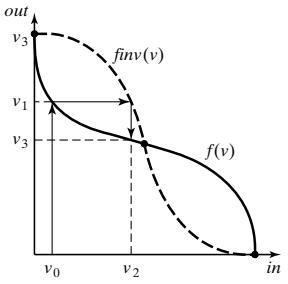
Simulated response

Regenerative Property (Another View)

实线的x,y坐标的意义和虚线的x,y坐标的意义相反，实线的输出是虚线的输入。
好的反相器具有两个特性：中间区域的高gain，高低区域具有低gain.

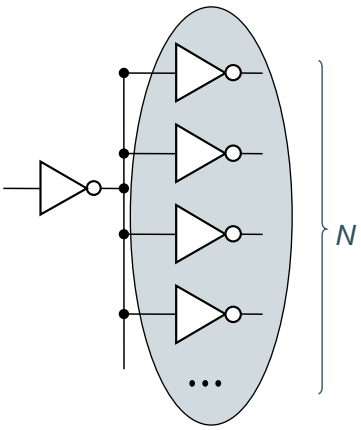


Regenerative

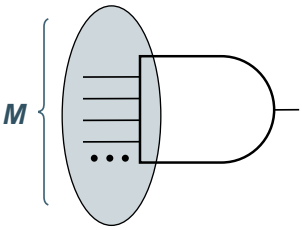


Non-Regenerative

Fan-in and Fan-out



Fan-out *N*



Fan-in *M*

There is a modified definition of fan-out for CMOS logic

Some of the reliability and performance functions of our gate are really going to be depending upon fanin.
Fanout will affect our performance because of load capacitances.

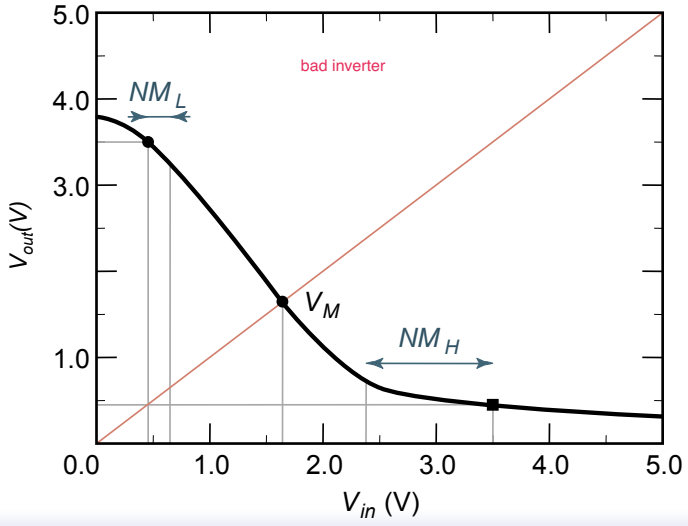
Key Reliability Properties

- Absolute noise margin values are not the only things that matter
  - e.g., floating (high impedance) nodes are more easily disturbed than low impedance nodes (in terms of voltage)
- Noise immunity (i.e., how well the gate suppresses noise sources) needs to be considered too

免疫力

- Summary of some key reliability metrics:
  - Noise transfer functions & margin (ideal: gain = ∞, margin = $V_{dd}/2$)
  - Output impedance (ideal: $R_o = 0$)
  - Input impedance (ideal: $R_i = \infty$)

Example: An Old-time Inverter



Example: An Old-time Inverter

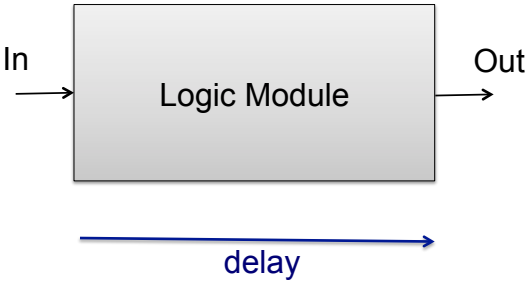
- V_{OH} = 3.6V
- V_{OL} = 0.4V
- V_{IL} = 0.6V
- V_{IH} = 2.3V
- $NM_H = V_{OH} - V_{IH}$ = 1.3V
- $NM_L = V_{IL} - V_{OL}$ = 0.2V

Summary

- Understanding the design metrics that govern digital design is crucial
  - We discussed cost and reliability so far
- Key design messages so far:
  - Keep chip area as small as possible
  - Pick design styles and parameters so that noise margins are reasonable

Design Metrics: Performance

Primary Performance Metric: Delay

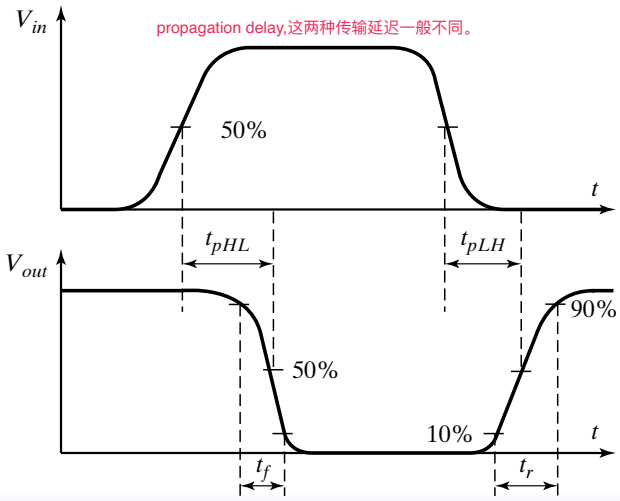


How to define delay in a universal way?

$t_p = \frac{t_{pHL} + t_{pLH}}{2}$ 为什么要除以2，参考传输特性曲线的VM

关键特性：可加性

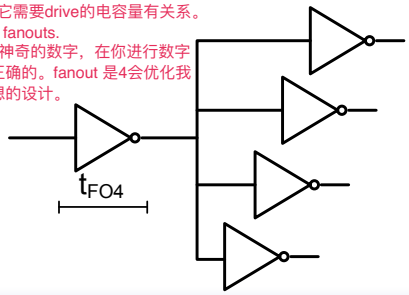
Delay Definitions



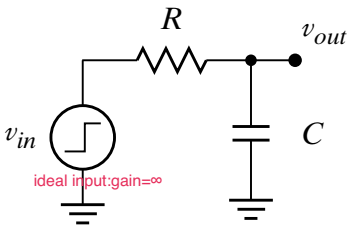
Fanout of Four (FO4) Delay

- Want a way to characterize the delay of a circuit (roughly) independent of environment
- Most common metric:
  - Delay of an inverter driving four copies of itself (t_{FO4})

一个门的传输延迟与它需要drive的电容量有关系。
delay is a function of fanouts.
为什么是4，4是一个神奇的数字，在你进行数字化设计时，4往往是正确的。fanout 是4会优化我们的设计，4也是理想的设计。



A First-Order RC Network



$$v_{out}(t) = (1 - e^{-t/\tau})\, V$$

=V/2计算传输延迟

V=VDD

解得

$$t_p = \ln(2)\,\tau = 0.69\,RC$$

τ=RC

Important model – matches delay of an inverter

Design Metrics: Energy & Power

Power Dissipation

Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply}i(t)$$

Peak power: 从电池/源可提供的最大功率考虑，我们必须保证电源可提供的最大功率大于等于芯片的峰值功率。其实是保证电池的电压不变，最大电流大于等于芯片的峰值电流。同时电线的电流承载能力也是有限的。

$$P_{peak} = V_{supply}i_{peak}$$

Average power: 从电池续航角度考虑，我们更关心平均功率。平均功率还决定了热耗散。

$$P_{ave} = \frac{1}{T}\int_t^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_t^{t+T} i_{supply}(t)dt$$

"Power-Delay" and Energy-Delay

- Want low power and low delay, so how about optimizing the product of the two?
  - So-called "Power-Delay Product"

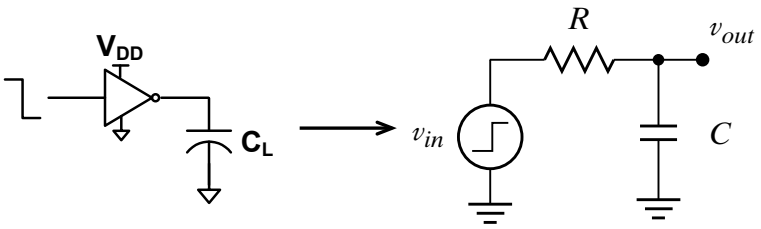
Energy per Operation
PDP= $P_{av}t_p$

It stands for the average energy consumed per switching event.

- Power·Delay is by definition Energy
  - Optimizing this pushes you to go as slow as possible
- Alternative gate metric: Energy-Delay Product
  - EDP = $(P_{av}\cdot t_p)\cdot t_p = E\cdot t_p$

It measures the energy needed to switch the the gate,which is an important property for sure.

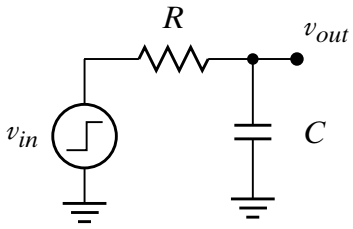
Energy in CMOS



- The voltage on C_L eventually settles to V_{DD}
- Thus, charge stored on the capacitor is $C_L V_{DD}$
  - This charge has to flow out of the power supply
    电荷，充电量
- So, energy is just $Q \cdot V_{DD} = (C_L V_{DD}) \cdot V_{DD}$

降低电压减少芯片能耗，因为电压在芯片能耗公式中存在平方。

Energy (the harder way)



$$E_{0\to 1} = \int_0^T P_{DD}(t)dt = V_{DD}\int_0^T i_{DD}(t)dt = V_{DD}\int_0^{V_{DD}} C_L dv_{out} = C_L V_{DD}^2$$

$$E_C = \int_0^T P_C(t)dt = \int_0^T v_{out} i_L(t)dt = \int_0^{V_{DD}} C_L v_{out} dv_{out} = \frac{1}{2} C_L V_{DD}^2$$

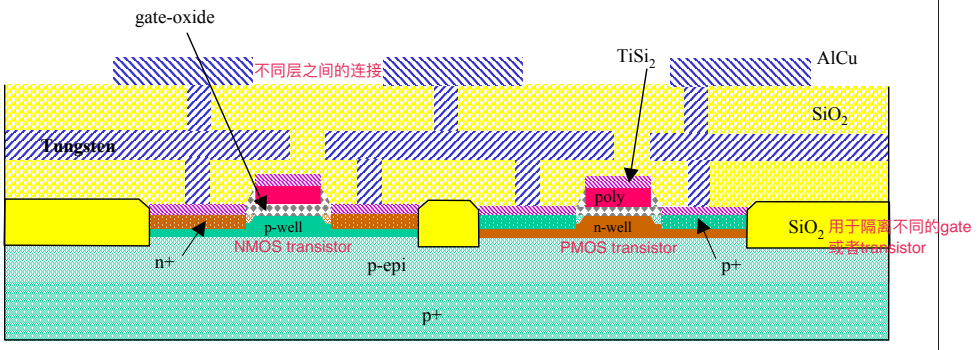
一半能量被消耗在热耗散中。如果放电的话，剩余那一半能量（电容器上所存储的能量）也会被消耗在热耗散中。

Summary

- Understanding the design metrics that govern digital design is crucial
  - Cost
  - Robustness
  - Performance/speed
  - Power and energy dissipation

Intermezzo: Design Rules

A Modern CMOS Process

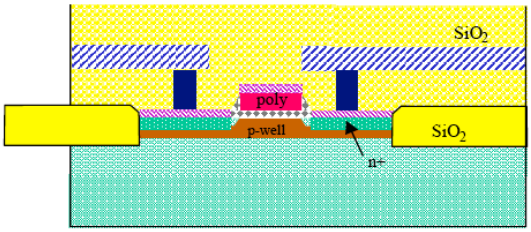


Dual-Well Shallow-Trench-Isolated CMOS Process

Transistor Layout

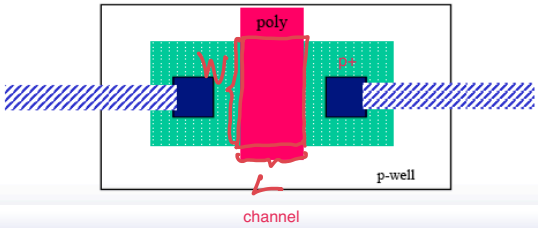
Cross-Sectional View

这个是晶圆厂所看到和所用到的东西。
需要关心器件厚度，三维空间



Layout View

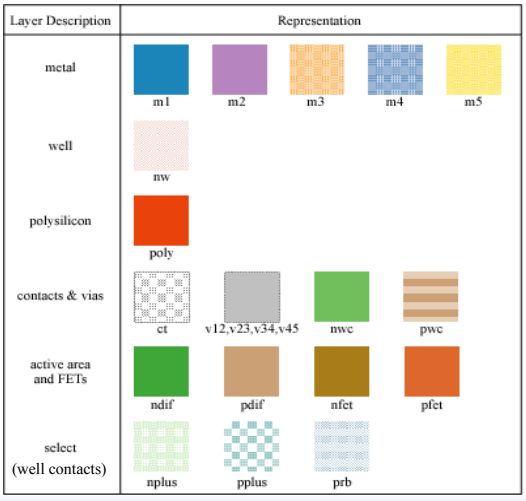
硬件设计师看到的和所用到的东西。
不需要关心器件厚度，二维平面



CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Well contact (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Layers in 0.25 μm CMOS process



Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter $\lambda = \frac{CD}{2}$
  - absolute dimensions (micron rules)

也称作lambda rules

a unit

为什么选择lambda做unit，因为更容易表达，不会出现分数，例如3lambda，lambda

CD=minimum feature size=critical dimension

Design Rules

three rules

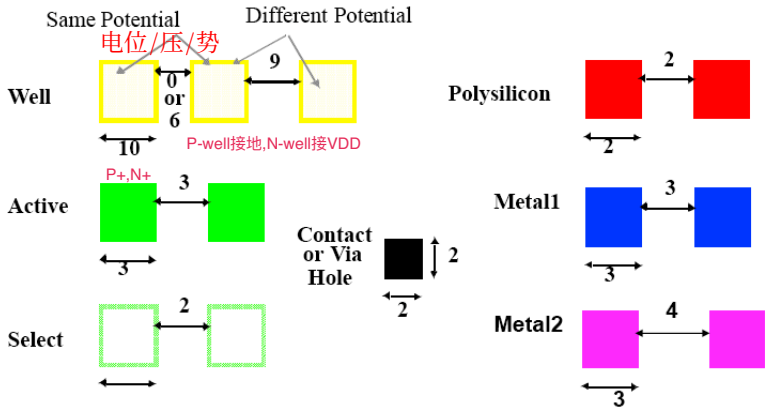
- Intra-layer rule
  - Widths, spacing, area (minimum, minimum, minimum) between objects on the same layer
- Inter-layer rule
  - Enclosures, distances, extensions, overlaps

how much overlaps can I have between two layers

- Special rules (sub-0.25μm)
  - Antenna rules, density rules, (area)

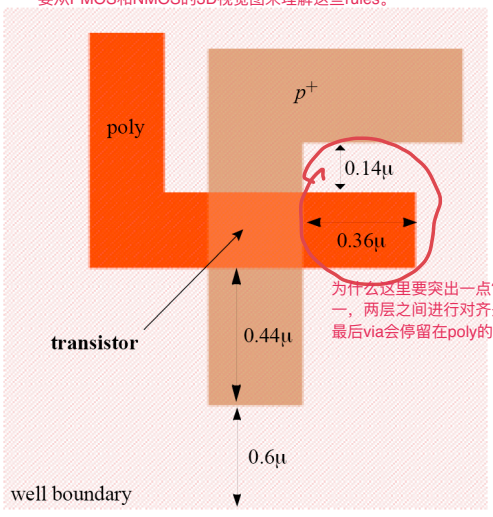
We have to use a minimum amount of coverage in every layer.

Intra-Layer Design Rules



Inter-Layer: Transistor Layout

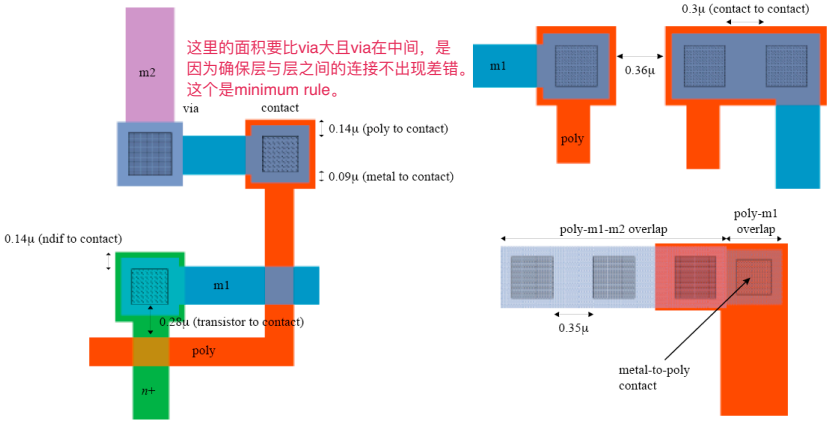
要从PMOS和NMOS的3D视觉图来理解这些rules。



为什么这里要突出一点?
一，两层之间进行对齐是很困难的，很难知道最后via会停留在poly的那个地方。

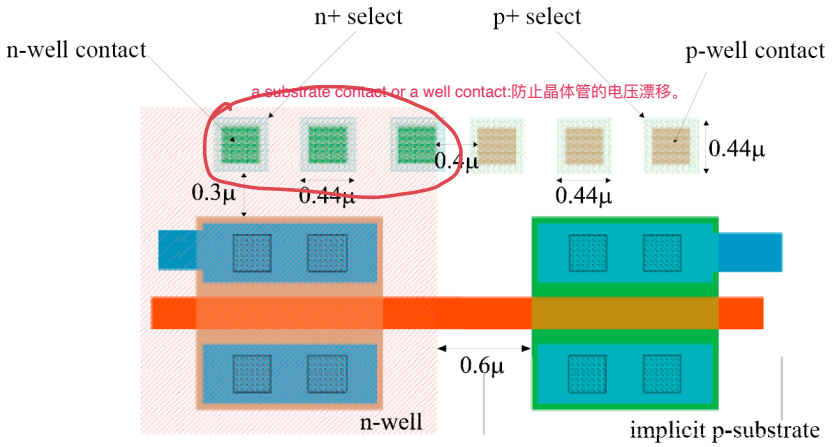
注意这些双向箭头标出的距离，就是Inter-Layer rules的一部分。

Inter-Layer: Vias and Contacts

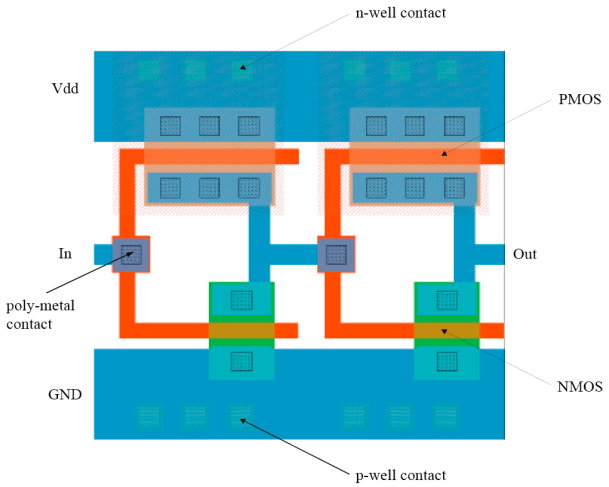


如果使用一个高电阻的via连接两条不同层的低电阻的电线，会导致电路出问题。maximum rules

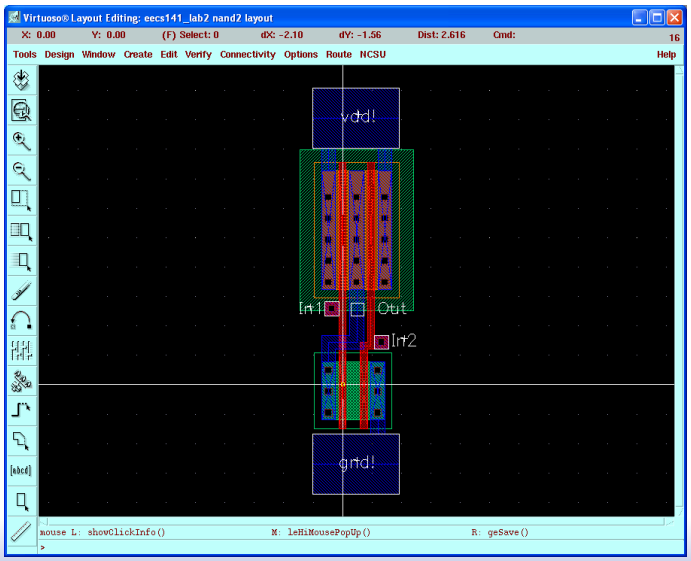
Inter-Layer: Well and Substrate



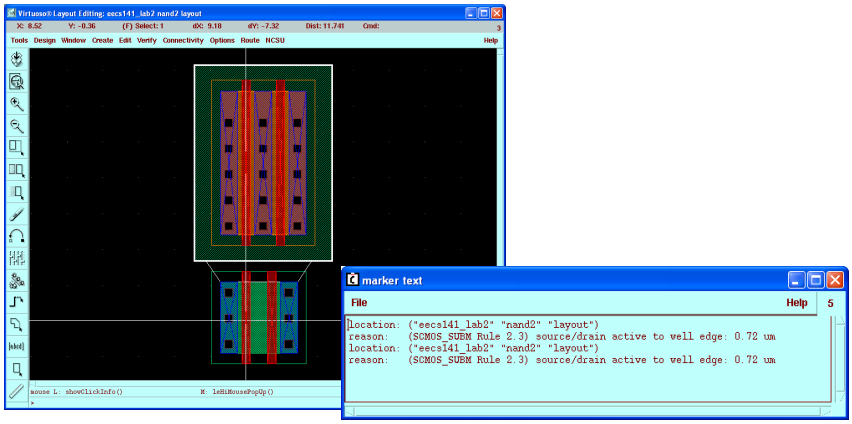
CMOS Inverter Layout



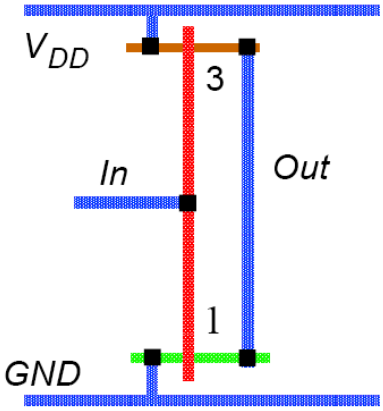
Layout Editor



Design Rule Checker



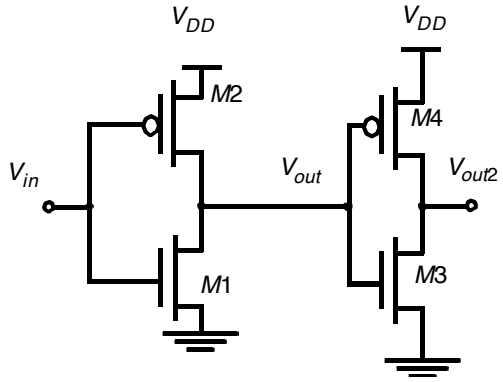
Sticks Diagram



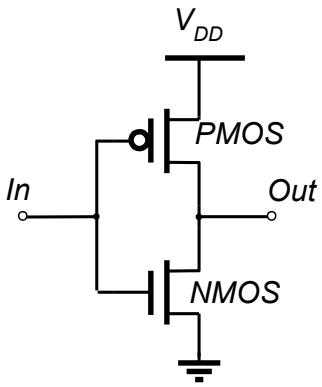
Stick diagram of inverter

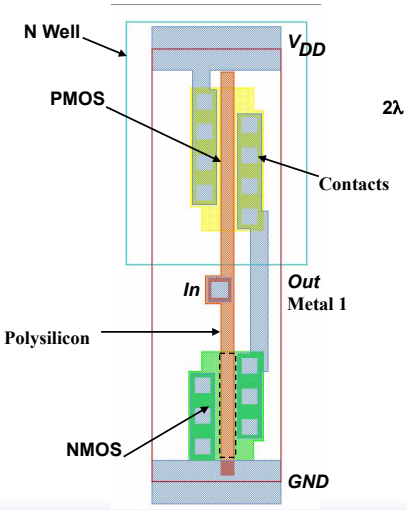
- Dimensionless layout entities
- Only topology is important

Circuit Under Design



CMOS Inverter

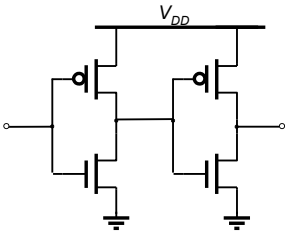


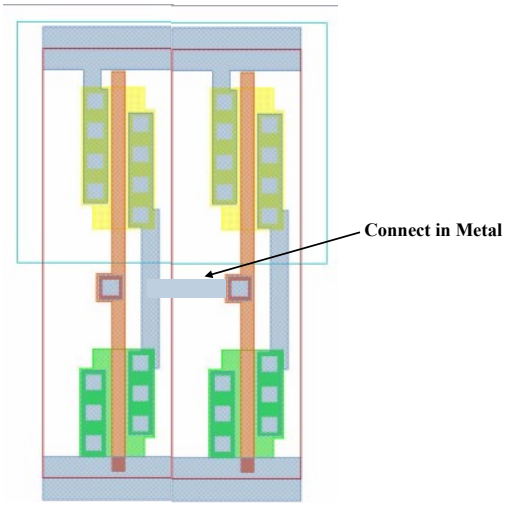


Two Inverters

Share power and ground

Abut cells





Next Lecture

- From simple to more complex gates …