EE141-Spring 2012 Digital Integrated Circuits

Lecture 21
Sequential + Timing

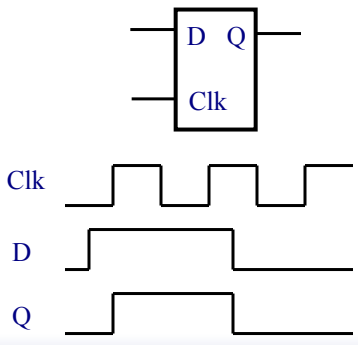
Administrativia

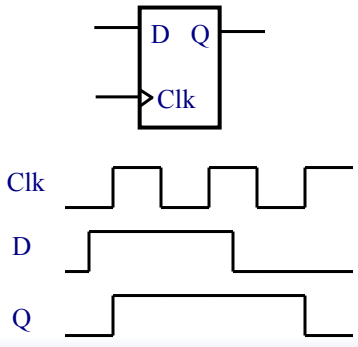
- Phase 2 due next We!

Sequential Circuits

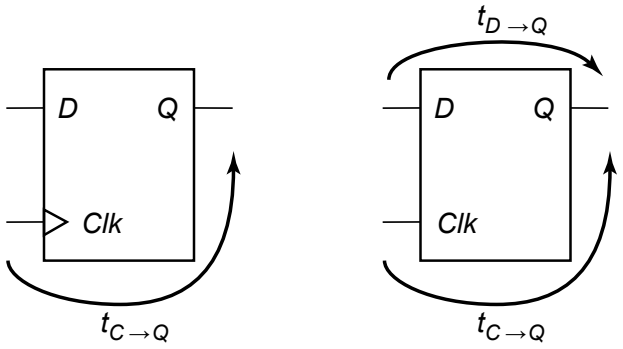
Latch versus Register (Flip-flop)

- Latch: level-sensitive
  clock is low - hold mode
  clock is high - transparent
- Register: edge-triggered
  stores data when
  clock rises



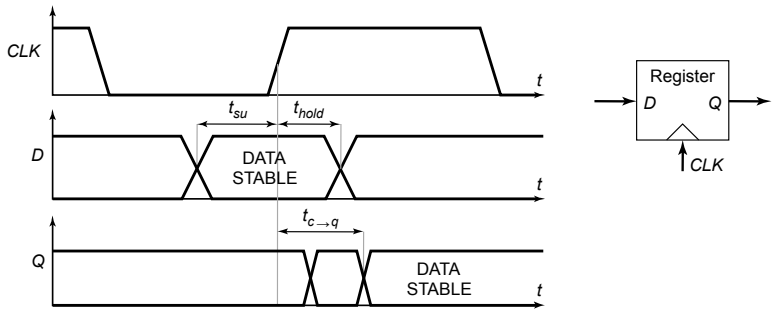


Characterizing Timing



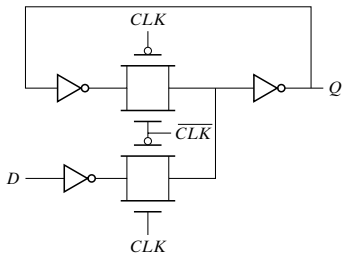
Register Latch

Timing Definitions – Set-up and Hold Times

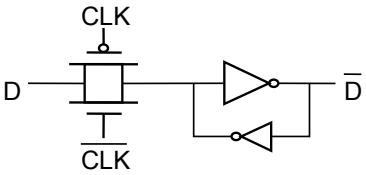


Writing into a Static Latch

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states

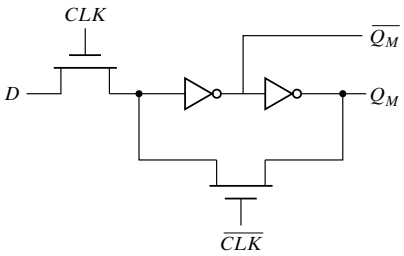


Converting into a MUX

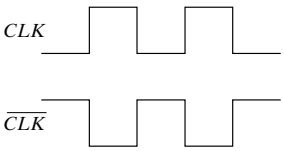


Forcing the state
(can implement as NMOS-only)

Mux-Based Latch



(a) Schematic diagram

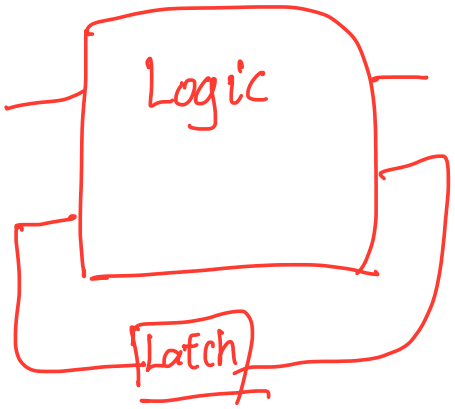


(b) Non overlapping clocks

NMOS only

Non-overlapping clocks

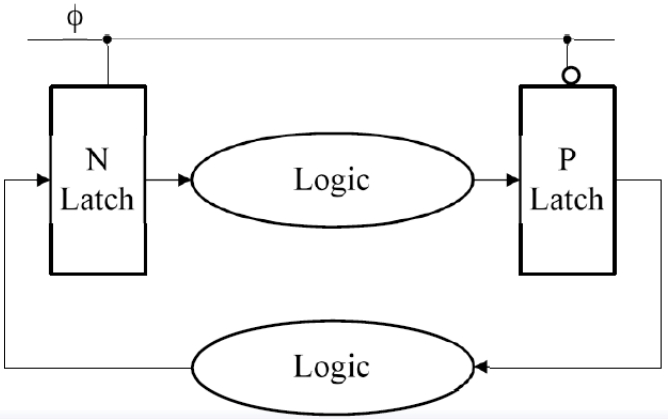
The race problem



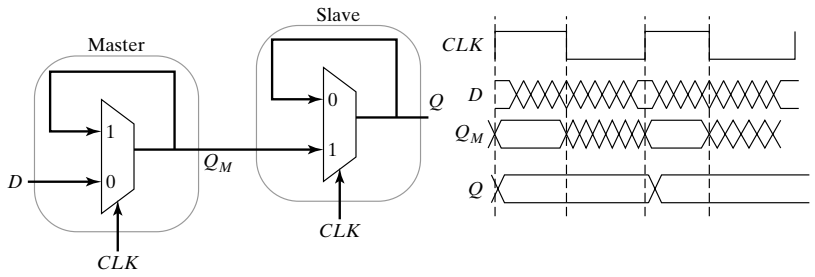
Two method to solve race problem:
(1)reduce the percentage of the high voltage of the clock so that it smaller than the propagation delay.(hard)
(2)use register to replace the latch
(3)latch-based design

Latch-Based Design

- N latch is transparent when $\Phi = 0$
- P latch is transparent when $\Phi = 1$



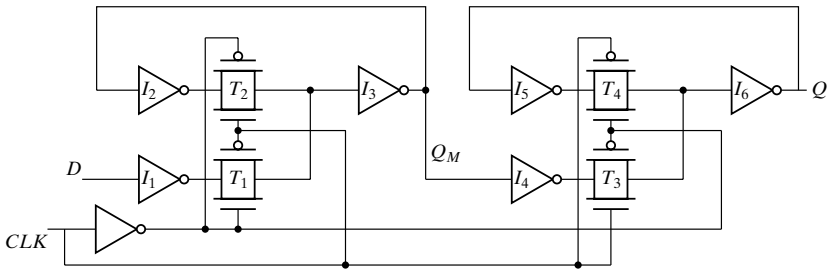
Master-Slave (Edge-Triggered) Register



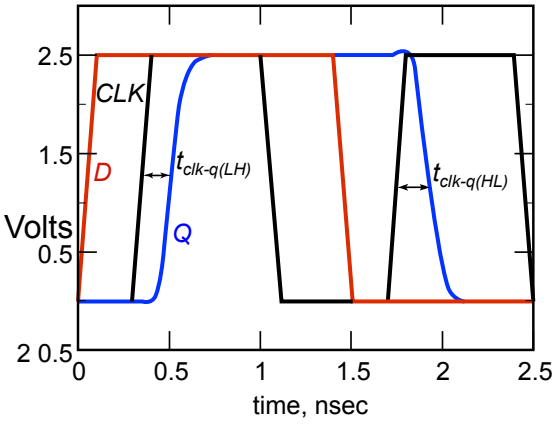
Two opposite latches trigger on edge
Also called master-slave latch pair

Master-Slave Register

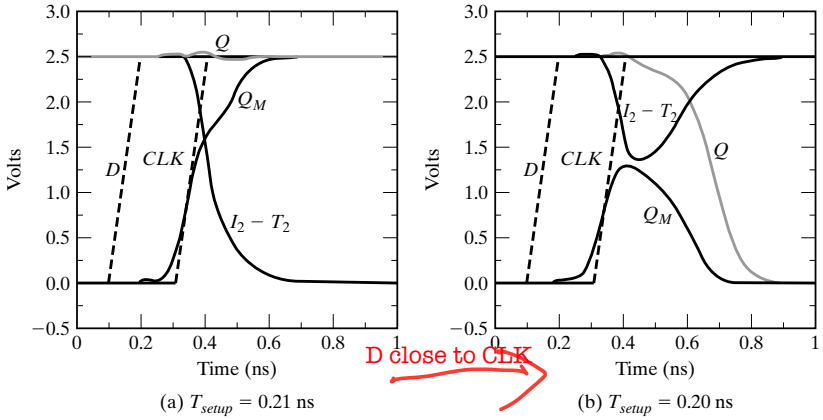
Multiplexer-based latch pair



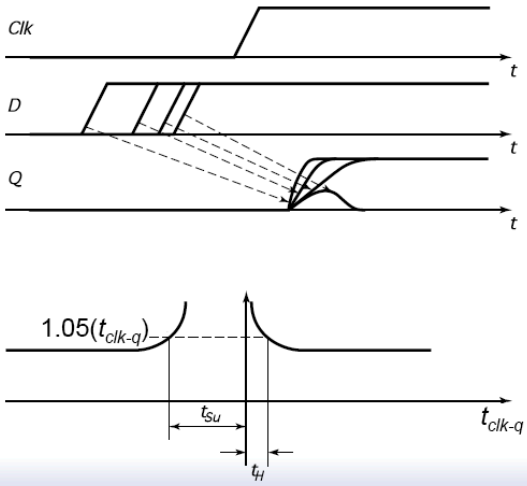
Clk-Q Delay



Setup Time



More Precise Setup Time

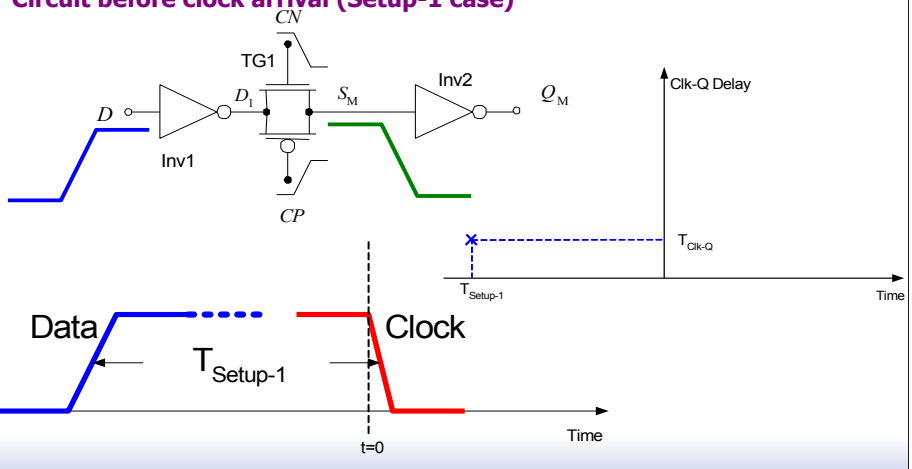


move D closer to Clk will get different Q

D closer to Clk => the set-up time smaller =>the time of clk to q bigger
so our set-up time is defined as the time of clk to q bigger 5 percentage.

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



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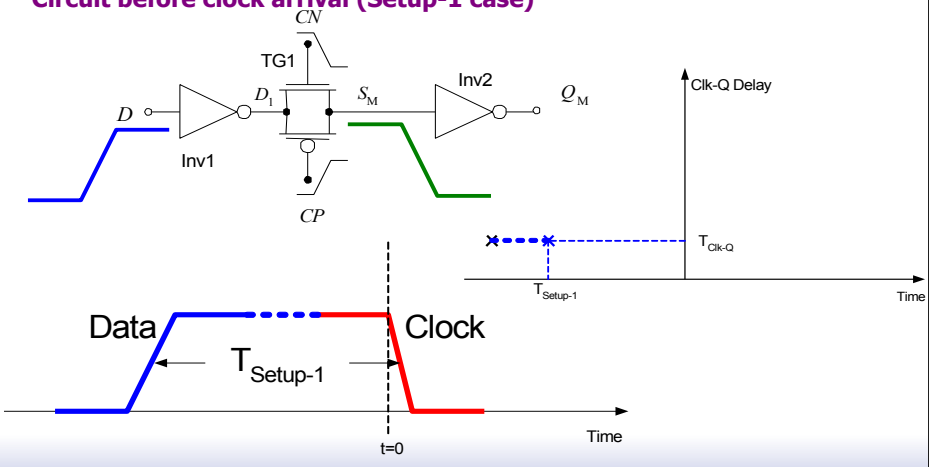

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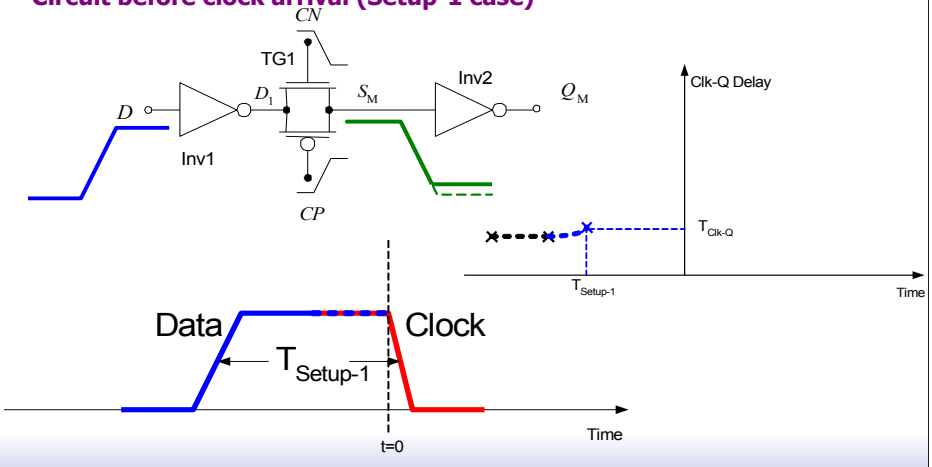

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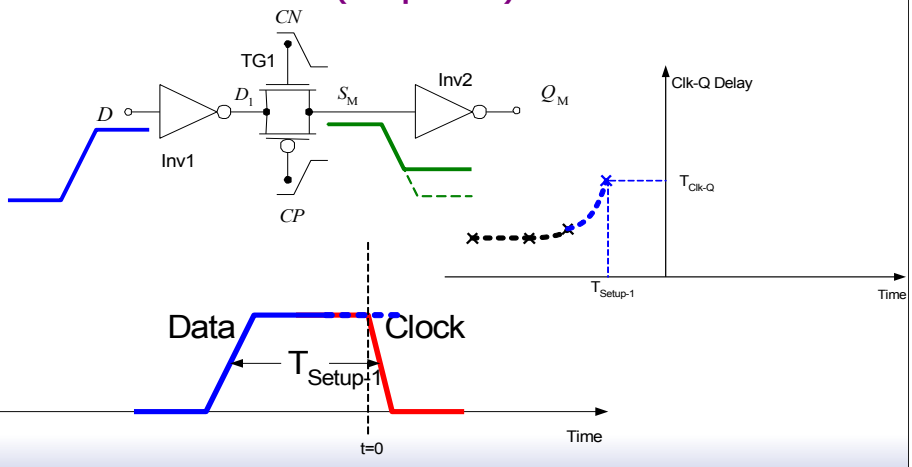

Setup-Hold Time Illustrations

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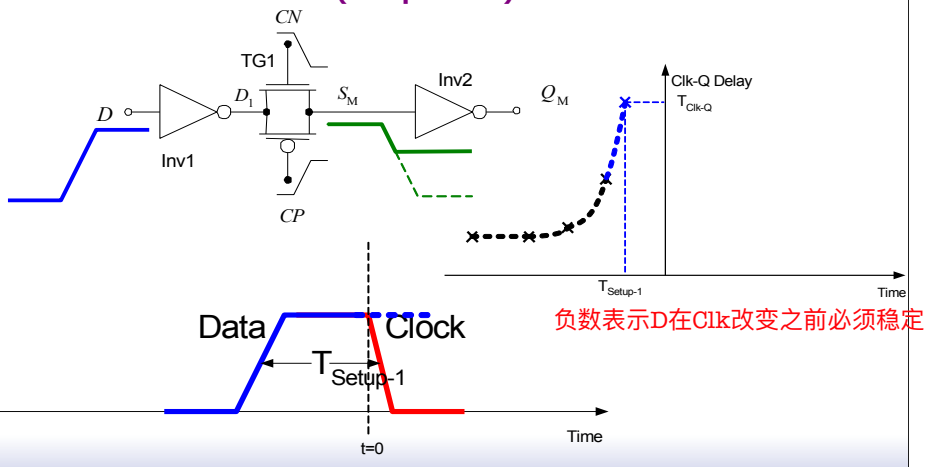
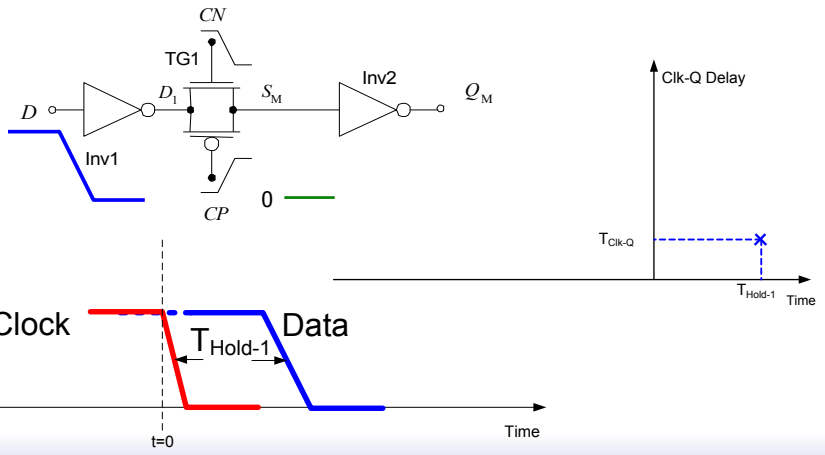


负数表示D在Clk改变之前必须稳定

Setup-Hold Time Illustrations

Hold-1 case



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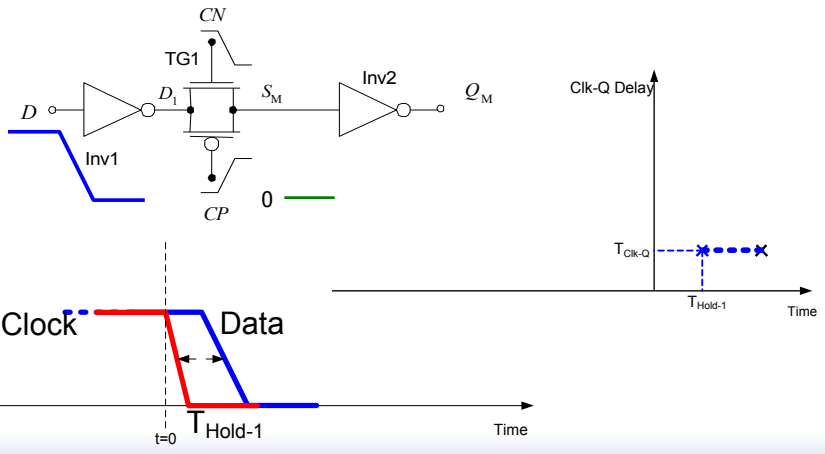
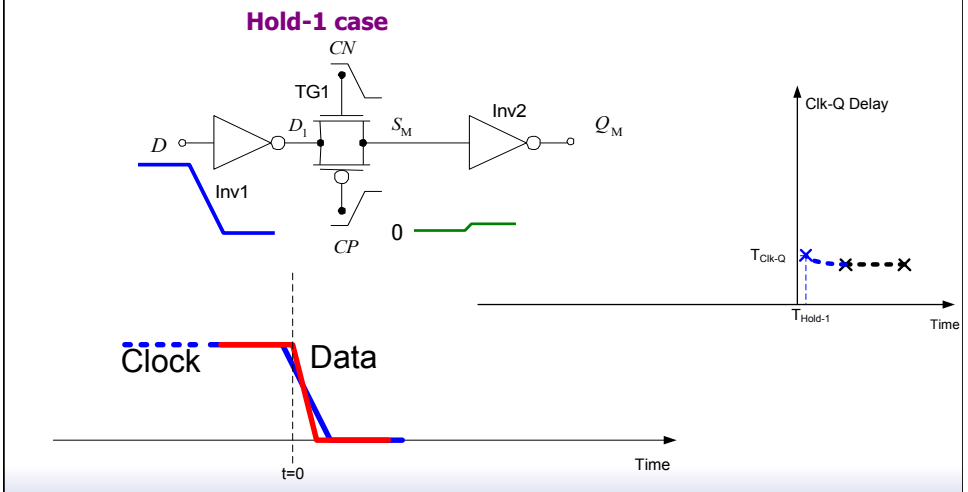
Setup-Hold Time Illustrations

Hold-1 case



Setup-Hold Time Illustrations



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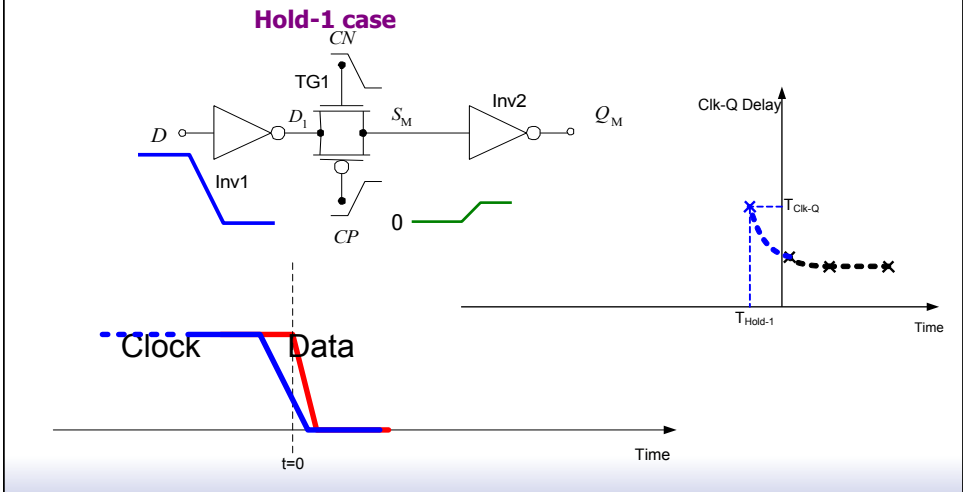

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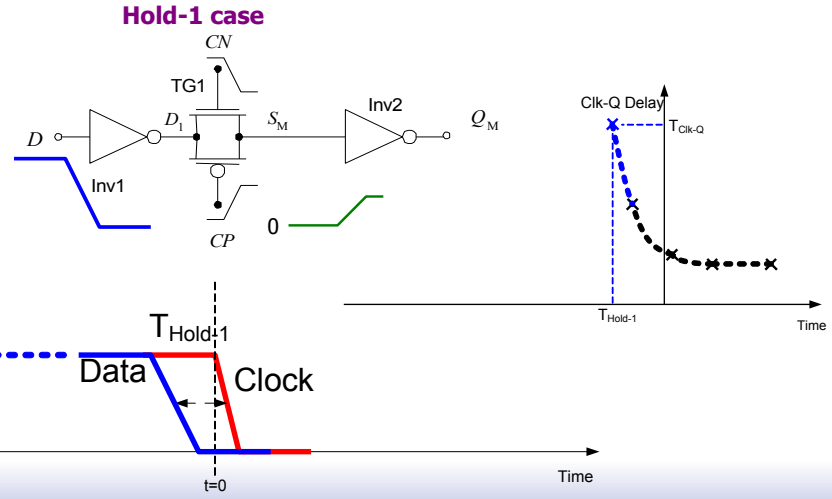
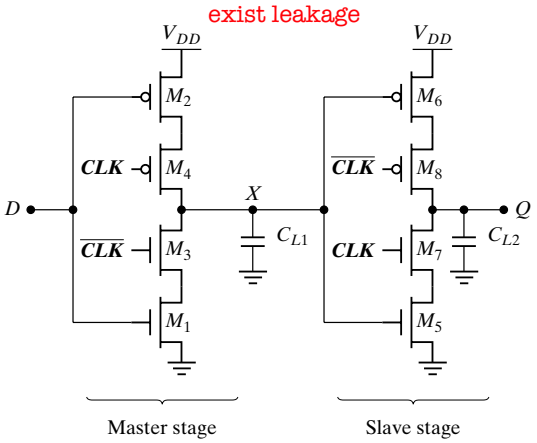


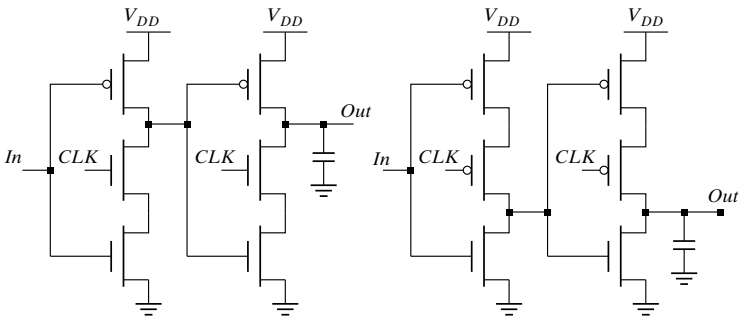
Other Latches/Registers: C²MOS



Keepers can be added to "staticize (?!)"

true single phase clock logic

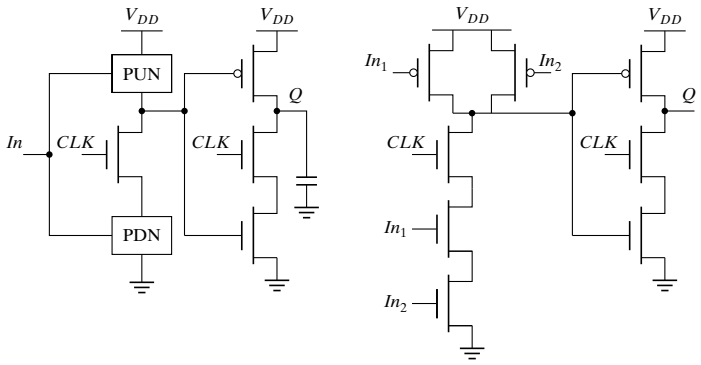
Other Latches/Registers: TSPC



Positive latch
(transparent when CLK= 1)

Negative latch
(transparent when CLK= 0)

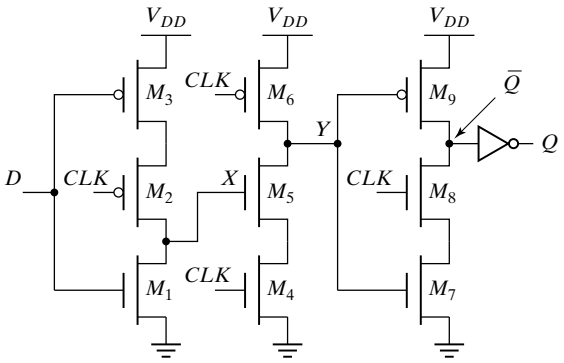
Including Logic in TSPC



Example: logic inside the latch

AND latch

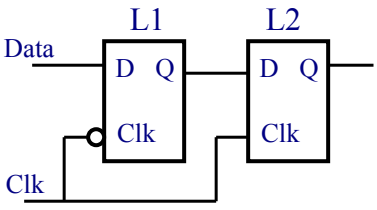
TSPC Register



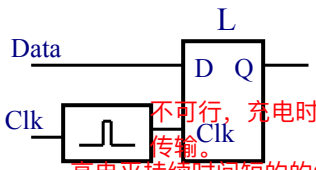
Pulse-Triggered Latches

Ways to design an edge-triggered sequential cell:

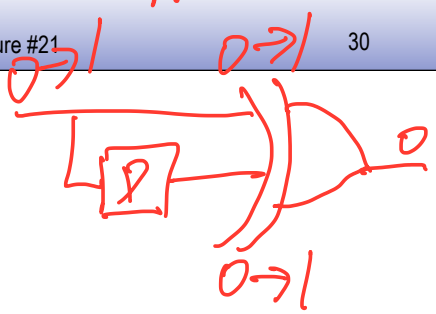
Master-Slave Latches



Pulse-Triggered Latch



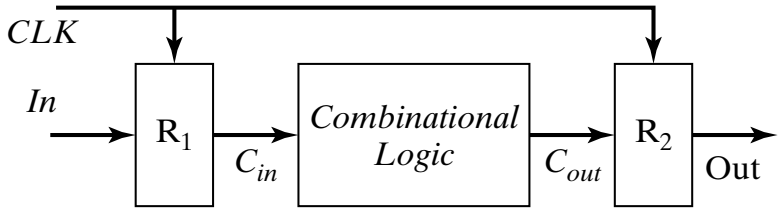
不可行，充电时间太短，可能导致信号无法保持或传输。
高电平持续时间短的的Clk



Why not route the pulse?

Timing

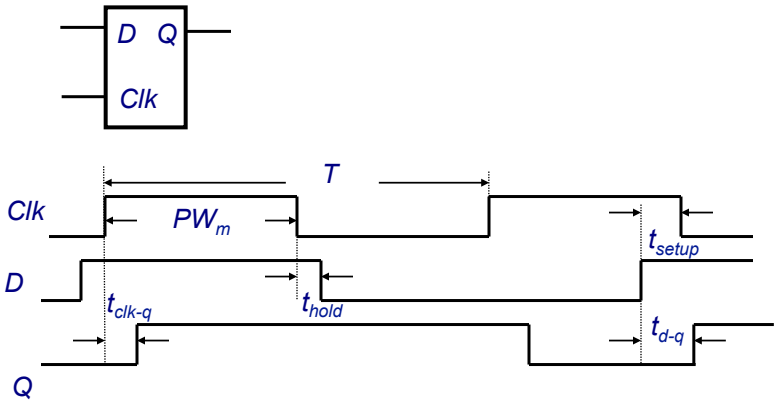
Synchronous Timing



$T_{clk} \geq t_{c\text{-}q} + t_{fpmax} + t_{su}$

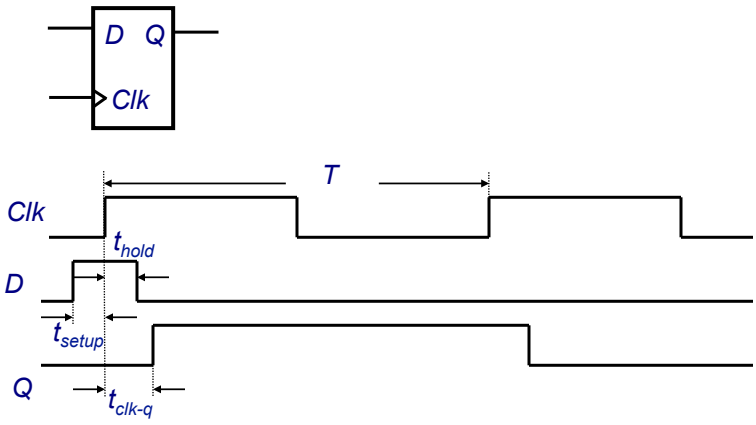
$t_{c\text{-}q} + t_{fpmin} \geq t_{hold}$

Latch Parameters



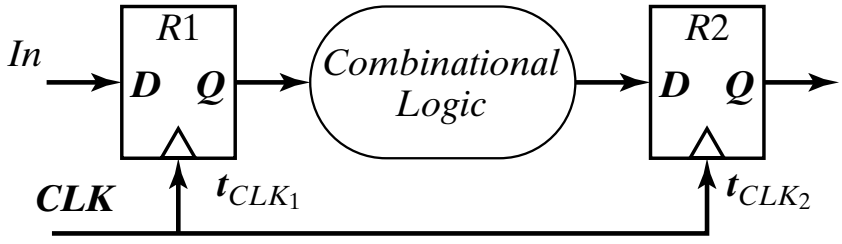
Delays can be different for rising and falling data transitions

Register Parameters



Delays can be different for rising and falling data transitions

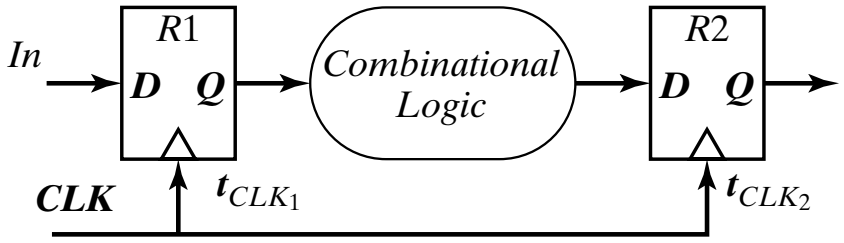
Timing Constraints



t_{clk-q}
$t_{clk-q,min}$
t_{setup}, t_{hold}

t_{logic}
$t_{logic,min}$

Timing Constraints



$t_{clk\text{-}q}$
$t_{clk\text{-}q,min}$
t_{setup}, t_{hold}

t_{logic}
$t_{logic,min}$

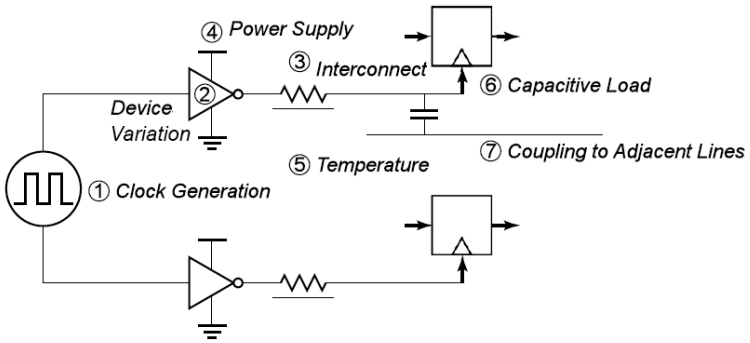
Cycle time (max): $T_{Clk} > t_{clk\text{-}q} + t_{logic} + t_{setup}$

Race margin (min): $t_{hold} < t_{clk\text{-}q,min} + t_{logic,min}$

Clock Nonidealities

- **Clock skew**
  - Spatial variation in temporally equivalent clock edges; deterministic + random, t_{SK}
- **Clock jitter**
  - Temporal variations in consecutive edges of the clock signal; modulation + random noise
  - Cycle-to-cycle (short-term) t_{JS}
  - Long term t_{JL}
- **Variation of the pulse width**
  - Important for level sensitive clocking

Clock Uncertainties



Sources of clock uncertainty