EE141-Spring 2012 Digital Integrated Circuits

Lecture 9
Transistors

Administrativia

- Midterm will be graded early next week
- Lab on Thursday, then resume normal schedule next week (Lab 4)
- Project to be launched next week

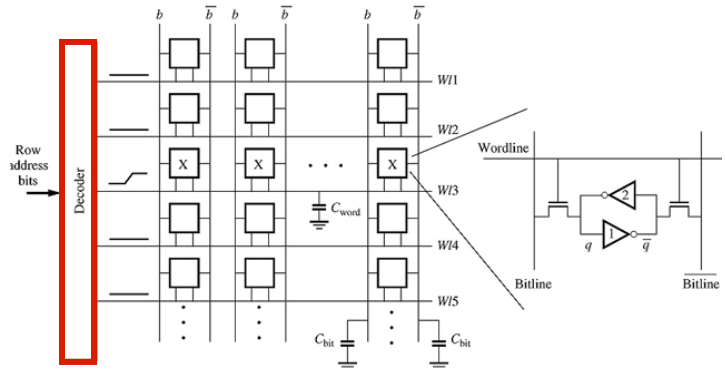
Class Material

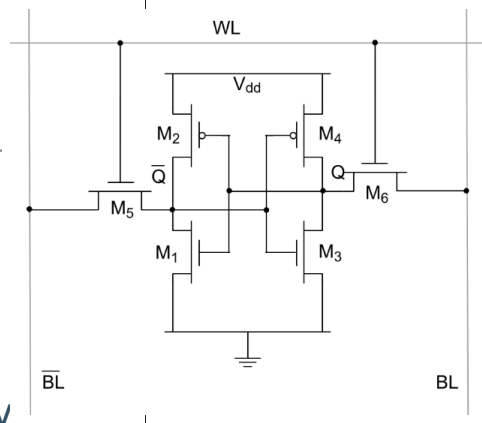
- Last lecture
  - Wiring + Decoders
- Today's lecture
  - Transistor models
- Reading (Ch 3)

Example: Memory Decoders

解码器的layout应该和存储单元的layout一致以使解码器的输出连接到储存单元上的wire都是直线。这样可以节省大量存储空间。或者讲解码器和存储单元应该集成在一起。

Decoder Design Example

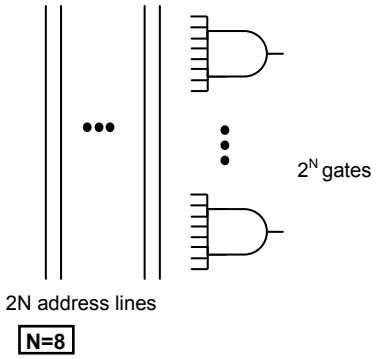




- Look at decoder for 256x256 memory block (8KBytes)

Problem Setup

- Goal: Build fastest possible decoder with static CMOS logic
- What we know
  - Basically need 256 AND gates, each one of them drives one word line



Problem Setup (1)

- Each word line has 256 cells connected to it 2^8
- Total output load is $256*C_{cell} + C_{wire}$
- Assume that decoder input capacitance is $C_{address}=4*C_{cell}$
- Each address drives $2^8/2$ AND gates B二
  - A0 drives ½ of the gates, A0_b the other ½ of the gates 为什么驱动的是与门？看上面图片。
- Neglecting C_{wire}, the fan-out on each one of the 16 address wires is: 8?

$$BF = \frac{C_{load}}{C_{in}} = \frac{(2^8/2)\left(2^8 C_{cell}\right)}{4C_{cell}} = 2^{13}$$

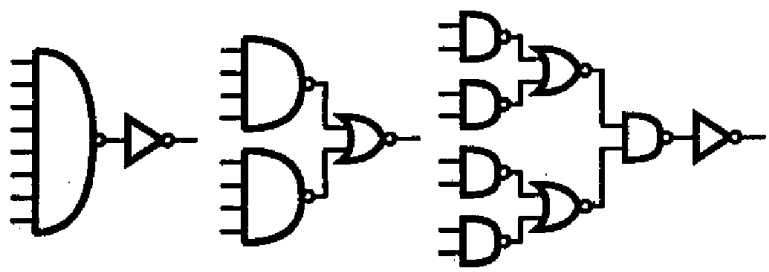
这里的计算不包括LE。

当地址线数量为2时，A0,A1,A0_b,A1_b的俩俩组合共有4种，有一半是A0,有一半是A0_b；A0=1时，A0_b=0；A0=0时，A0_b=1，所以仅有一半的与门被驱动，故地址线数量为8时，只有128个与门被驱动。

Decoder Fan-Out

- BF of at least 2^{13} means that we will want to use more than $\log_4(2^{13}) = 6.5$ stages to implement the AND8 根据这个不包含LE的结果重新设计8 input AND gate
- Need many stages anyways
  - So what is the best way to implement the AND gate?
  - Will see next that it's the one with the most stages and least complicated gates

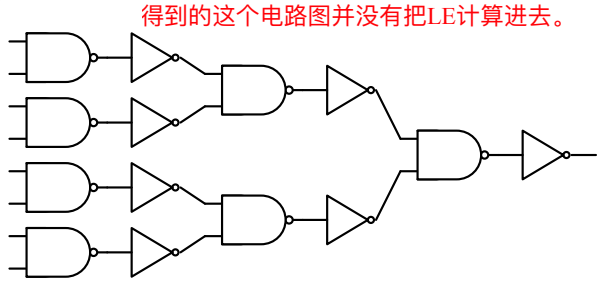
8-Input AND



LE=10/3 1	*LE*=2 5/3	*LE*=4/3 5/3 4/3 1
ΠLE = 10/3	ΠLE = 10/3	ΠLE = 80/27
P = 8 + 1	P = 4 + 2	P = 2 + 2 + 2 + 1

8-Input AND

得到的这个电路图并没有把LE计算进去。



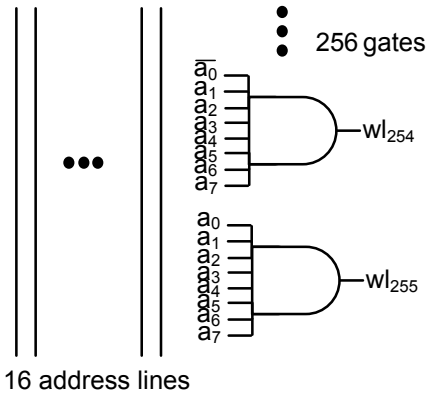
- Using 2-input NAND gates
  - 8-input gate takes 6 stages
- Total LE is $(4/3)^3 \approx 2.4$
- So PE is $2.4*2^{13}$ – optimal N of ~7.1 ???

$\log_4 2.4*2^{13} \approx 7.1$

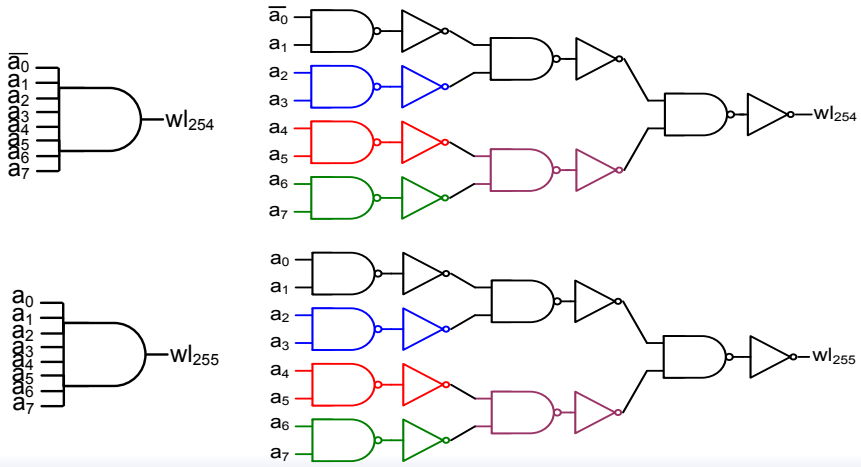
然而即使用了六个stage实现了8 input AND gate，仍然没达到最优的N值，因此可以添加额外的反相器来达到最优的N值。

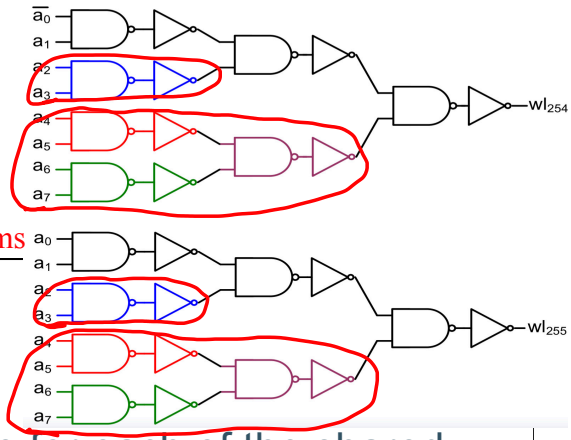
Decoder So Far

- 256 8-input AND gates
  - Each built out of tree of NAND gates and inverters
- Issue:
  - Every address line has to drive 128 gates (and wire) right away
  - Can't build gates small enough - Forces us to add buffers just to drive address inputs



Look Inside Each AND8 Gate

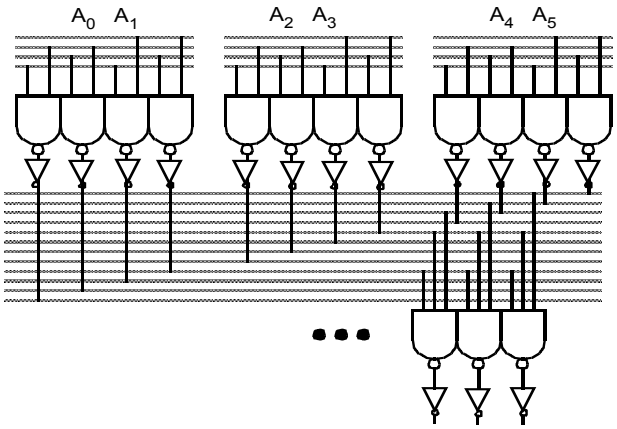




Predecoders

- Use a single gate for each of the shared terms
  - E.g., from A_0, $\overline{A_0}$, A_1, and $\overline{A_1}$, generate four signals: A_0A_1, $\overline{A_0}A_1$, $A_0\overline{A_1}$, $\overline{A_0}\overline{A_1}$
- In other words, we are decoding smaller groups of address bits first
  - And using the "predecoded" outputs to do the rest of the decoding

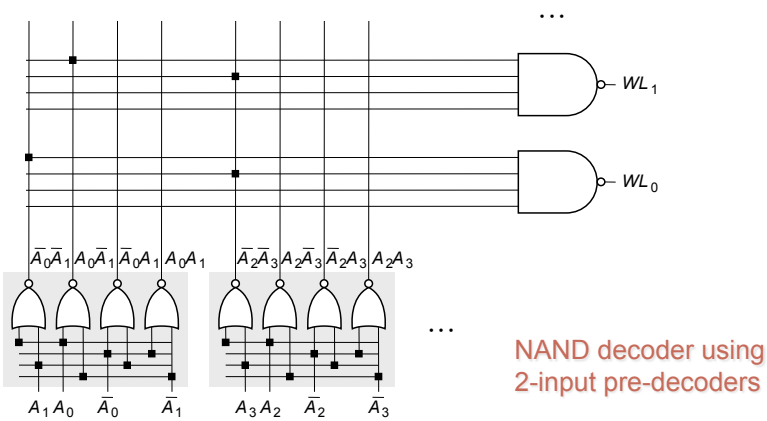
Predecoder and Decoder



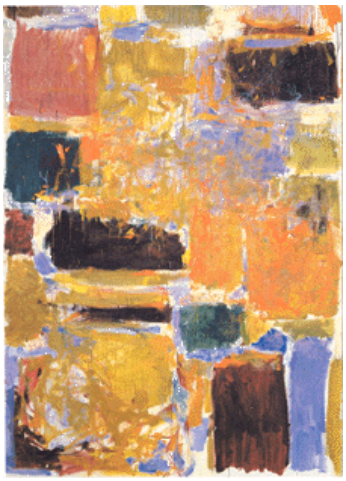
Hierarchical Decoders

节省空间，速度更快。

Multi-stage implementation improves performance



NAND decoder using 2-input pre-decoders



MOS Transistor

transistor decides , capacitors, current 都是非线性的。
但有方法，可以把这些东西转化为比较简单的模型进行分析。

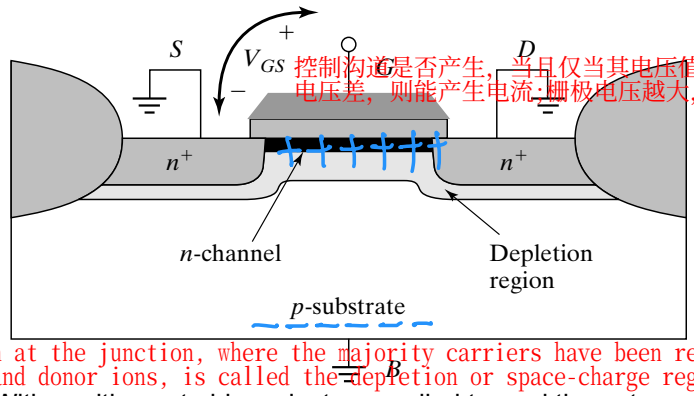
What do digital IC designers need to know?

The MOSFET is a four terminal device. The voltage applied to the gate terminal determines if and how much current flows between the source and the drain ports. The body represents the fourth terminal of the transistor. Its function is secondary as it only serves to modulate the device characteristics and parameters.

MOS devices can also be made by using an n-type substrate and p+ drain and source regions. In such a transistor, current is carried by holes moving through a p-type channel. The device is called a p-channel MOS, or PMOS transistor.

The NMOS transistor consists of n+ drain and source regions, embedded in a p-type substrate.

Threshold Voltage: Concept



控制沟道是否产生，当且仅当其电压值大于阈值电压时，沟道产生，此时若S和D存在电压差，则能产生电流；栅极电压越大，沟道越宽，电阻越低。

NMOS

The region at the junction, where the majority carriers have been removed, leaving the fixed acceptor and donor ions, is called the depletion or space-charge region.

- With positive gate bias, electrons pulled toward the gate
- With large enough bias, enough electrons will be pulled to "invert" the surface (p→n type)
- Voltage at which surface inverts: "magic" threshold voltage V_T

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对于二极管Diode：
forward-bias：正向偏置，P+接正极，N+接负极
reverse-bias：反向偏置，N+接正极，P+接负极

B=BODY=衬底
potential=电势

The Threshold Voltage

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, $\varepsilon_{ox} = 3.97\varepsilon_0 = 3.5\times10^{-11}$ F/m

- Threshold

Cox stands for the capacitance per unit area presented by the gate oxide

$$V_T = \varphi_{FB} + 2\varphi_F + \frac{Q_B}{C_{ox}}$$

Depletion charge

ε_{ox} is the oxide permittivity.

t_{ox} is the thickness of the oxide.

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{2\varphi_F}\right)$$

VT0 is an empirical parameter which is the threshold voltage for VSB =0.
The value of VGS where strong inversion occurs is called the threshold voltage VT0.
VSB is a substrate bias which is applied between source and body.
NA is the substrate doping.

- Fermi potential $\varphi = \phi$ 这里没区分大小写。

fermi potential $\phi_F = \phi_T \cdot \ln\frac{N_A}{n_i}$

$2\Phi_F$ is approximately 0.6V for p-type substrates

γ is the body factor body-effect coefficient.It expresses the impact of changes in VSB.

V_{T0} is approximately 0.45V for our process

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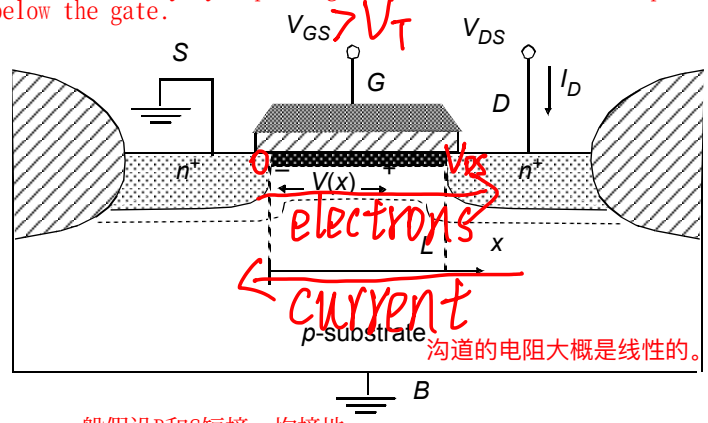
Threshold voltage has a positive value for a typical NMOS device, while it is negative for a normal PMOS transistor.
NA is the substrate doping

NMOS：p型衬底，磷或砷等五价元素参杂，自由电子是多数载流子，主要由五价元素提供，空穴是少数载流子，主要由热激发提供
在电子发生移动后，五价元素带正电
PMOS：n型衬底，硼或镓等三价元素参杂，空穴是多数载流子，主要由三价元素提供，自由电子是少数载流子，主要由热激发提供
空穴在俘获电子后，三价元素带负电
一般用增强型，耗尽型在实际设计中基本不用。

Transistor with Gate and Drain Bias

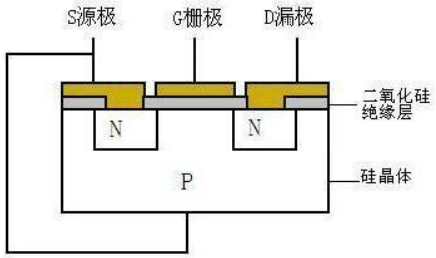
The positive gate voltage causes positive charge to accumulate on the gate electrode and negative charge on the substrate side. The latter manifests itself initially by repelling mobile holes. Hence, a depletion region is formed below the gate.

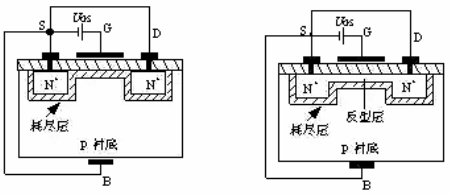


沟道的电阻大概是线性的。=Rlin

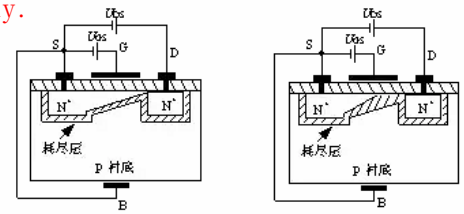
一般假设B和S短接，均接地

必须确保VGS>VT否则沟道会消失。你不会再出现反相。





(a) $0 < U_{GS} < U_T$ (b) $U_{GS} > U_T$



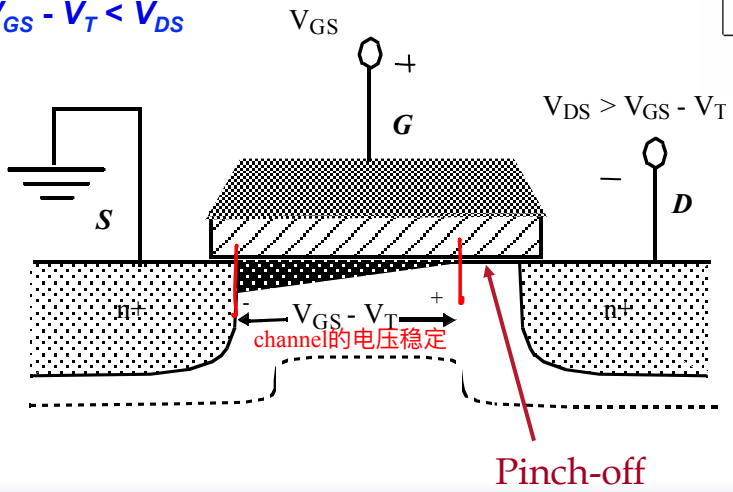
(a) $U_{DS}=U_{GS}-U_T$ (b) $U_{DS} > U_{GS}-U_T$

Circuit symbols for the various MOS transistors are shown abovefigure.The transistor is a four-port device with gate, source, drain, and body terminals. Since the body is generally connected to a dc supply that is identical for all devices of the same type (GND for NMOS, Vdd for PMOS), it is most often not shown on the schematics .If the fourth terminal is not shown, it is assumed that the body is connected to the appropriate supply.

VGS=VT，channel消失

Transistor in Saturation

$0 < V_{GS} - V_T < V_{DS}$



Saturation

- For $(V_{GS} - V_T) < V_{DS}$, the effective drain voltage and current saturate:

$$V_{DS,eff} = (V_{GS} - V_T)$$

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

- Of course, real drain current isn't totally independent of V_{DS}
  - For example, approx. for channel-length modulation:

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$$

$k_n' = \mu_n C_{ox}$

k'n is called the process transconductance parameter and equals
The product of the process transconductance and the (W/L) ratio of an (NMOS)
transistor is called the gain factor kn of the device.

W is the width of the channel in a direction perpendicular to the current flow.

Modes of Operation

Cutoff:

$V_{GS} - V_T < 0$ $\quad I_D = 0$

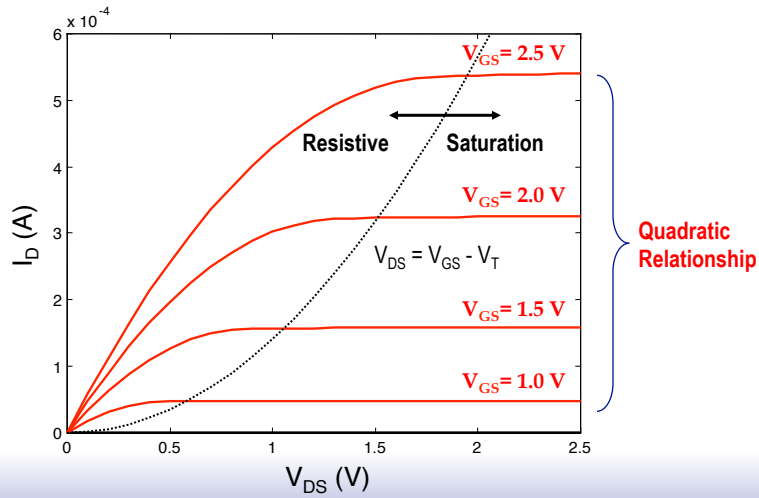
Linear (Resistive):

$V_{GS} - V_T > V_{DS}$ $\quad I_D = k_n' \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$

Saturation:

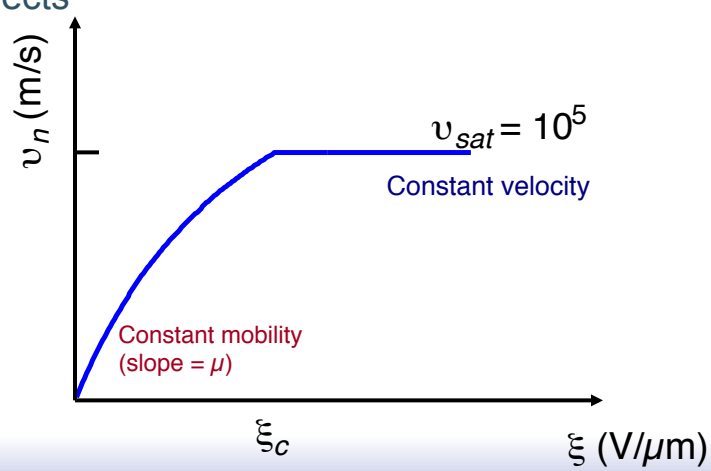
$0 < V_{GS} - V_T < V_{DS}$ $\quad I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$

Current-Voltage Relations: A Good Ol' Transistor



Velocity Saturation

- Velocity saturates due to carrier scattering effects



the velocity of the carriers is proportional to the electrical field, independent of the value of that field. In other words, the carrier mobility is a constant. However, at high field strengths, the carriers fail to follow this linear model. In fact, when the electrical field along the channel reaches a critical value ξc, the velocity of the carriers tends to saturate due to scattering effects (collisions suffered by the carriers).

Including Velocity Saturation

Approximate velocity:

$$\upsilon = \frac{\mu_n \xi}{1 + \xi/\xi_c} \quad \text{for} \quad \xi \le \xi_c$$

$$= \upsilon_{sat} \quad \text{for} \quad \xi \ge \xi_c$$

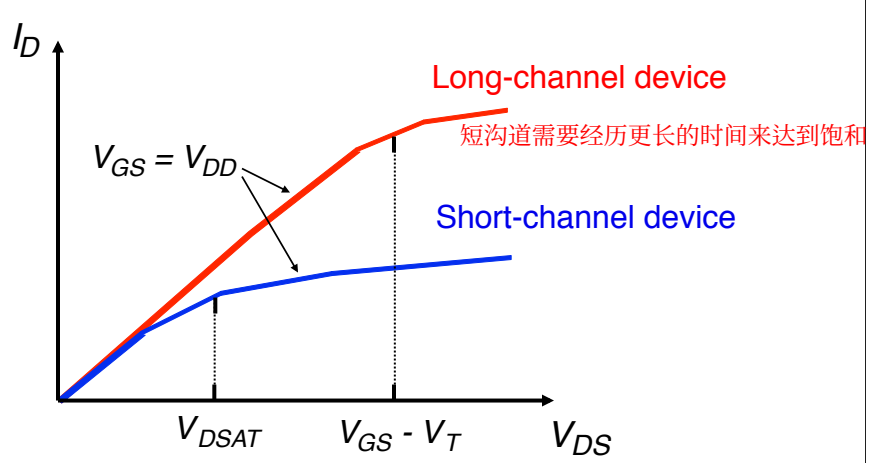
Continuity requires that:

$$\xi_c = 2\upsilon_{sat}/\mu_n$$

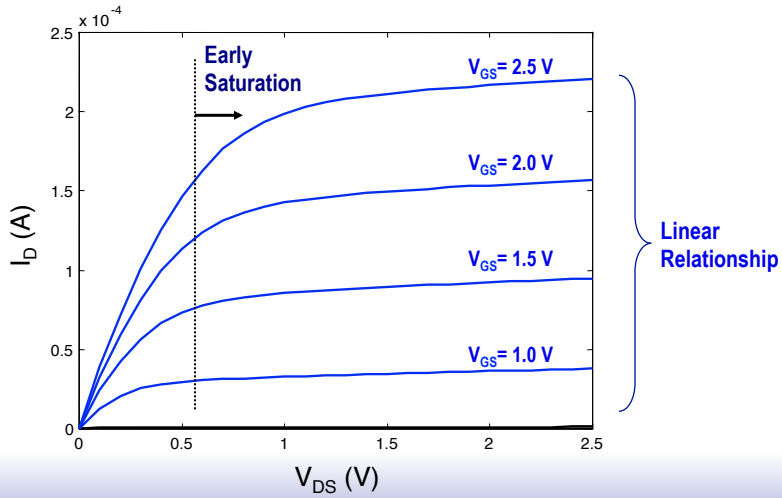
Integrating to find the current again:

$$I_D = \frac{\mu_n C_{ox}}{1 + (V_{DS}/\xi_c L)}\left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

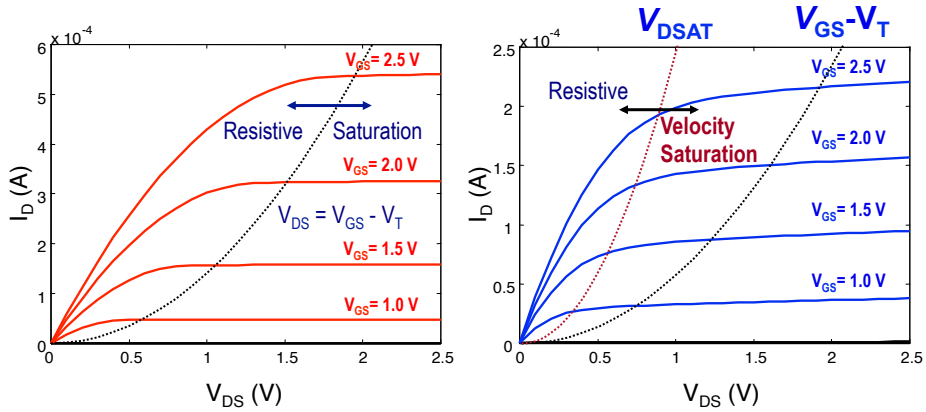
Velocity Saturation



Current-Voltage Relations: The Deep Sub-Micron Transistor



Regions of Operation

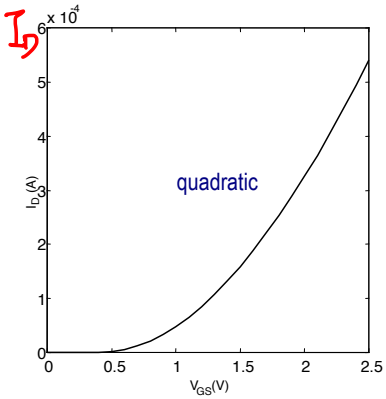


Long Channel (L=2.5μm)

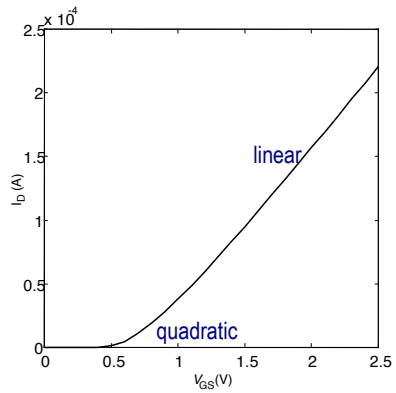
W/L=1.5

Short Channel (L=0.25μm)

I_D versus V_{GS}



Long Channel
(L=2.5μm)



Short Channel
(L=0.25μm)

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The saturation current IDSAT displays a linear dependence with respect to the gate-source voltage VGS, which is in contrast with the squared dependence in the long-channel device. This reduces the amount of current a transistor can deliver for a given control voltage. On the other hand, reducing the operating voltage does not have such a significant effect in submicron devices as it would have in a long-channel transistor

上面的真实模型太复杂，下面开始简化模型：

Models, Models, Models…

- Exact behavior of transistor in velocity sat. somewhat challenging if want simple/easy to use models
- So, many different models developed over the years
  - v-sat, alpha, unified, V_T*, etc.
- Simple model for manual analysis desirable
  - Assume velocity perfectly linear until υ_{sat}
  - Assume V_{DSAT} constant

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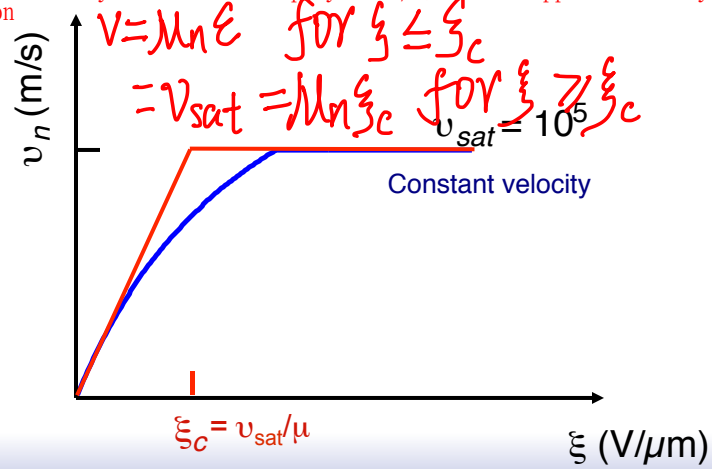
Simplified Velocity Saturation

- Assume velocity perfectly linear until hit υ_{sat}

The velocity saturates abruptly at ξc, and is approximated by the following expression

$v = \mu_n \mathcal{E}$ for $\xi \le \xi_c$

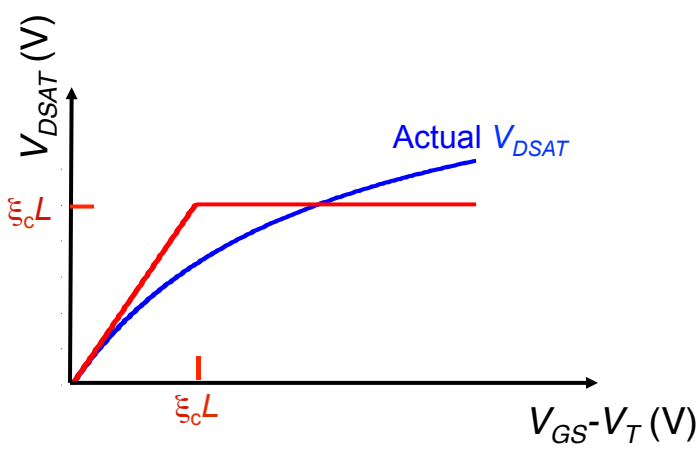
$= v_{sat} = \mu_n \xi_c$ for $\xi \ge \xi_c$



Simplified Velocity Saturation (cont'd)

$V_{GT} =$

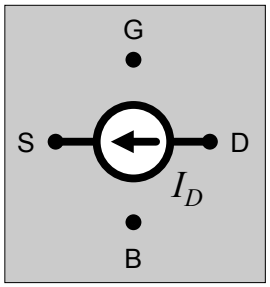
- Assume $V_{DSAT} = \xi_c L$ when $(V_{GS} - V_T) > \xi_c L$



The drain-source voltage VDSAT at which the critical electrical field is reached and velocity saturation comes into play is constant and is approximated

这个模型简单而直观，且不会产生复杂的方程，

A Unified Model for Manual Analysis



define $V_{GT} = V_{GS} - V_T$

for $V_{GT} \le 0$: $I_D = 0$

for $V_{GT} \ge 0$:

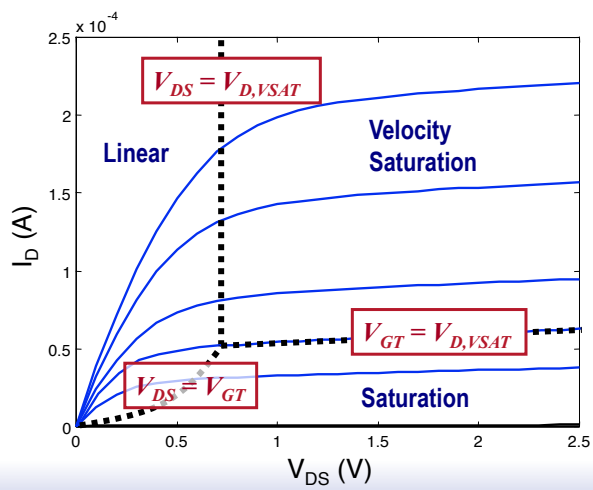
$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{DS,eff} - \frac{V_{DS,eff}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})$$

with $V_{DS,eff} = \min(V_{GT}, V_{DS}, V_{D,VSAT})$

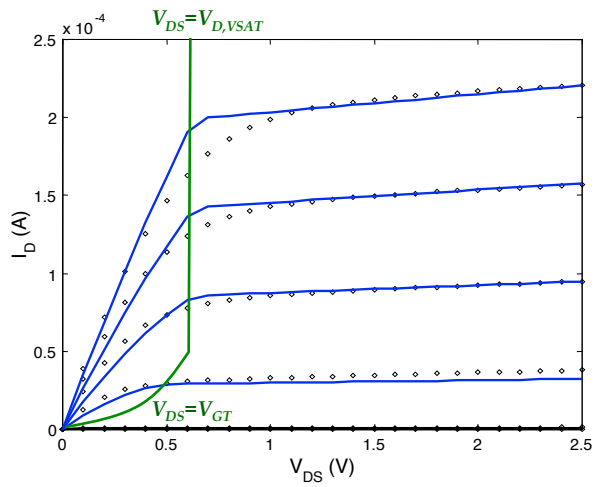
VTO，γ，VDSAT，k’这些参数要根据实际器件进行匹配。

Simplified Model

- Define $V_{GT} = V_{GS} - V_T$, $V_{D,VSAT} = \xi_c \cdot L$



Simple Model versus SPICE



Assuming that the supply voltage is substantially larger than the velocity-saturation voltage VDSAT of the transistor, it is fair to state that the transistor stays in velocity saturation for the entire duration of the transition. This scenario is plotted in for the case of an NMOS discharging a capacitor from VDD to VDD/2.

One Last Simplification

- If device always operates in velocity sat.:

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T - \frac{V_{D,VSAT}}{2} \right) V_{D,VSAT}$$

- "V_T*" model:

$$V_T^* \equiv V_T + \frac{V_{D,VSAT}}{2}$$

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T^* \right) V_{D,VSAT}$$

- Good for first cut, simple analysis

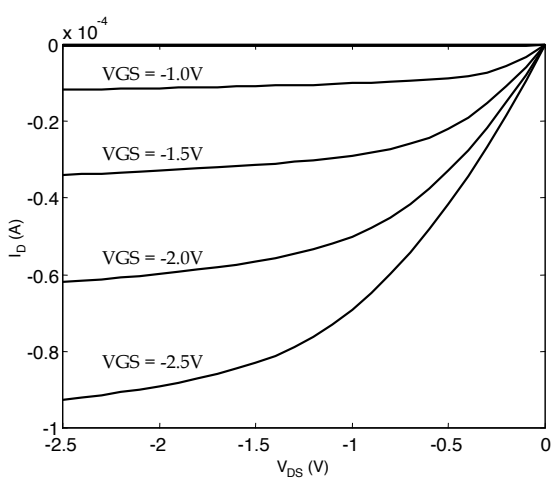
Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

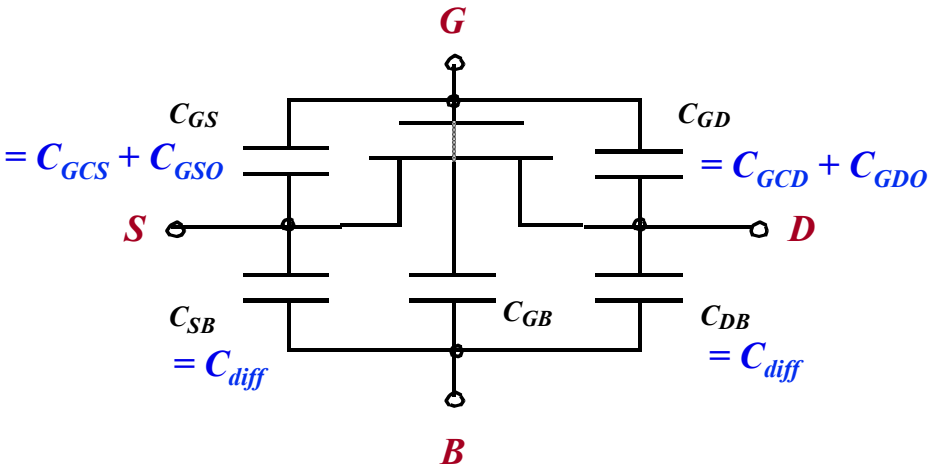
	V_{T0} (V)	γ ($V^{0.5}$)	V_{VSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

Textbook: page 103
ebook:91

A PMOS Transistor



- All variables negative
- I prefer to work with absolute values – makes life easier.

MOS Capacitance Sneak Preview

MOS Capacitances