EE141-Spring 2012 Digital Integrated Circuits

Lecture 2
Design Metrics

ADMINISTRATIVIA

Administrative Stuff

- Labs start next week
- Homework #1 is due next Wednesday
  - Your card key should be operational for Cory 125. Please check ASAP!
  - Have some more instructional accounts for those who may not have them yet.
  - Use cory, quasar, pulsar

Last Lecture

- Last lecture
  - Introduction, Moore's law, future of ICs
- Today's lecture
  - Introduces basic metrics for design of integrated circuits
  - How to measure cost?
  - Intro to IC manufacturing

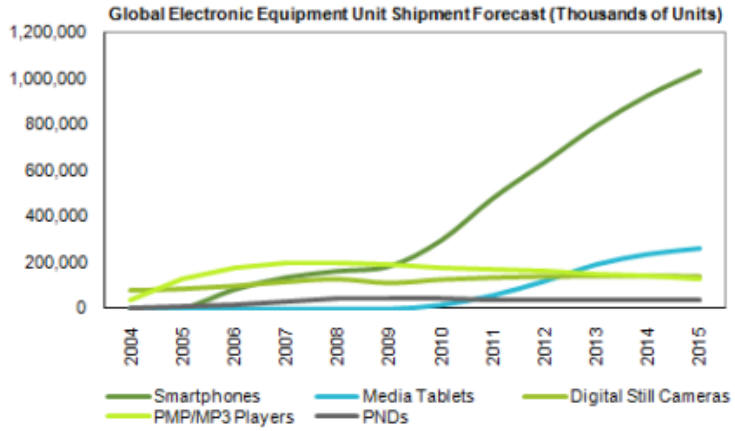
Scaling Impact Continued

Why Scaling?

Why choose 0.7;because area will go down with a factor of 2, and 0.7*0.7=0.49=1/2

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But … Function不变，晶体管数量不变，工艺提高，area缩小一半 cost缩小一半，也不完全正确，因为不只area影响cost
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Way Beyond Microprocessors



Source: IHS iSuppli, July 2011

Challenges in Digital Design

∝ DSM

"Microscopic Problems"

- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

Everything Looks a Little Different

?

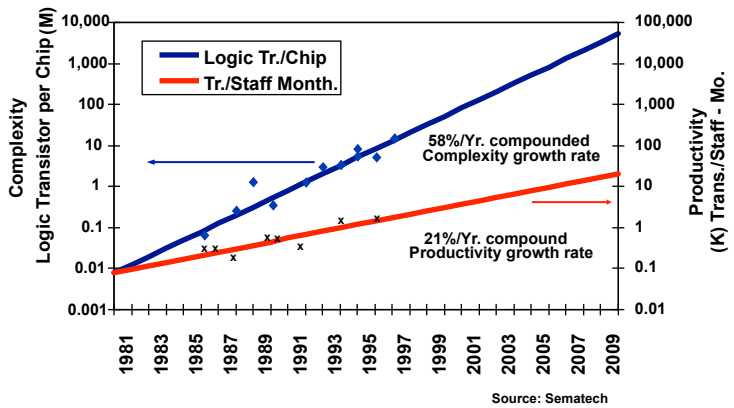
∝ 1/DSM

"Macroscopic Issues"

- Complexity
- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

…and There's a Lot of Them!

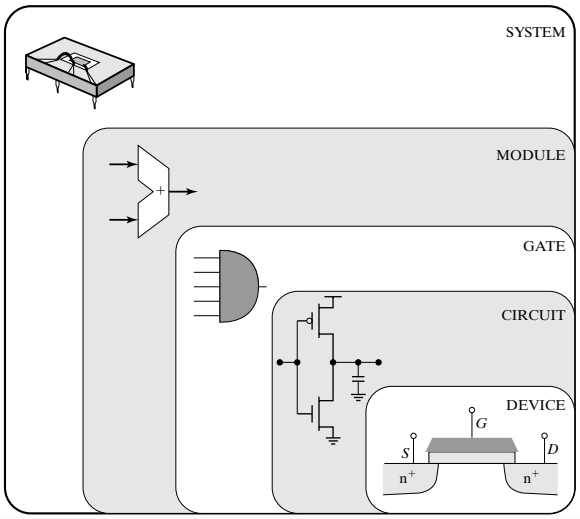
Productivity Trends



Complexity outpaces design productivity

Courtesy, ITRS Roadmap

Design Abstraction Levels



Design Metrics

Design Metrics

- How to evaluate quality/performance of a digital circuit (gate, block, …)?
  - Cost 最重要最优先考虑的因素
  - Reliability
  - Speed/Performance (delay, frequency)
  - Power

Design Metrics: Cost

Cost of Integrated Circuits

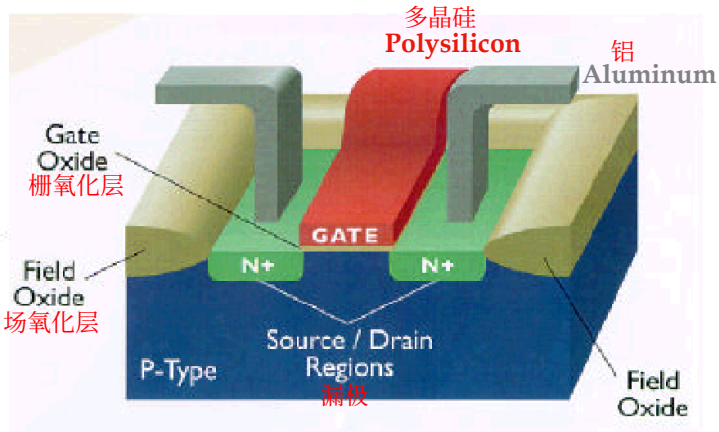
非经常性成本或一次性成本或非重复性成本

- NRE (non-recurrent engineering) costs - fixed
  - Independent of volume (i.e., number of units made/sold) 芯片数量
  - Examples: design time and effort, mask generation, equipment, etc. Photomask Fab晶圆厂
- Recurrent costs - variable
  - proportional to volume 面积越大，例子中的成本也会越大。它们的成本和面积成比例。recurrent costs和面积成比例。
  - Examples: silicon processing, packaging, test 材料成本，运输成本，testing
  - Most of these proportional to chip area在test上花费的时间越多，所需要的成本越多。

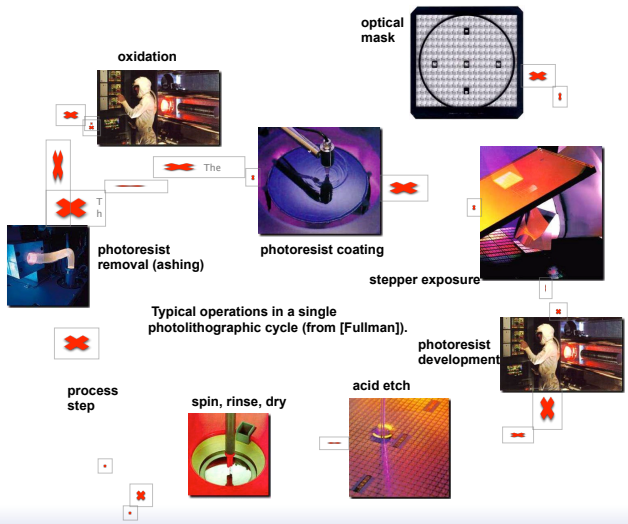
为了降低NRE成本，设计出来的芯片必须大量销售，如果芯片预计需求量低于某个阈值可以使用FPGA等可编程硬件代替。

芯片面积越大，生产出有问题的芯片的概率越高，所以recurrent costs会越大。

The MOS Transistor

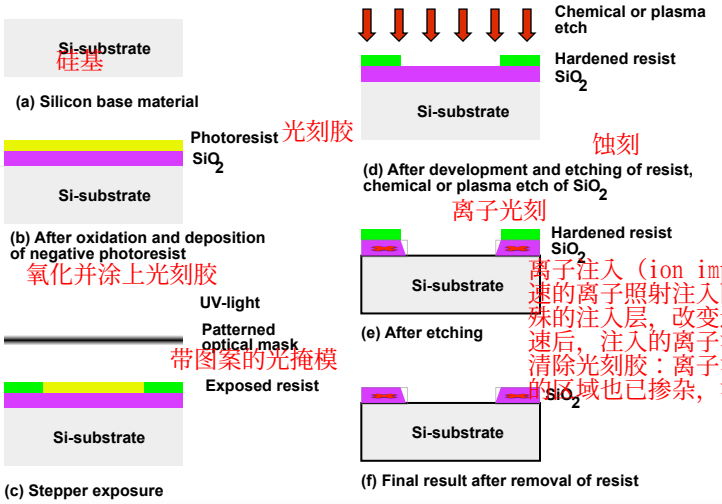


Review: Photo-Lithographic Process



Patterning of SiO_2

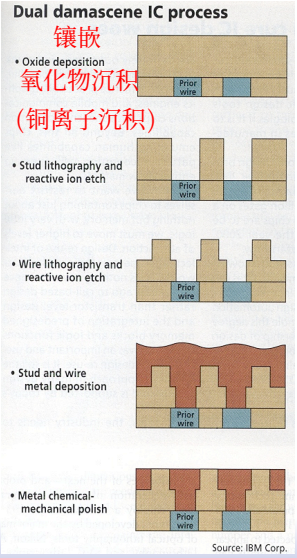
(d)(e)(f)用化学物质溶解掉暴露出来的晶圆部分，剩下的光刻胶保护着不应该蚀刻的部分。蚀刻完成后，清除全部光刻胶，露出一个个凹槽。再次浇上光刻胶，光刻后洗掉曝光部分，剩下的光刻胶用来保护不会离子注入的那部分材料。接着进行离子注入。

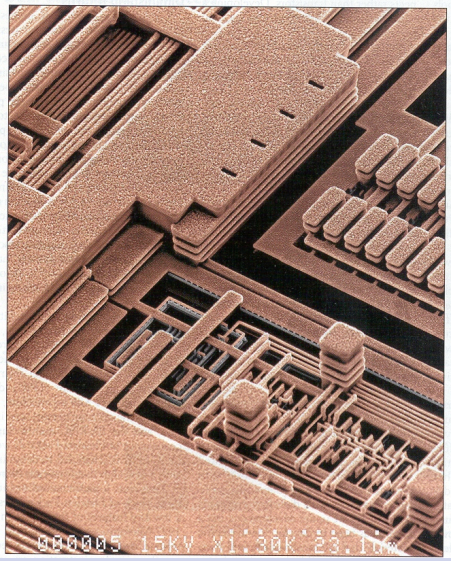


离子注入（ion implantation）：在真空系统中，用经过加速的离子照射注入固体材料，从而在被注入的区域形成特殊的注入层，改变这些区域的硅的导电性。经过电场的加速后，注入的离子流的速度可以超过30万千米每小时。清除光刻胶：离子注入完成后，光刻胶也被清除，而注入的区域也已掺杂，注入了不同的原子。

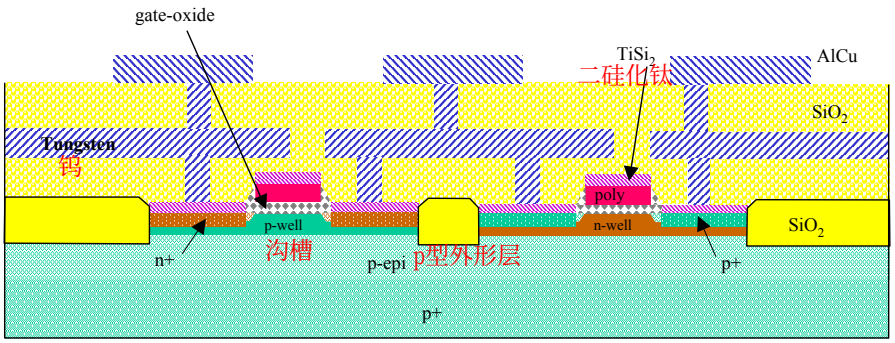
紫外线透过掩膜照射光刻胶，掩膜上印着预先设计好的电路图案。光刻过程中曝光在紫外线下的光刻胶被溶解掉，清除后留下的图案和掩膜上的一致。

Advanced Metallization





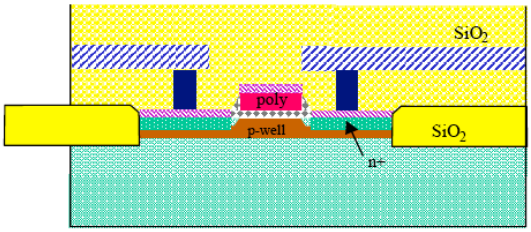
A Modern CMOS Process



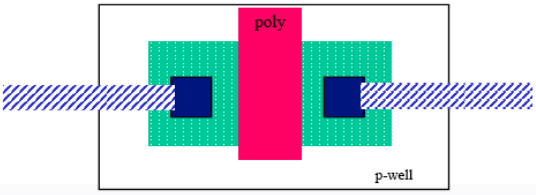
Dual-Well Shallow-Trench-Isolated CMOS Process
浅沟

Transistor Layout

Cross-Sectional View



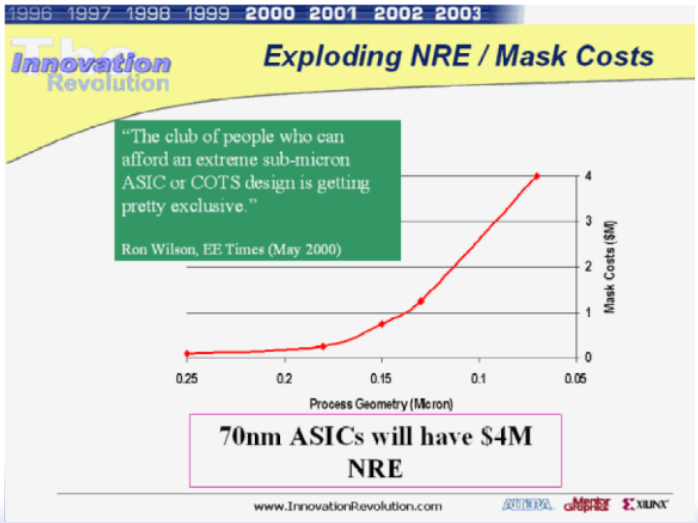
Layout View



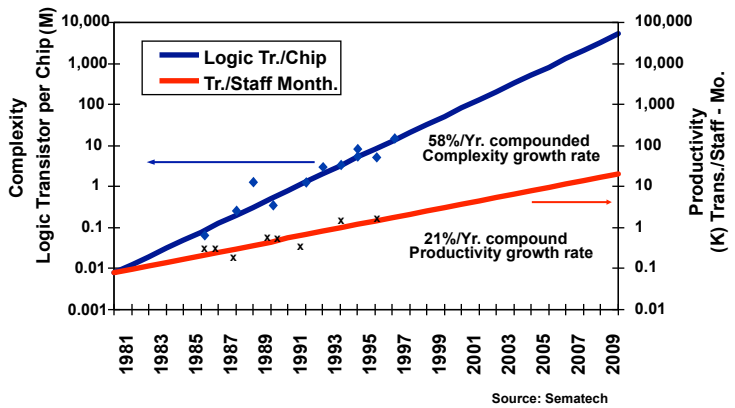
Back to Cost

- NRE (non-recurrent engineering) costs - fixed
  - Independent of volume (i.e., number of units made/sold)
  - Examples: design time and effort, mask generation, equipment, etc.
- Recurrent costs - variable
  - proportional to volume
  - Examples: silicon processing, packaging, test
  - Most of these proportional to chip area

NRE Cost is Increasing



Productivity Trends



Complexity outpaces design productivity

Courtesy, ITRS Roadmap

Total Cost

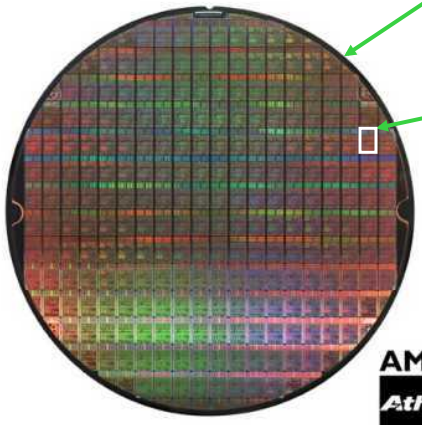
- Cost per IC

$$\text{cost per IC} = \underbrace{\text{variable cost per IC}} + \frac{\text{fixed cost}}{\text{volume}}$$

- Variable cost

$$\text{variable cost} = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}$$

Die Cost



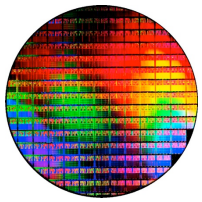
$$\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} * \text{die yield}}$$

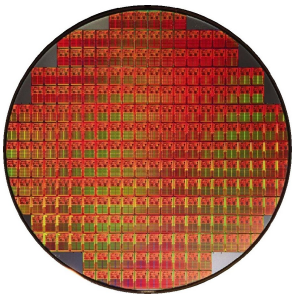
AMD Athlon

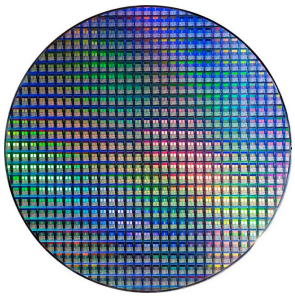
From: http://www.amd.com

Wafer size

AMD Athlon







8” (200mm)
90nm CMOS

12” (300mm)
90nm CMOS

12” (300mm)
65nm CMOS

Next: 18” Wafers?

From: http://www.sandpile.org

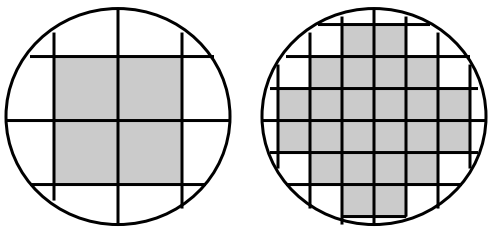
G. Moore, Keynote Address ISSCC 2003

Yield

$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

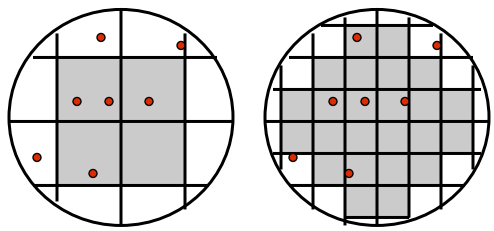
$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$



Defects

Yield = 1/4



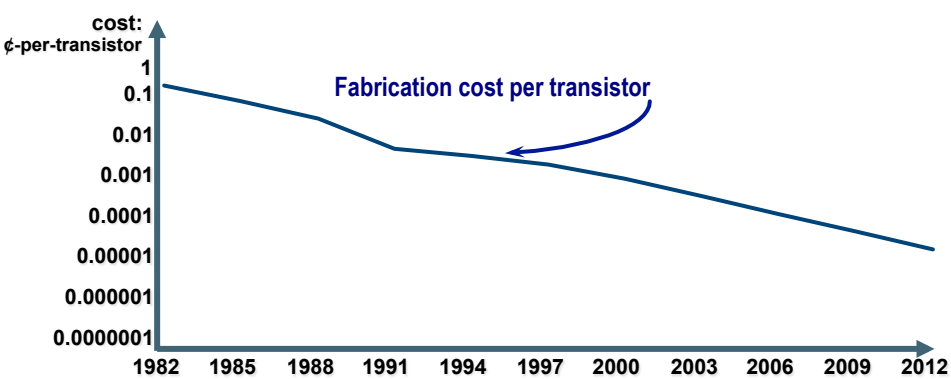
Yield = 19/24

$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$, where α is approximately 3

$$\downarrow$$

$$\text{die cost} \propto \frac{1}{\left[\left(\text{die/wafer} \propto \text{die area}^{-1}\right)\left(\text{yield} \propto \text{die area}^{-3}\right)\right]} \propto \text{die area}^{4}$$

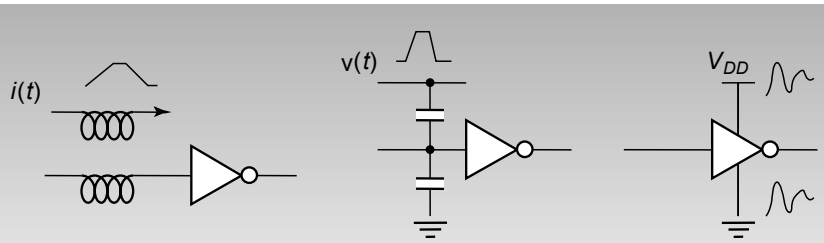
Cost per Transistor



Design Metrics: Reliability

Reliability

- The real world is analog
  - All physical quantities you deal with as a circuit designer are actually continuous
- Thus, even a "digital" signal can be noisy:



Inductive coupling | Capacitive coupling | Power and ground noise

电线位于物理空间中被电介质包围，如果有太多电线邻近，相邻的电线之间的电介质会形成电容器。

Noise and Digital Systems

Ignore all physical effect and translates it in two levels zero and one.

- Circuit needs to works despite "analog" noise
  - Digital gates can reject noise
  - This is actually how digital systems are defined
- Digital system is one where:
  - Discrete values mapped to analog levels and back
  - All the elements (gates) can reject noise
    - For "small" amounts of noise, output noise is less than input noise
  - Thus, for sufficiently "small" noise, the system acts as if it was noiseless

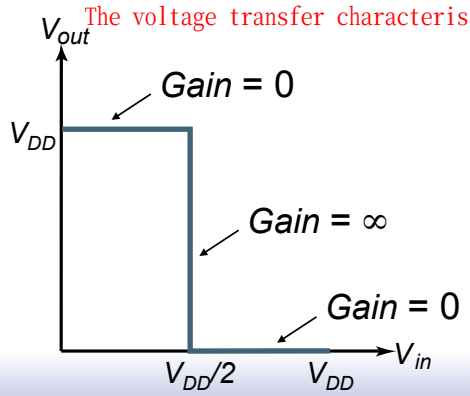
Noise Rejection

Maps DC behavior of our gates as a function
y为输出电压，x为输入电压

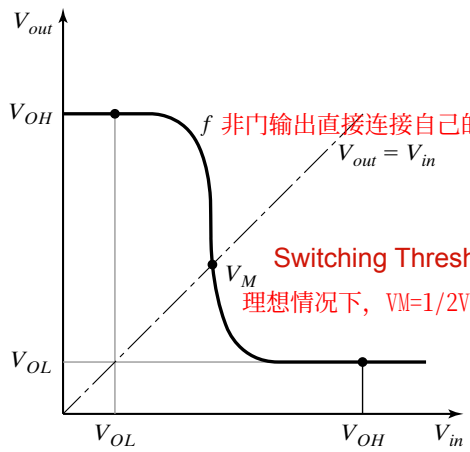
- To see if a gate rejects noise
  - Look at its DC voltage transfer characteristic (VTC)
  - See what happens when input is not exactly 1 or 0

The voltage transfer characteristic of inverter

- Ideal digital gate:
  - Noise needs to be larger than $V_{DD}/2$ to have any effect on gate output



More Realistic VTC



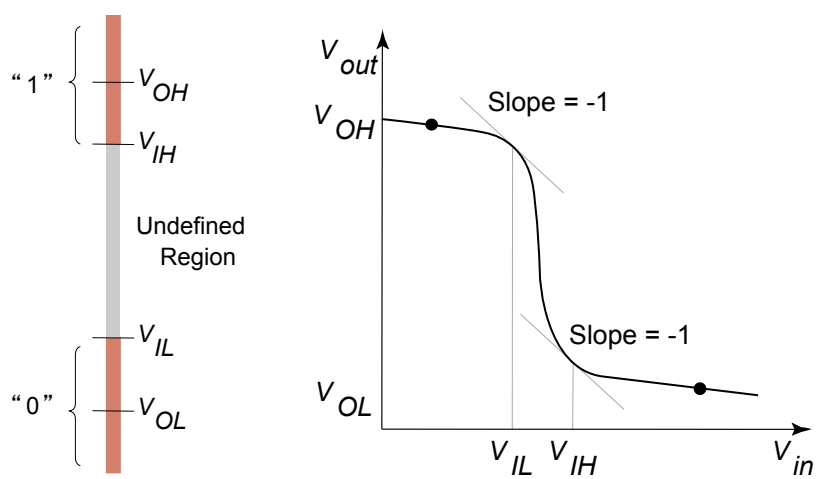
VOH = *f*(VOL)
VOL = *f*(VOH)
VM = *f*(VM)

Switching Threshold

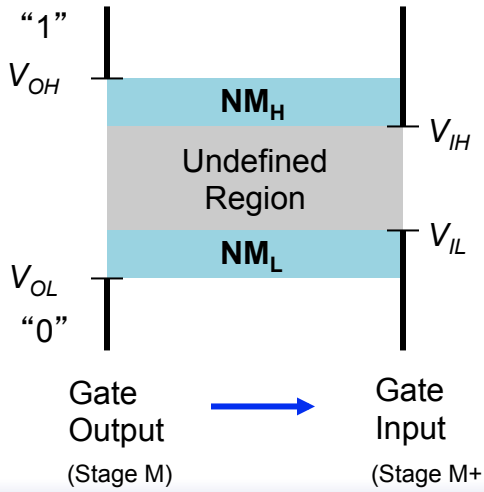
理想情况下，VM=1/2VDD，因为理想情况下，传输特性曲线是完全对称的。

Nominal Voltage Levels

Voltage Mapping



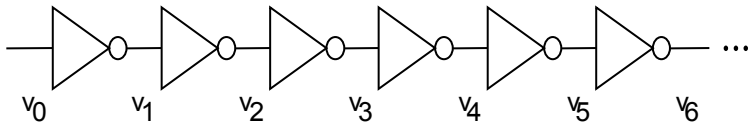
Definition of Noise Margins



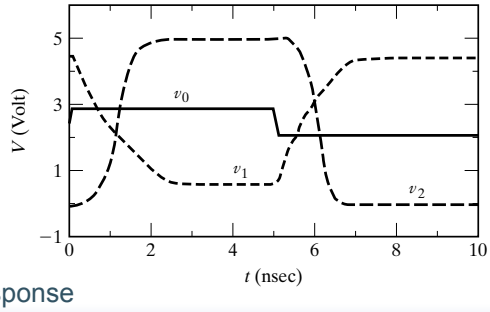
Noise margin high:
$NM_H = V_{OH} - V_{IH}$

Noise margin low:
$NM_L = V_{IL} - V_{OL}$

Digital Gate Noise Reduction: Regenerative Property

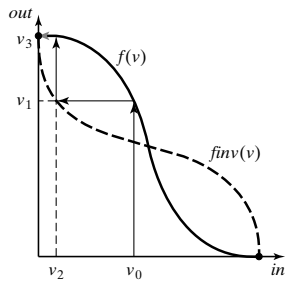


A chain of inverters

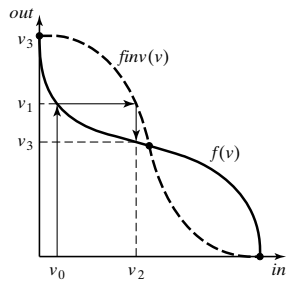


Simulated response

Regenerative Property (Another View)

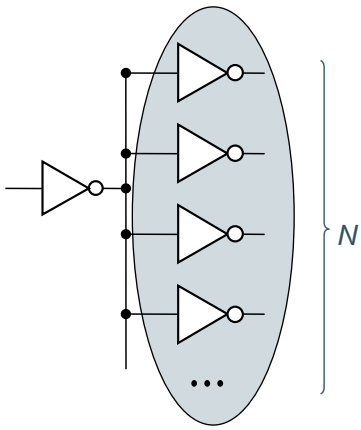


Regenerative

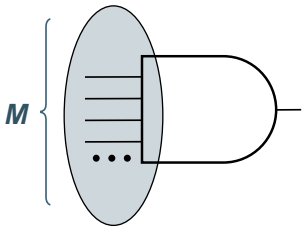


Non-Regenerative

Fan-in and Fan-out



Fan-out *N*



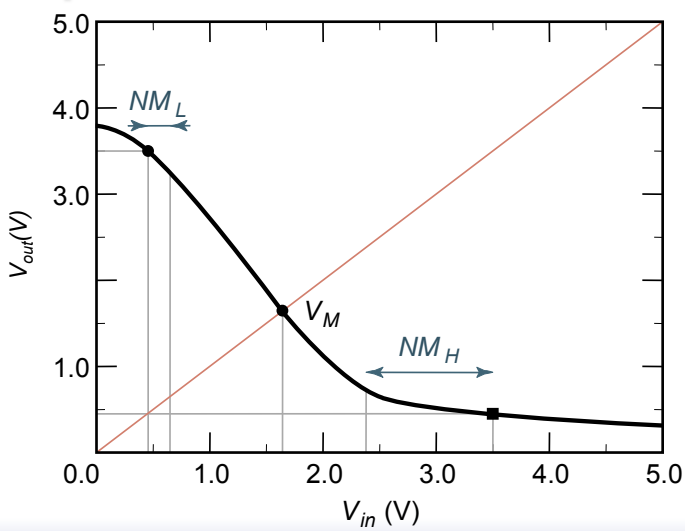
Fan-in *M*

There is a modified definition of fan-out for CMOS logic

Key Reliability Properties

- Absolute noise margin values are not the only things that matter
  - e.g., floating (high impedance) nodes are more easily disturbed than low impedance nodes (in terms of voltage)
- Noise immunity (i.e., how well the gate suppresses noise sources) needs to be considered too
- Summary of some key reliability metrics:
  - Noise transfer functions & margin (ideal: gain = ∞, margin = $V_{dd}/2$)
  - Output impedance (ideal: $R_o = 0$)
  - Input impedance (ideal: $R_i = \infty$)

Example: An Old-time Inverter



Example: An Old-time Inverter

- V_{OH} = 3.6V
- V_{OL} = 0.4V
- V_{IL} = 0.6V
- V_{IH} = 2.3V
- $NM_H = V_{OH} - V_{IH}$ = 1.3V
- $NM_L = V_{IL} - V_{OL}$ = 0.2V

Summary

- Understanding the design metrics that govern digital design is crucial
  - We discussed cost and reliability so far
- Key design messages so far:
  - Keep chip area as small as possible
  - Pick design styles and parameters so that noise margins are reasonable