EE141-Spring 2012 Digital Integrated Circuits

Lecture 16
Complex CMOS - Revisited

Administrativia

- Project questions?
- Midterm on Friday – covers wires, transistors, inverter VTC, and arithmetic
  - Review session planned for We evening.

Class Material

- Last lecture
  - SRAM, Inverter delay
- Today's lecture
  - Optimizing complex CMOS
- Reading: Ch 6

CMOS Power Dissipation

Where Does Power Go in CMOS?

- Switching power
  - Charging/discharging capacitors
- Leakage power
  - Transistors are imperfect switches
- Short-circuit power
  - Both pull-up and pull-down on during transition
- Static currents
  - Biasing currents, in e.g. analog, memory

$CV_{DD}^2 f$

$CV_{sw} V_{DD} f$ (if $V_{sw} < V_{DD}$)

determine ← rising time and falling time are important.

always exist

Transition Activity and Power

- Energy consumed in N cycles, E_N:

$$E_N = C_L \bullet V_{DD}^2 \bullet n_{0\to1}$$

$n_{0\to1}$ – number of 0→1 transitions in N cycles

$$P_{avg} = \lim_{N\to\infty} \frac{E_N}{N} \cdot f = \left(\lim_{N\to\infty} \frac{n_{0\to1}}{N} \right) \cdot C_L \cdot V_{DD}^2 \cdot f$$

$$\alpha_{0\to1} = \lim_{N\to\infty} \frac{n_{0\to1}}{N}$$ in a clock cycle

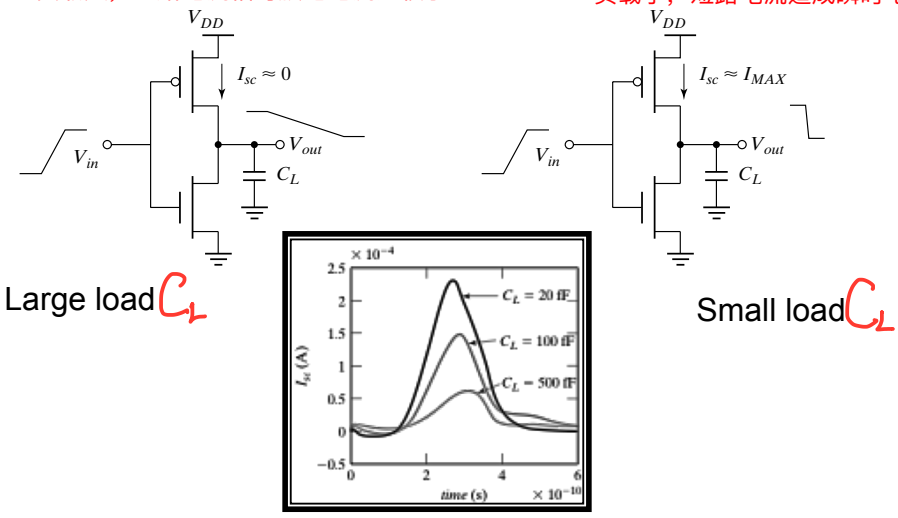
$$P_{avg} = \alpha_{0\to1} \cdot C_L \cdot V_{DD}^2 \cdot f$$ @ clock

为了使短路电流尽可能小，负载电容要尽可能大或者使输出尽可能缓慢。
另一种方法是使rising slope和falling slope尽可能一样

Short Circuit Current

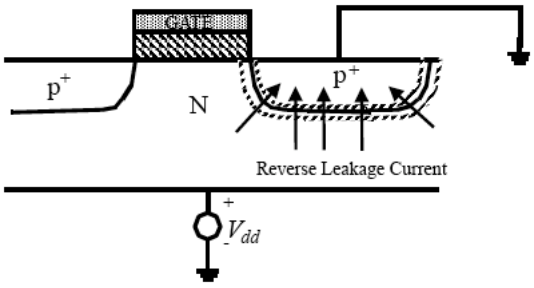
负载大，短路电流相对放电电流比较小

负载小，短路电流造成瞬时电流峰值



- Short circuit current usually well controlled

Diode Leakage



$$I_{DL} = J_S \times A$$

漏电电流

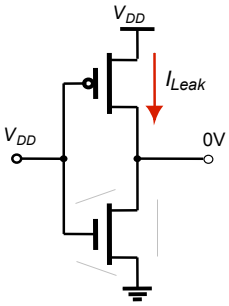
JS = 10-100 pA/µm2 at 25 deg C for 0.25µm CMOS

JS doubles for every 9 deg C!

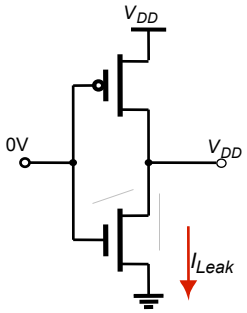
Much smaller than transistor leakage in deep submicron

Transistor Leakage

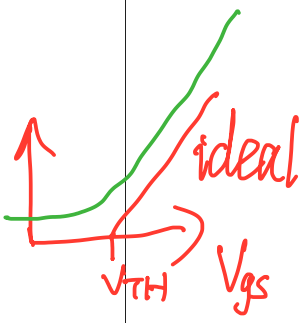
- Transistors that are supposed to be off - leak



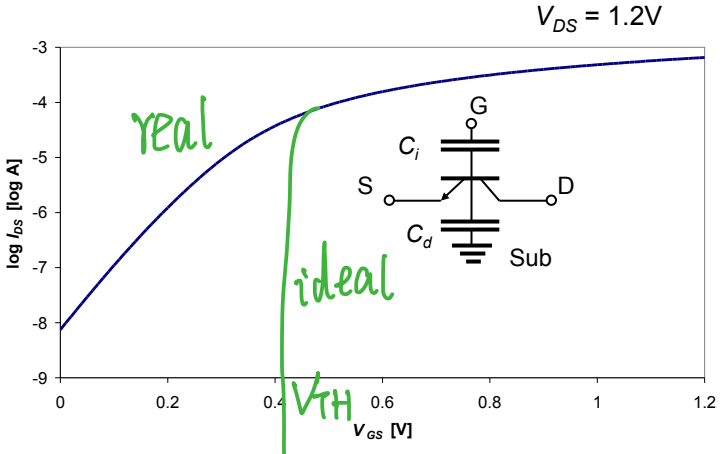
Input at V_{DD}



Input at 0

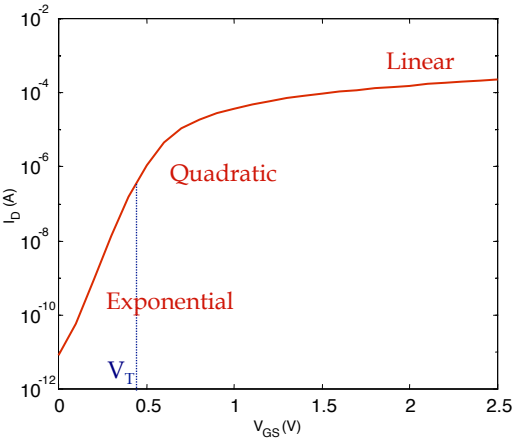


Transistor Leakage



Drain leakage current is exponential with V_{GS}-V_T

Sub-Threshold Conduction



Subthreshold Slope:

$$I_D \sim I_0 e^{\frac{q(V_{GS}-V_T)}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

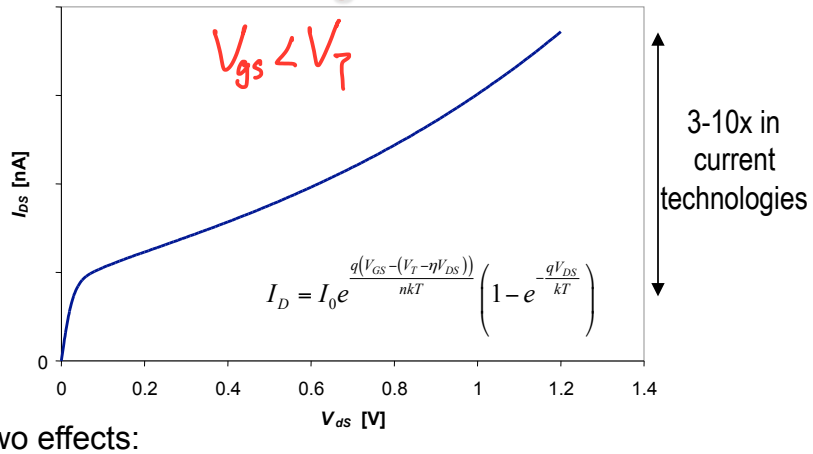
$$I_D \sim I_0 10^{\frac{(V_{GS}-V_T)}{S}}$$

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$ ideal n=1

S is ΔV_{GS} for I_{D2}/I_{D1} =10

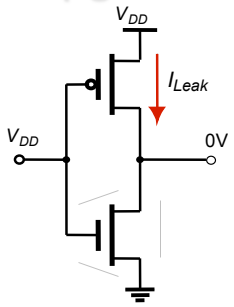
Typical values for S:
60 .. 100 mV/decade

Transistor Leakage

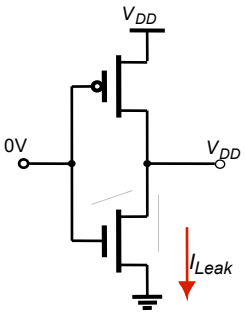


Two effects:
- diffusion current (like a bipolar transistor)
- exponential increase with V_{DS} (η: DIBL)

Roff (ignoring DIBL)



Input at V_{DD}

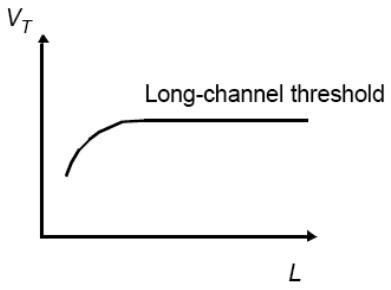


Input at 0

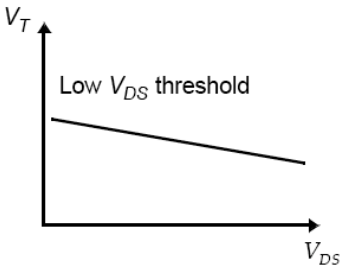
$$I_{Leak} \sim I_0 e^{\frac{-V_T}{nkT/q}}$$

$$R_{off} = \left(V_{DD} / I_0\right) e^{\frac{V_T}{nkT/q}}$$

Threshold Variations

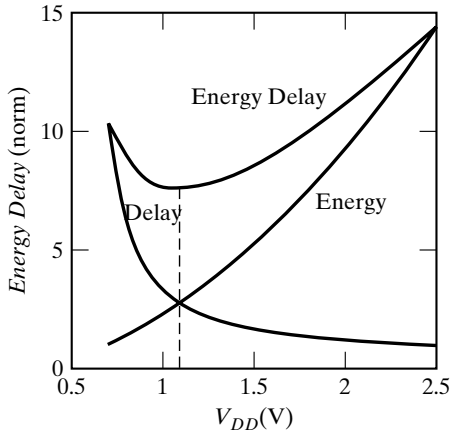


Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (DIBL) (for short L)

Trading off energy and delay



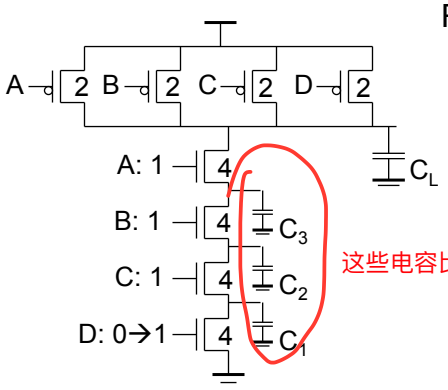
CMOS Logic Revisited

Analyzing and Optimizing Complex CMOS Gates

- Techniques very similar to the inverter case
- Logical Effort technique as the means for gate sizing and topology optimization
- However … some other things to be aware of!

Fan-In Considerations

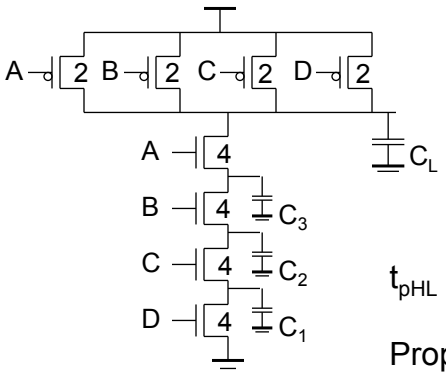
RC model:

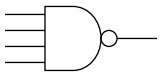


这些电容比较小，以前的分析中是忽略掉的。但这里不行。

Fan-In Considerations

lump model 会overestimate延迟



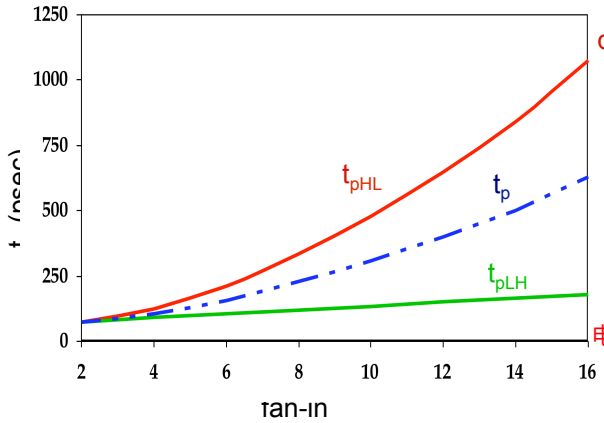


Distributed RC model
(Elmore delay)

$$t_{pHL} = 0.69\, R_{eqn}(C_1+2C_2+3C_3+4C_L)$$

Propagation delay deteriorates rapidly as a function of fan-in – quadratically in the worst case.

t_p as a Function of Fan-In

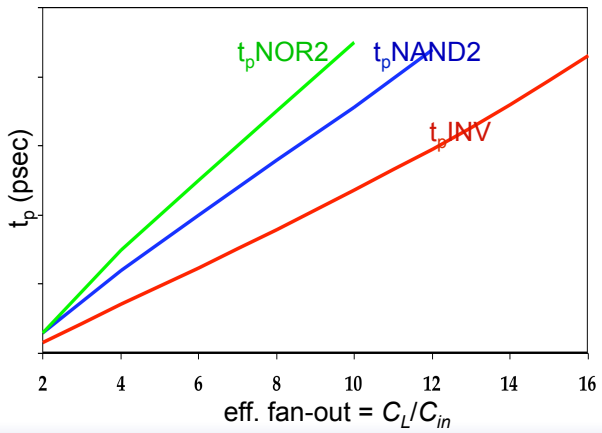


quadratic PMOS串行，电阻电容都增加

Gates with a fan-in greater than 4 should be avoided.

linear
电阻固定，只有电容增加，因为NOMS并行。

t_p as a Function of Fan-Out



All gates have the same drive current.

Slope is a function of "driving strength"

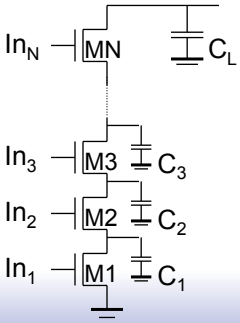
t_p as a Function of Fan-In and Fan-Out

- Fan-in: quadratic due to increasing resistance and capacitance
- Fan-out: each additional fan-out gate adds two gate capacitances to C_L

$$t_p = a_1 FI + a_2 FI^2 + a_3 FO$$

Fast Complex Gates: Design Technique 1

- Transistor sizing
  - as long as fan-out capacitance dominates
- Progressive sizing



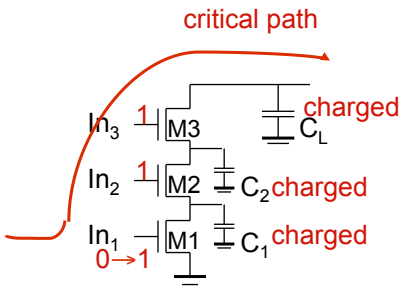
Distributed RC line

M1 > M2 > M3 > … > MN
(the FET closest to the output is the smallest)

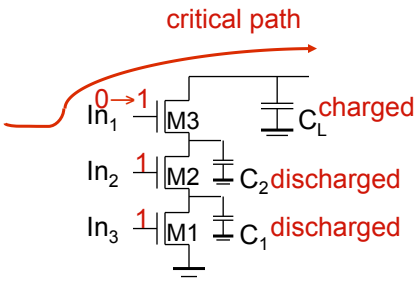
Can reduce delay by more than 20%;
Be careful: input loading, junction caps, decreasing gains as technology shrinks

Fast Complex Gates: Design Technique 2

- Transistor ordering



delay determined by time to discharge C_L, C_1 and C_2

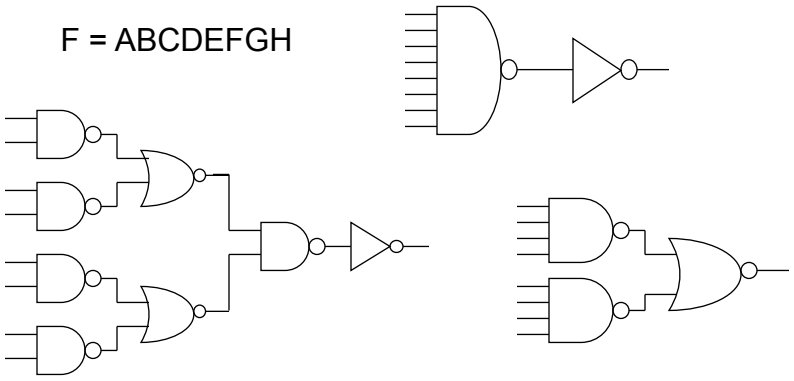


delay determined by time to discharge C_L

Fast Complex Gates: Design Technique 3

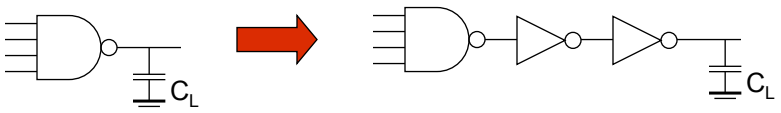
- Alternate logic structures

F = ABCDEFGH



Fast Complex Gates: Design Technique 4

- Isolating fan-in from fan-out using buffer insertion



Fast Complex Gates: Design Technique 5

- Reducing the voltage swing

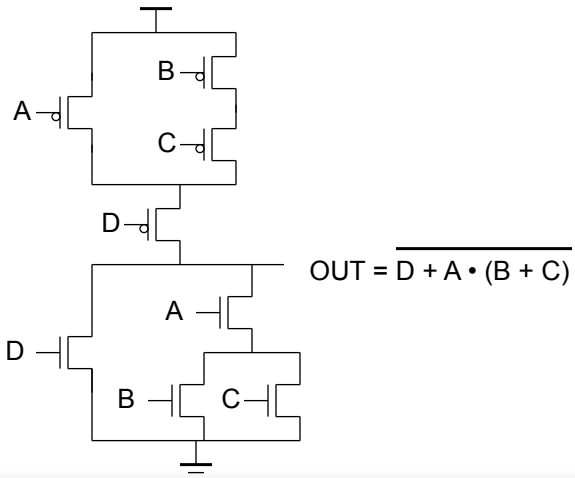
$$t_{pHL} = 0.5\,(C_L\,V_{DD}) / I_{DSATn}$$

$$= 0.5\,(C_L\,V_{swing}) / I_{DSATn}$$

  - linear reduction in delay
  - also reduces power consumption
- But the following gate is slower!
- Or requires use of "sense amplifiers" on the receiving end to restore the signal level (memory design)

CMOS Layout

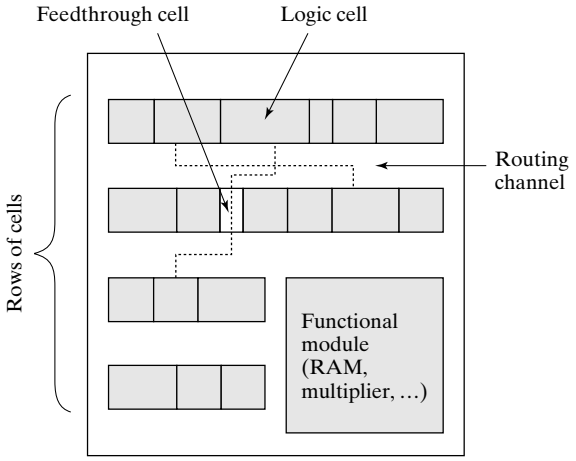
Complex CMOS Gate



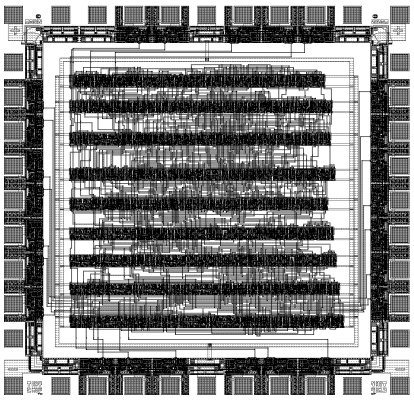
Cell Design

- Standard Cells
  - General purpose logic
  - Used to synthesize RTL/HDL
  - Same height, varying width
- Datapath Cells
  - For regular, structured designs (arithmetic)
  - Includes some wiring in the cell

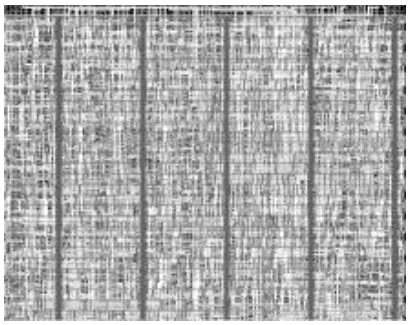
Standard Cell Methodology



Standard Cells – Then and Now

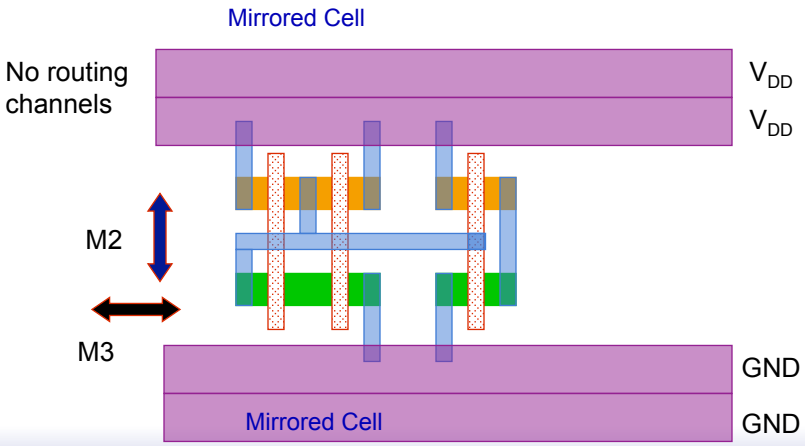


(a)

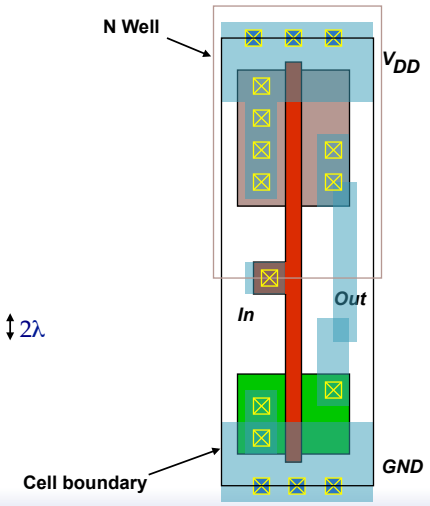


(b)

Standard Cell Layout Methodology – 1990s - Today



Standard Cells



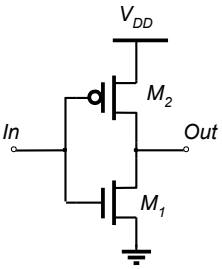
Cell height 12 metal tracks
Metal track is approx. 3λ + 3λ
Pitch =
repetitive distance between objects

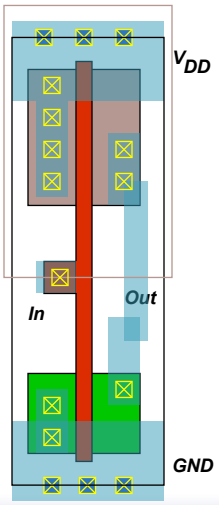
Cell height is "12 Mn pitch"

Rails ~10λ

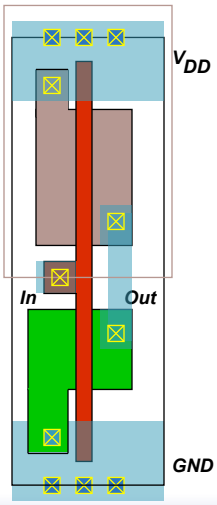
Standard Cells

With minimal diffusion routing

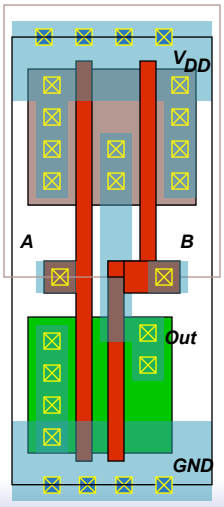




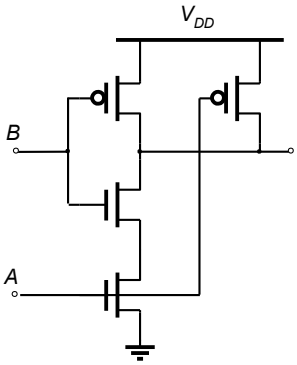
With silicided diffusion



Standard Cells



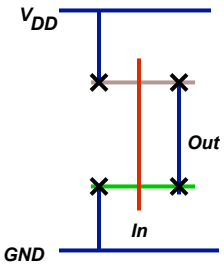
2-input NAND gate



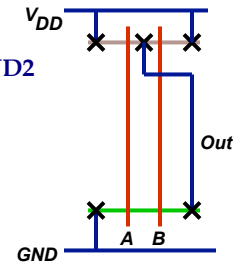
Stick Diagrams

Contains no dimensions
Represents relative positions of transistors

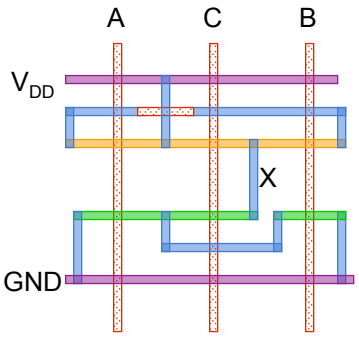
Inverter

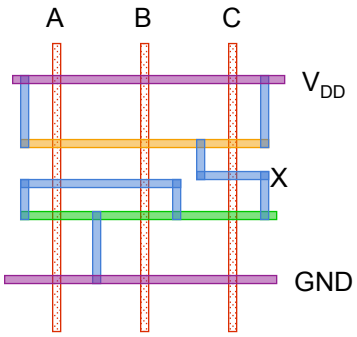


NAND2

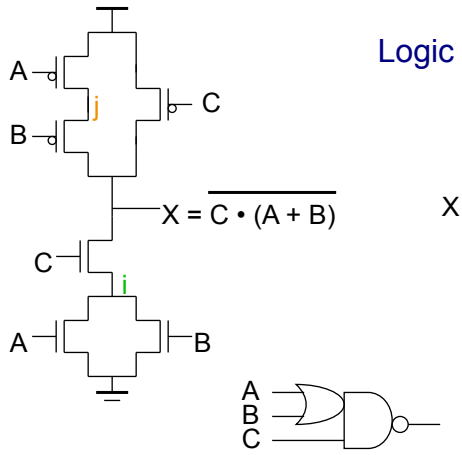


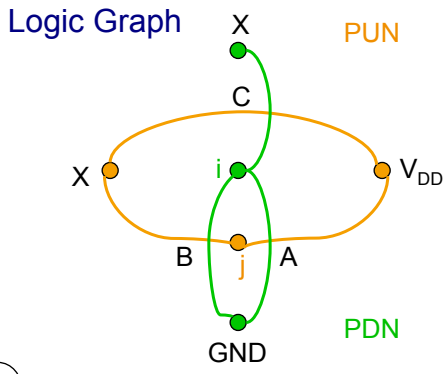
Two Versions of $\overline{C \cdot (A + B)}$





Logic Graphs





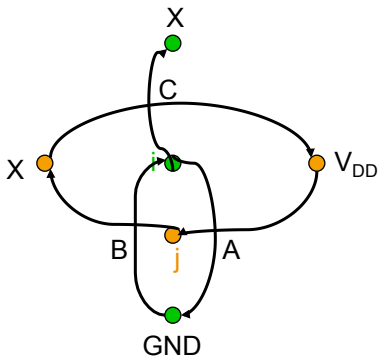
Consistent Euler Path

A B C

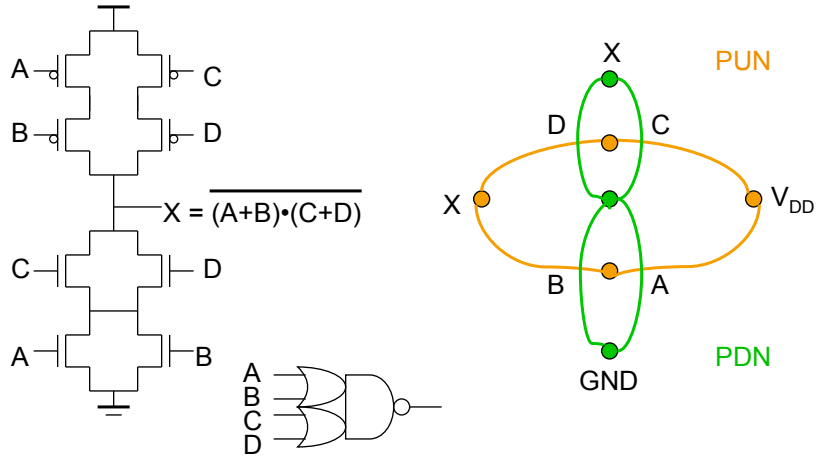
Has PDN and PUN

B C A

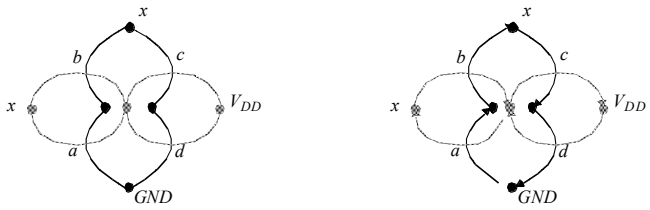
Has PUN, but no PDN



OAI22 Logic Graph

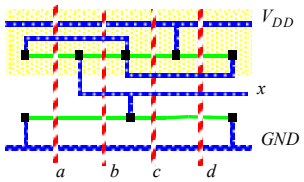


Example: x = ab+cd



(a) Logic graphs for $\overline{(ab+cd)}$

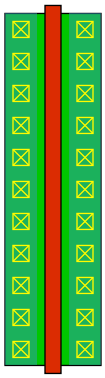
(b) Euler Paths {*a b c d*}



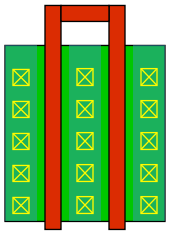
(c) stick diagram for ordering {a *b c d*}

Multi-Fingered Transistors

One finger



Two fingers (folded)



Less diffusion capacitance