EE141-Spring 2012 Digital Integrated Circuits

Lecture 17
Pass-Transistor Logic
Ratioed Logic

Guest Lecturer:
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Administrativia

- Project phase 1 due today!
- Midterm on Friday in 250 SDH – normal time.

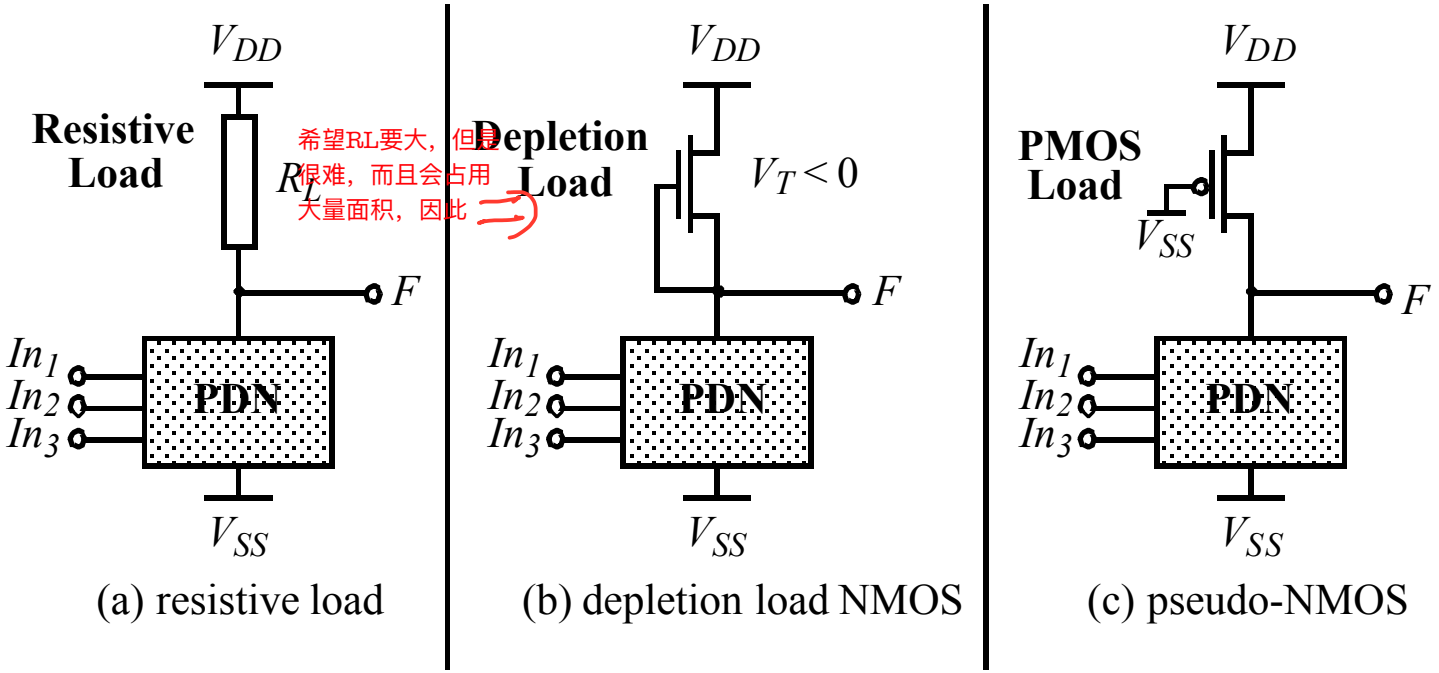
Class Material

- Last lecture
  - Complex logic
- Today's lecture
  - Pass transistor logic
  - Ratioed Logic
  - Intro to dynamic
- Reading (Ch 6)

Ratioed Logic

Ratioed Logic

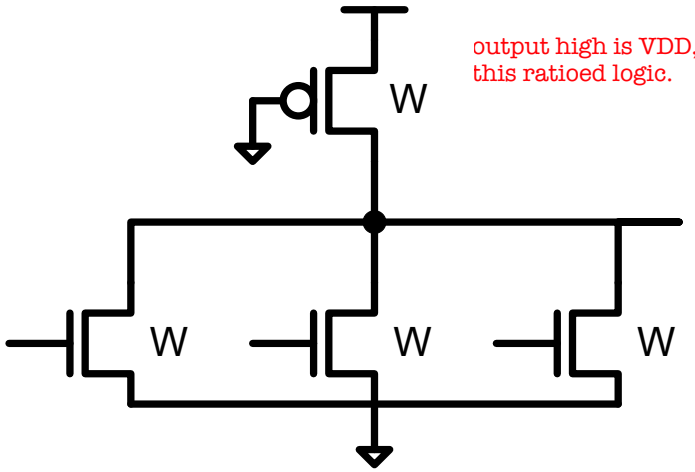
因为LE与输入电容有关，输入电容由于PMOS和NMOS的有关，而PMOS提供的电容比NMOS大，因此我们想要构建的电路更快，我们可以想办法删除PMOS。



Goal: build gates faster/smaller than static complementary CMOS

Ratioed Logic

- Spend power for speed
  - Use NOR gates, not NAND gates 避免串联，降低LE



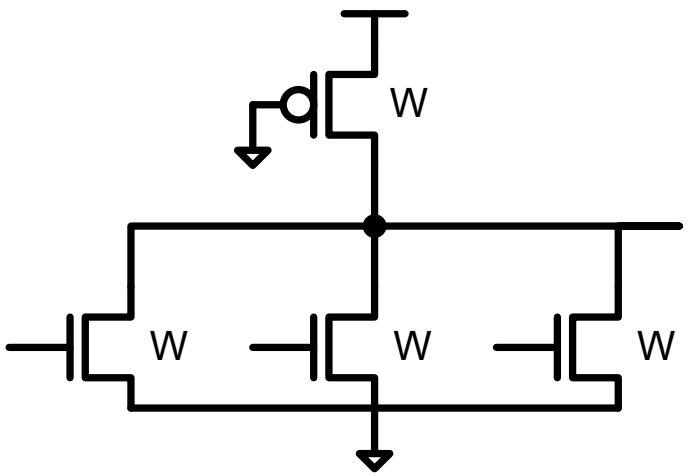
output high is VDD, but output low depended on PMOS to NMOS ratio. So we call this ratioed logic.

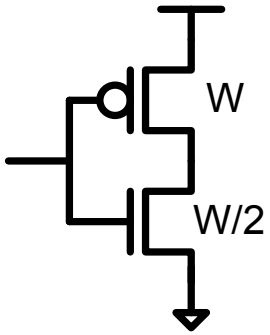
- DC characteristics:
  - V_{OH} = VDD
  - V_{OL} depends on PMOS to NMOS ratio

Ratioed Logic LE

$LE = \frac{R_g C_g}{R_{inv} C_{inv}}$

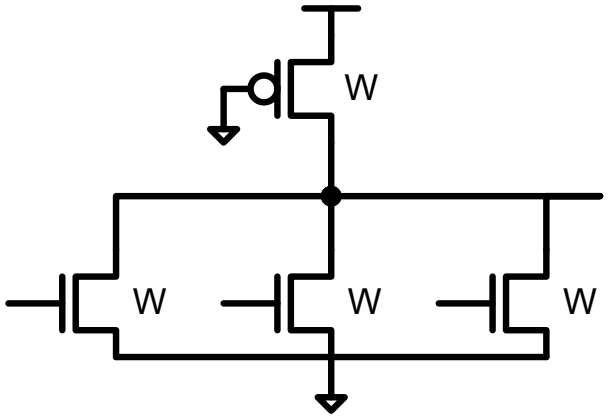
- Rising and falling delays aren't the same
  - Calculate LE for the two edges separately

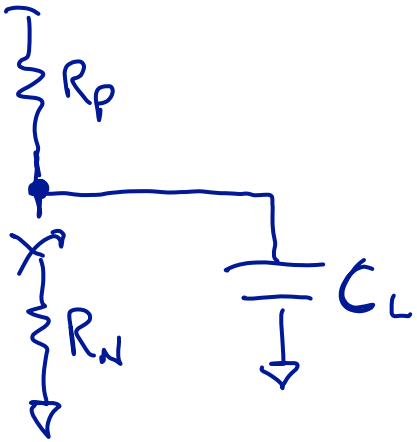




- For tpLH:
  - $C_{gate} = WC_G$ $C_{inv} = (3/2)WC_G$ $LE_{LH} =$

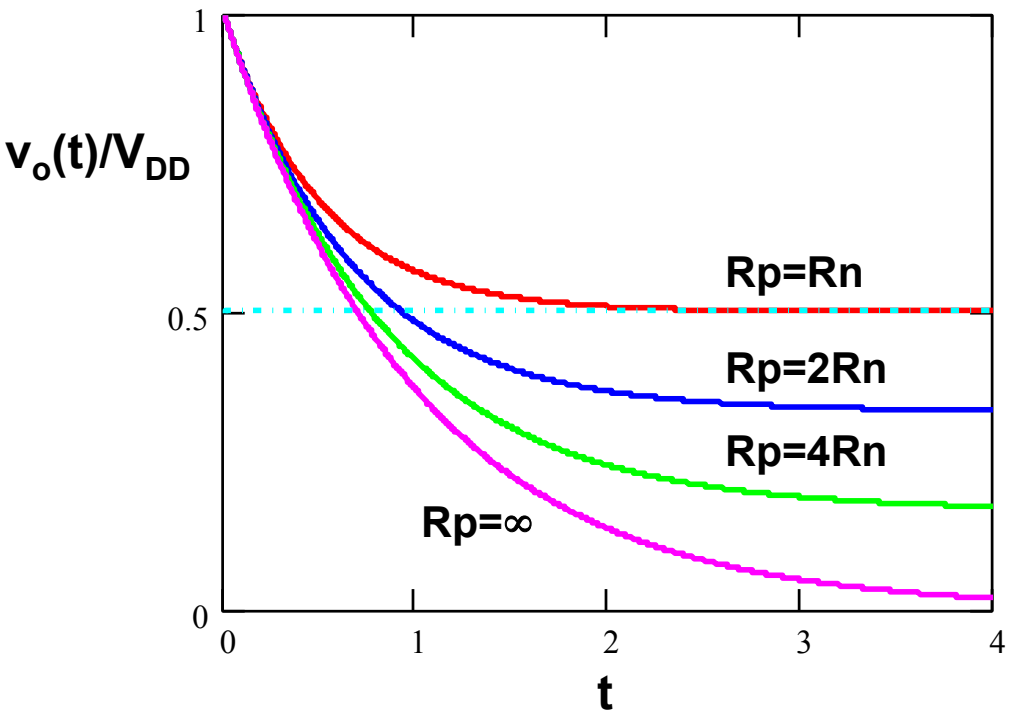
Ratioed Logic LE (pull-down edge)

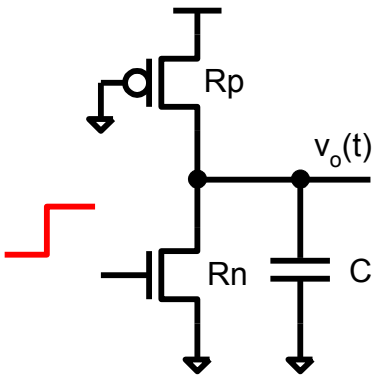




- What is LE for t_{pHL}?
- Switch model would predict $R_{eff} = R_n || R_p$
  - Would that give the right answer for LE?

Response on Falling Edge





$$\tau = \frac{Rn \cdot Rp}{Rn + Rp} \cdot C$$

$$\frac{v_o(t)}{V_{DD}} = \frac{Rn}{Rn + Rp} + \left(1 - \frac{Rn}{Rn + Rp}\right) e^{-t/\tau}$$

- Time constant is smaller, but it takes more time to complete 50% V_{DD} transient (arguably)
  - Rp actually takes some current away from discharging C

Ratioed Logic Pull-down Delay

- Think in terms of the current driving C_{load}

  电阻越大电流越小，驱动负载越慢

- When you have a conflict between currents
  - Available current is the difference between the two
  - In pseudo-nMOS case:

$$R_{drive} = \frac{1}{1/Rn - 1/Rp} \longrightarrow R_{drive} = \frac{Rn}{1 - \left(Rn/Rp\right)}$$

  - (Works because Rp >> Rn for good noise margin)

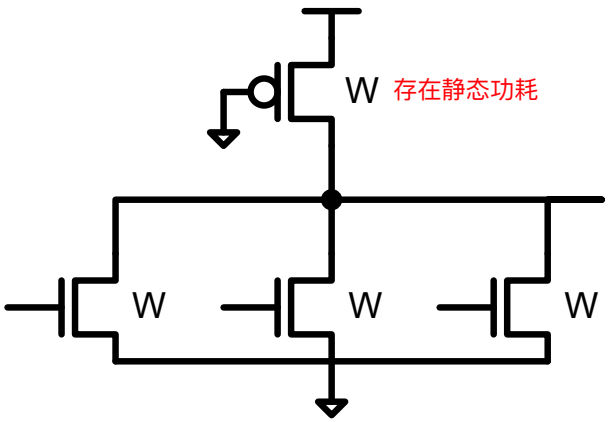
$I_N \sim \frac{V_{DD}}{R_N}$

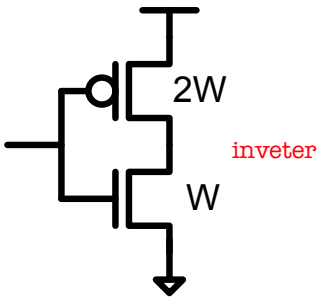
$I_p \sim \frac{V_{DD}}{R_p}$

$I = I_N - I_p$

$\frac{V_{DD}}{R_{eff}} = \frac{V_{DD}}{R_N} - \frac{V_{DD}}{R_p}$

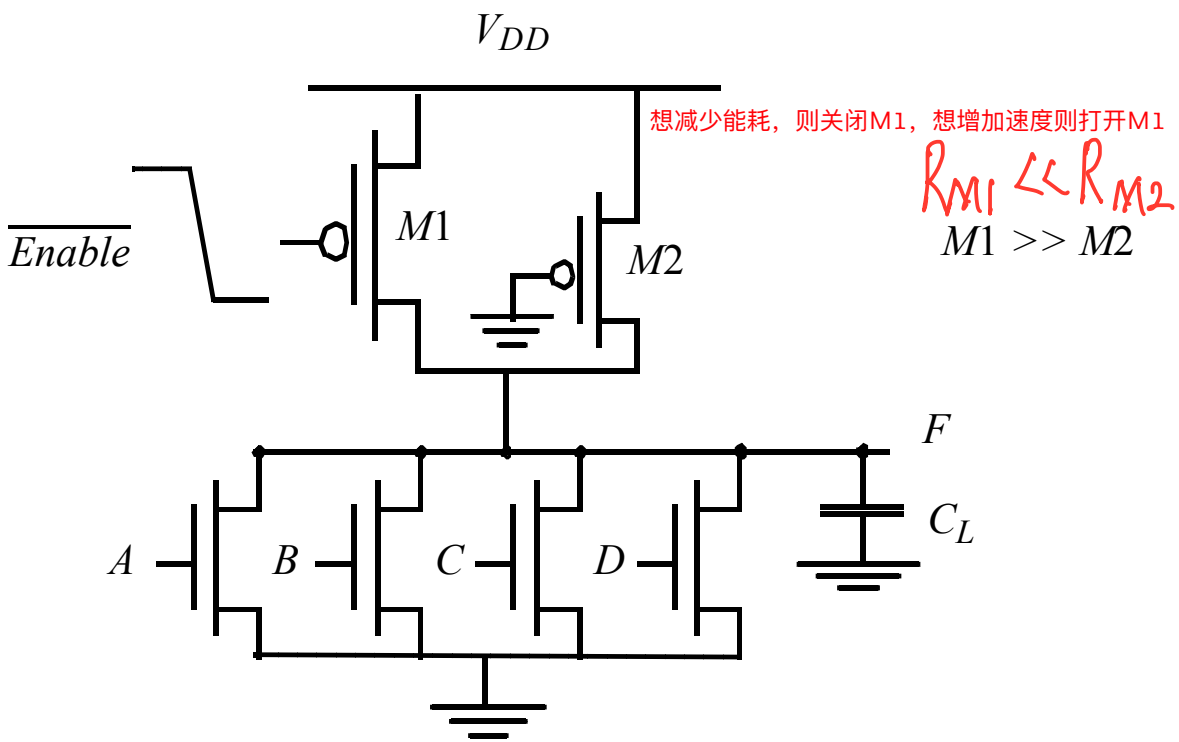
Ratioed Logic LE (pull-down edge)





- For t_{pHL} (assuming $R_{sqp} = 2R_{sqn}$):
  - $R_{gate} = R_n/(1\text{-}Rn/Rp) = 2Rn$ $\quad R_{inv} = R_n$
  - $C_{gate} = WC_G$ $\quad C_{inv} = 3WC_G$
  - $LE_{HL} = 2/3$
- LE is lower than an inverter!
  - But have static power dissipation…

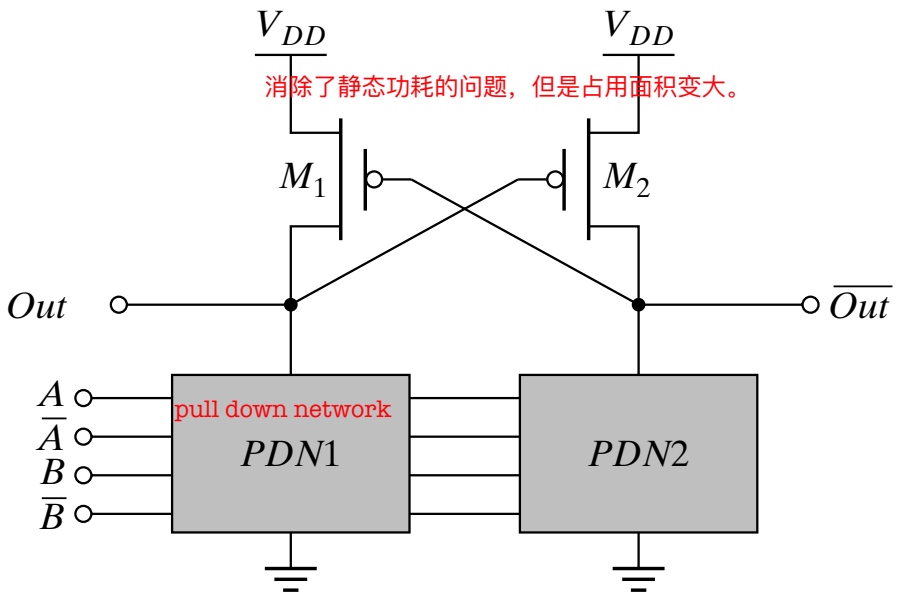
Improved Loads



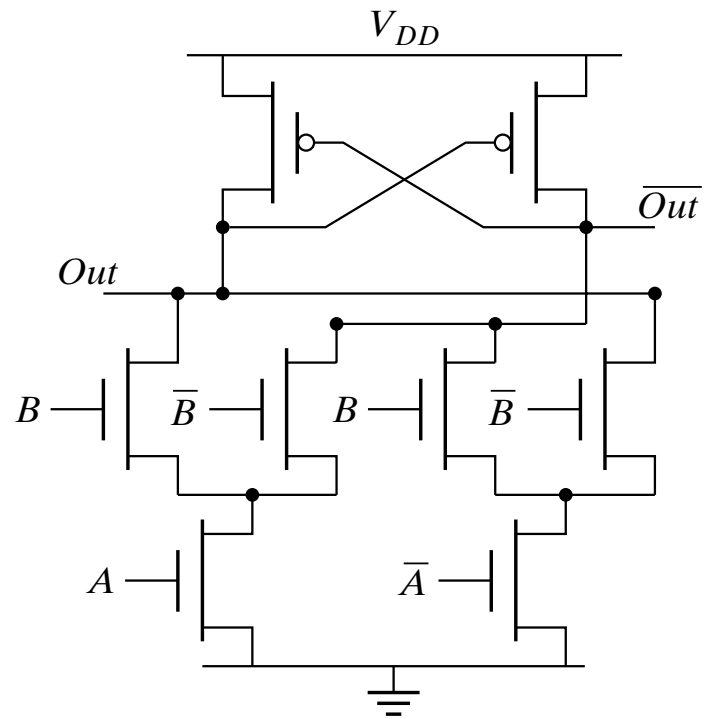
Adaptive Load

Improved Loads (2)

idea：一个电路实现真值表，另一个电路实现真值表的补集。



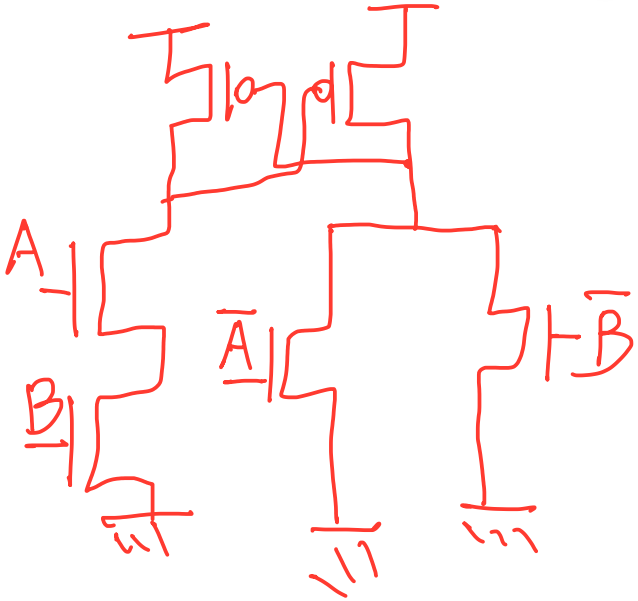
(a) Basic principle



(b) XOR–XNOR gate

Differential Cascode Voltage Switch Logic (DCVSL)

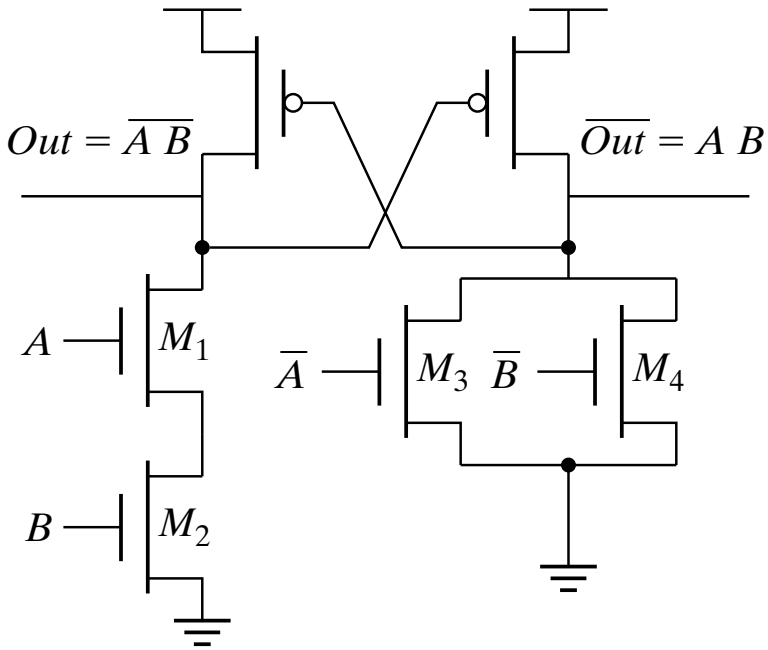
DCVSL Example1: AND

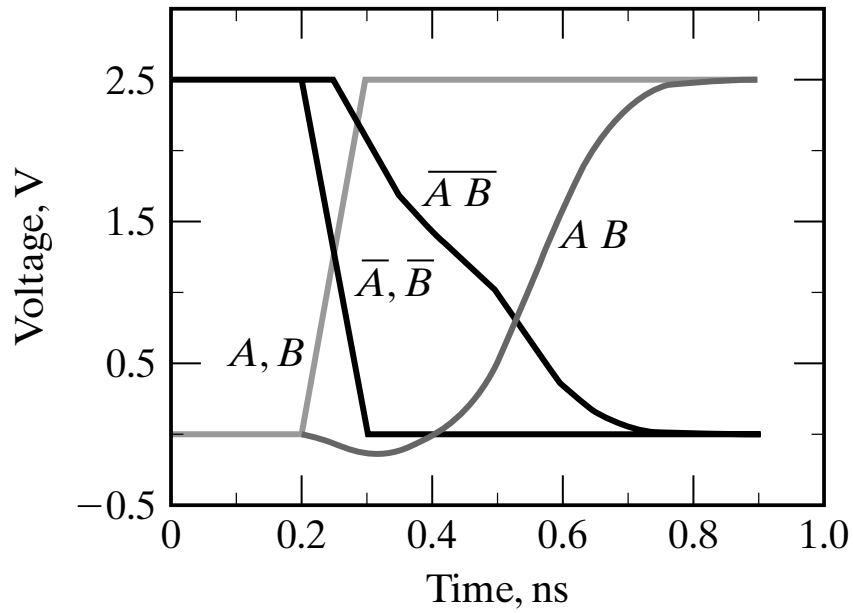


$Out = AB = \overline{\overline{A} + \overline{B}}$

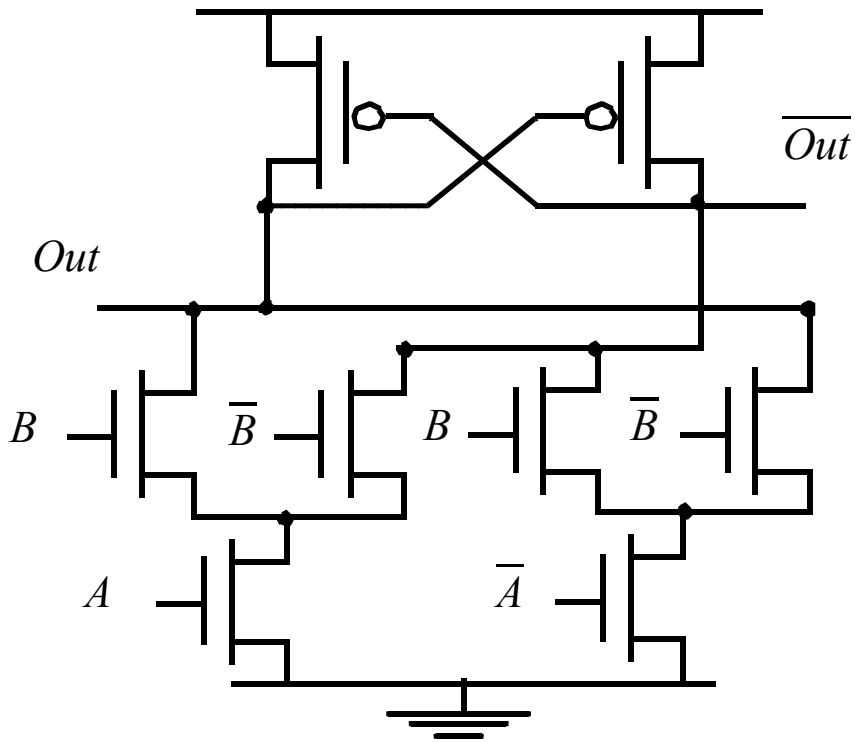
$\overline{Out} = \overline{AB}$

DCVSL Transient Response





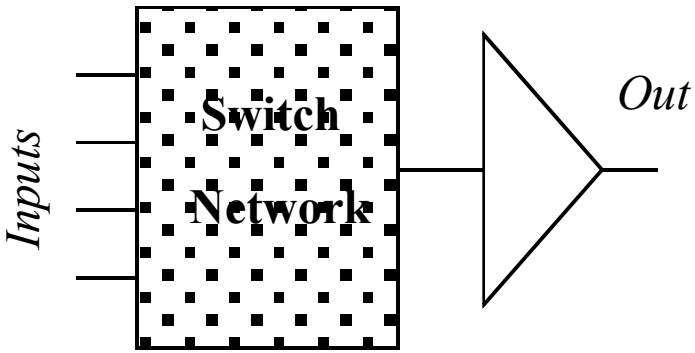
DCVSL Example2

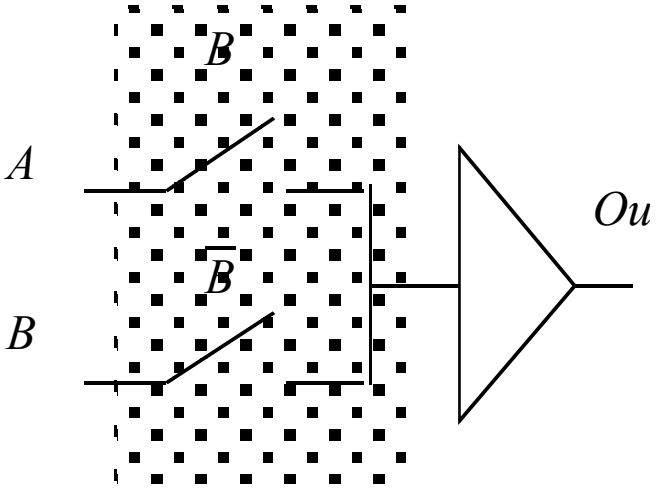


XOR/XNOR gate

Pass-Transistor Logic

Pass-Transistor Logic

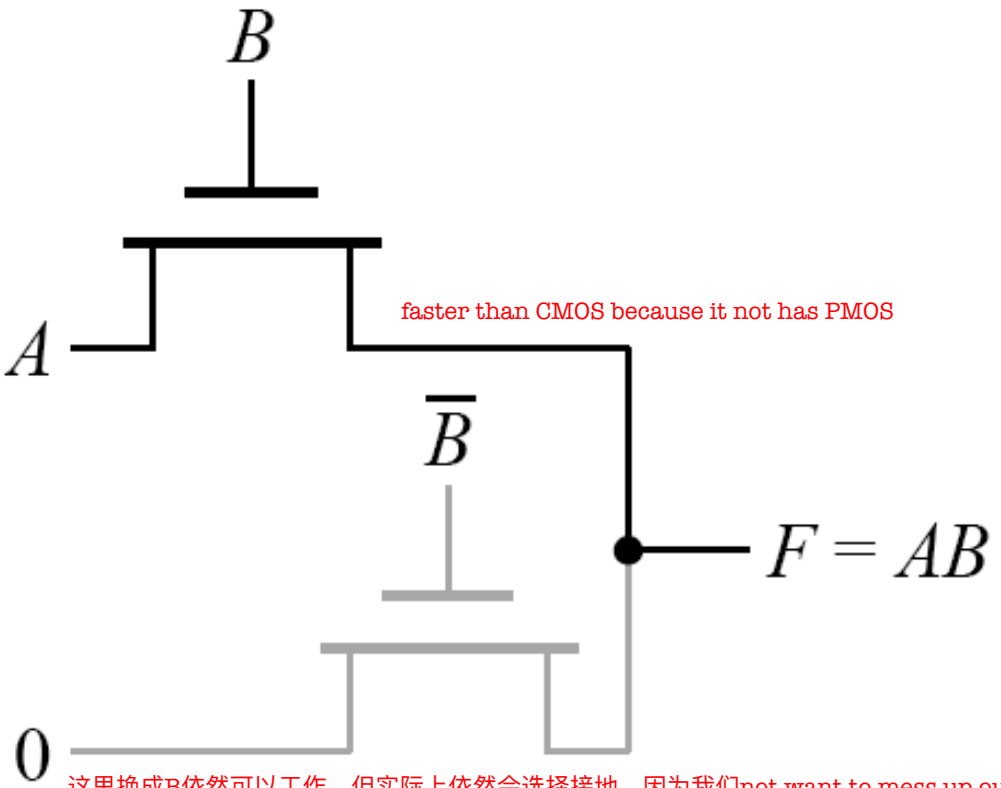




- N transistors
- No static consumption

Example: AND Gate

B	A	Out
1	1	1
1	0	0
0	x	

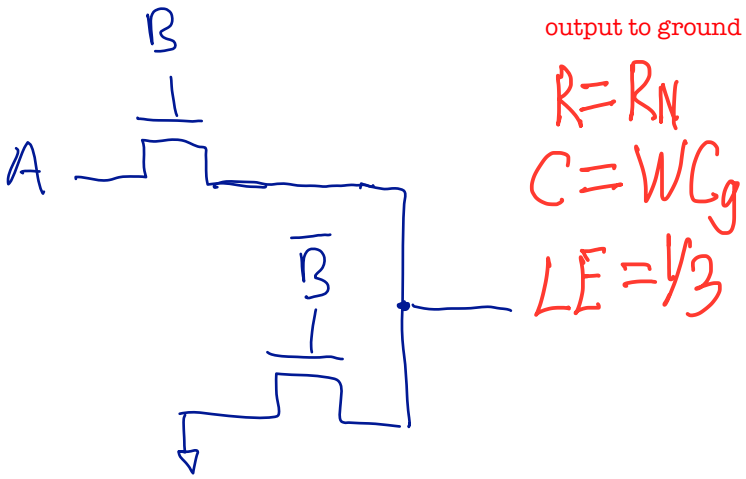


faster than CMOS because it not has PMOS

这里换成B依然可以工作，但实际上依然会选择接地，因为我们not want to mess up our critical paths and as if we have a chance to eliminate a capacitance and resistance on the path because something will be driving this simple B and we don't want to increase the fan out of that input.

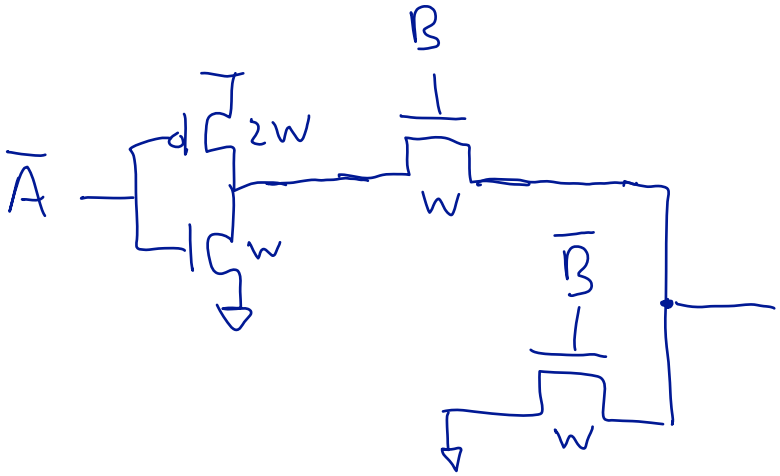
Pass Transistor Logic LE

- What is LE of "gate" shown below for A and B inputs?
  - Hint: Can you answer this question with only the information shown below?



Pass Transistor Logic LE

- In CMOS, a "gate" is defined only when trace a connection all the way back to a supply
  - Otherwise don't know what drive resistance really is

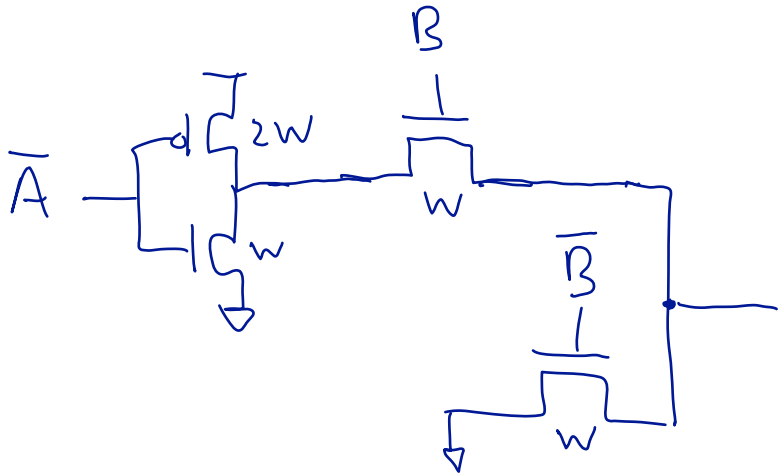


$C_{gate\bar{A}} = 3WC_g$

$R_{gate\bar{A}} = 2R_N$

$LE_{\bar{A}} = 2$

Pass Transistor Logic LE



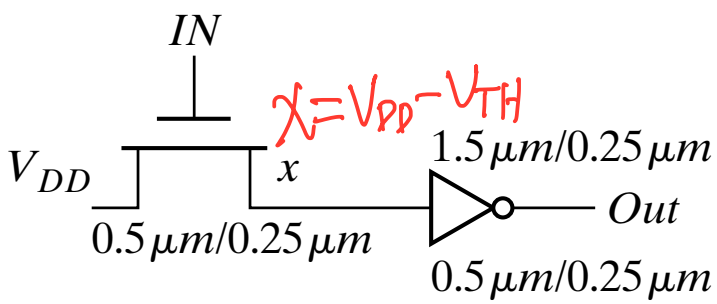
$C_{gate\,B} = WC_g$

$R_{gate\,B} = 2R_N$

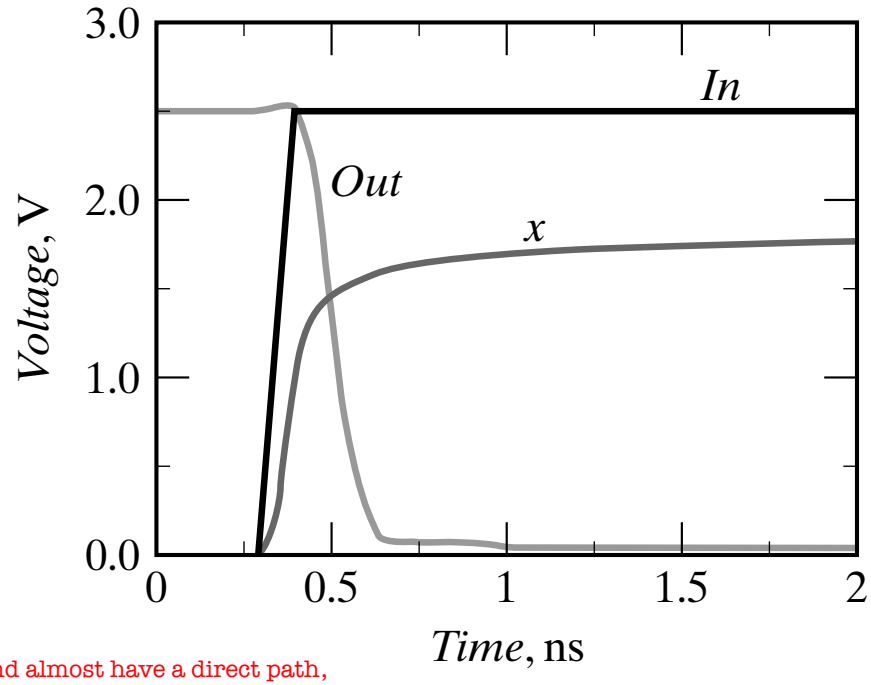
$LE_B = 2/3$

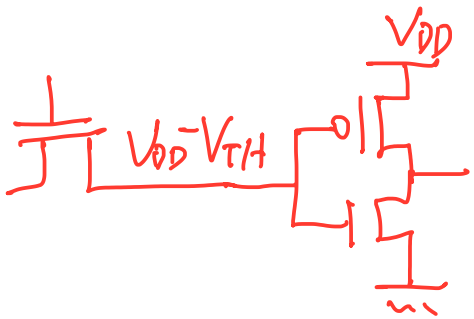
因此如果你有一个输入，我们更乐意连接到B而不是A

NMOS-Only Logic



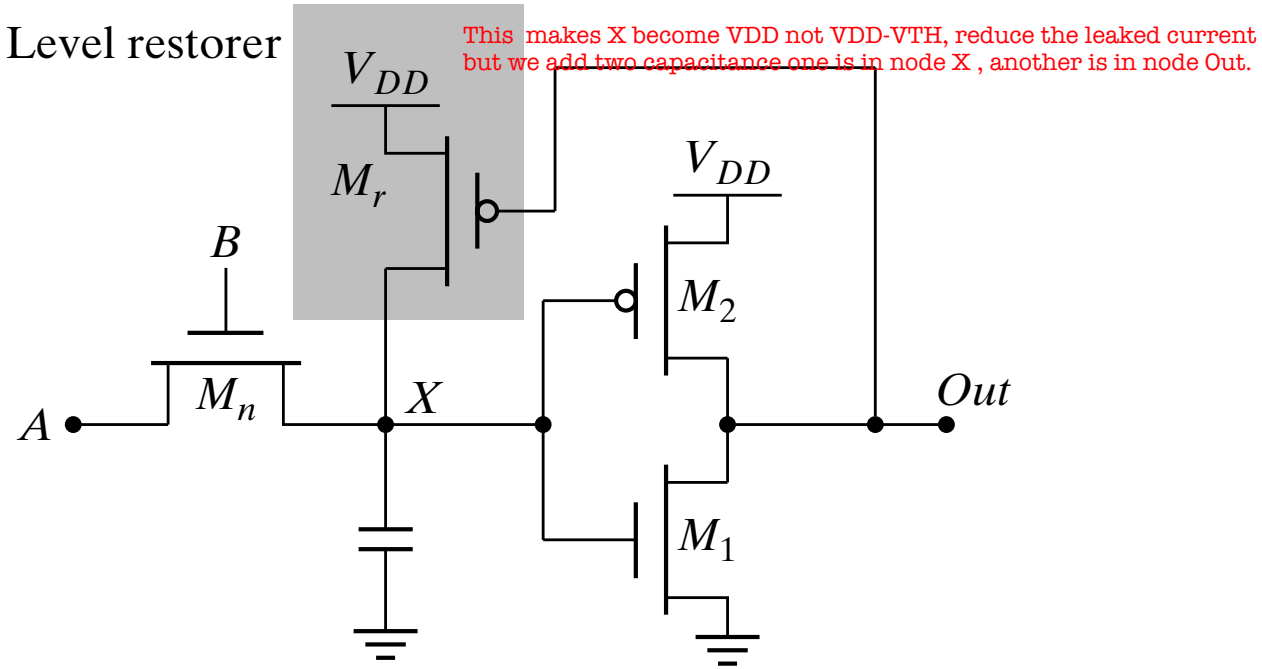
In terms of function, it has no problem.





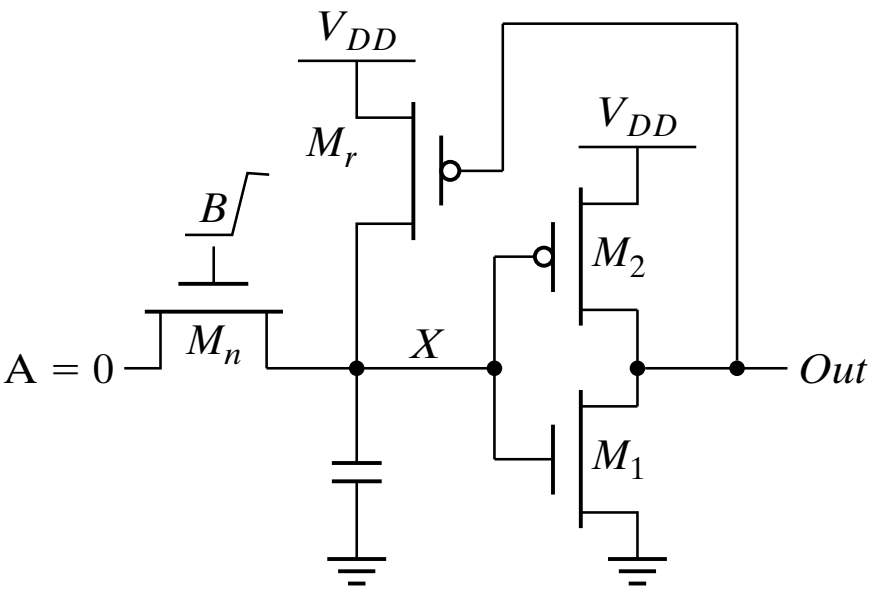
exist static power and almost have a direct path, leaked current,so the speed will be slower

NMOS Only Logic: Level Restoring Transistor



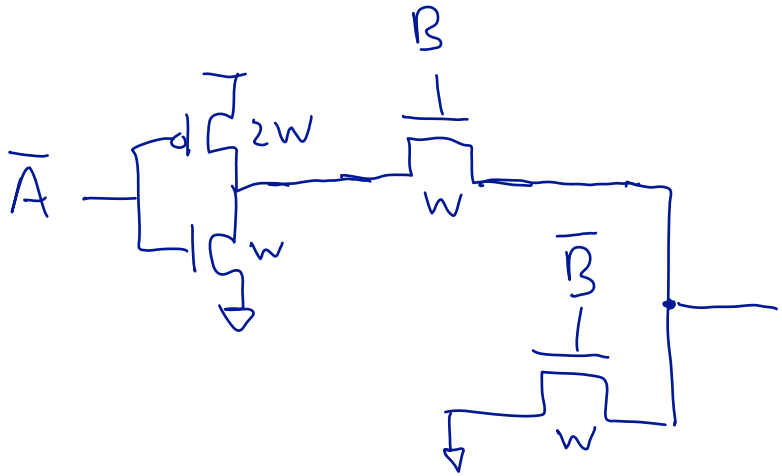
- Advantage: Full Swing
- Restorer adds capacitance, takes away pull down current at X
- Ratio problem like ratio logic

Restorer Sizing



- Upper limit on restorer size
- Pass-transistor pull-down can have several transistors in stack

Pass Transistor Logic LE

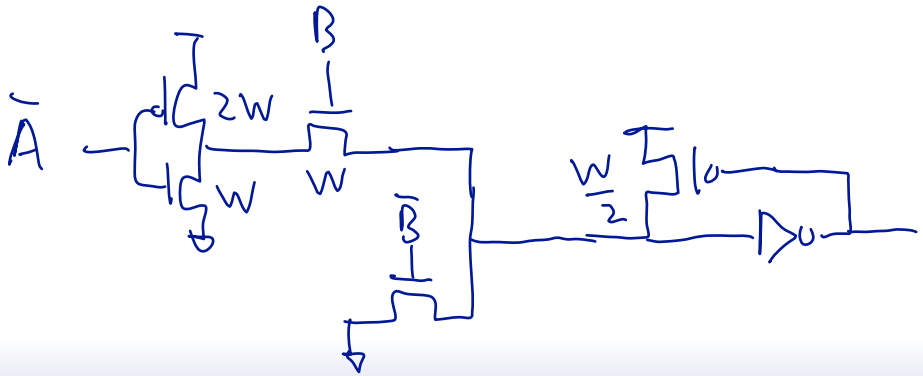


$C_{gate\,B} = WC_g$

$R_{gate\,B} = 2R_N$

$LE_B = 2/3$

With level restore:

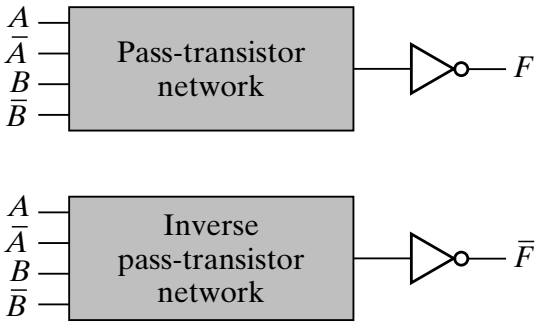


$R_\phi = 4R_N$

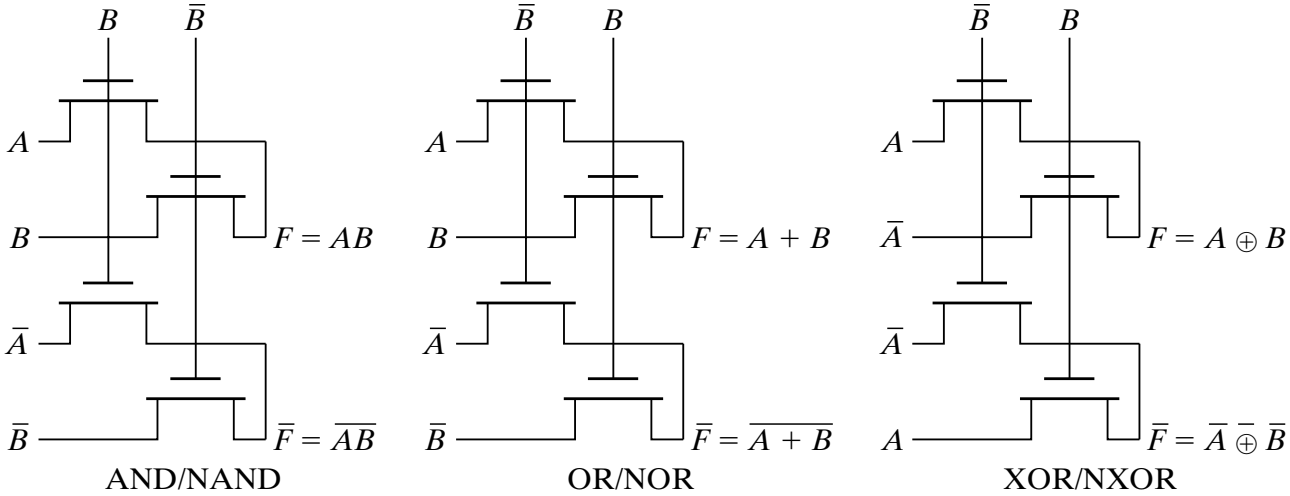
$R_{gate\,B} = 4R_N$

$LE_B = \frac{4}{3}$

Complementary Pass Transistor Logic

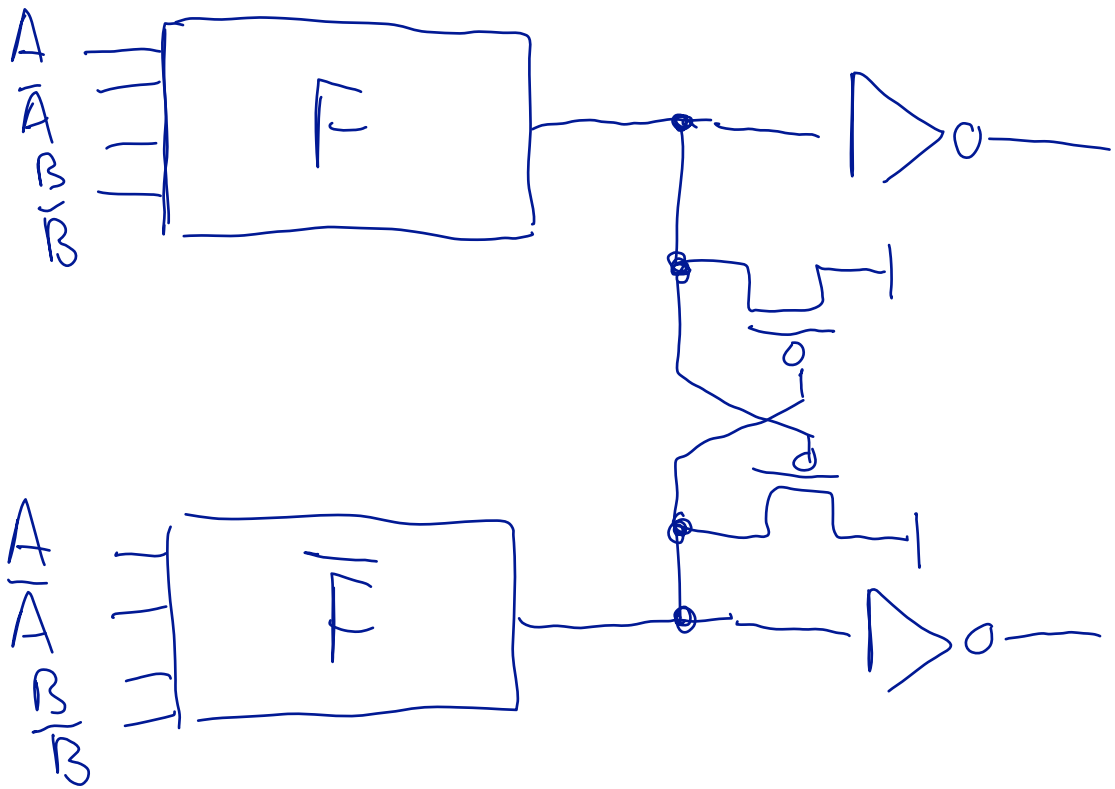


(a) Basic concept



(b) Example pass-transistor networks

CPL Level Restore



Solution 2: Transmission Gate

Resistance of Transmission Gate

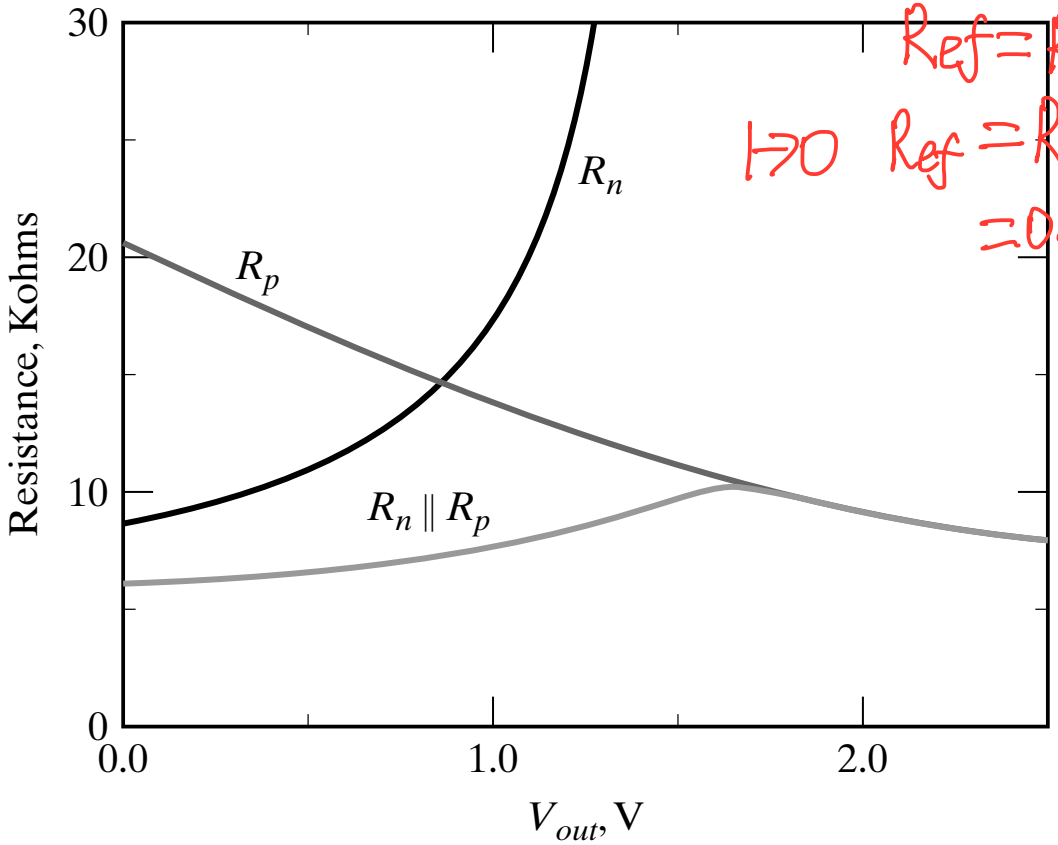
$0 \to 1$ $R_{eq} = R_p // 2R_N$

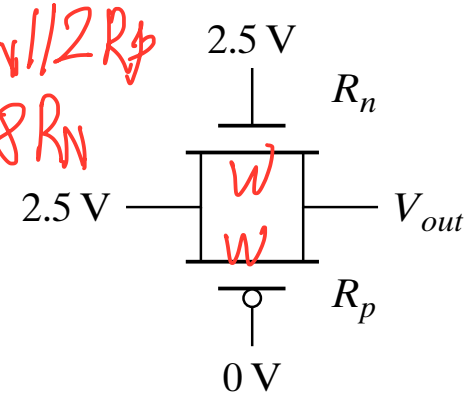
$\Downarrow$ $R_p = 2R_N$

$R_{eq} = R_N$

$1 \to 0$ $R_{eq} = R_N // 2R_p$

$= 0.8 R_N$



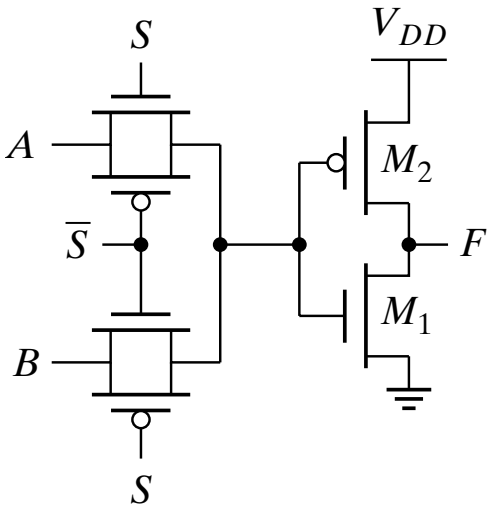


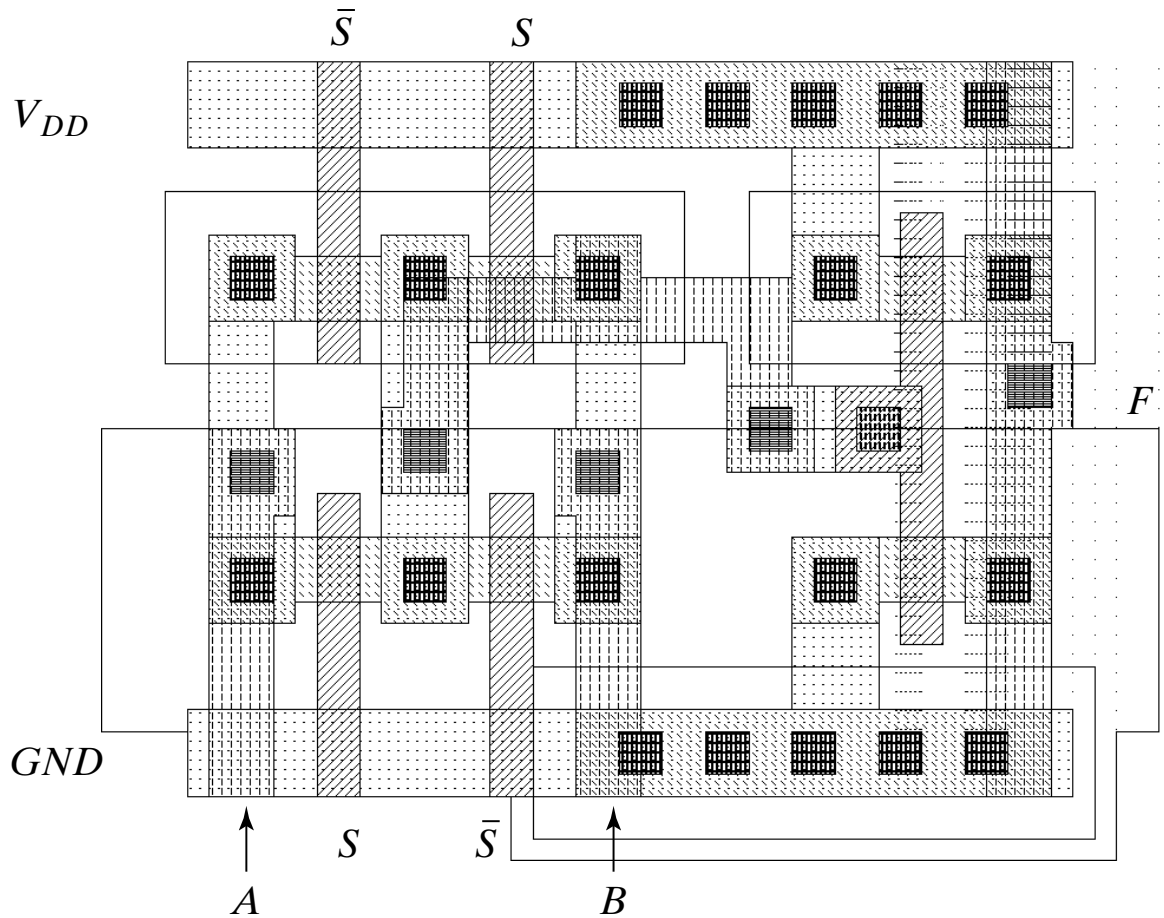
$R_{N\,PU} = 2R_{N\,PD}$

$R_{p\,PD} = 2R_{p\,PU}$

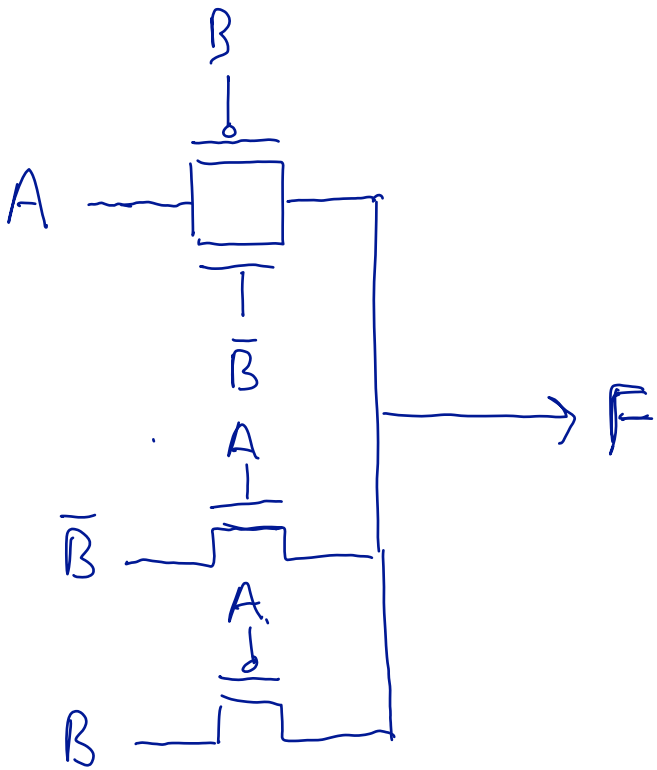
Pass-Transistor Based Multiplexer

Smaller then CMOS,if we use CMOS, we have to use eight transistors, but now we only use six transistors.





Transmission Gate XOR



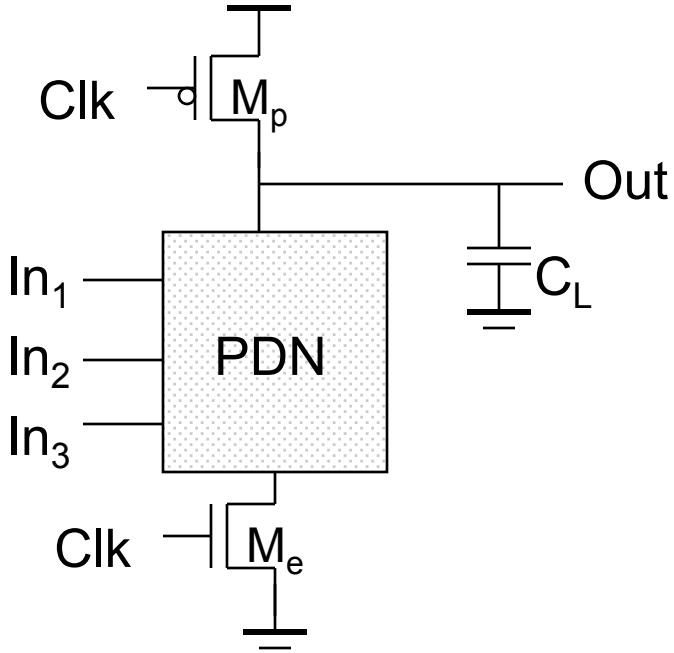
Dynamic Logic

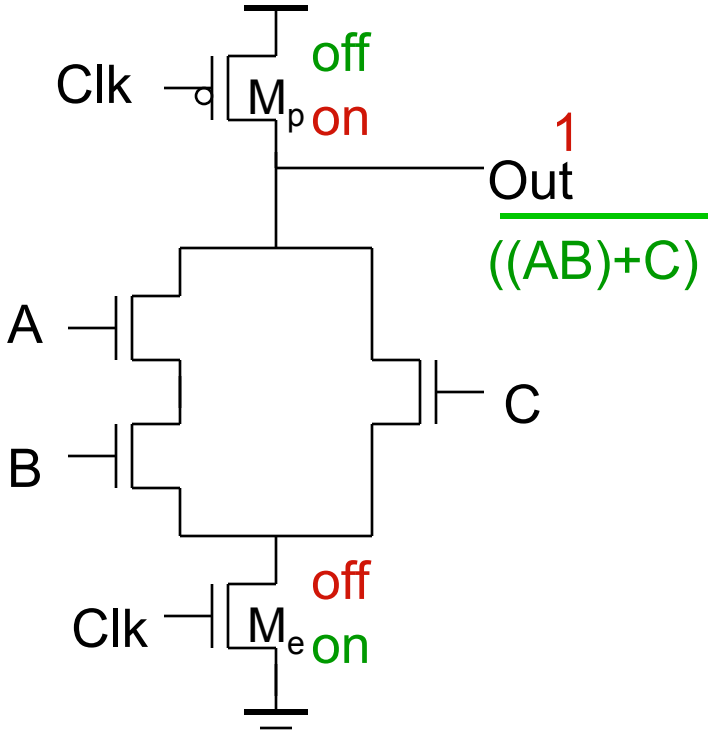
Dynamic CMOS

- In static circuits, at every point in time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.
  - fan-in of *n* requires 2*n* (*n* N-type + *n* P-type) devices

- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - only requires *n* + 2 (*n*+1 N-type + 1 P-type) transistors

Dynamic Gate



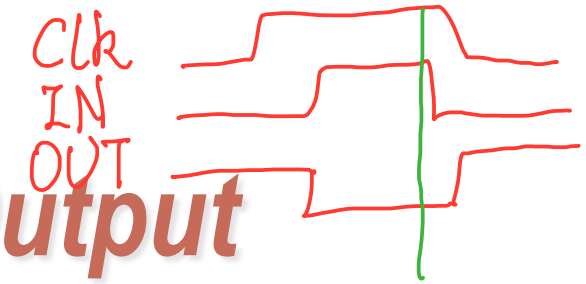


Two phase operation

Precharge (Clk = 0)

Evaluate (Clk = 1)

dynamic inverter



Conditions on Output

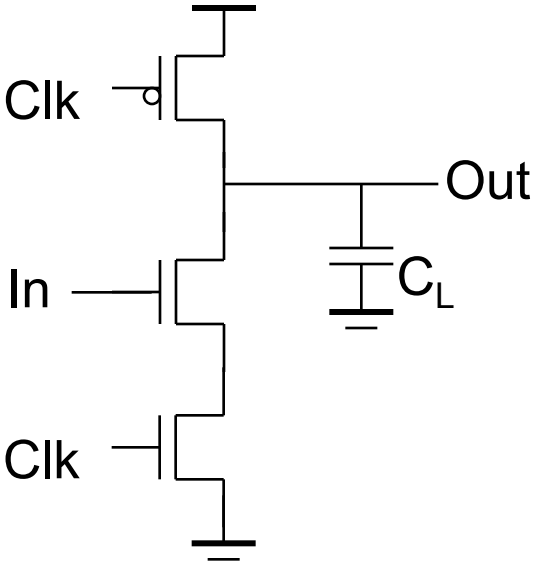
- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on C_L

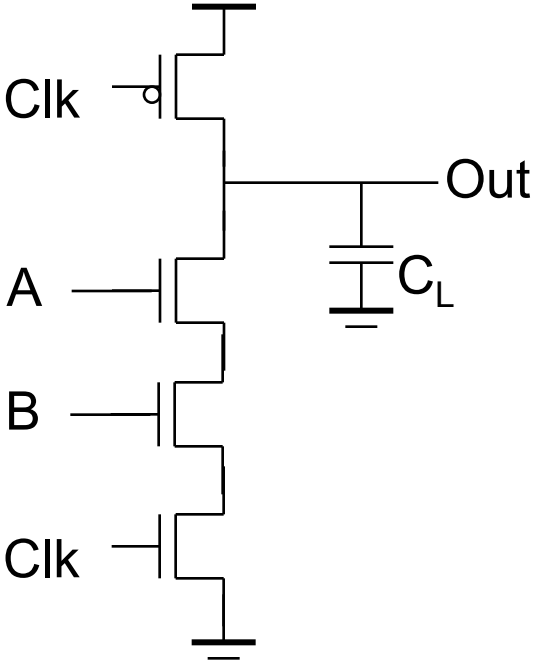
Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  - number of transistors is N + 2 (versus 2N for static complementary CMOS)
- Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})
- Non-ratioed - sizing of the devices does not affect the logic levels
- Faster switching speeds
  - reduced capacitance due to lower input capacitance (C_{in})
  - no I_{sc}, so all the current provided by PDN goes into discharging C_L

also not have static power.

LE of Dynamic Gates





C_{gate} = $2WC_g$
LE = $2/3$

C_{gate} = $3WC_g$
LE = 1

Properties of Dynamic Gates

- Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between V_{DD} and GND (including P_{sc})
  - no glitching
  - higher transition probabilities
  - extra load on Clk
- PDN starts to work as soon as the input signals exceed V_{Tn}, so V_M, V_{IH} and V_{IL} equal to V_{Tn}
  - low noise margin (NM_L)
- Needs a precharge/evaluate clock extra consumption power

$P = \alpha_{0\to1} f V_{DD}^2 C_L$

$\alpha_{0\to1} = P(\phi) \cdot P(1)$ here, $P(1) = 1$

Dynamic Logic - Challenges