EE141-Spring 2012 Digital Integrated Circuits

Lecture 7
Wires

Administrativia

- Lab 3 on Monday and Th (the week after)
- Midterm on Fr Febr 17 9:00-11:30am
- Review Session: Thursday

Class Material

- Last lecture
  - Optimizing complex logic
- Todays Lecture
  - Wires
- Reading (Ch 6.2, 4.2-4.4)

Logical Effort

The gate more complex , p bigger ,the intrinsic delay of gate bigger.

$$t_{pgate} = t_{inv}\,(p\gamma + LE \times f)$$

Measure everything in units of t_{inv} (divide by t_{inv}):

p – intrinsic delay ($k\gamma_g$) - gate parameter ≠ f(W)
LE – logical effort (k) – gate parameter ≠ f(W)
f – electrical effort (effective fanout)

Normalize everything to an inverter:
$LE_{inv} = 1$, $p_{inv} = \gamma$

Complex Logic Optimization – Final Words

$\gamma = 1$

$EF \approx 4$

$EF^N = PE \Rightarrow N \log_4 EF = \log_4 PE$

Method of Logical Effort

$\Rightarrow N = \log_4 PE$

EFi = LEifi

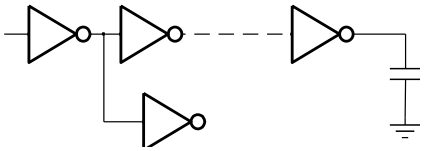
- Compute the path effort: PE = (ΠLE)*BF*
- Find the best number of stages $N \sim \log_4 PE$
- Compute the effective fanout/stage EF = $PE^{1/N}$
- Sketch the path with this number of stages
- Work either from either end, find sizes: $C_{in} = C_{out}$*LE/EF

Reference: Sutherland, Sproull, Harris, "Logical Effort, Morgan-Kaufmann 1999.

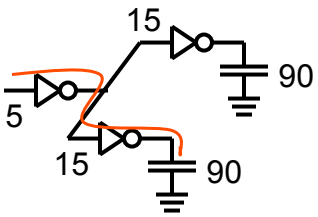
Add Branching Effort

Branching effort:

$$b = \frac{C_{on-path} + C_{off-path}}{C_{on-path}}$$



Branching Example 1

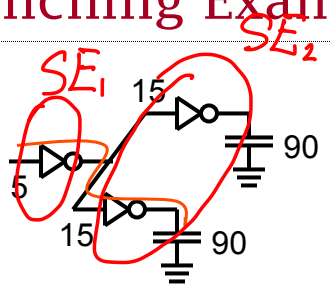


LE = 1
FO = 90/5 = 18
PE = 18 (wrong!)
SE_1 =
SE_2 =
PE =

stage efforts=SE

Branching Example 1

$f_i = \frac{C_{i+1,in}}{C_{i,in}}$



LE	= 1	
FO	= 90/5 = 18	
PE	= 18 (wrong!)	
SE_1	= (15+15)/5 = 6	$LE_i f_i$
SE_2	= 90/15 = 6	
PE	= 36, not 18!	

diffenerent

因为多条path的存在会使反相器不得不做更多的工作，这就是branching effort。在这里，工作量变为两倍。

Introduce new kind of effort to account for branching:

- Branching Effort: $b = \frac{C_{on\text{-}path} + C_{off\text{-}path}}{C_{on\text{-}path}}$
- Path Branching Effort: $B = \prod b_i$

Now we can compute the path effort:

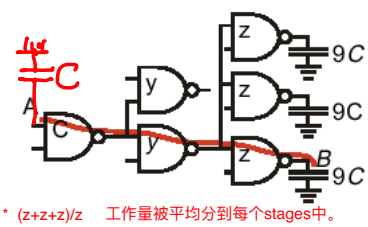
- Path Effort: $PE = \prod LE \cdot FO \cdot B$

Gate Type	Number of Inputs 1	2	3	n
Inverter	1			
NAND		4/3	5/3	(n + 2)/3
NOR		5/3	7/3	(2n + 1)/3
MUX= Multiplexer 2 to 1 MUX F=AC+AC' C=control signal		2	2	2
XOR		4	12	

Branching Example 2

Select gate sizes y and z to minimize delay from A to B

与非门相同的小写字母代表有相同的栅源极电容。



Logical Effort: $LE = (4/3)^3$

Electrical Effort: $FO = C_{out}/C_{in} = 9$

Branching Effort: $B = 2 \cdot 3 = 6$ (y+y)/y * (z+z+z)/z 工作量被平均分到每个stages中。

Path Effort: $PE = \prod LE \cdot FO \cdot B = 128$

Best Stage Effort: $SE = PE^{1/3} \approx 5$

Delay: $D = 3 \cdot 5 + 3 \cdot 2 = 21$

intrinsic delay和fanin基本成正比.

Work backward for sizes:

$$z = \frac{9C \cdot (4/3)}{5} = 2.4C$$

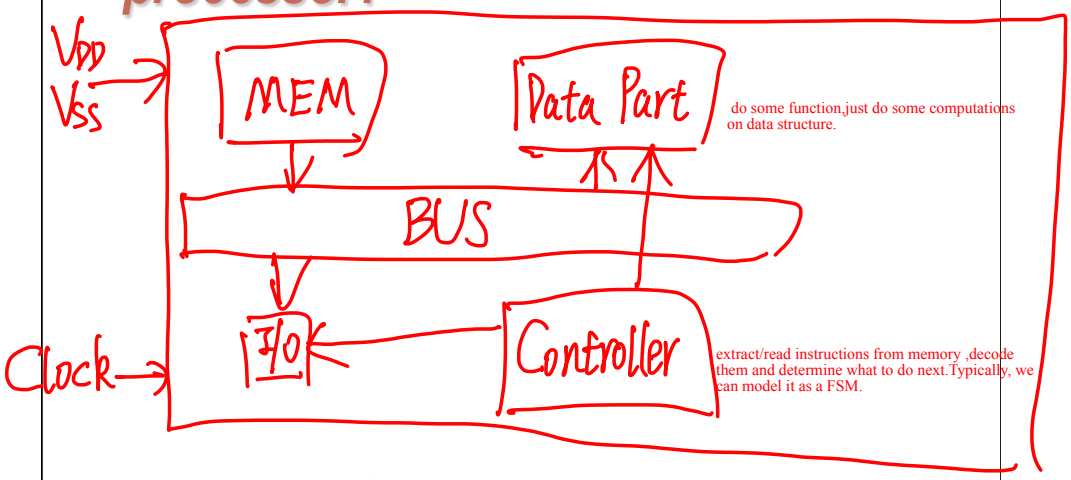
$$y = \frac{3z \cdot (4/3)}{5} = 1.9C$$

Method of Logical Effort

- Compute the path effort: PE = (ΠLE)*BF*
- Find the best number of stages $N \sim \log_4 PE$
- Compute the effective fanout/stage $EF = PE^{1/N}$
- Sketch the path with this number of stages
- Work either from either end, find sizes: $C_{in} = C_{out}$*LE/EF

Reference: Sutherland, Sproull, Harris, "Logical Effort, Morgan-Kaufmann 1999.

What do we need to build a processor?

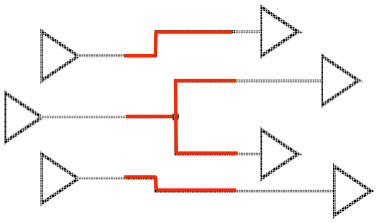


如果wire没有设计得好，可能会导致供能不足或者速度变慢。

Wires

The Wire

The impact of wire on circuit:
An increase in propagation delay , or , equivalently, a drop in performance.
An impact on the energy dissipation and the power distribution.
An introduction of extra noise sources, which affects the reliability of the circuit.



Schematic

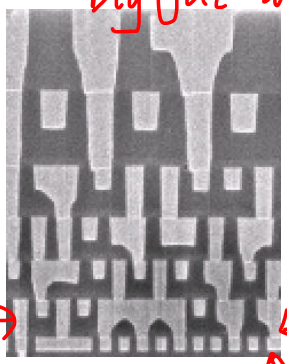
Physical

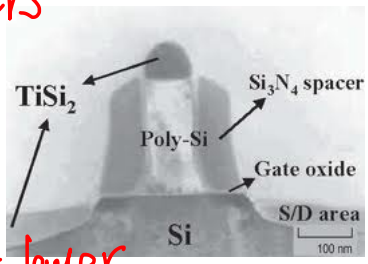
Wires have a certain finite thickness, finite width , finite high.It is a physical entity.
Wire are going to be sitting in a medium. Wires are not living on their own. They are surrounded by 半导体等材料
And they have a capacitor.
Wire are conductors which typically have a resistiance.
Thus, wires add a delay which is RC delay.
They also add power dissipation because you have to charge up their capacitors.
They also add a noise because of the fact that wires are basically coupling each other using capacitors.

The Importance of Wires

Big fat wire at the top layer

6 layers





60 nm transistor

tiny wire

first layer

transistor

Intel 90 nm CMOS cross-section

Wires are all not the same thickness or width

因为顶部的线更长，有更大的电阻，所以需要比底部的电线宽。
同时也可以承载更多的电流。
而底部的线需要连接transistor，因此底部的线需要和transistor差不多大小。

The Importance of Wires

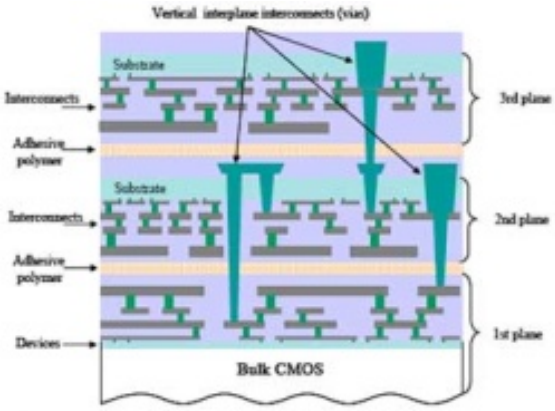


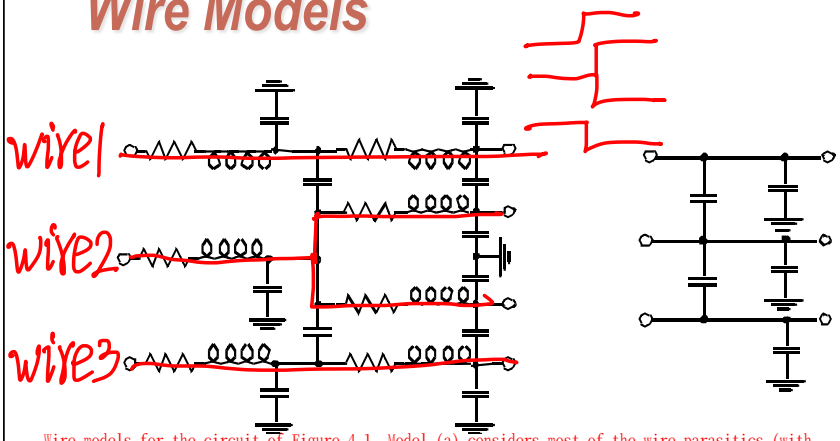
Figure 1. Schematic of a three-dimensional circuit [1].

Inductive effects can be ignored if the resistance of the wire is substantial — this is for instance the case for long Aluminum wires with a small cross-section — or if the rise and fall times of the applied signals are slow.

When the wires are short, the cross-section of the wire is large, or the interconnect material used has a low resistivity, a capacitance-only model can be used (Figure Capacitance-only).

Finally, when the separation between neighboring wires is large, or when the wires only run together for a short distance, inter-wire capacitance can be ignored, and all the parasitic capacitance can be modeled as capacitance to ground.

Wire Models



Wire models for the circuit of Figure 4.1. Model (a) considers most of the wire parasitics (with the exception of inter-wire resistance and mutual inductance), while model (b) only considers capacitance

All-inclusive model

Capacitance-only

线与线之间存在电容相连，因此会存在延迟。
以前导线又粗又好，感应影响比较小，但是随着技术发展，导线越来越小，频率越来越高，感应的影响越来越大。
There is inductance connected to every wiring loop.在低频时，这个inductance非常小。传输速度有限，不可能超高光速。光速1纳秒走30厘米。
但是在硅这些材料中，光速会变慢（没有在真空快，仅有真空中的光速的一半速度），此时，仅能1纳秒走15厘米。

A full-fledged circuit model, taking into account the parasitic capacitance, resistance, and the inductance of the interconnections, is shown in Figure All-inclusive model.

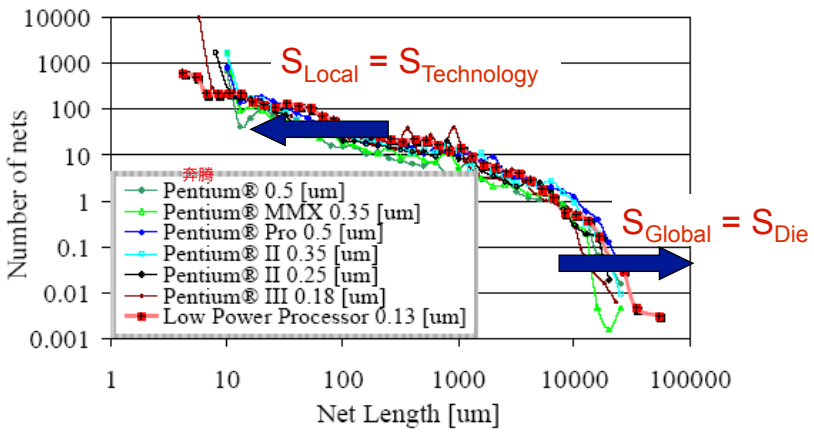
寄生电容是存在于线间的，不是某一点上的，当导线长度明显大于其宽度时，考虑寄生电容是必要的。

Impact of Interconnect Parasitics

寄生的

- Interconnect and its parasitics can affect all of the metrics we care about all are negative effect.
  - Cost, reliability, performance, power consumption
- Parasitics associated with interconnect:
  - Capacitance 走得非常慢，电容起主导作用
  - Resistance 走得快一点，电阻起主导作用
  - Inductance 走得最快，感应起主导作用。

Interconnect Length Distribution



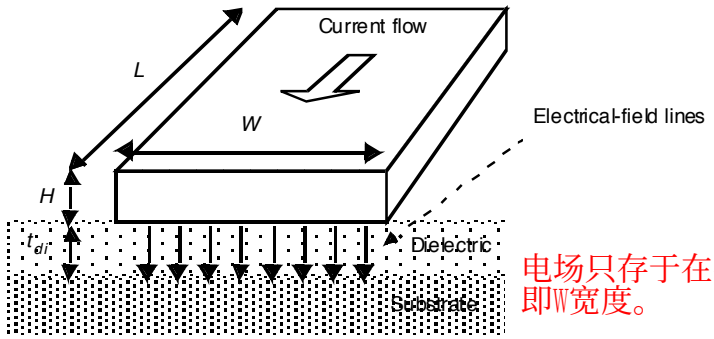
From Magen et al., "Interconnect Power Dissipation in a Microprocessor"

局部的线受到技术影响，全局的长度基本是恒定的，甚至可能会增加长度去连接更多的东西，即增加fanout。
function的功能基本是固定的，只是一个chip会随着技术发展，增加更多的function。

INTERCONNECT

Capacitance: The Parallel Plate Model =导线长度*导线宽度*单位面积电

Area (parallel-plate) capacitance



电场只存于在导体和基底间重叠的部分即W宽度。

Under those circumstances, the total capacitance of the wire can be approximated as $c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$

where W and L are respectively the width and length of the wire, and tdi and εdi represent the thickness of the dielectric layer and its permittivity.

If the width of the wire is substantially larger than the thickness of the insulating material, it may be assumed that the electrical-field lines are orthogonal tothe capacitor plates, and that its capacitance can be modeled by the parallel-plate capacitor model (also called area capacitance).

Permittivity

电容板中间夹着的材料系数，该系数越小，电容越小。

不用这个是担心把电路压缩在一起时会短路。

Material	ε_r
Free space	1
Aerogels 气溶胶	~1.5
Polyimides (organic)	3-4
Silicon dioxide 二氧化硅	3.9
Glass-epoxy (PC board) 玻璃环氧树脂	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package) 矾土	9.5
Silicon	11.7

ε is typically expressed as the product of two terms, or ε = εrε0. ε0 = 8.854 × 10^(-12) F/m is the permittivity of free space, and εr is the relative permittivity of the insulating material.

导线侧壁和基底之间的电容，称为边缘电容

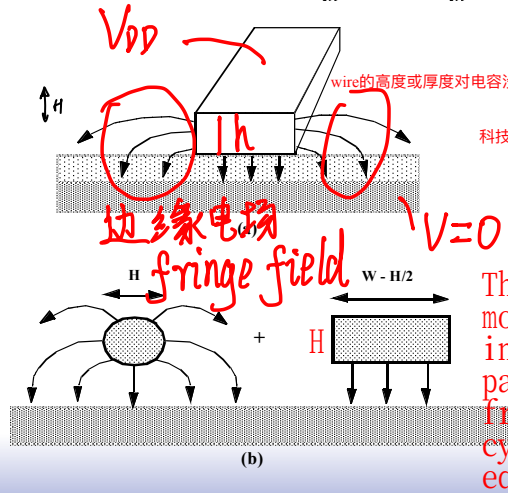
随着工艺的发展W/H的比例逐渐减少，W值变少，布线变密集，面积开销变少，导致fringing capacitance不能再被忽略，上面的模型不再适用。

Fringing Capacitance =导线的长度*单位长度电容

$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$

W=W-H/2

这个公式算出来的都是单位电容



The fringing-field capacitance. The model decomposes the capacitance into two contributions: a parallel-plate capacitance, and a fringing capacitance, modeled by a cylindrical wire with a diameter equal to the thickness of the wire.

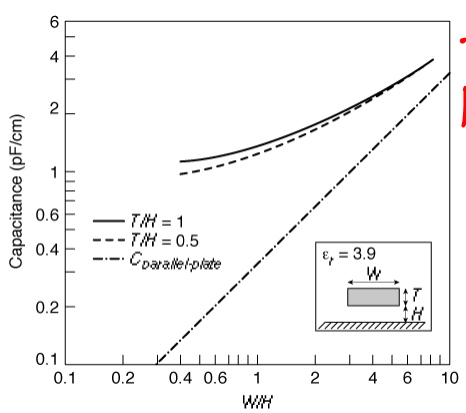
因此线的总电容是：$C_W = WLC_{pp} + 2LC_f$

因为导线有两面，所以这里有个2.

下面这幅图的变量名称和上面的不统一。

技术没成熟时这个影响占据主导地位，但是现在导线越来越细，右边的电容增长迅速，导致两个电容逐渐相等。

Fringing versus Parallel Plate



T=thickness
H=high.

(from [Bakoglu89])

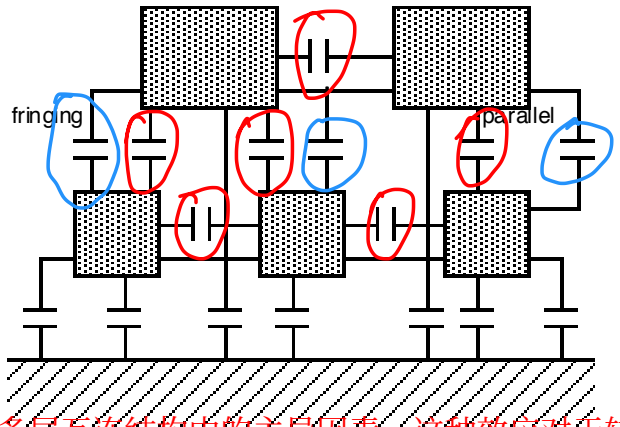
For larger values of (W/H) the total capacitance approaches the parallel-plate model. For (W/H) smaller than 1.5, the fringing component actually becomes the dominant component.

Capacitance of interconnect wire as a function of W/H, including fringing-field effects. Two values of T/H are considered. Silicon-dioxide with εr = 3.9 is used as dielectric.

上面的模型都是基于线放在接地层，且假设线与其它结构完全隔离，仅仅电容耦合到地，这种模型在层数只有一两层时适用，但是当层数不止一两层时，我们必须要有一种新的模型：每条导线不仅耦合到接地基板，还耦合到同一层和相邻层上的相邻导线

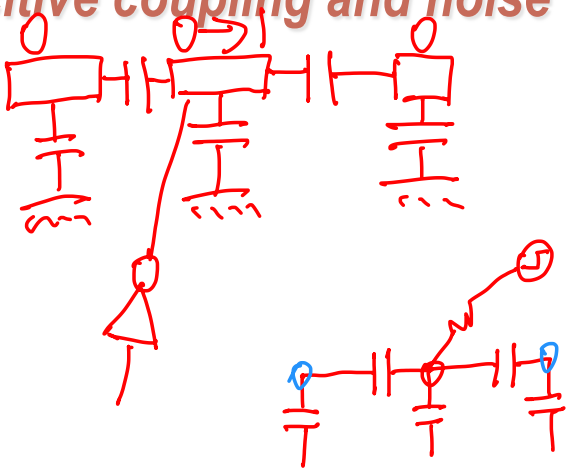
Interwire Capacitance 导线被耦合的长度*单位长度电容

夹在两条线间的电容就是parallel capacitance，
从线的一端引出，接到另一条线的一端的电容是fringing capacitance。
例如，红色圈圈的均是parallel capacitance，蓝色圈圈的均是fringing capacitance。



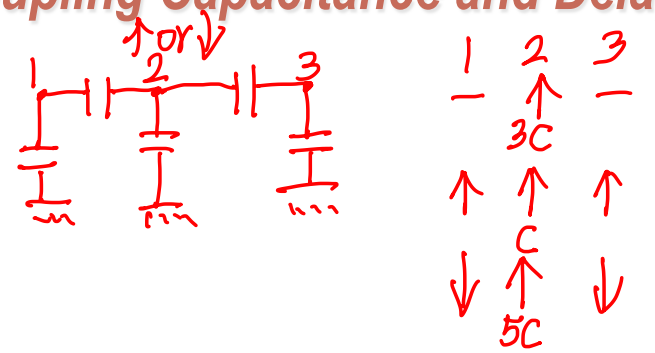
线间电容成为多层互连结构中的主导因素。这种效应对于较高互连层中的导线更明显，因为这些导线离衬底更远。随着特征尺寸的减小，线间电容对总电容的贡献越来越大。

Capacitive coupling and noise

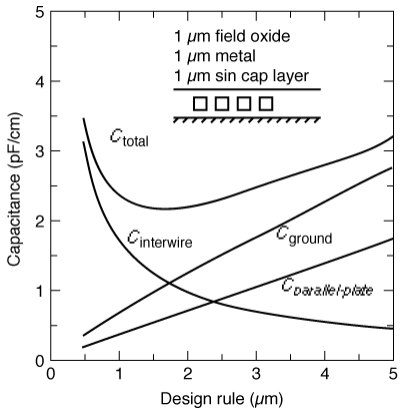


红圈电压从0变为1，蓝圈电压也会受到影响（变高一点点），即给蓝圈添加了噪声。即一条线的电压被改变，和它相邻的电线的电压也会受到影响，它们相当于一个电容分压器。如果这条线是floating wire不接电源或者不接地，那么这种改变是永久的。而且可能会因为受到影响而逐渐变得越来越大，大到一定阈值，晶体管会被打开，然后看到一些错误情况。但实际中，这种事不会发生，会有一些反相器会使它们变为0，不过仍然会有瞬时的影响，这些电线的电压可能会瞬间变高然后瞬速变为0，如果这个瞬时峰值达到一定阈值，晶体管开关依然会被打开。因此，巨大的噪音会产生糟糕的结果。因此电容耦合是一种噪声效应，它的重要性和持续时间取决于所使用的结构。可以同过减少电阻或者电容来削弱这个效应。静态逻辑总是将你的门连接到VDD和地，以抵抗这种影响。

Coupling Capacitance and Delay



Impact of Interwire Capacitance



Interconnect capacitance as a function of design rules. It consists of a capacitance to ground and an inter-wire capacitance

(from [Bakoglu89])

In this graph, which plots the capacitive components of a set of parallel wires routed above a ground plane, it is assumed that dielectric and wire thickness are held constant while scaling all other dimensions. When W becomes smaller than 1.75 H,the inter-wire capacitance starts to dominate.

Wire area and fringe capacitance values for typical 0.25 μm CMOS process. The table rows represent the top plate of the capacitor, the columns the bottom plate. The area capacitances are expressed in aF/μm2, while the fringe capacitances (given in the shaded rows) are in aF/μm.

Wiring Capacitances (0.25 μm CMOS)

Bottom plate

Top plate

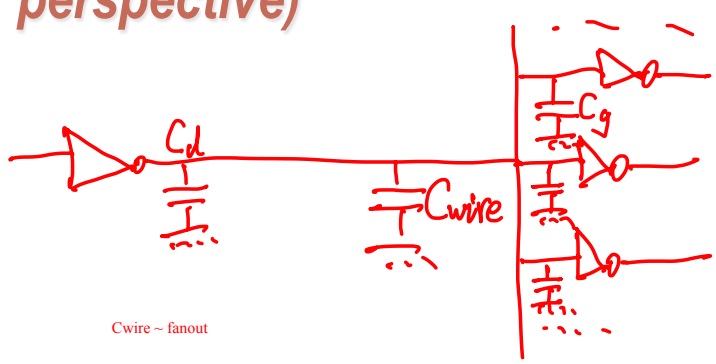
	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88	aF/μm²					
	54	aF/μm 單位					
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

Text126-127

This table tabulates indicative values for the capacitances between parallel wires placed on the same layer with a minimum spacing (as dictated by the design rules).

When computing the fringe capcaitance ,we should double the result because of its two side.

Wiring Capacitances (from a designer perspective)

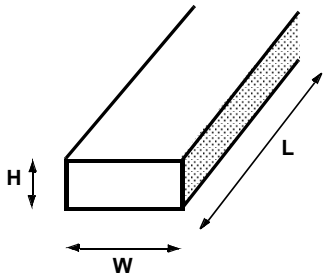


Cwire ~ fanout

INTERCONNECT

Wire Resistance

the constant ρ is the resistivity of the material (in ?-m).



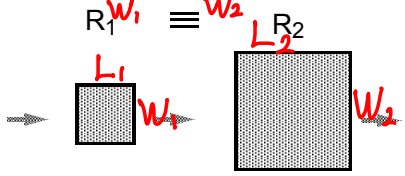
$$R = \rho \frac{L}{HW}$$

material constant

Sheet Resistance

R_o 常数，H是不变的，ρ是由材料和技术决定的

$\frac{L_1}{W_1} = \frac{L_2}{W_2}$



the sheet resistance of the material, having units of Ω/K

Interconnect Resistance

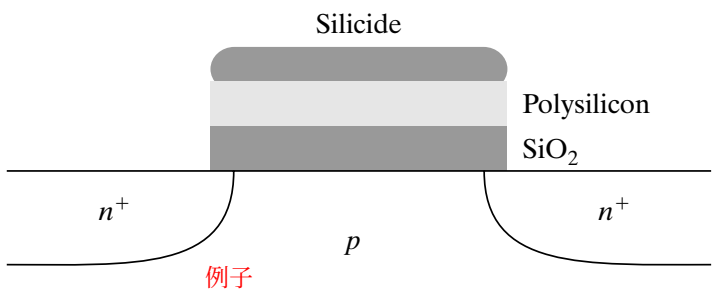
Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu) 处理复杂，不过现在用的就是铜 use a few	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al) 以前用的铝	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

choose, because of the diffusion of others

Dealing with Resistance

- **Use Better Interconnect Materials**
  - e.g. copper, silicides
- **More Interconnect Layers**
  - reduce average wire-length
- **Selective Technology Scaling**
  - (More later)

Polycide Gate MOSFET



Silicides: WSi_2, $TiSi_2$, $PtSi_2$ and TaSi

Conductivity: 8-10 times better than Poly 电阻系数是poly的1/8到1/10

Advanced processes also offer silicided polysilicon and diffusion layers. A silicide is a compound material formed using silicon and a refractory metal. This creates a highly conductive material that can withstand high-temperature process steps without melting.

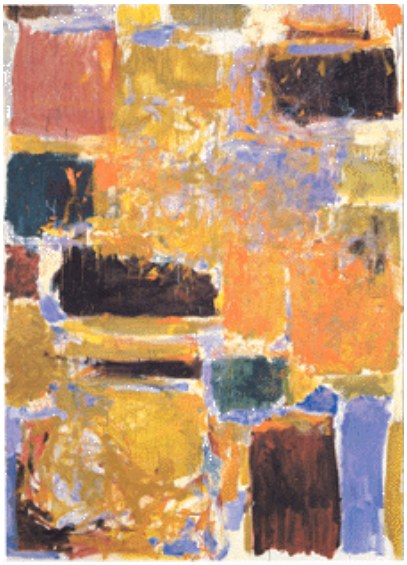
skin effect：当电流频率为高频时，电流密度随深度的增加呈指数下降，高频电流主要在表面流动。
In summary, the skin-effect is only an issue for wider wires. Since clocks tend to carry the highest-frequency signals on a chip and also are fairly wide to limit resistance, the skin effect is likely to have its first impact on these lines.

Sheet Resistance

Material	Sheet Resistance (Ω/❑)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

From this table, we conclude that Aluminum is the preferred material for the wiring of long interconnections. Polysilicon should only be used for local interconnect. Although the sheet resistance of the diffusion layer (n+, p+) is comparable to that of polysilicon, the use of diffusion wires should be avoided due to its large capacitance and the associated RC delay.

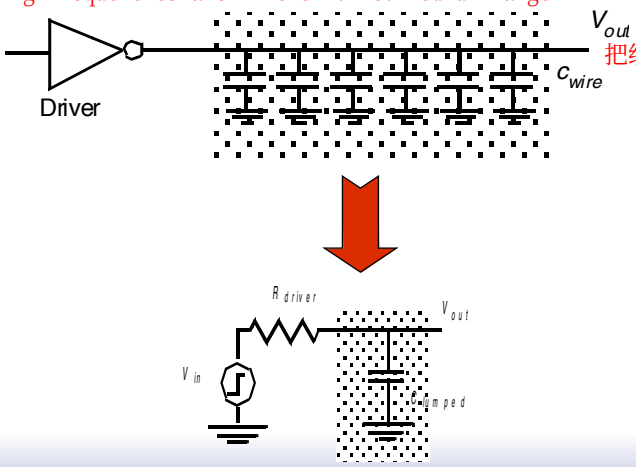
Transitions between routing layers add extra resistance to a wire, called the contact resistance. The preferred routing strategy is thus to keep signal wires on a single layer whenever possible and to avoid excess contacts or via's. It is possible to reduce the contact resistance by making the contact holes larger. Unfortunately, current tends to concentrate around the perimeter in a larger contact hole. This effect, called current crowding, puts a practical upper limit on the size of the contact.



Interconnect Modeling

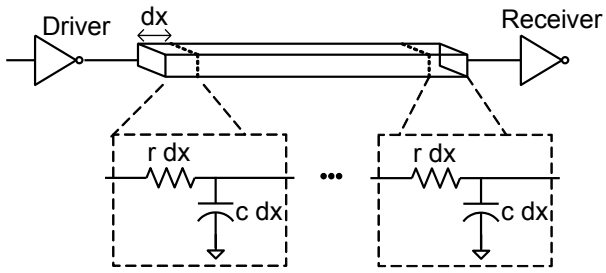
The Lumped Model

使用条件：the resistive component of the wire is small and the switching frequencies are in the low to medium range



把线对电路造成的延迟全部等分到Cwire中。

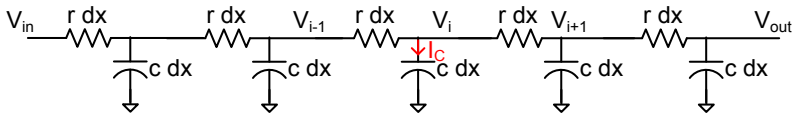
The Distributed RC-line



- Analysis method:
  - Break the wire up into segments of length dx
  - Each segment has resistance (r dx) and capacitance (c dx)

The Distributed RC-line

non-branched RC chain (or ladder)



$$I_C = c\Delta L\frac{\partial V}{\partial t} = \frac{(V_{i-1}-V_i)-(V_i-V_{i+1})}{r\Delta L} \longrightarrow \boxed{rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}}$$

$$\boxed{\tau = \frac{L^2}{2}rc}$$

Wire Model

Model the wire with N equal-length segments:

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \ldots + Nrc) = (rcL^2)\frac{N(N+1)}{2N^2} = RC\frac{N+1}{2N}$$

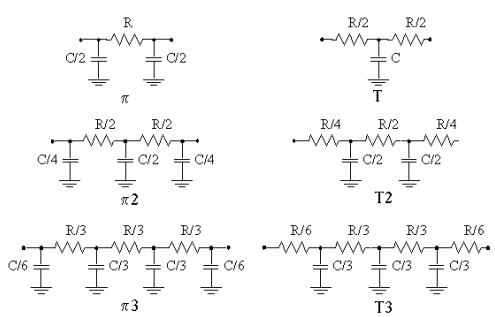
For large values of N:

$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

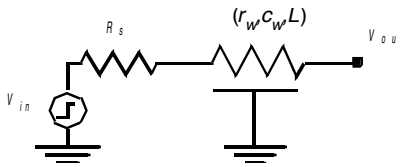
RC-Models

Voltage Range	Lumped RC-network	Distributed RC-network
0→50% (t_p)	0.69 RC	0.38 RC
0→63% (τ)	RC	0.5 RC
10%→90% (t_r)	2.2 RC	0.9 RC

Step Response of Lumped and Distributed RC Networks: Points of Interest.



Driving an RC-line



$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

$$t_p = 0.69 R_s C_w + 0.38 R_w C_w$$