EE141-Spring 2012 Digital Integrated Circuits

Lecture 4
Design Rules
Switch Logic

Administrivia

❑ Labs on Mo and We (next week)
  ▪ Everyone should have an EECS instructional account
❑ Homework #1 due on Monday

Summary

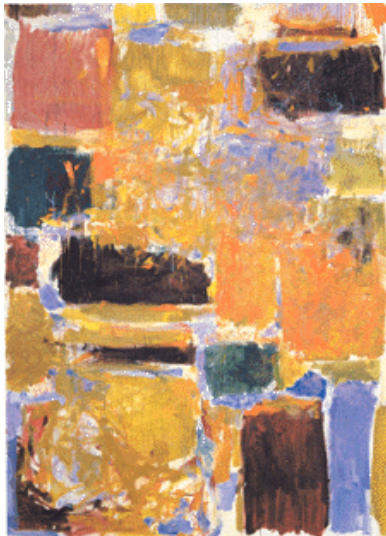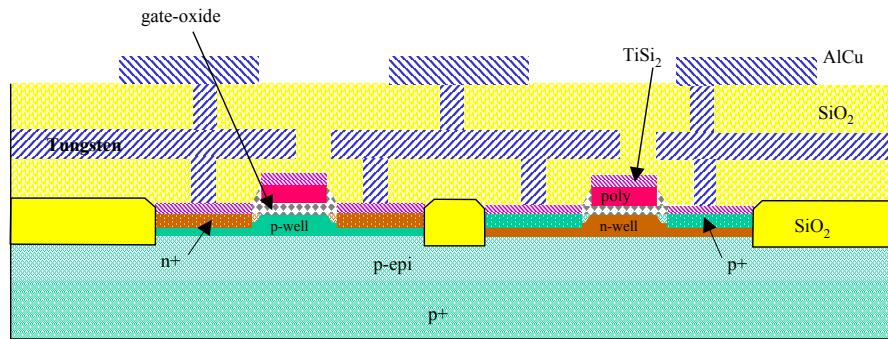❑ Last Lecture
  ▪ Metrics
❑ Today's Lecture
  ▪ Switch model

Intermezzo: Design Rules

A Modern CMOS Process

gate-oxide

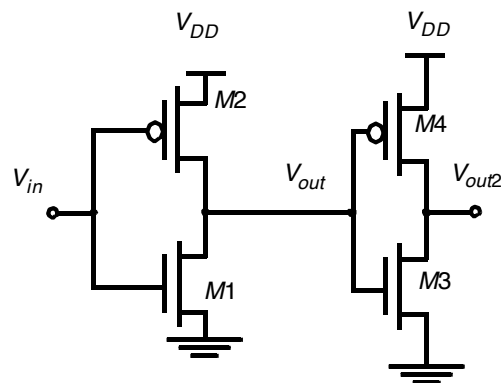TiSi$_2$ AlCu

SiO$_2$

Tungsten

poly

p-well n-well SiO$_2$

n+ p-epi p+

p+

Dual-Well Shallow-Trench-Isolated CMOS Process

Circuit Under Design

V_{DD} V_{DD}

$M2$ $M4$

V_{in} V_{out} V_{out2}

$M1$ $M3$

Two Inverters

size

电容电线开关甚至电阻以及圈出来那些地方都会决定电容大小。

Share power and ground

Abut cells

V_{DD}

Connect in Metal

决定电容大小   wire

wire

决定电阻大小
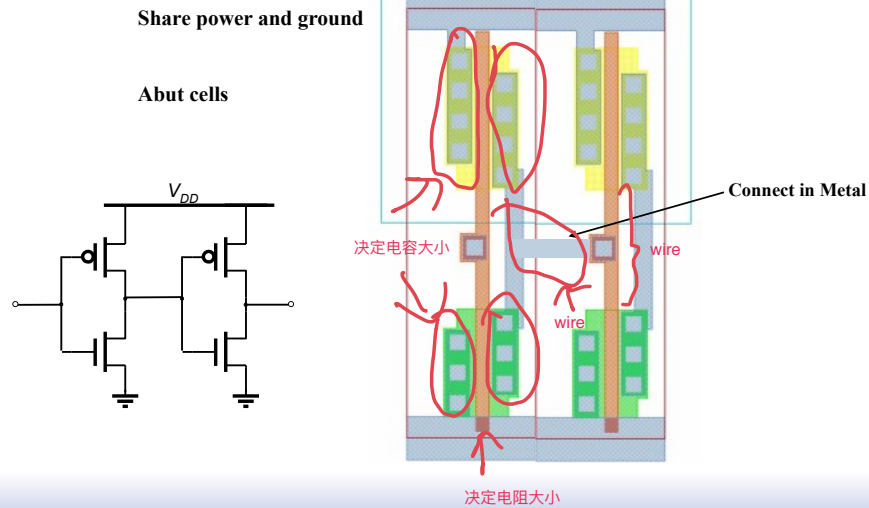
Sticks Diagram

拓扑结构的符号表示，不考虑晶体管的实际size。

仅仅显示晶体管相对于彼此之间的位置以及那个layer使用了那条wire等等，没有实际的size

V_{DD}

3

PMOS transistor

In   *Out*

mental wire

silicon wire

1

GND   NMOS transistor
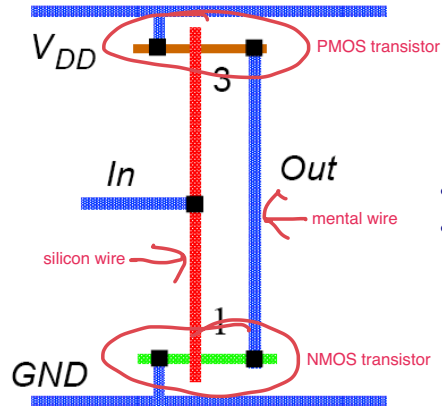
无尺寸的
• Dimensionless layout entities
• Only topology is important

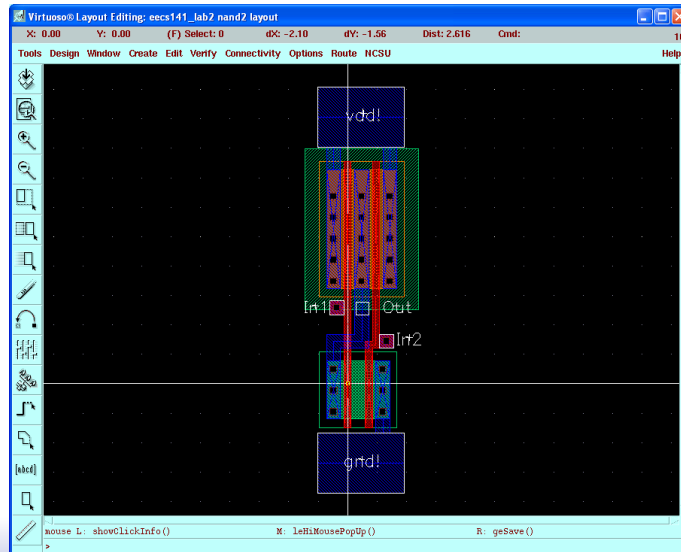**Stick diagram of inverter**

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Layout Editor symbolic layout

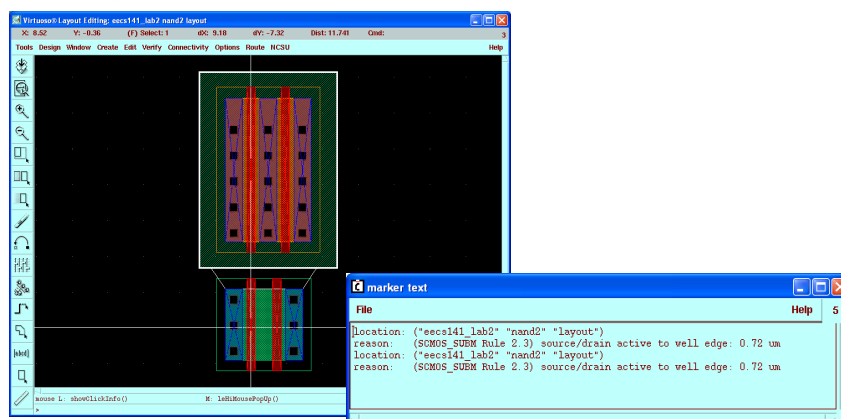

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Design Rule Checker
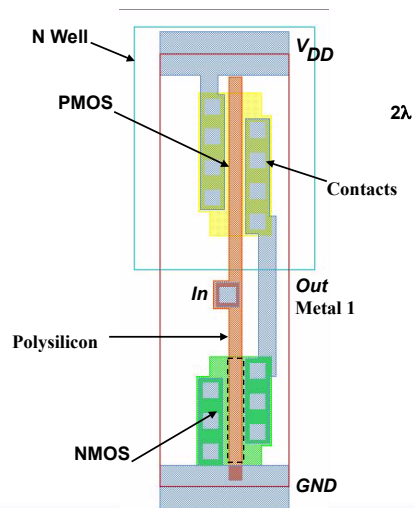

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CMOS Inverter
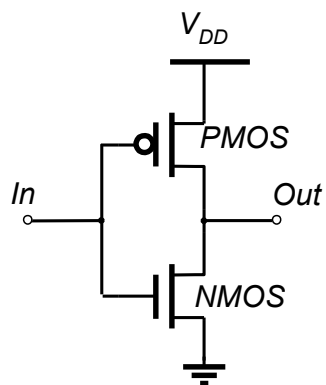
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Two Inverters

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Switch Logic

What is a Transistor?

An MOS Transistor ⟷ A Switch!

$|V_{GS}|$

G

S   D
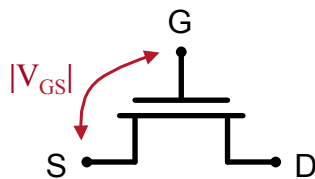
G:gate栅极 S:source源极 D:drain漏极
G形成控制节点（开关），S和D形成通道或者连通节点

控制信号

$|V_{GS}| \geq |V_T|$ threshold

R_{on} 导通电阻或者开关电阻，假设是理想的线性电阻

S   D
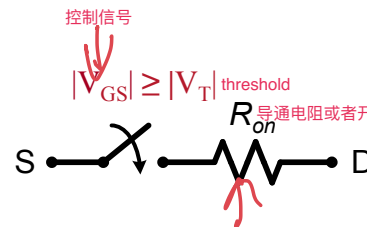
因为在现实中，S和D之间并不是理想的element，
会存在电阻，因此需要引入一个电阻。

Switch Model of MOS Transistor

模电希望器件尽可能是线性的，但是在这里（数电），我们希望器件尽可能是非线性的。

$|V_{GS}|$

G

S   D

R_{on}

S   D

S   D

$|V_{GS}| < |V_T|$

$|V_{GS}| > |V_T|$
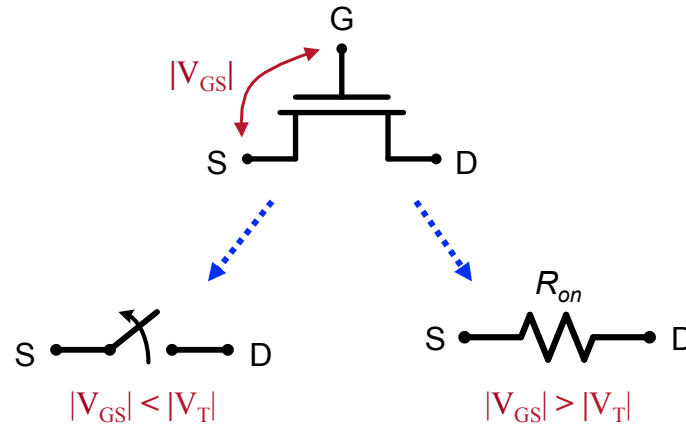
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A Modern Sub-100 nm Look …

$|V_{GS}|$

G

S   D

R_{off}

S   D

R_{on}

S   D

$|V_{GS}| < |V_T|$

$|V_{GS}| > |V_T|$
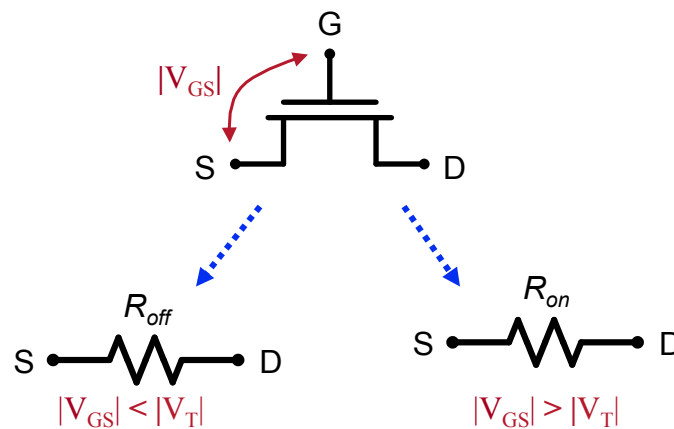
modern transistor   switch   S   O
S
switch   leaky switch

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NMOS and PMOS 互补开关complementary switch

NMOS Transistor

$V_{GS} > 0$

G

S   D

X R_{on}

Y   Z

Y=Z IF X=1

PMOS Transistor

$V_{GS} < 0$

G

这个小圆圈表示一个反相器。

S   D

X R_{on}

Y   Z

Y=Z IF X=0

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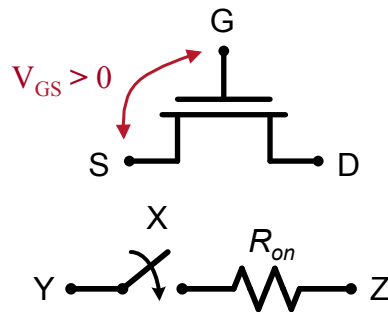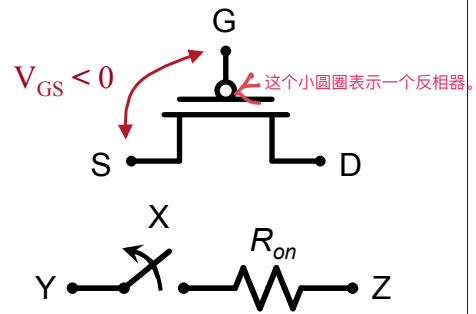
Building an Inverter with Switches

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The CMOS Inverter: A First Glance

DC characteristic:施加一个固定电压
给电路，观察电路的输出电压值。观察
这个特性时，不需要理会时间。=VTC=static behavior
因为PMOS和NMOS的构造有点不一样，
所以如果想要PMOS和NMOS的电阻大小
一样从而尽可能使得VM=VDD/2，那么
PMOS和NMOS的大小会有一点不一样，
但是应该尽可能一样。同时还要尽可能
使PMOS和NMOS尽可能接近。

symmetrical voltage transfer
等价于VM=VDD/2

V_{DD}

V_{in}

V_{out}

C_L

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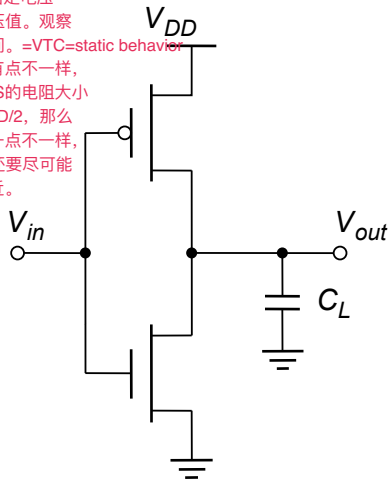## CMOS Inverter
First-Order DC Analysis

V_{DD}

V_{DD}

R_p

V_{out}

V_{out}

R_n

$V_{in} = V_{DD}$

$V_{in} = 0$
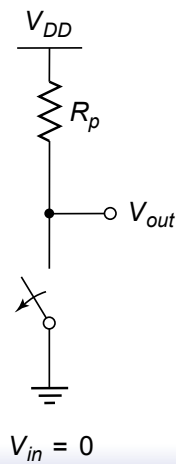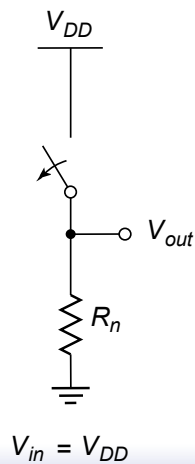
$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

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Simulated Inverter VTC (Spice)

VOH?

gain是VTC的导数

-1

为了找到noise margin，我们需要先找到VTC的两条切线
这两条切线的斜率都是-1.

上下各有一半区域的gain=

2

VIL-VOL

1.5

V_{out} (V)

1

在VM哪里，gain非常陡峭。

undefined
region

0.5

VOL

-1

VOL-VIH

0

0   0.5   VIL   VIH 1.5   2   2.5

V_{in} (V)
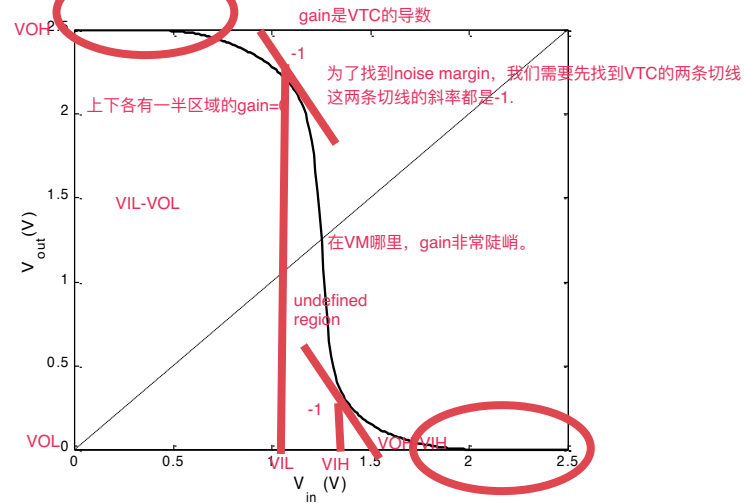
CMOS Inverter: DC Properties

❑ V_{OH} =

❑ V_{OL} =

❑ V_{IL} =

❑ V_{IH} =

❑ N_{MH} =

❑ N_{ML} =

❑ V_M =

CMOS Inverter: DC Properties

- $V_{OH} = V_{DD} = 2.5V$
- $V_{OL} = 0V$
- $V_M = 1.2V$
- $V_{IL} = 1.05V$
- $V_{IH} = 1.45V$
- $N_{MH} = 1.05V$
- $N_{ML} = 1.05V$

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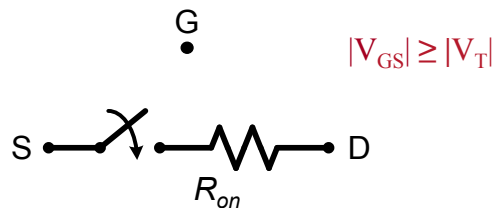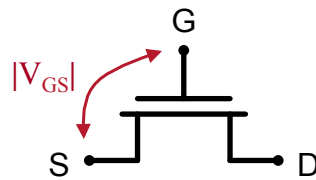# The Switch Revisited

$|V_{GS}|$

G

S   D

G

$|V_{GS}| \geq |V_T|$

S   D

R_{on}

静态电流=VDD/(Ron+Roff)
静态功率=静态电流*VDD
steady-state=static=switch is not activity or changing。

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The Switch Revisited

S和D一般会连接电容。G和S之间，G和D之间各有一个电容。

G

$|V_{GS}|$

S   D

V_{DD} C_{sp}

PMOS

$C_L = C_{DP} + C_{Dn}$

In   Out

$C_{gp} + C_{gn}$

NMOS

C_{sp}

上面这两个电容是存在浮动
或者漂移的电容，所以为了
方便处理，我们需要进行简化。

$|V_{GS}| \geq |V_T|$

G

C_{GS} C_{GP}

S   D

C_S R_{on} C_D

CL除了要把CDP和CDN相加以外还需要把fanout的所有CGP和CGN相加，还要把wire capacitance
（因为线与线之间存在电介质）添加进去。

G

C_g

$|V_{GS}| \geq |V_T|$

简化后：S   D

C_S R_{on} C_D
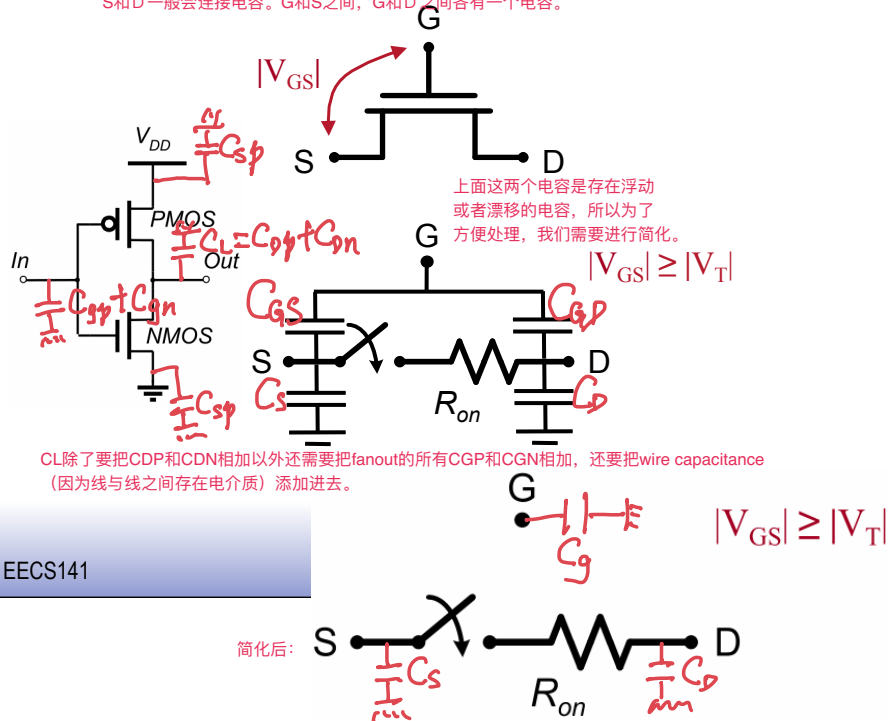
CMOS Inverter: Transient Response
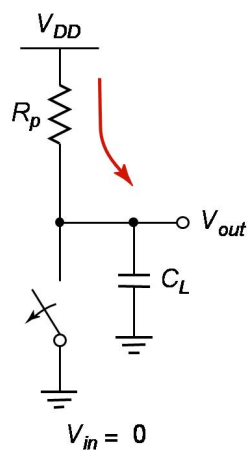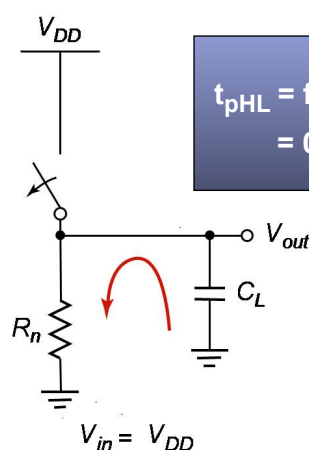
V_{DD} V_{DD}

R_p

V_{out}

C_L

$V_{in} = 0$

R_n

V_{out}

C_L

$V_{in} = V_{DD}$

$t_{pHL} = f(R_{on}C_L)$
$= 0.69\ R_n\ C_L$

(a) Low-to-high   (b) High-to-low

nmos
pmos
nmos
nmos 10k
nmos 10
pmos nmos 10k
cmos pmos
nmos pmos
nmos pmos
nmos pmos
n P nmos R pmos R
nmos 3RC(R C) R pmos nmos cmos
pmos

CMOS Properties

❑ Full rail-to-rail swing$_{VL=0}$，VH=VDD指电压变化由0变为VDD或由VDD变为0.

❑ Symmetrical VTC

❑ Propagation delay function of load capacitance and resistance of transistors

❑ No static power dissipation因为PMOS和NMOS互补

❑ Direct path current during switching

因为电压变化是存在坡度的，因此存在一个电压区间（或电压变化时间）使得PMOS和NMOS都是连通的，此时VDD和ground直接相连从而造成电源的能量直接流失在ground中而不对任何电容充电，例如VDD-VTP这一电压值。减少这种浪费的方法是加快PMOS和NMOS开关的转换或者开合速度。

$$P = C_L V_{DD}^2 f_{0 \to 1}$$

当输出由0变为1时，CL开始充电，其中一半的电能耗散在热能中，另一半的电能存储在CL中，当输出由1变为0时，CL放电，把自身存储的电能释放，转换成热能进行耗散，此时电源VDD断开连接，因此P与输出由1变为0无关，电源损失的能量也与输出由1变为0无关。

Impact on Reliability?

降低电压会使noise margin以2倍速度减少。不过，来自电路内部的耦合电容噪音也会随之缩小。电源电压噪声也会缩小，但部分噪声不变。

Impact on Performance?

Lecture #4

Impact on Power/Energy

Lecture #4

EE141

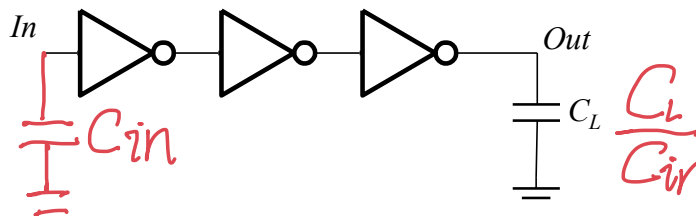stage?   four

The Next Question: Inverter Chain

In —▷○—▷○—▷○— *Out*

C_{in}

C_L $\dfrac{C_L}{C_{in}}$

❑ For some given C_L:
- How many stages are needed to minimize delay? two
- How to size the inverters?

第一个反相器的尺寸最小，接着从左往右的反相器依次递增。

❑ Anyone want to guess the solution?

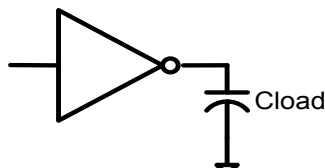EECS141   Lecture #4   31

Careful about Optimization Problems

❑ Get fastest delay if build one **very** big inverter
- So big that delay is set only by self-loading

—▷○— Cload

❑ Likely not the problem you're interested in
- Someone has to drive this inverter…

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Engineering Optimization Problems in General

❑ Need to have a set of constraints

❑ Constraints key to:
- Making the result useful
- Making the problem have a 'clean' solution

❑ For sizing problem:
- Need to constrain size of first inverter

Delay Optimization Problem #1

❑ You are given:
- A <u>fixed</u> number of inverters
- The size of the first inverter
- The size of the load that needs to be driven

❑ Your goal:
- Minimize the delay of the inverter chain

❑ Need model for inverter delay vs. size

PMOS的size/wide一般是NMOS的两倍，这样才可以使这两个transistor的电阻相同。
单位面积的电容由氧化物的厚度决定。增加较薄的氧化物的厚度的stages和改变transistor的电阻数值一样。
因此，结果是单位面积的电容都是一样的，但是PMOS的电容是栅极的两倍。
栅极的单位面积的电容=栅极的单位长度电容=栅极的单位宽度电容=Cg=单位面积电容=漏极/源极的单位面积电容

栅极单位面积的电容由栅极面积和单位面积电容决定

Inverter Delay

Delay: $t_{pHL} = (\ln 2) \, R_N C_L$ $t_{pLH} = (\ln 2) \, R_p C_L$

□ Assume we want equal rise/fall delays

$t_{pHL} = t_{pLH}$

- Need approximately equal resistances, $R_N = R_P$
- PMOS approximately 2 times larger resistance for same size;
- Must make PMOS 2 times wider, $W_P = 2W_N = 2W$
- $t_p = (\ln 2) \, (R_{inv}/W) \, C_L$ with R_{inv} resistance of minimum size NMOS

因为device是NMOS的W倍宽，所以其阻值是NMOS的1/W。

$C_P = 2WC_g$

2W

W

$C_N = WC_g$
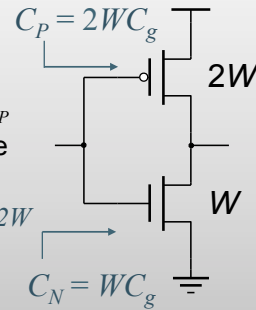
Loading on the previous stage: $C_{in} = WC_{ginv} = W(3C_G)$

$C_{pd} = 2C_{Nd}$

$C_{pg} = 2C_{Ng}$
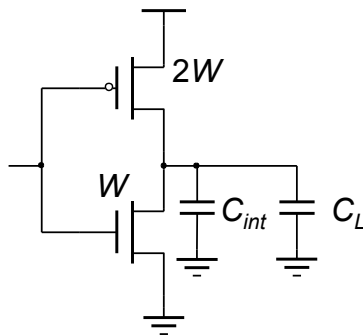
$C_{ps} = 2C_{Ns}$

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Inverter Delay Model

2W

W C_{int} C_L

$R = R_{inv}/W$
$C_{int} = W(3C_d) = WC_{dinv}$

Cd为漏极单位面积电容，Cdinv为反相器的栅极的单位面积电容。

Replace ln(2) with k (a constant):

Delay $= kR(C_{int} + C_L)$

Delay $= k(R_{min}/W)(WC_{dinv} + C_L)$

使晶体管变大，虽然使晶体管电阻变小，但是会使晶体管的内部电容变大，
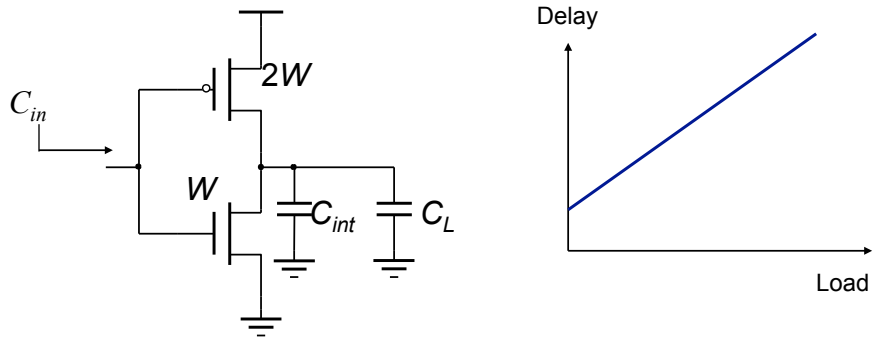从而导致晶体管的内部延迟会保持不变。但是外部电容是固定的，因此会导
致整体延迟减少。

$R_{min} = R_{inv}$

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Inverter with Load

C_{in}

2W

W

C_{int} C_L

Delay

Load

Delay = $kR\,C_{in}(C_{int}/C_{in} + C_L/C_{in})$
   = $kR_{min}C_{ginv}[C_{dinv}/C_{ginv} + C_L/(WC_{ginv})]$
   = Delay (Internal) + Delay (Load)

$C_{dinv}/C_{ginv} = \gamma =$ **Constant independent of size** 大部分这个常数约为1

s：源极 g：栅极 d：漏极 inv：inverter

Delay Formula

$$Delay \sim R_W\left(C_{int} + C_L\right)$$

$$t_p = kR_W C_{in}\left(C_{int}/C_{in} + C_L/C_{in}\right) = t_{inv}\left(\gamma + f\right)$$

fanout=0,   f=0

$C_{int} = \gamma\, C_{in}$ ($\gamma \approx 1$ for CMOS inverter)
$f = C_L/C_{in}$ – electrical fanout
$t_{inv} = kR_{min}C_{ginv}$ =the delay of the minimum inverter without any CL

t_{inv} is independent of sizing of the gate!!!

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