On Test Data Volume Reduction for Multiple Scan Chain Designs

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We consider issues related to the reduction of scan test data in designs with multiple scan chains. We propose a metric that can be used to evaluate the effectiveness of procedures for reducing the scan data volume. The metric compares the achieved compression to the compression which is intrinsic to the use of multiple scan chains. We also propose a procedure for modifying a given test set so as to achieve reductions in test data volume assuming a combinational decompressor circuit.

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1. INTRODUCTION

Reducing test data volume and test application time is important in reducing the cost of testing VLSI circuits. Several recent works have addressed these problems. In addition to the use of multiple scan chains, compact test set generation procedures are typically used to reduce the test application time and test data volume [Hamzaoglu and Patel 1999b; Kajihara et al. 1995; Pomeranz et al. 1993]. Other methods to reduce test data volume use encoding techniques to compress tests [Bayraktaroglu and Orailoglu 2001; Chandra and Chakrabarty 2001; Hamzaoglu and Patel 1999a; Hellebrand et al. 1995; Jas et al. 1999, 2000; Koneman 1993]. Some of these methods are applicable to given test sets [Chandra and Chakrabarty 2001; Hellebrand et al. 1995; Jas et al. 1999; Koneman 1993] and some modify test generation procedures to facilitate the encoding procedure used [Bayraktaroglu and Orailoglu 2001]. On-chip decompressor circuits are then used to derive the tests applied to the circuit-under-test. The method in Hamzaoglu and Patel [1999a] uses a single scan input to drive multiple internal scan chains. In order to achieve complete fault coverage, it uses parallel and serial loading of scan chains that are driven by one external scan input. This method reduces test data volume and also reduces test application time. However, compared to the test application time when the internal scan chains are loaded from independent scan inputs the test application time in Hamzaoglu and Patel [1999a] is higher since several tests are scanned in serially into all the scan elements that are connected to a single external scan input.

The main contribution of this work is a metric to evaluate the effectiveness of compression procedures for designs with multiple scan chains. The metric is based on the definition of an upper bound on the amount of test data that needs to be supplied to a combinational decompressor in order to apply a complete test set to the circuit. The upper bound defines a compression level which is intrinsic to the design and can be achieved in a trivial way. Given a test data compression procedure, we measure the level of test data compression it provides relative to the intrinsic compression level given by the upper bound. The ratio is smaller than one if the procedure achieves higher levels of compression than the trivial, intrinsic level.

We also propose a method to modify a given test set to achieve reductions in test data volume such that the proposed metric is smaller than one. The proposed method does not require modification of the ATPG since it works on a given test set.

The focus of the work is on the reduction of scan input test data volume. We do not consider test response compression. In the experimental results presented later we also do not consider compression of test data that drives the primary inputs of the circuit. However, if desired, compression of this data can also be included in the procedure.

2. A METHOD TO EVALUATE TEST DATA VOLUME REDUCTION PROCEDURES FOR MULTIPLE SCAN CHAIN DESIGNS

In Figure 1, we give the block diagram of a multiple scan chain design that uses encoding to reduce test data volume. The design has *NSC* internal scan chains.

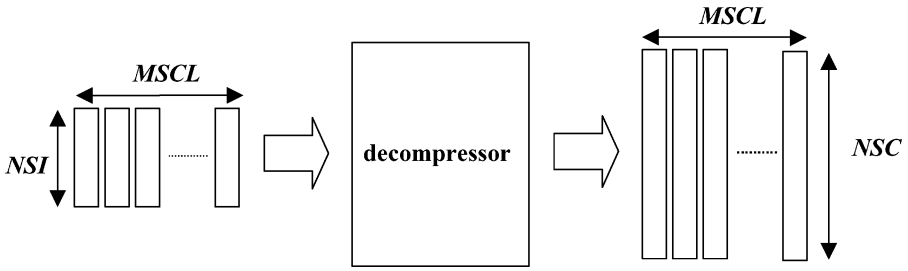

Fig. 1. A combinational decompressor.

The scan chains are driven by a decompressor circuit, which receives test data on *NSI* external scan input pins. The decompressor produces the vectors shifted into the *NSC* scan chains of the design one vector at a time. The decompressor circuit can be a combinational or a sequential circuit (a combinational descompressor is shown in Figure 1, as explained below).

In this work, we concentrate on the case of a combinational decompressor circuit. For combinational decompressors, the number of vectors that need to be supplied at the inputs of the decompressor to create one test is the same as the maximum length of an internal scan chain. This is demonstrated in Figure 1 where we show a combinational decompressor circuit that accepts *MSCL* vectors each consisting of *NSI* bits from the tester, and produces *MSCL* vectors each consisting of *NSC* bits to be applied to the circuit-under-test. Here, *MSCL* is the maximum length of a scan chain. The compression ratio is $CR = NSC/NSI$.

One can consider using more than one decompressor. For example, it is possible to use a separate decompressor for each test or subsets of tests. Using two or more decompressors may lead to better test data volume compression. One can also use separate decompressors for separate subsets of scan chains. This is expected to reduce the complexity of the design of decompressors, however may not lead to optimum test data volume reduction. In this article, we consider the case of using a single decompressor.

Another important issue is that the number of external scan inputs *NSI* can be arbitrarily reduced down to a minimum of one if test application time is not important. This can be done by time multiplexing the test data on to the chosen number of external scan inputs and using an appropriate-sized buffer driving the inputs of the decompressor. This however does not decrease test data volume. We do not include multiplexing test data on to external scan inputs in our study since it can be done in a straightforward manner when desired and the increase in test application time is acceptable.

For the case of a single combinational decompressor a bound on the number of external scan inputs *NSI* can be computed that is independent of the actual data (i.e., the bit values in the test set) and depends only on the number of tests *NT,* as follows. The maximum number of distinct *NSC* bit wide output vectors of the decompressor is $Min(2^{NSC}, MSCL*NT)$. This is the maximum number of distinct *NSC* bit wide vectors that are shifted into the scan chains of the circuit-under-test in order to apply all the tests. The number of inputs of the combinational decompressor needed to allow us to produce these distinct output

patterns is $MTPIN = \log_2(Min(2^{NSC}, MSCL*NT))$. Thus, the ratio $NSC/MTPIN$ can be viewed as the intrinsic achievable test data reduction capability of the multiple scan design.

Consider an example design with 256 scan chains of maximum length 1024 and 16,000 tests. For this design $MTPIN$ is 24 and hence the intrinsic achievable data compression for this design using a combinational decompressor is 256/24.

$MTPIN$ can be interpreted as an upper bound on the number of external scan inputs NSI that are needed to drive the decompressor. This bound is achievable for any given test set if we do not place any restrictions on the decompressor other than that it is a combinational circuit. It is possible to use fewer than $MTPIN$ scan inputs to drive the decompressor if the tests applied to the circuit-under-test are such that the number of distinct NSC bit wide vectors that need to be produced at the outputs of the decompressor does not exceed $2^{(MTPIN-1)}$, which is often the case.

3. THE PROPOSED METHOD TO REDUCE TEST DATA VOLUME

Given a design with multiple scan chains and the constraint of using a combinational decompressor one can use the following strategies to reduce test data volume. One can develop a test generation procedure that generates tests which require fewer external scan inputs. Another method is to modify a given test set such that the modified test set requires fewer external scan inputs. The latter method has the advantage of not requiring any modifications to existing test generators. We propose a procedure to reduce test data volume for multiple scan chain designs that is applicable to any given test set. In the proposed procedure we first change a maximal number of specified values in the given tests to unspecified values without losing fault coverage. We then change the unspecified values into specified values such that the total number of distinct output vectors produced at the output of the decompressor is minimized. If the number of distinct output vectors needed at the output of the decompressor for the modified tests is NDO then we need to use only $\log_2 NDO$ external scan inputs, or $NSI = \log_2 NDO$. Experimental results given demonstrate that the proposed procedure helps reduce the test data volume by showing that the ratio of $NSI/MTPIN$ for the procedure is smaller than 1.

3.1 Identification of Don't Care Inputs

In order to enhance the test data compression we modify some values in the test vectors. Given a test set in which all the input values in all the test vectors are specified to either 0 or 1, some primary input values may be changed to the opposite logic values without losing coverage of single stuck-at faults. We can regard such input values as don't-cares (X). An example is shown using Figure 2 and Table I. For the circuit in Figure 2, suppose that test set T in Table I(a) is generated. Test set T' in Table I(b) is obtained after changing some input values to X. T' detects the same stuck-at faults as T.

Recently, a method to identify input values in test vectors that can be set to X was given in Kajihara and Miyase [2001]. In this method, fault simulation and procedures similar to implication and justification of ATPG algorithms are

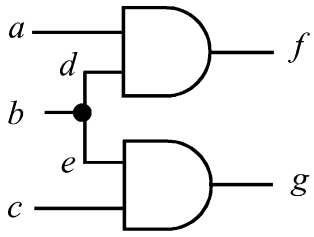

Fig. 2. Example circuit.

Table I(a). Given Test Set T

	a	b	c
t_1	1	1	0
t_2	1	0	1
t_3	0	1	0
t_4	0	1	1

Table I(b). Obtained Test Set T'

	a	b	c
t_1	1	1	x
t_2	1	0	1
t_3	0	1	0
t_4	x	1	1

employed with appropriate restrictions. We use this procedure to first change a maximal number of specified values in the test sets to don't-cares. Next, for the given number of scan chains, we determine the distinct patterns that are to be produced at the outputs of the decompressor. Since the test vectors now have don't-care values, the decompressor output patterns will also have don't-care values. We merge the compatible output patterns to reduce the total number of distinct patterns. This process is a similar to static test compaction Goel and Rosales [1979]. As a result, the number of scan-in inputs *NSI* computed as $\log_2 NDO$ is reduced.

As can be seen from the description of the proposed method, the method can be used with any test set and hence it is not necessary to modify the ATPG to apply the method. Furthermore, other encoding methods such as LFSR based methods [Hellebrand et al. 1995; Koneman 1993], statistical encoding methods [Jas et al. 1999] and run length-encoding methods [Chandra and Chakrabarty 2001] can be used to obtain additional reductions in test data volume.

3.2 Iteration of Don't Care Identification

After we obtain a modified test set T' by specifying Xs so that *NDO* becomes small, we can apply the method again by regarding the test set T' as a given test set T. The iteration may allow *NDO* to be smaller. In order to reduce *NSI*, which is computed as $\log_2 NDO$, *NDO* has to be reduced by a factor of two at least. Hence, reduction of *NDO* does not necessarily change *NSI*. Therefore, iteration may not contribute to reduction of test data volume. However, it would be effective for reducing the complexity of the decompressors.

In the process of iterating modification of the test set, we try to decrease *NDO*. We use the following heuristic for this. If a vector at the output of the decompressor appears many times, values of the vector do not have to be changed, that is, Xs don't have to be identified on such vectors. On the other hand, if a

Table II. Results of the Proposed Method

Circuit	*NT*	*NSC*	*MSCL*	*MTPIN*	*NDO*		*NSI*		*NSI*/*MTPIN*		*CR*
					wo_X	*w_X*	*wo_X*	*w_X*	*wo_X*	*w_X*	
s5378	100	8	23	8	251	26	8	5	1	0.63	1.60
	100	16	12	11	1135	45	11	6	1	0.55	2.67
	100	24	8	10	798	74	10	7	1	0.70	3.43
	100	32	6	10	600	141	10	8	1	0.80	4.00
s9234	111	8	29	8	248	36	8	6	1	0.75	1.33
	111	16	15	11	1369	69	11	7	1	0.64	2.29
	111	24	10	11	1104	103	11	7	1	0.64	2.29
	111	32	8	10	886	186	10	8	1	0.80	4.00
s13207	235	8	84	8	256	23	8	5	1	0.63	1.60
	235	16	42	14	3857	24	12	5	0.86	0.36	3.20
	235	24	28	13	5212	29	13	5	1	0.38	4.80
	235	32	21	13	4624	34	13	6	1	0.46	5.33
s15850	97	8	75	8	256	34	8	6	1	0.75	1.33
	97	16	38	12	2900	54	12	6	1	0.50	2.67
	97	24	25	12	2401	91	12	7	1	0.58	3.43
	97	32	19	11	1842	117	11	7	1	0.64	4.57
s35932	12	8	216	8	178	87	8	7	1	0.88	1.14
	12	16	108	11	406	180	9	8	0.82	0.73	2.00
	12	24	72	10	197	93	8	7	0.80	0.70	3.43
	12	32	54	10	397	237	9	8	0.90	0.80	4.00
s38417	87	8	205	8	256	37	8	6	1	0.75	1.33
	87	16	103	14	6573	124	13	7	0.93	0.50	2.29
	87	24	69	13	5941	264	13	9	1	0.69	2.67
	87	32	52	13	4524	343	13	9	1	0.69	3.56
s38584	114	8	182	8	256	29	8	5	1	0.63	1.60
	114	16	91	14	7820	53	13	6	0.93	0.43	2.67
	114	24	61	13	6876	99	13	7	1	0.54	3.43
	114	32	46	13	5241	133	13	8	1	0.62	4.00

NT: Number of tests
NSC: Number of scan chains
MSCL: Maximum length of a scan chain
MTPIN: Maximum number of decompressor inputs required
NDO: Number of distinct vectors at the output of the decompressor
NSI: Number of scan input pins that are inputs of the decompressor
CR: *NSC*/*NSI*

vector does not appear at the decompressor output many times, values on the vector should have Xs so that the vector becomes compatible with other vectors. Thus, we need to selectively convert specified values in tests to Xs. A procedure to identify Xs on specific bits was given in Miyase et al. [2002], and we employ it in the iteration process.

4. EXPERIMENTAL RESULTS

We implemented the proposed method using the C language on a PC (Dual Athlon MP 2000+, 512MB), and applied it to ISCAS'89 benchmark circuits. The test sets used in this experiment were generated by a test generator that uses dynamic and static test compaction techniques [Kajihara et al. 1995]. The number of internal scan chains of the designs (*NSC*) was set to 8, 16, 24 or 32. The order of scan elements in the scan chains was set arbitrarily. Table II gives

Table III. Comparison with the Method of Bayraktaroglu and Orailoglu [2001]

	Method of Bayraktaroglu and Orailoglu [2001]			Proposed Method		
Circuit	*NT*	*NSI*	*NSI*/*MTPIN*	*NT*	*NSI*	*NSI*/*MTPIN*
s38584	216	24	2.18	114	9	0.90
s38417	367	24	2.00	87	10	1
s35932	39	24	2.67	12	7	1
s15850	203	24	2.40	97	8	0.89
s13207	276	24	2.18	235	7	0.70

the results. The parameters *NT*, *NSC*, *MSCL*, *MTPIN*, *NDO*, *NSI*, *NSI*/*MTPIN* and *CR* in the table are the same as the ones defined above. In order to demonstrate the effectiveness of using unspecified values, we ran another experiment that does not employ the procedure of unspecified value identification. The columns headed *w_X* and *wo_X* give results with using unspecified values and without using unspecified values, respectively.

By using the proposed method, the ratio *NSI*/*MTPIN* is less than 1 for all the circuits. Also, the proposed method can reduce the number of distinct decompressor output vectors *NDO*. For circuits such as s13207 with more than 8 scan chains and s38584 with more than 8 scan chains, *NDO* decreased to less than 3% of its value when the given test set without the suggested modifications is used. It can be seen that as the number of scan chains is increased, the number of scan inputs *NSI* needed approaches *MTPIN*. However the proposed modifications keep the number of distinct decompressor output vectors below that obtained when the proposed modifications are not used.

In Table III, we compare the method proposed in this work with that of Bayraktaroglu and Orailoglu [2001]. For this comparison we assume 200 internal scan chains as in Bayraktaroglu and Orailoglu [2001]. In Table III, we give for each method the number of tests (*NT*), the number of external scan inputs needed (*NSI*) and the ratio *NSI*/*MTPIN*. It can be seen that the proposed method needs considerably fewer external scan inputs and test data volume (*NT***NSI*) compared to the method of Bayraktaroglu and Orailoglu [2001]. Furthermore, the proposed method uses fewer tests and hence has a lower test application time. On the other hand, the decompressor may require relatively more hardware and it is necessary to synthesize it.

An additional observation to be made is that compared to the case of not using a decompressor the test data volume reductions are much higher. This can be noted from the last column of Table II, which shows the ratio of the number of external scan inputs and the number of internal scan chains. For the case of 200 internal scan chains given in Table III, the proposed method reduces the number of external scan inputs by a factor of 20 or more from 200 to at most 10.

In order to measure the effectiveness of iteration the procedure, we show results with iteration of the proposed method in Table IV. The columns "*wo_it*" and "*w_it*" show the results without iteration and with iteration, respectively. The method could reduce, on the average, *NDO* and *NSI* to approximately 62% and 90% of their values without iteration, respectively. The last two columns

Table IV. Experimental Result with Iteration

Circuit	*NSC*	*NDO*			*NSI*			#it	Time(sec)	
		wo_it	*w_it*	*w_it/wo_it*	*wo_it*	*w_it*	*w_it/wo_it*		*wo_it*	*w_it*
s5378	8	51	26	0.51	6	5	0.83	3	1.3	3.2
	16	100	45	0.45	7	6	0.86	5	1.3	5.3
	24	121	74	0.61	7	7	1	6	1.3	6.4
	32	141	141	1	8	8	1	2	1.3	1.7
s9234	8	47	36	0.77	6	6	1	3	3.2	7.5
	16	104	69	0.66	7	7	1	5	3.2	13.8
	24	143	103	0.72	8	7	0.88	6	3.2	17.0
	32	186	186	1	8	8	1	2	3.2	4.0
s13207	8	43	23	0.53	6	5	0.83	3	9.5	19 .1
	16	59	24	0.41	6	5	0.83	4	9.4	21.1
	24	64	29	0.45	7	5	0.71	4	9.4	31.3
	32	65	34	0.52	7	6	0.86	4	9.4	31.6
s15850	8	62	34	0.55	6	6	1	4	5.7	19.3
	16	130	54	0.42	8	6	0.75	5	5.7	24.3
	24	189	91	0.48	8	7	0.88	5	5.7	25.2
	32	215	117	0.54	8	7	0.88	6	5.7	30.6
s35932	8	100	87	0.87	7	7	1	5	5.3	24.0
	16	205	180	0.88	8	8	1	3	5.5	12.6
	24	95	93	0.98	7	7	1	3	5.6	12.7
	32	237	237	1	8	8	1	2	5.6	8.2
s38417	8	81	37	0.46	7	6	0.86	6	15.0	57.2
	16	218	124	0.57	8	7	0.88	4	15.0	53.0
	24	372	264	0.71	9	9	1	5	15.0	67.9
	32	447	343	0.77	9	9	1	6	15.1	83.9
s38584	8	75	29	0.39	7	5	0.71	4	19.2	51.3
	16	192	53	0.28	8	6	0.75	6	19.2	92.5
	24	290	99	0.34	9	7	0.78	10	19.2	158.6
	32	369	133	0.36	9	8	0.89	7	19.3	115.8
Average				0.62			0.90			

in Table IV show CPU time not including the time to generate the original test sets.

To determine the complexity of the decompressors used for the proposed method, we synthesized PLA implementations of the decompressor circuits. We first used NOVA to correlate decompressor input vectors with decompressor output vectors determined by the test data. This was followed by ESPRESSO. The number of product terms needed for different values of the number of internal scan chains for the benchmark circuits are given in Table V. For the case of 200 scan chains, the data is given for only the larger circuits used in Table III. From the data in Table V it can be seen that using iteration of the proposed procedure the size of the decompressors could be reduced, on the average, by approximately 68% of their size when iteration is not used.

5. CONCLUSIONS

In this article, we proposed a metric that captures the intrinsic test data volume reduction property of designs with multiple scan chains. This metric can be used to evaluate the compression achieved by test data volume reduction procedures. We also proposed a method of test volume reduction for multiple scan chain

Table V. PLA Sizes for Decompressor

Circuit	*NSC*	# of Product Terms		
		wo_it	*w_it*	*w_it/wo_it*
s5378	8	37	20	0.54
	16	98	37	0.38
	24	119	74	0.62
	32	139	139	1
s9234	8	34	28	0.82
	16	104	60	0.58
	24	140	102	0.73
	32	185	185	1
s13207	8	33	17	0.52
	16	58	20	0.34
	24	63	29	0.46
	32	65	32	0.49
	200	148	116	0.78
s15850	8	44	27	0.61
	16	128	49	0.38
	24	186	91	0.49
	32	214	117	0.55
	200	194	194	1
s35932	8	54	54	1
	16	188	159	0.85
	24	80	86	1.08
	32	227	227	1
	200	69	69	1
s38417	8	46	29	0.63
	16	214	121	0.57
	24	372	263	0.71
	32	446	337	0.76
	200	586	586	1
s38584	8	51	24	0.47
	16	189	48	0.25
	24	289	99	0.34
	32	361	133	0.37
	200	460	460	1
Average				0.68

designs. By modifying and encoding scan-in vectors of the circuit-under-test, the proposed method reduced the number of scan inputs to the decompressor circuit. Experimental results showed the effectiveness of the proposed method.

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