Reconfiguration Technique for Reducing Test Time and Test Data Volume in Illinois Scan Architecture Based Designs *

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Abstract

As the complexity of VLSI circuits is increasing due to the exponential rise in transistor count per chip, testing cost is becoming an important factor in the overall integrated circuit (IC) manufacturing cost. This paper addresses the issue of decreasing test cost by lowering the test data bits and the number of clock cycles required to test a chip. We propose a technique based on the reconfiguration of scan chains to reduce test time and test data volume for Illinois Scan Architecture (ILS) based designs. This technique is presented with details of hardware implementation as well as the test generation and test application procedures. The reduction in test time and test data volume achieved using this technique is quite significant in most circuits.

1 Introduction

Testing cost is becoming an important factor in the overall integrated circuit (IC) manufacturing cost due to the exponential increase in transistor count per chip as predicted by Moore's Law. Transistor feature sizes on a VLSI chip reduce roughly by 10.5% per year, resulting in a transistor density increase of approximately 22.1% every year. Also an equal amount of increase is usually provided by wafer and chip size increases as well as circuit design and process innovations [1]. This increases the complexity of test and increases the testing costs incurred by test pattern generation and test application process. With the increasing complexity of circuits today, the automatic test equipment (ATE) needed to test these circuits is getting more costly. The cost of such ATE rises at the rate of thousands of dollars per pin [2]. In this paper, we address the issue of decreasing test cost by lowering the test data bits and the number of clock cycles required to test a chip.

A structured test technique like the full scan is widely used in the industry to achieve high coverage and to reduce the complexity of test generation by making all memory elements in the circuit both controllable and observable through a scan chain. The full scan technique involves controlling (observing) the memory elements by serially shifting in (out) the values to (from) the flip-flops. This serial access mechanism increases the test application time.

Many improvements to the test application time for full scan circuits have been suggested in the literature. Hybrid test generation schemes [3, 4, 5] are computationally expensive and are not applicable in case of large sequential circuits. The parallel loading technique through parallel direct access to all scan inputs and outputs [6] greatly reduces test application time, but is impractical due to high hardware overhead. Other techniques involve using multiple scan chains [7, 4] done by dividing the scan chain into multiple partitions and shifting each test vector in parallel. This requires additional input/output pins or the use of multiplexers, which degrades the performance of the circuit. A method suggesting the reordering of memory elements in a scan chain can reduce the test application time to some extent [8]. Similarly, several test data volume reduction techniques have also been suggested in the literature. A recently introduced technique utilizes a hybrid of automatic test pattern generation (ATPG) and built-in-self-test (BIST) to reduce data volume [9]. Another technique involves hybrid BIST based on weighted pseudo-random testing [10]. A technique based on compression/decompression using virtual scan chain has also been suggested [11]. Most of these techniques suggested in the literature do not address the needs for embedded cores used in SOC designs. Some of the work applicable to SOC designs involves the use of sophisticated compression schemes [12]. Therefore, a new architecture called the Illinois Scan Architecture (ILS) was

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recently proposed to accommodate the needs of embedded cores [13]. ILS is applicable to both standalone chips or chips used as embedded cores. When used in cores, this scheme is attractive because it does not require any additional test pins other than the ones used in scan. So far there has not been any thorough research involving ILS designs and techniques to improve ILS. In this paper, we propose a technique based on the reconfiguration of scan chains to reduce test time and test data volume for ILS based designs. This technique is presented with hardware implementation details as well as the test generation and test application procedures.

2 Introduction to Illinois scan architecture

The Illinois Scan Architecture (ILS) was first introduced in [13]. An overview of this architecture will be provided here.

The ILS consists of two modes of operation. The first mode is called the *broadcast scan mode* and the second mode is called the *serial scan mode*. Figure 1 diagrammatically represents this architecture. The top portion of this figure shows a normal scan chain in the serial scan mode while the bottom shows the broadcast scan mode. The ILS divides a scan chain into multiple segments and shifts in the same vector to each of the parallel scan chains through a single scan-in input. For example, in case of a scan chain of length 100 that would be split into four parallel chains, the flops 1, 26, 51, and 76 would be positioned such that they would receive identical scan-in data. Similarly, flops 2, 27, 52, and 77 would also receive identical scan-in data. This shared scan-in idea is similar to an earlier work where a single input was used to support multiple scan chains [14]. However, its application is limited to testing multiple independent full scan circuits in parallel. In ILS, the outputs of the scan chains are compressed into a multiple input signature analyzer (MISR). This is similar to the signature calculation mechanism in a full logic BIST implementation such as STUMPS [15]. Due to the use of a MISR, violation of certain design rules must be avoided. Such rules are avoiding unknown states, internal bus conflicts, and other violations that can corrupt the signature. The use of a MISR for compression may cause a slight decrease in fault coverage due to aliasing. The implementation of ILS does not require any additional test access pins other than the ones used in full scan technique, i.e., scan in, scan out, and test enable pins. The additional logic required to implement ILS consists of several multiplexers used to switch between two modes of operation and some control logic. The area overhead of these logic blocks is typically quite small compared to the overall chip area.

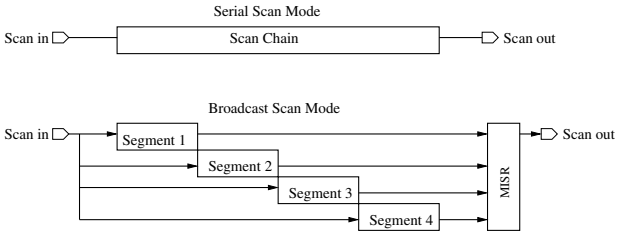

Figure 1. Two Modes of Illinois Scan Architecture

2.1 Testing with ILS

A scan-based automatic test pattern generator (ATPG) is used to generate test vectors for all faults in the broadcast mode of ILS. Since the broadcast mode imposes logic constraints on test patterns due to the placement of flip-flops in parallel chains, many faults become untestable. To cover these untestable faults, ATPG is again used, but time under the serial scan mode of ILS. The additional serial scan vectors cover the testable faults that were rendered untestable under broadcast mode.

Illinois Scan based designs are very effective in reducing both the test application time and test data volume [13]. In addition, a case study of industrial circuits has also shown the effectiveness of Illinois scan architecture [16]. These results have shown that since the cost of a serial pattern is many times higher than the cost of a broadcast pattern, it is desirable to keep the number of serial patterns low. Earlier work in reducing the number of serial patterns was done by optimally reordering the scan chain elements such that number of untestable faults in the broadcast mode is reduced [13]. However, reordering a scan chain requires changing the place and route information for the flops in the circuit which is very costly and may impact the functional timing of the circuit [17]. Therefore, in order to avoid this overhead, we present a reconfigurable technique that reduces the number of serial patterns by switching dynamically between two different ILS configurations. The proposed technique does not change the placement of flip-flops in the circuit so no penalty is incurred in terms of routing. By reducing the serial patterns, this technique is able to further reduce both the test data volume and test application time for a chosen ILS configuration. It should be noted that the reconfigurable technique can achieve considerable reduction in test time only in cases where the number of serial vectors needed to cover all the testable faults is large. This often might be the case when the number of parallel chains is large. In some cases, if the designer has already reached a target fault coverage goal with only the basic ILS broadcast patterns, then the reconfiguration technique may not even be required. However, we present this novel technique as a way to tackle cases where the number of serial vectors

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needed to cover the hard to detect faults is large because of a high fault coverage goal. In this paper, we do not present any fault coverage numbers because the purpose of reconfigurable ILS is not to increase fault coverage. We assume in our experimentation that the goal is to detect 100% of all detectable faults.

3 Reconfigurable Illinois scan architecture

In this section, the theoretical basis of Illinois scan architecture is discussed first, then the hardware implementation and the test generation procedure is described.

3.1 ILS-k organization

Let there be a scan chain with N flip-flops and the flip-flops be numbered 1, 2, ... , N from first to last. In an ILS-k organization, each scan segment consists of k flip-flops except the last one, which may contain less than k flip-flops. Figure 2 shows an ILS-k organization.

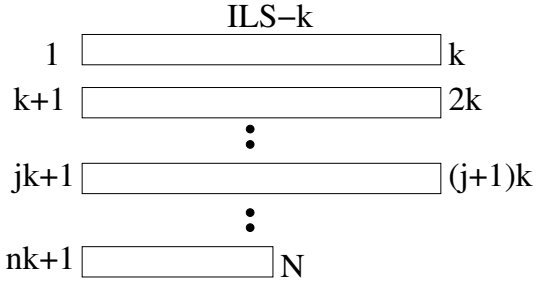

Figure 2. ILS-k Organization

In Figure 2, there are a total of n scan chain segments, $n-1$ of them are of length k, and the nth chain may be of length less than k. The scan chain is systematically divided such that a flip-flop j is placed in segment position q, where $j \equiv q$ mod k. Therefore, in the broadcast mode, two flip-flops i and j are lined up to receive the same logic values iff $i \equiv j$ mod k. Now we present the following theorem:

Theorem 1 *If k and m are relatively prime, and the number of flip-flops is less than km, then signal constraints of ILS-k and ILS-m are disjoint.*

Proof: We prove the theorem by contradiction. Assume two flip-flops i and j exist such that $i \equiv j$ mod k and $i \equiv j$ mod m. Therefore, i-j = nk and i-j = lm for some integers n and l. Therefore,

$$nk = lm$$
$$n = \frac{lm}{k}$$

Hence, k divides lm. Since k and m are relatively prime, there are no common factors between k and m. Therefore, k must divide $l \cdots (1)$

Now, consider i-j = lm. Since the number of flip-flops is less than km, $i <$ km and $j < km$, and hence the difference i-$j < km$. Therefore,

$$lm < km$$
$$l < k \cdots (2)$$

(1) and (2) cannot be both true, hence a contradiction. Therefore, no two flip-flops i and j satisfy both $i \equiv j$ mod k and $i \equiv j$ mod m. In the above theorem, the term *signal constraint* refers to the constraint put on the ATPG tool due to the signal assignments in the circuit, such that flip-flops in parallel chains are lined up to receive identical scan-in data.

3.2 Reconfigurable organization

The reconfigurable Illinois scan organization is diagramatically shown in Figure 3. In this figure, two organizations, ILS-k and ILS-(k+1), are shown. Since k and k+1 are relatively prime, according to Theorem 1, no signal constraints are common between ILS-k and ILS-(k+1). The maximum chain length k is chosen after running the incremental algorithm proposed in our earlier work in [18] and choosing the optimal configuration. It should be noted here that although any two relatively prime numbers can be chosen for reconfiguration, choosing k and k+1 makes the most sense because they both are structurally very close to the optimal configuration.

In Figure 3, the ILS-k organization consists of n parallel scan chains, each of length k. The ILS-(k+1) organization consists of m parallel scan chains, each of length k+1. The reconfigurable architecture is designed such that the switching between these two modes of operation can be done with a simple control. The main idea behind using this technique is that since the signal constraints of ILS-(k+1) is disjoint from the signal constraints of ILS-k, some of the faults that are undetectable in the broadcast mode of ILS-k can be detected in the broadcast mode of ILS-(k+1). This effect of reducing the number of undetectable faults is evident in Table 1. The columns in this table presents the circuit name, the length of the longest chain in ILS-k configuration, additional redundant faults in ILS-k, faults detected after switching to ILS-(k+1) mode, and the remaining redundant faults after ILS-k and ILS-(k+1) are combined. In this table, the columns 3 and 5 show the faults that are undetectable after applying all the broadcast patterns in ILS-k and ILS-(k+1) configurations, respectively. The difference between these two columns gives the number of faults that were undetectable in ILS-k mode and detected in ILS-(k+1) mode. All the faults that are redundant after ILS-(k+1) configurations are covered by serial patterns. For example, circuit s13207 has 179 faults redundant after ILS-50, and 154

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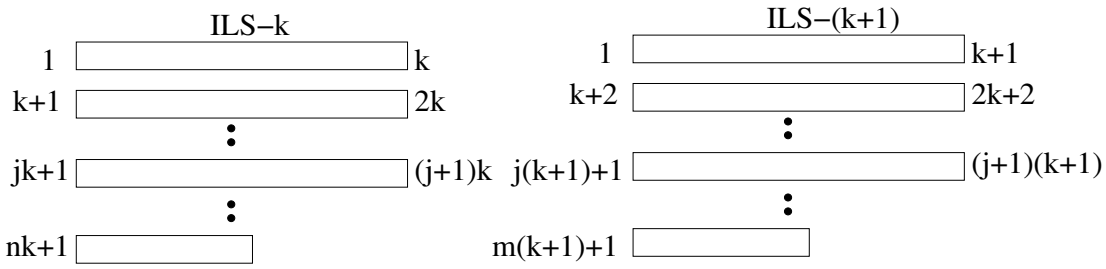
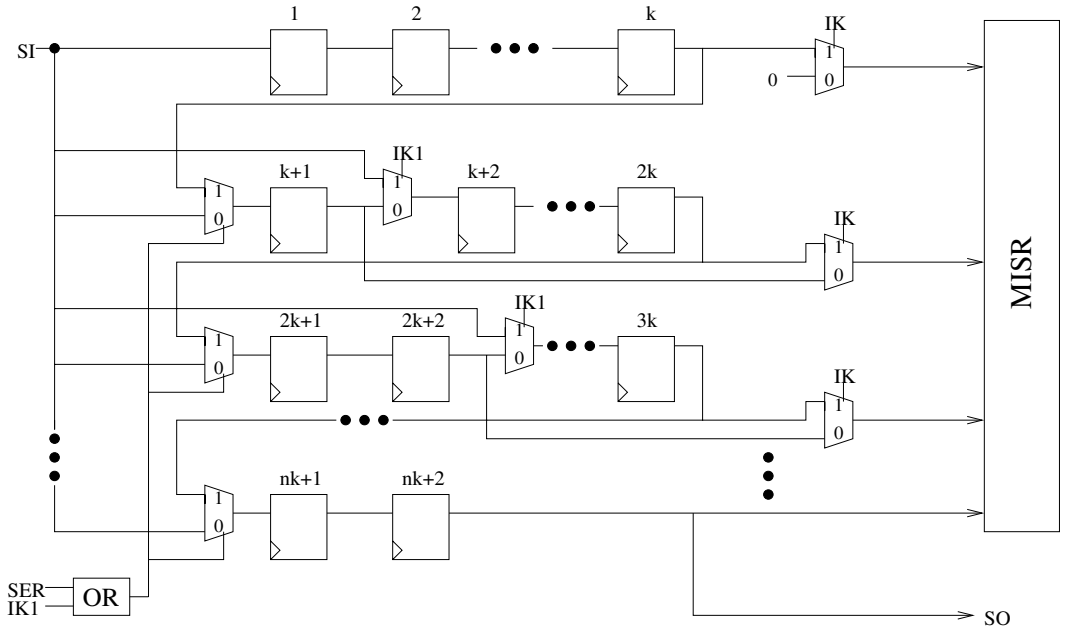
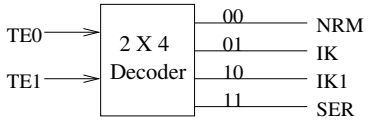


Figure 3. Reconfigurable Illnois Scan



(a)



(b)

Figure 4. Reconfigurable Illnois Scan Architecture

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Table 1. Redundant Faults in ILS-k and ILS-(k+1)

Circuit	ILS k	Add Red ILS-k	Faults Det	Rem Add Red
s13207	50	179	154	25
	180	130	28	102
s15850	75	74	47	27
	100	133	116	17
s38417	105	52	39	13
	210	40	29	11
s38584	100	208	153	55
	128	163	150	13

of these faults are detected in ILS-51. Only 25 remaining faults need serial patterns. Without reconfiguration, all 179 faults would have required serial patterns. This shows that the reconfiguration technique is very effective in reducing serial patterns. Previously, all the undetectable faults in ILS-k organization were covered by serial patterns only.

3.3 Hardware implementation and test application procedure

The architecture of a reconfigurable Illinois scan system is shown in Figure 4. Figure 4(a) shows the scan chain design. Figure 4(b) shows the generation of control signals used in Figure 4(a). This figure only shows the additional circuitry needed to implement the reconfiguration. It does not show the multiplexers that are present in a conventional scan environment to switch between the normal and test modes of operation. A low hardware overhead of mainly multiplexers is required. There are four modes of operation in the proposed reconfigurable architecture. The operation of this architecture is controlled by the two inputs $TE0$ and $TE1$. Signals $TE0$ and $TE1$ are decoded into four signals each one of which indicates a particular mode of operation. When signal $TE0$ and $TE1$ are both 0, signal *NRM* is asserted, which indicates the *normal mode* of operation. The operation of this circuit in the normal mode is the same as a full scan circuit in normal mode. When signal $TE0$ is 1 and $TE1$ is 0, signal *IK* is asserted, which indicates the *broadcast ILS-k mode* of operation. Here the length of all the parallel scan chains, except the last one, is of length k. When $TE0$ is 0 and $TE1$ is 1, signal *IK1* is asserted, which indicates *broadcast ILS-(k+1) mode* of operation. In this mode, the length of all the parallel scan chains, except the last one, is of length k+1. In both of the broadcast test modes, the input values are shifted into all the scan chains in parallel. In the broadcast test mode, the outputs from the flip-flops are shifted into a multiple input signature analyzer (MISR) for compression. Finally, when both $TE0$ and $TE1$ are 1, signal *SER* is asserted, which indicates the *serial mode* of operation. The operation of the ILS design in the serial test mode is the same as the operation of full scan circuits in the test mode, i.e., the new logic values are serially shifted in through the SI input, and shifted out serially through the SO output. The MISR is not used during the serial test mode.

The test application process for a reconfigurable ILS architecture is shown in Figure 5. In this figure, F is the number of flip-flops, L is the length of the MISR and C_k and C_{k+1} are the number of flip-flops in the longest scan chain in ILS-k and ILS-(k+1) broadcast test mode, respectively. Signals *NRM*, *IK*, *IK1* and *SER* are the decoder outputs shown in Figure 4. The steps 1-5 are used to apply the broadcast test vectors and observe their response in ILS-k organization. The steps 6-10 are used to apply the broadcast test vectors and observe their response in ILS-(k+1) organization. Finally, steps 11-15 are used to apply the serial test vectors and observe their responses. The final signature that is stored in the MISR, is observed in both steps 5 and 10 during the last L clock pulses through the output of the MISR.

3.4 Test generation procedure

The test generation procedure for the reconfigurable ILS design is shown in Figure 6. First, a set of broadcast patterns B_k is generated for ILS-k organization. Then patterns B_{k+1} is generated for the ILS-(k+1) organizations using the remaining undetected faults. Finally, serial patterns S is generated for the faults that were undetected in both ILS-k and ILS-(k+1) organizations. Then reverse fault simulation is performed for compaction of test sets S, B_k and B_{k+1}. The final test set is an union of sets S, B_k and B_{k+1}.

4 Experimental results

Experiments using the reconfigurable technique were carried out for four different ISCAS89 benchmark circuits [19]. Table 2 shows the test application time and test data volume requirement after using the reconfigurable ILS architecture. The columns in this table presents the circuit name, the length of the longest chain in the ILS-k configuration, the length of the longest chain in the ILS-(k+1) configuration, the number of broadcast patterns required in ILS-k configuration, the number of broadcast patterns required in ILS-(k+1) configuration, the number of serial patterns, the total test data bits required, the total test application time required in cycles, the test data volume reduction without reconfiguration, the test data volume reduction with reconfiguration, the test application time reduction without reconfiguration, and the test application time reduction with

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1. Assert signal *IK*. Shift in the broadcast test vector by applying C_k clock pulses.
2. Assert signal *NRM*, apply the primary input values, and after the combinational delay of the circuit, apply a clock pulse. This captures the test response in the flip-flops.
3. If all broadcast test vectors are applied, then go to step 5.
4. Assert signal *IK*, and shift in the next broadcast test vector and shift out the test response simultaneously by applying C_k clock pulses. Go to step 2.
5. Assert signal *IK*, and shift out the test response by applying (C_k + L) clock pulses.
6. Assert signal *IK1*. Shift in the broadcast test vectors by applying C_{k+1} clock pulses.
7. Assert signal *NRM*, apply the primary input values, and after the combinational delay of the circuit, apply a clock pulse. This captures the test response in the flip-flops.
8. If all broadcast test vectors are applied, then go to step 10.
9. Assert signal *IK1*, and shift in the next broadcast test vector and shift out the test response simultaneously by applying C_{k+1} clock pulses. Go to step 7.
10. Assert signal *IK1*, and shift out the test response by applying (C_{k+1} + L) clock pulses.
11. Assert signal *SER*. Shift in the serial test vectors by applying F clock pulses.
12. Assert signal *NRM*, apply the primary input values, and after the combinational delay of the circuit, apply a clock pulse. This caputures the test response into the flip-flops.
13. If all serial vectors are applied, go to step 15.
14. Assert signal *SER*, and shift in the next serial test vector and shift out the test response simultaneously by applying F clock pulses. Go to step 12.
15. Assert signal *SER*, and shift out the test response by applying F clock pulses.

Figure 5. Test Application Process

1. Let f_B be the set of complete faults in the circuit
2. Set logic constraints for ILS-k
3. For target fault set f_B, generate broadcast patterns B_k and let U_{B_k} be the set of undetected faults.
4. Set logic constraints for ILS-(k+1)
5. For target fault set U_{B_k}, generate broadcast patterns B_{k+1} and let $U_{B_{k+1}}$ be the set of undetected faults.
6. For the target fault set $U_{B_{k+1}}$, generate serial patterns S.
7. Fault simulate in reverse order the test sets S, B_{k+1} and B_k to obtain a compact test set.

Figure 6. Test Generation Procedure for Reconfigurable ILS

reconfiguration. All numbers for test patterns are after compaction using reverse fault simulation. The pattern generation was done using an efficient automatic test pattern generation system for combinational circuits called ATOM [20, 21].

Comparing the serial patterns required in Table 2 to the one presented in [18], it can be seen that the number of serial patterns is significantly reduced. For example, in circuit s38584, the number of serial patterns required in the basic ILS-128 configuration is 46, whereas in the reconfigurable ILS-128 configuration, it is 5. As explained previously, the reduction in the number of serial patterns is because the constraints in ILS-(k+1) configuration is disjoint from the constraints in ILS-k. This allows the faults that were undetected in ILS-k, to be detected in ILS-(k+1). Total number of vectors required is similar in both reconfigurable and non-reconfigurable designs. However, since serial patterns are many times more costly than broadcast patterns, the reduction in serial patterns results in overall improvement of both test data volume and time. In this table, 'Orig' refers to the original ILS-k circuit without reconfiguration and 'Reconf' refers to the reconfigurable circuit that combines ILS-k and ILS-(k+1). This table also shows the improvement in test data volume and test application time. The reduction factor was obtained from dividing the data (time) required in conventional full scan by the data (time) required in a particular ILS configuration. In many cases, the improvement is significant.

5 Conclusion

In this paper, we presented a new technique to reduce test data volume and test application time by the reconfiguration of scan chains in ILS designs. The proposed technique utilizes a low hardware overhead. We presented the

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Table 2. Results for Test Data Volume and Test Application Time

Circuit	Max Length ILS (k)	Max Length ILS (k+1)	Broadcast Patterns k	Broadcast Patterns k+1	Ser Patt	Test Data (bits)	Test Time (cycles)	Test Data Reduction Orig	Test Data Reduction Reconf	Test Time Reduction Orig	Test Time Reduction Reconf
s13207	50	51	390	39	13	106067	31398	4.46	6.67	5.60	10.16
	180	181	447	5	19	178379	94547	3.76	3.97	3.20	3.37
s15850	75	76	407	16	14	126243	40536	4.33	4.77	5.55	6.48
	100	101	412	13	7	127767	47922	4.21	4.71	4.81	5.49
s38417	105	106	737	22	8	208671	93572	10.81	15.39	11.22	16.50
	210	211	811	13	8	310717	186973	8.95	10.34	7.31	8.26
s38584	100	101	569	40	26	320594	99327	4.51	6.17	5.71	9.06
	128	129	600	36	5	281854	89345	5.04	7.01	6.25	10.07

test generation procedure as well as detailed test application procedure for implementing this technique. The experimental data for several of the ISCAS89 circuits show that this technique significantly reduces both the test application time and the test data volume in addition to the reduction provided by the basic ILS design. The reduction mainly comes from a decrease in the number of serial patterns required, and therefore, this technique is highly useful in circuits where a large number of serial vectors is needed to achieve the fault coverage goal.

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