



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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## FSP OVERVIEW

# FSP Overview

## 2.1 Technical Overview

The *Intel® Firmware Support Package (FSP)* provides chipset and processor initialization in a format that can easily be incorporated into many existing boot loaders.

The FSP will perform the necessary initialization steps as documented in the BWG including initialization of the CPU, memory controller, chipset and certain bus interfaces, if necessary.

FSP is not a stand-alone boot loader; therefore it needs to be integrated into a host boot loader to carry out other boot loader functions, such as: initializing non-Intel components, conducting bus enumeration, and discovering devices in the system and all industry standard initialization.

The FSP binary can be integrated easily into many different boot loaders, such as Coreboot, EDKII etc. and also into the embedded OS directly.

Below are some required steps for the integration:

- **Customizing** The static FSP configuration parameters are part of the FSP binary and can be customized by external tools that will be provided by Intel.
- **Rebasing** The FSP is not Position Independent Code (PIC) and the whole FSP has to be rebased if it is placed at a location which is different from the preferred address during build process.
- **Placing** Once the FSP binary is ready for integration, the boot loader build process needs to be modified to place this FSP binary at the specific rebasing location identified above.
- **Interfacing** The boot loader needs to add code to setup the operating environment for the FSP, call the FSP with correct parameters and parse the FSP output to retrieve the necessary information returned by the FSP.

## 2.2 FSP Distribution Package

- The FSP distribution package contains the following:
  - FSP Binary
  - FSP Integration Guide
  - BSF Configuration File
  - Data Structure Header File
- The FSP configuration utility called BCT is available as a separate package. It can be downloaded from link mentioned in Section 1.3.

### 2.2.1 Package Layout

- **Docs (Auto generated)**
  - CoffeeLake\_FSP\_Integration\_Guide.pdf
  - CoffeeLake\_FSP\_Integration\_Guide.chm
- **Include**
  - **FsptUpd.h**, **FspmUpd.h** and **FspUpd.h** (FSP UPD structure and related definitions)
  - **GpioSampleDef.h** (Sample enum definitions for Gpio table)
- CoffeeLakeFspBinPkg.dec (EDKII declaration file for package)
- Fsp.bsf (BSF file for configuring the data using BCT tool)
- Fsp.fd (FSP Binary)

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## FSP INTEGRATION

# 3 FSP Integration

## 3.1 Assumptions Used in this Document

The FSP for the CoffeeLake platform is built with a preferred base address given by **PcdFspAreaBaseAddress** and so the reference code provided in the document assumes that the FSP is placed at this base address during the final boot loader build. Users may rebase the FSP binary at a different location with Intel's Binary Configuration Tool (BCT) before integrating to the boot loader.

For other assumptions and conventions, please refer section 8 in the FSP External Architecture Specification version 2.0.

## **3.2 Boot Flow**

Please refer Chapter 7 in the FSP External Architecture Specification version 2.0 for Boot flow chart.

### **3.3 FSP INFO Header**

The FSP has an Information Header that provides critical information that is required by the bootloader to successfully interface with the FSP. The structure of the FSP Information Header is documented in the FSP External Architecture Specification version 2.0 with a HeaderRevision of 3.

## 3.4 FSP Image ID and Revision

FSP information header contains an Image ID field and an Image Revision field that provide the identification and revision information of the FSP binary. It is important to verify these fields while integrating the FSP as API parameters could change over different FSP IDs and revisions. All the FSP FV segments(FSP-T, FSP-M and FSP-S) must have same FSP Image ID and revision number, using FV segments with different revision numbers in a single FSP image is not valid. The FSP API parameters documented in this integration guide are applicable for the Image ID and Revision specified as below.

The FSP ImageId string in the FSP information header is given by **PcdFspImageIdString** and the ImageRevision field is given by **SiliconInitVersionMajor|Minor|FspVersionRevision|FspVersionBuild** (Ex:0x07020110).

## 3.5 FSP Global Data

FSP uses some amount of TempRam area to store FSP global data which contains some critical data like pointers to FSP information headers and UPD configuration regions, FSP/Bootloader stack pointers required for stack switching etc. HPET Timer register(2) **PcdGlobalDataPointerAddress** is reserved to store address of this global data, and hence boot loader should not use this register for any other purpose. If TempRAM initialization is done by boot loader, then HPET has to be initialized to the base so that access to the register will work fine.

## 3.6 FSP APIs

This release of the CoffeeLake FSP supports the all APIs required by the FSP External Architecture Specification version 2.0. The FSP information header contains the address offset for these APIs. Register usage is described in the FSP External Architecture Specification version 2.0. Any usage not described by the specification is described in the individual sections below.

The below sections will highlight any changes that are specific to this FSP release.

### 3.6.1 TempRamInit API

Please refer Chapter 8.5 in the FSP External Architecture Specification version 2.0 for complete details including the prototype, parameters and return value details for this API.

TempRamInit does basic early initialization primarily setting up temporary RAM using cache. It returns ECX pointing to beginning of temporary memory and EDX pointing to end of temporary memory + 1. The total temporary ram currently available is given by **PcdTemporaryRamSize** starting from the base address of **PcdTemporaryRamBase**. Out of total temporary memory available, last **PcdFspReservedBufferSize** bytes of space reserved by FSP for TempRamInit if temporary RAM initialization is done by FSP and remaining space from **TemporaryRamBase(ECX)** to **TemporaryRamBase+TemporaryRamSize-FspReservedBufferSize(EDX)** is available for both bootloader and FSP binary.

TempRamInit\*\* also sets up the code caching of the region passed CodeCacheBase and CodeCacheLength, which are input parameters to TempRamInitApi. If 0 is passed in for CodeCacheBase, the base used will be 4 GB - 1 - length to be code cached instead of starting from CodeCacheBase.

#### Note

: when programming MTRR CodeCacheLength will be reduced, if SKU LLC size is smaller than the requested.

It is a requirement for Firmware to have Firmware Interface Table (FIT), which contains pointers to each microcode update. The microcode update is loaded for all logical processors before reset vector. If more than microcode update for the CPU is present, the microcode update with the latest revision is loaded.

**FSPT\_UPD.MicrocodeRegionBase\*\*** and **FSPT\_UPD.MicrocodeRegionLength** are input parameters to TempRamInit API. If these values are 0, FSP will not attempt to update microcode. If a region is passed, then if a newer microcode update revision is in the region, it will be loaded by the FSP.

MTRRs are programmed to the default values to have the following memory map:

Memory range	Cache Attribute
0xEF00000 - 0x00040000	Write back
CodeCacheBase - CodeCacheLength	Write protect

### 3.6.2 FspMemoryInit API

Please refer to Chapter 8.6 in the FSP external Architecture Specification version 2.0 for the prototype, parameters and return value details for this API.

The **FspmUpdPtr** is pointer to **FSPM\_UPD** structure which is described in header file **FspmUpd.h**.

Boot Loader must pass valid CAR region for FSP stack use through **FSPM\_UPD.FspmArchUpd.StackBase** and **FSPM\_UPD.FspmArchUpd.StackSize** UPDs.

The minimum FSP stack size required for this revision of FSP is 160KB, stack base is 0xEF17F00 by default.

The base address of HECI device (Bus 0, Device 22, Function 0) is required to be initialized prior to perform FspMemoryInit flow. The default address is programmed to 0xFED1A000.

Calculate memory map determining memory regions TSEG, IED, GTT,

BDSM, ME stolen, Uncore PMRR, IOT, MOT, DPR, REMAP, TOLUD, TOUUD. Programming will be done at a different time.

### 3.6.3 TempRamExit API

Please refer to Chapter 8.7 in the FSP external Architecture Specification version 2.0 for the prototype, parameters and return value details for this API.

If Boot Loader initializes the Temporary RAM (CAR) and skip calling **TempRamInit API**, it is expected that bootloader must skip calling this API and bootloader will tear down the temporary memory area setup in the cache and bring the cache to normal mode of operation.

This revision of FSP doesn't have any fields/structure to pass as parameter for this API. Pass Null for *TempRamExitParamPtr*.

At the end of *TempRamExit* the original code and data caching are disabled. FSP will reconfigure all MTRRs as described in the table below for performance optimization.

Memory range	Cache Attribute
0x00000000 - 0x0009FFFF	Write back
0x000C0000 - Top of Low Memory	Write back
0xFF000000 - 0xFFFFFFFF (Flash region)	Write protect

#### **Todo:**

program 0x1000000000 - Top of High Memory | Write back

If the boot loader wish to reconfigure the MTRRs differently, it can be overridden immediately after this API call.

### 3.6.4 FspSiliconInit API

Please refer to Chapter 8.8 in the FSP external Architecture Specification version 2.0 for the prototype, parameters and return value details for this API.

The *FspSiliconInit* is pointer to **FSPS\_UPD** structure which is described

in header file **FspUpd.h**.

It is expected that boot loader will program MTRRs for SBSP as needed after **TempRamExit** but before entering **FspSiliconInit**. If MTRRs are not programmed properly, the boot performance might be impacted.

The region of 0x5\_8000 - 0x5\_8FFF is used by FspSiliconInit for starting APs. If this data is important to bootloader, then bootloader needs to preserve it before calling FspSiliconInit.

It is a requirement for bootloader to have Firmware Interface Table (FIT), which contains pointers to each microcode. The microcode is loaded for all cores before reset vector. If more than one microcode update for the CPU is present, the latest revision is loaded.

`MicrocodeRegionBase` and `MicrocodeRegionLength` are both input parameters to `TempRamInit` and UPD for `SiliconInit` API. UPD has priority and will be searched for a later revision than `TempRamInit`. If `MicrocodeRegionBase` and `MicrocodeRegionLength` values are 0, FSP will not attempt to update the microcode. If a microcode region is passed, and if a later revision of microcode is present in this region, FSP will load it.

FSP initializes PCH audio including selecting HD Audio verb table and initializes Codec.

PCH required initialization is done for the following HECI, USB, HSIO, Integrated Sensor Hub, Camera, PCI Express, Vt-d.

FSP initializes CPU features: XD, VMX, AES, IED, HDC, x(2)Apic, Intel® Processor Trace, Three strike counter, Machine check, Cache pre-fetchers, Core PMRR, Power management.

Initializes HECI, DMI, Internal Graphics. Publish `EFI_PEI_GRAPHICS_INFO_HOB` during normal boot but this HOB will not be published during S3 resume as FSP will not launch the PEI Graphics PEIM during S3 resume.

Programs SA Bars: MchBar, DmiBar, EpBar, GdxcBar, EDRAM (if supported). Please refer to section 2.8 (MemoryMap) for the

corresponding Bar values. GttMmadr (0x<sub>DF</sub>000000) and GmAdr(0xC0000000) are temporarily programmed and cleared after use in FSP.

### **3.6.5 NotifyPhase API**

Please refer Chapter 8.9 in the FSP External Architecture Specification version 2.0 for the prototype, parameters and return value details for this API.

#### **3.6.5.1 PostPciEnumeration Notification**

This phase *EnumInitPhaseAfterPciEnumeration* is to be called after PCI enumeration but before execution of third party code such as option ROMs. Currently, nothing is done in this phase, but in the future updates, programming may be done in this phase.

#### **3.6.5.2 ReadyToBoot Notification**

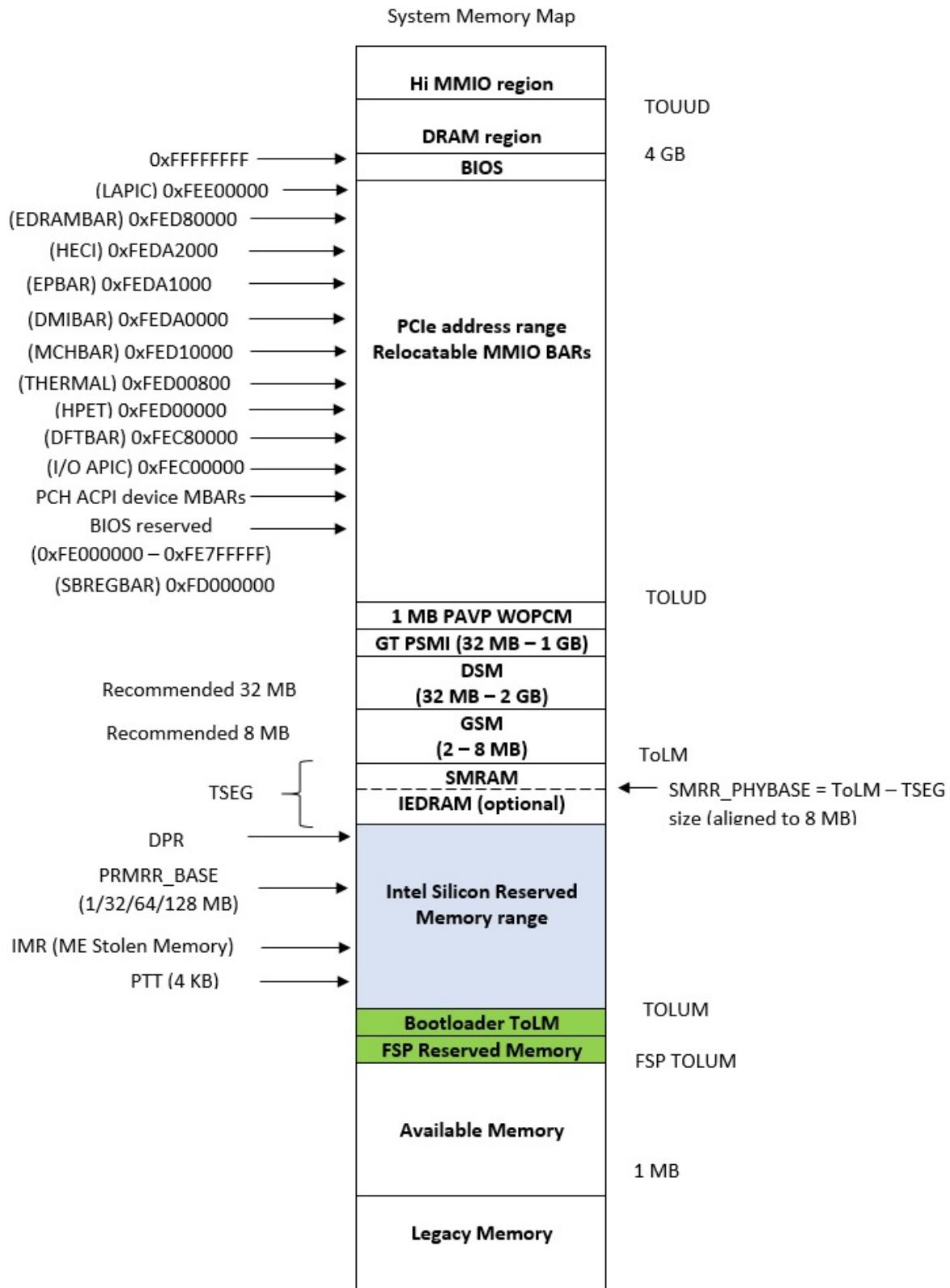
This phase *EnumInitPhaseReadyToBoot* is to be called before giving control to boot. It includes some final initialization steps recommended by the BWG, including power management settings, Send ME Message EOP (End of Post).

#### **3.6.5.3 EndOfFirmware Notification**

This phase *EnumInitEndOfFirmware* is to be called before the firmware/preboot environment transfers management of all system resources to the OS or next level execution environment. It includes final locking of chipset registers

## **3.7 Memory Map**

Below diagram represents the memory map allocated by FSP including the FSP specific regions.



**System Memory Map**

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## FSP PORTING RECOMMENDATION

# **4 FSP Porting Recommendation**

Here listed some notes or recommendation when porting with FSP.

## 4.1 Locking PAM register

FSP 2.0 introduced EndOfFirmware Notify phase callback which is a recommended place for locking PAM registers so FSP by default implemented this way. If it is still too early to lock PAM registers then the PAM locking code inside FSP can be disabled by UPD -> **FSP\_S\_TEST\_CONFIG** -> SkipPamLock or SA policy -> **\_SI\_PREMEM\_POLICY\_STRUCT** -> **SA\_MISC\_PEI\_CONFIG** -> SkipPamLock, and platform or wrapper code should do the PAM locking right before booting OS (so do it outside FSP instead) by programming one PCI config space register as below.

This PAM locking step has to been applied in all boot paths including S3 resume. To lock PAM register:

```
MmioOr32 (B0: D0: F0: Register 0x80, BIT0)
```

## 4.2 Locking SMRAM register

Since SMRAM locking is recommended to be locked before any 3rd party OpROM execution and highly depending on platform code implementation, the FSP code by default will not lock it. The platform or FSP Wrapper code should lock SMRAM by below programming step before any 3rd partiy OpRom execution (and should be locked in S3 resume right before OS waking vector).

```
PciOr8 (B0: D0: F0: Register 0x88, BIT4); Note: it  
must be programmed by CF8/CFC Standard PCI  
access mechanism. (MMIO access will not work)
```

## **4.3 Locking SMI register**

Global SMI bit is recommended to be locked before any 3rd party OpROM execution and highly depending on platform code implementation after SMM configuration. FSP by default will not lock it. Boot loader is responsible for locking below registers after SMM configuration. Set AcpiBase + 0x30[0] to 1b to enable global SMI. Set PMC PCI offset A0h[4] = 1b to lock SMI.

## 4.4 Verify below settings are correct for your platforms

PMC PciCfgSpace is not PCI compliant. FSP will hide the PMC controller to avoid external software or OS from corrupting the BAR addresses. FSP will program the PMC controller IO and MMIO BAR's with below addresses. Please use this address in the wrapper code instead of reading from PMC controller.

Register	Values
ABASE	0x1800
PWRMBASE	0xFE000000
PCIEXBAR_BASE_ADDRESS	0xE0000000

### Note

- Boot Loader can use different value for PCIEXBAR\_BASE\_ADDRESS either by modifying the UPD (under FSP-T) or by overriding the PCIEXBAR (B0:D0:F0:R60h) before calling FspMemoryInit Api.
- Boot Loader should avoid using conflicting address when reprogramming PCIEXBAR\_BASE\_ADDRESS than the recommended one.

## 4.5 FSP\_STATUS\_RESET\_REQUIRED

As per FSP External Architecture Specification version 2.0, Any reset required in the FSP flow will be reported as return status FSP\_STATUS\_RESET\_REQUIREDx by the API. It is the bootloader responsibility to reset the system according to the reset type requested.

Below table specifies the return status returned by FSP API and the requested reset type.

FSP_STATUS_RESET_REQUIRED Code	Reset Type requested
0x40000001	Cold Reset
0x40000002	Warm Reset
0x40000003	Global Reset - Puts the system to Global reset through Heci or Full Reset through PCH
0x40000004	Reserved
0x40000005	Reserved
0x40000006	Reserved
0x40000007	Reserved
0x40000008	Reserved

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## **UPD PORTING GUIDE**

# 5 UPD porting guide

UPD porting guide:

UPD	Dependency	Description
EnableSgx	CoffeeLake Platform	Temporary workarounds
PchTraceHubMode	CoffeeLake Pch A0	BIOS workarounds for Trace power gate issue on A0
PchTraceHubMemReg0Size	CoffeeLake Pch A0	BIOS workarounds for Trace power gate issue on A0
PchTraceHubMemReg1Size	CoffeeLake Pch A0	BIOS workarounds for Trace power gate issue on A0
CstateLatencyControl1Irtl	Server platform	Server platform should have different setting
PchPcieHsioRxSetCtleEnable	Board design	Different board requires different
		Different board

PchPcieHsioRxSetCtle	Board design	requires different
PchSataHsioRxGen3EqBoostMagEnable	Board design	Different board requires different
PchSataHsioRxGen3EqBoostMag	Board design	Different board requires different
PchSataHsioTxGen1DownscaleAmpEnable	Board design	Different board requires different
PchSataHsioTxGen1DownscaleAmp	Board design	Different board requires different
PchSataHsioTxGen2DownscaleAmpEnable	Board design	Different board requires different
PchSataHsioTxGen2DownscaleAmp	Board design	Different board requires different
PchNumRsvdSmbusAddresses	Board design	Different board requires different
RsvdSmbusAddressTablePtr	Board design	Different board requires different
BiosSize	Board design	Different board requires

different

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## FSP OUTPUT

# 6 FSP Output

The FSP builds a series of data structures called the Hand-Off-Blocks (HOBs) as it progresses through initializing the silicon.

Please refer to the Platform Initialization (PI) Specification - Volume 3: Shared Architectural Elements specification for PI Architectural HOBs. Please refer Chapter 9 in the FSP External Architecture Specification version 2.0 for details about FSP Architectural HOBs.

Below section describe the HOBs not covered in the above two specifications.

## 6.1 SMRAM Resource Descriptor HOB

The FSP will report the system SMRAM T-SEG range through a generic resource HOB if T-SEG is enabled. The owner field of the HOB identifies the owner as T-SEG.

```
#define FSP_HOB_RESOURCE_OWNER_TSEG_GUID \
{ 0xd038747c, 0xd00c, 0x4980, { 0xb3, 0x19, 0x49, \
    0x01, 0x99, 0xa4, 0x7d, 0x55 } }
```

## 6.2 SMBIOS INFO HOB

The FSP will report the SMBIOS through a HOB with below GUID. This information can be consumed by the bootloader to produce the SMBIOS tables. These structures are included as part of [MemInfoHob.h](#) , [SmbiosCacheInfoHob.h](#), [SmbiosProcessorInfoHob.h](#) & [FirmwareVersionInfoHob.h](#)

```
#define SI_MEMORY_INFO_DATA_HOB_GUID \
{ 0x9b2071d4, 0xb054, 0x4e0c, { 0x8d, 0x09, 0x11,
    0xcf, 0x8b, 0x9f, 0x03, 0x23 } };

typedef struct {
    MrcDimmStatus Status;           ///<
        See MrcDimmStatus for the definition of this
        field.

    UINT8          DimmId;          ///<
    UINT32         DimmCapacity;    ///<
        DIMM size in MBytes.

    UINT16         MfgId;          ///<
    UINT8          ModulePartNum[20]; ///<
        Module part number for DDR3 is 18 bytes
        however for DRR4 20 bytes as per JEDEC Spec,
        so reserving 20 bytes

    UINT8          RankInDimm;     ///<
        The number of ranks in this DIMM.

    UINT8          SpdDramDeviceType; ///<
        Save SPD DramDeviceType information needed for
        SMBIOS structure creation.

    UINT8          SpdModuleType;    ///<
        Save SPD ModuleType information needed for
        SMBIOS structure creation.

    UINT8          SpdModuleMemoryBusWidth; ///<
        Save SPD ModuleMemoryBusWidth information
        needed for SMBIOS structure creation.

    UINT8          SpdSave[MAX_SPD_SAVE_DATA]; ///<
```

```

        Save SPD Manufacturing information needed for
        SMBIOS structure creation.
} DIMM_INFO;

typedef struct {
    UINT8          Status;           ///<
    Indicates whether this channel should be used.
    UINT8          ChannelId;
    UINT8          DimmCount;        ///<
    Number of valid DIMMs that exist in the
    channel.
    MRC_CH_TIMING Timing[MAX_PROFILE];   ///<
    The channel timing values.
    DIMM_INFO     Dimm[MAX_DIMM];      ///<
    Save the DIMM output characteristics.
} CHANNEL_INFO;

typedef struct {
    UINT8          Status;           ///<
    Indicates whether this controller should be
    used.
    UINT16         DeviceId;         ///<
    The PCI device id of this memory controller.
    UINT8          RevisionId;       ///<
    The PCI revision id of this memory controller.
    UINT8          ChannelCount;     ///<
    Number of valid channels that exist on the
    controller.
    CHANNEL_INFO   Channel[MAX_CH];  ///<
    The following are channel level definitions.
} CONTROLLER_INFO;

typedef struct {
    EFI_HOB_GUID_TYPE EfiHobGuidType;
    UINT8            Revision;
    UINT16           DataWidth;
    /// As defined in SMBIOS 3.0 spec
    /// Section 7.18.2 and Table 75

```

```

    UINT8           DdrType;           ///<
    DDR type: DDR3, DDR4, or LPDDR3
    UINT32          Frequency;        ///<
    The system's common memory controller
    frequency in MT/s.
/// As defined in SMBIOS 3.0 spec
/// Section 7.17.3 and Table 72
    UINT8          ErrorCorrectionType;

    SiMrcVersion    Version;
    UINT32          FreqMax;
    BOOLEAN         EccSupport;
    UINT8           MemoryProfile;
    UINT32          TotalPhysicalMemorySize;
    BOOLEAN         XmpProfileEnable;
    UINT8           Ratio;
    UINT8           RefClk;
    UINT32          VddVoltage[MAX_PROFILE];
    CONTROLLER_INFO Controller[MAX_NODE];
} MEMORY_INFO_DATA_HOB;

#define SI_MEMORY_PLATFORM_DATA_HOB \
{ 0x6210d62f, 0x418d, 0x4999, { 0xa2, 0x45, \
    0x22, 0x10, 0xa, 0x5d, 0xea, 0x44 } }

typedef struct {
    UINT8           Revision;
    UINT8           Reserved[3];
    UINT32          BootMode;
    UINT32          TsegSize;
    UINT32          TsegBase;
    UINT32          PrmrrSize;
    UINT32          PrmrrBase;
    UINT32          GttBase;
    UINT32          MmioSize;
    UINT32          PciEBaseAddress;
} MEMORY_PLATFORM_DATA;

typedef struct {

```

```

EFI_HOB_GUID_TYPE      EfiHobGuidType;
MEMORY_PLATFORM_DATA  Data;
UINT8                  *Buffer;
} MEMORY_PLATFORM_DATA_HOB;

#define SMBIOS_CACHE_INFO_HOB_GUID \
{ 0xd805b74e, 0x1460, 0x4755, {0xbb, 0x36, 0x1e, \
    0x8c, 0x8a, 0xd6, 0x78, 0xd7} }

///
/// SMBIOS Cache Info HOB Structure
///
typedef struct {
    UINT16    ProcessorSocketNumber;
    UINT16    NumberOfCacheLevels;           ///<
                                                Based on Number of Cache Types L1/L2/L3
    UINT8     SocketDesignationStrIndex;    ///<
                                                String Index in the string Buffer. Example
                                                "L1-CACHE"
    UINT16    CacheConfiguration;           ///<
                                                Format defined in SMBIOS Spec v3.0 Section7.8
                                                Table36
    UINT16    MaxCacheSize;                ///<
                                                Format defined in SMBIOS Spec v3.0
                                                Section7.8.1
    UINT16    InstalledSize;               ///<
                                                Format defined in SMBIOS Spec v3.0
                                                Section7.8.1
    UINT16    SupportedSramType;          ///<
                                                Format defined in SMBIOS Spec v3.0
                                                Section7.8.2
    UINT16    CurrentSramType;            ///<
                                                Format defined in SMBIOS Spec v3.0
                                                Section7.8.2
    UINT8     CacheSpeed;                 ///<
                                                Cache Speed in nanoseconds. 0 if speed is
                                                unknown.
    UINT8     ErrorCorrectionType;        ///<

```

```

    ENUM Format defined in SMBIOS Spec v3.0
Section 7.8.3
UINT8      SystemCacheType;           ///<
    ENUM Format defined in SMBIOS Spec v3.0
Section 7.8.4
UINT8      Associativity;           ///<
    ENUM Format defined in SMBIOS Spec v3.0
Section 7.8.5
///String Buffer - each string terminated by
NULL "0x00"
///String buffer terminated by double NULL
"0x0000"
} SMBIOS_CACHE_INFO;

#define SMBIOS_PROCESSOR_INFO_HOB_GUID \
{ 0xe6d73d92, 0xff56, 0x4146, {0xaf, 0xac, 0x1c,
0x18, 0x81, 0x7d, 0x68, 0x71} }

///
/// SMBIOS Processor Info HOB Structure
///
typedef struct {
    UINT16      TotalNumberOfSockets;
    UINT16      CurrentSocketNumber;
    UINT8       ProcessorType;           ///<
        ENUM defined in SMBIOS Spec v3.0 Section 7.5.1
    ///This info is used for both ProcessorFamily
        and ProcessorFamily2 fields
    ///See ENUM defined in SMBIOS Spec v3.0 Section
        7.5.2
    UINT16      ProcessorFamily;
    UINT8       ProcessorManufacturerStrIndex; ///<
        Index of the String in the String Buffer
    UINT64      ProcessorId;           ///<
        ENUM defined in SMBIOS Spec v3.0 Section 7.5.3
    UINT8       ProcessorVersionStrIndex; ///<
        Index of the String in the String Buffer
    UINT8       Voltage;               ///<

```

```
Format defined in SMBIOS Spec v3.0 Section  
7.5.4  
UINT16      ExternalClockInMHz;           ///<  
External Clock Frequency. Set to 0 if unknown.  
UINT16      CurrentSpeedInMHz;          ///<  
Snapshot of current processor speed during  
boot  
UINT8       Status;                   ///<  
Format defined in the SMBIOS Spec v3.0 Table  
21  
UINT8       ProcessorUpgrade;          ///<  
ENUM defined in SMBIOS Spec v3.0 Section 7.5.5  
///This info is used for both CoreCount &  
CoreCount2 fields  
/// See detailed description in SMBIOS Spec v3.0  
Section 7.5.6  
UINT16      CoreCount;                ///<  
///This info is used for both CoreEnabled &  
CoreEnabled2 fields  
///See detailed description in SMBIOS Spec v3.0  
Section 7.5.7  
UINT16      EnabledCoreCount;         ///<  
///This info is used for both ThreadCount &  
ThreadCount2 fields  
/// See detailed description in SMBIOS Spec v3.0  
Section 7.5.8  
UINT16      ThreadCount;  
UINT16      ProcessorCharacteristics;  ///<  
Format defined in SMBIOS Spec v3.0 Section  
7.5.9  
/// String Buffer - each string terminated by  
NULL "0x00"  
/// String buffer terminated by double NULL  
"0x0000"  
} SMBIOS_PROCESSOR_INFO;  
  
#define SMBIOS_FIRMWARE_VERSION_INFO_HOB_GUID \
```

```

{ 0x798e722e, 0x15b2, 0x4e13, { 0x8a, 0xe9,
    0x6b, 0xa3, 0x0f, 0xf7, 0xf1, 0x67 } }

///
/// Firmware Version Structure
///
typedef struct {
    UINT8                         MajorVersion;
    UINT8                         MinorVersion;
    UINT8                         Revision;
    UINT16                        BuildNumber;
} FIRMWARE_VERSION;

///
/// Firmware Version Information Structure
///
typedef struct {
    UINT8
        ComponentNameIndex;           ///< Offset 0
        Index of Component Name
    UINT8
        VersionStringIndex;          ///< Offset 1
        Index of Version String
    FIRMWARE_VERSION                Version;
        ///< Offset 2-6 Firmware version
} FIRMWARE_VERSION_INFO;

///
/// The Smbios structure header.
///
typedef struct {
    UINT8                         Type;
    UINT8                         Length;
    UINT16                        Handle;
} SMBIOS_STRUCTURE;

///
/// Firmware Version Information HOB Structure
///

```

```
typedef struct {
    EFI_HOB_GUID_TYPE           Header;
    ///< Offset 0-23  The header of FVI HOB
    SMBIOS_STRUCTURE            SmbiosData;
    ///< Offset 24-27  The SMBIOS header of FVI
    HOB
    UINT8                       Count;
    ///< Offset 28      Number of FVI elements
    included.

    ///
    /// FIRMWARE_VERSION_INFO structures followed by
    the null terminated string buffer
    ///
} FIRMWARE_VERSION_INFO_HOB;
```

## 6.3 CHIPSETINIT INFO HOB

The FSP will report the ChipsetInit CRC through a HOB with below GUID. This information can be consumed by the bootloader to check if ChipsetInit CRC is matched between BIOS and ME. These structures are included as part of [FspUpd.h](#)

```
#define CHIPSETINIT_INFO_HOB_GUID \
{ 0xc1392859, 0x1f65, 0x446e, { 0xb3, 0xf5, 0x84,
    0x35, 0xfc, 0xc7, 0xd1, 0xc4 } }

///
/// The ChipsetInit Info structure provides the
/// information of ME ChipsetInit CRC and BIOS
/// ChipsetInit CRC.
///
typedef struct {
    UINT8          Revision;
    UINT8          Rsvd[3];
    UINT16         MeChipInitCrc;
    UINT16         BiosChipInitCrc;
} CHIPSET_INIT_INFO;
```

## 6.4 HOB USAGE INFO HOB

The FSP will report the Hob memory usage through a HOB with below GUID. This information can be consumed by the bootloader to check how many the temporary ram left.

```
#define HOB_USAGE_DATA_HOB_GUID \
{0xc764a821, 0xec41, 0x450d, { 0x9c, 0x99, 0x27,
    0x20, 0xfc, 0x7c, 0xe1, 0xf6 }}

typedef struct {
    EFI_PHYSICAL_ADDRESS EfiMemoryTop;
    EFI_PHYSICAL_ADDRESS EfiMemoryBottom;
    EFI_PHYSICAL_ADDRESS EfiFreeMemoryTop;
    EFI_PHYSICAL_ADDRESS EfiFreeMemoryBottom;
    UINTN                FreeMemory;
} HOB_USAGE_DATA_HOB;
```



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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**FSP POSTCODE**

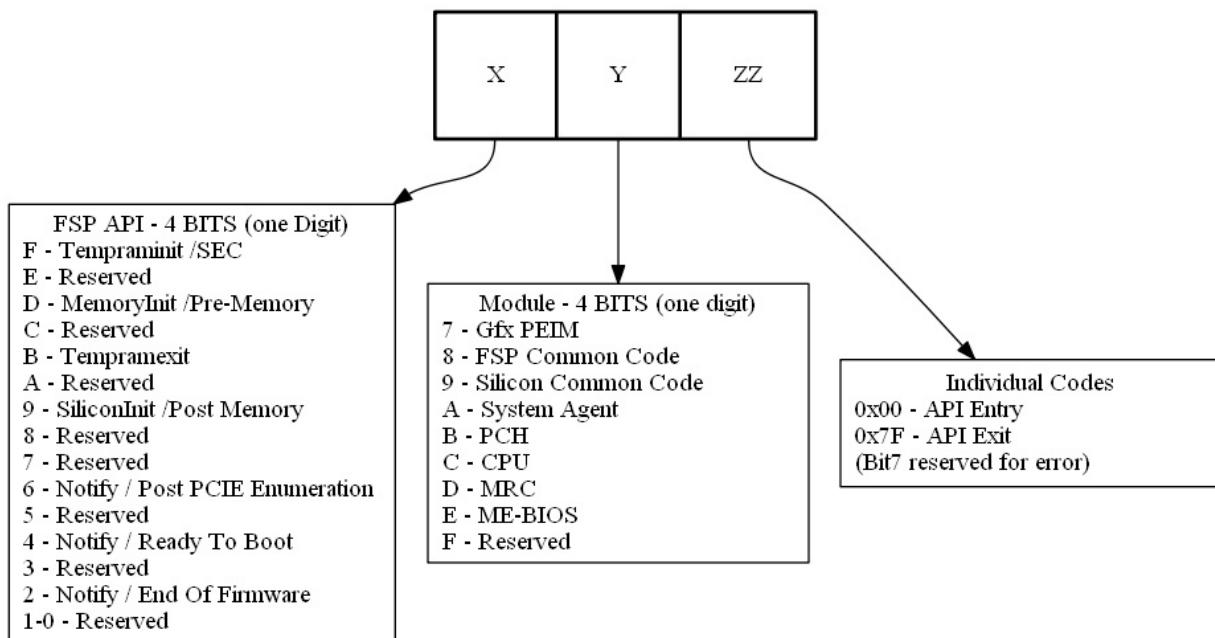
## 7 FSP PostCode

The FSP outputs 16 bit postcode to indicate which API and in which module the execution is happening.

Bit Range	Description
Bit15 - Bit12 (X)	used to indicate the phase/api under which the code is executing
Bit11 - Bit8 (Y)	used to indicate the module
Bit7 (ZZ bit 7)	reserved for error
Bit6 - Bit0 (ZZ)	individual codes

## 7.1 PostCode Info

Below diagram represents the 16 bit PostCode usage in FSP.



### 7.1.1 TempRamInit API Status Codes (0xFxxx)

PostCode	Module	Description
0x0000	FSP	TempRamInit API Entry (The change in upper byte is due to not enabling of the Port81 early in the boot)
0x007F	FSP	TempRamInit API Exit

### 7.1.2 FspMemoryInit API Status Codes (0xDxxx)

PostCode	Module	Description
0xD800	FSP	FspMemoryInit API Entry
0xD87F	FSP	FSpMemoryInit API Exit
0xDA00	SA	Pre-Mem Salnit Entry
0xDA02	SA	OverrideDev0Did Start

0xDA04	SA	OverrideDev2Did Start
0xDA06	SA	Programming SA Bars
0xDA08	SA	Install SA HOBs
0xDA0A	SA	Reporting SA PCIe code version
0xDA0C	SA	SaSvInit Start
0xDA10	SA	Initializing DMI
0xDA15	SA	Initialize TCSS PreMem
0xDA1F	SA	Initializing DMI/OPI Max PayLoad Size
0xDA20	SA	Initializing SwitchableGraphics
0xDA30	SA	Initializing SA PCIe
0xDA3F	SA	Programming PEG credit values Start
0xDA40	SA	Initializing DMI Tc/Vc mapping
0xDA42	SA	CheckOffboardPcieVga
0xDA44	SA	CheckAndInitializePegVga
0xDA50	SA	Initializing Graphics
0xDA52	SA	Initializing System Agent Overclocking
0xDA7F	SA	Pre-Mem Salnit Exit
0xDB00	PCH	Pre-Mem PchInit Entry
0xDB02	PCH	Pre-Mem Disable PCH fused controllers
0xDB15	PCH	Pre-Mem SMBUS configuration
0xDB48	PCH	Pre-Mem PchOnPolicyInstalled Entry
0xDB49	PCH	Pre-Mem Program HSIO
0xDB4A	PCH	Pre-Mem DCI configuration
0xDB4C	PCH	Pre-Mem Host DCI enabled
0xDB4D	PCH	Pre-Mem Trace Hub - Early configuration
0xDB4E	PCH	Pre-Mem Trace Hub - Device disabled
0xDB4F	PCH	Pre-Mem TraceHub - Programming MSR
0xDB50	PCH	Pre-Mem Trace Hub - Power gating configuration
0xDB51	PCH	Pre-Mem Trace Hub - Power gating Trace Hub device and locking HSWPGCR1 register
0xDB52	PCH	Pre-Mem Initialize HPET timer

0xDB55	PCH	Pre-Mem PchOnPolicyInstalled Exit
0xDB7F	PCH	Pre-Mem PchInit Exit
0xDC00	CPU	CPU Pre-Mem Entry
0xDC0F	CPU	CpuAddPreMemConfigBlocks Done
0xDC20	CPU	CpuOnPolicyInstalled Start
0xDC2F	CPU	XmmInit Start
0xDC3F	CPU	TxtInit Start
0xDC4F	CPU	Init CPU Straps
0xDC5F	CPU	Init Overclocking
0xDC6F	CPU	CPU Pre-Mem Exit
0x**55	SA	MRC_MEM_INIT_DONE
0x**D5	SA	MRC_MEM_INIT_DONE_WITH_ERRORS
0xDD00	SA	MRC_INITIALIZATION_START
0xDD10	SA	MRC_CMD_PLOT_2D
0xDD1B	SA	MRC_FAST_BOOT_PERMITTED
0xDD1C	SA	MRC_RESTORE_NON_TRAINING
0xDD1D	SA	MRC_PRINT_INPUT_PARAMS
0xDD1E	SA	MRC_SET_OVERRIDES_PSPD
0xDD20	SA	MRC_SPD_PROCESSING
0xDD21	SA	MRC_SET_OVERRIDES
0xDD22	SA	MRC_MC_CAPABILITY
0xDD23	SA	MRC_MC_CONFIG
0xDD24	SA	MRC_MC_MEMORY_MAP
0xDD25	SA	MRC_JEDEC_INIT_LPDDR3
0xDD26	SA	MRC_RESET_SEQUENCE
0xDD27	SA	MRC_PRE_TRAINING
0xDD28	SA	MRC_EARLY_COMMAND
0xDD29	SA	MRC_SENSE_AMP_OFFSET
0xDD2A	SA	MRC_READ_MPR
0xDD2B	SA	MRC_RECEIVE_ENABLE
0xDD2C	SA	MRC_JEDEC_WRITE_LEVELING

0xDD2D	SA	MRC_LPDDR_LATENCY_SET_B
0xDD2E	SA	MRC_WRITE_TIMING_1D
0xDD2F	SA	MRC_READ_TIMING_1D
0xDD30	SA	MRC_DIMM_ODT
0xDD31	SA	MRC_EARLY_WRITE_TIMING_2D
0xDD32	SA	MRC_WRITE_DS
0xDD33	SA	MRC_WRITE_EQ
0xDD34	SA	MRC_EARLY_READ_TIMING_2D
0xDD35	SA	MRC_READ_ODT
0xDD36	SA	MRC_READ_EQ
0xDD37	SA	MRC_READ_AMP_POWER
0xDD38	SA	MRC_WRITE_TIMING_2D
0xDD39	SA	MRC_READ_TIMING_2D
0xDD3A	SA	MRC_CMD_VREF
0xDD3B	SA	MRC_WRITE_VREF_2D
0xDD3C	SA	MRC_READ_VREF_2D
0xDD3D	SA	MRC_POST_TRAINING
0xDD3E	SA	MRC_LATE_COMMAND
0xDD3F	SA	MRC_ROUND_TRIP_LAT
0xDD40	SA	MRC_TURN_AROUND
0xDD41	SA	MRC_CMP_OPT
0xDD42	SA	MRC_SAVE_MC_VALUES
0xDD43	SA	MRC_RESTORE_TRAINING
0xDD44	SA	MRC_RMT_TOOL
0xDD45	SA	MRC_WRITE_SR
0xDD46	SA	MRC_DIMM_RON
0xDD47	SA	MRC_RCVEN_TIMING_1D
0xDD48	SA	MRC_MR_FILL
0xDD49	SA	MRC_PWR_MTR
0xDD4A	SA	MRC_DDR4_MAPPING
0xDD4B	SA	MRC_WRITE_VOLTAGE_1D
0xDD4C	SA	MRC_EARLY_RDMPR_TIMING_2D

0xDD4D	SA	MRC_FORCE_OLTM
0xDD50	SA	MRC_MC_ACTIVATE
0xDD51	SA	MRC_RH_PREVENTION
0xDD52	SA	MRC_GET_MRC_DATA
0xDD53	SA	Reserved
0xDD58	SA	MRC_RETRAIN_CHECK
0xDD5A	SA	MRC_SA_GV_SWITCH
0xDD5B	SA	MRC_ALIAS_CHECK
0xDD5C	SA	MRC_ECC_CLEAN_START
0xDD5D	SA	MRC_DONE
0xDD5F	SA	MRC_CPGC_MEMORY_TEST
0xDD60	SA	MRC_TXT_ALIAS_CHECK
0xDD61	SA	MRC_ENG_PERF_GAIN
0xDD68	SA	MRC_MEMORY_TEST
0xDD69	SA	MRC_FILL_RMT_STRUCTURE
0xDD70	SA	MRC_SELF_REFRESH_EXIT
0xDD71	SA	MRC_NORMAL_MODE
0xDD7D	SA	MRC_SSA_PRE_STOP_POINT
0xDD7F	SA	MRC_SSA_STOP_POINT, MRC_INITIALIZATION_END
0xDD90	SA	MRC_CMD_PLOT_2D_ERROR
0xDD9B	SA	MRC_FAST_BOOT_PERMITTED_ERROR
0xDD9C	SA	MRC_RESTORE_NON_TRAINING_ERROR
0xDD9D	SA	MRC_PRINT_INPUT_PARAMS_ERROR
0xDD9E	SA	MRC_SET_OVERRIDES_PSPD_ERROR
0xDDA0	SA	MRC_SPD_PROCESSING_ERROR
0xDDA1	SA	MRC_SET_OVERRIDES_ERROR
0xDDA2	SA	MRC_MC_CAPABILITY_ERROR
0xDDA3	SA	MRC_MC_CONFIG_ERROR
0xDDA4	SA	MRC_MC_MEMORY_MAP_ERROR
0xDDA5	SA	MRC_JEDEC_INIT_LPDDR3_ERROR
0xDDA6	SA	MRC_RESET_ERROR

0xDDA7	SA	MRC_PRE_TRAINING_ERROR
0xDDA8	SA	MRC_EARLY_COMMAND_ERROR
0xDDA9	SA	MRC_SENSE_AMP_OFFSET_ERROR
0xDDAA	SA	MRC_READ_MPR_ERROR
0xDDAB	SA	MRC_RECEIVE_ENABLE_ERROR
0xDDAC	SA	MRC_JEDEC_WRITE_LEVELING_ERROR
0xDDAD	SA	MRC_LPDDR_LATENCY_SET_B_ERROR
0xDDAE	SA	MRC_WRITE_TIMING_1D_ERROR
0xDDAF	SA	MRC_READ_TIMING_1D_ERROR
0xDDB0	SA	MRC_DIMM_ODT_ERROR
0xDDB1	SA	MRC_EARLY_WRITE_TIMING_ERROR
0xDDB2	SA	MRC_WRITE_DS_ERROR
0xDDB3	SA	MRC_WRITE_EQ_ERROR
0xDDB4	SA	MRC_EARLY_READ_TIMING_ERROR
0xDDB5	SA	MRC_READ_ODT_ERROR
0xDDB6	SA	MRC_READ_EQ_ERROR
0xDDB7	SA	MRC_READ_AMP_POWER_ERROR
0xDDB8	SA	MRC_WRITE_TIMING_2D_ERROR
0xDDB9	SA	MRC_READ_TIMING_2D_ERROR
0xDDBA	SA	MRC_CMD_VREF_ERROR
0xDDBB	SA	MRC_WRITE_VREF_2D_ERROR
0xDDBC	SA	MRC_READ_VREF_2D_ERROR
0xDDBD	SA	MRC_POST_TRAINING_ERROR
0xDDBE	SA	MRC_LATE_COMMAND_ERROR
0xDDBF	SA	MRC_ROUND_TRIP_LAT_ERROR
0xDDC0	SA	MRC_TURN_AROUND_ERROR
0xDDC1	SA	MRC_CMP_OPT_ERROR
0xDDC2	SA	MRC_SAVE_MC_VALUES_ERROR
0xDDC3	SA	MRC_RESTORE_TRAINING_ERROR
0xDDC4	SA	MRC_RMT_TOOL_ERROR
0xDDC5	SA	MRC_WRITE_SR_ERROR
0xDDC6	SA	MRC_DIMM_RON_ERROR

0xDDC7	SA	MRC_RCVEN_TIMING_1D_ERROR
0xDDC8	SA	MRC_MR_FILL_ERROR
0xDDC9	SA	MRC_PWR_MTR_ERROR
0xDDCA	SA	MRC_DDR4_MAPPING_ERROR
0xDDCB	SA	MRC_WRITE_VOLTAGE_1D_ERROR
0xDDCC	SA	MRC_EARLY_RDMPR_TIMING_2D_ERROR
0xDDCD	SA	MRC_FORCE_OLTM_ERROR
0xDDD0	SA	MRC_MC_ACTIVATE_ERROR
0xDDD1	SA	MRC_RH_PREVENTION_ERROR
0xDDD2	SA	MRC_GET_MRC_DATA_ERROR
0xDDD3	SA	Reserved
0xDDD8	SA	MRC_RETRAIN_CHECK_ERROR
0xDDDA	SA	MRC_SA_GV_SWITCH_ERROR
0xDDDB	SA	MRC_ALIAS_CHECK_ERROR
0xDDDC	SA	MRC_ECC_CLEAN_ERROR
0xDDDD	SA	MRC_DONE_WITH_ERROR
0xDDDF	SA	MRC_CPGC_MEMORY_TEST_ERROR
0xDDE0	SA	MRC_TXT_ALIAS_CHECK_ERROR
0xDDE1	SA	MRC_ENG_PERF_GAIN_ERROR
0xDDE8	SA	MRC_MEMORY_TEST_ERROR
0xDDE9	SA	MRC_FILL_RMT_STRUCTURE_ERROR
0xDDF0	SA	MRC_SELF_REFRESH_EXIT_ERROR
0xDDF1	SA	MRC_MRC_NORMAL_MODE_ERROR
0xDDFD	SA	MRC_SSA_PRE_STOP_POINT_ERROR
0xDDFE	SA	MRC_NO_MEMORY_DETECTED

### 7.1.3 TempRamExit API Status Codes (0xBxxx)

PostCode	Module	Description
0xB800	FSP	TempRamExit API Entry
0xB87F	FSP	TempRamExit API Exit

## 7.1.4 FspSiliconInit API Status Codes (0x9xxx)

PostCode	Module	Description
0x9800	FSP	FspSiliconInit API Entry
0x987F	FSP	FspSiliconInit API Exit
0x9A00	SA	PostMem Salnit Entry
0x9A01	SA	DeviceConfigure Start
0x9A02	SA	UpdateSaHobPostMem Start
0x9A03	SA	Initializing Pei Display
0x9A04	SA	PeiGraphicsNotifyCallback Entry
0x9A05	SA	CallPpiAndFillFrameBuffer
0x9A06	SA	GraphicsPpiInit
0x9A07	SA	GraphicsPpiGetMode
0x9A08	SA	FillFrameBufferAndShowLogo
0x9A0F	SA	PeiGraphicsNotifyCallback Exit
0x9A14	SA	Initializing SA IPU device
0x9A16	SA	Initializing SA GNA device
0x9A1A	SA	SaProgramLlcWays Start
0x9A20	SA	Initializing PciExpressInitPostMem
0x9A22	SA	Initializing ConfigureNorthIntelTraceHub
0x9A30	SA	Initializing Vtd
0x9A31	SA	Initializing TCSS
0x9A32	SA	Initializing Pavp
0x9A34	SA	PeiInstallSmmAccessPpi Start
0x9A36	SA	EdramWa Start
0x9A4F	SA	Post-Mem Salnit Exit
0x9A50	SA	SaSecurityLock Start
0x9A5F	SA	SaSecurityLock End
0x9A60	SA	SaSResetComplete Entry
0x9A61	SA	Set BIOS_RESET_CPL to indicate all configurations complete
0x9A62	SA	SaSvInit2 Start

0x9A63	SA	GraphicsPmInit Start
0x9A64	SA	SaPciPrint Start
0x9A6F	SA	SaSResetComplete Exit
0x9A70	SA	SaS3ResumeAtEndOfPei Callback Entry
0x9A7F	SA	SaS3ResumeAtEndOfPei Callback Exit
0x9B00	PCH	Post-Mem PchInit Entry
0x9B03	PCH	Post-Mem Tune the USB 2.0 high-speed signals quality
0x9B04	PCH	Post-Mem Tune the USB 3.0 signals quality
0x9B05	PCH	Post-Mem Configure PCH xHCI
0x9B06	PCH	Post-Mem Performs configuration of PCH xHCI SSIC
0x9B07	PCH	Post-Mem Configure PCH xHCI after init
0x9B08	PCH	Post-Mem Configures PCH USB device (xDCI)
0x9B0A	PCH	Post-Mem DMI/OP-DMI configuration
0x9B0B	PCH	Post-Mem Initialize P2SB controller
0x9B0C	PCH	Post-Mem IOAPIC initialization
0x9B0D	PCH	Post-Mem PCH devices interrupt configuration
0x9B0E	PCH	Post-Mem HD Audio initialization
0x9B0F	PCH	Post-Mem HD Audio Codec enumeration
0x9B10	PCH	Post-Mem HD Audio Codec not detected
0x9B13	PCH	Post-Mem SCS initialization
0x9B14	PCH	Post-Mem ISH initialization
0x9B15	PCH	Post-Mem Configure SMBUS power management
0x9B16	PCH	Post-Mem Reserved
0x9B17	PCH	Post-Mem Performing global reset
0x9B18	PCH	Post-Mem Reserved
0x9B19	PCH	Post-Mem Reserved
0x9B40	PCH	Post-Mem OnEndOfPEI Entry

0x9B41	PCH	Post-Mem Initialize Thermal controller
0x9B42	PCH	Post-Mem Configure Memory Throttling
0x9B47	PCH	Post-Mem OnEndOfPEI Exit
0x9B4D	PCH	Post-Mem Trace Hub - Memory configuration
0x9B4E	PCH	Post-Mem Trace Hub - MSC0 configured
0x9B4F	PCH	Post-Mem Trace Hub - MSC1 configured
0x9B7F	PCH	Post-Mem PchInit Exit
0x9C00	CPU	CPU Post-Mem Entry
0x9C09	CPU	CpuAddConfigBlocks Done
0x9C0A	CPU	SetCpuStrapAndEarlyPowerOnConfig Start
0x9C13	CPU	SetCpuStrapAndEarlyPowerOnConfig Reset
0x9C14	CPU	SetCpuStrapAndEarlyPowerOnConfig Done
0x9C15	CPU	CpuInit Start
0x9C16	CPU	SgxInitializationPrePatchLoad Start
0x9C17	CPU	CollectProcessorFeature Start
0x9C18	CPU	ProgramProcessorFeature Start
0x9C19	CPU	ProgramProcessorFeature Done
0x9C20	CPU	CpuInitPreResetCpl Start
0x9C21	CPU	ProcessorsPrefetcherInitialization Start
0x9C22	CPU	InitRatl Start
0x9C23	CPU	ConfigureSvidVrs Start
0x9C24	CPU	ConfigurePidSettings Start
0x9C25	CPU	SetBootFrequency Start
0x9C26	CPU	CpuOcInitPreMem Start
0x9C27	CPU	CpuOcInit Reset
0x9C28	CPU	BiosGuardInit Start
0x9C29	CPU	BiosGuardInit Reset
0x9C3F	CPU	CpuInitPreResetCpl Done
0x9C42	CPU	SgxActivation Start
0x9C43	CPU	InitializeCpuDataHob Start

0x9C44	CPU	InitializeCpuDataHob Done
0x9C4F	CPU	CpuInit Done
0x9C50	CPU	S3InitializeCpu Start
0x9C55	CPU	MpRendezvousProcedure Start
0x9C56	CPU	MpRendezvousProcedure Done
0x9C69	CPU	S3InitializeCpu Done
0x9C6A	CPU	CpuPowerMgmtInit Start
0x9C71	CPU	InitPpm
0x9C7F	CPU	CPU Post-Mem Exit
0x9C80	CPU	ReloadMicrocodePatch Start
0x9C81	CPU	ReloadMicrocodePatch Done
0x9C82	CPU	ApSafePostMicrocodePatchInit Start
0x9C83	CPU	ApSafePostMicrocodePatchInit Done

### 7.1.5 NotifyPhase API Status Codes (0x6xx)

PostCode	Module	Description
0x6800	FSP	NotifyPhase API Entry
0x687F	FSP	NotifyPhase API Exit

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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## Todo List

### **Page FSP INTEGRATION**

program 0x1000000000 - Top of High Memory | Write back

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## Deprecated List

### **Member FSP\_S\_CONFIG::SkipMpInit**

SkipMpInit has been moved to FspmUpd \$EN\_DIS

### **Member FSP\_S\_TEST\_CONFIG::DebugInterfaceEnable**

Enable or Disable processor debug features; 0: **Disable**; 1: Enable.  
\$EN\_DIS

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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## Class List

Here are the classes, structs, unions and interfaces with brief descriptions:

<a href="#"> AUDIO_AZALIA_VERB_TABLE</a>	Audio Azalia Verb Table
<a href="#"> AZALIA_HEADER</a>	Azalia Header structure
<a href="#"> CHIPSET_INIT_INFO</a>	The ChipsetInit Info stru the information of ME CI and BIOS ChipsetInit CF
<a href="#"> DIMM_INFO</a>	Memory SMBIOS & OC Hob
<a href="#"> FIRMWARE_VERSION</a>	Firmware Version Struct
<a href="#"> FIRMWARE_VERSION_INFO</a>	Firmware Version Inform Structure
<a href="#"> FIRMWARE_VERSION_INFO_HOB</a>	Firmware Version Inform Structure
<a href="#"> FSP_M_CONFIG</a>	Fsp M Configuration
<a href="#"> FSP_M_TEST_CONFIG</a>	Fsp M Test Configuration
<a href="#"> FSP_S_CONFIG</a>	Fsp S Configuration
<a href="#"> FSP_S_TEST_CONFIG</a>	Fsp S Test Configuration
<a href="#"> FSP_T_CONFIG</a>	Fsp T Configuration
<a href="#"> FSPM_UPD</a>	Fsp M UPD Configuratio

<a href="#"> <b>FSPS_UPD</b></a>	Fsp S UPD Configuration
<a href="#"> <b>FSPT_CORE_UPD</b></a>	Fsp T Core UPD
<a href="#"> <b>FSPT_UPD</b></a>	Fsp T UPD Configuration
<a href="#"> <b>GPIO_CONFIG</b></a>	GPIO configuration structure pin programming
<a href="#"> <b>HOB_USAGE_DATA_HOB</b></a>	Hob Usage Data Hob
<a href="#"> <b>MEMORY_PLATFORM_DATA</b></a>	Memory Platform Data
<a href="#"> <b>SI_PCH_DEVICE_INTERRUPT_CONFIG</b></a>	The PCH_DEVICE_INTERRUPT_CONFIG block describes interrupt interrupt mode for PCH
<a href="#"> <b>SMBIOS_CACHE_INFO</b></a>	SMBIOS Cache Info HO
<a href="#"> <b>SMBIOS_PROCESSOR_INFO</b></a>	SMBIOS Processor Info Structure
<a href="#"> <b>SMBIOS_STRUCTURE</b></a>	The Smbios structure he

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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[Public Attributes](#) | [List of all members](#)

## AUDIO\_AZALIA\_VERB\_TABLE Struct Reference

Audio Azalia Verb Table structure. More...

```
#include <FspUpd.h>
```

Collaboration diagram for AUDIO\_AZALIA\_VERB\_TABLE:



[[legend](#)]

## Public Attributes

---

### **AZALIA\_HEADER** **Header**

AZALIA PCH header.

### **UINT32 \*** **Data**

Pointer to the data buffer. Its length is specified in the header.

---

## Detailed Description

---

Audio Azalia Verb Table structure.

Definition at line **56** of file [FspUpd.h](#).

---

The documentation for this struct was generated from the following file:

- [FspUpd.h](#)
- 

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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Class List	Class Index	Class Members	
<b>AZALIA_HEADER</b> <b>Struct Reference</b>			<a href="#">Public Attributes</a>   <a href="#">List of all members</a>

Azalia Header structure. [More...](#)

```
#include <FspUpd.h>
```

## Public Attributes

---

UINT16 **VendorId**

Codec Vendor ID.

UINT16 **DeviceId**

Codec Device ID.

UINT8 **RevisionId**

Revision ID of the codec. 0xFF matches any revision.

UINT8 **SdiNum**

SDI number, 0xFF matches any SDI.

UINT16 **DataDwords**

Number of data DWORDs pointed by the codec data buffer.

UINT32 **Reserved**

Reserved for future use. Must be set to 0.

---

## Detailed Description

---

Azalia Header structure.

Definition at line **44** of file [FspUpd.h](#).

---

The documentation for this struct was generated from the following file:

- [FspUpd.h](#)
- 

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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<a href="#">Public Attributes</a>   <a href="#">List of all members</a>			
<h2>CHIPSET_INIT_INFO Struct Reference</h2>			

The ChipsetInit Info structure provides the information of ME ChipsetInit CRC and BIOS ChipsetInit CRC. [More...](#)

```
#include <FspmUpd.h>
```

## Public Attributes

---

UINT8 **Revision**

Chipset Init Info Revision.

UINT8 **Rsvd** [3]

Reserved.

UINT16 **MeChipInitCrc**

16 bit CRC value of MeChipInit Table

UINT16 **BiosChipInitCrc**

16 bit CRC value of PchChipInit Table

---

## Detailed Description

---

The ChipsetInit Info structure provides the information of ME ChipsetInit CRC and BIOS ChipsetInit CRC.

Definition at line [46](#) of file [FspmUpd.h](#).

---

The documentation for this struct was generated from the following file:

- [FspmUpd.h](#)
- 

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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<b>DIMM_INFO Struct Reference</b>			<a href="#">Public Attributes</a>   <a href="#">List of all members</a>

Memory SMBIOS & OC Memory Data Hob. [More...](#)

```
#include <MemInfoHob.h>
```

## Public Attributes

UINT8 **Status**

See MrcDimmStatus for the definition of this field.

UINT32 **DimmCapacity**

DIMM size in MBytes.

UINT8 **ModulePartNum** [20]

Module part number for DDR3 is 18 bytes however for DRR4 20 bytes as per JEDEC Spec, so reserving 20 bytes.

UINT8 **RankInDimm**

The number of ranks in this DIMM.

UINT8 **SpdDramDeviceType**

Save SPD DramDeviceType information needed for SMBIOS structure creation.

UINT8 **SpdModuleType**

Save SPD ModuleType information needed for SMBIOS structure creation.

UINT8 **SpdModuleMemoryBusWidth**

Save SPD ModuleMemoryBusWidth information needed for SMBIOS structure creation.

UINT8 **SpdSave** [**MAX\_SPD\_SAVE**]

Save SPD Manufacturing information needed for SMBIOS structure creation.

UINT16 **Speed**

The maximum capable speed of the device, in MHz.

## Detailed Description

---

Memory SMBIOS & OC Memory Data Hob.

Definition at line **175** of file **MemInfoHob.h**.

---

The documentation for this struct was generated from the following file:

- **MemInfoHob.h**
- 

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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<h2>FIRMWARE_VERSION Struct Reference</h2>			

Firmware Version Structure. [More...](#)

#include <[FirmwareVersionInfoHob.h](#)>

## Detailed Description

---

Firmware Version Structure.

Definition at line **28** of file **FirmwareVersionInfoHob.h**.

---

The documentation for this struct was generated from the following file:

- **FirmwareVersionInfoHob.h**
- 

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

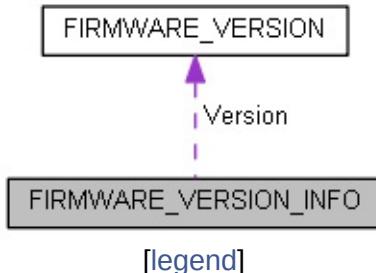
[Main Page](#)[Related Pages](#)[Classes](#)[Files](#)[Class List](#)[Class Index](#)[Class Members](#)[Public Attributes](#) | [List of all members](#)

## FIRMWARE\_VERSION\_INFO Struct Reference

Firmware Version Information Structure. [More...](#)

```
#include <FirmwareVersionInfoHob.h>
```

Collaboration diagram for FIRMWARE\_VERSION\_INFO:

[\[legend\]](#)

## Public Attributes

---

UINT8 **ComponentNameIndex**

Offset 0 Index of Component Name.

UINT8 **VersionStringIndex**

Offset 1 Index of Version String.

**FIRMWARE\_VERSION Version**

Offset 2-6 Firmware version.

---

## Detailed Description

---

Firmware Version Information Structure.

Definition at line **38** of file **FirmwareVersionInfoHob.h**.

---

The documentation for this struct was generated from the following file:

- **FirmwareVersionInfoHob.h**
- 

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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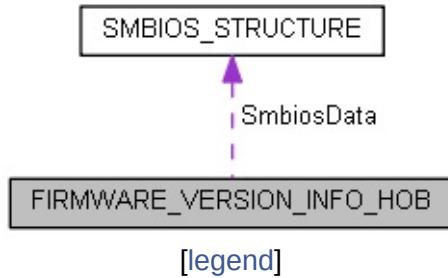
[Public Attributes](#) | [List of all members](#)

## FIRMWARE\_VERSION\_INFO\_HOB Struct Reference

Firmware Version Information HOB Structure. [More...](#)

#include <[FirmwareVersionInfoHob.h](#)>

Collaboration diagram for FIRMWARE\_VERSION\_INFO\_HOB:



## Public Attributes

---

**EFI\_HOB\_GUID\_TYPE** **Header**

Offset 0-23 The header of FVI HOB.

**SMBIOS\_STRUCTURE** **SmbiosData**

Offset 24-27 The SMBIOS header of FVI HOB.

**UINT8** **Count**

Offset 28 Number of FVI elements included. [More...](#)

---

## Detailed Description

---

Firmware Version Information HOB Structure.

Definition at line **58** of file [\*\*FirmwareVersionInfoHob.h\*\*](#).

# Member Data Documentation

---

## **UINT8 FIRMWARE\_VERSION\_INFO\_HOB::Count**

---

Offset 28 Number of FVI elements included.

Definition at line **61** of file [FirmwareVersionInfoHob.h](#).

---

The documentation for this struct was generated from the following file:

- [FirmwareVersionInfoHob.h](#)

---

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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## FSP\_M\_CONFIG Struct Reference

Fsp M Configuration. [More...](#)

```
#include <FspmUpd.h>
```

## Public Attributes

UINT64 **PlatformMemorySize**

Offset 0x0040 - Platform Reserved Memory Size The minimum platform memory size required to pass control into DXE.

UINT32 **MemorySpdPtr00**

Offset 0x0048 - Memory SPD Pointer Channel 0 Dimm 0 Pointer to SPD data, will be used only when SpdAddressTable SPD Address are marked as 00.

UINT32 **MemorySpdPtr01**

Offset 0x004C - Memory SPD Pointer Channel 0 Dimm 1 Pointer to SPD data, will be used only when SpdAddressTable SPD Address are marked as 00.

UINT32 **MemorySpdPtr10**

Offset 0x0050 - Memory SPD Pointer Channel 1 Dimm 0 Pointer to SPD data, will be used only when SpdAddressTable SPD Address are marked as 00.

UINT32 **MemorySpdPtr11**

Offset 0x0054 - Memory SPD Pointer Channel 1 Dimm 1 Pointer to SPD data, will be used only when SpdAddressTable SPD Address are marked as 00.

UINT16 **MemorySpdDataLen**

Offset 0x0058 - SPD Data Length Length of SPD Data 0x100:256 Bytes, 0x200:512 Bytes.

UINT8 **DqByteMapCh0 [12]**

Offset 0x005A - Dq Byte Map CH0 Dq byte mapping between CPU and DRAM, Channel 0: board-dependent.

UINT8 **DqByteMapCh1 [12]**

Offset 0x0066 - Dq Byte Map CH1 Dq byte mapping between CPU and DRAM, Channel 1: board-dependent.

UINT8 **DqsMapCpu2DramCh0** [8]

Offset 0x0072 - Dqs Map CPU to DRAM CH 0 Set Dqs mapping relationship between CPU and DRAM, Channel 0: board-dependent.

UINT8 **DqsMapCpu2DramCh1** [8]

Offset 0x007A - Dqs Map CPU to DRAM CH 1 Set Dqs mapping relationship between CPU and DRAM, Channel 1: board-dependent.

UINT16 **RcompResistor** [3]

Offset 0x0082 - RcompResister settings Indicates RcompResister settings: CNL - 0's means MRC auto configured based on Design Guidelines, otherwise input an Ohmic value per segment. [More...](#)

UINT16 **RcompTarget** [5]

Offset 0x0088 - RcompTarget settings RcompTarget settings: CNL - 0's mean MRC auto configured based on Design Guidelines, otherwise input an Ohmic value per segment. [More...](#)

UINT8 **DqPinsInterleaved**

Offset 0x0092 - Dqs Pins Interleaved Setting Indicates DqPinsInterleaved setting: board-dependent \$EN\_DIS.

UINT8 **CaVrefConfig**

Offset 0x0093 - VREF\_CA CA Vref routing: board-dependent 0:VREF\_CA goes to both CH\_A and CH\_B, 1: VREF\_CA to CH\_A and VREF\_DQ\_A to CH\_B, 2:VREF\_CA to CH\_A and VREF\_DQ\_B to CH\_B.

UINT8 **SmramMask**

Offset 0x0094 - Smram Mask The SMM Regions AB-SEG and/or H-SEG reserved 0: Neither, 1:AB-SEG, 2:H-SEG, 3:

Both.

**UINT8 [MrcFastBoot](#)**

Offset 0x0095 - MRC Fast Boot Enables/Disable the MRC fast path thru the MRC \$EN\_DIS.

**UINT8 [RmtPerTask](#)**

Offset 0x0096 - Rank Margin Tool per Task This option enables the user to execute Rank Margin Tool per major training step in the MRC. [More...](#)

**UINT8 [TrainTrace](#)**

Offset 0x0097 - Training Trace This option enables the trained state tracing feature in MRC. [More...](#)

**UINT32 [IedSize](#)**

Offset 0x0098 - Intel Enhanced Debug Intel Enhanced Debug (IED): 0=Disabled, 0x400000=Enabled and 4MB SMRAM occupied 0 : Disable, 0x400000 : Enable.

**UINT32 [TsegSize](#)**

Offset 0x009C - Tseg Size Size of SMRAM memory reserved. [More...](#)

**UINT16 [MmioSize](#)**

Offset 0x00A0 - MMIO Size Size of MMIO space reserved for devices. [More...](#)

**UINT8 [ProbelessTrace](#)**

Offset 0x00A2 - Probeless Trace Probeless Trace: 0=Disabled, 1=Enable. [More...](#)

**UINT8 [GdxclotSize](#)**

Offset 0x00A3 - GDXC IOT SIZE Size of IOT and MOT is in 8 MB chunks.

**UINT8 [GdxcMotSize](#)**

Offset 0x00A4 - GDXC MOT SIZE Size of IOT and MOT is in 8 MB chunks.

**UINT8 [SmbusEnable](#)**

Offset 0x00A5 - Enable SMBus Enable/disable SMBus controller. [More...](#)

**UINT8 [SpdAddressTable](#) [4]**

Offset 0x00A6 - Spd Address Tabl Specify SPD Address table for CH0D0/CH0D1/CH1D0&CH1D1. [More...](#)

**UINT8 [PlatformDebugConsent](#)**

Offset 0x00AA - Platform Debug Consent To 'opt-in' for debug, please select 'Enabled' with the desired debug probe type. [More...](#)

**UINT8 [DciUsb3TypecUfpDbg](#)**

Offset 0x00AB - USB3 Type-C UFP2DFP Kernel/Platform Debug Support This BIOS option enables kernel and platform debug for USB3 interface over a UFP Type-C receptacle, select 'No Change' will do nothing to UFP2DFP setting. [More...](#)

**UINT8 [PchTraceHubMode](#)**

Offset 0x00AC - PCH Trace Hub Mode Select 'Host Debugger' if Trace Hub is used with host debugger tool or 'Target Debugger' if Trace Hub is used by target debugger software or 'Disable' trace hub functionality. [More...](#)

**UINT8 [PchTraceHubMemReg0Size](#)**

Offset 0x00AD - PCH Trace Hub Memory Region 0 buffer Size Specify size of Pch trace memory region 0 buffer, the size can be 0, 1MB, 8MB, 64MB, 128MB, 256MB, 512MB. [More...](#)

**UINT8 [PchTraceHubMemReg1Size](#)**

Offset 0x00AE - PCH Trace Hub Memory Region 1 buffer

**Size** Specify size of Pch trace memory region 1 buffer, the size can be 0, 1MB, 8MB, 64MB, 128MB, 256MB, 512MB.  
[More...](#)

**UINT8 [PchPreMemRsvd](#) [9]**

Offset 0x00AF - PchPreMemRsvd Reserved for PCH Pre-Mem Reserved \$EN\_DIS.

**UINT8 [IgdDvmt50PreAlloc](#)**

Offset 0x00B8 - Internal Graphics Pre-allocated Memory  
Size of memory preallocated for internal graphics. [More...](#)

**UINT8 [InternalGfx](#)**

Offset 0x00B9 - Internal Graphics Enable/disable internal graphics. [More...](#)

**UINT8 [ApertureSize](#)**

Offset 0x00BA - Aperture Size Select the Aperture Size.  
[More...](#)

**UINT8 [UserBd](#)**

Offset 0x00BB - Board Type MrcBoardType, Options are  
0=Mobile/Mobile Halo, 1=Desktop/DT Halo,  
5=ULT/ULX/Mobile Halo, 7=UP Server 0:Mobile/Mobile  
Halo, 1:Desktop/DT Halo, 5:ULT/ULX/Mobile Halo, 7:UP  
Server.

**UINT8 [SaGv](#)**

Offset 0x00BC - SA GV System Agent dynamic frequency support and when enabled memory will be training at two different frequencies. [More...](#)

**UINT8 [UnusedUpdSpace0](#)**

Offset 0x00BD.

**UINT16 [DdrFreqLimit](#)**

Offset 0x00BE - DDR Frequency Limit Maximum Memory

Frequency Selections in Mhz. [More...](#)

**UINT16 FreqSaGvLow**

Offset 0x00C0 - Low Frequency SAGV Low Frequency Selections in Mhz. [More...](#)

**UINT16 FreqSaGvMid**

Offset 0x00C2 - Mid Frequency SAGV Mid Frequency Selections in Mhz. [More...](#)

**UINT8 RMT**

Offset 0x00C4 - Rank Margin Tool Enable/disable Rank Margin Tool. [More...](#)

**UINT8 DisableDimmChannel0**

Offset 0x00C5 - Channel A DIMM Control Channel A DIMM Control Support - Enable or Disable Dimms on Channel A. [More...](#)

**UINT8 DisableDimmChannel1**

Offset 0x00C6 - Channel B DIMM Control Channel B DIMM Control Support - Enable or Disable Dimms on Channel B. [More...](#)

**UINT8 ScramblerSupport**

Offset 0x00C7 - Scrambler Support This option enables data scrambling in memory. [More...](#)

**UINT8 SkipMpInit**

Offset 0x00C8 - Skip Multi-Processor Initialization When this is skipped, boot loader must initialize processors before SiliconInit API. [More...](#)

**UINT8 UnusedUpdSpace1 [15]**

Offset 0x00C9.

**UINT8 SpdProfileSelected**

Offset 0x00D8 - SPD Profile Selected Select DIMM timing profile. [More...](#)

**UINT8 RefClk**

Offset 0x00D9 - Memory Reference Clock 100MHz, 133MHz. [More...](#)

**UINT16 VddVoltage**

Offset 0x00DA - Memory Voltage Memory Voltage Override (Vddq). [More...](#)

**UINT8 Ratio**

Offset 0x00DC - Memory Ratio Automatic or the frequency will equal ratio times reference clock. [More...](#)

**UINT8 OddRatioMode**

Offset 0x00DD - QCLK Odd Ratio Adds 133 or 100 MHz to QCLK frequency, depending on RefClk \$EN\_DIS.

**UINT8 tCL**

Offset 0x00DE - tCL CAS Latency, 0: AUTO, max: 31.

**UINT8 tCWL**

Offset 0x00DF - tCWL Min CAS Write Latency Delay Time, 0: AUTO, max: 34.

**UINT8 tRCDtRP**

Offset 0x00E0 - tRCD/tRP RAS to CAS delay time and Row Precharge delay time, 0: AUTO, max: 63.

**UINT8 tRRD**

Offset 0x00E1 - tRRD Min Row Active to Row Active Delay Time, 0: AUTO, max: 15.

**UINT16 tFAW**

Offset 0x00E2 - tFAW Min Four Activate Window Delay Time, 0: AUTO, max: 63.

**UINT16 [tRAS](#)**

Offset 0x00E4 - tRAS RAS Active Time, 0: AUTO, max: 64.

**UINT16 [tREFI](#)**

Offset 0x00E6 - tREFI Refresh Interval, 0: AUTO, max: 65535.

**UINT16 [tRFC](#)**

Offset 0x00E8 - tRFC Min Refresh Recovery Delay Time, 0: AUTO, max: 1023.

**UINT8 [tRTP](#)**

Offset 0x00EA - tRTP Min Internal Read to Precharge Command Delay Time, 0: AUTO, max: 15. [More...](#)

**UINT8 [tWR](#)**

Offset 0x00EB - tWR Min Write Recovery Time, 0: AUTO, legal values: 5, 6, 7, 8, 10, 12, 14, 16, 18, 20, 24, 30, 34, 40  
0:Auto, 5:5, 6:6, 7:7, 8:8, 10:10, 12:12, 14:14, 16:16, 18:18, 20:20, 24:24, 30:30, 34:34, 40:40.

**UINT8 [tWTR](#)**

Offset 0x00EC - tWTR Min Internal Write to Read Command Delay Time, 0: AUTO, max: 28.

**UINT8 [NModeSupport](#)**

Offset 0x00ED - NMode System command rate, range 0-2, 0 means auto, 1 = 1N, 2 = 2N.

**UINT8 [DIBwEn0](#)**

Offset 0x00EE - DIBwEn[0] DIBwEn[0], for 1067 (0..7)

**UINT8 [DIBwEn1](#)**

Offset 0x00EF - DII BwEn[1] DII BwEn[1], for 1333 (0..7)

UINT8 **DII BwEn2**

Offset 0x00F0 - DII BwEn[2] DII BwEn[2], for 1600 (0..7)

UINT8 **DII BwEn3**

Offset 0x00F1 - DII BwEn[3] DII BwEn[3], for 1867 and up (0..7)

UINT8 **IsvtIoPort**

Offset 0x00F2 - ISVT IO Port Address ISVT IO Port Address. [More...](#)

UINT8 **CpuTraceHubMode**

Offset 0x00F3 - CPU Trace Hub Mode Select 'Target Debugger' if Trace Hub is used by target debugger software or 'Disable' trace hub functionality. [More...](#)

UINT8 **CpuTraceHubMemReg0Size**

Offset 0x00F4 - CPU Trace Hub Memory Region 0 CPU Trace Hub Memory Region 0, The available memory size is : 0MB, 1MB, 8MB, 64MB, 128MB, 256MB, 512MB. [More...](#)

UINT8 **CpuTraceHubMemReg1Size**

Offset 0x00F5 - CPU Trace Hub Memory Region 1 CPU Trace Hub Memory Region 1. [More...](#)

UINT8 **PeciC10Reset**

Offset 0x00F6 - Enable or Disable Peci C10 Reset command Enable or Disable Peci C10 Reset command. [More...](#)

UINT8 **PeciSxReset**

Offset 0x00F7 - Enable or Disable Peci Sx Reset command Enable or Disable Peci Sx Reset command; 0: **Disable**; 1: Enable. [More...](#)

**UINT8 UnusedUpdSpace2 [4]**

Offset 0x00F8.

**UINT8 PchHdaEnable**

Offset 0x00FC - Enable Intel HD Audio (Azalia) 0: Disable, 1: Enable (Default) Azalia controller \$EN\_DIS.

**UINT8 PchIshEnable**

Offset 0x00FD - Enable PCH ISH Controller 0: Disable, 1: Enable (Default) ISH Controller \$EN\_DIS.

**UINT8 HeciTimeouts**

Offset 0x00FE - HECL Timeouts 0: Disable, 1: Enable (Default) timeout check for HECL \$EN\_DIS.

**UINT8 UnusedUpdSpace3**

Offset 0x00FF.

**UINT32 Heci1BarAddress**

Offset 0x0100 - HECL1 BAR address BAR address of HECL1.

**UINT32 Heci2BarAddress**

Offset 0x0104 - HECL2 BAR address BAR address of HECL2.

**UINT32 Heci3BarAddress**

Offset 0x0108 - HECL3 BAR address BAR address of HECL3.

**UINT16 SgDelayAfterPwrEn**

Offset 0x010C - SG dGPU Power Delay SG dGPU delay interval after power enabling: 0=Minimal, 1000=Maximum, default is 300=300 microseconds.

**UINT16 SgDelayAfterHoldReset**

Offset 0x010E - SG dGPU Reset Delay SG dGPU delay

interval for Reset complete: 0=Minimal, 1000=Maximum, default is 100=100 microseconds.

**UINT16 [MmioSizeAdjustment](#)**

Offset 0x0110 - MMIO size adjustment for AUTO mode  
Positive number means increasing MMIO size, Negative value means decreasing MMIO size: 0 (Default)=no change to AUTO mode MMIO size.

**UINT8 [DmiGen3ProgramStaticEq](#)**

Offset 0x0112 - Enable/Disable DMI GEN3 Static EQ Phase1 programming Program DMI Gen3 EQ Phase1 Static Presets. [More...](#)

**UINT8 [Peg0Enable](#)**

Offset 0x0113 - Enable/Disable PEG 0 Disabled(0x0): Disable PEG Port, Enabled(0x1): Enable PEG Port (If Silicon SKU permits it), Auto(0x2)(Default): If an endpoint is present, enable the PEG Port, Disable otherwise 0:Disable, 1:Enable, 2:AUTO.

**UINT8 [Peg1Enable](#)**

Offset 0x0114 - Enable/Disable PEG 1 Disabled(0x0): Disable PEG Port, Enabled(0x1): Enable PEG Port (If Silicon SKU permits it), Auto(0x2)(Default): If an endpoint is present, enable the PEG Port, Disable otherwise 0:Disable, 1:Enable, 2:AUTO.

**UINT8 [Peg2Enable](#)**

Offset 0x0115 - Enable/Disable PEG 2 Disabled(0x0): Disable PEG Port, Enabled(0x1): Enable PEG Port (If Silicon SKU permits it), Auto(0x2)(Default): If an endpoint is present, enable the PEG Port, Disable otherwise 0:Disable, 1:Enable, 2:AUTO.

**UINT8 [Peg3Enable](#)**

Offset 0x0116 - Enable/Disable PEG 3 Disabled(0x0): Disable PEG Port, Enabled(0x1): Enable PEG Port (If

Silicon SKU permits it), Auto(0x2)(Default): If an endpoint is present, enable the PEG Port, Disable otherwise 0:Disable, 1:Enable, 2:AUTO.

#### UINT8 **Peg0MaxLinkSpeed**

Offset 0x0117 - PEG 0 Max Link Speed Auto (Default)(0x0): Maximum possible link speed, Gen1(0x1): Limit Link to Gen1 Speed, Gen2(0x2): Limit Link to Gen2 Speed, Gen3(0x3):Limit Link to Gen3 Speed 0:Auto, 1:Gen1, 2:Gen2, 3:Gen3.

#### UINT8 **Peg1MaxLinkSpeed**

Offset 0x0118 - PEG 1 Max Link Speed Auto (Default)(0x0): Maximum possible link speed, Gen1(0x1): Limit Link to Gen1 Speed, Gen2(0x2): Limit Link to Gen2 Speed, Gen3(0x3):Limit Link to Gen3 Speed 0:Auto, 1:Gen1, 2:Gen2, 3:Gen3.

#### UINT8 **Peg2MaxLinkSpeed**

Offset 0x0119 - PEG 2 Max Link Speed Auto (Default)(0x0): Maximum possible link speed, Gen1(0x1): Limit Link to Gen1 Speed, Gen2(0x2): Limit Link to Gen2 Speed, Gen3(0x3):Limit Link to Gen3 Speed 0:Auto, 1:Gen1, 2:Gen2, 3:Gen3.

#### UINT8 **Peg3MaxLinkSpeed**

Offset 0x011A - PEG 3 Max Link Speed Auto (Default)(0x0): Maximum possible link speed, Gen1(0x1): Limit Link to Gen1 Speed, Gen2(0x2): Limit Link to Gen2 Speed, Gen3(0x3):Limit Link to Gen3 Speed 0:Auto, 1:Gen1, 2:Gen2, 3:Gen3.

#### UINT8 **Peg0MaxLinkWidth**

Offset 0x011B - PEG 0 Max Link Width Auto (Default)(0x0): Maximum possible link width, (0x1): Limit Link to x1, (0x2): Limit Link to x2, (0x3):Limit Link to x4, (0x4): Limit Link to x8 0:Auto, 1:x1, 2:x2, 3:x4, 4:x8.

**UINT8 Peg1MaxLinkWidth**

Offset 0x011C - PEG 1 Max Link Width Auto (Default)(0x0): Maximum possible link width, (0x1): Limit Link to x1, (0x2): Limit Link to x2, (0x3):Limit Link to x4 0:Auto, 1:x1, 2:x2, 3:x4.

**UINT8 Peg2MaxLinkWidth**

Offset 0x011D - PEG 2 Max Link Width Auto (Default)(0x0): Maximum possible link width, (0x1): Limit Link to x1, (0x2): Limit Link to x2 0:Auto, 1:x1, 2:x2.

**UINT8 Peg3MaxLinkWidth**

Offset 0x011E - PEG 3 Max Link Width Auto (Default)(0x0): Maximum possible link width, (0x1): Limit Link to x1, (0x2): Limit Link to x2 0:Auto, 1:x1, 2:x2.

**UINT8 Peg0PowerDownUnusedLanes**

Offset 0x011F - Power down unused lanes on PEG 0 (0x0): Do not power down any lane, (0x1): Bios will power down unused lanes based on the max possible link width 0:No power saving, 1:Auto.

**UINT8 Peg1PowerDownUnusedLanes**

Offset 0x0120 - Power down unused lanes on PEG 1 (0x0): Do not power down any lane, (0x1): Bios will power down unused lanes based on the max possible link width 0:No power saving, 1:Auto.

**UINT8 Peg2PowerDownUnusedLanes**

Offset 0x0121 - Power down unused lanes on PEG 2 (0x0): Do not power down any lane, (0x1): Bios will power down unused lanes based on the max possible link width 0:No power saving, 1:Auto.

**UINT8 Peg3PowerDownUnusedLanes**

Offset 0x0122 - Power down unused lanes on PEG 3 (0x0):

Do not power down any lane, (0x1): Bios will power down unused lanes based on the max possible link width 0:No power saving, 1:Auto.

UINT8 **InitPcieAspmAfterOeprom**

Offset 0x0123 - PCIe ASPM programming will happen in relation to the Oeprom Select when PCIe ASPM programming will happen in relation to the Oeprom. [More...](#)

UINT8 **PegDisableSpreadSpectrumClocking**

Offset 0x0124 - PCIe Disable Spread Spectrum Clocking PCIe Disable Spread Spectrum Clocking. [More...](#)

UINT8 **UnusedUpdSpace4** [3]

Offset 0x0125.

UINT8 **DmiGen3RootPortPreset** [8]

Offset 0x0128 - DMI Gen3 Root port preset values per lane  
Used for programming DMI Gen3 preset values per lane.  
[More...](#)

UINT8 **DmiGen3EndPointPreset** [8]

Offset 0x0130 - DMI Gen3 End port preset values per lane  
Used for programming DMI Gen3 preset values per lane.  
[More...](#)

UINT8 **DmiGen3EndPointHint** [8]

Offset 0x0138 - DMI Gen3 End port Hint values per lane  
Used for programming DMI Gen3 Hint values per lane.  
[More...](#)

UINT8 **DmiGen3RxCtlePeaking** [4]

Offset 0x0140 - DMI Gen3 RxCTLEp per-Bundle control  
Range: 0-15, 0 is default for each bundle, must be specified based upon platform design.

**UINT8 [TvbRatioClipping](#)**

Offset 0x0144 - Thermal Velocity Boost Ratio clipping  
0(Default): Disabled, 1: Enabled. [More...](#)

**UINT8 [TvbVoltageOptimization](#)**

Offset 0x0145 - Thermal Velocity Boost voltage optimization  
0: Disabled, 1: Enabled(Default). [More...](#)

**UINT8 [UnusedUpdSpace5 \[2\]](#)**

Offset 0x0146.

**UINT8 [PegGen3RxCtlePeaking \[10\]](#)**

Offset 0x0148 - PEG Gen3 RxCTLEp per-Bundle control  
Range: 0-15, 12 is default for each bundle, must be  
specified based upon platform design.

**UINT32 [PegDataPtr](#)**

Offset 0x0152 - Memory data pointer for saved preset  
search results The reference code will store the Gen3  
Preset Search results in the SaDataHob's PegData  
structure (SA\_PEG\_DATA) and platform code can  
save/restore this data to skip preset search in the following  
boots. [More...](#)

**UINT8 [PegGpioData \[28\]](#)**

Offset 0x0156 - PEG PERST# GPIO information The  
reference code will use the information in this structure in  
order to reset PCIe Gen3 devices during equalization, if  
necessary.

**UINT8 [PegRootPortHPE \[4\]](#)**

Offset 0x0172 - PCIe Hot Plug Enable/Disable per port  
0(Default): Disable, 1: Enable.

**UINT8 [DmiDeEmphasis](#)**

Offset 0x0176 - DeEmphasis control for DMI DeEmphasis  
control for DMI. [More...](#)

**UINT8 PrimaryDisplay**

Offset 0x0177 - Selection of the primary display device  
0=iGFX, 1=PEG, 2=PCIe Graphics on PCH,  
3(Default)=AUTO, 4=Switchable Graphics 0:iGFX, 1:PEG,  
2:PCIe Graphics on PCH, 3:AUTO, 4:Switchable Graphics.

**UINT16 GttSize**

Offset 0x0178 - Selection of iGFX GTT Memory size  
1=2MB, 2=4MB, 3=8MB, Default is 3 1:2MB, 2:4MB,  
3:8MB.

**UINT32 GmAdr**

Offset 0x017A - Temporary MMIO address for GMADR The reference code will use this as Temporary MMIO address space to access GMADR Registers. Platform should provide conflict free Temporary MMIO Range: GmAdr to (GmAdr + ApertureSize). [More...](#)

**UINT32 GttMmAdr**

Offset 0x017E - Temporary MMIO address for GTTMMADR The reference code will use this as Temporary MMIO address space to access GTTMMADR Registers. Platform should provide conflict free Temporary MMIO Range: GttMmAdr to (GttMmAdr + 2MB MMIO + 6MB Reserved + GttSize). [More...](#)

**UINT8 PsmiRegionSize**

Offset 0x0182 - Selection of PSMI Region size 0=32MB, 1=288MB, 2=544MB, 3=800MB, 4=1024MB Default is 0 0:32MB, 1:288MB, 2:544MB, 3:800MB, 4:1024MB.

**UINT8 SaRtd3Pcie0Gpio [24]**

Offset 0x0183 - Switchable Graphics GPIO information for PEG 0 Switchable Graphics GPIO information for PEG 0, for Reset, power and wake GPIOs.

**UINT8 SaRtd3Pcie1Gpio [24]**

Offset 0x019B - Switchable Graphics GPIO information for PEG 1 Switchable Graphics GPIO information for PEG 1, for Reset, power and wake GPIOs.

**UINT8 SaRtd3Pcie2Gpio [24]**

Offset 0x01B3 - Switchable Graphics GPIO information for PEG 2 Switchable Graphics GPIO information for PEG 2, for Reset, power and wake GPIOs.

**UINT8 SaRtd3Pcie3Gpio [24]**

Offset 0x01CB - Switchable Graphics GPIO information for PEG 3 Switchable Graphics GPIO information for PEG 3, for Reset, power and wake GPIOs.

**UINT8 TxtImplemented**

Offset 0x01E3 - Enable/Disable MRC TXT dependency  
When enabled MRC execution will wait for TXT initialization to be done first. [More...](#)

**UINT8 SaOcSupport**

Offset 0x01E4 - Enable/Disable SA OcSupport  
Enable SA OcSupport, Disable(Default): Disable SA OcSupport \$EN\_DIS.

**UINT8 GtVoltageMode**

Offset 0x01E5 - GT slice Voltage Mode 0(Default): Adaptive, 1: Override 0: Adaptive, 1: Override.

**UINT8 GtMaxOcRatio**

Offset 0x01E6 - Maximum GTs turbo ratio override  
0(Default)=Minimal/Auto, 60=Maximum.

**UINT16 GtVoltageOffset**

Offset 0x01E7 - The voltage offset applied to GT slice  
0(Default)=Minimal, 1000=Maximum.

**UINT16 GtVoltageOverride**  
Offset 0x01E9 - The GT slice voltage override which is applied to the entire range of GT frequencies  
0(Default)=Minimal, 2000=Maximum.

**UINT16 GtExtraTurboVoltage**  
Offset 0x01EB - adaptive voltage applied during turbo frequencies 0(Default)=Minimal, 2000=Maximum.

**UINT16 SaVoltageOffset**  
Offset 0x01ED - voltage offset applied to the SA  
0(Default)=Minimal, 1000=Maximum.

**UINT8 RootPortIndex**  
Offset 0x01EF - PCIe root port Function number for Switchable Graphics dGPU Root port Index number to indicate which PCIe root port has dGPU.

**UINT8 RealtimeMemoryTiming**  
Offset 0x01F0 - Realtime Memory Timing 0(Default):  
Disabled, 1: Enabled. [More...](#)

**UINT8 SalpuEnable**  
Offset 0x01F1 - Enable/Disable SA IPU Enable(Default):  
Enable SA IPU, Disable: Disable SA IPU \$EN\_DIS.

**UINT8 SalpulmrConfiguration**  
Offset 0x01F2 - IPU IMR Configuration 0:IPU Camera,  
1:IPU Gen Default is 0 0:IPU Camera, 1:IPU Gen.

**UINT8 GtPsmiSupport**  
Offset 0x01F3 - Selection of PSMI Support On/Off  
0(Default) = FALSE, 1 = TRUE. [More...](#)

**UINT8 GtusVoltageMode**  
Offset 0x01F4 - GT unslice Voltage Mode 0(Default):  
Adaptive, 1: Override 0: Adaptive, 1: Override.

**UINT16 GtusVoltageOffset**

Offset 0x01F5 - voltage offset applied to GT unslice  
0(Default)=Minimal, 2000=Maximum.

**UINT16 GtusVoltageOverride**

Offset 0x01F7 - GT unslice voltage override which is applied to the entire range of GT frequencies  
0(Default)=Minimal, 2000=Maximum.

**UINT16 GtusExtraTurboVoltage**

Offset 0x01F9 - adaptive voltage applied during turbo frequencies 0(Default)=Minimal, 2000=Maximum.

**UINT8 GtusMaxOcRatio**

Offset 0x01FB - Maximum GTus turbo ratio override  
0(Default)=Minimal, 60=Maximum.

**UINT8 SaPreMemProductionRsvd [4]**

Offset 0x01FC - SaPreMemProductionRsvd Reserved for SA Pre-Mem Production \$EN\_DIS.

**UINT8 BistOnReset**

Offset 0x0200 - BIST on Reset Enable or Disable BIST on Reset; **0: Disable**; 1: Enable. More...

**UINT8 SkipStopPbet**

Offset 0x0201 - Skip Stop PBET Timer Enable/Disable Skip Stop PBET Timer; **0: Disable**; 1: Enable \$EN\_DIS.

**UINT8 EnableC6Dram**

Offset 0x0202 - C6DRAM power gating feature This policy indicates whether or not BIOS should allocate PRMRR memory for C6DRAM power gating feature. More...

**UINT8 OcSupport**

Offset 0x0203 - Over clocking support Over clocking support; **0: Disable**; 1: Enable \$EN\_DIS.

#### UINT8 **OcLock**

Offset 0x0204 - Over clocking Lock Over clocking Lock Enable/Disable; **0: Disable**; 1: Enable. [More...](#)

#### UINT8 **CoreMaxOcRatio**

Offset 0x0205 - Maximum Core Turbo Ratio Override Maximum core turbo ratio override allows to increase CPU core frequency beyond the fused max turbo ratio limit. [More...](#)

#### UINT8 **CoreVoltageMode**

Offset 0x0206 - Core voltage mode Core voltage mode; **0: Adaptive**; 1: Override. [More...](#)

#### UINT8 **DisableMtrrProgram**

Offset 0x0207 - Program Cache Attributes Program Cache Attributes; **0: Program**; 1: Disable Program. [More...](#)

#### UINT8 **RingMaxOcRatio**

Offset 0x0208 - Maximum clr turbo ratio override Maximum clr turbo ratio override allows to increase CPU clr frequency beyond the fused max turbo ratio limit. [More...](#)

#### UINT8 **HyperThreading**

Offset 0x0209 - Hyper Threading Enable/Disable Enable or Disable Hyper Threading; 0: Disable; **1: Enable** \$EN\_DIS.

#### UINT8 **CpuRatio**

Offset 0x020A - CPU ratio value CPU ratio value. [More...](#)

#### UINT8 **BootFrequency**

Offset 0x020B - Boot frequency Sets the boot frequency starting from reset vector. [More...](#)

**UINT8 ActiveCoreCount**

Offset 0x020C - Number of active cores Number of active cores(Depends on Number of cores). [More...](#)

**UINT8 FClkFrequency**

Offset 0x020D - Processor Early Power On Configuration FCLK setting **0: 800 MHz (ULT/ULX)**. [More...](#)

**UINT8 JtagC10PowerGateDisable**

Offset 0x020E - Set JTAG power in C10 and deeper power states False: JTAG is power gated in C10 state. [More...](#)

**UINT8 VmxEnable**

Offset 0x020F - Enable or Disable VMX Enable or Disable VMX; 0: Disable; **1: Enable**. [More...](#)

**UINT8 Avx2RatioOffset**

Offset 0x0210 - AVX2 Ratio Offset 0(Default)= No Offset. [More...](#)

**UINT8 Avx3RatioOffset**

Offset 0x0211 - AVX3 Ratio Offset 0(Default)= No Offset. [More...](#)

**UINT8 BclkAdaptiveVoltage**

Offset 0x0212 - BCLK Adaptive Voltage Enable When enabled, the CPU V/F curves are aware of BCLK frequency when calculated. [More...](#)

**UINT8 CorePllVoltageOffset**

Offset 0x0213 - Core PLL voltage offset Core PLL voltage offset. [More...](#)

**UINT16 CoreVoltageOverride**

Offset 0x0214 - core voltage override The core voltage override which is applied to the entire range of cpu core frequencies. [More...](#)

**UINT16 CoreVoltageAdaptive**

Offset 0x0216 - Core Turbo voltage Adaptive Extra Turbo voltage applied to the cpu core when the cpu is operating in turbo mode. [More...](#)

**UINT16 CoreVoltageOffset**

Offset 0x0218 - Core Turbo voltage Offset The voltage offset applied to the core while operating in turbo mode. Valid Range 0 to 1000.

**UINT8 RingDownBin**

Offset 0x021A - Ring Downbin Ring Downbin enable/disable. [More...](#)

**UINT8 RingVoltageMode**

Offset 0x021B - Ring voltage mode Ring voltage mode; 0: **Adaptive**; 1: Override. [More...](#)

**UINT16 RingVoltageOverride**

Offset 0x021C - Ring voltage override The ring voltage override which is applied to the entire range of cpu ring frequencies. [More...](#)

**UINT16 RingVoltageAdaptive**

Offset 0x021E - Ring Turbo voltage Adaptive Extra Turbo voltage applied to the cpu ring when the cpu is operating in turbo mode. [More...](#)

**UINT16 RingVoltageOffset**

Offset 0x0220 - Ring Turbo voltage Offset The voltage offset applied to the ring while operating in turbo mode. [More...](#)

**UINT8 TjMaxOffset**

Offset 0x0222 - TjMax Offset TjMax offset. Specified value here is clipped by pCode (125 - TjMax Offset) to support

TjMax in the range of 62 to 115 deg Celsius. More...

UINT8 **BiosGuard**

Offset 0x0223 - BiosGuard Enable/Disable. More...

UINT8 **BiosGuardToolsInterface**

Offset 0x0224.

UINT8 **EnableSgx**

Offset 0x0225 - EnableSgx Enable/Disable. More...

UINT8 **Txt**

Offset 0x0226 - Txt Enable/Disable. More...

UINT8 **UnusedUpdSpace6**

Offset 0x0227.

UINT32 **PrmrrSize**

Offset 0x0228 - PrmrrSize 0=Invalid, 32MB=0x2000000,  
64MB=0x4000000, 128MB=0x8000000,  
256MB=0x10000000.

UINT32 **SinitMemorySize**

Offset 0x022C - SinitMemorySize Enable/Disable. More...

UINT32 **TxtHeapMemorySize**

Offset 0x0230 - TxtHeapMemorySize Enable/Disable.  
More...

UINT32 **TxtDprMemorySize**

Offset 0x0234 - TxtDprMemorySize Enable/Disable. More...

UINT64 **TxtDprMemoryBase**

Offset 0x0238 - TxtDprMemoryBase Enable/Disable.  
More...

**UINT32 BiosAcmBase**  
Offset 0x0240 - BiosAcmBase Enable/Disable. [More...](#)

**UINT32 BiosAcmSize**  
Offset 0x0244 - BiosAcmSize Enable/Disable. [More...](#)

**UINT32 ApStartupBase**  
Offset 0x0248 - ApStartupBase Enable/Disable. [More...](#)

**UINT32 TgaSize**  
Offset 0x024C - TgaSize Enable/Disable. [More...](#)

**UINT64 TxtLcpPdBase**  
Offset 0x0250 - TxtLcpPdBase Enable/Disable. [More...](#)

**UINT64 TxtLcpPdSize**  
Offset 0x0258 - TxtLcpPdSize Enable/Disable. [More...](#)

**UINT8 IsTPMPresence**  
Offset 0x0260 - IsTPMPresence IsTPMPresence default values.

**UINT8 ReservedSecurityPreMem [15]**  
Offset 0x0261 - ReservedSecurityPreMem Reserved for Security Pre-Mem \$EN\_DIS.

**UINT8 PchPcieHsioRxSetCtleEnable [24]**  
Offset 0x0270 - Enable PCH HSIO PCIE Rx Set Ctle Enable PCH PCIe Gen 3 Set CTLE Value.

**UINT8 PchPcieHsioRxSetCtle [24]**  
Offset 0x0288 - PCH HSIO PCIE Rx Set Ctle Value PCH PCIe Gen 3 Set CTLE Value.

**UINT8 PchPcieHsioTxGen1DownscaleAmpEnable [24]**  
Offset 0x02A0 - Enble PCH HSIO PCIE TX Gen 1

Downscale Amplitude Adjustment value override 0: Disable;  
1: Enable.

- |       |  |
|-------|--|
| UINT8 | <b>PchPcieHsioTxGen1DownscaleAmp [24]</b><br>Offset 0x02B8 - PCH HSIO PCIE Gen 2 TX Output<br>Downscale Amplitude Adjustment value PCH PCIe Gen 2<br>TX Output Downscale Amplitude Adjustment value. |
| UINT8 | <b>PchPcieHsioTxGen2DownscaleAmpEnable [24]</b><br>Offset 0x02D0 - Enable PCH HSIO PCIE TX Gen 2<br>Downscale Amplitude Adjustment value override 0: Disable;<br>1: Enable.                          |
| UINT8 | <b>PchPcieHsioTxGen2DownscaleAmp [24]</b><br>Offset 0x02E8 - PCH HSIO PCIE Gen 2 TX Output<br>Downscale Amplitude Adjustment value PCH PCIe Gen 2<br>TX Output Downscale Amplitude Adjustment value. |
| UINT8 | <b>PchPcieHsioTxGen3DownscaleAmpEnable [24]</b><br>Offset 0x0300 - Enable PCH HSIO PCIE TX Gen 3<br>Downscale Amplitude Adjustment value override 0: Disable;<br>1: Enable.                          |
| UINT8 | <b>PchPcieHsioTxGen3DownscaleAmp [24]</b><br>Offset 0x0318 - PCH HSIO PCIE Gen 3 TX Output<br>Downscale Amplitude Adjustment value PCH PCIe Gen 3<br>TX Output Downscale Amplitude Adjustment value. |
| UINT8 | <b>PchPcieHsioTxGen1DeEmphEnable [24]</b><br>Offset 0x0330 - Enable PCH HSIO PCIE Gen 1 TX Output<br>De-Emphasis Adjustment Setting value override 0: Disable;<br>1: Enable.                         |
| UINT8 | <b>PchPcieHsioTxGen1DeEmph [24]</b><br>Offset 0x0348 - PCH HSIO PCIE Gen 1 TX Output De-<br>Emphasis Adjustment value PCH PCIe Gen 1 TX Output<br>De-Emphasis Adjustment Setting.                    |

**UINT8 PchPcieHsioTxGen2DeEmph3p5Enable [24]**  
Offset 0x0360 - Enable PCH HSIO PCIE Gen 2 TX Output  
-3.5dB De-Emphasis Adjustment Setting value override 0:  
Disable; 1: Enable.

**UINT8 PchPcieHsioTxGen2DeEmph3p5 [24]**  
Offset 0x0378 - PCH HSIO PCIE Gen 2 TX Output -3.5dB  
De-Emphasis Adjustment value PCH PCIe Gen 2 TX  
Output -3.5dB De-Emphasis Adjustment Setting.

**UINT8 PchPcieHsioTxGen2DeEmph6p0Enable [24]**  
Offset 0x0390 - Enable PCH HSIO PCIE Gen 2 TX Output  
-6.0dB De-Emphasis Adjustment Setting value override 0:  
Disable; 1: Enable.

**UINT8 PchPcieHsioTxGen2DeEmph6p0 [24]**  
Offset 0x03A8 - PCH HSIO PCIE Gen 2 TX Output -6.0dB  
De-Emphasis Adjustment value PCH PCIe Gen 2 TX  
Output -6.0dB De-Emphasis Adjustment Setting.

**UINT8 PchSataHsioRxGen1EqBoostMagEnable [8]**  
Offset 0x03C0 - Enable PCH HSIO SATA Receiver  
Equalization Boost Magnitude Adjustment Value override 0:  
Disable; 1: Enable.

**UINT8 PchSataHsioRxGen1EqBoostMag [8]**  
Offset 0x03C8 - PCH HSIO SATA 1.5 Gb/s Receiver  
Equalization Boost Magnitude Adjustment value PCH HSIO  
SATA 1.5 Gb/s Receiver Equalization Boost Magnitude  
Adjustment value.

**UINT8 PchSataHsioRxGen2EqBoostMagEnable [8]**  
Offset 0x03D0 - Enable PCH HSIO SATA Receiver  
Equalization Boost Magnitude Adjustment Value override 0:  
Disable; 1: Enable.

**UINT8 PchSataHsioRxGen2EqBoostMag [8]**  
Offset 0x03D8 - PCH HSIO SATA 3.0 Gb/s Receiver  
Equalization Boost Magnitude Adjustment value PCH HSIO  
SATA 3.0 Gb/s Receiver Equalization Boost Magnitude  
Adjustment value.

**UINT8 PchSataHsioRxGen3EqBoostMagEnable [8]**  
Offset 0x03E0 - Enable PCH HSIO SATA Receiver  
Equalization Boost Magnitude Adjustment Value override 0:  
Disable; 1: Enable.

**UINT8 PchSataHsioRxGen3EqBoostMag [8]**  
Offset 0x03E8 - PCH HSIO SATA 6.0 Gb/s Receiver  
Equalization Boost Magnitude Adjustment value PCH HSIO  
SATA 6.0 Gb/s Receiver Equalization Boost Magnitude  
Adjustment value.

**UINT8 PchSataHsioTxGen1DownscaleAmpEnable [8]**  
Offset 0x03F0 - Enable PCH HSIO SATA 1.5 Gb/s TX  
Output Downscale Amplitude Adjustment value override 0:  
Disable; 1: Enable.

**UINT8 PchSataHsioTxGen1DownscaleAmp [8]**  
Offset 0x03F8 - PCH HSIO SATA 1.5 Gb/s TX Output  
Downscale Amplitude Adjustment value PCH HSIO SATA  
1.5 Gb/s TX Output Downscale Amplitude Adjustment  
value.

**UINT8 PchSataHsioTxGen2DownscaleAmpEnable [8]**  
Offset 0x0400 - Enable PCH HSIO SATA 3.0 Gb/s TX  
Output Downscale Amplitude Adjustment value override 0:  
Disable; 1: Enable.

**UINT8 PchSataHsioTxGen2DownscaleAmp [8]**  
Offset 0x0408 - PCH HSIO SATA 3.0 Gb/s TX Output  
Downscale Amplitude Adjustment value PCH HSIO SATA  
3.0 Gb/s TX Output Downscale Amplitude Adjustment  
value.

- UINT8 **PchSataHsioTxGen3DownscaleAmpEnable** [8]  
Offset 0x0410 - Enable PCH HSIO SATA 6.0 Gb/s TX  
Output Downscale Amplitude Adjustment value override 0:  
Disable; 1: Enable.
- UINT8 **PchSataHsioTxGen3DownscaleAmp** [8]  
Offset 0x0418 - PCH HSIO SATA 6.0 Gb/s TX Output  
Downscale Amplitude Adjustment value PCH HSIO SATA  
6.0 Gb/s TX Output Downscale Amplitude Adjustment  
value.
- UINT8 **PchSataHsioTxGen1DeEmphEnable** [8]  
Offset 0x0420 - Enable PCH HSIO SATA 1.5 Gb/s TX  
Output De-Emphasis Adjustment Setting value override 0:  
Disable; 1: Enable.
- UINT8 **PchSataHsioTxGen1DeEmph** [8]  
Offset 0x0428 - PCH HSIO SATA 1.5 Gb/s TX Output De-  
Emphasis Adjustment Setting PCH HSIO SATA 1.5 Gb/s TX  
Output De-Emphasis Adjustment Setting.
- UINT8 **PchSataHsioTxGen2DeEmphEnable** [8]  
Offset 0x0430 - Enable PCH HSIO SATA 3.0 Gb/s TX  
Output De-Emphasis Adjustment Setting value override 0:  
Disable; 1: Enable.
- UINT8 **PchSataHsioTxGen2DeEmph** [8]  
Offset 0x0438 - PCH HSIO SATA 3.0 Gb/s TX Output De-  
Emphasis Adjustment Setting PCH HSIO SATA 3.0 Gb/s TX  
Output De-Emphasis Adjustment Setting.
- UINT8 **PchSataHsioTxGen3DeEmphEnable** [8]  
Offset 0x0440 - Enable PCH HSIO SATA 6.0 Gb/s TX  
Output De-Emphasis Adjustment Setting value override 0:  
Disable; 1: Enable.

**UINT8 PchSataHsioTxGen3DeEmph [8]**  
Offset 0x0448 - PCH HSIO SATA 6.0 Gb/s TX Output De-Emphasis Adjustment Setting PCH HSIO SATA 6.0 Gb/s TX Output De-Emphasis Adjustment Setting.

**UINT8 PchLpcEnhancePort8xhDecoding**  
Offset 0x0450 - PCH LPC Enhance the port 8xh decoding  
Original LPC only decodes one byte of port 80h. [More...](#)

**UINT8 PchPort80Route**  
Offset 0x0451 - PCH Port80 Route Control where the Port 80h cycles are sent, 0: LPC; 1: PCI. [More...](#)

**UINT8 SmbusArpEnable**  
Offset 0x0452 - Enable SMBus ARP support  
Enable SMBus ARP support. [More...](#)

**UINT8 PchNumRsvdSmbusAddresses**  
Offset 0x0453 - Number of RsvdSmbusAddressTable.  
[More...](#)

**UINT16 PchSmbusIoBase**  
Offset 0x0454 - SMBUS Base Address  
SMBUS Base Address (IO space).

**UINT16 PcieImrSize**  
Offset 0x0456 - Size of PCIe IMR. [More...](#)

**UINT32 RsvdSmbusAddressTablePtr**  
Offset 0x0458 - Point of RsvdSmbusAddressTable Array of addresses reserved for non-ARP-capable SMBus devices.

**UINT32 PcieRpEnableMask**  
Offset 0x045C - Enable PCIE RP Mask  
Enable/disable PCIE Root Ports. [More...](#)

**UINT8 PcieImrEnabled**

Offset 0x0460 - Enable PCIe IMR 0:Disable, 1:Enable  
\$EN\_DIS.

**UINT8 [ImrRpSelection](#)**

Offset 0x0461 - Root port number for IMR. [More...](#)

**UINT8 [PchSmbAlertEnable](#)**

Offset 0x0462 - Enable SMBus Alert Pin Enable SMBus Alert Pin. [More...](#)

**UINT8 [ReservedPchPreMem \[13\]](#)**

Offset 0x0463 - ReservedPchPreMem Reserved for Pch Pre-Mem \$EN\_DIS.

**UINT8 [PcdDebugInterfaceFlags](#)**

Offset 0x0470 - Debug Interfaces Debug Interfaces. [More...](#)

**UINT8 [PcdSerialloUartNumber](#)**

Offset 0x0471 - PcdSerialloUartNumber Select Seriallo Uart Controller for debug. [More...](#)

**UINT8 [PcdIsaSerialUartBase](#)**

Offset 0x0472 - ISA Serial Base selection Select ISA Serial Base address. [More...](#)

**UINT8 [GtPIIVoltageOffset](#)**

Offset 0x0473 - GT PLL voltage offset Core PLL voltage offset. [More...](#)

**UINT8 [RingPIIVoltageOffset](#)**

Offset 0x0474 - Ring PLL voltage offset Core PLL voltage offset. [More...](#)

**UINT8 [SaPIIVoltageOffset](#)**

Offset 0x0475 - System Agent PLL voltage offset Core PLL voltage offset. [More...](#)

**UINT8 McPIIVoltageOffset**

Offset 0x0476 - Memory Controller PLL voltage offset Core PLL voltage offset. [More...](#)

**UINT8 MrcSafeConfig**

Offset 0x0477 - MRC Safe Config Enables/Disable MRC Safe Config \$EN\_DIS.

**UINT8 PcdSerialDebugBaudRate**

Offset 0x0478 - PcdSerialDebugBaudRate Baud Rate for Serial Debug Messages. [More...](#)

**UINT8 HobBufferSize**

Offset 0x0479 - HobBufferSize Size to set HOB Buffer. [More...](#)

**UINT8 ECT**

Offset 0x047A - Early Command Training Enables/Disable Early Command Training \$EN\_DIS.

**UINT8 SOT**

Offset 0x047B - SenseAmp Offset Training Enables/Disable SenseAmp Offset Training \$EN\_DIS.

**UINT8 ERDMPRTC2D**

Offset 0x047C - Early ReadMPR Timing Centering 2D Enables/Disable Early ReadMPR Timing Centering 2D \$EN\_DIS.

**UINT8 RDMPRT**

Offset 0x047D - Read MPR Training Enables/Disable Read MPR Training \$EN\_DIS.

**UINT8 RCVET**

Offset 0x047E - Receive Enable Training Enables/Disable Receive Enable Training \$EN\_DIS.

**UINT8 JWRL**

Offset 0x047F - Jedec Write Leveling Enables/Disable  
Jedec Write Leveling \$EN\_DIS.

**UINT8 EWRTC2D**

Offset 0x0480 - Early Write Time Centering 2D  
Enables/Disable Early Write Time Centering 2D \$EN\_DIS.

**UINT8 ERDTC2D**

Offset 0x0481 - Early Read Time Centering 2D  
Enables/Disable Early Read Time Centering 2D \$EN\_DIS.

**UINT8 WRTC1D**

Offset 0x0482 - Write Timing Centering 1D Enables/Disable  
Write Timing Centering 1D \$EN\_DIS.

**UINT8 WRVC1D**

Offset 0x0483 - Write Voltage Centering 1D  
Enables/Disable Write Voltage Centering 1D \$EN\_DIS.

**UINT8 RDTCT1D**

Offset 0x0484 - Read Timing Centering 1D Enables/Disable  
Read Timing Centering 1D \$EN\_DIS.

**UINT8 DIMMODTT**

Offset 0x0485 - Dimm ODT Training Enables/Disable Dimm  
ODT Training \$EN\_DIS.

**UINT8 DIMMRONT**

Offset 0x0486 - DIMM RON Training Enables/Disable DIMM  
RON Training \$EN\_DIS.

**UINT8 WRDSEQT**

Offset 0x0487 - Write Drive Strength/Equalization 2D  
Enables/Disable Write Drive Strength/Equalization 2D  
\$EN\_DIS.

**UINT8 WRSRT**

Offset 0x0488 - Write Slew Rate Training Enables/Disable Write Slew Rate Training \$EN\_DIS.

**UINT8 RDODTT**

Offset 0x0489 - Read ODT Training Enables/Disable Read ODT Training \$EN\_DIS.

**UINT8 RDEQT**

Offset 0x048A - Read Equalization Training Enables/Disable Read Equalization Training \$EN\_DIS.

**UINT8 RDADPT**

Offset 0x048B - Read Amplifier Training Enables/Disable Read Amplifier Training \$EN\_DIS.

**UINT8 WRTC2D**

Offset 0x048C - Write Timing Centering 2D Enables/Disable Write Timing Centering 2D \$EN\_DIS.

**UINT8 RDTC2D**

Offset 0x048D - Read Timing Centering 2D Enables/Disable Read Timing Centering 2D \$EN\_DIS.

**UINT8 WRVC2D**

Offset 0x048E - Write Voltage Centering 2D Enables/Disable Write Voltage Centering 2D \$EN\_DIS.

**UINT8 RDVC2D**

Offset 0x048F - Read Voltage Centering 2D Enables/Disable Read Voltage Centering 2D \$EN\_DIS.

**UINT8 CMDVC**

Offset 0x0490 - Command Voltage Centering Enables/Disable Command Voltage Centering \$EN\_DIS.

**UINT8 LCT**

Offset 0x0491 - Late Command Training Enables/Disable Late Command Training \$EN\_DIS.

**UINT8 RTL**

Offset 0x0492 - Round Trip Latency Training Enables/Disable Round Trip Latency Training \$EN\_DIS.

**UINT8 TAT**

Offset 0x0493 - Turn Around Timing Training Enables/Disable Turn Around Timing Training \$EN\_DIS.

**UINT8 MEMTST**

Offset 0x0494 - Memory Test Enables/Disable Memory Test \$EN\_DIS.

**UINT8 ALIASCHK**

Offset 0x0495 - DIMM SPD Alias Test Enables/Disable DIMM SPD Alias Test \$EN\_DIS.

**UINT8 RCVENC1D**

Offset 0x0496 - Receive Enable Centering 1D Enables/Disable Receive Enable Centering 1D \$EN\_DIS.

**UINT8 RMC**

Offset 0x0497 - Retrain Margin Check Enables/Disable Retrain Margin Check \$EN\_DIS.

**UINT8 WRDSUDT**

Offset 0x0498 - Write Drive Strength Up/Dn independently Enables/Disable Write Drive Strength Up/Dn independently \$EN\_DIS.

**UINT8 EccSupport**

Offset 0x0499 - ECC Support Enables/Disable ECC Support \$EN\_DIS.

**UINT8 RemapEnable**

Offset 0x049A - Memory Remap Enables/Disable Memory Remap \$EN\_DIS.

**UINT8 RankInterleave**

Offset 0x049B - Rank Interleave support Enables/Disable Rank Interleave support. [More...](#)

**UINT8 EnhancedInterleave**

Offset 0x049C - Enhanced Interleave support Enables/Disable Enhanced Interleave support \$EN\_DIS.

**UINT8 MemoryTrace**

Offset 0x049D - Memory Trace Enable Memory Trace of Ch 0 to Ch 1 using Stacked Mode. [More...](#)

**UINT8 ChHashEnable**

Offset 0x049E - Ch Hash Support Enable/Disable Channel Hash Support. [More...](#)

**UINT8 EnableExtts**

Offset 0x049F - Extern Therm Status Enables/Disable Extern Therm Status \$EN\_DIS.

**UINT8 EnableCltm**

Offset 0x04A0 - Closed Loop Therm Manage Enables/Disable Closed Loop Therm Manage \$EN\_DIS.

**UINT8 EnableOltm**

Offset 0x04A1 - Open Loop Therm Manage Enables/Disable Open Loop Therm Manage \$EN\_DIS.

**UINT8 EnablePwrDn**

Offset 0x04A2 - DDR PowerDown and idle counter Enables/Disable DDR PowerDown and idle counter \$EN\_DIS.

**UINT8 EnablePwrDnLpddr**

Offset 0x04A3 - DDR PowerDown and idle counter - LPDDR Enables/Disable DDR PowerDown and idle counter(For LPDDR Only) \$EN\_DIS.

**UINT8 UserPowerWeightsEn**

Offset 0x04A4 - Use user provided power weights, scale factor, and channel power floor values Enables/Disable Use user provided power weights, scale factor, and channel power floor values \$EN\_DIS.

**UINT8 RapILim2Lock**

Offset 0x04A5 - RAPL PL Lock Enables/Disable RAPL PL Lock \$EN\_DIS.

**UINT8 RapILim2Ena**

Offset 0x04A6 - RAPL PL 2 enable Enables/Disable RAPL PL 2 enable \$EN\_DIS.

**UINT8 RapILim1Ena**

Offset 0x04A7 - RAPL PL 1 enable Enables/Disable RAPL PL 1 enable \$EN\_DIS.

**UINT8 SrefCfgEna**

Offset 0x04A8 - SelfRefresh Enable Enables/Disable SelfRefresh Enable \$EN\_DIS.

**UINT8 ThrtCkeMinDefeatLpddr**

Offset 0x04A9 - Throttler CKEMin Defeature - LPDDR Enables/Disable Throttler CKEMin Defeature(For LPDDR Only) \$EN\_DIS.

**UINT8 ThrtCkeMinDefeat**

Offset 0x04AA - Throttler CKEMin Defeature Enables/Disable Throttler CKEMin Defeature \$EN\_DIS.

**UINT8 RhPrevention**

Offset 0x04AB - Enable RH Prevention Enables/Disable RH Prevention \$EN\_DIS.

**UINT8 ExitOnFailure**

Offset 0x04AC - Exit On Failure (MRC) Enables/Disable Exit On Failure (MRC) \$EN\_DIS.

**UINT8 DdrThermalSensor**

Offset 0x04AD - LPDDR Thermal Sensor Enables/Disable LPDDR Thermal Sensor \$EN\_DIS.

**UINT8 Ddr4DdpSharedClock**

Offset 0x04AE - Select if CLK0 is shared between Rank0 and Rank1 in DDR4 DDP Select if CLK0 is shared between Rank0 and Rank1 in DDR4 DDP \$EN\_DIS.

**UINT8 Ddr4DdpSharedZq**

Offset 0x04AF - Select if ZQ pin is shared between Rank0 and Rank1 in DDR4 DDP ESelect if ZQ pin is shared between Rank0 and Rank1 in DDR4 DDP \$EN\_DIS.

**UINT16 ChHashMask**

Offset 0x04B0 - Ch Hash Mask Set the BIT(s) to be included in the XOR function. [More...](#)

**UINT32 BClkFrequency**

Offset 0x04B2 - Base reference clock value Base reference clock value, in Hertz(Default is 125Hz) 100000000:100Hz, 125000000:125Hz, 167000000:167Hz, 250000000:250Hz.

**UINT8 ChHashInterleaveBit**

Offset 0x04B6 - Ch Hash Interleaved Bit Select the BIT to be used for Channel Interleaved mode. [More...](#)

**UINT8 EnergyScaleFact**

Offset 0x04B7 - Energy Scale Factor Energy Scale Factor,

Default is 4.

#### UINT16 **Idd3n**

Offset 0x04B8 - EPG DIMM Idd3N Active standby current (Idd3N) in millamps from datasheet. [More...](#)

#### UINT16 **Idd3p**

Offset 0x04BA - EPG DIMM Idd3P Active power-down current (Idd3P) in millamps from datasheet. [More...](#)

#### UINT8 **CMDSR**

Offset 0x04BC - CMD Slew Rate Training Enable/Disable CMD Slew Rate Training \$EN\_DIS.

#### UINT8 **CMDDSEQ**

Offset 0x04BD - CMD Drive Strength and Tx Equalization Enable/Disable CMD Drive Strength and Tx Equalization \$EN\_DIS.

#### UINT8 **CMDNORM**

Offset 0x04BE - CMD Normalization Enable/Disable CMD Normalization \$EN\_DIS.

#### UINT8 **EWRDSEQ**

Offset 0x04BF - Early DQ Write Drive Strength and Equalization Training Enable/Disable Early DQ Write Drive Strength and Equalization Training \$EN\_DIS.

#### UINT8 **RhActProbability**

Offset 0x04C0 - RH Activation Probability RH Activation Probability, Probability value is  $1/2^{(\text{inputvalue})}$

#### UINT8 **RaplLim2WindX**

Offset 0x04C1 - RAPL PL 2 WindowX Power PL 2 time window X value,  $(1/1024)*(1+(x/4))*(2^y)$  (1=Def)

**UINT8 RapILim2WindY**  
Offset 0x04C2 - RAPL PL 2 WindowY Power PL 2 time  
window Y value,  $(1/1024)*(1+(x/4))*(2^y)$  (1=Def)

**UINT8 RapILim1WindX**  
Offset 0x04C3 - RAPL PL 1 WindowX Power PL 1 time  
window X value,  $(1/1024)*(1+(x/4))*(2^y)$  (0=Def)

**UINT8 RapILim1WindY**  
Offset 0x04C4 - RAPL PL 1 WindowY Power PL 1 time  
window Y value,  $(1/1024)*(1+(x/4))*(2^y)$  (0=Def)

**UINT16 RapILim2Pwr**  
Offset 0x04C5 - RAPL PL 2 Power range[0;2^14-1]=[  
2047.875;0]in W, (222= Def)

**UINT16 RapILim1Pwr**  
Offset 0x04C7 - RAPL PL 1 Power range[0;2^14-1]=[  
2047.875;0]in W, (0= Def)

**UINT8 WarmThresholdCh0Dimm0**  
Offset 0x04C9 - Warm Threshold Ch0 Dimm0  
range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for  
CLTM. [More...](#)

**UINT8 WarmThresholdCh0Dimm1**  
Offset 0x04CA - Warm Threshold Ch0 Dimm1  
range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for  
CLTM. [More...](#)

**UINT8 WarmThresholdCh1Dimm0**  
Offset 0x04CB - Warm Threshold Ch1 Dimm0  
range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for  
CLTM. [More...](#)

**UINT8 WarmThresholdCh1Dimm1**  
Offset 0x04CC - Warm Threshold Ch1 Dimm1

range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM. [More...](#)

**UINT8 [HotThresholdCh0Dimm0](#)**

Offset 0x04CD - Hot Threshold Ch0 Dimm0 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM. [More...](#)

**UINT8 [HotThresholdCh0Dimm1](#)**

Offset 0x04CE - Hot Threshold Ch0 Dimm1 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM. [More...](#)

**UINT8 [HotThresholdCh1Dimm0](#)**

Offset 0x04CF - Hot Threshold Ch1 Dimm0 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM. [More...](#)

**UINT8 [HotThresholdCh1Dimm1](#)**

Offset 0x04D0 - Hot Threshold Ch1 Dimm1 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM. [More...](#)

**UINT8 [WarmBudgetCh0Dimm0](#)**

Offset 0x04D1 - Warm Budget Ch0 Dimm0 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

**UINT8 [WarmBudgetCh0Dimm1](#)**

Offset 0x04D2 - Warm Budget Ch0 Dimm1 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

**UINT8 [WarmBudgetCh1Dimm0](#)**

Offset 0x04D3 - Warm Budget Ch1 Dimm0 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

**UINT8 [WarmBudgetCh1Dimm1](#)**

Offset 0x04D4 - Warm Budget Ch1 Dimm1 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

**UINT8 [HotBudgetCh0Dimm0](#)**

Offset 0x04D5 - Hot Budget Ch0 Dimm0 range[255;0]=

[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

#### UINT8 **HotBudgetCh0Dimm1**

Offset 0x04D6 - Hot Budget Ch0 Dimm1 range[255;0]=  
[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

#### UINT8 **HotBudgetCh1Dimm0**

Offset 0x04D7 - Hot Budget Ch1 Dimm0 range[255;0]=  
[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

#### UINT8 **HotBudgetCh1Dimm1**

Offset 0x04D8 - Hot Budget Ch1 Dimm1 range[255;0]=  
[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

#### UINT8 **IdleEnergyCh0Dimm0**

Offset 0x04D9 - Idle Energy Ch0Dimm0 Idle Energy  
Consumed for 1 clk w/dimm idle/cke on, range[63;0],(10=Def)

#### UINT8 **IdleEnergyCh0Dimm1**

Offset 0x04DA - Idle Energy Ch0Dimm1 Idle Energy  
Consumed for 1 clk w/dimm idle/cke on, range[63;0],(10=Def)

#### UINT8 **IdleEnergyCh1Dimm0**

Offset 0x04DB - Idle Energy Ch1Dimm0 Idle Energy  
Consumed for 1 clk w/dimm idle/cke on, range[63;0],(10=Def)

#### UINT8 **IdleEnergyCh1Dimm1**

Offset 0x04DC - Idle Energy Ch1Dimm1 Idle Energy  
Consumed for 1 clk w/dimm idle/cke on, range[63;0],(10=Def)

#### UINT8 **PdEnergyCh0Dimm0**

Offset 0x04DD - PowerDown Energy Ch0Dimm0

PowerDown Energy Consumed w/dimm idle/cke off,  
range[63;0],(5= Def)

UINT8 **PdEnergyCh0Dimm1**

Offset 0x04DE - PowerDown Energy Ch0Dimm1  
PowerDown Energy Consumed w/dimm idle/cke off,  
range[63;0],(5= Def)

UINT8 **PdEnergyCh1Dimm0**

Offset 0x04DF - PowerDown Energy Ch1Dimm0  
PowerDown Energy Consumed w/dimm idle/cke off,  
range[63;0],(5= Def)

UINT8 **PdEnergyCh1Dimm1**

Offset 0x04E0 - PowerDown Energy Ch1Dimm1  
PowerDown Energy Consumed w/dimm idle/cke off,  
range[63;0],(5= Def)

UINT8 **ActEnergyCh0Dimm0**

Offset 0x04E1 - Activate Energy Ch0Dimm0 Activate  
Energy Contribution, range[255;0],(172= Def)

UINT8 **ActEnergyCh0Dimm1**

Offset 0x04E2 - Activate Energy Ch0Dimm1 Activate  
Energy Contribution, range[255;0],(172= Def)

UINT8 **ActEnergyCh1Dimm0**

Offset 0x04E3 - Activate Energy Ch1Dimm0 Activate  
Energy Contribution, range[255;0],(172= Def)

UINT8 **ActEnergyCh1Dimm1**

Offset 0x04E4 - Activate Energy Ch1Dimm1 Activate  
Energy Contribution, range[255;0],(172= Def)

UINT8 **RdEnergyCh0Dimm0**

Offset 0x04E5 - Read Energy Ch0Dimm0 Read Energy  
Contribution, range[255;0],(212= Def)

**UINT8 RdEnergyCh0Dimm1**

Offset 0x04E6 - Read Energy Ch0Dimm1 Read Energy Contribution, range[255;0],(212= Def)

**UINT8 RdEnergyCh1Dimm0**

Offset 0x04E7 - Read Energy Ch1Dimm0 Read Energy Contribution, range[255;0],(212= Def)

**UINT8 RdEnergyCh1Dimm1**

Offset 0x04E8 - Read Energy Ch1Dimm1 Read Energy Contribution, range[255;0],(212= Def)

**UINT8 WrEnergyCh0Dimm0**

Offset 0x04E9 - Write Energy Ch0Dimm0 Write Energy Contribution, range[255;0],(221= Def)

**UINT8 WrEnergyCh0Dimm1**

Offset 0x04EA - Write Energy Ch0Dimm1 Write Energy Contribution, range[255;0],(221= Def)

**UINT8 WrEnergyCh1Dimm0**

Offset 0x04EB - Write Energy Ch1Dimm0 Write Energy Contribution, range[255;0],(221= Def)

**UINT8 WrEnergyCh1Dimm1**

Offset 0x04EC - Write Energy Ch1Dimm1 Write Energy Contribution, range[255;0],(221= Def)

**UINT8 ThrtCkeMinTmr**

Offset 0x04ED - Throttler CKEMin Timer Timer value for CKEMin, range[255;0]. [More...](#)

**UINT8 CkeRankMapping**

Offset 0x04EE - Cke Rank Mapping Bits [7:4] - Channel 1, bits [3:0] - Channel 0. [More...](#)

UINT8	<b>RaplPwrFICh0</b> Offset 0x04EF - Rapl Power Floor Ch0 Power budget ,range[255;0],(0= 5.3W Def)
UINT8	<b>RaplPwrFICh1</b> Offset 0x04F0 - Rapl Power Floor Ch1 Power budget ,range[255;0],(0= 5.3W Def)
UINT8	<b>EnCmdRate</b> Offset 0x04F1 - Command Rate Support CMD Rate and Limit Support Option. <a href="#">More...</a>
UINT8	<b>Refresh2X</b> Offset 0x04F2 - REFRESH_2X_MODE 0- (Default)Disabled 1-iMC enables 2xRef when Warm and Hot 2- iMC enables 2xRef when Hot 0:Disable, 1:Enabled for WARM or HOT, 2:Enabled HOT only.
UINT8	<b>EpgEnable</b> Offset 0x04F3 - Energy Performance Gain Enable/disable(default) Energy Performance Gain. <a href="#">More...</a>
UINT8	<b>RhSolution</b> Offset 0x04F4 - Row Hammer Solution Type of method used to prevent Row Hammer. <a href="#">More...</a>
UINT8	<b>UserThresholdEnable</b> Offset 0x04F5 - User Manual Threshold Disabled: Predefined threshold will be used. <a href="#">More...</a>
UINT8	<b>UserBudgetEnable</b> Offset 0x04F6 - User Manual Budget Disabled: Configuration of memories will defined the Budget value. <a href="#">More...</a>
UINT8	<b>TsodTcritMax</b> Offset 0x04F7 - TcritMax Maximum Critical Temperature in

Centigrade of the On-DIMM Thermal Sensor. [More...](#)

UINT8 **TsodEventMode**

Offset 0x04F8 - Event mode Disable:Comparator mode.

[More...](#)

UINT8 **TsodEventPolarity**

Offset 0x04F9 - EVENT polarity Disable:Active LOW.

[More...](#)

UINT8 **TsodCriticalEventOnly**

Offset 0x04FA - Critical event only Disable:Trips on alarm or critical. [More...](#)

UINT8 **TsodEventOutputControl**

Offset 0x04FB - Event output control Disable:Event output disable. [More...](#)

UINT8 **TsodAlarmwindowLockBit**

Offset 0x04FC - Alarm window lock bit Disable:Alarm trips are not locked and can be changed. [More...](#)

UINT8 **TsodCriticaltripLockBit**

Offset 0x04FD - Critical trip lock bit Disable:Critical trip is not locked and can be changed. [More...](#)

UINT8 **TsodShutdownMode**

Offset 0x04FE - Shutdown mode Disable:Temperature sensor enable. [More...](#)

UINT8 **TsodThigMax**

Offset 0x04FF - ThighMax Thigh = ThighMax (Default is 93)

UINT8 **TsodManualEnable**

Offset 0x0500 - User Manual Thig and Tcrit

Disabled(Default): Temperature will be given by the configuration of memories and 1x or 2xrefresh rate. [More...](#)

**UINT8 ForceOltmOrRefresh2x**

Offset 0x0501 - Force OLTM or 2X Refresh when needed  
Disabled(Default) = Force OLTM. [More...](#)

**UINT8 PwdwnIdleCounter**

Offset 0x0502 - Pwr Down Idle Timer The minimum value should = to the worst case Roundtrip delay + Burst\_Length.  
[More...](#)

**UINT8 CmdRanksTerminated**

Offset 0x0503 - Bitmask of ranks that have CA bus terminated  
Offset 225 LPDDR4: Bitmask of ranks that have CA bus terminated. [More...](#)

**UINT8 GdxcEnable**

Offset 0x0504 - GDXC MOT enable GDXC MOT enable.  
[More...](#)

**UINT8 PcdSerialDebugLevel**

Offset 0x0505 - PcdSerialDebugLevel Serial Debug Message Level. [More...](#)

**UINT8 FivrFaults**

Offset 0x0506 - Fivr Faults Fivr Faults; 0: Disabled; **1: Enabled.** [More...](#)

**UINT8 FivrEfficiency**

Offset 0x0507 - Fivr Efficiency Fivr Efficiency Management; 0: Disabled; **1: Enabled.** [More...](#)

**UINT8 SafeMode**

Offset 0x0508 - Safe Mode Support This option configures the varous items in the IO and MC to be more conservative.  
[More...](#)

**UINT8 CleanMemory**

Offset 0x0509 - Ask MRC to clear memory content Ask MRC to clear memory content 0: Do not Clear Memory; 1: Clear Memory. [More...](#)

**UINT8 [LpDdrDqDqsReTraining](#)**

Offset 0x050A - LpDdrDqDqsReTraining Enables/Disable LpDdrDqDqsReTraining \$EN\_DIS.

**UINT16 [PostCodeOutputPort](#)**

Offset 0x050B - Post Code Output Port This option configures Post Code Output Port.

**UINT8 [RMTLoopCount](#)**

Offset 0x050D - RMTLoopCount Specifies the Loop Count to be used during Rank Margin Tool Testing. [More...](#)

**UINT8 [EnBER](#)**

Offset 0x050E - BER Support Enable/Disable the Rank Margin Tool interpolation/extrapolation. [More...](#)

**UINT8 [DualDimmPerChannelBoardType](#)**

Offset 0x050F - Dual Dimm Per-Channel Board Type Option to indicate if Board Layout includes One/Two DIMMs per channel. [More...](#)

**UINT8 [Ddr4MixedUDimm2DpcLimit](#)**

Offset 0x0510 - DDR4 Mixed U-DIMM 2DPC Limitation Enable/Disable 2667 Frequency Limitation for DDR4 U-DIMM Mixed Dimm 2DPC population. [More...](#)

**UINT8 [ReservedFspmUpdCfl \[2\]](#)**

Offset 0x0511 - CFL Reserved Reserved FspmConfig CFL \$EN\_DIS.

**UINT8 [MemTestOnWarmBoot](#)**

Offset 0x0513 - Memory Test on Warm Boot Run Base Memory Test on Warm Boot 0:Disable, 1:Enable.

**UINT8 ThrtCkeMinTmrLpddr**

Offset 0x0514 - Throttler CKEMin Timer - LPDDR Timer  
value for CKEMin (For LPDDR Only), range[255;0]. [More...](#)

**UINT8 ReservedFspmUpd [10]**

Offset 0x0515.

---

## Detailed Description

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Fsp M Configuration.

Definition at line **56** of file [FspmUpd.h](#).

## Member Data Documentation

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### **UINT8 FSP\_M\_CONFIG::ActiveCoreCount**

---

Offset 0x020C - Number of active cores Number of active cores(Depends on Number of cores).

0: All; 1: 1 ; 2: 2 ; 3: 3 0:All, 1:1, 2:2, 3:3

Definition at line [1007](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::ApertureSize**

---

Offset 0x00BA - Aperture Size Select the Aperture Size.

0:128 MB, 1:256 MB, 2:512 MB

Definition at line [267](#) of file [FspmUpd.h](#).

### **UINT32 FSP\_M\_CONFIG::ApStartupBase**

---

Offset 0x0248 - ApStartupBase Enable/Disable.

0: Disable, define default value of BiosAcmBase , 1: enable

Definition at line [1170](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::Avx2RatioOffset**

---

Offset 0x0210 - AVX2 Ratio Offset 0(Default)= No Offset.

Range 0 - 31. Specifies number of bins to decrease AVX ratio vs.

Core Ratio. Uses Mailbox MSR 0x150, cmd 0x1B.

Definition at line [1033](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::Avx3RatioOffset**

---

Offset 0x0211 - AVX3 Ratio Offset 0(Default)= No Offset.

Range 0 - 31. Specifies number of bins to decrease AVX ratio vs. Core Ratio. Uses Mailbox MSR 0x150, cmd 0x1B.

Definition at line [1039](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::BclkAdaptiveVoltage**

---

Offset 0x0212 - BCLK Adaptive Voltage Enable When enabled, the CPU V/F curves are aware of BCLK frequency when calculated.

0: Disable; **1: Enable \$EN\_DIS**

Definition at line [1046](#) of file [FspmUpd.h](#).

### **UINT32 FSP\_M\_CONFIG::BiosAcmBase**

---

Offset 0x0240 - BiosAcmBase Enable/Disable.

0: Disable, define default value of BiosAcmBase , 1: enable

Definition at line [1160](#) of file [FspmUpd.h](#).

### **UINT32 FSP\_M\_CONFIG::BiosAcmSize**

---

Offset 0x0244 - BiosAcmSize Enable/Disable.

0: Disable, define default value of BiosAcmSize , 1: enable

Definition at line [1165](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::BiosGuard**

---

Offset 0x0223 - BiosGuard Enable/Disable.

0: Disable, Enable/Disable BIOS Guard feature, 1: enable \$EN\_DIS

Definition at line [1110](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::BistOnReset**

---

Offset 0x0200 - BIST on Reset Enable or Disable BIST on Reset; 0: **Disable**; 1: Enable.

\$EN\_DIS

Definition at line [931](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::BootFrequency**

---

Offset 0x020B - Boot frequency Sets the boot frequency starting from reset vector.

- 0: Maximum battery performance.- **1: Maximum non-turbo performance.**- 2: Turbo performance.

### **Note**

If Turbo is selected BIOS will start in max non-turbo mode and switch to Turbo mode. 0:0, 1:1, 2:2

Definition at line [1000](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::ChHashEnable**

---

Offset 0x049E - Ch Hash Support Enable/Disable Channel Hash

Support.

NOTE: ONLY if Memory interleaved Mode \$EN\_DIS

Definition at line [1704](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::ChHashInterleaveBit**

---

Offset 0x04B6 - Ch Hash Interleaved Bit Select the BIT to be used for Channel Interleaved mode.

NOTE: BIT7 will interlace the channels at a 2 cacheline granularity, BIT8 at 4 and BIT9 at 8. Default is BIT8 0:BIT6, 1:BIT7, 2:BIT8, 3:BIT9, 4:BIT10, 5:BIT11, 6:BIT12, 7:BIT13

Definition at line [1826](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_CONFIG::ChHashMask**

---

Offset 0x04B0 - Ch Hash Mask Set the BIT(s) to be included in the XOR function.

NOTE BIT mask corresponds to BITS [19:6]

Definition at line [1813](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::CkeRankMapping**

---

Offset 0x04EE - Cke Rank Mapping Bits [7:4] - Channel 1, bits [3:0] - Channel 0.

**0xAA=Default** Bit [i] specifies which rank CKE[i] goes to.

Definition at line [2094](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::CleanMemory**

---

Offset 0x0509 - Ask MRC to clear memory content Ask MRC to clear memory content **0: Do not Clear Memory; 1: Clear Memory.**

\$EN\_DIS

Definition at line [2269](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::CmdRanksTerminated**

---

Offset 0x0503 - Bitmask of ranks that have CA bus terminated Offset 225 LPDDR4: Bitmask of ranks that have CA bus terminated.

**0x01=Default, Rank0 is terminating and Rank1 is non-terminating**

Definition at line [2230](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::CoreMaxOcRatio**

---

Offset 0x0205 - Maximum Core Turbo Ratio Override Maximum core turbo ratio override allows to increase CPU core frequency beyond the fused max turbo ratio limit.

**0: Hardware defaults.** Range: 0-255

Definition at line [963](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::CorePIIVoltageOffset**

---

Offset 0x0213 - Core PLL voltage offset Core PLL voltage offset.

**0: No offset.** Range 0-63

Definition at line [1051](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_CONFIG::CoreVoltageAdaptive**

---

Offset 0x0216 - Core Turbo voltage Adaptive Extra Turbo voltage applied to the cpu core when the cpu is operating in turbo mode.

Valid Range 0 to 2000

Definition at line [1063](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::CoreVoltageMode**

---

Offset 0x0206 - Core voltage mode Core voltage mode; **0: Adaptive**; 1: Override.

\$EN\_DIS

Definition at line [969](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_CONFIG::CoreVoltageOverride**

---

Offset 0x0214 - core voltage override The core voltage override which is applied to the entire range of cpu core frequencies.

Valid Range 0 to 2000

Definition at line [1057](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::CpuRatio**

---

Offset 0x020A - CPU ratio value CPU ratio value.

Valid Range 0 to 63. CPU Ratio is 0 when disabled.

Definition at line [992](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::CpuTraceHubMemReg0Size**

---

Offset 0x00F4 - CPU Trace Hub Memory Region 0 CPU Trace Hub Memory Region 0, The available memory size is : 0MB, 1MB, 8MB, 64MB, 128MB, 256MB, 512MB.

Note : Limitation of total buffer size (CPU + PCH) is 512MB. 0:0, 1:1MB, 2:8MB, 3:64MB, 4:128MB, 5:256MB, 6:512MB

Definition at line [479](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::CpuTraceHubMemReg1Size**

---

Offset 0x00F5 - CPU Trace Hub Memory Region 1 CPU Trace Hub Memory Region 1.

The available memory size is : 0MB, 1MB, 8MB, 64MB, 128MB, 256MB, 512MB. Note : Limitation of total buffer size (CPU + PCH) is 512MB. 0:0, 1:1MB, 2:8MB, 3:64MB, 4:128MB, 5:256MB, 6:512MB

Definition at line [486](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::CpuTraceHubMode**

---

Offset 0x00F3 - CPU Trace Hub Mode Select 'Target Debugger' if Trace Hub is used by target debugger software or 'Disable' trace hub functionality.

0: Disable, 1:Target Debugger Mode

Definition at line [472](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::DciUsb3TypecUfpDbg**

---

Offset 0x00AB - USB3 Type-C UFP2DFP Kernel/Platform Debug

Support This BIOS option enables kernel and platform debug for USB3 interface over a UFP Type-C receptacle, select 'No Change' will do nothing to UFP2DFP setting.

0:Disabled, 1:Enabled, 2:No Change

Definition at line [222](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::Ddr4MixedUDimm2DpcLimit**

---

Offset 0x0510 - DDR4 Mixed U-DIMM 2DPC Limitation  
Enable/Disable 2667 Frequency Limitation for DDR4 U-DIMM Mixed  
Dimm 2DPC population.

Disable(Default)=0, Enable=1 \$EN\_DIS

Definition at line [2305](#) of file [FspmUpd.h](#).

### **UINT16 FSP\_M\_CONFIG::DdrFreqLimit**

---

Offset 0x00BE - DDR Frequency Limit Maximum Memory Frequency  
Selections in Mhz.

Valid values should match the refclk, i.e. divide by 133 or 100  
1067:1067, 1333:1333, 1400:1400, 1600:1600, 1800:1800,  
1867:1867, 2000:2000, 2133:2133, 2200:2200, 2400:2400,  
2600:2600, 2667:2667, 2800:2800, 2933:2933, 3000:3000,  
3200:3200, 0:Auto

Definition at line [294](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::DisableDimmChannel0**

---

Offset 0x00C5 - Channel A DIMM Control Channel A DIMM Control  
Support - Enable or Disable Dimms on Channel A.

0:Enable both DIMMs, 1:Disable DIMM0, 2:Disable DIMM1,  
3:Disable both DIMMs

Definition at line [320](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::DisableDimmChannel1**

---

Offset 0x00C6 - Channel B DIMM Control Channel B DIMM Control  
Support - Enable or Disable Dimms on Channel B.

0:Enable both DIMMs, 1:Disable DIMM0, 2:Disable DIMM1,  
3:Disable both DIMMs

Definition at line [326](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::DisableMtrrProgram**

---

Offset 0x0207 - Program Cache Attributes Program Cache  
Attributes; **0: Program**; 1: Disable Program.

\$EN\_DIS

Definition at line [975](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::DmiDeEmphasis**

---

Offset 0x0176 - DeEmphasis control for DMI DeEmphasis control for  
DMI.

0=-6dB, 1(Default)=-3.5 dB 0: -6dB, 1: -3.5dB

Definition at line [765](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::DmiGen3EndPointHint[8]**

---

Offset 0x0138 - DMI Gen3 End port Hint values per lane Used for programming DMI Gen3 Hint values per lane.

Range: 0-6, 2 is default for each lane

Definition at line [712](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::DmiGen3EndPointPreset[8]**

---

Offset 0x0130 - DMI Gen3 End port preset values per lane Used for programming DMI Gen3 preset values per lane.

Range: 0-9, 7 is default for each lane

Definition at line [707](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::DmiGen3ProgramStaticEq**

---

Offset 0x0112 - Enable/Disable DMI GEN3 Static EQ Phase1 programming Program DMI Gen3 EQ Phase1 Static Presets.

Disabled(0x0): Disable EQ Phase1 Static Presets Programming,  
Enabled(0x1)(Default): Enable EQ Phase1 Static Presets  
Programming \$EN\_DIS

Definition at line [566](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::DmiGen3RootPortPreset[8]**

---

Offset 0x0128 - DMI Gen3 Root port preset values per lane Used for programming DMI Gen3 preset values per lane.

Range: 0-9, 8 is default for each lane

Definition at line [702](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::DualDimmPerChannelBoardType**

---

Offset 0x050F - Dual Dimm Per-Channel Board Type Option to indicate if Board Layout includes One/Two DIMMs per channel.

This is used to limit maximum frequency for some SKUs. 0:1DPC, 1:2DPC

Definition at line [2298](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::EnableC6Dram**

---

Offset 0x0202 - C6DRAM power gating feature This policy indicates whether or not BIOS should allocate PRMRR memory for C6DRAM power gating feature.

- 0: Don't allocate any PRMRR memory for C6DRAM power gating feature.- **1: Allocate PRMRR memory for C6DRAM power gating feature.** \$EN\_DIS

Definition at line [945](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::EnableSgx**

---

Offset 0x0225 - EnableSgx Enable/Disable.

0: Disable, Enable/Disable SGX feature, 1: enable, 2: Software Control  
0: Disable, 1: Enable, 2: Software Control

Definition at line [1120](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::EnBER**

---

Offset 0x050E - BER Support Enable/Disable the Rank Margin Tool

interpolation/extrapolation.

0:Disable, 1:Enable

Definition at line [2291](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::EnCmdRate**

---

Offset 0x04F1 - Command Rate Support CMD Rate and Limit Support Option.

NOTE: ONLY supported in 1N Mode, Default is 3 CMDS  
0:Disable, 1:1 CMD, 2:2 CMDS, 3:3 CMDS, 4:4 CMDS, 5:5 CMDS, 6:6 CMDS, 7:7 CMDS

Definition at line [2110](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::EpgEnable**

---

Offset 0x04F3 - Energy Performance Gain Enable/disable(default) Energy Performance Gain.

\$EN\_DIS

Definition at line [2122](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::FClkFrequency**

---

Offset 0x020D - Processor Early Power On Configuration FCLK setting **0: 800 MHz (ULT/ULX)**.

**1: 1 GHz (DT/Halo)**. Not supported on ULT/ULX. - 2: 400 MHz. - 3: Reserved  
0:800 MHz, 1: 1 GHz, 2: 400 MHz, 3: Reserved

Definition at line [1014](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::FivrEfficiency**

---

Offset 0x0507 - Fivr Efficiency Fivr Efficiency Management; 0: Disabled; **1: Enabled.**

\$EN\_DIS

Definition at line [2257](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::FivrFaults**

---

Offset 0x0506 - Fivr Faults Fivr Faults; 0: Disabled; **1: Enabled.**

\$EN\_DIS

Definition at line [2251](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::ForceOltmOrRefresh2x**

---

Offset 0x0501 - Force OLTM or 2X Refresh when needed  
Disabled(Default): = Force OLTM.

Enabled: = Force 2x Refresh. \$EN\_DIS

Definition at line [2218](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_CONFIG::FreqSaGvLow**

---

Offset 0x00C0 - Low Frequency SAGV Low Frequency Selections in Mhz.

Options are 1067, 1333, 1600, 1867, 2133, 2400, 2667, 2933 and 0 for Auto. 1067:1067, 1333:1333, 1600:1600, 1867:1867, 2133:2133, 2400:2400, 2667:2667, 2933:2933, 0:Auto

Definition at line [301](#) of file [FspmUpd.h](#).

### **UINT16 FSP\_M\_CONFIG::FreqSaGvMid**

---

Offset 0x00C2 - Mid Frequency SAGV Mid Frequency Selections in Mhz.

Options are 1067, 1333, 1600, 1867, 2133, 2400, 2667, 2933 and 0 for Auto. 1067:1067, 1333:1333, 1600:1600, 1867:1867, 2133:2133, 2400:2400, 2667:2667, 2933:2933, 0:Auto

Definition at line [308](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::GdxcEnable**

---

Offset 0x0504 - GDXC MOT enable GDXC MOT enable.

\$EN\_DIS

Definition at line [2236](#) of file [FspmUpd.h](#).

### **UINT32 FSP\_M\_CONFIG::GmAdr**

---

Offset 0x017A - Temporary MMIO address for GMADR The reference code will use this as Temporary MMIO address space to access GMADR Registers. Platform should provide conflict free Temporary MMIO Range: GmAdr to (GmAdr + ApertureSize).

Default is (PciExpressBaseAddress - ApertureSize) to (PciExpressBaseAddress

- 0x1) (Where ApertureSize = 256MB)

Definition at line [785](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::GtPllVoltageOffset**

---

Offset 0x0473 - GT PLL voltage offset Core PLL voltage offset.

**0: No offset.** Range 0-63

Definition at line [1446](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::GtPsmiSupport**

---

Offset 0x01F3 - Selection of PSMI Support On/Off 0(Default) = FALSE, 1 = TRUE.

When TRUE, it will allow the PSMI Support \$EN\_DIS

Definition at line [893](#) of file [FspmUpd.h](#).

## **UINT32 FSP\_M\_CONFIG::GttMmAdr**

---

Offset 0x017E - Temporary MMIO address for GTTMMADR The reference code will use this as Temporary MMIO address space to access GTTMMADR Registers. Platform should provide conflict free Temporary MMIO Range: GttMmAdr to (GttMmAdr + 2MB MMIO + 6MB Reserved + GttSize).

Default is (GmAdr - (2MB MMIO

- 6MB Reserved + GttSize)) to (GmAdr - 0x1) (Where GttSize = 8MB)

Definition at line [793](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::HobBufferSize**

---

Offset 0x0479 - HobBufferSize Size to set HOB Buffer.

0:Default, 1: 1 Byte, 2: 1 KB, 3: Max value(assuming 63KB total HOB size). 0:Default, 1: 1 Byte, 2: 1 KB, 3: Max value

Definition at line [1480](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::HotThresholdCh0Dimm0**

---

Offset 0x04CD - Hot Threshold Ch0 Dimm0 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

Default is 255

Definition at line [1927](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::HotThresholdCh0Dimm1**

---

Offset 0x04CE - Hot Threshold Ch0 Dimm1 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

Default is 255

Definition at line [1932](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::HotThresholdCh1Dimm0**

---

Offset 0x04CF - Hot Threshold Ch1 Dimm0 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

Default is 255

Definition at line [1937](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::HotThresholdCh1Dimm1**

---

Offset 0x04D0 - Hot Threshold Ch1 Dimm1 range[255;0]=[31.875;0]

in W for OLTM, [127.5;0] in C for CLTM.

Default is 255

Definition at line [1942](#) of file [FspmUpd.h](#).

### **UINT16 FSP\_M\_CONFIG::Idd3n**

---

Offset 0x04B8 - EPG DIMM Idd3N Active standby current (Idd3N) in millamps from datasheet.

Must be calculated on a per DIMM basis. Default is 26

Definition at line [1837](#) of file [FspmUpd.h](#).

### **UINT16 FSP\_M\_CONFIG::Idd3p**

---

Offset 0x04BA - EPG DIMM Idd3P Active power-down current (Idd3P) in millamps from datasheet.

Must be calculated on a per DIMM basis. Default is 11

Definition at line [1843](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::IgdDvmt50PreAlloc**

---

Offset 0x00B8 - Internal Graphics Pre-allocated Memory Size of memory preallocated for internal graphics.

0x00:0 MB, 0x01:32 MB, 0x02:64 MB

Definition at line [255](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::ImrRpSelection**

---

Offset 0x0461 - Root port number for IMR.

Root port number for IMR.

Definition at line [1411](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::InitPcieAspmAfterOeprom**

---

Offset 0x0123 - PCIe ASPM programming will happen in relation to the Oeprom Select when PCIe ASPM programming will happen in relation to the Oeprom.

Before(0x0)(Default): Do PCIe ASPM programming before Oeprom,  
After(0x1): Do PCIe ASPM programming after Oeprom, requires an SMI handler to save/restore ASPM settings during S3 resume  
0:Before, 1:After

Definition at line [686](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::InternalGfx**

---

Offset 0x00B9 - Internal Graphics Enable/disable internal graphics.

\$EN\_DIS

Definition at line [261](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::IsvtIoPort**

---

Offset 0x00F2 - ISVT IO Port Address ISVT IO Port Address.

0=Minimal, 0xFF=Maximum, 0x99=Default

Definition at line [465](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::JtagC10PowerGateDisable**

---

Offset 0x020E - Set JTAG power in C10 and deeper power states  
False: JTAG is power gated in C10 state.

True: keeps the JTAG power up during C10 and deeper power states for debug purpose. **0: False**; 1: True. 0: False, 1: True

Definition at line [1021](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::McPIIVoltageOffset**

---

Offset 0x0476 - Memory Controller PLL voltage offset Core PLL voltage offset.

**0: No offset.** Range 0-63

Definition at line [1461](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::MemoryTrace**

---

Offset 0x049D - Memory Trace Enable Memory Trace of Ch 0 to Ch 1 using Stacked Mode.

Both channels must be of equal size. This option may change TOLUD and REMAP values as needed. \$EN\_DIS

Definition at line [1698](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_CONFIG::MmioSize**

---

Offset 0x00A0 - MMIO Size Size of MMIO space reserved for devices.

0(Default)=Auto, non-Zero=size in MB

Definition at line [176](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::OcLock**

---

Offset 0x0204 - Over clocking Lock Over clocking Lock  
Enable/Disable; 0: **Disable**; 1: Enable.

\$EN\_DIS

Definition at line [957](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::PcdDebugInterfaceFlags**

---

Offset 0x0470 - Debug Interfaces Debug Interfaces.

BIT0-RAM, BIT1-UART, BIT3-USB3, BIT4-Serial IO, BIT5-TraceHub,  
BIT2 - Not used.

Definition at line [1429](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::PcdIsaSerialUartBase**

---

Offset 0x0472 - ISA Serial Base selection Select ISA Serial Base  
address.

Default is 0x3F8. 0:0x3F8, 1:0x2F8

Definition at line [1441](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::PcdSerialDebugBaudRate**

---

Offset 0x0478 - PcdSerialDebugBaudRate Baud Rate for Serial  
Debug Messages.

3:9600, 4:19200, 6:56700, 7:115200. 3:9600, 4:19200, 6:56700,

7:115200

Definition at line [1473](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::PcdSerialDebugLevel**

---

Offset 0x0505 - PcdSerialDebugLevel Serial Debug Message Level.

0:Disable, 1:Error Only, 2:Error & Warnings, 3:Load, Error, Warnings & Info, 4:Load, Error, Warnings, Info & Event, 5:Load, Error, Warnings, Info & Verbose. 0:Disable, 1:Error Only, 2:Error and Warnings, 3:Load Error Warnings and Info, 4:Load Error Warnings and Info, 5:Load Error Warnings Info and Verbose

Definition at line [2245](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::PcdSerialloUartNumber**

---

Offset 0x0471 - PcdSerialloUartNumber Select Seriallo Uart Controller for debug.

0:SerialloUart0, 1:SerialloUart1, 2:SerialloUart2

Definition at line [1435](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::PchLpcEnhancePort8xhDecoding**

---

Offset 0x0450 - PCH LPC Enhance the port 8xh decoding Original LPC only decodes one byte of port 80h.

\$EN\_DIS

Definition at line [1362](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::PchNumRsvdSmbusAddresses**

---

Offset 0x0453 - Number of RsvdSmbusAddressTable.

The number of elements in the RsvdSmbusAddressTable.

Definition at line [1379](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::PchPort80Route**

---

Offset 0x0451 - PCH Port80 Route Control where the Port 80h cycles are sent, 0: LPC; 1: PCI.

\$EN\_DIS

Definition at line [1368](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::PchSmbAlertEnable**

---

Offset 0x0462 - Enable SMBus Alert Pin Enable SMBus Alert Pin.

\$EN\_DIS

Definition at line [1417](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::PchTraceHubMemReg0Size**

---

Offset 0x00AD - PCH Trace Hub Memory Region 0 buffer Size  
Specify size of Pch trace memory region 0 buffer, the size can be 0, 1MB, 8MB, 64MB, 128MB, 256MB, 512MB.

Note : Limitation of total buffer size (PCH + CPU) is 512MB. 0:0, 1:1MB, 2:8MB, 3:64MB, 4:128MB, 5:256MB, 6:512MB

Definition at line [236](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::PchTraceHubMemReg1Size**

---

Offset 0x00AE - PCH Trace Hub Memory Region 1 buffer Size  
Specify size of Pch trace memory region 1 buffer, the size can be 0, 1MB, 8MB, 64MB, 128MB, 256MB, 512MB.

Note : Limitation of total buffer size (PCH + CPU) is 512MB. 0:0, 1:1MB, 2:8MB, 3:64MB, 4:128MB, 5:256MB, 6:512MB

Definition at line [243](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::PchTraceHubMode**

---

Offset 0x00AC - PCH Trace Hub Mode Select 'Host Debugger' if Trace Hub is used with host debugger tool or 'Target Debugger' if Trace Hub is used by target debugger software or 'Disable' trace hub functionality.

0: Disable, 1: Target Debugger Mode, 2: Host Debugger Mode

Definition at line [229](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_CONFIG::PcieImrSize**

---

Offset 0x0456 - Size of PCIe IMR.

Size of PCIe IMR in megabytes

Definition at line [1389](#) of file [FspmUpd.h](#).

## **UINT32 FSP\_M\_CONFIG::PcieRpEnableMask**

---

Offset 0x045C - Enable PCIE RP Mask Enable/disable PCIE Root Ports.

0: disable, 1: enable. One bit for each port, bit0 for port1, bit1 for

port2, and so on.

Definition at line [1400](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::PeciC10Reset**

---

Offset 0x00F6 - Enable or Disable Peci C10 Reset command  
Enable or Disable Peci C10 Reset command.

If Enabled, BIOS will send the CPU message to disable peci reset on C10 exit. The default value is **0: Disable** for CNL, and **1: Enable** for all other CPU's \$EN\_DIS

Definition at line [494](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::PeciSxReset**

---

Offset 0x00F7 - Enable or Disable Peci Sx Reset command  
Enable or Disable Peci Sx Reset command; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line [500](#) of file [FspmUpd.h](#).

## **UINT32 FSP\_M\_CONFIG::PegDataPtr**

---

Offset 0x0152 - Memory data pointer for saved preset search results  
The reference code will store the Gen3 Preset Search results in the SaDataHob's PegData structure (SA\_PEG\_DATA) and platform code can save/restore this data to skip preset search in the following boots.

Range: 0-0xFFFFFFFF, default is 0

Definition at line [748](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::PegDisableSpreadSpectrumClocking**

---

Offset 0x0124 - PCIe Disable Spread Spectrum Clocking PCIe  
Disable Spread Spectrum Clocking.

Normal Operation(0x0)(Default) - SSC enabled, Disable SSC(0X1) -  
Disable SSC per platform design or for compliance testing 0:Normal  
Operation, 1:Disable SSC

Definition at line [693](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::PlatformDebugConsent**

---

Offset 0x00AA - Platform Debug Consent To 'opt-in' for debug,  
please select 'Enabled' with the desired debug probe type.

Enabling this BIOS option may alter the default value of other  
debug-related BIOS options. Note: DCI OOB (aka BSSB) uses CCA  
probe; [DCI OOB+DbC] and [USB2 DbC] have the same setting  
0:Disabled, 1:Enabled (DCI OOB+[DbC]), 2:Enabled (DCI OOB),  
3:Enabled (USB3 DbC), 4:Enabled (XDP/MIPI60), 5:Enabled (USB2  
DbC)

Definition at line [215](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::ProbelessTrace**

---

Offset 0x00A2 - Probeless Trace Probeless Trace: 0=Disabled,  
1=Enable.

Enabling Probeless Trace will reserve 128MB. This also requires  
IED to be enabled. \$EN\_DIS

Definition at line [183](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::PwdwnIdleCounter**

---

Offset 0x0502 - Pwr Down Idle Timer The minimum value should = to the worst case Roundtrip delay + Burst\_Length.

0 means AUTO: 64 for ULX/ULT, 128 for DT/Halo

Definition at line [2224](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::RankInterleave**

---

Offset 0x049B - Rank Interleave support Enables/Disable Rank Interleave support.

NOTE: RI and HORI can not be enabled at the same time. \$EN\_DIS

Definition at line [1685](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::Ratio**

---

Offset 0x00DC - Memory Ratio Automatic or the frequency will equal ratio times reference clock.

Set to Auto to recalculate memory timings listed below. 0:Auto, 4:4, 5:5, 6:6, 7:7, 8:8, 9:9, 10:10, 11:11, 12:12, 13:13, 14:14, 15:15

Definition at line [370](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_CONFIG::RcompResistor[3]**

---

Offset 0x0082 - RcompResister settings Indicates RcompReister settings: CNL - 0's means MRC auto configured based on Design Guidelines, otherwise input an Ohmic value per segment.

CFL will need to provide the appropriate values.

Definition at line [114](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_CONFIG::RcompTarget[5]**

---

Offset 0x0088 - RcompTarget settings RcompTarget settings: CNL - 0's mean MRC auto configured based on Design Guidelines, otherwise input an Ohmic value per segment.

CFL will need to provide the appropriate values.

Definition at line [120](#) of file **FspmUpd.h**.

## **UINT8 FSP\_M\_CONFIG::RealtimeMemoryTiming**

---

Offset 0x01F0 - Realtime Memory Timing 0(Default): Disabled, 1: Enabled.

When enabled, it will allow the system to perform realtime memory timing changes after MRC\_DONE. 0: Disabled, 1: Enabled

Definition at line [875](#) of file **FspmUpd.h**.

## **UINT8 FSP\_M\_CONFIG::RefClk**

---

Offset 0x00D9 - Memory Reference Clock 100MHz, 133MHz.

0:133MHz, 1:100MHz

Definition at line [356](#) of file **FspmUpd.h**.

## **UINT8 FSP\_M\_CONFIG::RhSolution**

---

Offset 0x04F4 - Row Hammer Solution Type of method used to prevent Row Hammer.

Default is Hardware RHP 0:Hardware RHP, 1:2x Refresh

Definition at line [2128](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::RingDownBin**

---

Offset 0x021A - Ring Downbin Ring Downbin enable/disable.

When enabled, CPU will ensure the ring ratio is always lower than the core ratio.  
0: Disable; **1: Enable.** \$EN\_DIS

Definition at line [1075](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::RingMaxOcRatio**

---

Offset 0x0208 - Maximum clr turbo ratio override Maximum clr turbo ratio override allows to increase CPU clr frequency beyond the fused max turbo ratio limit.

**0: Hardware defaults.** Range: 0-255

Definition at line [981](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::RingPllVoltageOffset**

---

Offset 0x0474 - Ring PLL voltage offset Core PLL voltage offset.

**0: No offset.** Range 0-63

Definition at line [1451](#) of file [FspmUpd.h](#).

### **UINT16 FSP\_M\_CONFIG::RingVoltageAdaptive**

---

Offset 0x021E - Ring Turbo voltage Adaptive Extra Turbo voltage applied to the cpu ring when the cpu is operating in turbo mode.

Valid Range 0 to 2000

Definition at line [1093](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::RingVoltageMode**

---

Offset 0x021B - Ring voltage mode Ring voltage mode; 0: Adaptive;  
1: Override.

\$EN\_DIS

Definition at line [1081](#) of file [FspmUpd.h](#).

### **UINT16 FSP\_M\_CONFIG::RingVoltageOffset**

---

Offset 0x0220 - Ring Turbo voltage Offset The voltage offset applied  
to the ring while operating in turbo mode.

Valid Range 0 to 1000

Definition at line [1098](#) of file [FspmUpd.h](#).

### **UINT16 FSP\_M\_CONFIG::RingVoltageOverride**

---

Offset 0x021C - Ring voltage override The ring voltage override  
which is applied to the entire range of cpu ring frequencies.

Valid Range 0 to 2000

Definition at line [1087](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::RMT**

---

Offset 0x00C4 - Rank Margin Tool Enable/disable Rank Margin Tool.

\$EN\_DIS

Definition at line [314](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::RMTLoopCount**

---

Offset 0x050D - RMTLoopCount Specifies the Loop Count to be used during Rank Margin Tool Testing.

0 - AUTO

Definition at line [2285](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::RmtPerTask**

---

Offset 0x0096 - Rank Margin Tool per Task This option enables the user to execute Rank Margin Tool per major training step in the MRC.

\$EN\_DIS

Definition at line [152](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::SafeMode**

---

Offset 0x0508 - Safe Mode Support This option configures the varous items in the IO and MC to be more conservative.

(def=Disable) \$EN\_DIS

Definition at line [2263](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::SaGv**

---

Offset 0x00BC - SA GV System Agent dynamic frequency support and when enabled memory will be training at two different frequencies.

Only effects ULX/ULT CPUs. 0=Disabled, 1=FixedLow, 2=FixedHigh, and 3=Enabled. 0:Disabled, 1:FixedLow, 2:FixedHigh, 3:Enabled

Definition at line [282](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::SaPIIVoltageOffset**

---

Offset 0x0475 - System Agent PLL voltage offset Core PLL voltage offset.

**0: No offset.** Range 0-63

Definition at line [1456](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::ScramblerSupport**

---

Offset 0x00C7 - Scrambler Support This option enables data scrambling in memory.

\$EN\_DIS

Definition at line [332](#) of file [FspmUpd.h](#).

## **UINT32 FSP\_M\_CONFIG::SinitMemorySize**

---

Offset 0x022C - SinitMemorySize Enable/Disable.

0: Disable, define default value of SinitMemorySize , 1: enable

Definition at line [1140](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::SkipMpInit**

---

Offset 0x00C8 - Skip Multi-Processor Initialization When this is

skipped, boot loader must initialize processors before SiliconInit API.

0: Initialize; 1: Skip \$EN\_DIS

Definition at line [339](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::SmbusArpEnable**

---

Offset 0x0452 - Enable SMBus ARP support Enable SMBus ARP support.

\$EN\_DIS

Definition at line [1374](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::SmbusEnable**

---

Offset 0x00A5 - Enable SMBus Enable/disable SMBus controller.

\$EN\_DIS

Definition at line [199](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::SpdAddressTable[4]**

---

Offset 0x00A6 - Spd Address Tabl Specify SPD Address table for CH0D0/CH0D1/CH1D0&CH1D1.

MemorySpdPtr will be used if SPD Address is 00

Definition at line [205](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::SpdProfileSelected**

---

Offset 0x00D8 - SPD Profile Selected Select DIMM timing profile.

Options are 0=Default profile, 1=Custom profile, 2=XMP Profile 1, 3=XMP Profile 2 0:Default profile, 1:Custom profile, 2:XMP profile 1, 3:XMP profile 2

Definition at line [350](#) of file [FspmUpd.h](#).

### **UINT32 FSP\_M\_CONFIG::TgaSize**

---

Offset 0x024C - TgaSize Enable/Disable.

0: Disable, define default value of TgaSize , 1: enable

Definition at line [1175](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::ThrtCkeMinTmr**

---

Offset 0x04ED - Throttler CKEMin Timer Timer value for CKEMin, range[255;0].

Req'd min of SC\_ROUND\_T + BYTE\_LENGTH (4). Default is 0x30

Definition at line [2088](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::ThrtCkeMinTmrLpddr**

---

Offset 0x0514 - Throttler CKEMin Timer - LPDDR Timer value for CKEMin (For LPDDR Only), range[255;0].

Req'd min of SC\_ROUND\_T + BYTE\_LENGTH (4). Default is 0x40

Definition at line [2323](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::TjMaxOffset**

---

Offset 0x0222 - TjMax Offset TjMax offset.Specified value here is clipped by pCode (125 - TjMax Offset) to support TjMax in the range of 62 to 115 deg Celsius.

Valid Range 10 - 63

Definition at line [1104](#) of file **FspmUpd.h**.

## **UINT8 FSP\_M\_CONFIG::TrainTrace**

---

Offset 0x0097 - Training Trace This option enables the trained state tracing feature in MRC.

This feature will print out the key training parameters state across major training steps. \$EN\_DIS

Definition at line [159](#) of file **FspmUpd.h**.

## **UINT8 FSP\_M\_CONFIG::tRTP**

---

Offset 0x00EA - tRTP Min Internal Read to Precharge Command Delay Time, 0: AUTO, max: 15.

DDR4 legal values: 5, 6, 7, 8, 9, 10, 12

Definition at line [422](#) of file **FspmUpd.h**.

## **UINT32 FSP\_M\_CONFIG::TsegSize**

---

Offset 0x009C - Tseg Size Size of SMRAM memory reserved.

0x400000 for Release build and 0x1000000 for Debug build  
0x0400000:4MB, 0x01000000:16MB

Definition at line [171](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::TsodAlarmwindowLockBit**

---

Offset 0x04FC - Alarm window lock bit  
Disable:Alarm trips are not locked and can be changed.

Enable:Alarm trips are locked and cannot be changed \$EN\_DIS

Definition at line [2184](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::TsodCriticalEventOnly**

---

Offset 0x04FA - Critical event only  
Disable:Trips on alarm or critical.

Enable:Trips only if critical temperature is reached \$EN\_DIS

Definition at line [2170](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::TsodCriticaltripLockBit**

---

Offset 0x04FD - Critical trip lock bit  
Disable:Critical trip is not locked and can be changed.

Enable:Critical trip is locked and cannot be changed \$EN\_DIS

Definition at line [2191](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::TsodEventManager**

---

Offset 0x04F8 - Event mode  
Disable:Comparator mode.

Enable:Interrupt mode \$EN\_DIS

Definition at line [2156](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::TsodEventOutputControl**

---

Offset 0x04FB - Event output control Disable:Event output disable.

Enable:Event output enabled \$EN\_DIS

Definition at line [2177](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::TsodEventPolarity**

---

Offset 0x04F9 - EVENT polarity Disable:Active LOW.

Enable:Active HIGH \$EN\_DIS

Definition at line [2163](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::TsodManualEnable**

---

Offset 0x0500 - User Manual Thig and Tcrit Disabled(Default):  
Temperature will be given by the configuration of memories and 1x  
or 2xrefresh rate.

Enabled: User Input will define for Thigh and Tcrit. \$EN\_DIS

Definition at line [2211](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::TsodShutdownMode**

---

Offset 0x04FE - Shutdown mode Disable:Temperature sensor enable.

Enable:Temperature sensor disable \$EN\_DIS

Definition at line [2198](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::TsodTcritMax**

---

Offset 0x04F7 - TcritMax Maximum Critical Temperature in Centigrade of the On-DIMM Thermal Sensor.

TCRITMax has to be greater than THIGHMax .  
Critical temperature will be TcritMax

Definition at line [2149](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::TvbRatioClipping**

---

Offset 0x0144 - Thermal Velocity Boost Ratio clipping 0(Default):  
Disabled, 1: Enabled.

This service controls Core frequency reduction caused by high package temperatures for processors that implement the Intel Thermal Velocity Boost (TVB) feature 0: Disabled, 1: Enabled

Definition at line [725](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::TvbVoltageOptimization**

---

Offset 0x0145 - Thermal Velocity Boost voltage optimization 0:  
Disabled, 1: Enabled(Default).

This service controls thermal based voltage optimizations for

processors that implement the Intel Thermal Velocity Boost (TVB) feature. 0: Disabled, 1: Enabled

Definition at line [732](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::Txt**

---

Offset 0x0226 - Txt Enable/Disable.

0: Disable, Enable/Disable Txt feature, 1: enable \$EN\_DIS

Definition at line [1126](#) of file [FspmUpd.h](#).

### **UINT64 FSP\_M\_CONFIG::TxtDprMemoryBase**

---

Offset 0x0238 - TxtDprMemoryBase Enable/Disable.

0: Disable, define default value of TxtDprMemoryBase , 1: enable

Definition at line [1155](#) of file [FspmUpd.h](#).

### **UINT32 FSP\_M\_CONFIG::TxtDprMemorySize**

---

Offset 0x0234 - TxtDprMemorySize Enable/Disable.

0: Disable, define default value of TxtDprMemorySize , 1: enable

Definition at line [1150](#) of file [FspmUpd.h](#).

### **UINT32 FSP\_M\_CONFIG::TxtHeapMemorySize**

---

Offset 0x0230 - TxtHeapMemorySize Enable/Disable.

0: Disable, define default value of TxtHeapMemorySize , 1: enable

Definition at line [1145](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::TxtImplemented**

---

Offset 0x01E3 - Enable/Disable MRC TXT dependency When enabled MRC execution will wait for TXT initialization to be done first.

Disabled(0x0)(Default): MRC will not wait for TXT initialization,  
Enabled(0x1): MRC will wait for TXT initialization \$EN\_DIS

Definition at line [826](#) of file [FspmUpd.h](#).

## **UINT64 FSP\_M\_CONFIG::TxtLcpPdBase**

---

Offset 0x0250 - TxtLcpPdBase Enable/Disable.

0: Disable, define default value of TxtLcpPdBase , 1: enable

Definition at line [1180](#) of file [FspmUpd.h](#).

## **UINT64 FSP\_M\_CONFIG::TxtLcpPdSize**

---

Offset 0x0258 - TxtLcpPdSize Enable/Disable.

0: Disable, define default value of TxtLcpPdSize , 1: enable

Definition at line [1185](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_CONFIG::UserBudgetEnable**

---

Offset 0x04F6 - User Manual Budget Disabled: Configuration of memories will defined the Budget value.

Enabled: User Input will be used. \$EN\_DIS

Definition at line [2142](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::UserThresholdEnable**

---

Offset 0x04F5 - User Manual Threshold Disabled: Predefined threshold will be used.

Enabled: User Input will be used. \$EN\_DIS

Definition at line [2135](#) of file [FspmUpd.h](#).

### **UINT16 FSP\_M\_CONFIG::VddVoltage**

---

Offset 0x00DA - Memory Voltage Memory Voltage Override (Vddq).

Default = no override 0:Default, 1200:1.20 Volts, 1250:1.25 Volts, 1300:1.30 Volts, 1350:1.35 Volts, 1400:1.40 Volts, 1450:1.45 Volts, 1500:1.50 Volts, 1550:1.55 Volts, 1600:1.60 Volts, 1650:1.65 Volts

Definition at line [363](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::VmxEnable**

---

Offset 0x020F - Enable or Disable VMX Enable or Disable VMX; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line [1027](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_CONFIG::WarmThresholdCh0Dimm0**

---

Offset 0x04C9 - Warm Threshold Ch0 Dimm0 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

Default is 255

Definition at line [1907](#) of file [FspmUpd.h](#).

---

### **UINT8 FSP\_M\_CONFIG::WarmThresholdCh0Dimm1**

---

Offset 0x04CA - Warm Threshold Ch0 Dimm1 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

Default is 255

Definition at line [1912](#) of file [FspmUpd.h](#).

---

### **UINT8 FSP\_M\_CONFIG::WarmThresholdCh1Dimm0**

---

Offset 0x04CB - Warm Threshold Ch1 Dimm0 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

Default is 255

Definition at line [1917](#) of file [FspmUpd.h](#).

---

### **UINT8 FSP\_M\_CONFIG::WarmThresholdCh1Dimm1**

---

Offset 0x04CC - Warm Threshold Ch1 Dimm1 range[255;0]=[31.875;0] in W for OLTM, [127.5;0] in C for CLTM.

Default is 255

Definition at line [1922](#) of file [FspmUpd.h](#).

---

The documentation for this struct was generated from the following file:

- [FspmUpd.h](#)

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(FSP) Integration Guide by [doxygen](#) 1.8.10



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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<b>FSP_M_TEST_CONFIG</b> <b>Struct Reference</b>			<a href="#">Public Attributes</a>   <a href="#">List of all members</a>

Fsp M Test Configuration. [More...](#)

```
#include <FspmUpd.h>
```

## Public Attributes

UINT32 **Signature**

Offset 0x0520.

UINT8 **SkipExtGfxScan**

Offset 0x0524 - Skip external display device scanning  
Enable: Do not scan for external display device, Disable  
(Default): Scan external display devices \$EN\_DIS.

UINT8 **BdatEnable**

Offset 0x0525 - Generate BIOS Data ACPI Table  
Enable: Generate BDAT for MRC RMT or SA PCIe data. [More...](#)

UINT8 **ScanExtGfxForLegacyOpRom**

Offset 0x0526 - Detect External Graphics device for  
LegacyOpROM Detect and report if external graphics  
device only support LegacyOpROM or not (to support CSM  
auto-enable). [More...](#)

UINT8 **LockPTMregs**

Offset 0x0527 - Lock PCU Thermal Management registers  
Lock PCU Thermal Management registers. [More...](#)

UINT8 **DmiMaxLinkSpeed**

Offset 0x0528 - DMI Max Link Speed Auto (Default)(0x0):  
Maximum possible link speed, Gen1(0x1): Limit Link to  
Gen1 Speed, Gen2(0x2): Limit Link to Gen2 Speed,  
Gen3(0x3):Limit Link to Gen3 Speed 0:Auto, 1:Gen1,  
2:Gen2, 3:Gen3.

UINT8 **DmiGen3EqPh2Enable**

Offset 0x0529 - DMI Equalization Phase 2 DMI Equalization  
Phase 2. [More...](#)

UINT8 **DmiGen3EqPh3Method**

Offset 0x052A - DMI Gen3 Equalization Phase3 DMI Gen3 Equalization Phase3. [More...](#)

UINT8 **Peg0Gen3EqPh2Enable**

Offset 0x052B - Phase2 EQ enable on the PEG 0:1:0.  
[More...](#)

UINT8 **Peg1Gen3EqPh2Enable**

Offset 0x052C - Phase2 EQ enable on the PEG 0:1:1.  
[More...](#)

UINT8 **Peg2Gen3EqPh2Enable**

Offset 0x052D - Phase2 EQ enable on the PEG 0:1:2.  
[More...](#)

UINT8 **Peg3Gen3EqPh2Enable**

Offset 0x052E - Phase2 EQ enable on the PEG 0:1:3.  
[More...](#)

UINT8 **Peg0Gen3EqPh3Method**

Offset 0x052F - Phase3 EQ method on the PEG 0:1:0.  
[More...](#)

UINT8 **Peg1Gen3EqPh3Method**

Offset 0x0530 - Phase3 EQ method on the PEG 0:1:1.  
[More...](#)

UINT8 **Peg2Gen3EqPh3Method**

Offset 0x0531 - Phase3 EQ method on the PEG 0:1:2.  
[More...](#)

UINT8 **Peg3Gen3EqPh3Method**

Offset 0x0532 - Phase3 EQ method on the PEG 0:1:3.  
[More...](#)

UINT8 **PegGen3ProgramStaticEq**

Offset 0x0533 - Enable/Disable PEG GEN3 Static EQ

Phase1 programming Program PEG Gen3 EQ Phase1  
Static Presets. [More...](#)

**UINT8 [Gen3SwEqAlwaysAttempt](#)**

Offset 0x0534 - PEG Gen3 SwEq Always Attempt Gen3 Software Equalization will be executed every boot. [More...](#)

**UINT8 [Gen3SwEqNumberOfPresets](#)**

Offset 0x0535 - Select number of TxEq presets to test in the PCIe/DMI SwEq Select number of TxEq presets to test in the PCIe/DMI SwEq. [More...](#)

**UINT8 [Gen3SwEqEnableVocTest](#)**

Offset 0x0536 - Enable use of the Voltage Offset and Centering Test in the PCIe SwEq Enable use of the Voltage Offset and Centering Test in the PCIe Software Equalization Algorithm. [More...](#)

**UINT8 [PegRxCemTestingMode](#)**

Offset 0x0537 - PCIe Rx Compliance Testing Mode  
Disabled(0x0)(Default): Normal Operation - Disable PCIe Rx Compliance testing, Enabled(0x1): PCIe Rx Compliance Test Mode - PEG controller is in Rx Compliance Testing Mode; it should only be set when doing PCIe compliance testing \$EN\_DIS.

**UINT8 [PegRxCemLoopbackLane](#)**

Offset 0x0538 - PCIe Rx Compliance Loopback Lane When PegRxCemTestingMode is Enabled the specified Lane (0 - 15) will be used for RxCEMLoopback. [More...](#)

**UINT8 [PegGenerateBdatMarginTable](#)**

Offset 0x0539 - Generate PCIe BDAT Margin Table Set this policy to enable the generation and addition of PCIe margin data to the BDAT table. [More...](#)

**UINT8 [PegRxCemNonProtocolAwareness](#)**

Offset 0x053A - PCIe Non-Protocol Awareness for Rx Compliance Testing Set this policy to enable the generation and addition of PCIe margin data to the BDAT table. [More...](#)

**UINT8 [PegGen3RxCtleOverride](#)**

Offset 0x053B - PCIe Override RxCTLE Disable(0x0)  
(Default): Normal Operation - RxCTLE adaptive behavior enabled, Enable(0x1): Override RxCTLE - Disable RxCTLE adaptive behavior to keep the configured RxCTLE peak values unmodified \$EN\_DIS.

**UINT8 [PegGen3Rsvd](#)**

Offset 0x053C - Rsvd Disable(0x0)(Default): Normal Operation - RxCTLE adaptive behavior enabled, Enable(0x1): Override RxCTLE - Disable RxCTLE adaptive behavior to keep the configured RxCTLE peak values unmodified \$EN\_DIS.

**UINT8 [PegGen3RootPortPreset](#) [20]**

Offset 0x053D - PEG Gen3 Root port preset values per lane Used for programming PEG Gen3 preset values per lane. [More...](#)

**UINT8 [PegGen3EndPointPreset](#) [20]**

Offset 0x0551 - PEG Gen3 End port preset values per lane Used for programming PEG Gen3 preset values per lane. [More...](#)

**UINT8 [PegGen3EndPointHint](#) [20]**

Offset 0x0565 - PEG Gen3 End port Hint values per lane Used for programming PEG Gen3 Hint values per lane. [More...](#)

**UINT8 [UnusedUpdSpace8](#)**

Offset 0x0579.

**UINT16 [Gen3SwEqJitterDwellTime](#)**

Offset 0x057A - Jitter Dwell Time for PCIe Gen3 Software

Equalization Range: 0-65535, default is 1000. [More...](#)

**UINT16 Gen3SwEqJitterErrorTarget**

Offset 0x057C - Jitter Error Target for PCIe Gen3 Software  
Equalization Range: 0-65535, default is 1. [More...](#)

**UINT16 Gen3SwEqVocDwellTime**

Offset 0x057E - VOC Dwell Time for PCIe Gen3 Software  
Equalization Range: 0-65535, default is 10000. [More...](#)

**UINT16 Gen3SwEqVocErrorTarget**

Offset 0x0580 - VOC Error Target for PCIe Gen3 Software  
Equalization Range: 0-65535, default is 2. [More...](#)

**UINT8 PanelPowerEnable**

Offset 0x0582 - Panel Power Enable Control for  
enabling/disabling VDD force bit (Required only for early  
enabling of eDP panel). [More...](#)

**UINT8 BdatTestType**

Offset 0x0583 - BdatTestType Indicates the type of Memory  
Training data to populate into the BDAT ACPI table. [More...](#)

**UINT8 SaPreMemTestRsvd [12]**

Offset 0x0584 - SaPreMemTestRsvd Reserved for SA Pre-  
Mem Test \$EN\_DIS.

**UINT16 TotalFlashSize**

Offset 0x0590 - TotalFlashSize Enable/Disable. [More...](#)

**UINT16 BiosSize**

Offset 0x0592 - BiosSize Enable/Disable. [More...](#)

**UINT8 TxtAcheckRequest**

Offset 0x0594 - TxtAcheckRequest Enable/Disable. [More...](#)

**UINT8 [SecurityTestRsvd](#) [3]**  
Offset 0x0595 - SecurityTestRsvd Reserved for SA Pre-Mem Test \$EN\_DIS.

**UINT8 [SmbusDynamicPowerGating](#)**  
Offset 0x0598 - Smbus dynamic power gating Disable or Enable Smbus dynamic power gating. [More...](#)

**UINT8 [WdtDisableAndLock](#)**  
Offset 0x0599 - Disable and Lock Watch Dog Register Set 1 to clear WDT status, then disable and lock WDT registers. [More...](#)

**UINT8 [SmbusSpdWriteDisable](#)**  
Offset 0x059A - SMBUS SPD Write Disable Set/Clear Smbus SPD Write Disable. [More...](#)

**UINT8 [ChipsetInitMessage](#)**  
Offset 0x059B - ChipsetInit HECI message DEPRECATED \$EN\_DIS.

**UINT8 [BypassPhySyncReset](#)**  
Offset 0x059C - Bypass ChipsetInit sync reset. [More...](#)

**UINT8 [DidInitStat](#)**  
Offset 0x059D - Force ME DID Init Status Test, 0: disable, 1: Success, 2: No Memory in Channels, 3: Memory Init Error, Set ME DID init stat value \$EN\_DIS.

**UINT8 [DisableCpuReplacedPolling](#)**  
Offset 0x059E - CPU Replaced Polling Disable Test, 0: disable, 1: enable, Setting this option disables CPU replacement polling loop \$EN\_DIS.

**UINT8 [SendDidMsg](#)**  
Offset 0x059F - ME DID Message Test, 0: disable, 1: enable, Enable/Disable ME DID Message (disable will

prevent the DID message from being sent) \$EN\_DIS.

**UINT8 DisableHeciRetry**

Offset 0x05A0 - Retry mechanism for HECL APIs Test, 0: disable, 1: enable, Enable/Disable HECL retry. [More...](#)

**UINT8 DisableMessageCheck**

Offset 0x05A1 - Check HECL message before send Test, 0: disable, 1: enable, Enable/Disable message check. [More...](#)

**UINT8 SkipMbpHob**

Offset 0x05A2 - Skip MBP HOB Test, 0: disable, 1: enable, Enable/Disable MOB HOB. [More...](#)

**UINT8 HeciCommunication2**

Offset 0x05A3 - HECL2 Interface Communication Test, 0: disable, 1: enable, Adds or Removes HECL2 Device from PCI space. [More...](#)

**UINT8 KtDeviceEnable**

Offset 0x05A4 - Enable KT device Test, 0: disable, 1: enable, Enable or Disable KT device. [More...](#)

**UINT8 tRd2RdSG**

Offset 0x05A5 - tRd2RdSG Delay between Read-to-Read commands in the same Bank Group. [More...](#)

**UINT8 tRd2RdDG**

Offset 0x05A6 - tRd2RdDG Delay between Read-to-Read commands in different Bank Group for DDR4. [More...](#)

**UINT8 tRd2RdDR**

Offset 0x05A7 - tRd2RdDR Delay between Read-to-Read commands in different Ranks. [More...](#)

**UINT8 tRd2RdDD**

Offset 0x05A8 - tRd2RdDD Delay between Read-to-Read

commands in different DIMMs. [More...](#)

**UINT8 [tWr2RdSG](#)**

Offset 0x05A9 - tWr2RdSG Delay between Write-to-Read commands in the same Bank Group. [More...](#)

**UINT8 [tWr2RdDG](#)**

Offset 0x05AA - tWr2RdDG Delay between Write-to-Read commands in different Bank Group for DDR4. [More...](#)

**UINT8 [tWr2RdDR](#)**

Offset 0x05AB - tWr2RdDR Delay between Write-to-Read commands in different Ranks. [More...](#)

**UINT8 [tWr2RdDD](#)**

Offset 0x05AC - tWr2RdDD Delay between Write-to-Read commands in different DIMMs. [More...](#)

**UINT8 [tWr2WrSG](#)**

Offset 0x05AD - tWr2WrSG Delay between Write-to-Write commands in the same Bank Group. [More...](#)

**UINT8 [tWr2WrDG](#)**

Offset 0x05AE - tWr2WrDG Delay between Write-to-Write commands in different Bank Group for DDR4. [More...](#)

**UINT8 [tWr2WrDR](#)**

Offset 0x05AF - tWr2WrDR Delay between Write-to-Write commands in different Ranks. [More...](#)

**UINT8 [tWr2WrDD](#)**

Offset 0x05B0 - tWr2WrDD Delay between Write-to-Write commands in different DIMMs. [More...](#)

**UINT8 [tRd2WrSG](#)**

Offset 0x05B1 - tRd2WrSG Delay between Read-to-Write commands in the same Bank Group. [More...](#)

**UINT8 [tRd2WrDG](#)**

Offset 0x05B2 - tRd2WrDG Delay between Read-to-Write commands in different Bank Group for DDR4. [More...](#)

**UINT8 [tRd2WrDR](#)**

Offset 0x05B3 - tRd2WrDR Delay between Read-to-Write commands in different Ranks. [More...](#)

**UINT8 [tRd2WrDD](#)**

Offset 0x05B4 - tRd2WrDD Delay between Read-to-Write commands in different DIMMs. [More...](#)

**UINT8 [tRRD\\_L](#)**

Offset 0x05B5 - tRRD\_L Min Row Active to Row Active Delay Time for Same Bank Group, DDR4 Only. [More...](#)

**UINT8 [tRRD\\_S](#)**

Offset 0x05B6 - tRRD\_S Min Row Active to Row Active Delay Time for Different Bank Group, DDR4 Only. [More...](#)

**UINT8 [tWTR\\_L](#)**

Offset 0x05B7 - tWTR\_L Min Internal Write to Read Command Delay Time for Same Bank Group, DDR4 Only. [More...](#)

**UINT8 [tWTR\\_S](#)**

Offset 0x05B8 - tWTR\_S Min Internal Write to Read Command Delay Time for Different Bank Group, DDR4 Only. [More...](#)

**UINT8 [ReservedFspmTestUpd](#) [3]**

Offset 0x05B9.

## Detailed Description

---

Fsp M Test Configuration.

Definition at line **2332** of file **FspmUpd.h**.

## Member Data Documentation

---

### **UINT8 FSP\_M\_TEST\_CONFIG::BdatEnable**

---

Offset 0x0525 - Generate BIOS Data ACPI Table Enable: Generate BDAT for MRC RMT or SA PCIe data.

Disable (Default): Do not generate it \$EN\_DIS

Definition at line [2349](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::BdatTestType**

---

Offset 0x0583 - BdatTestType Indicates the type of Memory Training data to populate into the BDAT ACPI table.

0:Rank Margin Tool, 1:Margin2D

Definition at line [2585](#) of file [FspmUpd.h](#).

### **UINT16 FSP\_M\_TEST\_CONFIG::BiosSize**

---

Offset 0x0592 - BiosSize Enable/Disable.

0: Disable, define default value of BiosSize , 1: enable

Definition at line [2601](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::BypassPhySyncReset**

---

Offset 0x059C - Bypass ChipsetInit sync reset.

**DEPRECATED \$EN\_DIS**

Definition at line [2644](#) of file [FspmUpd.h](#).

---

### **UINT8 FSP\_M\_TEST\_CONFIG::DisableHeciRetry**

Offset 0x05A0 - Retry mechanism for HECI APIs Test, 0: disable, 1: enable, Enable/Disable HECI retry.

**\$EN\_DIS**

Definition at line [2670](#) of file [FspmUpd.h](#).

---

### **UINT8 FSP\_M\_TEST\_CONFIG::DisableMessageCheck**

Offset 0x05A1 - Check HECI message before send Test, 0: disable, 1: enable, Enable/Disable message check.

**\$EN\_DIS**

Definition at line [2676](#) of file [FspmUpd.h](#).

---

### **UINT8 FSP\_M\_TEST\_CONFIG::DmiGen3EqPh2Enable**

Offset 0x0529 - DMI Equalization Phase 2 DMI Equalization Phase 2.

(0x0): Disable phase 2, (0x1): Enable phase 2, (0x2)(Default): AUTO - Use the current default method 0:Disable phase2, 1:Enable phase2, 2:Auto

Definition at line [2376](#) of file [FspmUpd.h](#).

---

### **UINT8 FSP\_M\_TEST\_CONFIG::DmiGen3EqPh3Method**

Offset 0x052A - DMI Gen3 Equalization Phase3 DMI Gen3 Equalization Phase3.

Auto(0x0)(Default): Use the current default method, HwEq(0x1): Use Adaptive Hardware Equalization, SwEq(0x2): Use Adaptive Software Equalization (Implemented in BIOS Reference Code), Static(0x3): Use the Static EQs provided in DmiGen3EndPointPreset array for Phase1 AND Phase3 (Instead of just Phase1), Disabled(0x4): Bypass Equalization Phase 3 0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq, 4:BypassPhase3

Definition at line [2386](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::Gen3SwEqAlwaysAttempt**

---

Offset 0x0534 - PEG Gen3 SwEq Always Attempt Gen3 Software Equalization will be executed every boot.

Disabled(0x0)(Default): Reuse EQ settings saved/restored from NVRAM whenever possible, Enabled(0x1): Re-test and generate new EQ values every boot, not recommended 0:Disable, 1:Enable

Definition at line [2469](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::Gen3SwEqEnableVocTest**

---

Offset 0x0536 - Enable use of the Voltage Offset and Centering Test in the PCIe SwEq Enable use of the Voltage Offset and Centering Test in the PCIe Software Equalization Algorithm.

Disabled(0x0): Disable VOC Test, Enabled(0x1): Enable VOC Test, Auto(0x2)(Default): Use the current default 0:Disable, 1:Enable, 2:Auto

Definition at line [2487](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_TEST\_CONFIG::Gen3SwEqJitterDwellTime**

---

Offset 0x057A - Jitter Dwell Time for PCIe Gen3 Software Equalization Range: 0-65535, default is 1000.

### **Warning**

Do not change from the default

Definition at line [2557](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_TEST\_CONFIG::Gen3SwEqJitterErrorTarget**

---

Offset 0x057C - Jitter Error Target for PCIe Gen3 Software Equalization Range: 0-65535, default is 1.

### **Warning**

Do not change from the default

Definition at line [2562](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::Gen3SwEqNumberOfPresets**

---

Offset 0x0535 - Select number of TxEq presets to test in the PCIe/DMI SwEq Select number of TxEq presets to test in the PCIe/DMI SwEq.

P7,P3,P5(0x0): Test Presets 7, 3, and 5, P0-P9(0x1): Test Presets 0-9, Auto(0x2)(Default): Use the current default method (Default)Auto will test Presets 7, 3, and 5. It is possible for this default to change over time;using Auto will ensure Reference Code always uses the latest default settings 0:P7 P3 P5, 1:P0 to P9, 2:Auto

Definition at line [2479](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_TEST\_CONFIG::Gen3SwEqVocDwellTime**

---

Offset 0x057E - VOC Dwell Time for PCIe Gen3 Software Equalization Range: 0-65535, default is 10000.

### Warning

Do not change from the default

Definition at line [2567](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_TEST\_CONFIG::Gen3SwEqVocErrorTarget**

---

Offset 0x0580 - VOC Error Target for PCIe Gen3 Software Equalization Range: 0-65535, default is 2.

### Warning

Do not change from the default

Definition at line [2572](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::HeciCommunication2**

---

Offset 0x05A3 - HECI2 Interface Communication Test, 0: disable, 1: enable, Adds or Removes HECI2 Device from PCI space.

\$EN\_DIS

Definition at line [2688](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::KtDeviceEnable**

---

Offset 0x05A4 - Enable KT device Test, 0: disable, 1: enable, Enable or Disable KT device.

\$EN\_DIS

Definition at line [2694](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::LockPTMregs**

---

Offset 0x0527 - Lock PCU Thermal Management registers Lock PCU Thermal Management registers.

Enable(Default)=1, Disable=0 \$EN\_DIS

Definition at line [2362](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::PanelPowerEnable**

---

Offset 0x0582 - Panel Power Enable Control for enabling/disabling VDD force bit (Required only for early enabling of eDP panel).

0=Disable, 1(Default)=Enable \$EN\_DIS

Definition at line [2579](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::Peg0Gen3EqPh2Enable**

---

Offset 0x052B - Phase2 EQ enable on the PEG 0:1:0.

Phase2 EQ enable on the PEG 0:1:0. Disabled(0x0): Disable phase 2, Enabled(0x1): Enable phase 2, Auto(0x2)(Default): Use the current default method 0:Disable, 1:Enable, 2:Auto

Definition at line [2393](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::Peg0Gen3EqPh3Method**

---

Offset 0x052F - Phase3 EQ method on the PEG 0:1:0.

PEG Gen3 Equalization Phase3. Auto(0x0)(Default): Use the current default method, HwEq(0x1): Use Adaptive Hardware Equalization, SwEq(0x2): Use Adaptive Software Equalization (Implemented in

BIOS Reference Code), Static(0x3): Use the Static EQs provided in DmiGen3EndPointPreset array for Phase1 AND Phase3 (Instead of just Phase1), Disabled(0x4): Bypass Equalization Phase 3 0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq, 4:BypassPhase3

Definition at line [2424](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::Peg1Gen3EqPh2Enable**

---

Offset 0x052C - Phase2 EQ enable on the PEG 0:1:1.

Phase2 EQ enable on the PEG 0:1:0. Disabled(0x0): Disable phase 2, Enabled(0x1): Enable phase 2, Auto(0x2)(Default): Use the current default method 0:Disable, 1:Enable, 2:Auto

Definition at line [2400](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::Peg1Gen3EqPh3Method**

---

Offset 0x0530 - Phase3 EQ method on the PEG 0:1:1.

PEG Gen3 Equalization Phase3. Auto(0x0)(Default): Use the current default method, HwEq(0x1): Use Adaptive Hardware Equalization, SwEq(0x2): Use Adaptive Software Equalization (Implemented in BIOS Reference Code), Static(0x3): Use the Static EQs provided in DmiGen3EndPointPreset array for Phase1 AND Phase3 (Instead of just Phase1), Disabled(0x4): Bypass Equalization Phase 3 0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq, 4:BypassPhase3

Definition at line [2434](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::Peg2Gen3EqPh2Enable**

---

Offset 0x052D - Phase2 EQ enable on the PEG 0:1:2.

Phase2 EQ enable on the PEG 0:1:0. Disabled(0x0): Disable phase

2, Enabled(0x1): Enable phase 2, Auto(0x2)(Default): Use the current default method 0:Disable, 1:Enable, 2:Auto

Definition at line [2407](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::Peg2Gen3EqPh3Method**

---

Offset 0x0531 - Phase3 EQ method on the PEG 0:1:2.

PEG Gen3 Equalization Phase3. Auto(0x0)(Default): Use the current default method, HwEq(0x1): Use Adaptive Hardware Equalization, SwEq(0x2): Use Adaptive Software Equalization (Implemented in BIOS Reference Code), Static(0x3): Use the Static EQs provided in DmiGen3EndPointPreset array for Phase1 AND Phase3 (Instead of just Phase1), Disabled(0x4): Bypass Equalization Phase 3 0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq, 4:BypassPhase3

Definition at line [2444](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::Peg3Gen3EqPh2Enable**

---

Offset 0x052E - Phase2 EQ enable on the PEG 0:1:3.

Phase2 EQ enable on the PEG 0:1:0. Disabled(0x0): Disable phase 2, Enabled(0x1): Enable phase 2, Auto(0x2)(Default): Use the current default method 0:Disable, 1:Enable, 2:Auto

Definition at line [2414](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::Peg3Gen3EqPh3Method**

---

Offset 0x0532 - Phase3 EQ method on the PEG 0:1:3.

PEG Gen3 Equalization Phase3. Auto(0x0)(Default): Use the current default method, HwEq(0x1): Use Adaptive Hardware Equalization, SwEq(0x2): Use Adaptive Software Equalization (Implemented in

BIOS Reference Code), Static(0x3): Use the Static EQs provided in DmiGen3EndPointPreset array for Phase1 AND Phase3 (Instead of just Phase1), Disabled(0x4): Bypass Equalization Phase 3 0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq, 4:BypassPhase3

Definition at line [2454](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::PegGen3EndPointHint[20]**

---

Offset 0x0565 - PEG Gen3 End port Hint values per lane Used for programming PEG Gen3 Hint values per lane.

Range: 0-6, 2 is default for each lane

Definition at line [2548](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::PegGen3EndPointPreset[20]**

---

Offset 0x0551 - PEG Gen3 End port preset values per lane Used for programming PEG Gen3 preset values per lane.

Range: 0-9, 7 is default for each lane

Definition at line [2543](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::PegGen3ProgramStaticEq**

---

Offset 0x0533 - Enable/Disable PEG GEN3 Static EQ Phase1 programming Program PEG Gen3 EQ Phase1 Static Presets.

Disabled(0x0): Disable EQ Phase1 Static Presets Programming, Enabled(0x1)(Default): Enable EQ Phase1 Static Presets Programming \$EN\_DIS

Definition at line [2461](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::PegGen3RootPortPreset[20]**

---

Offset 0x053D - PEG Gen3 Root port preset values per lane Used for programming PEG Gen3 preset values per lane.

Range: 0-9, 8 is default for each lane

Definition at line [2538](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::PegGenerateBdatMarginTable**

---

Offset 0x0539 - Generate PCIe BDAT Margin Table Set this policy to enable the generation and addition of PCIe margin data to the BDAT table.

Disabled(0x0)(Default): Normal Operation - Disable PCIe BDAT margin data generation, Enable(0x1): Generate PCIe BDAT margin data \$EN\_DIS

Definition at line [2508](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::PegRxCemLoopbackLane**

---

Offset 0x0538 - PCIe Rx Compliance Loopback Lane When PegRxCemTestingMode is Enabled the specified Lane (0 - 15) will be used for RxCEMLoopback.

Default is Lane 0

Definition at line [2500](#) of file [FspmUpd.h](#).

## **UINT8**

## **FSP\_M\_TEST\_CONFIG::PegRxCemNonProtocolAwareness**

---

Offset 0x053A - PCIe Non-Protocol Awareness for Rx Compliance Testing Set this policy to enable the generation and addition of PCIe

margin data to the BDAT table.

Disabled(0x0)(Default): Normal Operation - Disable non-protocol awareness, Enable(0x1): Non-Protocol Awareness Enabled - Enable non-protocol awareness for compliance testing \$EN\_DIS

Definition at line [2517](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::ScanExtGfxForLegacyOpRom**

---

Offset 0x0526 - Detect External Graphics device for LegacyOpROM  
Detect and report if external graphics device only support LegacyOpROM or not (to support CSM auto-enable).

Enable(Default)=1, Disable=0 \$EN\_DIS

Definition at line [2356](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::SkipMbphob**

---

Offset 0x05A2 - Skip MBP HOB Test, 0: disable, 1: enable,  
Enable/Disable MOB HOB.

\$EN\_DIS

Definition at line [2682](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::SmbusDynamicPowerGating**

---

Offset 0x0598 - Smbus dynamic power gating Disable or Enable Smbus dynamic power gating.

\$EN\_DIS

Definition at line [2619](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::SmbusSpdWriteDisable**

---

Offset 0x059A - SMBUS SPD Write Disable Set/Clear Smbus SPD Write Disable.

0: leave SPD Write Disable bit; 1: set SPD Write Disable bit. For security recommendations, SPD write disable bit must be set.  
\$EN\_DIS

Definition at line [2632](#) of file [FspmUpd.h](#).

## **UINT16 FSP\_M\_TEST\_CONFIG::TotalFlashSize**

---

Offset 0x0590 - TotalFlashSize Enable/Disable.

0: Disable, define default value of TotalFlashSize , 1: enable

Definition at line [2596](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::tRd2RdDD**

---

Offset 0x05A8 - tRd2RdDD Delay between Read-to-Read commands in different DIMMs.

0-Auto, Range 4-54.

Definition at line [2715](#) of file [FspmUpd.h](#).

## **UINT8 FSP\_M\_TEST\_CONFIG::tRd2RdDG**

---

Offset 0x05A6 - tRd2RdDG Delay between Read-to-Read commands in different Bank Group for DDR4.

All other DDR technologies should set this equal to SG. 0-Auto, Range 4-54.

Definition at line [2705](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tRd2RdDR**

---

Offset 0x05A7 - tRd2RdDR Delay between Read-to-Read commands in different Ranks.

0-Auto, Range 4-54.

Definition at line [2710](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tRd2RdSG**

---

Offset 0x05A5 - tRd2RdSG Delay between Read-to-Read commands in the same Bank Group.

0-Auto, Range 4-54.

Definition at line [2699](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tRd2WrDD**

---

Offset 0x05B4 - tRd2WrDD Delay between Read-to-Write commands in different DIMMs.

0-Auto, Range 4-54.

Definition at line [2778](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tRd2WrDG**

---

Offset 0x05B2 - tRd2WrDG Delay between Read-to-Write commands in different Bank Group for DDR4.

All other DDR technologies should set this equal to SG. 0-Auto,

Range 4-54.

Definition at line [2768](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tRd2WrDR**

---

Offset 0x05B3 - tRd2WrDR Delay between Read-to-Write commands in different Ranks.

0-Auto, Range 4-54.

Definition at line [2773](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tRd2WrSG**

---

Offset 0x05B1 - tRd2WrSG Delay between Read-to-Write commands in the same Bank Group.

0-Auto, Range 4-54.

Definition at line [2762](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tRRD\_L**

---

Offset 0x05B5 - tRRD\_L Min Row Active to Row Active Delay Time for Same Bank Group, DDR4 Only.

0: AUTO, max: 31

Definition at line [2783](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tRRD\_S**

---

Offset 0x05B6 - tRRD\_S Min Row Active to Row Active Delay Time for Different Bank Group, DDR4 Only.

0: AUTO, max: 31

Definition at line [2789](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tWr2RdDD**

---

Offset 0x05AC - tWr2RdDD Delay between Write-to-Read commands in different DIMMs.

0-Auto, Range 4-54.

Definition at line [2736](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tWr2RdDG**

---

Offset 0x05AA - tWr2RdDG Delay between Write-to-Read commands in different Bank Group for DDR4.

All other DDR technologies should set this equal to SG. 0-Auto, Range 4-54.

Definition at line [2726](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tWr2RdDR**

---

Offset 0x05AB - tWr2RdDR Delay between Write-to-Read commands in different Ranks.

0-Auto, Range 4-54.

Definition at line [2731](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tWr2RdSG**

---

Offset 0x05A9 - tWr2RdSG Delay between Write-to-Read

commands in the same Bank Group.

0-Auto, Range 4-86.

Definition at line [2720](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tWr2WrDD**

---

Offset 0x05B0 - tWr2WrDD Delay between Write-to-Write commands in different DIMMs.

0-Auto, Range 4-54.

Definition at line [2757](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tWr2WrDG**

---

Offset 0x05AE - tWr2WrDG Delay between Write-to-Write commands in different Bank Group for DDR4.

All other DDR technologies should set this equal to SG. 0-Auto, Range 4-54.

Definition at line [2747](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tWr2WrDR**

---

Offset 0x05AF - tWr2WrDR Delay between Write-to-Write commands in different Ranks.

0-Auto, Range 4-54.

Definition at line [2752](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tWr2WrSG**

---

Offset 0x05AD - tWr2WrSG Delay between Write-to-Write commands in the same Bank Group.

0-Auto, Range 4-54.

Definition at line [2741](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tWTR\_L**

---

Offset 0x05B7 - tWTR\_L Min Internal Write to Read Command Delay Time for Same Bank Group, DDR4 Only.

0: AUTO, max: 60

Definition at line [2795](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::tWTR\_S**

---

Offset 0x05B8 - tWTR\_S Min Internal Write to Read Command Delay Time for Different Bank Group, DDR4 Only.

0: AUTO, max: 28

Definition at line [2801](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::TxtAcheckRequest**

---

Offset 0x0594 - TxtAcheckRequest Enable/Disable.

When Enabled, it will forcing calling TXT Acheck once. \$EN\_DIS

Definition at line [2607](#) of file [FspmUpd.h](#).

### **UINT8 FSP\_M\_TEST\_CONFIG::WdtDisableAndLock**

---

Offset 0x0599 - Disable and Lock Watch Dog Register Set 1 to clear WDT status, then disable and lock WDT registers.

\$EN\_DIS

Definition at line [2625](#) of file [FspmUpd.h](#).

---

The documentation for this struct was generated from the following file:

- [FspmUpd.h](#)
- 

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(FSP) Integration Guide by [doxygen](#) 1.8.10



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

Main Page	Related Pages	Classes	Files
Class List	Class Index	Class Members	
<b>FSP_S_CONFIG Struct Reference</b>			<a href="#">Public Attributes</a>   <a href="#">List of all members</a>

Fsp S Configuration. More...

```
#include <FspSUpd.h>
```

## Public Attributes

UINT32 **LogoPtr**

Offset 0x0020 - Logo Pointer Points to PEI Display Logo Imag

UINT32 **LogoSize**

Offset 0x0024 - Logo Size Size of PEI Display Logo Image.

UINT32 **GraphicsConfigPtr**

Offset 0x0028 - Graphics Configuration Ptr Points to VBT.

UINT8 **Device4Enable**

Offset 0x002C - Enable Device 4 Enable/disable Device 4 \$EN

UINT8 **PchHdaDspEnable**

Offset 0x002D - Enable HD Audio DSP Enable/disable HD Au feature. [More...](#)

UINT8 **UnusedUpdSpace0 [3]**

Offset 0x002E.

UINT8 **ScsEmmcEnabled**

Offset 0x0031 - Enable eMMC Controller Enable/disable eMM Controller. [More...](#)

UINT8 **ScsEmmcHs400Enabled**

Offset 0x0032 - Enable eMMC HS400 Mode Enable eMMC HS Mode. [More...](#)

UINT8 **ScsSdCardEnabled**

Offset 0x0033 - Enable SdCard Controller Enable/disable SD Controller. [More...](#)

UINT8 **ShowSpiController**

Offset 0x0034 - Show SPI controller Enable/disable to show S controller. [More...](#)

UINT8 **UnusedUpdSpace1** [3]

Offset 0x0035.

UINT32 **MicrocodeRegionBase**

Offset 0x0038 - MicrocodeRegionBase Memory Base of Micro Updates.

UINT32 **MicrocodeRegionSize**

Offset 0x003C - MicrocodeRegionSize Size of Microcode Upd

UINT8 **TurboMode**

Offset 0x0040 - Turbo Mode Enable/Disable Turbo mode. Mor

UINT8 **SataSalpSupport**

Offset 0x0041 - Enable SATA SALP Support Enable/disable S, Aggressive Link Power Management. [More...](#)

UINT8 **SataPortsEnable** [8]

Offset 0x0042 - Enable SATA ports Enable/disable SATA ports

UINT8 **SataPortsDevSlp** [8]

Offset 0x004A - Enable SATA DEVSLP Feature Enable/disable DEVSLP per port. [More...](#)

UINT8 **PortUsb20Enable** [16]

Offset 0x0052 - Enable USB2 ports Enable/disable per USB2

[More...](#)

UINT8 **PortUsb30Enable** [10]

Offset 0x0062 - Enable USB3 ports Enable/disable per USB3

[More...](#)

UINT8 **XdcisEnabled**

Offset 0x006C - Enable xDCI controller Enable/disable to xDC controller. [More...](#)

**UINT8 UnusedUpdSpace2 [2]**

Offset 0x006D.

**UINT8 SerialloDevMode [12]**

Offset 0x006F - Enable Seriallo Device Mode 0:Disabled, 1:Pc 2:Acpi mode, 3:Hidden mode (Legacy UART mode) - Enable/Disable Seriallo I2C0,I2C1,I2C2,I2C3,I2C4,I2C5,SPI0,SPI1,SPI2,UART0,UART1 device mode respectively. [More...](#)

**UINT32 DevIntConfigPtr**

Offset 0x007B - Address of PCH\_DEVICE\_INTERRUPT\_CONFIG table. [More...](#)

**UINT8 NumOfDevIntConfig**

Offset 0x007F - Number of DevIntConfig Entry Number of Dev Interrupt Configuration Entry. [More...](#)

**UINT8 PxRcConfig [8]**

Offset 0x0080 - PIRQx to IRQx Map Config PIRQx to IRQx map. [More...](#)

**UINT8 GpioIrqRoute**

Offset 0x0088 - Select GPIO IRQ Route GPIO IRQ Select. [More...](#)

**UINT8 ScilrqSelect**

Offset 0x0089 - Select ScilrqSelect SCI IRQ Select. [More...](#)

**UINT8 TcolrqSelect**

Offset 0x008A - Select TcolrqSelect TCO IRQ Select. [More...](#)

**UINT8 TcolrqEnable**

Offset 0x008B - Enable/Disable Tco IRQ Enable/disable TCO \$EN\_DIS.

**UINT8 PchHdaVerbTableEntryNum**

Offset 0x008C - PCH HDA Verb Table Entry Number Number of

in Verb Table.

**UINT32 [PchHdaVerbTablePtr](#)**

Offset 0x008D - PCH HDA Verb Table Pointer Pointer to Array pointers to Verb Table.

**UINT8 [PchHdaCodecSxWakeCapability](#)**

Offset 0x0091 - PCH HDA Codec Sx Wake Capability Capability detect wake initiated by a codec in Sx.

**UINT8 [SataEnable](#)**

Offset 0x0092 - Enable SATA Enable/disable SATA controller. [More...](#)

**UINT8 [SataMode](#)**

Offset 0x0093 - SATA Mode Select SATA controller working mode. [More...](#)

**UINT8 [Usb2AfePetxiset](#) [16]**

Offset 0x0094 - USB Per Port HS Preemphasis Bias USB Per Port Preemphasis Bias. [More...](#)

**UINT8 [Usb2AfeTxiset](#) [16]**

Offset 0x00A4 - USB Per Port HS Transmitter Bias USB Per Port Transmitter Bias. [More...](#)

**UINT8 [Usb2AfePredeemp](#) [16]**

Offset 0x00B4 - USB Per Port HS Transmitter Emphasis USB Per Port Transmitter Emphasis. [More...](#)

**UINT8 [Usb2AfePehalfbit](#) [16]**

Offset 0x00C4 - USB Per Port Half Bit Pre-emphasis USB Per Port Bit Pre-emphasis. [More...](#)

**UINT8 [Usb3HsioTxDeEmphEnable](#) [10]**

Offset 0x00D4 - Enable the write to USB 3.0 TX Output -3.5dB Emphasis Adjustment Enable the write to USB 3.0 TX Output De-Emphasis Adjustment. [More...](#)

**UINT8 [Usb3HsioTxDeEmph](#) [10]**

Offset 0x00DE - USB 3.0 TX Output -3.5dB De-Emphasis Adj  
Setting USB 3.0 TX Output -3.5dB De-Emphasis Adjustment \$  
HSIO\_TX\_DWORD5[21:16], **Default = 29h** (approximately -3.  
Emphasis). [More...](#)

**UINT8 [Usb3HsioTxDownscaleAmpEnable](#) [10]**

Offset 0x00E8 - Enable the write to USB 3.0 TX Output Downscale Amplitude Adjustment  
Enable the write to USB 3.0 TX Output Downscale Amplitude Adjustment, Each value in array can be 0-1. [More...](#)

**UINT8 [Usb3HsioTxDownscaleAmp](#) [10]**

Offset 0x00F2 - USB 3.0 TX Output Downscale Amplitude Adjustment  
USB 3.0 TX Output Downscale Amplitude Adjustment,  
HSIO\_TX\_DWORD8[21:16], **Default = 00h**. [More...](#)

**UINT8 [PchLanEnable](#)**

Offset 0x00FC - Enable LAN Enable/disable LAN controller. [M](#)

**UINT8 [PchHdaAudioLinkHda](#)**

Offset 0x00FD - Enable HD Audio Link Enable/disable HD Audio Link  
[More...](#)

**UINT8 [PchHdaAudioLinkDmic0](#)**

Offset 0x00FE - Enable HD Audio DMIC0 Link Enable/disable  
DMIC0 link. [More...](#)

**UINT8 [PchHdaAudioLinkDmic1](#)**

Offset 0x00FF - Enable HD Audio DMIC1 Link Enable/disable  
DMIC1 link. [More...](#)

**UINT8 [PchHdaAudioLinkSsp0](#)**

Offset 0x0100 - Enable HD Audio SSP0 Link Enable/disable HD Audio SSP0/I2S link. [More...](#)

- UINT8 [PchHdaAudioLinkSsp1](#)**  
Offset 0x0101 - Enable HD Audio SSP1 Link Enable/disable HD Audio SSP1/I2S link. [More...](#)
- UINT8 [PchHdaAudioLinkSsp2](#)**  
Offset 0x0102 - Enable HD Audio SSP2 Link Enable/disable HD Audio SSP2/I2S link. [More...](#)
- UINT8 [PchHdaAudioLinkSndw1](#)**  
Offset 0x0103 - Enable HD Audio SoundWire#1 Link Enable/disable HD Audio SNDW1 link. [More...](#)
- UINT8 [PchHdaAudioLinkSndw2](#)**  
Offset 0x0104 - Enable HD Audio SoundWire#2 Link Enable/disable HD Audio SNDW2 link. [More...](#)
- UINT8 [PchHdaAudioLinkSndw3](#)**  
Offset 0x0105 - Enable HD Audio SoundWire#3 Link Enable/disable HD Audio SNDW3 link. [More...](#)
- UINT8 [PchHdaAudioLinkSndw4](#)**  
Offset 0x0106 - Enable HD Audio SoundWire#4 Link Enable/disable HD Audio SNDW4 link. [More...](#)
- UINT8 [PchHdaSndwBufferRcomp](#)**  
Offset 0x0107 - Soundwire Clock Buffer GPIO RCOMP Setting  
0: ACT - 50 Ohm driver impedance, 1: ACT - 8 Ohm driver impedance  
[More...](#)
- UINT32 [PcieRpPtmMask](#)**  
Offset 0x0108 - PTM for PCIE RP Mask Enable/disable Precise Measurement for PCIE Root Ports. [More...](#)
- UINT32 [PcieRpDpcMask](#)**  
Offset 0x010C - DPC for PCIE RP Mask Enable/disable Down Port Containment for PCIE Root Ports. [More...](#)

UINT32	<b>PcieRpDpcExtensionsMask</b> Offset 0x0110 - DPC Extensions PCIE RP Mask Enable/disable Extensions for PCIE Root Ports. <a href="#">More...</a>
UINT8	<b>UsbPdoProgramming</b> Offset 0x0114 - USB PDO Programming Enable/disable PDO programming for USB in PEI phase. <a href="#">More...</a>
UINT32	<b>PmcPowerButtonDebounce</b> Offset 0x0115 - Power button debounce configuration Debounce for PWRBTN in microseconds. <a href="#">More...</a>
UINT8	<b>PchEspiBmeMasterSlaveEnabled</b> Offset 0x0119 - PCH eSPI Master and Slave BME enabled PC Master and Slave BME enabled \$EN_DIS.
UINT8	<b>SataRstLegacyOrom</b> Offset 0x011A - PCH SATA use RST Legacy OROM Use PCH RST Legacy OROM when CSM is Enabled \$EN_DIS.
UINT32	<b>TraceHubMemBase</b> Offset 0x011B - Trace Hub Memory Base If Trace Hub is enabled trace to memory is desired, BootLoader needs to allocate trace memory as reserved and uncacheable, set the base to ensure Hub memory is configured properly.
UINT8	<b>PmcDbgMsgEn</b> Offset 0x011F - PMC Debug Message Enable When Enabled, will send debug messages to trace hub; When Disabled, PMC never send debug messages to trace hub. <a href="#">More...</a>
UINT32	<b>ChipsetInitBinPtr</b> Offset 0x0120 - Pointer of ChipsetInit Binary ChipsetInit Binary
UINT32	<b>ChipsetInitBinLen</b> Offset 0x0124 - Length of ChipsetInit Binary ChipsetInit Binary

- UINT8 **PchPostMemRsvd** [29]  
Offset 0x0128 - PchPostMemRsvd Reserved for PCH Post-Memory Range decode \$EN\_DIS.
- UINT8 **ScsUfsEnabled**  
Offset 0x0145 - Enable Ufs Controller Enable/disable Ufs 2.0 Controller  
More...
- UINT8 **PchCnviMode**  
Offset 0x0146 - CNVi Configuration This option allows for auto detection of Connectivity Solution. More...
- UINT8 **SdCardPowerEnableActiveHigh**  
Offset 0x0147 - SdCard power enable polarity Choose SD\_PV polarity 0: Active low, 1: Active high.
- UINT8 **PchUsb2PhySusPgEnable**  
Offset 0x0148 - PCH USB2 PHY Power Gating enable 1: Will enable USB2 PHY SUS Well Power Gating, 0: Will not enable PG of USB2 PHY Sus Well PG \$EN\_DIS.
- UINT8 **PchUsbOverCurrentEnable**  
Offset 0x0149 - PCH USB OverCurrent mapping enable 1: Will map USB OC pin mapping in xHCI controller memory, 0: Will clear mapping allow for NOA usage of OC pins \$EN\_DIS.
- UINT8 **UnusedUpdSpace3**  
Offset 0x014A.
- UINT8 **PchCnviMfUart1Type**  
Offset 0x014B - CNVi MfUart1 Type This option configures UART which connects to MfUart1 0:ISH Uart0, 1:SerialIO Uart2, 2:User external pads.
- UINT8 **PchEspiLgmrEnable**  
Offset 0x014C - Espi Lgmr Memory Range decode This option enables or disables espi lgmr \$EN\_DIS.

**UINT8 Heci3Enabled**

Offset 0x014D - HECl3 state The HECl3 state from Mbp for re S3 path or when MbpHob is not installed. [More...](#)

**UINT8 UnusedUpdSpace4**

Offset 0x014E.

**UINT8 PchHotEnable**

Offset 0x014F - PCHHOT# pin Enable PCHHOT# pin assertion temperature is higher than PchHotLevel. [More...](#)

**UINT8 SataLedEnable**

Offset 0x0150 - SATA LED SATA LED indicating SATA controller status. [More...](#)

**UINT8 PchPmVrAlert**

Offset 0x0151 - VRAlert# Pin When VRAlert# feature pin is enabled its state is '0', the PMC requests throttling to a T3 Tstate to the throttling unit. [More...](#)

**UINT8 PchPmSlpS0VmRuntimeControl**

Offset 0x0152 - SLP\_S0 VM Dynamic Control SLP\_S0 Voltage Margining Runtime Control Policy. [More...](#)

**UINT8 PchPmSlpS0Vm070VSupport**

Offset 0x0153 - SLP\_S0 VM 0.70V Support SLP\_S0 Voltage Margining 0.70V Support Policy. [More...](#)

**UINT8 PchPmSlpS0Vm075VSupport**

Offset 0x0154 - SLP\_S0 VM 0.75V Support SLP\_S0 Voltage Margining 0.75V Support Policy. [More...](#)

**UINT8 AmtEnabled**

Offset 0x0155 - AMT Switch Enable/Disable. [More...](#)

**UINT8 WatchDog**

Offset 0x0156 - WatchDog Timer Switch Enable/Disable. More...

UINT8 **AsfEnabled**

Offset 0x0157 - ASF Switch Enable/Disable. More...

UINT8 **ManageabilityMode**

Offset 0x0158 - Manageability Mode set by Mebx Enable/Disable. More...

UINT8 **FwProgress**

Offset 0x0159 - PET Progress Enable/Disable. More...

UINT8 **AmtSolEnabled**

Offset 0x015A - SOL Switch Enable/Disable. More...

UINT16 **WatchDogTimerOs**

Offset 0x015B - OS Timer 16 bits Value, Set OS watchdog tim

UINT16 **WatchDogTimerBios**

Offset 0x015D - BIOS Timer 16 bits Value, Set BIOS watchdog tim  
More...

UINT8 **RemoteAssistance**

Offset 0x015F - Remote Assistance Trigger Availability Enable  
More...

UINT8 **AmtKvmEnabled**

Offset 0x0160 - KVM Switch Enable/Disable. More...

UINT8 **ForcMebxSyncUp**

Offset 0x0161 - MEBX execution Enable/Disable. More...

UINT8 **UnusedUpdSpace5 [1]**

Offset 0x0162.

UINT8 **PcieRpSlotImplemented [24]**

Offset 0x0163 - PCH PCIe root port connection type 0: built-in 1:slot.

**UINT8 [PcieClkSrcUsage](#) [16]**

Offset 0x017B - Usage type for ClkSrc 0-23: PCH rootport, 0x0: PEG port, 0x70:LAN, 0x80: unspecified but in use (free running not used).

**UINT8 [PcieClkSrcClkReq](#) [16]**

Offset 0x018B - ClkReq-to-ClkSrc mapping Number of ClkReq assigned to ClkSrc.

**UINT8 [PcieRpAcsEnabled](#) [24]**

Offset 0x019B - PCIE RP Access Control Services Extended Control Enable/Disable PCIE RP Access Control Services Extended Control

**UINT8 [PcieRpEnableCpm](#) [24]**

Offset 0x01B3 - PCIE RP Clock Power Management Enable/Disable PCIE RP Clock Power Management, even if disabled, CLKRE can still be controlled by L1 PM substates mechanism.

**UINT16 [PcieRpDetectTimeoutMs](#) [24]**

Offset 0x01CB - PCIE RP Detect Timeout Ms The number of milliseconds within 0~65535 in reference code will wait for link Detect state for enabled ports before assuming there is no device present potentially disabling the port.

**UINT8 [PmcModPhySusPgEnable](#)**

Offset 0x01FB - ModPHY SUS Power Domain Dynamic Gating Enable/Disable ModPHY SUS Power Domain Dynamic Gating

**UINT8 [SlpS0WithGbeSupport](#)**

Offset 0x01FC - SlpS0WithGbeSupport Enable/Disable SLP\_S GBE Support. [More...](#)

**UINT8 [UnusedUpdSpace6](#) [3]**

Offset 0x01FD.

**UINT8 CridEnable**

Offset 0x0200 - Enable/Disable SA CRID Enable: SA CRID, D  
(Default): SA CRID \$EN\_DIS.

**UINT8 DmiAspm**

Offset 0x0201 - DMI ASPM 0=Disable, 1:L0s, 2:L1, 3(Default):  
0:Disable, 1:L0s, 2:L1, 3:L0sL1.

**UINT8 PegDeEmphasis [4]**

Offset 0x0202 - PCIe DeEmphasis control per root port 0: -6dB  
1(Default): -3.5dB 0:-6dB, 1:-3.5dB.

**UINT8 PegSlotPowerLimitValue [4]**

Offset 0x0206 - PCIe Slot Power Limit value per root port Slot  
limit value per root port.

**UINT8 PegSlotPowerLimitScale [4]**

Offset 0x020A - PCIe Slot Power Limit scale per root port Slot  
limit scale per root port 0:1.0x, 1:0.1x, 2:0.01x, 3:0x001x.

**UINT16 PegPhysicalSlotNumber [4]**

Offset 0x020E - PCIe Physical Slot Number per root port Phys  
Number per root port.

**UINT8 PavpEnable**

Offset 0x0216 - Enable/Disable PavpEnable Enable(Default): 1:  
PavpEnable, Disable: Disable PavpEnable \$EN\_DIS.

**UINT8 CdClock**

Offset 0x0217 - CdClock Frequency selection 0=337.5 Mhz, 1:  
2=540 Mhz, 3(Default)=675 Mhz 0: 337.5 Mhz, 1: 450 Mhz, 2:  
3: 675 Mhz.

**UINT8 PeiGraphicsPeimInit**

Offset 0x0218 - Enable/Disable PeiGraphicsPeimInit Enable: E  
PeiGraphicsPeimInit, Disable(Default): Disable PeiGraphicsPe

\$EN\_DIS.

UINT8 **UnusedUpdSpace7**

Offset 0x0219.

UINT8 **GnaEnable**

Offset 0x021A - Enable or disable GNA device 0=Disable, 1(Default)=Enable \$EN\_DIS.

UINT8 **X2ApicOptOut**

Offset 0x021B - State of X2APIC\_OPT\_OUT bit in the DMAR 0=Disable/Clear, 1=Enable/Set \$EN\_DIS.

UINT32 **VtdBaseAddress [3]**

Offset 0x021C - Base addresses for VT-d function MMIO access addresses for VT-d MMIO access per VT-d engine.

UINT8 **DdiPortEdp**

Offset 0x0228 - Enable or disable eDP device 0=Disable, 1(Default)=Enable \$EN\_DIS.

UINT8 **DdiPortBHpd**

Offset 0x0229 - Enable or disable HPD of DDI port B 0=Disable, 1(Default)=Enable \$EN\_DIS.

UINT8 **DdiPortCHpd**

Offset 0x022A - Enable or disable HPD of DDI port C 0=Disable, 1(Default)=Enable \$EN\_DIS.

UINT8 **DdiPortDHpd**

Offset 0x022B - Enable or disable HPD of DDI port D 0=Disable, 1(Default)=Enable \$EN\_DIS.

UINT8 **DdiPortFHpD**

Offset 0x022C - Enable or disable HPD of DDI port F 0=Disable, 1(Default)=Enable \$EN\_DIS.

**UINT8 DdiPortBDdc**  
Offset 0x022D - Enable or disable DDC of DDI port B 0=Disable 1(Default)=Enable \$EN\_DIS.

**UINT8 DdiPortCDdc**  
Offset 0x022E - Enable or disable DDC of DDI port C 0=Disable 1(Default)=Enable \$EN\_DIS.

**UINT8 DdiPortDDdc**  
Offset 0x022F - Enable or disable DDC of DDI port D 0=Disable 1(Default)=Enable \$EN\_DIS.

**UINT8 DdiPortFDdc**  
Offset 0x0230 - Enable or disable DDC of DDI port F  
0(Default)=Disable, 1=Enable \$EN\_DIS.

**UINT8 SkipS3CdClockInit**  
Offset 0x0231 - Enable/Disable SkipS3CdClockInit  
Enable: Skip clock initializaton, Disable(Default): Initialize the full CD clock in resume due to GOP absent \$EN\_DIS.

**UINT16 DeltaT12PowerCycleDelay**  
Offset 0x0232 - Delta T12 Power Cycle Delay required in ms  
\$S value for delay required. [More...](#)

**UINT32 BltBufferAddress**  
Offset 0x0234 - Blt Buffer Address Address of Blt buffer.

**UINT32 BltBufferSize**  
Offset 0x0238 - Blt Buffer Size Size of Blt Buffer, is equal to PixelHeight \* 4 bytes (the size of EFI\_GRAPHICS\_OUTPUT\_BLT\_PIXEL)

**UINT8 SaPostMemProductionRsvd [35]**  
Offset 0x023C - SaPostMemProductionRsvd Reserved for SA Mem Production \$EN\_DIS.

**UINT8 PcieRootPortGen2Pll1CgDisable [24]**

Offset 0x025F - PCIE RP Disable Gen2PLL Shutdown and L1 Gating Enable PCIE RP Disable Gen2PLL Shutdown and L1 C Gating Enable Workaround needed for Alpine ridge.

**UINT8 AesEnable**

Offset 0x0277 - Advanced Encryption Standard (AES) feature Disable Advanced Encryption Standard (AES) feature; 0: Disable \$EN\_DIS.

**UINT8 Psi3Enable [5]**

Offset 0x0278 - Power State 3 enable/disable PCODE MMIO Power State 3 enable/disable; 0: Disable; **1: Enable.** [More...](#)

**UINT8 Psi4Enable [5]**

Offset 0x027D - Power State 4 enable/disable PCODE MMIO Power State 4 enable/disable; 0: Disable; **1: Enable.** For all VF

**UINT8 ImonSlope [5]**

Offset 0x0282 - Imon slope correction PCODE MMIO Mailbox: slope correction. [More...](#)

**UINT8 ImonOffset [5]**

Offset 0x0287 - Imon offset correction PCODE MMIO Mailbox: offset correction. [More...](#)

**UINT8 VrConfigEnable [5]**

Offset 0x028C - Enable/Disable BIOS configuration of VR Enable/Disable BIOS configuration of VR; **0: Disable;** **1: Enable.** VR Indexes.

**UINT8 TdcEnable [5]**

Offset 0x0291 - Thermal Design Current enable/disable PCOD Mailbox: Thermal Design Current enable/disable; **0: Disable;** **1: Enable.** For all VR Indexes.

**UINT8 TdcTimeWindow [5]**

Offset 0x0296 - HECI3 state PCODE MMIO Mailbox: Thermal Current time window. [More...](#)

UINT8 **TdcLock [5]**

Offset 0x029B - Thermal Design Current Lock PCODE MMIO Thermal Design Current Lock; 0: **Disable**; 1: Enable. For all VF

UINT8 **PsysSlope**

Offset 0x02A0 - Platform Psys slope correction PCODE MMIC Platform Psys slope correction. [More...](#)

UINT8 **PsysOffset**

Offset 0x02A1 - Platform Psys offset correction PCODE MMIC Platform Psys offset correction. [More...](#)

UINT8 **AcousticNoiseMitigation**

Offset 0x02A2 - Acoustic Noise Mitigation feature Enable or Disable Acoustic Noise Mitigation feature. [More...](#)

UINT8 **FastPkgCRampDisableIa**

Offset 0x02A3 - Disable Fast Slew Rate for Deep Package C S VR IA domain Disable Fast Slew Rate for Deep Package C St based on Acoustic Noise Mitigation feature enabled. [More...](#)

UINT8 **SlowSlewRateForIa**

Offset 0x02A4 - Slew Rate configuration for Deep Package C VR IA domain Slew Rate configuration for Deep Package C St VR IA domain based on Acoustic Noise Mitigation feature enabled. [More...](#)

UINT8 **SlowSlewRateForGt**

Offset 0x02A5 - Slew Rate configuration for Deep Package C VR GT domain Slew Rate configuration for Deep Package C St VR GT domain based on Acoustic Noise Mitigation feature enabled. [More...](#)

UINT8 **SlowSlewRateForSa**

Offset 0x02A6 - Slew Rate configuration for Deep Package C VR SA domain Slew Rate configuration for Deep Package C S VR SA domain based on Acoustic Noise Mitigation feature enable  
[More...](#)

**UINT16 [TdcPowerLimit](#) [5]**

Offset 0x02A7 - Thermal Design Current current limit PCODE MMIO Mailbox: Thermal Design Current current limit. [More...](#)

**UINT16 [AcLoadline](#) [5]**

Offset 0x02B1 - AcLoadline PCODE MMIO Mailbox: AcLoadline current limit in 1/100 mOhms (ie. [More...](#))

**UINT8 [UnusedUpdSpace8](#) [10]**

Offset 0x02BB.

**UINT16 [DcLoadline](#) [5]**

Offset 0x02C5 - DcLoadline PCODE MMIO Mailbox: DcLoadline current limit in 1/100 mOhms (ie. [More...](#))

**UINT16 [Psi1Threshold](#) [5]**

Offset 0x02CF - Power State 1 Threshold current PCODE MMIO Mailbox: Power State 1 current cutoff in 1/4 Amp increments. [More...](#)

**UINT16 [Psi2Threshold](#) [5]**

Offset 0x02D9 - Power State 2 Threshold current PCODE MMIO Mailbox: Power State 2 current cutoff in 1/4 Amp increments. [More...](#)

**UINT16 [Psi3Threshold](#) [5]**

Offset 0x02E3 - Power State 3 Threshold current PCODE MMIO Mailbox: Power State 3 current cutoff in 1/4 Amp increments. [More...](#)

**UINT16 [IccMax](#) [5]**

Offset 0x02ED - Icc Max limit PCODE MMIO Mailbox: VR Icc limit. [More...](#)

**UINT16 [VrVoltageLimit](#) [5]**

Offset 0x02F7 - VR Voltage Limit PCODE MMIO Mailbox: VR Limit. [More...](#)

**UINT8 [FastPkgCRampDisableGt](#)**

Offset 0x0301 - Disable Fast Slew Rate for Deep Package C S VR GT domain Disable Fast Slew Rate for Deep Package C S based on Acoustic Noise Mitigation feature enabled. [More...](#)

**UINT8 [FastPkgCRampDisableSa](#)**

Offset 0x0302 - Disable Fast Slew Rate for Deep Package C S VR SA domain Disable Fast Slew Rate for Deep Package C S based on Acoustic Noise Mitigation feature enabled. [More...](#)

**UINT8 [SendVrMbxCmd](#)**

Offset 0x0303 - Enable VR specific mailbox command VR spe mailbox commands. [More...](#)

**UINT8 [Reserved2](#)**

Offset 0x0304 - Reserved Reserved.

**UINT8 [TxtEnable](#)**

Offset 0x0305 - Enable or Disable TXT Enable or Disable TXT Disable; **1: Enable**. [More...](#)

**UINT8 [UnusedUpdSpace9 \[6\]](#)**

Offset 0x0306.

**UINT8 [SkipMpInit](#)**

Offset 0x030C - Deprecated DO NOT USE Skip Multi-Process Initialization. [More...](#)

**UINT8 [McivrRfiFrequencyPrefix](#)**

Offset 0x030D - McIVR RFI Frequency Prefix PCODE MMIO M McIVR RFI Frequency Adjustment Prefix. [More...](#)

**UINT8 [McivrRfiFrequencyAdjust](#)**

Offset 0x030E - McIVR RFI Frequency Adjustment PCODE M

Mailbox: Adjust the RFI frequency relative to the nominal frequency in increments of 100KHz. [More...](#)

**UINT16 [FivrRfiFrequency](#)**

Offset 0x030F - FIVR RFI Frequency PCODE MMIO Mailbox: desired RFI frequency, in increments of 100KHz. [More...](#)

**UINT8 [McivrSpreadSpectrum](#)**

Offset 0x0311 - McIVR RFI Spread Spectrum PCODE MMIO Mailbox: McIVR RFI Spread Spectrum. [More...](#)

**UINT8 [FivrSpreadSpectrum](#)**

Offset 0x0312 - FIVR RFI Spread Spectrum PCODE MMIO Mailbox: FIVR RFI Spread Spectrum, in 0.1% increments. [More...](#)

**UINT8 [FastPkgCRampDisableFivr](#)**

Offset 0x0313 - Disable Fast Slew Rate for Deep Package C S VR FIVR domain Disable Fast Slew Rate for Deep Package C based on Acoustic Noise Mitigation feature enabled. [More...](#)

**UINT8 [SlowSlewRateForFivr](#)**

Offset 0x0314 - Slew Rate configuration for Deep Package C S VR FIVR domain Slew Rate configuration for Deep Package C for VR FIVR domain based on Acoustic Noise Mitigation feature enabled. [More...](#)

**UINT32 [CpuBistData](#)**

Offset 0x0315 - CpuBistData Pointer CPU BIST Data.

**UINT8 [IsIVrCmd](#)**

Offset 0x0319 - Activates VR mailbox command for Intersil VR issues. [More...](#)

**UINT16 [ImonSlope1](#) [5]**

Offset 0x031A - Imon slope1 correction PCODE MMIO Mailbox: slope correction. [More...](#)

**UINT32 VrPowerDeliveryDesign**

Offset 0x0324 - CPU VR Power Delivery Design Used to com  
the power delivery design capability of the board. [More...](#)

**UINT8 PreWake**

Offset 0x0328 - Pre Wake Randomization time PCODE MMIO  
Acoustic Mitigation Range.Defines the maximum pre-wake  
randomization time in micro ticks.This can be programmed on  
AcousticNoiseMitigation is enabled. [More...](#)

**UINT8 RampUp**

Offset 0x0329 - Ramp Up Randomization time PCODE MMIO  
Acoustic Mitigation Range.Defines the maximum Ramp Up  
randomization time in micro ticks.This can be programmed on  
AcousticNoiseMitigation is enabled.Range 0-255 0.

**UINT8 RampDown**

Offset 0x032A - Ramp Down Randomization time PCODE MM  
Mailbox: Acoustic Mitigation Range.Defines the maximum Ra  
randomization time in micro ticks.This can be programmed on  
AcousticNoiseMitigation is enabled.Range 0-255 0.

**UINT32 CpuMpPpi**

Offset 0x032B - CpuMpPpi Pointer for CpuMpPpi.

**UINT32 CpuMpHob**

Offset 0x032F - CpuMpHob Pointer for CpuMpHob. [More...](#)

**UINT8 DebugInterfaceEnable**

Offset 0x0333 - Enable or Disable processor debug features E  
Disable processor debug features; 0: **Disable**; 1: Enable. [More...](#)

**UINT8 ReservedCpuPostMemProduction [18]**

Offset 0x0334 - ReservedCpuPostMemProduction Reserved f  
Post-Mem Production \$EN\_DIS.

**UINT8 PchDmiAspm**

Offset 0x0346 - Enable DMI ASPM Deprecated. [More...](#)

**UINT8 PchPwrOptEnable**

Offset 0x0347 - Enable Power Optimizer Enable DMI Power C on PCH side. [More...](#)

**UINT8 PchWriteProtectionEnable [5]**

Offset 0x0348 - PCH Flash Protection Ranges Write Enble Wr erase is blocked by hardware.

**UINT8 PchReadProtectionEnable [5]**

Offset 0x034D - PCH Flash Protection Ranges Read Enble Re blocked by hardware.

**UINT16 PchProtectedRangeLimit [5]**

Offset 0x0352 - PCH Protect Range Limit Left shifted address with address bits 11:0 are assumed to be FFFh for limit compa

**UINT16 PchProtectedRangeBase [5]**

Offset 0x035C - PCH Protect Range Base Left shifted address bits with address bits 11:0 are assumed to be 0.

**UINT8 PchHdaPme**

Offset 0x0366 - Enable Pme Enable Azalia wake-on-ring. [More...](#)

**UINT8 UnusedUpdSpace10**

Offset 0x0367.

**UINT8 PchHdaVcType**

Offset 0x0368 - VC Type Virtual Channel Type Select: 0: VC0, [More...](#)

**UINT8 PchHdaLinkFrequency**

Offset 0x0369 - HD Audio Link Frequency HDA Link Freq (PCH\_HDAUDIO\_LINK\_FREQUENCY enum): 0: 6MHz, 1: 12 24MHz. [More...](#)

- UINT8 PchHdaIDispLinkFrequency**  
Offset 0x036A - iDisp-Link Frequency iDisp-Link Freq  
(PCH\_HDAUDIO\_LINK\_FREQUENCY enum): 4: 96MHz, 3: 4  
[More...](#)
- UINT8 PchHdaIDispLinkTmode**  
Offset 0x036B - iDisp-Link T-mode iDisp-Link T-Mode  
(PCH\_HDAUDIO\_IDISP\_TMODE enum): 0: 2T, 1: 1T. [More...](#)
- UINT8 PchHdaDspUaaCompliance**  
Offset 0x036C - Universal Audio Architecture compliance for D enabled system 0: Not-UAA Compliant (Intel SST driver supported), 1: UAA Compliant (HDA Inbox driver or SST driver supported).
- UINT8 PchHdaIDispCodecDisconnect**  
Offset 0x036D - iDisplay Audio Codec disconnection 0: Not disconnected, enumerable, 1: Disconnected SDI, not enumerable  
[More...](#)
- UINT8 PchUsbHsioFilterSel [10]**  
Offset 0x036E - USB LFPS Filter selection For each byte bits 0:p, bits 4:6 are for n. [More...](#)
- UINT8 UnusedUpdSpace11 [5]**  
Offset 0x0378.
- UINT8 PchIoApicEntry24\_119**  
Offset 0x037D - Enable PCH Io Apic Entry 24-119 0: Disable; 1: Enable  
[More...](#)
- UINT8 PchIoApicId**  
Offset 0x037E - PCH Io Apic ID This member determines IOAPIC ID  
[More...](#)
- UINT8 UnusedUpdSpace12**  
Offset 0x037F.

**UINT8 PchIshSpiGpioAssign**

Offset 0x0380 - Enable PCH ISH SPI GPIO pins assigned 0: Disable; 1: Enable. [More...](#)

**UINT8 PchIshUart0GpioAssign**

Offset 0x0381 - Enable PCH ISH UART0 GPIO pins assigned 0: Disable; 1: Enable. [More...](#)

**UINT8 PchIshUart1GpioAssign**

Offset 0x0382 - Enable PCH ISH UART1 GPIO pins assigned 0: Disable; 1: Enable. [More...](#)

**UINT8 PchIshI2c0GpioAssign**

Offset 0x0383 - Enable PCH ISH I2C0 GPIO pins assigned 0: 1: Enable. [More...](#)

**UINT8 PchIshI2c1GpioAssign**

Offset 0x0384 - Enable PCH ISH I2C1 GPIO pins assigned 0: 1: Enable. [More...](#)

**UINT8 PchIshI2c2GpioAssign**

Offset 0x0385 - Enable PCH ISH I2C2 GPIO pins assigned 0: 1: Enable. [More...](#)

**UINT8 PchIshGp0GpioAssign**

Offset 0x0386 - Enable PCH ISH GP\_0 GPIO pin assigned 0: 1: Enable. [More...](#)

**UINT8 PchIshGp1GpioAssign**

Offset 0x0387 - Enable PCH ISH GP\_1 GPIO pin assigned 0: 1: Enable. [More...](#)

**UINT8 PchIshGp2GpioAssign**

Offset 0x0388 - Enable PCH ISH GP\_2 GPIO pin assigned 0: 1: Enable. [More...](#)

**UINT8 PchIshGp3GpioAssign**

Offset 0x0389 - Enable PCH ISH GP\_3 GPIO pin assigned 0:  
1: Enable. [More...](#)

UINT8 **PchIshGp4GpioAssign**

Offset 0x038A - Enable PCH ISH GP\_4 GPIO pin assigned 0:  
1: Enable. [More...](#)

UINT8 **PchIshGp5GpioAssign**

Offset 0x038B - Enable PCH ISH GP\_5 GPIO pin assigned 0:  
1: Enable. [More...](#)

UINT8 **PchIshGp6GpioAssign**

Offset 0x038C - Enable PCH ISH GP\_6 GPIO pin assigned 0:  
1: Enable. [More...](#)

UINT8 **PchIshGp7GpioAssign**

Offset 0x038D - Enable PCH ISH GP\_7 GPIO pin assigned 0:  
1: Enable. [More...](#)

UINT8 **PchIshPdtUnlock**

Offset 0x038E - PCH ISH PDT Unlock Msg 0: False; 1: True. [M](#)

UINT8 **PchLanLtrEnable**

Offset 0x038F - Enable PCH Lan LTR capability of PCH internal  
Disable; 1: Enable. [More...](#)

UINT8 **UnusedUpdSpace13 [3]**

Offset 0x0390.

UINT8 **PchLockDownBiosLock**

Offset 0x0393 - Enable LOCKDOWN BIOS LOCK Enable the  
Lock feature and set EISS bit (D31:F5:RegDCh[5]) for the BIO  
protection. [More...](#)

UINT8 **PchCrid**

Offset 0x0394 - PCH Compatibility Revision ID This member controls  
whether or not the CRID feature of PCH should be enabled. [M](#)

- UINT8 [PchLockDownRtcMemoryLock](#)**  
Offset 0x0395 - RTC CMOS MEMORY LOCK Enable RTC low upper 128 byte Lock bits to lock Bytes 38h-3Fh in the upper and lower 128-byte bank of RTC RAM. [More...](#)
- UINT8 [PcieRpHotPlug](#) [24]**  
Offset 0x0396 - Enable PCIE RP HotPlug Indicate whether the hot plug available.
- UINT8 [PcieRpPmSci](#) [24]**  
Offset 0x03AE - Enable PCIE RP Pm Sci Indicate whether the power manager SCI is enabled.
- UINT8 [PcieRpExtSync](#) [24]**  
Offset 0x03C6 - Enable PCIE RP Ext Sync Indicate whether the extended synch is enabled.
- UINT8 [PcieRpTransmitterHalfSwing](#) [24]**  
Offset 0x03DE - Enable PCIE RP Transmitter Half Swing Indicate whether the Transmitter Half Swing is enabled.
- UINT8 [PcieRpClkReqDetect](#) [24]**  
Offset 0x03F6 - Enable PCIE RP Clk Req Detect Probe CLKREQ# signal before enabling CLKREQ# based power management.
- UINT8 [PcieRpAdvancedErrorReporting](#) [24]**  
Offset 0x040E - PCIE RP Advanced Error Report Indicate whether Advanced Error Reporting is enabled.
- UINT8 [PcieRpUnsupportedRequestReport](#) [24]**  
Offset 0x0426 - PCIE RP Unsupported Request Report Indicate whether the Unsupported Request Report is enabled.
- UINT8 [PcieRpFatalErrorReport](#) [24]**  
Offset 0x043E - PCIE RP Fatal Error Report Indicate whether Error Report is enabled.

UINT8 **PcieRpNoFatalErrorReport** [24]  
Offset 0x0456 - PCIE RP No Fatal Error Report Indicate whether Fatal Error Report is enabled.

UINT8 **PcieRpCorrectableErrorReport** [24]  
Offset 0x046E - PCIE RP Correctable Error Report Indicate whether Correctable Error Report is enabled.

UINT8 **PcieRpSystemErrorOnFatalError** [24]  
Offset 0x0486 - PCIE RP System Error On Fatal Error Indicate whether the System Error on Fatal Error is enabled.

UINT8 **PcieRpSystemErrorOnNonFatalError** [24]  
Offset 0x049E - PCIE RP System Error On Non Fatal Error Indicate whether the System Error on Non Fatal Error is enabled.

UINT8 **PcieRpSystemErrorOnCorrectableError** [24]  
Offset 0x04B6 - PCIE RP System Error On Correctable Error Indicate whether the System Error on Correctable Error is enabled.

UINT8 **PcieRpMaxPayload** [24]  
Offset 0x04CE - PCIE RP Max Payload Max Payload Size supported Default 128B, see enum PCH\_PCIE\_MAX\_PAYLOAD.

UINT8 **PchUsbHsioRxTuningParameters** [10]  
Offset 0x04E6 - PCH USB3 RX HSIO Tuning parameters Bits Signed Magnitude number added to the CTLE code, Bits 2:0 controlling the input offset.

UINT8 **PchUsbHsioRxTuningEnable** [10]  
Offset 0x04F0 - PCH USB3 HSIO Rx Tuning Enable Mask for tuning of HSIO Rx signals of USB3 ports. [More...](#)

UINT8 **UnusedUpdSpace14** [4]  
Offset 0x04FA.

**UINT8 PcieRpPcieSpeed [24]**  
Offset 0x04FE - PCIE RP Pcie Speed Determines each PCIE speed capability. [More...](#)

**UINT8 PcieRpGen3EqPh3Method [24]**  
Offset 0x0516 - PCIE RP Gen3 Equalization Phase Method PCIE Eq Ph3 Method (see PCH\_PCIE\_EQ\_METHOD). [More...](#)

**UINT8 PcieRpPhysicalSlotNumber [24]**  
Offset 0x052E - PCIE RP Physical Slot Number Indicates the slot number for the root port. [More...](#)

**UINT8 PcieRpCompletionTimeout [24]**  
Offset 0x0546 - PCIE RP Completion Timeout The root port completion timeout(see: PCH\_PCIE\_COMPLETION\_TIMEOUT). [More...](#)

**UINT8 UnusedUpdSpace15 [106]**  
Offset 0x055E.

**UINT8 PcieRpAspm [24]**  
Offset 0x05C8 - PCIE RP Aspm The ASPM configuration of the root port (see: PCH\_PCIE\_ASPM\_CONTROL). [More...](#)

**UINT8 PcieRpL1Substates [24]**  
Offset 0x05E0 - PCIE RP L1 Substates The L1 Substates control of the root port (see: PCH\_PCIE\_L1SUBSTATES\_CONTROL)

**UINT8 PcieRpLtrEnable [24]**  
Offset 0x05F8 - PCIE RP Ltr Enable Latency Tolerance Reporting Mechanism.

**UINT8 PcieRpLtrConfigLock [24]**  
Offset 0x0610 - PCIE RP Ltr Config Lock 0: Disable; 1: Enable

**UINT8 PcieEqPh3LaneParamCm [24]**  
Offset 0x0628 - PCIE Eq Ph3 Lane Param Cm PCH\_PCIE\_EQ\_LANE\_PARAM. [More...](#)

- UINT8 **PcieEqPh3LaneParamCp** [24]  
Offset 0x0640 - PCIE Eq Ph3 Lane Param Cp  
PCH\_PCIE\_EQ\_LANE\_PARAM. [More...](#)
- UINT8 **PcieSwEqCoeffListCm** [5]  
Offset 0x0658 - PCIE Sw Eq CoeffList Cm PCH\_PCIE\_EQ\_PA  
[More...](#)
- UINT8 **PcieSwEqCoeffListCp** [5]  
Offset 0x065D - PCIE Sw Eq CoeffList Cp PCH\_PCIE\_EQ\_PA  
[More...](#)
- UINT8 **PcieDisableRootPortClockGating**  
Offset 0x0662 - PCIE Disable RootPort Clock Gating Describe  
the PCI Express Clock Gating for each root port is enabled by  
modules. [More...](#)
- UINT8 **PcieEnablePeerMemoryWrite**  
Offset 0x0663 - PCIE Enable Peer Memory Write This member  
describes whether Peer Memory Writes are enabled on the pl  
[More...](#)
- UINT8 **UnusedUpdSpace16**  
Offset 0x0664.
- UINT8 **PcieComplianceTestMode**  
Offset 0x0665 - PCIE Compliance Test Mode Compliance Test  
shall be enabled when using Compliance Load Board. [More...](#)
- UINT8 **PcieRpFunctionSwap**  
Offset 0x0666 - PCIE Rp Function Swap Allows BIOS to use re  
function number swapping when root port of function 0 is disabled.  
[More...](#)
- UINT8 **TetonGlacierSupport**  
Offset 0x0667 - Teton Glacier Support Enables support for the

Glacier card. [More...](#)

UINT8 **TetonGlacierCR**

Offset 0x0668 - Teton Glacier Cycle Router Specify to which cycle router Teton Glacier is connected, it is valid only when Teton Glacier is enabled. [More...](#)

UINT8 **PchPmPmeB0S5Dis**

Offset 0x0669 - PCH Pm PME\_B0\_S5\_DIS When cleared (deasserted) wake events from PME\_B0\_STS are allowed in S5 if PME\_B0\_STS is asserted. [More...](#)

UINT8 **SerialloSpiCsPolarity [3]**

Offset 0x066A - SPI ChipSelect signal polarity Selects SPI ChipSelect signal polarity.

UINT8 **PcieRpImrEnabled**

Offset 0x066D - PCIE IMR Enables Isolated Memory Region feature. [More...](#)

UINT8 **PcieRpImrSelection**

Offset 0x066E - PCIE IMR port number Selects PCIE root port number for IMR feature.

UINT8 **UnusedUpdSpace17**

Offset 0x066F.

UINT8 **PchPmWolEnableOverride**

Offset 0x0670 - PCH Pm WOL Enable Override Corresponds to the Enable Override bit in the General PM Configuration B (GEN\_PMCON\_B) register. [More...](#)

UINT8 **PchPmPcieWakeFromDeepSx**

Offset 0x0671 - PCH Pm Pcie Wake From DeepSx Determine which PCIe to wake from deep Sx. [More...](#)

UINT8 **PchPmWoWlanEnable**

Offset 0x0672 - PCH Pm WoW Ian Enable Determine if WLAN from Sx, corresponds to the HOST\_WLAN\_PP\_EN bit in the PWRM\_CFG3 register. [More...](#)

UINT8 **PchPmWoWlanDeepSxEnable**

Offset 0x0673 - PCH Pm WoW Ian DeepSx Enable Determine wake from DeepSx, corresponds to the DSX\_WLAN\_PP\_EN bit in PWRM\_CFG3 register. [More...](#)

UINT8 **PchPmLanWakeFromDeepSx**

Offset 0x0674 - PCH Pm Lan Wake From DeepSx Determine LAN to wake from deep Sx. [More...](#)

UINT8 **PchPmDeepSxPol**

Offset 0x0675 - PCH Pm Deep Sx Pol Deep Sx Policy. [More...](#)

UINT8 **PchPmSlpS3MinAssert**

Offset 0x0676 - PCH Pm Slp S3 Min Assert SLP\_S3 Minimum Width Policy. [More...](#)

UINT8 **PchPmSlpS4MinAssert**

Offset 0x0677 - PCH Pm Slp S4 Min Assert SLP\_S4 Minimum Width Policy. [More...](#)

UINT8 **PchPmSlpSusMinAssert**

Offset 0x0678 - PCH Pm Slp Sus Min Assert SLP\_SUS Minimum Assertion Width Policy. [More...](#)

UINT8 **PchPmSlpAMinAssert**

Offset 0x0679 - PCH Pm Slp A Min Assert SLP\_A Minimum Assertion Width Policy. [More...](#)

UINT8 **SlpS0Override**

Offset 0x067A - SLP\_S0# Override Select 'Auto', it will be auto configured according to probe type. [More...](#)

UINT8 **SlpS0DisQForDebug**

Offset 0x067B - S0ix Override Settings Select 'Auto', it will be configured according to probe type. [More...](#)

UINT8 **PchEnableDbcObs**

Offset 0x067C - USB Overcurrent Override for DbC This option overrides USB Over Current enablement state that USB OC will be disabled after enabling this option. [More...](#)

UINT8 **UnusedUpdSpace18 [3]**

Offset 0x067D.

UINT8 **PchPmLpcClockRun**

Offset 0x0680 - PCH Pm Lpc Clock Run This member describes whether or not the LPC ClockRun feature of PCH should be enabled. [More...](#)

UINT8 **PchPmSlpStrchSusUp**

Offset 0x0681 - PCH Pm Slp Strch Sus Up Enable SLP\_X Suspend After SUS Well Power Up. [More...](#)

UINT8 **PchPmSlpLanLowDc**

Offset 0x0682 - PCH Pm Slp Lan Low Dc Enable/Disable SLP\_X Suspend Low on DC Power. [More...](#)

UINT8 **PchPmPwrBtnOverridePeriod**

Offset 0x0683 - PCH Pm Pwr Btn Override Period PCH power override period. [More...](#)

UINT8 **PchPmDisableDsxAcPresentPulldown**

Offset 0x0684 - PCH Pm Disable Dsx Ac Present Pulldown When disable, PCH will internal pull down AC\_PRESENT in deep S3 during G3 exit. [More...](#)

UINT8 **UnusedUpdSpace19**

Offset 0x0685.

UINT8 **PchPmDisableNativePowerButton**

Offset 0x0686 - PCH Pm Disable Native Power Button Power native mode disable. [More...](#)

UINT8 **PchPmSlpS0Enable**

Offset 0x0687 - PCH Pm Slp S0 Enable Indicates whether SLI to be asserted when PCH reaches idle state. [More...](#)

UINT8 **PchPmMeWakeSts**

Offset 0x0688 - PCH Pm ME\_WAKE\_STS Clear the ME\_WAKE bit in the Power and Reset Status (PRSTS) register. [More...](#)

UINT8 **PchPmWolOvrWkSts**

Offset 0x0689 - PCH Pm WOL\_OVR\_WK\_STS Clear the WOL\_OVR\_WK\_STS bit in the Power and Reset Status (PRS) register. [More...](#)

UINT8 **PchPmPwrCycDur**

Offset 0x068A - PCH Pm Reset Power Cycle Duration Could be customized in the unit of second. [More...](#)

UINT8 **PchPmPciePlsSsc**

Offset 0x068B - PCH Pm Pcie PlsSsc Specifies the Pcie PlsSsc Spectrum Percentage. [More...](#)

UINT8 **UnusedUpdSpace20**

Offset 0x068C.

UINT8 **SataPwrOptEnable**

Offset 0x068D - PCH Sata Pwr Opt Enable SATA Power Optimizer PCH side. [More...](#)

UINT8 **EsataSpeedLimit**

Offset 0x068E - PCH Sata eSATA Speed Limit When enabled, configure the PxSCTL.SPD to 2 to limit the eSATA port speed.

UINT8 **SataSpeedLimit**

Offset 0x068F - PCH Sata Speed Limit Indicates the maximum

the SATA controller can support 0h: PchSataSpeedDefault.

**UINT8 [SataPortsHotPlug](#) [8]**

Offset 0x0690 - Enable SATA Port HotPlug Enable SATA Port

**UINT8 [SataPortsInterlockSw](#) [8]**

Offset 0x0698 - Enable SATA Port Interlock Sw Enable SATA F  
Interlock Sw.

**UINT8 [SataPortsExternal](#) [8]**

Offset 0x06A0 - Enable SATA Port External Enable SATA Port

**UINT8 [SataPortsSpinUp](#) [8]**

Offset 0x06A8 - Enable SATA Port SpinUp Enable the COMRE  
initialization Sequence to the device.

**UINT8 [SataPortsSolidStateDrive](#) [8]**

Offset 0x06B0 - Enable SATA Port Solid State Drive 0: HDD; 1

**UINT8 [SataPortsEnableDitoConfig](#) [8]**

Offset 0x06B8 - Enable SATA Port Enable Dito Config Enable  
Idle Timeout settings (DmVal, DitoVal).

**UINT8 [SataPortsDmVal](#) [8]**

Offset 0x06C0 - Enable SATA Port DmVal DITO multiplier. More...

**UINT16 [SataPortsDitoVal](#) [8]**

Offset 0x06C8 - Enable SATA Port DmVal DEVSLP Idle Timeout  
Default is 625.

**UINT8 [SataPortsZpOdd](#) [8]**

Offset 0x06D8 - Enable SATA Port ZpOdd Support zero power

**UINT8 [SataRstRaidDeviceId](#)**

Offset 0x06E0 - PCH Sata Rst Raid Device Id Enable RAID AI  
ID. More...

**UINT8 [SataRstRaid0](#)**

Offset 0x06E1 - PCH SATA RST RAID0. [More...](#)

**UINT8 [SataRstRaid1](#)**

Offset 0x06E2 - PCH SATA RST RAID1. [More...](#)

**UINT8 [SataRstRaid10](#)**

Offset 0x06E3 - PCH SATA RST RAID10. [More...](#)

**UINT8 [SataRstRaid5](#)**

Offset 0x06E4 - PCH SATA RST RAID5. [More...](#)

**UINT8 [SataRstIrrt](#)**

Offset 0x06E5 - PCH SATA RST IRRT Intel Rapid Recovery Techn  
[More...](#)

**UINT8 [SataRstOromUiBanner](#)**

Offset 0x06E6 - PCH SATA RST OROM UI Banner OROM UI and  
BANNER. [More...](#)

**UINT8 [SataRstOromUiDelay](#)**

Offset 0x06E7 - PCH SATA RST OROM UI Delay 00b: 2 secs; 01  
10b: 6 secs; 11: 8 secs (see: PCH\_SATA\_OROM\_DELAY).

**UINT8 [SataRstHddUnlock](#)**

Offset 0x06E8 - PCH SATA RST HDD Unlock Indicates that the F  
password unlock in the OS is enabled. [More...](#)

**UINT8 [SataRstLedLocate](#)**

Offset 0x06E9 - PCH SATA RST LED LOCATE Indicates that the  
LED/SGPIO hardware is attached and ping to locate feature is  
on the OS. [More...](#)

**UINT8 [SataRstIrrtOnly](#)**

Offset 0x06EA - PCH SATA RST IRRT ONLY Allow only IRRT drives  
internal and external ports. [More...](#)

**UINT8 [SataRstSmartStorage](#)**  
Offset 0x06EB - PCH Sata Rst Smart Storage RST Smart Storage Caching Bit. More...

**UINT8 [SataRstPcieEnable](#) [3]**  
Offset 0x06EC - PCH Sata Rst Pcie Storage Remap enable Enable RST for PCIe Storage remapping.

**UINT8 [SataRstPcieStoragePort](#) [3]**  
Offset 0x06EF - PCH Sata Rst Pcie Storage Port Intel RST for Storage remapping - PCIe Port Selection (1-based, 0 = auto/default).

**UINT8 [SataRstPcieDeviceResetDelay](#) [3]**  
Offset 0x06F2 - PCH Sata Rst Pcie Device Reset Delay PCIe Device Reset Delay in milliseconds. More...

**UINT8 [PchScsEmmcHs400TuningRequired](#)**  
Offset 0x06F5 - Enable eMMC HS400 Training Deprecated. More...

**UINT8 [PchScsEmmcHs400DIIDataValid](#)**  
Offset 0x06F6 - Set HS400 Tuning Data Valid Set if HS400 Tuning Data Valid. More...

**UINT8 [PchScsEmmcHs400RxStrobeDII1](#)**  
Offset 0x06F7 - Rx Strobe Delay Control Rx Strobe Delay Control Strobe Delay DLL 1 (HS400 Mode).

**UINT8 [PchScsEmmcHs400TxDataDII](#)**  
Offset 0x06F8 - Tx Data Delay Control Tx Data Delay Control Data Delay (HS400 Mode).

**UINT8 [PchScsEmmcHs400DriverStrength](#)**  
Offset 0x06F9 - I/O Driver Strength Deprecated. More...

**UINT8 [PchSerialloI2cPadsTermination](#) [6]**  
Offset 0x06FA - PCH Seriallo I2C Pads Termination 0x0: Hard

default, 0x1: None, 0x13: 1kOhm weak pull-up, 0x15: 5kOhm weak pull-up, 0x19: 20kOhm weak pull-up - Enable/disable SerialIO I2C0,I2C1,I2C2,I2C3,I2C4,I2C5 pads termination respectively.

UINT8 **UnusedUpdSpace21**  
Offset 0x0700.

UINT8 **SerialIoUart0PinMuxing**  
Offset 0x0701 - PcdSerialIoUart0PinMuxing Select SerialIo Uart0 Pin Muxing. [More...](#)

UINT8 **UnusedUpdSpace22 [1]**  
Offset 0x0702.

UINT8 **SerialIoUartHwFlowCtrl [3]**  
Offset 0x0703 - Enables UART hardware flow control, CTS and RTS lines Enables UART hardware flow control, CTS and RTS lines. [More...](#)

UINT8 **SerialIoDebugUartNumber**  
Offset 0x0706 - UART Number For Debug Purpose UART number for debug purpose. [More...](#)

UINT8 **SerialIoEnableDebugUartAfterPost**  
Offset 0x0707 - Enable Debug UART Controller Enable debug controller after post. [More...](#)

UINT8 **PchSirqEnable**  
Offset 0x0708 - Enable Serial IRQ Determines if enable Serial IRQ. [More...](#)

UINT8 **PchSirqMode**  
Offset 0x0709 - Serial IRQ Mode Select Serial IRQ Mode Selection 0: quiet mode, 1: continuous mode. [More...](#)

UINT8 **PchStartFramePulse**  
Offset 0x070A - Start Frame Pulse Width Start Frame Pulse Width Selection 0: PchSfpw4Clk, 1: PchSfpw6Clk, 2: PchSfpw8Clk. [More...](#)

**UINT8 ReservedForFuture1**

Offset 0x070B - Reserved Reserved \$EN\_DIS.

**UINT8 PchTsmicLock**

Offset 0x070C - Thermal Device SMI Enable This locks down  
Enable on Alert Thermal Sensor Trip. [More...](#)

**UINT16 PchT0Level**

Offset 0x070D - Thermal Throttling Customized T0Level Value  
Customized T0Level value.

**UINT16 PchT1Level**

Offset 0x070F - Thermal Throttling Customized T1Level Value  
Customized T1Level value.

**UINT16 PchT2Level**

Offset 0x0711 - Thermal Throttling Customized T2Level Value  
Customized T2Level value.

**UINT8 PchTTEnable**

Offset 0x0713 - Enable The Thermal Throttle Enable the thermal  
function. [More...](#)

**UINT8 PchTTState13Enable**

Offset 0x0714 - PMSync State 13 When set to 1 and the program  
GPIO pin is a 1, then PMSync state 13 will force at least T2 state.  
[More...](#)

**UINT8 PchTTLock**

Offset 0x0715 - Thermal Throttle Lock Thermal Throttle Lock.

**UINT8 TTsuggestedSetting**

Offset 0x0716 - Thermal Throttling Suggested Setting Thermal  
Throttling Suggested Setting. [More...](#)

**UINT8 TTCrossThrottling**

Offset 0x0717 - Enable PCH Cross Throttling Enable/Disable | Cross Throttling \$EN\_DIS.

UINT8 **PchDmiTsawEn**

Offset 0x0718 - DMI Thermal Sensor Autonomous Width Enable | Thermal Sensor Autonomous Width Enable. [More...](#)

UINT8 **DmiSuggestedSetting**

Offset 0x0719 - DMI Thermal Sensor Suggested Setting DMT sensor suggested representative values. [More...](#)

UINT8 **DmiTS0TW**

Offset 0x071A - Thermal Sensor 0 Target Width DMT thermal sensor suggested representative values. [More...](#)

UINT8 **DmiTS1TW**

Offset 0x071B - Thermal Sensor 1 Target Width Thermal Sensor Target Width. [More...](#)

UINT8 **DmiTS2TW**

Offset 0x071C - Thermal Sensor 2 Target Width Thermal Sensor Target Width. [More...](#)

UINT8 **DmiTS3TW**

Offset 0x071D - Thermal Sensor 3 Target Width Thermal Sensor Target Width. [More...](#)

UINT8 **SataP0T1M**

Offset 0x071E - Port 0 T1 Multiplier Port 0 T1 Multiplier.

UINT8 **SataP0T2M**

Offset 0x071F - Port 0 T2 Multiplier Port 0 T2 Multiplier.

UINT8 **SataP0T3M**

Offset 0x0720 - Port 0 T3 Multiplier Port 0 T3 Multiplier.

UINT8 **SataP0TDisp**

Offset 0x0721 - Port 0 Tdispatch Port 0 Tdispatch.

UINT8 **SataP1T1M**

Offset 0x0722 - Port 1 T1 Multipler Port 1 T1 Multipler.

UINT8 **SataP1T2M**

Offset 0x0723 - Port 1 T2 Multipler Port 1 T2 Multipler.

UINT8 **SataP1T3M**

Offset 0x0724 - Port 1 T3 Multipler Port 1 T3 Multipler.

UINT8 **SataP1TDisp**

Offset 0x0725 - Port 1 Tdispatch Port 1 Tdispatch.

UINT8 **SataP0Tinact**

Offset 0x0726 - Port 0 Tinactive Port 0 Tinactive.

UINT8 **SataP0TDispFinit**

Offset 0x0727 - Port 0 Alternate Fast Init Tdispatch Port 0 Alte Init Tdispatch. [More...](#)

UINT8 **SataP1Tinact**

Offset 0x0728 - Port 1 Tinactive Port 1 Tinactive.

UINT8 **SataP1TDispFinit**

Offset 0x0729 - Port 1 Alternate Fast Init Tdispatch Port 1 Alte Init Tdispatch. [More...](#)

UINT8 **SataThermalSuggestedSetting**

Offset 0x072A - Sata Thermal Throttling Suggested Setting Sa Thermal Throttling Suggested Setting. [More...](#)

UINT8 **PchMemoryThrottlingEnable**

Offset 0x072B - Enable Memory Thermal Throttling Enable Me Thermal Throttling. [More...](#)

**UINT8 PchMemoryPmsyncEnable [2]**  
Offset 0x072C - Memory Thermal Throttling Enable Memory T  
Throttling.

**UINT8 PchMemoryC0TransmitEnable [2]**  
Offset 0x072E - Enable Memory Thermal Throttling Enable Me  
Thermal Throttling.

**UINT8 PchMemoryPinSelection [2]**  
Offset 0x0730 - Enable Memory Thermal Throttling Enable Me  
Thermal Throttling.

**UINT16 PchTemperatureHotLevel**  
Offset 0x0732 - Thermal Device Temperature Decides the tem

**UINT8 PchEnableComplianceMode**  
Offset 0x0734 - Enable xHCI Compliance Mode Compliance M  
be enabled for testing through this option but this is disabled b  
More...

**UINT8 Usb2OverCurrentPin [16]**  
Offset 0x0735 - USB2 Port Over Current Pin Describe the spe  
current pin number of USB 2.0 Port N.

**UINT8 Usb3OverCurrentPin [10]**  
Offset 0x0745 - USB3 Port Over Current Pin Describe the spe  
current pin number of USB 3.0 Port N.

**UINT8 Enable8254ClockGating**  
Offset 0x074F - Enable 8254 Static Clock Gating Set 8254CG  
required for SLP\_S0 support. More...

**UINT8 SataRstOptaneMemory**  
Offset 0x0750 - PCH Sata Rst Optane Memory Optane Memo  
\$EN\_DIS.

**UINT8 SataRstCpuAttachedStorage**

Offset 0x0751 - PCH Sata Rst CPU Attached Storage CPU At Storage \$EN\_DIS.

**UINT8 [Enable8254ClockGatingOnS3](#)**

Offset 0x0752 - Enable 8254 Static Clock Gating On S3 This is applicable when Enable8254ClockGating is disabled. [More...](#)

**UINT8 [UnusedUpdSpace23](#)**

Offset 0x0753.

**UINT32 [PchPcieDeviceOverrideTablePtr](#)**

Offset 0x0754 - Pch PCIE device override table pointer The Pch table is being used to override PCIe device ASPM settings. [More...](#)

**UINT8 [EnableTcoTimer](#)**

Offset 0x0758 - Enable TCO timer. [More...](#)

**UINT64 [BgpdtHash \[4\]](#)**

Offset 0x0759 - BgpdtHash[4] BgpdtHash values.

**UINT32 [BiosGuardAttr](#)**

Offset 0x0779 - BiosGuardAttr BiosGuardAttr default values.

**UINT64 [BiosGuardModulePtr](#)**

Offset 0x077D - BiosGuardModulePtr BiosGuardModulePtr default values.

**UINT64 [SendEcCmd](#)**

Offset 0x0785 - SendEcCmd SendEcCmd function pointer. [More...](#)

**UINT8 [EcCmdProvisionEav](#)**

Offset 0x078D - EcCmdProvisionEav Ephemeral Authorization default values. [More...](#)

**UINT8 [EcCmdLock](#)**

Offset 0x078E - EcCmdLock EcCmdLock default values. [More...](#)

**UINT64 SgxEpoch0**  
Offset 0x078F - SgxEpoch0 SgxEpoch0 default values.

**UINT64 SgxEpoch1**  
Offset 0x0797 - SgxEpoch1 SgxEpoch1 default values.

**UINT8 SgxSinitNvsData**  
Offset 0x079F - SgxSinitNvsData SgxSinitNvsData default values.

**UINT8 SiCsmFlag**  
Offset 0x07A0 - Si Config CSM Flag. More...

**UINT32 SiSsidTablePtr**  
Offset 0x07A1.

**UINT16 SiNumberOfSsidTableEntry**  
Offset 0x07A5.

**UINT8 SataRstInterrupt**  
Offset 0x07A7 - SATA RST Interrupt Mode Allowes to choose which interrupts will be implemented by SATA controller in RAID mode.

**UINT8 MeUnconfigOnRtcClear**  
Offset 0x07A8 - ME Unconfig on RTC clear 0: Disable ME Unconfig on Rtc Clear. More...

**UINT8 PsOnEnable**  
Offset 0x07A9 - Enable PS\_ON. More...

**UINT8 PmcCpuC10GatePinEnable**  
Offset 0x07AA - Pmc Cpu C10 Gate Pin Enable Enable/Disable support for CPU\_C10\_GATE# pin to control gating of CPU Vcc and VccSTG rails instead of SLP\_S0# pin. More...

**UINT8 PchDmiAspmCtrl**  
Offset 0x07AB - Pch Dmi Aspm Ctrl ASPM configuration on the

side of the DMI/OPI Link. More...

---

UINT8 **ReservedFspUpd** [1]

Offset 0x07AC.

---

## Detailed Description

---

Fsp S Configuration.

Definition at line **86** of file [FspSUpd.h](#).

## Member Data Documentation

---

### **UINT16 FSP\_S\_CONFIG::AcLoadline[5]**

---

Offset 0x02B1 - AcLoadline PCODE MMIO Mailbox: AcLoadline in 1/100 mOhms (ie.

1250 = 12.50 mOhm); Range is 0-6249. **Intel Recommended Defaults vary by domain and SKU.**

Definition at line [965](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::AcousticNoiseMitigation**

---

Offset 0x02A2 - Acoustic Noise Mitigation feature Enable or Disable Acoustic Noise Mitigation feature.

This has to be enabled to program slew rate configuration for all VR domains, Pre Wake, Ramp Up and, Ramp Down times.**0: Disabled;**  
**1: Enabled \$EN\_DIS**

Definition at line [925](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::AmtEnabled**

---

Offset 0x0155 - AMT Switch Enable/Disable.

**0: Disable, 1: enable,** Enable or disable AMT functionality. **\$EN\_DIS**

Definition at line [571](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::AmtKvmEnabled**

---

Offset 0x0160 - KVM Switch Enable/Disable.

0: Disable, 1: enable, KVM enable/disable state by Mebx \$EN\_DIS

Definition at line [626](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::AmtSolEnabled**

---

Offset 0x015A - SOL Switch Enable/Disable.

0: Disable, 1: enable, Serial Over Lan enable/disable state by Mebx \$EN\_DIS

Definition at line [602](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::AsfEnabled**

---

Offset 0x0157 - ASF Switch Enable/Disable.

0: Disable, 1: enable, Enable or disable ASF functionality. \$EN\_DIS

Definition at line [583](#) of file [FspUpd.h](#).

### **UINT32 FSP\_S\_CONFIG::CpuMpHob**

---

Offset 0x032F - CpuMpHob Pointer for CpuMpHob.

This is optional data buffer for CpuMpPpi usage.

Definition at line [1143](#) of file [FspUpd.h](#).

### **UINT16 FSP\_S\_CONFIG::DcLoadline[5]**

---

Offset 0x02C5 - DcLoadline PCODE MMIO Mailbox: DcLoadline in

1/100 mOhms (ie.

1250 = 12.50 mOhm); Range is 0-6249.**Intel Recommended Defaults vary by domain and SKU.**

Definition at line [975](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::DebugInterfaceEnable**

---

Offset 0x0333 - Enable or Disable processor debug features Enable or Disable processor debug features; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line [1149](#) of file [FspUpd.h](#).

### **UINT16 FSP\_S\_CONFIG::DeltaT12PowerCycleDelay**

---

Offset 0x0232 - Delta T12 Power Cycle Delay required in ms Select the value for delay required.

0(Default)= No delay, 0xFFFF = Auto calculate T12 Delay to max 500ms 0 : No Delay, 0xFFFF : Auto Calulate T12 Delay

Definition at line [828](#) of file [FspUpd.h](#).

### **UINT32 FSP\_S\_CONFIG::DevIntConfigPtr**

---

Offset 0x007B - Address of PCH\_DEVICE\_INTERRUPT\_CONFIG table.

The address of the table of PCH\_DEVICE\_INTERRUPT\_CONFIG.

Definition at line [214](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::DmiSuggestedSetting**

---

Offset 0x0719 - DMI Thermal Sensor Suggested Setting DMT thermal sensor suggested representative values.

\$EN\_DIS

Definition at line [2070](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::DmiTS0TW**

---

Offset 0x071A - Thermal Sensor 0 Target Width DMT thermal sensor suggested representative values.

0:x1, 1:x2, 2:x4, 3:x8, 4:x16

Definition at line [2076](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::DmiTS1TW**

---

Offset 0x071B - Thermal Sensor 1 Target Width Thermal Sensor 1 Target Width.

0:x1, 1:x2, 2:x4, 3:x8, 4:x16

Definition at line [2082](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::DmiTS2TW**

---

Offset 0x071C - Thermal Sensor 2 Target Width Thermal Sensor 2 Target Width.

0:x1, 1:x2, 2:x4, 3:x8, 4:x16

Definition at line [2088](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::DmiTS3TW**

---

Offset 0x071D - Thermal Sensor 3 Target Width Thermal Sensor 3 Target Width.

0:x1, 1:x2, 2:x4, 3:x8, 4:x16

Definition at line [2094](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::EcCmdLock**

---

Offset 0x078E - EcCmdLock EcCmdLock default values.

Locks Ephemeral Authorization Value sent previously

Definition at line [2285](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::EcCmdProvisionEav**

---

Offset 0x078D - EcCmdProvisionEav Ephemeral Authorization Value default values.

Provisions an ephemeral shared secret to the EC

Definition at line [2280](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::Enable8254ClockGating**

---

Offset 0x074F - Enable 8254 Static Clock Gating Set 8254CGE=1 is required for SLP\_S0 support.

However, set 8254CGE=1 in POST time might fail to boot legacy OS using 8254 timer. Make sure it is disabled to support boot legacy OS using 8254 timer. Also enable this while S0ix is enabled. \$EN\_DIS

Definition at line [2213](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::Enable8254ClockGatingOnS3**

---

Offset 0x0752 - Enable 8254 Static Clock Gating On S3 This is only applicable when Enable8254ClockGating is disabled.

FSP will do the 8254 CGE programming on S3 resume when Enable8254ClockGatingOnS3 is enabled. This avoids the SMI requirement for the programming. \$EN\_DIS

Definition at line [2233](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::EnableTcoTimer**

---

Offset 0x0758 - Enable TCO timer.

When FALSE, it disables PCH ACPI timer, and stops TCO timer.  
NOTE: This will have huge power impact when it's enabled. If TCO timer is disabled, uCode ACPI timer emulation must be enabled, and WDAT table must not be exposed to the OS. \$EN\_DIS

Definition at line [2253](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::EsataSpeedLimit**

---

Offset 0x068E - PCH Sata eSATA Speed Limit When enabled, BIOS will configure the PxSCTL.SPD to 2 to limit the eSATA port speed.

\$EN\_DIS

Definition at line [1777](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::FastPkgCRampDisableFivr**

---

Offset 0x0313 - Disable Fast Slew Rate for Deep Package C States for VR FIVR domain Disable Fast Slew Rate for Deep Package C States based on Acoustic Noise Mitigation feature enabled.

**0: False; 1: True \$EN\_DIS**

Definition at line [1081](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::FastPkgCRampDisableGt**

---

Offset 0x0301 - Disable Fast Slew Rate for Deep Package C States for VR GT domain Disable Fast Slew Rate for Deep Package C States based on Acoustic Noise Mitigation feature enabled.

**0: False; 1: True \$EN\_DIS**

Definition at line [1007](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::FastPkgCRampDisableIa**

---

Offset 0x02A3 - Disable Fast Slew Rate for Deep Package C States for VR IA domain Disable Fast Slew Rate for Deep Package C States based on Acoustic Noise Mitigation feature enabled.

**0: False; 1: True \$EN\_DIS**

Definition at line [932](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::FastPkgCRampDisableSa**

---

Offset 0x0302 - Disable Fast Slew Rate for Deep Package C States for VR SA domain Disable Fast Slew Rate for Deep Package C States based on Acoustic Noise Mitigation feature enabled.

**0: False; 1: True \$EN\_DIS**

Definition at line [1014](#) of file [FspUpd.h](#).

## **UINT16 FSP\_S\_CONFIG::FivrRfiFrequency**

---

Offset 0x030F - FIVR RFI Frequency PCODE MMIO Mailbox: Set the desired RFI frequency, in increments of 100KHz.

**0: Auto.** Range varies based on XTAL clock: 0-1918 (Up to 191.8MHz) for 24MHz clock; 0-1535 (Up to 153.5MHz) for 19MHz clock.

Definition at line [1062](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::FivrSpreadSpectrum**

---

Offset 0x0312 - FIVR RFI Spread Spectrum PCODE MMIO Mailbox: FIVR RFI Spread Spectrum, in 0.1% increments.

**0: 0%**; Range: 0.0% to 10.0% (0-100).

Definition at line [1074](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::ForcMebxSyncUp**

---

Offset 0x0161 - MEBX execution Enable/Disable.

0: Disable, 1: enable, Force MEBX execution \$EN\_DIS

Definition at line [632](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::FwProgress**

---

Offset 0x0159 - PET Progress Enable/Disable.

0: Disable, 1: enable, Enable/Disable PET Events Progress to

receive PET Events. \$EN\_DIS

Definition at line [596](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::GpioIrqRoute**

---

Offset 0x0088 - Select GPIO IRQ Route GPIO IRQ Select.

The valid value is 14 or 15.

Definition at line [232](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::Heci3Enabled**

---

Offset 0x014D - HECl3 state The HECl3 state from Mbp for reference in S3 path or when MbpHob is not installed.

0: disable, 1: enable \$EN\_DIS

Definition at line [524](#) of file [FspUpd.h](#).

### **UINT16 FSP\_S\_CONFIG::IccMax[5]**

---

Offset 0x02ED - Icc Max limit PCODE MMIO Mailbox: VR Icc Max limit.

0-255A in 1/4 A units. 400 = 100A

Definition at line [995](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::ImonOffset[5]**

---

Offset 0x0287 - Imon offset correction PCODE MMIO Mailbox: Imon offset correction.

Value is a 2's complement signed integer. Units 1/1000, Range 0-63999. For an offset = 12.580, use 12580. **0: Auto**

Definition at line [881](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::ImonSlope[5]**

---

Offset 0x0282 - Imon slope correction PCODE MMIO Mailbox: Imon slope correction.

Specified in 1/100 increment values. Range is 0-200. 125 = 1.25. **0: Auto**.For all VR Indexes

Definition at line [875](#) of file [FspUpd.h](#).

### **UINT16 FSP\_S\_CONFIG::ImonSlope1[5]**

---

Offset 0x031A - Imon slope1 correction PCODE MMIO Mailbox: Imon slope correction.

Specified in 1/100 increment values. Range is 0-200. 125 = 1.25. **0: Auto**.For all VR Indexes

Definition at line [1105](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::IsIVrCmd**

---

Offset 0x0319 - Activates VR mailbox command for Intersil VR C-state issues.

Intersil VR mailbox command. **0 - no mailbox command sent**. 1 - VR mailbox command sent for IA/GT rails only. 2 - VR mailbox command sent for IA/GT/SA rails.

Definition at line [1099](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::ManageabilityMode**

---

Offset 0x0158 - Manageability Mode set by Mebx Enable/Disable.

0: Disable, 1: enable, Enable or disable Manageability Mode.  
\$EN\_DIS

Definition at line [589](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::McivrRfiFrequencyAdjust**

---

Offset 0x030E - McIVR RFI Frequency Adjustment PCODE MMIO Mailbox: Adjust the RFI frequency relative to the nominal frequency in increments of 100KHz.

For subtraction, change McivrRfiFrequencyPrefix. **0: Auto**.

Definition at line [1055](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::McivrRfiFrequencyPrefix**

---

Offset 0x030D - McIVR RFI Frequency Prefix PCODE MMIO Mailbox: McIVR RFI Frequency Adjustment Prefix.

**0: Plus (+); 1: Minus (-).**

Definition at line [1049](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::McivrSpreadSpectrum**

---

Offset 0x0311 - McIVR RFI Spread Spectrum PCODE MMIO Mailbox: McIVR RFI Spread Spectrum.

**0: 0%; 1: +/- 0.5%; 2: +/- 1%; 3: +/- 1.5%; 4: +/- 2%; 5: +/- 3%; 6: +/- 4%; 7: +/- 5%; 8: +/- 6%.**

Definition at line [1068](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::MeUnconfigOnRtcClear**

---

Offset 0x07A8 - ME Unconfig on RTC clear 0: Disable ME Unconfig On Rtc Clear.

1: Enable ME Unconfig On Rtc Clear. 2: Cmos is clear, status unkown. 3: Reserved 0: Disable ME Unconfig On Rtc Clear, 1: Enable ME Unconfig On Rtc Clear, 2: Cmos is clear, 3: Reserved

Definition at line [2328](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::NumOfDevIntConfig**

---

Offset 0x007F - Number of DevIntConfig Entry Number of Device Interrupt Configuration Entry.

If this is not zero, the DevIntConfigPtr must not be NULL.

Definition at line [220](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchCnviMode**

---

Offset 0x0146 - CNVi Configuration This option allows for automatic detection of Connectivity Solution.

[Auto Detection] assumes that CNVi will be enabled when available, [Disable] allows for disabling CNVi. 0:Disable, 1:Auto

Definition at line [481](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchCrid**

---

Offset 0x0394 - PCH Compatibility Revision ID This member

describes whether or not the CRID feature of PCH should be enabled.

**\$EN\_DIS**

Definition at line [1373](#) of file [FspUpd.h](#).

---

### **UINT8 FSP\_S\_CONFIG::PchDmiAspm**

Offset 0x0346 - Enable DMI ASPM Deprecated.

**\$EN\_DIS**

Definition at line [1161](#) of file [FspUpd.h](#).

---

### **UINT8 FSP\_S\_CONFIG::PchDmiAspmCtrl**

Offset 0x07AB - Pch Dmi Aspm Ctrl ASPM configuration on the PCH side of the DMI/OPI Link.

Default is **PchPcieAspmAutoConfig** 0:Disabled, 1:L0s, 2:L1, 3:L0sL1, 4:Auto

Definition at line [2349](#) of file [FspUpd.h](#).

---

### **UINT8 FSP\_S\_CONFIG::PchDmiTsawEn**

Offset 0x0718 - DMI Thermal Sensor Autonomous Width Enable DMI Thermal Sensor Autonomous Width Enable.

**\$EN\_DIS**

Definition at line [2064](#) of file [FspUpd.h](#).

---

### **UINT8 FSP\_S\_CONFIG::PchEnableComplianceMode**

Offset 0x0734 - Enable xHCI Compliance Mode Compliance Mode can be enabled for testing through this option but this is disabled by default.

\$EN\_DIS

Definition at line [2195](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchEnableDbcObs**

---

Offset 0x067C - USB Overcurrent Override for DbC This option overrides USB Over Current enablement state that USB OC will be disabled after enabling this option.

Enable when DbC is used to avoid signaling conflicts. \$EN\_DIS

Definition at line [1687](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchHdaAudioLinkDmic0**

---

Offset 0x00FE - Enable HD Audio DMIC0 Link Enable/disable HD Audio DMIC0 link.

Muxed with SNDW4. \$EN\_DIS

Definition at line [341](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchHdaAudioLinkDmic1**

---

Offset 0x00FF - Enable HD Audio DMIC1 Link Enable/disable HD Audio DMIC1 link.

Muxed with SNDW3. \$EN\_DIS

Definition at line [347](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchHdaAudioLinkHda**

---

Offset 0x00FD - Enable HD Audio Link Enable/disable HD Audio Link.

Muxed with SSP0/SSP1/SNDW1. \$EN\_DIS

Definition at line [335](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchHdaAudioLinkSndw1**

---

Offset 0x0103 - Enable HD Audio SoundWire#1 Link Enable/disable HD Audio SNDW1 link.

Muxed with HDA. \$EN\_DIS

Definition at line [371](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchHdaAudioLinkSndw2**

---

Offset 0x0104 - Enable HD Audio SoundWire#2 Link Enable/disable HD Audio SNDW2 link.

Muxed with SSP1. \$EN\_DIS

Definition at line [377](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchHdaAudioLinkSndw3**

---

Offset 0x0105 - Enable HD Audio SoundWire#3 Link Enable/disable HD Audio SNDW3 link.

Muxed with DMIC1. \$EN\_DIS

Definition at line [383](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchHdaAudioLinkSndw4**

---

Offset 0x0106 - Enable HD Audio SoundWire#4 Link Enable/disable HD Audio SNDW4 link.

Muxed with DMIC0. \$EN\_DIS

Definition at line [389](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchHdaAudioLinkSsp0**

---

Offset 0x0100 - Enable HD Audio SSP0 Link Enable/disable HD Audio SSP0/I2S link.

Muxed with HDA. \$EN\_DIS

Definition at line [353](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchHdaAudioLinkSsp1**

---

Offset 0x0101 - Enable HD Audio SSP1 Link Enable/disable HD Audio SSP1/I2S link.

Muxed with HDA/SNDW2. \$EN\_DIS

Definition at line [359](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchHdaAudioLinkSsp2**

---

Offset 0x0102 - Enable HD Audio SSP2 Link Enable/disable HD Audio SSP2/I2S link.

\$EN\_DIS

Definition at line [365](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchHdaDspEnable**

---

Offset 0x002D - Enable HD Audio DSP Enable/disable HD Audio DSP feature.

\$EN\_DIS

Definition at line [113](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchHdaDspUaaCompliance**

---

Offset 0x036C - Universal Audio Architecture compliance for DSP enabled system 0: Not-UAA Compliant (Intel SST driver supported only), 1: UAA Compliant (HDA Inbox driver or SST driver supported).

\$EN\_DIS

Definition at line [1229](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchHdalDispCodecDisconnect**

---

Offset 0x036D - iDisplay Audio Codec disconnection 0: Not disconnected, enumerable, 1: Disconnected SDI, not enumerable.

\$EN\_DIS

Definition at line [1235](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchHdalDispLinkFrequency**

---

Offset 0x036A - iDisp-Link Frequency iDisp-Link Freq (PCH\_HDAUDIO\_LINK\_FREQUENCY enum): 4: 96MHz, 3: 48MHz.

4: 96MHz, 3: 48MHz

Definition at line [1216](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchHdalDispLinkTmode**

---

Offset 0x036B - iDisp-Link T-mode iDisp-Link T-Mode (PCH\_HDAUDIO\_IDISP\_TMODE enum): 0: 2T, 1: 1T.

0: 2T, 1: 1T

Definition at line [1222](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchHdaLinkFrequency**

---

Offset 0x0369 - HD Audio Link Frequency HDA Link Freq (PCH\_HDAUDIO\_LINK\_FREQUENCY enum): 0: 6MHz, 1: 12MHz, 2: 24MHz.

0: 6MHz, 1: 12MHz, 2: 24MHz

Definition at line [1210](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchHdaPme**

---

Offset 0x0366 - Enable Pme Enable Azalia wake-on-ring.

\$EN\_DIS

Definition at line [1194](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchHdaSndwBufferRcomp**

---

Offset 0x0107 - Soundwire Clock Buffer GPIO RCOMP Setting 0: non-ACT - 50 Ohm driver impedance, 1: ACT - 8 Ohm driver

impedance.

\$EN\_DIS

Definition at line [395](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchHdaVcType**

---

Offset 0x0368 - VC Type Virtual Channel Type Select: 0: VC0, 1: VC1.

0: VC0, 1: VC1

Definition at line [1204](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchHotEnable**

---

Offset 0x014F - PCHHOT# pin Enable PCHHOT# pin assertion when temperature is higher than PchHotLevel.

0: disable, 1: enable \$EN\_DIS

Definition at line [534](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIoApicEntry24\_119**

---

Offset 0x037D - Enable PCH Io Apic Entry 24-119 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line [1251](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIoApicId**

---

Offset 0x037E - PCH Io Apic ID This member determines IOAPIC ID.

Default is 0x02.

Definition at line [1256](#) of file [FspsUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchIshGp0GpioAssign**

---

Offset 0x0386 - Enable PCH ISH GP\_0 GPIO pin assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line [1302](#) of file [FspsUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchIshGp1GpioAssign**

---

Offset 0x0387 - Enable PCH ISH GP\_1 GPIO pin assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line [1308](#) of file [FspsUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchIshGp2GpioAssign**

---

Offset 0x0388 - Enable PCH ISH GP\_2 GPIO pin assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line [1314](#) of file [FspsUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIshGp3GpioAssign**

---

Offset 0x0389 - Enable PCH ISH GP\_3 GPIO pin assigned 0:  
Disable; 1: Enable.

\$EN\_DIS

Definition at line [1320](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIshGp4GpioAssign**

---

Offset 0x038A - Enable PCH ISH GP\_4 GPIO pin assigned 0:  
Disable; 1: Enable.

\$EN\_DIS

Definition at line [1326](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIshGp5GpioAssign**

---

Offset 0x038B - Enable PCH ISH GP\_5 GPIO pin assigned 0:  
Disable; 1: Enable.

\$EN\_DIS

Definition at line [1332](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIshGp6GpioAssign**

---

Offset 0x038C - Enable PCH ISH GP\_6 GPIO pin assigned 0:  
Disable; 1: Enable.

\$EN\_DIS

Definition at line [1338](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIshGp7GpioAssign**

---

Offset 0x038D - Enable PCH ISH GP\_7 GPIO pin assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line [1344](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIshI2c0GpioAssign**

---

Offset 0x0383 - Enable PCH ISH I2C0 GPIO pins assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line [1284](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIshI2c1GpioAssign**

---

Offset 0x0384 - Enable PCH ISH I2C1 GPIO pins assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line [1290](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIshI2c2GpioAssign**

---

Offset 0x0385 - Enable PCH ISH I2C2 GPIO pins assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line [1296](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIshPdtUnlock**

---

Offset 0x038E - PCH ISH PDT Unlock Msg 0: False; 1: True.

\$EN\_DIS

Definition at line [1350](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIshSpiGpioAssign**

---

Offset 0x0380 - Enable PCH ISH SPI GPIO pins assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line [1266](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIshUart0GpioAssign**

---

Offset 0x0381 - Enable PCH ISH UART0 GPIO pins assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line [1272](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchIshUart1GpioAssign**

---

Offset 0x0382 - Enable PCH ISH UART1 GPIO pins assigned 0: Disable; 1: Enable.

\$EN\_DIS

Definition at line [1278](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchLanEnable**

---

Offset 0x00FC - Enable LAN Enable/disable LAN controller.

\$EN\_DIS

Definition at line [329](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchLanLtrEnable**

---

Offset 0x038F - Enable PCH Lan LTR capability of PCH internal LAN  
0: Disable; 1: Enable.

\$EN\_DIS

Definition at line [1356](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchLockDownBiosLock**

---

Offset 0x0393 - Enable LOCKDOWN BIOS LOCK Enable the BIOS Lock feature and set EISS bit (D31:F5:RegDCh[5]) for the BIOS region protection.

\$EN\_DIS

Definition at line [1367](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchLockDownRtcMemoryLock**

---

Offset 0x0395 - RTC CMOS MEMORY LOCK Enable RTC lower and upper 128 byte Lock bits to lock Bytes 38h-3Fh in the upper and lower 128-byte bank of RTC RAM.

\$EN\_DIS

Definition at line [1380](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchMemoryThrottlingEnable**

---

Offset 0x072B - Enable Memory Thermal Throttling Enable Memory Thermal Throttling.

\$EN\_DIS

Definition at line [2168](#) of file [FspUpd.h](#).

### **UINT32 FSP\_S\_CONFIG::PchPcieDeviceOverrideTablePtr**

---

Offset 0x0754 - Pch PCIE device override table pointer The PCIe device table is being used to override PCIe device ASPM settings.

This is a pointer points to a 32bit address. And it's only used in PostMem phase. Please refer to PCH\_PCIE\_DEVICE\_OVERRIDE structure for the table. Last entry VendorId must be 0.

Definition at line [2245](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmDeepSxPol**

---

Offset 0x0675 - PCH Pm Deep Sx Pol Deep Sx Policy.

\$EN\_DIS

Definition at line [1639](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmDisableDsxAcPresentPulldown**

---

Offset 0x0684 - PCH Pm Disable Dsx Ac Present Pulldown When Disable, PCH will internal pull down AC\_PRESENT in deep SX and during G3 exit.

**\$EN\_DIS**

Definition at line [1721](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmDisableNativePowerButton**

---

Offset 0x0686 - PCH Pm Disable Native Power Button Power button native mode disable.

**\$EN\_DIS**

Definition at line [1731](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmLanWakeFromDeepSx**

---

Offset 0x0674 - PCH Pm Lan Wake From DeepSx Determine if enable LAN to wake from deep Sx.

**\$EN\_DIS**

Definition at line [1633](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmLpcClockRun**

---

Offset 0x0680 - PCH Pm Lpc Clock Run This member describes whether or not the LPC ClockRun feature of PCH should be enabled.

Default value is Disabled **\$EN\_DIS**

Definition at line [1698](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmMeWakeSts**

---

Offset 0x0688 - PCH Pm ME\_WAKE\_STS Clear the

ME\_WAKE\_STS bit in the Power and Reset Status (PRSTS) register.

\$EN\_DIS

Definition at line [1743](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmPciePllSsc**

---

Offset 0x068B - PCH Pm Pcie Pll Ssc Specifies the Pcie Pll Spread Spectrum Percentage.

The default is 0xFF: AUTO - No BIOS override.

Definition at line [1761](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmPcieWakeFromDeepSx**

---

Offset 0x0671 - PCH Pm Pcie Wake From DeepSx Determine if enable PCIe to wake from deep Sx.

\$EN\_DIS

Definition at line [1614](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmPmeB0S5Dis**

---

Offset 0x0669 - PCH Pm PME\_B0\_S5\_DIS When cleared (default), wake events from PME\_B0\_STS are allowed in S5 if PME\_B0\_EN = 1.

\$EN\_DIS

Definition at line [1582](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchPmPwrBtnOverridePeriod**

---

Offset 0x0683 - PCH Pm Pwr Btn Override Period PCH power button override period.

000b-4s, 001b-6s, 010b-8s, 011b-10s, 100b-12s, 101b-14s.

Definition at line [1715](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchPmPwrCycDur**

---

Offset 0x068A - PCH Pm Reset Power Cycle Duration Could be customized in the unit of second.

Please refer to EDS for all support settings. 0 is default, 1 is 1 second, 2 is 2 seconds, ...

Definition at line [1755](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchPmSlpAMinAssert**

---

Offset 0x0679 - PCH Pm Slp A Min Assert SLP\_A Minimum Assertion Width Policy.

Default is PchSlpA2s.

Definition at line [1659](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchPmSlpLanLowDc**

---

Offset 0x0682 - PCH Pm Slp Lan Low Dc Enable/Disable SLP\_LAN# Low on DC Power.

\$EN\_DIS

Definition at line [1710](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchPmSlpS0Enable**

---

Offset 0x0687 - PCH Pm Slp S0 Enable Indicates whether SLP\_S0# is to be asserted when PCH reaches idle state.

\$EN\_DIS

Definition at line [1737](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchPmSlpS0Vm070VSupport**

---

Offset 0x0153 - SLP\_S0 VM 0.70V Support SLP\_S0 Voltage Margining 0.70V Support Policy.

0: disable, 1: enable \$EN\_DIS

Definition at line [559](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchPmSlpS0Vm075VSupport**

---

Offset 0x0154 - SLP\_S0 VM 0.75V Support SLP\_S0 Voltage Margining 0.75V Support Policy.

0: disable, 1: enable \$EN\_DIS

Definition at line [565](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchPmSlpS0VmRuntimeControl**

---

Offset 0x0152 - SLP\_S0 VM Dynamic Control SLP\_S0 Voltage Margining Runtime Control Policy.

0: disable, 1: enable \$EN\_DIS

Definition at line [553](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmSlpS3MinAssert**

---

Offset 0x0676 - PCH Pm Slp S3 Min Assert SLP\_S3 Minimum Assertion Width Policy.

Default is PchSlpS350ms.

Definition at line [1644](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmSlpS4MinAssert**

---

Offset 0x0677 - PCH Pm Slp S4 Min Assert SLP\_S4 Minimum Assertion Width Policy.

Default is PchSlpS44s.

Definition at line [1649](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmSlpStrchSusUp**

---

Offset 0x0681 - PCH Pm Slp Strch Sus Up Enable SLP\_X Stretching After SUS Well Power Up.

\$EN\_DIS

Definition at line [1704](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmSlpSusMinAssert**

---

Offset 0x0678 - PCH Pm Slp Sus Min Assert SLP\_SUS Minimum Assertion Width Policy.

Default is PchSlpSus4s.

Definition at line [1654](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchPmVrAlert**

---

Offset 0x0151 - VRAalert# Pin When VRAalert# feature pin is enabled and its state is '0', the PMC requests throttling to a T3 Tstate to the PCH throttling unit.

. 0: disable, 1: enable \$EN\_DIS

Definition at line [547](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchPmWoLEnableOverride**

---

Offset 0x0670 - PCH Pm WoL Enable Override Corresponds to the WoL Enable Override bit in the General PM Configuration B (GEN\_PMCON\_B) register.

\$EN\_DIS

Definition at line [1608](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchPmWoLOvrWkSts**

---

Offset 0x0689 - PCH Pm WOL\_OVR\_WK\_STS Clear the WOL\_OVR\_WK\_STS bit in the Power and Reset Status (PRSTS) register.

\$EN\_DIS

Definition at line [1749](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchPmWoWlanDeepSxEnable**

---

Offset 0x0673 - PCH Pm WoW lan DeepSx Enable Determine if

WLAN wake from DeepSx, corresponds to the DSX\_WLAN\_PP\_EN bit in the PWRM\_CFG3 register.

\$EN\_DIS

Definition at line [1627](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPmWoWlanEnable**

---

Offset 0x0672 - PCH Pm WoW Ian Enable Determine if WLAN wake from Sx, corresponds to the HOST\_WLAN\_PP\_EN bit in the PWRM\_CFG3 register.

\$EN\_DIS

Definition at line [1620](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchPwrOptEnable**

---

Offset 0x0347 - Enable Power Optimizer Enable DMI Power Optimizer on PCH side.

\$EN\_DIS

Definition at line [1167](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PchScsEmmcHs400DIIDataValid**

---

Offset 0x06F6 - Set HS400 Tuning Data Valid Set if HS400 Tuning Data Valid.

\$EN\_DIS

Definition at line [1926](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchScsEmmcHs400DriverStrength**

---

Offset 0x06F9 - I/O Driver Strength Deprecated.

0:33 Ohm, 1:40 Ohm, 2:50 Ohm

Definition at line [1942](#) of file [FspsUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchScsEmmcHs400TuningRequired**

---

Offset 0x06F5 - Enable eMMC HS400 Training Deprecated.

\$EN\_DIS

Definition at line [1920](#) of file [FspsUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchSerialloI2cPadsTermination[6]**

---

Offset 0x06FA - PCH Seriallo I2C Pads Termination 0x0: Hardware default, 0x1: None, 0x13: 1kOhm weak pull-up, 0x15: 5kOhm weak pull-up, 0x19: 20kOhm weak pull-up - Enable/disable Seriallo I2C0,I2C1,I2C2,I2C3,I2C4,I2C5 pads termination respectively.

One byte for each controller, byte0 for I2C0, byte1 for I2C1, and so on.

Definition at line [1950](#) of file [FspsUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchSirqEnable**

---

Offset 0x0708 - Enable Serial IRQ Determines if enable Serial IRQ.

\$EN\_DIS

Definition at line [1988](#) of file [FspsUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchSirqMode**

---

Offset 0x0709 - Serial IRQ Mode Select Serial IRQ Mode Select, 0: quiet mode, 1: continuous mode.

\$EN\_DIS

Definition at line [1994](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchStartFramePulse**

---

Offset 0x070A - Start Frame Pulse Width Start Frame Pulse Width, 0: PchSfpw4Clk, 1: PchSfpw6Clk, 2: PchSfpw8Clk.

0: PchSfpw4Clk, 1: PchSfpw6Clk, 2: PchSfpw8Clk

Definition at line [2000](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchTsmicLock**

---

Offset 0x070C - Thermal Device SMI Enable This locks down SMI Enable on Alert Thermal Sensor Trip.

\$EN\_DIS

Definition at line [2012](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchTTEnable**

---

Offset 0x0713 - Enable The Thermal Throttle Enable the thermal throttle function.

\$EN\_DIS

Definition at line [2033](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchTTLock**

---

Offset 0x0715 - Thermal Throttle Lock Thermal Throttle Lock.

\$EN\_DIS

Definition at line [2046](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchTTState13Enable**

---

Offset 0x0714 - PMSync State 13 When set to 1 and the programmed GPIO pin is a 1, then PMSync state 13 will force at least T2 state.

\$EN\_DIS

Definition at line [2040](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchUsbHsioFilterSel[10]**

---

Offset 0x036E - USB LFPS Filter selection For each byte bits 2:0 are for p, bits 4:6 are for n.

0h:1.6ns, 1h:2.4ns, 2h:3.2ns, 3h:4.0ns, 4h:4.8ns, 5h:5.6ns, 6h:6.4ns.

Definition at line [1241](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PchUsbHsioRxTuningEnable[10]**

---

Offset 0x04F0 - PCH USB3 HSIO Rx Tuning Enable Mask for enabling tuning of HSIO Rx signals of USB3 ports.

Bits: 0 - HsioCtrlAdaptOffsetCfgEnable, 1 - HsioFilterSelNENable, 2 - HsioFilterSelPENable, 3 - HsioOlfpsCfgPullUpDwnResEnable

Definition at line [1462](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PcieComplianceTestMode**

---

Offset 0x0665 - PCIE Compliance Test Mode Compliance Test Mode shall be enabled when using Compliance Load Board.

\$EN\_DIS

Definition at line [1557](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PcieDisableRootPortClockGating**

---

Offset 0x0662 - PCIE Disable RootPort Clock Gating Describes whether the PCI Express Clock Gating for each root port is enabled by platform modules.

0: Disable; 1: Enable. \$EN\_DIS

Definition at line [1541](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PcieEnablePeerMemoryWrite**

---

Offset 0x0663 - PCIE Enable Peer Memory Write This member describes whether Peer Memory Writes are enabled on the platform.

\$EN\_DIS

Definition at line [1547](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PcieEqPh3LaneParamCm[24]**

---

Offset 0x0628 - PCIE Eq Ph3 Lane Param Cm  
PCH\_PCIE\_EQ\_LANE\_PARAM.

Coefficient C-1.

Definition at line [1519](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PcieEqPh3LaneParamCp[24]**

---

Offset 0x0640 - PCIE Eq Ph3 Lane Param Cp  
PCH\_PCIE\_EQ\_LANE\_PARAM.

Coefficient C+1.

Definition at line [1524](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PcieRpAspm[24]**

---

Offset 0x05C8 - PCIE RP Aspm The ASPM configuration of the root port (see: PCH\_PCIE\_ASPM\_CONTROL).

Default is PchPcieAspmAutoConfig.

Definition at line [1498](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PcieRpCompletionTimeout[24]**

---

Offset 0x0546 - PCIE RP Completion Timeout The root port completion timeout(see: PCH\_PCIE\_COMPLETION\_TIMEOUT).

Default is PchPcieCompletionTO\_Default.

Definition at line [1488](#) of file [FspUpd.h](#).

### **UINT32 FSP\_S\_CONFIG::PcieRpDpcExtensionsMask**

---

Offset 0x0110 - DPC Extensions PCIE RP Mask Enable/disable DPC Extensions for PCIE Root Ports.

0: disable, 1: enable. One bit for each port, bit0 for port1, bit1 for port2, and so on.

Definition at line [413](#) of file [FspUpd.h](#).

## **UINT32 FSP\_S\_CONFIG::PcieRpDpcMask**

---

Offset 0x010C - DPC for PCIE RP Mask Enable/disable Downstream Port Containment for PCIE Root Ports.

0: disable, 1: enable. One bit for each port, bit0 for port1, bit1 for port2, and so on.

Definition at line [407](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PcieRpFunctionSwap**

---

Offset 0x0666 - PCIE Rp Function Swap Allows BIOS to use root port function number swapping when root port of function 0 is disabled.

\$EN\_DIS

Definition at line [1564](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PcieRpGen3EqPh3Method[24]**

---

Offset 0x0516 - PCIE RP Gen3 Equalization Phase Method PCIe Gen3 Eq Ph3 Method (see PCH\_PCIE\_EQ\_METHOD).

0: DEPRECATED, hardware equalization; 1: hardware equalization;  
4: Fixed Coeficients.

Definition at line [1478](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PcieRpImrEnabled**

---

Offset 0x066D - PCIE IMR Enables Isolated Memory Region for PCIe.

\$EN\_DIS

Definition at line [1593](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PcieRpL1Substates[24]**

---

Offset 0x05E0 - PCIE RP L1 Substates The L1 Substates configuration of the root port (see: PCH\_PCIE\_L1SUBSTATES\_CONTROL).

Default is PchPcieL1SubstatesL1\_1\_2.

Definition at line [1504](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PcieRpPcieSpeed[24]**

---

Offset 0x04FE - PCIE RP Pcie Speed Determines each PCIE Port speed capability.

0: Auto; 1: Gen1; 2: Gen2; 3: Gen3 (see: PCH\_PCIE\_SPEED).

Definition at line [1472](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PcieRpPhysicalSlotNumber[24]**

---

Offset 0x052E - PCIE RP Physical Slot Number Indicates the slot number for the root port.

Default is the value as root port index.

Definition at line [1483](#) of file [FspUpd.h](#).

## **UINT32 FSP\_S\_CONFIG::PcieRpPtmMask**

---

Offset 0x0108 - PTM for PCIE RP Mask Enable/disable Precision Time Measurement for PCIE Root Ports.

0: disable, 1: enable. One bit for each port, bit0 for port1, bit1 for port2, and so on.

Definition at line [401](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PcieSwEqCoeffListCm[5]**

---

Offset 0x0658 - PCIE Sw Eq CoeffList Cm PCH\_PCIE\_EQ\_PARAM.

Coefficient C-1.

Definition at line [1529](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PcieSwEqCoeffListCp[5]**

---

Offset 0x065D - PCIE Sw Eq CoeffList Cp PCH\_PCIE\_EQ\_PARAM.

Coefficient C+1.

Definition at line [1534](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PmcCpuC10GatePinEnable**

---

Offset 0x07AA - Pmc Cpu C10 Gate Pin Enable Enable/Disable platform support for CPU\_C10\_GATE# pin to control gating of CPU VccIO and VccSTG rails instead of SLP\_S0# pin.

\$EN\_DIS

Definition at line [2343](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PmcDbgMsgEn**

---

Offset 0x011F - PMC Debug Message Enable When Enabled, PMC HW will send debug messages to trace hub; When Disabled, PMC HW will never send debug messages to trace hub.

Noted: When Enabled, may not enter S0ix \$EN\_DIS

Definition at line [452](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PmcModPhySusPgEnable**

---

Offset 0x01FB - ModPHY SUS Power Domain Dynamic Gating Enable/Disable ModPHY SUS Power Domain Dynamic Gating.

Setting not supported on PCH-H. 0: disable, 1: enable \$EN\_DIS

Definition at line [677](#) of file [FspUpd.h](#).

### **UINT32 FSP\_S\_CONFIG::PmcPowerButtonDebounce**

---

Offset 0x0115 - Power button debounce configuration Debounce time for PWRBTN in microseconds.

For values not supported by HW, they will be rounded down to closest supported on. 0: disable, 250-1024000us: supported range

Definition at line [426](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PortUsb20Enable[16]**

---

Offset 0x0052 - Enable USB2 ports Enable/disable per USB2 ports.

One byte for each port, byte0 for port0, byte1 for port1, and so on.

Definition at line [185](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PortUsb30Enable[10]**

---

Offset 0x0062 - Enable USB3 ports Enable/disable per USB3 ports.

One byte for each port, byte0 for port0, byte1 for port1, and so on.

Definition at line [191](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PreWake**

---

Offset 0x0328 - Pre Wake Randomization time PCODE MMIO  
Mailbox: Acoustic Mitigation Range.Defines the maximum pre-wake randomization time in micro ticks.This can be programmed only if AcousticNoiseMitigation is enabled.

Range 0-255 0.

Definition at line [1119](#) of file [FspUpd.h](#).

### **UINT16 FSP\_S\_CONFIG::Psi1Threshold[5]**

---

Offset 0x02CF - Power State 1 Threshold current PCODE MMIO  
Mailbox: Power State 1 current cutoff in 1/4 Amp increments.

Range is 0-128A.

Definition at line [980](#) of file [FspUpd.h](#).

### **UINT16 FSP\_S\_CONFIG::Psi2Threshold[5]**

---

Offset 0x02D9 - Power State 2 Threshold current PCODE MMIO

Mailbox: Power State 2 current cutoff in 1/4 Amp increments.

Range is 0-128A.

Definition at line [985](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::Psi3Enable[5]**

---

Offset 0x0278 - Power State 3 enable/disablePCODE MMIO  
Mailbox: Power State 3 enable/disable; 0: Disable; **1: Enable**.

For all VR Indexes

Definition at line [863](#) of file [FspUpd.h](#).

### **UINT16 FSP\_S\_CONFIG::Psi3Threshold[5]**

---

Offset 0x02E3 - Power State 3 Threshold currentPCODE MMIO  
Mailbox: Power State 3 current cutoff in 1/4 Amp increments.

Range is 0-128A.

Definition at line [990](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::PsOnEnable**

---

Offset 0x07A9 - Enable PS\_ON.

PS\_ON is a new C10 state from the CPU on desktop SKUs that enables a lower power target that will be required by the California Energy Commission (CEC). When FALSE, PS\_ON is to be disabled.  
**\$EN\_DIS**

Definition at line [2336](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::PsysOffset**

---

Offset 0x02A1 - Platform Psys offset correction PCODE MMIO  
Mailbox: Platform Psys offset correction.

**0 - Auto** Units 1/4, Range 0-255. Value of 100 =  $100/4 = 25$  offset

Definition at line [917](#) of file **FspUpd.h**.

## **UINT8 FSP\_S\_CONFIG::PsysSlope**

---

Offset 0x02A0 - Platform Psys slope correction PCODE MMIO  
Mailbox: Platform Psys slope correction.

**0 - Auto** Specified in 1/100 increment values. Range is 0-200. 125 = 1.25

Definition at line [911](#) of file **FspUpd.h**.

## **UINT8 FSP\_S\_CONFIG::PxRcConfig[8]**

---

Offset 0x0080 - PIRQx to IRQx Map Config PIRQx to IRQx mapping.

The valid value is 0x00 to 0x0F for each. First byte is for PIRQA, second byte is for PIRQB, and so on. The setting is only available in Legacy 8259 PCI mode.

Definition at line [227](#) of file **FspUpd.h**.

## **UINT8 FSP\_S\_CONFIG::RemoteAssistance**

---

Offset 0x015F - Remote Assistance Trigger Availability  
Enable/Disable.

0: Disable, 1: enable, Remote Assistance enable/disable state by Mebx \$EN\_DIS

Definition at line [620](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::SataEnable**

---

Offset 0x0092 - Enable SATA Enable/disable SATA controller.

\$EN\_DIS

Definition at line [269](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::SataLedEnable**

---

Offset 0x0150 - SATA LED SATA LED indicating SATA controller activity.

0: disable, 1: enable \$EN\_DIS

Definition at line [540](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::SataMode**

---

Offset 0x0093 - SATA Mode Select SATA controller working mode.

0:AHCI, 1:RAID

Definition at line [275](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::SataP0TDispFinit**

---

Offset 0x0727 - Port 0 Alternate Fast Init Tdispatch Port 0 Alternate Fast Init Tdispatch.

\$EN\_DIS

Definition at line [2145](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataP1TDispFinit**

---

Offset 0x0729 - Port 1 Alternate Fast Init Tdispatch Port 1 Alternate Fast Init Tdispatch.

\$EN\_DIS

Definition at line [2156](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataPortsDevSlp[8]**

---

Offset 0x004A - Enable SATA DEVSLP Feature Enable/disable SATA DEVSLP per port.

0 is disable, 1 is enable. One byte for each port, byte0 for port0, byte1 for port1, and so on.

Definition at line [179](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataPortsDmVal[8]**

---

Offset 0x06C0 - Enable SATA Port DmVal DITO multiplier.

Default is 15.

Definition at line [1817](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataPortsEnable[8]**

---

Offset 0x0042 - Enable SATA ports Enable/disable SATA ports.

One byte for each port, byte0 for port0, byte1 for port1, and so on.

Definition at line [173](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataPwrOptEnable**

---

Offset 0x068D - PCH Sata Pwr Opt Enable SATA Power Optimizer on PCH side.

\$EN\_DIS

Definition at line [1771](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataRstHddUnlock**

---

Offset 0x06E8 - PCH Sata Rst Hdd Unlock Indicates that the HDD password unlock in the OS is enabled.

\$EN\_DIS

Definition at line [1880](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataRstInterrupt**

---

Offset 0x07A7 - SATA RST Interrupt Mode Allowes to choose which interrupts will be implemented by SATA controller in RAID mode.

0:Msix, 1:Msi, 2:Legacy

Definition at line [2320](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataRstIrrt**

---

Offset 0x06E5 - PCH Sata Rst Irrt Intel Rapid Recovery Technology.

\$EN\_DIS

Definition at line [1863](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataRstIrrtOnly**

---

Offset 0x06EA - PCH Sata Rst Irrt Only Allow only IRRT drives to span internal and external ports.

\$EN\_DIS

Definition at line [1893](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataRstLedLocate**

---

Offset 0x06E9 - PCH Sata Rst Led Locate Indicates that the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS.

\$EN\_DIS

Definition at line [1887](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataRstOromUiBanner**

---

Offset 0x06E6 - PCH Sata Rst Orom Ui Banner OROM UI and BANNER.

\$EN\_DIS

Definition at line [1869](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataRstPcieDeviceResetDelay[3]**

---

Offset 0x06F2 - PCH Sata Rst Pcie Device Reset Delay PCIe Storage Device Reset Delay in milliseconds.

Default value is 100ms

Definition at line [1914](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::SataRstRaid0**

---

Offset 0x06E1 - PCH Sata Rst Raid0 RAID0.

\$EN\_DIS

Definition at line [1839](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::SataRstRaid1**

---

Offset 0x06E2 - PCH Sata Rst Raid1 RAID1.

\$EN\_DIS

Definition at line [1845](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::SataRstRaid10**

---

Offset 0x06E3 - PCH Sata Rst Raid10 RAID10.

\$EN\_DIS

Definition at line [1851](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::SataRstRaid5**

---

Offset 0x06E4 - PCH Sata Rst Raid5 RAID5.

\$EN\_DIS

Definition at line [1857](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataRstRaidDeviceId**

---

Offset 0x06E0 - PCH Sata Rst Raid Device Id Enable RAID Alternate ID.

0:Client, 1:Alternate, 2:Server

Definition at line [1833](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataRstSmartStorage**

---

Offset 0x06EB - PCH Sata Rst Smart Storage RST Smart Storage caching Bit.

\$EN\_DIS

Definition at line [1899](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataSalpSupport**

---

Offset 0x0041 - Enable SATA SALP Support Enable/disable SATA Aggressive Link Power Management.

\$EN\_DIS

Definition at line [167](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SataThermalSuggestedSetting**

---

Offset 0x072A - Sata Thermal Throttling Suggested Setting Sata Thermal Throttling Suggested Setting.

\$EN\_DIS

Definition at line [2162](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::ScilrqSelect**

---

Offset 0x0089 - Select ScilrqSelect SCI IRQ Select.

The valid value is 9, 10, 11, and 20, 21, 22, 23 for APIC only.

Definition at line [237](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::ScsEmmcEnabled**

---

Offset 0x0031 - Enable eMMC Controller Enable/disable eMMC Controller.

\$EN\_DIS

Definition at line [123](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::ScsEmmcHs400Enabled**

---

Offset 0x0032 - Enable eMMC HS400 Mode Enable eMMC HS400 Mode.

\$EN\_DIS

Definition at line [129](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::ScsSdCardEnabled**

---

Offset 0x0033 - Enable SdCard Controller Enable/disable SD Card Controller.

\$EN\_DIS

Definition at line [135](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::ScsUfsEnabled**

---

Offset 0x0145 - Enable Ufs Controller Enable/disable Ufs 2.0 Controller.

\$EN\_DIS

Definition at line [474](#) of file [FspUpd.h](#).

## **UINT64 FSP\_S\_CONFIG::SendEcCmd**

---

Offset 0x0785 - SendEcCmd SendEcCmd function pointer.

```
typedef EFI_STATUS (EFIAPI
    *PLATFORM_SEND_EC_COMMAND) (IN
        EC_COMMAND_TYPE
    EcCmdType, IN UINT8 EcCmd, IN UINT8 SendData,
    IN OUT UINT8 *ReceiveData);
```

Definition at line [2275](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SendVrMbxCmd**

---

Offset 0x0303 - Enable VR specific mailbox command VR specific mailbox commands.

**00b - no VR specific command sent.** 01b - A VR mailbox command specifically for the MPS IMPV8 VR will be sent. 10b - VR specific command sent for PS4 exit issue. 11b - Reserved. \$EN\_DIS

Definition at line [1022](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SerialIoDebugUartNumber**

---

Offset 0x0706 - UART Number For Debug Purpose UART number for debug purpose.

0:UART0, 1: UART1, 2:UART2. Note: If UART0 is selected as CNVi BT Core interface, it cannot be used for debug purpose. 0:UART0, 1:UART1, 2:UART2

Definition at line [1976](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SerialloDevMode[12]**

---

Offset 0x006F - Enable Seriallo Device Mode 0:Disabled, 1:PCI Mode, 2:Acpi mode, 3:Hidden mode (Legacy UART mode) - Enable/disable Seriallo I2C0,I2C1,I2C2,I2C3,I2C4,I2C5,SPI0,SPI1,SPI2,UART0,UART1,UART device mode respectively.

One byte for each controller, byte0 for I2C0, byte1 for I2C1, and so on.

Definition at line [209](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SerialloEnableDebugUartAfterPost**

---

Offset 0x0707 - Enable Debug UART Controller Enable debug UART controller after post.

\$EN\_DIS

Definition at line [1982](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SerialloUart0PinMuxing**

---

Offset 0x0701 - PcdSerialloUart0PinMuxing Select Seriallo Uart0 pin muxing.

Setting applicable only if SerialIO UART0 is enabled. 0:default pins, 1:pins muxed with CNV\_BRI/RGI

Definition at line [1960](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::ShowSpiController**

---

Offset 0x0034 - Show SPI controller Enable/disable to show SPI controller.

\$EN\_DIS

Definition at line [141](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SiCsmFlag**

---

Offset 0x07A0 - Si Config CSM Flag.

Platform specific common policies that used by several silicon components. CSM status flag. \$EN\_DIS

Definition at line [2306](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SkipMpInit**

---

Offset 0x030C - Deprecated DO NOT USE Skip Multi-Processor Initialization.

### **Deprecated:**

SkipMpInit has been moved to FspmUpd \$EN\_DIS

Definition at line [1043](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SlowSlewRateForFivr**

---

Offset 0x0314 - Slew Rate configuration for Deep Package C States for VR FIVR domain Slew Rate configuration for Deep Package C States for VR FIVR domain based on Acoustic Noise Mitigation feature enabled.

**0: Fast/2;** 1: Fast/4; 2: Fast/8; 3: Fast/16 0: Fast/2, 1: Fast/4, 2: Fast/8, 3: Fast/16

Definition at line [1088](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SlowSlewRateForGt**

---

Offset 0x02A5 - Slew Rate configuration for Deep Package C States for VR GT domain Slew Rate configuration for Deep Package C States for VR GT domain based on Acoustic Noise Mitigation feature enabled.

**0: Fast/2;** 1: Fast/4; 2: Fast/8; 3: Fast/16 0: Fast/2, 1: Fast/4, 2: Fast/8, 3: Fast/16

Definition at line [946](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SlowSlewRateForIa**

---

Offset 0x02A4 - Slew Rate configuration for Deep Package C States for VR IA domain Slew Rate configuration for Deep Package C States for VR IA domain based on Acoustic Noise Mitigation feature enabled.

**0: Fast/2;** 1: Fast/4; 2: Fast/8; 3: Fast/16 0: Fast/2, 1: Fast/4, 2: Fast/8, 3: Fast/16

Definition at line [939](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SlowSlewRateForSa**

---

Offset 0x02A6 - Slew Rate configuration for Deep Package C States for VR SA domain Slew Rate configuration for Deep Package C States for VR SA domain based on Acoustic Noise Mitigation feature enabled.

**0: Fast/2;** 1: Fast/4; 2: Fast/8; 3: Fast/16 0: Fast/2, 1: Fast/4, 2: Fast/8, 3: Fast/16

Definition at line [953](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SlpS0DisQForDebug**

---

Offset 0x067B - S0ix Override Settings Select 'Auto', it will be auto-configured according to probe type.

'No Change' will keep PMC default settings. Or select the desired debug probe type for S0ix Override settings.

Reminder: DCI OOB (aka BSSB) uses CCA probe.

Note: This BIOS option should keep 'Auto', other options are intended for advanced configuration only. 0:No Change, 1:DCI OOB, 2:USB2 DbC, 3:Auto

Definition at line [1680](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SlpS0Override**

---

Offset 0x067A - SLP\_S0# Override Select 'Auto', it will be auto-configured according to probe type.

Select 'Enabled' will disable SLP\_S0# assertion whereas 'Disabled' will enable SLP\_S0# assertion when debug is enabled.

Note: This BIOS option should keep 'Auto', other options are intended for advanced configuration only. 0:Disabled, 1:Enabled, 2:Auto

Definition at line [1669](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::SlpS0WithGbeSupport**

---

Offset 0x01FC - SlpS0WithGbeSupport Enable/Disable SLP\_S0 with GBE Support.

0: disable, 1: enable \$EN\_DIS

Definition at line [683](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::TcoIrqSelect**

---

Offset 0x008A - Select TcoIrqSelect TCO IRQ Select.

The valid value is 9, 10, 11, 20, 21, 22, 23.

Definition at line [242](#) of file [FspUpd.h](#).

## **UINT16 FSP\_S\_CONFIG::TdcPowerLimit[5]**

---

Offset 0x02A7 - Thermal Design Current current limit PCODE MMIO Mailbox: Thermal Design Current current limit.

Specified in 1/8A units. Range is 0-4095. 1000 = 125A. **0: Auto.** For all VR Indexes

Definition at line [959](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_CONFIG::TdcTimeWindow[5]**

---

Offset 0x0296 - HECI3 state PCODE MMIO Mailbox: Thermal Design Current time window.

Defined in milli seconds. Valid Values 1 - 1ms , 2 - 2ms , 3 - 3ms , 4 - 4ms , 5 - 5ms , 6 - 6ms , 7 - 7ms , 8 - 8ms , 10 - 10ms. For all VR Indexe

Definition at line [899](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::TetonGlacierCR**

---

Offset 0x0668 - Teton Glacier Cycle Router Specify to which cycle router Teton Glacier is connected, it is valid only when Teton Glacier support is enabled.

Default is 0 for CNP-H system and 1 for CNP-LP system

Definition at line [1576](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::TetonGlacierSupport**

---

Offset 0x0667 - Teton Glacier Support Enables support for the Teton Glacier card.

\$EN\_DIS

Definition at line [1570](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::TTSuggestedSetting**

---

Offset 0x0716 - Thermal Throttling Suggested Setting Thermal Throttling Suggested Setting.

\$EN\_DIS

Definition at line [2052](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::TurboMode**

---

Offset 0x0040 - Turbo Mode Enable/Disable Turbo mode.

0: disable, 1: enable \$EN\_DIS

Definition at line [161](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::TxtEnable**

---

Offset 0x0305 - Enable or Disable TXT Enable or Disable TXT; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line [1033](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::Usb2AfePehalfbit[16]**

---

Offset 0x00C4 - USB Per Port Half Bit Pre-emphasis USB Per Port Half Bit Pre-emphasis.

1b - half-bit pre-emphasis, 0b - full-bit pre-emphasis. One byte for each port.

Definition at line [299](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::Usb2AfePetxiset[16]**

---

Offset 0x0094 - USB Per Port HS Preemphasis Bias USB Per Port HS Preemphasis Bias.

000b-0mV, 001b-11.25mV, 010b-16.9mV, 011b-28.15mV, 100b-28.15mV, 101b-39.35mV, 110b-45mV, 111b-56.3mV. One byte for each port.

Definition at line [281](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::Usb2AfePredeemp[16]**

---

Offset 0x00B4 - USB Per Port HS Transmitter Emphasis USB Per

Port HS Transmitter Emphasis.

00b - Emphasis OFF, 01b - De-emphasis ON, 10b - Pre-emphasis ON, 11b - Pre-emphasis & De-emphasis ON. One byte for each port.

Definition at line [293](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::Usb2AfeTxiset[16]**

---

Offset 0x00A4 - USB Per Port HS Transmitter Bias USB Per Port HS Transmitter Bias.

000b-0mV, 001b-11.25mV, 010b-16.9mV, 011b-28.15mV, 100b-28.15mV, 101b-39.35mV, 110b-45mV, 111b-56.3mV, One byte for each port.

Definition at line [287](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::Usb3HsioTxDeEmph[10]**

---

Offset 0x00DE - USB 3.0 TX Output -3.5dB De-Emphasis Adjustment Setting USB 3.0 TX Output -3.5dB De-Emphasis Adjustment Setting, HSIO\_TX\_DWORD5[21:16], **Default = 29h** (approximately -3.5dB De-Emphasis).

One byte for each port.

Definition at line [311](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::Usb3HsioTxDeEmphEnable[10]**

---

Offset 0x00D4 - Enable the write to USB 3.0 TX Output -3.5dB De-Emphasis Adjustment Enable the write to USB 3.0 TX Output -3.5dB De-Emphasis Adjustment.

Each value in array can be between 0-1. One byte for each port.

Definition at line [305](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::Usb3HsioTxDownscaleAmp[10]**

---

Offset 0x00F2 - USB 3.0 TX Output Downscale Amplitude Adjustment USB 3.0 TX Output Downscale Amplitude Adjustment, HSIO\_TX\_DWORD8[21:16], **Default = 00h**.

One byte for each port.

Definition at line [323](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::Usb3HsioTxDownscaleAmpEnable[10]**

---

Offset 0x00E8 - Enable the write to USB 3.0 TX Output Downscale Amplitude Adjustment Enable the write to USB 3.0 TX Output Downscale Amplitude Adjustment, Each value in array can be between 0-1.

One byte for each port.

Definition at line [317](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::UsbPdoProgramming**

---

Offset 0x0114 - USB PDO Programming Enable/disable PDO programming for USB in PEI phase.

Disabling will allow for programming during later phase. 1: enable, 0: disable \$EN\_DIS

Definition at line [420](#) of file [FspUpd.h](#).

### **UINT32 FSP\_S\_CONFIG::VrPowerDeliveryDesign**

---

Offset 0x0324 - CPU VR Power Delivery Design Used to communicate the power delivery design capability of the board.

This value is an enum of the available power delivery segments that are defined in the Platform Design Guide.

Definition at line [1112](#) of file [FspUpd.h](#).

### **UINT16 FSP\_S\_CONFIG::VrVoltageLimit[5]**

---

Offset 0x02F7 - VR Voltage Limit PCODE MMIO Mailbox: VR Voltage Limit.

Range is 0-7999mV.

Definition at line [1000](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_CONFIG::WatchDog**

---

Offset 0x0156 - WatchDog Timer Switch Enable/Disable.

0: Disable, 1: enable, Enable or disable WatchDog timer. \$EN\_DIS

Definition at line [577](#) of file [FspUpd.h](#).

### **UINT16 FSP\_S\_CONFIG::WatchDogTimerBios**

---

Offset 0x015D - BIOS Timer 16 bits Value, Set BIOS watchdog timer.

\$EN\_DIS

Definition at line [614](#) of file [FspUpd.h](#).

## **UINT16 FSP\_S\_CONFIG::WatchDogTimerOs**

---

Offset 0x015B - OS Timer 16 bits Value, Set OS watchdog timer.

\$EN\_DIS

Definition at line **608** of file **FspUpd.h**.

---

## **UINT8 FSP\_S\_CONFIG::XdcEnable**

---

Offset 0x006C - Enable xDCI controller Enable/disable to xDCI controller.

\$EN\_DIS

Definition at line **197** of file **FspUpd.h**.

---

The documentation for this struct was generated from the following file:

- **FspUpd.h**
-



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

Main Page	Related Pages	Classes	Files
Class List	Class Index	Class Members	
<b>FSP_S_TEST_CONFIG</b> <b>Struct Reference</b>			<a href="#">Public Attributes</a>   <a href="#">List of all members</a>

Fsp S Test Configuration. [More...](#)

```
#include <FspSUpd.h>
```

## Public Attributes

UINT32 **Signature**

Offset 0x07AD.

UINT8 **ChapDeviceEnable**

Offset 0x07B1 - Enable/Disable Device 7 Enable: Device 7 enabled, Disable (Default): Device 7 disabled \$EN\_DIS.

UINT8 **SkipPamLock**

Offset 0x07B2 - Skip PAM register lock Enable: PAM register will not be locked by RC, platform code should lock it, Disable(Default): PAM registers will be locked by RC \$EN\_DIS.

UINT8 **EdramTestMode**

Offset 0x07B3 - EDRAM Test Mode Enable: PAM register will not be locked by RC, platform code should lock it, Disable(Default): PAM registers will be locked by RC 0: EDRAM SW disable, 1: EDRAM SW Enable, 2: EDRAM HW mode.

UINT8 **DmiExtSync**

Offset 0x07B4 - DMI Extended Sync Control Enable: Enable DMI Extended Sync Control, Disable(Default): Disable DMI Extended Sync Control \$EN\_DIS.

UINT8 **Dmilot**

Offset 0x07B5 - DMI IOT Control Enable: Enable DMI IOT Control, Disable(Default): Disable DMI IOT Control \$EN\_DIS.

UINT8 **PegMaxPayload [4]**

Offset 0x07B6 - PEG Max Payload size per root port  
0xFF(Default):Auto, 0x1: Force 128B, 0x2: Force 256B  
0xFF: Auto, 0x1: Force 128B, 0x2: Force 256B.

**UINT8 RenderStandby**

Offset 0x07BA - Enable/Disable IGFX RenderStandby  
Enable(Default): Enable IGFX RenderStandby, Disable:  
Disable IGFX RenderStandby \$EN\_DIS.

**UINT8 PmSupport**

Offset 0x07BB - Enable/Disable IGFX PmSupport  
Enable(Default): Enable IGFX PmSupport, Disable: Disable  
IGFX PmSupport \$EN\_DIS.

**UINT8 CdynmaxClampEnable**

Offset 0x07BC - Enable/Disable CdynmaxClamp  
Enable(Default): Enable CdynmaxClamp, Disable: Disable  
CdynmaxClamp \$EN\_DIS.

**UINT8 VtdDisable**

Offset 0x07BD - Disable VT-d 0=Enable/FALSE(VT-d  
enabled), 1=Disable/TRUE (VT-d disabled) \$EN\_DIS.

**UINT8 GtFreqMax**

Offset 0x07BE - GT Frequency Limit 0xFF: Auto(Default), 2:  
100 Mhz, 3: 150 Mhz, 4: 200 Mhz, 5: 250 Mhz, 6: 300 Mhz,  
7: 350 Mhz, 8: 400 Mhz, 9: 450 Mhz, 0xA: 500 Mhz, 0xB:  
550 Mhz, 0xC: 600 Mhz, 0xD: 650 Mhz, 0xE: 700 Mhz, 0xF:  
750 Mhz, 0x10: 800 Mhz, 0x11: 850 Mhz, 0x12: 900 Mhz,  
0x13: 950 Mhz, 0x14: 1000 Mhz, 0x15: 1050 Mhz, 0x16:  
1100 Mhz, 0x17: 1150 Mhz, 0x18: 1200 Mhz 0xFF:  
Auto(Default), 2: 100 Mhz, 3: 150 Mhz, 4: 200 Mhz, 5: 250  
Mhz, 6: 300 Mhz, 7: 350 Mhz, 8: 400 Mhz, 9: 450 Mhz, 0xA:  
500 Mhz, 0xB: 550 Mhz, 0xC: 600 Mhz, 0xD: 650 Mhz, 0xE:  
700 Mhz, 0xF: 750 Mhz, 0x10: 800 Mhz, 0x11: 850 Mhz,  
0x12: 900 Mhz, 0x13: 950 Mhz, 0x14: 1000 Mhz, 0x15: 1050  
Mhz, 0x16: 1100 Mhz, 0x17: 1150 Mhz, 0x18: 1200 Mhz.

**UINT8 DisableTurboGt**

Offset 0x07BF - Disable Turbo GT 0=Disable: GT frequency  
is not limited, 1=Enable: Disables Turbo GT frequency  
\$EN\_DIS.

**UINT8 [SaPostMemTestRsvd](#) [11]**

Offset 0x07C0 - SaPostMemTestRsvd Reserved for SA Post-Mem Test \$EN\_DIS.

**UINT8 [OneCoreRatioLimit](#)**

Offset 0x07CB - 1-Core Ratio Limit 1-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255. [More...](#)

**UINT8 [TwoCoreRatioLimit](#)**

Offset 0x07CC - 2-Core Ratio Limit 2-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255. [More...](#)

**UINT8 [ThreeCoreRatioLimit](#)**

Offset 0x07CD - 3-Core Ratio Limit 3-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255. [More...](#)

**UINT8 [FourCoreRatioLimit](#)**

Offset 0x07CE - 4-Core Ratio Limit 4-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255. [More...](#)

**UINT8 [Hwp](#)**

Offset 0x07CF - Enable or Disable HWP Enable or Disable HWP(Hardware P states) Support. [More...](#)

**UINT8 [HdcControl](#)**

Offset 0x07D0 - Hardware Duty Cycle Control Hardware Duty Cycle Control configuration. [More...](#)

**UINT8 [PowerLimit1Time](#)**

Offset 0x07D1 - Package Long duration turbo mode time Package Long duration turbo mode time window in seconds. [More...](#)

**UINT8 [PowerLimit2](#)**

Offset 0x07D2 - Short Duration Turbo Mode Enable or Disable short duration Turbo Mode. [More...](#)

**UINT8 TurboPowerLimitLock**  
Offset 0x07D3 - Turbo settings Lock Lock all Turbo settings Enable/Disable; **0: Disable** , 1: Enable \$EN\_DIS.

**UINT8 PowerLimit3Time**  
Offset 0x07D4 - Package PL3 time window Package PL3 time window range for this policy from 0 to 64ms.

**UINT8 PowerLimit3DutyCycle**  
Offset 0x07D5 - Package PL3 Duty Cycle Package PL3 Duty Cycle; Valid Range is 0 to 100.

**UINT8 PowerLimit3Lock**  
Offset 0x07D6 - Package PL3 Lock Package PL3 Lock Enable/Disable; **0: Disable** ; **1: Enable \$EN\_DIS**.

**UINT8 PowerLimit4Lock**  
Offset 0x07D7 - Package PL4 Lock Package PL4 Lock Enable/Disable; **0: Disable** ; **1: Enable \$EN\_DIS**.

**UINT8 TccActivationOffset**  
Offset 0x07D8 - TCC Activation Offset TCC Activation Offset. [More...](#)

**UINT8 TccOffsetClamp**  
Offset 0x07D9 - Tcc Offset Clamp Enable/Disable Tcc Offset Clamp for Runtime Average Temperature Limit (RATL) allows CPU to throttle below P1. For Y SKU, the recommended default for this policy is **1: Enabled**, For all other SKUs the recommended default are **0: Disabled**. [More...](#)

**UINT8 TccOffsetLock**  
Offset 0x07DA - Tcc Offset Lock Tcc Offset Lock for Runtime Average Temperature Limit (RATL) to lock temperature target; **0: Disabled**; 1: Enabled. [More...](#)

**UINT8 NumberOfEntries**

Offset 0x07DB - Custom Ratio State Entries The number of custom ratio state entries, ranges from 0 to 40 for a valid custom ratio table.Sets the number of custom P-states.

[More...](#)

**UINT8 Custom1PowerLimit1Time**

Offset 0x07DC - Custom Short term Power Limit time window Short term Power Limit time window value for custom CTDP level 1. [More...](#)

**UINT8 Custom1TurboActivationRatio**

Offset 0x07DD - Custom Turbo Activation Ratio Turbo Activation Ratio for custom cTDP level 1. [More...](#)

**UINT8 Custom1ConfigTdpControl**

Offset 0x07DE - Custom Config Tdp Control Config Tdp Control (0/1/2) value for custom cTDP level 1. [More...](#)

**UINT8 Custom2PowerLimit1Time**

Offset 0x07DF - Custom Short term Power Limit time window Short term Power Limit time window value for custom CTDP level 2. [More...](#)

**UINT8 Custom2TurboActivationRatio**

Offset 0x07E0 - Custom Turbo Activation Ratio Turbo Activation Ratio for custom cTDP level 2. [More...](#)

**UINT8 Custom2ConfigTdpControl**

Offset 0x07E1 - Custom Config Tdp Control Config Tdp Control (0/1/2) value for custom cTDP level 1. [More...](#)

**UINT8 Custom3PowerLimit1Time**

Offset 0x07E2 - Custom Short term Power Limit time window Short term Power Limit time window value for custom CTDP level 3. [More...](#)

**UINT8 Custom3TurboActivationRatio**

Offset 0x07E3 - Custom Turbo Activation Ratio Turbo Activation Ratio for custom cTDP level 3. [More...](#)

**UINT8 Custom3ConfigTdpControl**

Offset 0x07E4 - Custom Config Tdp Control Config Tdp Control (0/1/2) value for custom cTDP level 1. [More...](#)

**UINT8 ConfigTdpLock**

Offset 0x07E5 - ConfigTdp mode settings Lock Lock the ConfigTdp mode settings from runtime changes; **0: Disable**; **1: Enable \$EN\_DIS**.

**UINT8 ConfigTdpBios**

Offset 0x07E6 - Load Configurable TDP SSDT Configure whether to load Configurable TDP SSDT; **0: Disable**; **1: Enable**. [More...](#)

**UINT8 PsysPowerLimit1**

Offset 0x07E7 - PL1 Enable value PL1 Enable value to limit average platform power. [More...](#)

**UINT8 PsysPowerLimit1Time**

Offset 0x07E8 - PL1 timewindow PL1 timewindow in seconds. [More...](#)

**UINT8 PsysPowerLimit2**

Offset 0x07E9 - PL2 Enable Value PL2 Enable activates the PL2 value to limit average platform power. [More...](#)

**UINT8 MlcStreamerPrefetcher**

Offset 0x07EA - Enable or Disable MLC Streamer Prefetcher Enable or Disable MLC Streamer Prefetcher; **0: Disable**; **1: Enable**. [More...](#)

**UINT8 MlcSpatialPrefetcher**

Offset 0x07EB - Enable or Disable MLC Spatial Prefetcher  
Enable or Disable MLC Spatial Prefetcher; 0: Disable; **1: Enable** \$EN\_DIS.

UINT8 **MonitorMwaitEnable**

Offset 0x07EC - Enable or Disable Monitor /MWAIT  
instructions Enable or Disable Monitor /MWAIT instructions;  
0: Disable; **1: Enable**. [More...](#)

UINT8 **MachineCheckEnable**

Offset 0x07ED - Enable or Disable initialization of machine  
check registers Enable or Disable initialization of machine  
check registers; 0: Disable; **1: Enable**. [More...](#)

UINT8 **DebugInterfaceEnable**

Offset 0x07EE - Deprecated DO NOT USE Enable or  
Disable processor debug features. [More...](#)

UINT8 **DebugInterfaceLockEnable**

Offset 0x07EF - Lock or Unlock debug interface features  
Lock or Unlock debug interface features; 0: Disable; **1: Enable**. [More...](#)

UINT8 **ApIdleManner**

Offset 0x07F0 - AP Idle Manner of waiting for SIPI AP Idle  
Manner of waiting for SIPI; 1: HALT loop; **2: MWAIT loop**;  
3: RUN loop. [More...](#)

UINT8 **ProcessorTraceOutputScheme**

Offset 0x07F1 - Control on Processor Trace output scheme  
Control on Processor Trace output scheme; **0: Single Range Output**; 1: ToPA Output. [More...](#)

UINT8 **ProcessorTraceEnable**

Offset 0x07F2 - Enable or Disable Processor Trace feature  
Enable or Disable Processor Trace feature; **0: Disable**; 1:  
Enable. [More...](#)

- UINT64 ProcessorTraceMemBase**  
Offset 0x07F3 - Base of memory region allocated for Processor Trace Base address of memory region allocated for Processor Trace. [More...](#)
- UINT32 ProcessorTraceMemLength**  
Offset 0x07FB - Memory region allocation for Processor Trace Length in bytes of memory region allocated for Processor Trace. [More...](#)
- UINT8 VoltageOptimization**  
Offset 0x07FF - Enable or Disable Voltage Optimization feature  
Enable or Disable Voltage Optimization feature 0:  
**Disable; 1: Enable** \$EN\_DIS.
- UINT8 Eist**  
Offset 0x0800 - Enable or Disable Intel SpeedStep Technology  
Enable or Disable Intel SpeedStep Technology. [More...](#)
- UINT8 EnergyEfficientPState**  
Offset 0x0801 - Enable or Disable Energy Efficient P-state  
Enable or Disable Energy Efficient P-state will be applied in Turbo mode. [More...](#)
- UINT8 EnergyEfficientTurbo**  
Offset 0x0802 - Enable or Disable Energy Efficient Turbo  
Enable or Disable Energy Efficient Turbo, will be applied in Turbo mode. [More...](#)
- UINT8 TStates**  
Offset 0x0803 - Enable or Disable T states  
Enable or Disable T states; **0: Disable; 1: Enable.** [More...](#)
- UINT8 BiProcHot**  
Offset 0x0804 - Enable or Disable Bi-Directional

PROCHOT# Enable or Disable Bi-Directional PROCHOT#;  
0: Disable; **1: Enable** \$EN\_DIS.

UINT8 **DisableProcHotOut**

Offset 0x0805 - Enable or Disable PROCHOT# signal being driven externally  
Enable or Disable PROCHOT# signal being driven externally; 0: Disable; **1: Enable**. [More...](#)

UINT8 **ProcHotResponse**

Offset 0x0806 - Enable or Disable PROCHOT# Response  
Enable or Disable PROCHOT# Response; **0: Disable**; **1: Enable**. [More...](#)

UINT8 **DisableVrThermalAlert**

Offset 0x0807 - Enable or Disable VR Thermal Alert  
Enable or Disable VR Thermal Alert; **0: Disable**; **1: Enable**. [More...](#)

UINT8 **AutoThermalReporting**

Offset 0x0808 - Enable or Disable Thermal Reporting  
Enable or Disable Thermal Reporting through ACPI tables;  
0: Disable; **1: Enable**. [More...](#)

UINT8 **ThermalMonitor**

Offset 0x0809 - Enable or Disable Thermal Monitor  
Enable or Disable Thermal Monitor; 0: Disable; **1: Enable**  
\$EN\_DIS.

UINT8 **Cx**

Offset 0x080A - Enable or Disable CPU power states (C-states)  
Enable or Disable CPU power states (C-states).  
[More...](#)

UINT8 **PmgCstCfgCtrlLock**

Offset 0x080B - Configure C-State Configuration Lock  
Configure C-State Configuration Lock; 0: Disable; **1: Enable**. [More...](#)

**UINT8 C1e**

Offset 0x080C - Enable or Disable Enhanced C-states  
Enable or Disable Enhanced C-states. [More...](#)

**UINT8 PkgCStateDemotion**

Offset 0x080D - Enable or Disable Package Cstate  
Demotion Enable or Disable Package Cstate Demotion.  
[More...](#)

**UINT8 PkgCStateUnDemotion**

Offset 0x080E - Enable or Disable Package Cstate  
UnDemotion Enable or Disable Package Cstate  
UnDemotion. [More...](#)

**UINT8 CStatePreWake**

Offset 0x080F - Enable or Disable CState-Pre wake Enable  
or Disable CState-Pre wake. [More...](#)

**UINT8 TimedMwait**

Offset 0x0810 - Enable or Disable TimedMwait Support.  
[More...](#)

**UINT8 CstCfgCtrlIoMwaitRedirection**

Offset 0x0811 - Enable or Disable IO to MWAIT redirection  
Enable or Disable IO to MWAIT redirection; **0: Disable**; **1:**  
Enable. [More...](#)

**UINT8 PkgCStateLimit**

Offset 0x0812 - Set the Max Pkg Cstate Set the Max Pkg  
Cstate. [More...](#)

**UINT8 CstateLatencyControl0TimeUnit**

Offset 0x0813 - TimeUnit for C-State Latency Control0  
TimeUnit for C-State Latency Control0; Valid values 0 - 1ns  
, 1 - 32ns , 2 - 1024ns , 3 - 32768ns , 4 - 1048576ns , 5 -  
33554432ns.

**UINT8 CstateLatencyControl1TimeUnit**  
Offset 0x0814 - TimeUnit for C-State Latency Control1  
TimeUnit for C-State Latency Control1;Valid values 0 - 1ns ,  
1 - 32ns , 2 - 1024ns , 3 - 32768ns , 4 - 1048576ns , 5 -  
33554432ns.

**UINT8 CstateLatencyControl2TimeUnit**  
Offset 0x0815 - TimeUnit for C-State Latency Control2  
TimeUnit for C-State Latency Control2;Valid values 0 - 1ns ,  
1 - 32ns , 2 - 1024ns , 3 - 32768ns , 4 - 1048576ns , 5 -  
33554432ns.

**UINT8 CstateLatencyControl3TimeUnit**  
Offset 0x0816 - TimeUnit for C-State Latency Control3  
TimeUnit for C-State Latency Control3;Valid values 0 - 1ns ,  
1 - 32ns , 2 - 1024ns , 3 - 32768ns , 4 - 1048576ns , 5 -  
33554432ns.

**UINT8 CstateLatencyControl4TimeUnit**  
Offset 0x0817 - TimeUnit for C-State Latency Control4  
Time - 1ns , 1 - 32ns , 2 - 1024ns , 3 - 32768ns , 4 - 1048576ns ,  
5 - 33554432ns.

**UINT8 CstateLatencyControl5TimeUnit**  
Offset 0x0818 - TimeUnit for C-State Latency Control5  
TimeUnit for C-State Latency Control5;Valid values 0 - 1ns ,  
1 - 32ns , 2 - 1024ns , 3 - 32768ns , 4 - 1048576ns , 5 -  
33554432ns.

**UINT8 PpmIrmSetting**  
Offset 0x0819 - Interrupt Redirection Mode Select  
Interrupt Redirection Mode Select.0: Fixed priority; 1: Round robin;2:  
Hash vector;4: PAIR with fixed priority;5: PAIR with round  
robin;6: PAIR with hash vector;7: No change.

**UINT8 ProcHotLock**  
Offset 0x081A - Lock prochot configuration  
Lock prochot configuration Enable/Disable; 0: **Disable**; 1: **Enable**

\$EN\_DIS.

**UINT8 ConfigTdpLevel**

Offset 0x081B - Configuration for boot TDP selection  
Configuration for boot TDP selection; 0: **TDP Nominal**; 1:  
TDP Down; 2: TDP Up; 0xFF : Deactivate.

**UINT8 RaceToHalt**

Offset 0x081C - Race To Halt Enable/Disable Race To Halt  
feature. [More...](#)

**UINT8 MaxRatio**

Offset 0x081D - Max P-State Ratio Max P-State Ratio, Valid  
Range 0 to 0x7F.

**UINT8 StateRatio [40]**

Offset 0x081E - P-state ratios for custom P-state table P-  
state ratios for custom P-state table. [More...](#)

**UINT8 StateRatioMax16 [16]**

Offset 0x0846 - P-state ratios for max 16 version of custom  
P-state table P-state ratios for max 16 version of custom P-  
state table. [More...](#)

**UINT16 PsySPmax**

Offset 0x0856 - Platform Power Pmax PCODE MMIO  
Mailbox: Platform Power Pmax. [More...](#)

**UINT16 CstateLatencyControl0Irtl**

Offset 0x0858 - Interrupt Response Time Limit of C-State  
LatencyContol0 Interrupt Response Time Limit of C-State  
LatencyContol0.Range of value 0 to 0x3FF.

**UINT16 CstateLatencyControl1Irtl**

Offset 0x085A - Interrupt Response Time Limit of C-State  
LatencyContol1 Interrupt Response Time Limit of C-State  
LatencyContol1.Range of value 0 to 0x3FF.

**UINT16 CstateLatencyControl2Irtl**

Offset 0x085C - Interrupt Response Time Limit of C-State LatencyContol2 Interrupt Response Time Limit of C-State LatencyContol2.Range of value 0 to 0x3FF.

**UINT16 CstateLatencyControl3Irtl**

Offset 0x085E - Interrupt Response Time Limit of C-State LatencyContol3 Interrupt Response Time Limit of C-State LatencyContol3.Range of value 0 to 0x3FF.

**UINT16 CstateLatencyControl4Irtl**

Offset 0x0860 - Interrupt Response Time Limit of C-State LatencyContol4 Interrupt Response Time Limit of C-State LatencyContol4.Range of value 0 to 0x3FF.

**UINT16 CstateLatencyControl5Irtl**

Offset 0x0862 - Interrupt Response Time Limit of C-State LatencyContol5 Interrupt Response Time Limit of C-State LatencyContol5.Range of value 0 to 0x3FF.

**UINT32 PowerLimit1**

Offset 0x0864 - Package Long duration turbo mode power limit Package Long duration turbo mode power limit. [More...](#)

**UINT32 PowerLimit2Power**

Offset 0x0868 - Package Short duration turbo mode power limit Package Short duration turbo mode power limit. [More...](#)

**UINT32 PowerLimit3**

Offset 0x086C - Package PL3 power limit Package PL3 power limit. [More...](#)

**UINT32 PowerLimit4**

Offset 0x0870 - Package PL4 power limit Package PL4 power limit. [More...](#)

**UINT32 [TccOffsetTimeWindowForRatl](#)**

Offset 0x0874 - Tcc Offset Time Window for RATL Package PL4 power limit. [More...](#)

**UINT32 [Custom1PowerLimit1](#)**

Offset 0x0878 - Short term Power Limit value for custom cTDP level 1 Short term Power Limit value for custom cTDP level 1. [More...](#)

**UINT32 [Custom1PowerLimit2](#)**

Offset 0x087C - Long term Power Limit value for custom cTDP level 1 Long term Power Limit value for custom cTDP level 1. [More...](#)

**UINT32 [Custom2PowerLimit1](#)**

Offset 0x0880 - Short term Power Limit value for custom cTDP level 2 Short term Power Limit value for custom cTDP level 2. [More...](#)

**UINT32 [Custom2PowerLimit2](#)**

Offset 0x0884 - Long term Power Limit value for custom cTDP level 2 Long term Power Limit value for custom cTDP level 2. [More...](#)

**UINT32 [Custom3PowerLimit1](#)**

Offset 0x0888 - Short term Power Limit value for custom cTDP level 3 Short term Power Limit value for custom cTDP level 3. [More...](#)

**UINT32 [Custom3PowerLimit2](#)**

Offset 0x088C - Long term Power Limit value for custom cTDP level 3 Long term Power Limit value for custom cTDP level 3. [More...](#)

**UINT32 [PsysPowerLimit1Power](#)**

Offset 0x0890 - Platform PL1 power Platform PL1 power. [More...](#)

**UINT32 [PsysPowerLimit2Power](#)**

Offset 0x0894 - Platform PL2 power Platform PL2 power.  
[More...](#)

**UINT8 [ThreeStrikeCounterDisable](#)**

Offset 0x0898 - Set Three Strike Counter Disable False (default): Three Strike counter will be incremented and True: Prevents Three Strike counter from incrementing; 0: **False**; 1: True. [More...](#)

**UINT8 [HwlInterruptControl](#)**

Offset 0x0899 - Set HW P-State Interrupts Enabled for for MISC\_PWR\_MGMT Set HW P-State Interrupts Enabled for for MISC\_PWR\_MGMT; 0: **Disable**; 1: Enable. [More...](#)

**UINT8 [FiveCoreRatioLimit](#)**

Offset 0x089A - 5-Core Ratio Limit 5-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255. [More...](#)

**UINT8 [SixCoreRatioLimit](#)**

Offset 0x089B - 6-Core Ratio Limit 6-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255. [More...](#)

**UINT8 [SevenCoreRatioLimit](#)**

Offset 0x089C - 7-Core Ratio Limit 7-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255. [More...](#)

**UINT8 [EightCoreRatioLimit](#)**

Offset 0x089D - 8-Core Ratio Limit 8-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255. [More...](#)

**UINT8 [Enableltbm](#)**

Offset 0x089E - Intel Turbo Boost Max Technology 3.0 Intel Turbo Boost Max Technology 3.0. [More...](#)

**UINT8 [EnableltbmDriver](#)**

Offset 0x089F - Intel Turbo Boost Max Technology 3.0  
Driver Intel Turbo Boost Max Technology 3.0 Driver 0:  
**Disabled**; 1: Enabled \$EN\_DIS.

UINT8 **C1StateAutoDemotion**

Offset 0x08A0 - Enable or Disable C1 Cstate Demotion  
Enable or Disable C1 Cstate Demotion. [More...](#)

UINT8 **C1StateUnDemotion**

Offset 0x08A1 - Enable or Disable C1 Cstate UnDemotion  
Enable or Disable C1 Cstate UnDemotion. [More...](#)

UINT8 **CpuWakeUpTimer**

Offset 0x08A2 - CpuWakeUpTimer Enable long CPU  
Wakeup Timer. [More...](#)

UINT8 **MinRingRatioLimit**

Offset 0x08A3 - Minimum Ring ratio limit override Minimum  
Ring ratio limit override. [More...](#)

UINT8 **MaxRingRatioLimit**

Offset 0x08A4 - Minimum Ring ratio limit override Maximum  
Ring ratio limit override. [More...](#)

UINT8 **C3StateAutoDemotion**

Offset 0x08A5 - Enable or Disable C3 Cstate Demotion  
Enable or Disable C3 Cstate Demotion. [More...](#)

UINT8 **C3StateUnDemotion**

Offset 0x08A6 - Enable or Disable C3 Cstate UnDemotion  
Enable or Disable C3 Cstate UnDemotion. [More...](#)

UINT8 **ReservedCpuPostMemTest [19]**

Offset 0x08A7 - ReservedCpuPostMemTest Reserved for  
CPU Post-Mem Test \$EN\_DIS.

UINT8 **SgxSinitDataFromTpm**

Offset 0x08BA - SgxSinitDataFromTpm  
SgxSinitDataFromTpm default values.

UINT8 **EndOfPostMessage**

Offset 0x08BB - End of Post message Test, Send End of Post message. [More...](#)

UINT8 **DisableD0I3SettingForHeci**

Offset 0x08BC - D0I3 Setting for HECI Disable Test, 0: disable, 1: enable, Setting this option disables setting D0I3 bit for all HECI devices \$EN\_DIS.

UINT16 **PchHdaResetWaitTimer**

Offset 0x08BD - HD Audio Reset Wait Timer The delay timer after Azalia reset, the value is number of microseconds. [More...](#)

UINT8 **PchLockDownGlobalSmi**

Offset 0x08BF - Enable LOCKDOWN SMI Enable SMI\_LOCK bit to prevent writes to the Global SMI Enable bit. [More...](#)

UINT8 **PchLockDownBiosInterface**

Offset 0x08C0 - Enable LOCKDOWN BIOS Interface Enable BIOS Interface Lock Down bit to prevent writes to the Backup Control Register. [More...](#)

UINT8 **PchUnlockGpioPads**

Offset 0x08C1 - Unlock all GPIO pads Force all GPIO pads to be unlocked for debug purpose. [More...](#)

UINT8 **PchSbiUnlock**

Offset 0x08C2 - PCH Unlock SBI access Deprecated \$EN\_DIS.

UINT8 **PchSbAccessUnlock**

Offset 0x08C3 - PCH Unlock SideBand access The SideBand PortID mask for certain end point (e.g. More...)

UINT16 **PcieRpLtrMaxSnoopLatency** [24]  
Offset 0x08C4 - PCIE RP Ltr Max Snoop Latency Latency Tolerance Reporting, Max Snoop Latency.

UINT16 **PcieRpLtrMaxNoSnoopLatency** [24]  
Offset 0x08F4 - PCIE RP Ltr Max No Snoop Latency Latency Tolerance Reporting, Max Non-Snoop Latency.

UINT8 **PcieRpSnoopLatencyOverrideMode** [24]  
Offset 0x0924 - PCIE RP Snoop Latency Override Mode Latency Tolerance Reporting, Snoop Latency Override Mode.

UINT8 **PcieRpSnoopLatencyOverrideMultiplier** [24]  
Offset 0x093C - PCIE RP Snoop Latency Override Multiplier Latency Tolerance Reporting, Snoop Latency Override Multiplier.

UINT16 **PcieRpSnoopLatencyOverrideValue** [24]  
Offset 0x0954 - PCIE RP Snoop Latency Override Value Latency Tolerance Reporting, Snoop Latency Override Value.

UINT8 **PcieRpNonSnoopLatencyOverrideMode** [24]  
Offset 0x0984 - PCIE RP Non Snoop Latency Override Mode Latency Tolerance Reporting, Non-Snoop Latency Override Mode.

UINT8 **PcieRpNonSnoopLatencyOverrideMultiplier** [24]  
Offset 0x099C - PCIE RP Non Snoop Latency Override Multiplier Latency Tolerance Reporting, Non-Snoop Latency Override Multiplier.

**UINT16 [PcieRpNonSnoopLatencyOverrideValue](#) [24]**  
Offset 0x09B4 - PCIE RP Non Snoop Latency Override Value Latency Tolerance Reporting, Non-Snoop Latency Override Value.

**UINT8 [PcieRpSlotPowerLimitScale](#) [24]**  
Offset 0x09E4 - PCIE RP Slot Power Limit Scale Specifies scale used for slot power limit value. [More...](#)

**UINT16 [PcieRpSlotPowerLimitValue](#) [24]**  
Offset 0x09FC - PCIE RP Slot Power Limit Value Specifies upper limit on power supplie by slot. [More...](#)

**UINT8 [PcieRpUptp](#) [24]**  
Offset 0x0A2C - PCIE RP Upstream Port Transmiter Preset Used during Gen3 Link Equalization. [More...](#)

**UINT8 [PcieRpDptp](#) [24]**  
Offset 0x0A44 - PCIE RP Downstream Port Transmiter Preset Used during Gen3 Link Equalization. [More...](#)

**UINT8 [PcieEnablePort8xhDecode](#)**  
Offset 0x0A5C - PCIE RP Enable Port8xh Decode This member describes whether PCIE root port Port 8xh Decode is enabled. [More...](#)

**UINT8 [PchPciePort8xhDecodePortIndex](#)**  
Offset 0x0A5D - PCIE Port8xh Decode Port Index The Index of PCIe Port that is selected for Port8xh Decode (0 Based).

**UINT8 [PchPmDisableEnergyReport](#)**  
Offset 0x0A5E - PCH Energy Reporting Disable/Enable PCH to CPU energy report feature. [More...](#)

**UINT8 [SataTestMode](#)**

Offset 0x0A5F - PCH SATA Test Mode Allow entrance to the PCH SATA test modes. [More...](#)

**UINT8 [PchXhciOcLock](#)**

Offset 0x0A60 - PCH USB OverCurrent mapping lock enable If this policy option is enabled then BIOS will program OCCFDONE bit in xHCI meaning that OC mapping data will be consumed by xHCI and OC mapping registers will be locked. [More...](#)

**UINT8 [UnusedUpdSpace24](#) [17]**

Offset 0x0A61.

**UINT8 [SkipPostBootSai](#)**

Offset 0x0A72 - Skip POSTBOOT SAI Deprecated \$EN\_DIS.

**UINT8 [MctpBroadcastCycle](#)**

Offset 0x0A73 - Mctp Broadcast Cycle Test, Determine if MCTP Broadcast is enabled 0: **Disable**; 1: Enable. [More...](#)

**UINT8 [ReservedFspsTestUpd](#) [12]**

Offset 0x0A74.

## Detailed Description

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Fsp S Test Configuration.

Definition at line **2358** of file **FspsUpd.h**.

## Member Data Documentation

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### **UINT8 FSP\_S\_TEST\_CONFIG::ApIdleManner**

---

Offset 0x07F0 - AP Idle Manner of waiting for SIPI AP Idle Manner of waiting for SIPI; 1: HALT loop; **2: MWAIT loop**; 3: RUN loop.

1: HALT loop, 2: MWAIT loop, 3: RUN loop

Definition at line [2681](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::AutoThermalReporting**

---

Offset 0x0808 - Enable or Disable Thermal Reporting Enable or Disable Thermal Reporting through ACPI tables; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line [2767](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::C1e**

---

Offset 0x080C - Enable or Disable Enhanced C-states Enable or Disable Enhanced C-states.

0: Disable; **1: Enable** \$EN\_DIS

Definition at line [2791](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::C1StateAutoDemotion**

---

Offset 0x08A0 - Enable or Disable C1 Cstate Demotion Enable or Disable C1 Cstate Demotion.

Disable; **1: Enable \$EN\_DIS**

Definition at line [3083](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::C1StateUnDemotion**

---

Offset 0x08A1 - Enable or Disable C1 Cstate UnDemotion Enable or Disable C1 Cstate UnDemotion.

Disable; **1: Enable \$EN\_DIS**

Definition at line [3089](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::C3StateAutoDemotion**

---

Offset 0x08A5 - Enable or Disable C3 Cstate Demotion Enable or Disable C3 Cstate Demotion.

Disable; **1: Enable \$EN\_DIS**

Definition at line [3114](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::C3StateUnDemotion**

---

Offset 0x08A6 - Enable or Disable C3 Cstate UnDemotion Enable or Disable C3 Cstate UnDemotion.

Disable; **1: Enable \$EN\_DIS**

Definition at line [3120](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::ConfigTdpBios**

---

Offset 0x07E6 - Load Configurable TDP SSDT Configure whether to load Configurable TDP SSDT; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line [2620](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::CpuWakeUpTimer**

---

Offset 0x08A2 - CpuWakeUpTimer Enable long CPU Wakeup Timer.

When enabled, the cpu internal wakeup time is increased to 180 seconds. 0: Disable; **1: Enable** \$EN\_DIS

Definition at line [3096](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::CStatePreWake**

---

Offset 0x080F - Enable or Disable CState-Pre wake Enable or Disable CState-Pre wake.

0: Disable; **1: Enable** \$EN\_DIS

Definition at line [2809](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::CstCfgCtrlIoMwaitRedirection**

---

Offset 0x0811 - Enable or Disable IO to MWAIT redirection Enable or Disable IO to MWAIT redirection; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line [2821](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::Custom1ConfigTdpControl**

---

Offset 0x07DE - Custom Config Tdp Control Config Tdp Control (0/1/2) value for custom cTDP level 1.

Valid Range is 0 to 2

Definition at line [2576](#) of file [FspUpd.h](#).

## **UINT32 FSP\_S\_TEST\_CONFIG::Custom1PowerLimit1**

---

Offset 0x0878 - Short term Power Limit value for custom cTDP level 1 Short term Power Limit value for custom cTDP level 1.

Units are based on

POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line [2982](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::Custom1PowerLimit1Time**

---

Offset 0x07DC - Custom Short term Power Limit time window Short term Power Limit time window value for custom CTDP level 1.

Valid Range 0 to 128, 0 = AUTO

Definition at line [2566](#) of file [FspUpd.h](#).

## **UINT32 FSP\_S\_TEST\_CONFIG::Custom1PowerLimit2**

---

Offset 0x087C - Long term Power Limit value for custom cTDP level 1 Long term Power Limit value for custom cTDP level 1.

Units are based on

`POWER_MGMT_CONFIG.CustomPowerUnit`.Valid Range 0 to 4095875 in Step size of 125

Definition at line [2988](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::Custom1TurboActivationRatio**

---

Offset 0x07DD - Custom Turbo Activation Ratio Turbo Activation Ratio for custom cTDP level 1.

Valid Range 0 to 255

Definition at line [2571](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::Custom2ConfigTdpControl**

---

Offset 0x07E1 - Custom Config Tdp Control Config Tdp Control (0/1/2) value for custom cTDP level 1.

Valid Range is 0 to 2

Definition at line [2592](#) of file [FspUpd.h](#).

### **UINT32 FSP\_S\_TEST\_CONFIG::Custom2PowerLimit1**

---

Offset 0x0880 - Short term Power Limit value for custom cTDP level 2 Short term Power Limit value for custom cTDP level 2.

Units are based on

`POWER_MGMT_CONFIG.CustomPowerUnit`.Valid Range 0 to 4095875 in Step size of 125

Definition at line [2994](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::Custom2PowerLimit1Time**

---

Offset 0x07DF - Custom Short term Power Limit time window Short term Power Limit time window value for custom CTDP level 2.

Valid Range 0 to 128, 0 = AUTO

Definition at line [2582](#) of file [FspsUpd.h](#).

### **UINT32 FSP\_S\_TEST\_CONFIG::Custom2PowerLimit2**

---

Offset 0x0884 - Long term Power Limit value for custom cTDP level 2 Long term Power Limit value for custom cTDP level 2.

Units are based on

POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line [3000](#) of file [FspsUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::Custom2TurboActivationRatio**

---

Offset 0x07E0 - Custom Turbo Activation Ratio Turbo Activation Ratio for custom cTDP level 2.

Valid Range 0 to 255

Definition at line [2587](#) of file [FspsUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::Custom3ConfigTdpControl**

---

Offset 0x07E4 - Custom Config Tdp Control Config Tdp Control (0/1/2) value for custom cTDP level 1.

Valid Range is 0 to 2

Definition at line [2608](#) of file [FspsUpd.h](#).

## **UINT32 FSP\_S\_TEST\_CONFIG::Custom3PowerLimit1**

---

Offset 0x0888 - Short term Power Limit value for custom cTDP level 3 Short term Power Limit value for custom cTDP level 3.

Units are based on

POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line [3006](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::Custom3PowerLimit1Time**

---

Offset 0x07E2 - Custom Short term Power Limit time window Short term Power Limit time window value for custom CTDP level 3.

Valid Range 0 to 128, 0 = AUTO

Definition at line [2598](#) of file [FspUpd.h](#).

## **UINT32 FSP\_S\_TEST\_CONFIG::Custom3PowerLimit2**

---

Offset 0x088C - Long term Power Limit value for custom cTDP level 3 Long term Power Limit value for custom cTDP level 3.

Units are based on

POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line [3012](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::Custom3TurboActivationRatio**

---

Offset 0x07E3 - Custom Turbo Activation Ratio Turbo Activation Ratio for custom cTDP level 3.

Valid Range 0 to 255

Definition at line [2603](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::Cx**

---

Offset 0x080A - Enable or Disable CPU power states (C-states)  
Enable or Disable CPU power states (C-states).

0: Disable; **1: Enable** \$EN\_DIS

Definition at line [2779](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::DebugInterfaceEnable**

---

Offset 0x07EE - Deprecated DO NOT USE Enable or Disable processor debug features.

### **Deprecated:**

Enable or Disable processor debug features; **0: Disable**; **1: Enable**. \$EN\_DIS

Definition at line [2669](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::DebugInterfaceLockEnable**

---

Offset 0x07EF - Lock or Unlock debug interface features Lock or Unlock debug interface features; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line [2675](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::DisableProcHotOut**

---

Offset 0x0805 - Enable or Disable PROCHOT# signal being driven externally  
Enable or Disable PROCHOT# signal being driven externally; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line [2749](#) of file [FspUpd.h](#).

## UINT8 FSP\_S\_TEST\_CONFIG::DisableVrThermalAlert

---

Offset 0x0807 - Enable or Disable VR Thermal Alert Enable or Disable VR Thermal Alert; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line [2761](#) of file [FspUpd.h](#).

## UINT8 FSP\_S\_TEST\_CONFIG::EightCoreRatioLimit

---

Offset 0x089D - 8-Core Ratio Limit 8-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255.

This 8-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit. Range is 0 to 255 0x0:0xFF

Definition at line [3065](#) of file [FspUpd.h](#).

## UINT8 FSP\_S\_TEST\_CONFIG::Eist

---

Offset 0x0800 - Enable or Disable Intel SpeedStep Technology  
Enable or Disable Intel SpeedStep Technology.

0: Disable; **1: Enable** \$EN\_DIS

Definition at line [2717](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::EnableItbm**

---

Offset 0x089E - Intel Turbo Boost Max Technology 3.0 Intel Turbo Boost Max Technology 3.0.

0: Disabled; **1: Enabled \$EN\_DIS**

Definition at line [3071](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::EndOfPostMessage**

---

Offset 0x08BB - End of Post message Test, Send End of Post message.

Disable(0x0): Disable EOP message, Send in PEI(0x1): EOP send in PEI, Send in DXE(0x2)(Default): EOP send in PEI 0:Disable, 1:Send in PEI, 2:Send in DXE, 3:Reserved

Definition at line [3138](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::EnergyEfficientPState**

---

Offset 0x0801 - Enable or Disable Energy Efficient P-state Enable or Disable Energy Efficient P-state will be applied in Turbo mode.

Disable; **1: Enable \$EN\_DIS**

Definition at line [2724](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::EnergyEfficientTurbo**

---

Offset 0x0802 - Enable or Disable Energy Efficient Turbo Enable or Disable Energy Efficient Turbo, will be applied in Turbo mode.

Disable; **1: Enable \$EN\_DIS**

Definition at line [2731](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::FiveCoreRatioLimit**

---

Offset 0x089A - 5-Core Ratio Limit 5-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255.

This 5-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit. Range is 0 to 255 0x0:0xFF

Definition at line [3044](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::FourCoreRatioLimit**

---

Offset 0x07CE - 4-Core Ratio Limit 4-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255.

This 4-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit. Range is 0 to 255

Definition at line [2477](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::HdcControl**

---

Offset 0x07D0 - Hardware Duty Cycle Control Hardware Duty Cycle Control configuration.

0: Disabled; **1: Enabled** 2-3:Reserved \$EN\_DIS

Definition at line [2490](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::Hwp**

---

Offset 0x07CF - Enable or Disable HWP Enable or Disable HWP(Hardware P states) Support.

0: Disable; **1: Enable**; 2-3:Reserved \$EN\_DIS

Definition at line [2484](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::HwpInterruptControl**

---

Offset 0x0899 - Set HW P-State Interrupts Enabled for for  
MISC\_PWR\_MGMT Set HW P-State Interrupts Enabled for for  
MISC\_PWR\_MGMT; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line [3037](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::MachineCheckEnable**

---

Offset 0x07ED - Enable or Disable initialization of machine check  
registers Enable or Disable initialization of machine check registers;  
0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line [2663](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::MaxRingRatioLimit**

---

Offset 0x08A4 - Minimum Ring ratio limit override Maximum Ring  
ratio limit override.

**0: Hardware defaults.** Range: 0 - Max turbo ratio limit

Definition at line [3108](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::MctpBroadcastCycle**

---

Offset 0x0A73 - Mctp Broadcast Cycle Test, Determine if MCTP Broadcast is enabled **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line [3288](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::MinRingRatioLimit**

---

Offset 0x08A3 - Minimum Ring ratio limit override Minimum Ring ratio limit override.

**0: Hardware defaults.** Range: 0 - Max turbo ratio limit

Definition at line [3102](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::MLCStreamerPrefetcher**

---

Offset 0x07EA - Enable or Disable MLC Streamer Prefetcher Enable or Disable MLC Streamer Prefetcher; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line [2645](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::MonitorMwaitEnable**

---

Offset 0x07EC - Enable or Disable Monitor /MWAIT instructions Enable or Disable Monitor /MWAIT instructions; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line [2657](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::NumberOfEntries**

---

Offset 0x07DB - Custom Ratio State Entries The number of custom ratio state entries, ranges from 0 to 40 for a valid custom ratio table. Sets the number of custom P-states.

At least 2 states must be present

Definition at line [2560](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::OneCoreRatioLimit**

---

Offset 0x07CB - 1-Core Ratio Limit 1-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255.

This 1-Core Ratio Limit Must be greater than or equal to 2-Core Ratio Limit, 3-Core Ratio Limit, 4-Core Ratio Limit, 5-Core Ratio Limit, 6-Core Ratio Limit, 7-Core Ratio Limit, 8-Core Ratio Limit. Range is 0 to 255

Definition at line [2459](#) of file [FspUpd.h](#).

## **UINT16 FSP\_S\_TEST\_CONFIG::PchHdaResetWaitTimer**

---

Offset 0x08BD - HD Audio Reset Wait Timer The delay timer after Azalia reset, the value is number of microseconds.

Default is 600.

Definition at line [3150](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::PchLockDownBiosInterface**

---

Offset 0x08C0 - Enable LOCKDOWN BIOS Interface Enable BIOS Interface Lock Down bit to prevent writes to the Backup Control Register.

`$EN_DIS`

Definition at line [3162](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::PchLockDownGlobalSmi**

---

Offset 0x08BF - Enable LOCKDOWN SMI Enable SMI\_LOCK bit to prevent writes to the Global SMI Enable bit.

`$EN_DIS`

Definition at line [3156](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::PchPmDisableEnergyReport**

---

Offset 0x0A5E - PCH Energy Reporting Disable/Enable PCH to CPU energy report feature.

`$EN_DIS`

Definition at line [3259](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::PchSbAccessUnlock**

---

Offset 0x08C3 - PCH Unlock SideBand access The SideBand PortID mask for certain end point (e.g.

PSFx) will be locked before 3rd party code execution. 0: Lock SideBand access; 1: Unlock SideBand access. `$EN_DIS`

Definition at line [3181](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::PchUnlockGpioPads**

---

Offset 0x08C1 - Unlock all GPIO pads Force all GPIO pads to be

unlocked for debug purpose.

\$EN\_DIS

Definition at line [3168](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::PchXhciOcLock**

---

Offset 0x0A60 - PCH USB OverCurrent mapping lock enable If this policy option is enabled then BIOS will program OCCFDONE bit in xHCI meaning that OC mapping data will be consumed by xHCI and OC mapping registers will be locked.

\$EN\_DIS

Definition at line [3272](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::PcieEnablePort8xhDecode**

---

Offset 0x0A5C - PCIE RP Enable Port8xh Decode This member describes whether PCIE root port Port 8xh Decode is enabled.

0: Disable; 1: Enable. \$EN\_DIS

Definition at line [3248](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::PcieRpDptp[24]**

---

Offset 0x0A44 - PCIE RP Downstream Port Transmter Preset Used during Gen3 Link Equalization.

Used for all lanes. Default is 7.

Definition at line [3241](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::PcieRpSlotPowerLimitScale[24]**

---

Offset 0x09E4 - PCIE RP Slot Power Limit Scale Specifies scale used for slot power limit value.

Leave as 0 to set to default.

Definition at line [3226](#) of file [FspUpd.h](#).

## **UINT16 FSP\_S\_TEST\_CONFIG::PcieRpSlotPowerLimitValue[24]**

---

Offset 0x09FC - PCIE RP Slot Power Limit Value Specifies upper limit on power supplie by slot.

Leave as 0 to set to default.

Definition at line [3231](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::PcieRpUptp[24]**

---

Offset 0x0A2C - PCIE RP Upstream Port Transmiter Preset Used during Gen3 Link Equalization.

Used for all lanes. Default is 5.

Definition at line [3236](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::PkgCStateDemotion**

---

Offset 0x080D - Enable or Disable Package Cstate Demotion  
Enable or Disable Package Cstate Demotion.

**0: Disable; 1: Enable** \$EN\_DIS

Definition at line [2797](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::PkgCStateLimit**

---

Offset 0x0812 - Set the Max Pkg Cstate Set the Max Pkg Cstate.

Default set to Auto which limits the Max Pkg Cstate to deep C-state.  
Valid values 0 - C0/C1 , 1 - C2 , 2 - C3 , 3 - C6 , 4 - C7 , 5 - C7S , 6 - C8 , 7 - C9 , 8 - C10 , 254 - CPU Default , 255 - Auto

Definition at line [2828](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::PkgCStateUnDemotion**

---

Offset 0x080E - Enable or Disable Package Cstate UnDemotion  
Enable or Disable Package Cstate UnDemotion.

**0: Disable; 1: Enable** \$EN\_DIS

Definition at line [2803](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::PmgCstCfgCtrlLock**

---

Offset 0x080B - Configure C-State Configuration Lock Configure C-State Configuration Lock; 0: Disable; **1: Enable**.

\$EN\_DIS

Definition at line [2785](#) of file [FspUpd.h](#).

## **UINT32 FSP\_S\_TEST\_CONFIG::PowerLimit1**

---

Offset 0x0864 - Package Long duration turbo mode power limit  
Package Long duration turbo mode power limit.

Units are based on POWER\_MGMT\_CONFIG.CustomPowerUnit.  
Valid Range 0 to 4095875 in Step size of 125

Definition at line [2952](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::PowerLimit1Time**

---

Offset 0x07D1 - Package Long duration turbo mode time Package Long duration turbo mode time window in seconds.

0 = AUTO, uses 28 seconds. Valid values(Unit in seconds) 1 to 8 , 10 , 12 ,14 , 16 , 20 , 24 , 28 , 32 , 40 , 48 , 56 , 64 , 80 , 96 , 112 , 128

Definition at line [2497](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::PowerLimit2**

---

Offset 0x07D2 - Short Duration Turbo Mode Enable or Disable short duration Turbo Mode.

0 : Disable; 1: **Enable** \$EN\_DIS

Definition at line [2503](#) of file [FspUpd.h](#).

## **UINT32 FSP\_S\_TEST\_CONFIG::PowerLimit2Power**

---

Offset 0x0868 - Package Short duration turbo mode power limit Package Short duration turbo mode power limit.

Units are based on  
POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line [2958](#) of file [FspUpd.h](#).

## **UINT32 FSP\_S\_TEST\_CONFIG::PowerLimit3**

---

Offset 0x086C - Package PL3 power limit Package PL3 power limit.

Units are based on

POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to  
4095875 in Step size of 125

Definition at line [2964](#) of file [FspUpd.h](#).

### **UINT32 FSP\_S\_TEST\_CONFIG::PowerLimit4**

---

Offset 0x0870 - Package PL4 power limit Package PL4 power limit.

Units are based on

POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to  
1023875 in Step size of 125

Definition at line [2970](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::ProcessorTraceEnable**

---

Offset 0x07F2 - Enable or Disable Processor Trace feature Enable  
or Disable Processor Trace feature; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line [2693](#) of file [FspUpd.h](#).

### **UINT64 FSP\_S\_TEST\_CONFIG::ProcessorTraceMemBase**

---

Offset 0x07F3 - Base of memory region allocated for Processor  
Trace Base address of memory region allocated for Processor  
Trace.

Processor Trace requires 2^N alignment and size in bytes per  
thread, from 4KB to 128MB. **0: Disable**

Definition at line [2699](#) of file [FspUpd.h](#).

### **UINT32 FSP\_S\_TEST\_CONFIG::ProcessorTraceMemLength**

---

Offset 0x07FB - Memory region allocation for Processor Trace Length in bytes of memory region allocated for Processor Trace.

Processor Trace requires  $2^N$  alignment and size in bytes per thread, from 4KB to 128MB. **0: Disable**

Definition at line [2705](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::ProcessorTraceOutputScheme**

---

Offset 0x07F1 - Control on Processor Trace output scheme Control on Processor Trace output scheme; **0: Single Range Output; 1: ToPA Output.**

0: Single Range Output, 1: ToPA Output

Definition at line [2687](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::ProcHotResponse**

---

Offset 0x0806 - Enable or Disable PROCHOT# Response Enable or Disable PROCHOT# Response; **0: Disable; 1: Enable.**

\$EN\_DIS

Definition at line [2755](#) of file [FspUpd.h](#).

### **UINT16 FSP\_S\_TEST\_CONFIG::PsysPmax**

---

Offset 0x0856 - Platform Power Pmax PCODE MMIO Mailbox: Platform Power Pmax.

**0 - Auto** Specified in 1/8 Watt increments. Range 0-1024 Watts.  
Value of 800 = 100W

Definition at line [2916](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::PsysPowerLimit1**

---

Offset 0x07E7 - PL1 Enable value PL1 Enable value to limit average platform power.

**0: Disable; 1: Enable.** \$EN\_DIS

Definition at line [2626](#) of file [FspUpd.h](#).

### **UINT32 FSP\_S\_TEST\_CONFIG::PsysPowerLimit1Power**

---

Offset 0x0890 - Platform PL1 power Platform PL1 power.

Units are based on  
POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to  
4095875 in Step size of 125

Definition at line [3018](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::PsysPowerLimit1Time**

---

Offset 0x07E8 - PL1 timewindow PL1 timewindow in seconds.

0 = AUTO, uses 28 seconds. Valid values(Unit in seconds) 1 to 8 ,  
10 , 12 ,14 , 16 , 20 , 24 , 28 , 32 , 40 , 48 , 56 , 64 , 80 , 96 , 112 ,  
128

Definition at line [2632](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::PsysPowerLimit2**

---

Offset 0x07E9 - PL2 Enable Value PL2 Enable activates the PL2 value to limit average platform power.

**0: Disable; 1: Enable.** \$EN\_DIS

Definition at line [2639](#) of file [FspUpd.h](#).

### **UINT32 FSP\_S\_TEST\_CONFIG::PsysPowerLimit2Power**

---

Offset 0x0894 - Platform PL2 power Platform PL2 power.

Units are based on

POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 4095875 in Step size of 125

Definition at line [3024](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::RaceToHalt**

---

Offset 0x081C - Race To Halt Enable/Disable Race To Halt feature.

RTH will dynamically increase CPU frequency in order to enter pkg C-State faster to reduce overall power. (RTH is controlled through MSR 1FC bit 20)  
**Disable; 1: Enable** \$EN\_DIS

Definition at line [2889](#) of file [FspUpd.h](#).

### **UINT8 FSP\_S\_TEST\_CONFIG::SataTestMode**

---

Offset 0x0A5F - PCH Sata Test Mode Allow entrance to the PCH SATA test modes.

\$EN\_DIS

Definition at line [3265](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::SevenCoreRatioLimit**

---

Offset 0x089C - 7-Core Ratio Limit 7-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255.

This 7-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit. Range is 0 to 255 0x0:0xFF

Definition at line [3058](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::SixCoreRatioLimit**

---

Offset 0x089B - 6-Core Ratio Limit 6-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255.

This 6-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit. Range is 0 to 255 0x0:0xFF

Definition at line [3051](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::StateRatio[40]**

---

Offset 0x081E - P-state ratios for custom P-state table P-state ratios for custom P-state table.

NumberOfEntries has valid range between 0 to 40. For no. of P-States supported(NumberOfEntries) , StateRatio[NumberOfEntries] are configurable. Valid Range of each entry is 0 to 0x7F

Definition at line [2901](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::StateRatioMax16[16]**

---

Offset 0x0846 - P-state ratios for max 16 version of custom P-state table P-state ratios for max 16 version of custom P-state table.

This table is used for OS versions limited to a max of 16 P-States. If the first entry of this table is 0, or if Number of Entries is 16 or less, then this table will be ignored, and up to the top 16 values of the StateRatio table will be used instead. Valid Range of each entry is 0 to 0x7F

Definition at line [2910](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::TccActivationOffset**

---

Offset 0x07D8 - TCC Activation Offset TCC Activation Offset.

Offset from factory set TCC activation temperature at which the Thermal Control Circuit must be activated. TCC will be activated at TCC Activation Temperature, in volts. For Y SKU, the recommended default for this policy is **15**, For all other SKUs the recommended default are **0**

Definition at line [2539](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::TccOffsetClamp**

---

Offset 0x07D9 - Tcc Offset Clamp Enable/Disable Tcc Offset Clamp for Runtime Average Temperature Limit (RATL) allows CPU to throttle below P1. For Y SKU, the recommended default for this policy is **1: Enabled**, For all other SKUs the recommended default are **0: Disabled**.

\$EN\_DIS

Definition at line [2547](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::TccOffsetLock**

---

Offset 0x07DA - Tcc Offset Lock Tcc Offset Lock for Runtime Average Temperature Limit (RATL) to lock temperature target; **0:**

**Disabled**; 1: Enabled.

\$EN\_DIS

Definition at line [2554](#) of file [FspUpd.h](#).

## **UINT32 FSP\_S\_TEST\_CONFIG::TccOffsetTimeWindowForRatl**

---

Offset 0x0874 - Tcc Offset Time Window for RATL Package PL4 power limit.

Units are based on

POWER\_MGMT\_CONFIG.CustomPowerUnit.Valid Range 0 to 1023875 in Step size of 125

Definition at line [2976](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::ThreeCoreRatioLimit**

---

Offset 0x07CD - 3-Core Ratio Limit 3-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255.

This 3-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit.Range is 0 to 255

Definition at line [2471](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::ThreeStrikeCounterDisable**

---

Offset 0x0898 - Set Three Strike Counter Disable False (default): Three Strike counter will be incremented and True: Prevents Three Strike counter from incrementing; 0: **False**; 1: **True**.

0: False, 1: True

Definition at line [3031](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::TimedMwait**

---

Offset 0x0810 - Enable or Disable TimedMwait Support.

Enable or Disable TimedMwait Support. **0: Disable**; 1: Enable  
\$EN\_DIS

Definition at line [2815](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::TStates**

---

Offset 0x0803 - Enable or Disable T states Enable or Disable T states; **0: Disable**; 1: Enable.

\$EN\_DIS

Definition at line [2737](#) of file [FspUpd.h](#).

## **UINT8 FSP\_S\_TEST\_CONFIG::TwoCoreRatioLimit**

---

Offset 0x07CC - 2-Core Ratio Limit 2-Core Ratio Limit: LFM to Fused, For overclocking part: LFM to 255.

This 2-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit. Range is 0 to 255

Definition at line [2465](#) of file [FspUpd.h](#).

---

The documentation for this struct was generated from the following file:

- [FspUpd.h](#)



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

Main Page	Related Pages	Classes	Files
Class List	Class Index	Class Members	
<b>FSP_T_CONFIG Struct Reference</b>			<a href="#">Public Attributes</a>   <a href="#">List of all members</a>

Fsp T Configuration. More...

```
#include <FsptUpd.h>
```

## Public Attributes

UINT8 **PcdSerialloUartDebugEnable**

Offset 0x0040 - PcdSerialloUartDebugEnable Enable Seriallo Uart debug library with/without initializing Seriallo Uart device in FSP. [More...](#)

UINT8 **PcdSerialloUartNumber**

Offset 0x0041 - PcdSerialloUartNumber - FSPT Select Seriallo Uart Controller for debug. [More...](#)

UINT8 **PcdSerialloUart0PinMUXing**

Offset 0x0042 - PcdSerialloUart0PinMUXing - FSPT Select Seriallo Uart0 pin muxing. [More...](#)

UINT8 **UnusedUpdSpace0**

Offset 0x0043.

UINT32 **PcdSerialloUartInputClock**

Offset 0x0044.

UINT64 **PcdPciExpressBaseAddress**

Offset 0x0048 - Pci Express Base Address Base address to be programmed for Pci Express.

UINT32 **PcdPciExpressRegionLength**

Offset 0x0050 - Pci Express Region Length Region Length to be programmed for Pci Express.

UINT8 **ReservedFsptUpd1 [44]**

Offset 0x0054.

## Detailed Description

---

Fsp T Configuration.

Definition at line **68** of file [FsptUpd.h](#).

## Member Data Documentation

---

### **UINT8 FSP\_T\_CONFIG::PcdSerialloUart0PinMuxing**

---

Offset 0x0042 - PcdSerialloUart0PinMuxing - FSPT Select Seriallo Uart0 pin muxing.

Setting valid only if PcdSerialloUartNumber is set to UART0.  
0:default pins, 1:pins muxed with CNV\_BRI/RGI

Definition at line [88](#) of file [FsptUpd.h](#).

### **UINT8 FSP\_T\_CONFIG::PcdSerialloUartDebugEnabled**

---

Offset 0x0040 - PcdSerialloUartDebugEnabled Enable Seriallo Uart debug library with/without initializing Seriallo Uart device in FSP.

0:Disable, 1:Enable and Initialize, 2:Enable without Initializing

Definition at line [74](#) of file [FsptUpd.h](#).

### **UINT8 FSP\_T\_CONFIG::PcdSerialloUartNumber**

---

Offset 0x0041 - PcdSerialloUartNumber - FSPT Select Seriallo Uart Controller for debug.

Note: If UART0 is selected as CNVi BT Core interface, it cannot be used for debug purpose. 0:SerialloUart0, 1:SerialloUart1, 2:SerialloUart2

Definition at line [81](#) of file [FsptUpd.h](#).

---

The documentation for this struct was generated from the following file:

- [FsptUpd.h](#)

---

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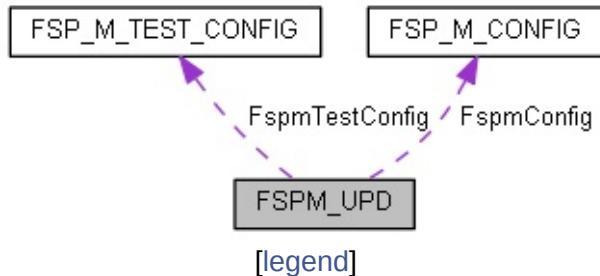
# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

Main Page	Related Pages	Classes	Files
Class List	Class Index	Class Members	
<b>FSPM_UPD Struct Reference</b>			<a href="#">Public Attributes</a>   <a href="#">List of all members</a>

Fsp M UPD Configuration. More...

```
#include <FspmUpd.h>
```

Collaboration diagram for FSPM\_UPD:



## Public Attributes

---

FSP\_UPD\_HEADER **FspUpdHeader**  
Offset 0x0000.

FSPM\_ARCH\_UPD **FspmArchUpd**  
Offset 0x0020.

**FSP\_M\_CONFIG** **FspmConfig**  
Offset 0x0040.

UINT8 **UnusedUpdSpace7**  
Offset 0x051F.

**FSP\_M\_TEST\_CONFIG** **FspmTestConfig**  
Offset 0x0520.

---

UINT32 **UpdTerminator**  
Offset 0x05BC.

## Detailed Description

---

Fsp M UPD Configuration.

Definition at line **2810** of file **FspmUpd.h**.

---

The documentation for this struct was generated from the following file:

- **FspmUpd.h**
- 

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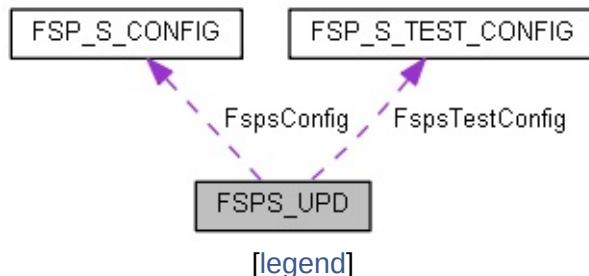
# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

Main Page	Related Pages	Classes	Files
Class List	Class Index	Class Members	
<b>FSPS_UPD Struct Reference</b>			<a href="#">Public Attributes</a>   <a href="#">List of all members</a>

Fsp S UPD Configuration. [More...](#)

```
#include <FspSUpd.h>
```

Collaboration diagram for FSPS\_UPD:



## Public Attributes

---

FSP\_UPD\_HEADER **FspUpdHeader**  
Offset 0x0000.

FSP\_S\_CONFIG **FspsConfig**  
Offset 0x0020.

FSP\_S\_TEST\_CONFIG **FspsTestConfig**  
Offset 0x07AD.

UINT16 **UpdTerminator**  
Offset 0x0A80.

---

## Detailed Description

---

Fsp S UPD Configuration.

Definition at line **3297** of file **FspsUpd.h**.

---

The documentation for this struct was generated from the following file:

- **FspsUpd.h**
- 

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

Main Page	Related Pages	Classes	Files
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<b>FSPT_CORE_UPD</b> <b>Struct Reference</b>			<a href="#">Public Attributes</a>   <a href="#">List of all members</a>

Fsp T Core UPD. [More...](#)

```
#include <FsptUpd.h>
```

## Public Attributes

---

UINT32 **MicrocodeRegionBase**  
Offset 0x0020.

UINT32 **MicrocodeRegionSize**  
Offset 0x0024.

UINT32 **CodeRegionBase**  
Offset 0x0028.

UINT32 **CodeRegionSize**  
Offset 0x002C.

UINT8 **Reserved [16]**  
Offset 0x0030.

---

## Detailed Description

---

Fsp T Core UPD.

Definition at line **43** of file [FsptUpd.h](#).

---

The documentation for this struct was generated from the following file:

- [FsptUpd.h](#)
- 

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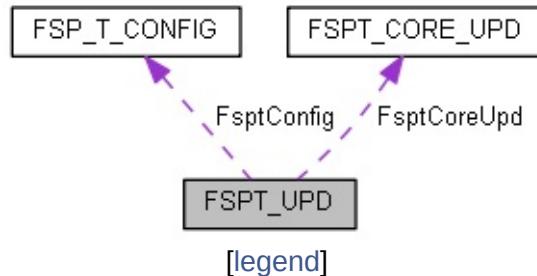
# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

Main Page	Related Pages	Classes	Files
Class List	Class Index	Class Members	
FSPT_UPD Struct Reference			<a href="#">Public Attributes</a>   <a href="#">List of all members</a>

Fsp T UPD Configuration. [More...](#)

```
#include <FsptUpd.h>
```

Collaboration diagram for FSPT\_UPD:



## Public Attributes

---

FSP\_UPD\_HEADER **FspUpdHeader**  
Offset 0x0000.

FSPT\_CORE\_UPD **FsptCoreUpd**  
Offset 0x0020.

FSP\_T\_CONFIG **FsptConfig**  
Offset 0x0040.

UINT16 **UpdTerminator**  
Offset 0x0080.

---

## Detailed Description

---

Fsp T UPD Configuration.

Definition at line **115** of file **FsptUpd.h**.

---

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- **FsptUpd.h**
- 

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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<b>GPIO_CONFIG Struct Reference</b>			<a href="#">Public Attributes</a>   <a href="#">List of all members</a>

GPIO configuration structure used for pin programming. [More...](#)

```
#include <GpioConfig.h>
```

## Public Attributes

UINT32 **PadMode:** 5

Pad Mode Pad can be set as GPIO or one of its native functions. [More...](#)

UINT32 **HostSoftPadOwn:** 2

Host Software Pad Ownership Set pad to ACPI mode or GPIO Driver Mode. [More...](#)

UINT32 **Direction:** 6

GPIO Direction Can choose between In, In with inversion, Out, both In and Out, both In with inversion and out or disabling both. [More...](#)

UINT32 **OutputState:** 2

Output State Set Pad output value. [More...](#)

UINT32 **InterruptConfig:** 9

GPIO Interrupt Configuration Set Pad to cause one of interrupts (IOxAPIC/SCI/SMI/NMI). [More...](#)

UINT32 **PowerConfig:** 8

GPIO Power Configuration. [More...](#)

UINT32 **ElectricalConfig:** 9

GPIO Electrical Configuration This setting controls pads termination. [More...](#)

UINT32 **LockConfig:** 4

GPIO Lock Configuration This setting controls pads lock. [More...](#)

UINT32 **OtherSettings:** 9

Additional GPIO configuration Refer to definition of GPIO\_OTHER\_CONFIG for supported settings.

**UINT32 RsvdBits: 10**

Reserved bits for future extension.

---

## Detailed Description

---

GPIO configuration structure used for pin programming.

Structure contains fields that can be used to configure pad.

Definition at line **36** of file **GpioConfig.h**.

## Member Data Documentation

---

### **UINT32 GPIO\_CONFIG::Direction**

---

GPIO Direction Can choose between In, In with inversion, Out, both In and Out, both In with inversion and out or disabling both.

Refer to definition of GPIO\_DIRECTION for supported settings.

Definition at line [57](#) of file [GpioConfig.h](#).

### **UINT32 GPIO\_CONFIG::ElectricalConfig**

---

GPIO Electrical Configuration This setting controls pads termination.

Refer to definition of GPIO\_ELECTRICAL\_CONFIG for supported settings.

Definition at line [83](#) of file [GpioConfig.h](#).

### **UINT32 GPIO\_CONFIG::HostSoftPadOwn**

---

Host Software Pad Ownership Set pad to ACPI mode or GPIO Driver Mode.

Refer to definition of GPIO\_HOSTSW OWN.

Definition at line [51](#) of file [GpioConfig.h](#).

### **UINT32 GPIO\_CONFIG::InterruptConfig**

---

GPIO Interrupt Configuration Set Pad to cause one of interrupts

(IOxAPIC/SCI/SMI/NMI).

This setting is applicable only if GPIO is in GpioMode with input enabled. Refer to definition of GPIO\_INT\_CONFIG for supported settings.

Definition at line [71](#) of file [GpioConfig.h](#).

### **UINT32 GPIO\_CONFIG::LockConfig**

---

GPIO Lock Configuration This setting controls pads lock.

Refer to definition of GPIO\_LOCK\_CONFIG for supported settings.

Definition at line [89](#) of file [GpioConfig.h](#).

### **UINT32 GPIO\_CONFIG::OutputState**

---

Output State Set Pad output value.

Refer to definition of GPIO\_OUTPUT\_STATE for supported settings. This setting takes place when output is enabled.

Definition at line [64](#) of file [GpioConfig.h](#).

### **UINT32 GPIO\_CONFIG::PadMode**

---

Pad Mode Pad can be set as GPIO or one of its native functions.

When in native mode setting Direction (except Inversion), OutputState, InterruptConfig, Host Software Pad Ownership and OutputStateLock are unnecessary. Refer to definition of GPIO\_PAD\_MODE. Refer to EDS for each native mode according to the pad.

Definition at line [45](#) of file [GpioConfig.h](#).

## **UINT32 GPIO\_CONFIG::PowerConfig**

---

GPIO Power Configuration.

This setting controls Pad Reset Configuration. Refer to definition of GPIO\_RESET\_CONFIG for supported settings.

Definition at line [77](#) of file [GpioConfig.h](#).

---

The documentation for this struct was generated from the following file:

- [GpioConfig.h](#)

---

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<b>HOB_USAGE_DATA_HOB Struct Reference</b>				

Hob Usage Data Hob. [More...](#)

#include <[HobUsageDataHob.h](#)>

## Detailed Description

---

Hob Usage Data Hob.

### Revision 1:

- Initial version.

Definition at line **30** of file **HobUsageDataHob.h**.

---

The documentation for this struct was generated from the following file:

- **HobUsageDataHob.h**

---

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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<b>MEMORY_PLATFORM_DATA Struct Reference</b>			List of all members	
Memory Platform Data Hob. <a href="#">More...</a>				

Memory Platform Data Hob. [More...](#)

#include <[MemInfoHob.h](#)>

## Detailed Description

---

Memory Platform Data Hob.

### Revision 1:

- Initial version. **Revision 2:**
- Added TsegBase, PrmrrSize, PrmrrBase, Gttbase, MmioSize, PciEBaseAddress fields

Definition at line [247](#) of file **MemInfoHob.h**.

---

The documentation for this struct was generated from the following file:

- **MemInfoHob.h**
- 

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<a href="#">Public Attributes</a>   <a href="#">List of all members</a>			
<h2>SI_PCH_DEVICE_INTERRUPT_CONFIG Struct Reference</h2>			

The PCH\_DEVICE\_INTERRUPT\_CONFIG block describes interrupt pin, IRQ and interrupt mode for PCH device. [More...](#)

```
#include <FspSUpd.h>
```

## Public Attributes

---

UINT8 **Device**

Device number.

UINT8 **Function**

Device function.

UINT8 **IntX**

Interrupt pin: INTA-INTD (see SI\_PCH\_INT\_PIN)

UINT8 **Irq**

IRQ to be set for device.

---

## Detailed Description

---

The PCH\_DEVICE\_INTERRUPT\_CONFIG block describes interrupt pin, IRQ and interrupt mode for PCH device.

Definition at line **74** of file [FspUpd.h](#).

---

The documentation for this struct was generated from the following file:

- [FspUpd.h](#)
- 

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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Class List	Class Index	Class Members	
<b>SMBIOS_CACHE_INFO</b> <b>Struct Reference</b>			<a href="#">Public Attributes</a>   <a href="#">List of all members</a>

SMBIOS Cache Info HOB Structure. [More...](#)

```
#include <SmbiosCacheInfoHob.h>
```

## Public Attributes

UINT16 **NumberOfCacheLevels**

Based on Number of Cache Types L1/L2/L3.

UINT8 **SocketDesignationStrIndex**

String Index in the string Buffer. Example "L1-CACHE".

UINT16 **CacheConfiguration**

Format defined in SMBIOS Spec v3.1 Section 7.8 Table 36.

UINT16 **MaxCacheSize**

Format defined in SMBIOS Spec v3.1 Section 7.8.1.

UINT16 **InstalledSize**

Format defined in SMBIOS Spec v3.1 Section 7.8.1.

UINT16 **SupportedSramType**

Format defined in SMBIOS Spec v3.1 Section 7.8.2.

UINT16 **CurrentSramType**

Format defined in SMBIOS Spec v3.1 Section 7.8.2.

UINT8 **CacheSpeed**

Cache Speed in nanoseconds. 0 if speed is unknown.

UINT8 **ErrorCorrectionType**

ENUM Format defined in SMBIOS Spec v3.1 Section 7.8.3.

UINT8 **SystemCacheType**

ENUM Format defined in SMBIOS Spec v3.1 Section 7.8.4.

UINT8 **Associativity**

ENUM Format defined in SMBIOS Spec v3.1 Section 7.8.5.

**UINT32 MaximumCacheSize2**

Format defined in SMBIOS Spec v3.1 Section7.8.1.

**UINT32 InstalledSize2**

Format defined in SMBIOS Spec v3.1 Section7.8.1.

---

## Detailed Description

---

SMBIOS Cache Info HOB Structure.

Definition at line **30** of file **SmbiosCacheInfoHob.h**.

---

The documentation for this struct was generated from the following file:

- **SmbiosCacheInfoHob.h**
- 

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<a href="#">Public Attributes</a>   <a href="#">List of all members</a>			
<h2>SMBIOS_PROCESSOR_INFO Struct Reference</h2>			

SMBIOS Processor Info HOB Structure. [More...](#)

#include <[SmbiosProcessorInfoHob.h](#)>

## Public Attributes

### UINT8 **ProcessorType**

ENUM defined in SMBIOS Spec v3.1 Section 7.5.1.

### UINT16 **ProcessorFamily**

This info is used for both ProcessorFamily and ProcessorFamily2 fields See ENUM defined in SMBIOS Spec v3.1 Section 7.5.2.

### UINT8 **ProcessorManufacturerStrIndex**

Index of the String in the String Buffer.

### UINT64 **ProcessorId**

ENUM defined in SMBIOS Spec v3.1 Section 7.5.3.

### UINT8 **ProcessorVersionStrIndex**

Index of the String in the String Buffer.

### UINT8 **Voltage**

Format defined in SMBIOS Spec v3.1 Section 7.5.4.

### UINT16 **ExternalClockInMHz**

External Clock Frequency. Set to 0 if unknown.

### UINT16 **CurrentSpeedInMHz**

Snapshot of current processor speed during boot.

### UINT8 **Status**

Format defined in the SMBIOS Spec v3.1 Table 21.

### UINT8 **ProcessorUpgrade**

ENUM defined in SMBIOS Spec v3.1 Section 7.5.5.

### UINT16 **CoreCount**

This info is used for both CoreCount & CoreCount2 fields  
See detailed description in SMBIOS Spec v3.1 Section 7.5.6.

**UINT16 EnabledCoreCount**

This info is used for both CoreEnabled & CoreEnabled2 fields  
See detailed description in SMBIOS Spec v3.1 Section 7.5.7.

**UINT16 ThreadCount**

This info is used for both ThreadCount & ThreadCount2 fields  
See detailed description in SMBIOS Spec v3.1 Section 7.5.8.

**UINT16 ProcessorCharacteristics**

Format defined in SMBIOS Spec v3.1 Section 7.5.9.

---

## Detailed Description

---

SMBIOS Processor Info HOB Structure.

Definition at line **29** of file **SmbiosProcessorInfoHob.h**.

---

The documentation for this struct was generated from the following file:

- **SmbiosProcessorInfoHob.h**
- 

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Main Page	Related Pages	Classes	Files
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<h2>SMBIOS_STRUCTURE Struct Reference</h2>			

The Smbios structure header. [More...](#)

```
#include <FirmwareVersionInfoHob.h>
```

## Detailed Description

---

The Smbios structure header.

Definition at line **48** of file **FirmwareVersionInfoHob.h**.

---

The documentation for this struct was generated from the following file:

- **FirmwareVersionInfoHob.h**
- 

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**A**

[AUDIO\\_AZALIA\\_VERB\\_TABLE](#)  
[AZALIA\\_HEADER](#)

**F**

[FIRMWARE\\_VERSION](#)  
[FIRMWARE\\_VERSION\\_INFO](#)  
[FIRMWARE\\_VERSION\\_INFO\\_HO](#)  
[FSP\\_M\\_CONFIG](#)  
[FSP\\_M\\_TEST\\_CONFIG](#)  
[FSP\\_S\\_CONFIG](#)

**C**

[CHIPSET\\_INIT\\_INFO](#)

**D**

[DIMM\\_INFO](#)

[A](#) | [C](#) | [D](#) | [F](#) | [G](#) | [H](#) | [M](#) | [S](#)



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Here is a list of all documented class members with links to the class documentation for each member:

## - a -

- AcLoadline : [FSP\\_S\\_CONFIG](#)
- AcousticNoiseMitigation : [FSP\\_S\\_CONFIG](#)
- ActEnergyCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- ActEnergyCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- ActEnergyCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- ActEnergyCh1Dimm1 : [FSP\\_M\\_CONFIG](#)
- ActiveCoreCount : [FSP\\_M\\_CONFIG](#)
- AesEnable : [FSP\\_S\\_CONFIG](#)
- ALIASCHK : [FSP\\_M\\_CONFIG](#)
- AmtEnabled : [FSP\\_S\\_CONFIG](#)
- AmtKvmEnabled : [FSP\\_S\\_CONFIG](#)
- AmtSolEnabled : [FSP\\_S\\_CONFIG](#)
- ApertureSize : [FSP\\_M\\_CONFIG](#)
- ApIdleManner : [FSP\\_S\\_TEST\\_CONFIG](#)
- ApStartupBase : [FSP\\_M\\_CONFIG](#)
- AsfEnabled : [FSP\\_S\\_CONFIG](#)
- Associativity : [SMBIOS\\_CACHE\\_INFO](#)
- AutoThermalReporting : [FSP\\_S\\_TEST\\_CONFIG](#)
- Avx2RatioOffset : [FSP\\_M\\_CONFIG](#)

- Avx3RatioOffset : **FSP\_M\_CONFIG**
- 

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All	Variables																					
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Here is a list of all documented class members with links to the class documentation for each member:

## - b -

- BclkAdaptiveVoltage : [FSP\\_M\\_CONFIG](#)
- BClkFrequency : [FSP\\_M\\_CONFIG](#)
- BdatEnable : [FSP\\_M\\_TEST\\_CONFIG](#)
- BdatTestType : [FSP\\_M\\_TEST\\_CONFIG](#)
- BgpdtHash : [FSP\\_S\\_CONFIG](#)
- BiosAcmBase : [FSP\\_M\\_CONFIG](#)
- BiosAcmSize : [FSP\\_M\\_CONFIG](#)
- BiosChipInitCrc : [CHIPSET\\_INIT\\_INFO](#)
- BiosGuard : [FSP\\_M\\_CONFIG](#)
- BiosGuardAttr : [FSP\\_S\\_CONFIG](#)
- BiosGuardModulePtr : [FSP\\_S\\_CONFIG](#)
- BiosGuardToolsInterface : [FSP\\_M\\_CONFIG](#)
- BiosSize : [FSP\\_M\\_TEST\\_CONFIG](#)
- BiProcHot : [FSP\\_S\\_TEST\\_CONFIG](#)
- BistOnReset : [FSP\\_M\\_CONFIG](#)
- BltBufferAddress : [FSP\\_S\\_CONFIG](#)
- BltBufferSize : [FSP\\_S\\_CONFIG](#)
- BootFrequency : [FSP\\_M\\_CONFIG](#)
- BypassPhySyncReset : [FSP\\_M\\_TEST\\_CONFIG](#)

---

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Here is a list of all documented class members with links to the class documentation for each member:

## - C -

- C1e : [FSP\\_S\\_TEST\\_CONFIG](#)
- C1StateAutoDemotion : [FSP\\_S\\_TEST\\_CONFIG](#)
- C1StateUnDemotion : [FSP\\_S\\_TEST\\_CONFIG](#)
- C3StateAutoDemotion : [FSP\\_S\\_TEST\\_CONFIG](#)
- C3StateUnDemotion : [FSP\\_S\\_TEST\\_CONFIG](#)
- CacheConfiguration : [SMBIOS\\_CACHE\\_INFO](#)
- CacheSpeed : [SMBIOS\\_CACHE\\_INFO](#)
- CaVrefConfig : [FSP\\_M\\_CONFIG](#)
- CdClock : [FSP\\_S\\_CONFIG](#)
- CdynmaxClampEnable : [FSP\\_S\\_TEST\\_CONFIG](#)
- ChapDeviceEnable : [FSP\\_S\\_TEST\\_CONFIG](#)
- ChHashEnable : [FSP\\_M\\_CONFIG](#)
- ChHashInterleaveBit : [FSP\\_M\\_CONFIG](#)
- ChHashMask : [FSP\\_M\\_CONFIG](#)
- ChipsetInitBinLen : [FSP\\_S\\_CONFIG](#)
- ChipsetInitBinPtr : [FSP\\_S\\_CONFIG](#)
- ChipsetInitMessage : [FSP\\_M\\_TEST\\_CONFIG](#)
- CkeRankMapping : [FSP\\_M\\_CONFIG](#)
- CleanMemory : [FSP\\_M\\_CONFIG](#)

- CMDDSEQ : **FSP\_M\_CONFIG**
- CMDNORM : **FSP\_M\_CONFIG**
- CmdRanksTerminated : **FSP\_M\_CONFIG**
- CMDSR : **FSP\_M\_CONFIG**
- CMDVC : **FSP\_M\_CONFIG**
- CodeRegionBase : **FSPT\_CORE\_UPD**
- CodeRegionSize : **FSPT\_CORE\_UPD**
- ComponentNameIndex : **FIRMWARE\_VERSION\_INFO**
- ConfigTdpBios : **FSP\_S\_TEST\_CONFIG**
- ConfigTdpLevel : **FSP\_S\_TEST\_CONFIG**
- ConfigTdpLock : **FSP\_S\_TEST\_CONFIG**
- CoreCount : **SMBIOS\_PROCESSOR\_INFO**
- CoreMaxOcRatio : **FSP\_M\_CONFIG**
- CorePllVoltageOffset : **FSP\_M\_CONFIG**
- CoreVoltageAdaptive : **FSP\_M\_CONFIG**
- CoreVoltageMode : **FSP\_M\_CONFIG**
- CoreVoltageOffset : **FSP\_M\_CONFIG**
- CoreVoltageOverride : **FSP\_M\_CONFIG**
- Count : **FIRMWARE\_VERSION\_INFO\_HOB**
- CpuBistData : **FSP\_S\_CONFIG**
- CpuMpHob : **FSP\_S\_CONFIG**
- CpuMpPpi : **FSP\_S\_CONFIG**
- CpuRatio : **FSP\_M\_CONFIG**
- CpuTraceHubMemReg0Size : **FSP\_M\_CONFIG**
- CpuTraceHubMemReg1Size : **FSP\_M\_CONFIG**
- CpuTraceHubMode : **FSP\_M\_CONFIG**
- CpuWakeUpTimer : **FSP\_S\_TEST\_CONFIG**
- CridEnable : **FSP\_S\_CONFIG**
- CstateLatencyControl0Irtl : **FSP\_S\_TEST\_CONFIG**
- CstateLatencyControl0TimeUnit : **FSP\_S\_TEST\_CONFIG**
- CstateLatencyControl1Irtl : **FSP\_S\_TEST\_CONFIG**
- CstateLatencyControl1TimeUnit : **FSP\_S\_TEST\_CONFIG**
- CstateLatencyControl2Irtl : **FSP\_S\_TEST\_CONFIG**
- CstateLatencyControl2TimeUnit : **FSP\_S\_TEST\_CONFIG**
- CstateLatencyControl3Irtl : **FSP\_S\_TEST\_CONFIG**
- CstateLatencyControl3TimeUnit : **FSP\_S\_TEST\_CONFIG**
- CstateLatencyControl4Irtl : **FSP\_S\_TEST\_CONFIG**
- CstateLatencyControl4TimeUnit : **FSP\_S\_TEST\_CONFIG**
- CstateLatencyControl5Irtl : **FSP\_S\_TEST\_CONFIG**
- CstateLatencyControl5TimeUnit : **FSP\_S\_TEST\_CONFIG**

- CStatePreWake : **FSP\_S\_TEST\_CONFIG**
- CstCfgCtrlIoMwaitRedirection : **FSP\_S\_TEST\_CONFIG**
- CurrentSpeedInMHz : **SMBIOS\_PROCESSOR\_INFO**
- CurrentSramType : **SMBIOS\_CACHE\_INFO**
- Custom1ConfigTdpControl : **FSP\_S\_TEST\_CONFIG**
- Custom1PowerLimit1 : **FSP\_S\_TEST\_CONFIG**
- Custom1PowerLimit1Time : **FSP\_S\_TEST\_CONFIG**
- Custom1PowerLimit2 : **FSP\_S\_TEST\_CONFIG**
- Custom1TurboActivationRatio : **FSP\_S\_TEST\_CONFIG**
- Custom2ConfigTdpControl : **FSP\_S\_TEST\_CONFIG**
- Custom2PowerLimit1 : **FSP\_S\_TEST\_CONFIG**
- Custom2PowerLimit1Time : **FSP\_S\_TEST\_CONFIG**
- Custom2PowerLimit2 : **FSP\_S\_TEST\_CONFIG**
- Custom2TurboActivationRatio : **FSP\_S\_TEST\_CONFIG**
- Custom3ConfigTdpControl : **FSP\_S\_TEST\_CONFIG**
- Custom3PowerLimit1 : **FSP\_S\_TEST\_CONFIG**
- Custom3PowerLimit1Time : **FSP\_S\_TEST\_CONFIG**
- Custom3PowerLimit2 : **FSP\_S\_TEST\_CONFIG**
- Custom3TurboActivationRatio : **FSP\_S\_TEST\_CONFIG**
- Cx : **FSP\_S\_TEST\_CONFIG**



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Here is a list of all documented class members with links to the class documentation for each member:

## - d -

- Data : [AUDIO\\_AZALIA\\_VERB\\_TABLE](#)
- DataDwords : [AZALIA\\_HEADER](#)
- DciUsb3TypecUfpDbg : [FSP\\_M\\_CONFIG](#)
- DcLoadline : [FSP\\_S\\_CONFIG](#)
- DdiPortBDdc : [FSP\\_S\\_CONFIG](#)
- DdiPortBHpd : [FSP\\_S\\_CONFIG](#)
- DdiPortCDdc : [FSP\\_S\\_CONFIG](#)
- DdiPortCHpd : [FSP\\_S\\_CONFIG](#)
- DdiPortDDdc : [FSP\\_S\\_CONFIG](#)
- DdiPortDHpd : [FSP\\_S\\_CONFIG](#)
- DdiPortEdp : [FSP\\_S\\_CONFIG](#)
- DdiPortFDdc : [FSP\\_S\\_CONFIG](#)
- DdiPortFHpd : [FSP\\_S\\_CONFIG](#)
- Ddr4DdpSharedClock : [FSP\\_M\\_CONFIG](#)
- Ddr4DdpSharedZq : [FSP\\_M\\_CONFIG](#)
- Ddr4MixedUDimm2DpcLimit : [FSP\\_M\\_CONFIG](#)
- DdrFreqLimit : [FSP\\_M\\_CONFIG](#)
- DdrThermalSensor : [FSP\\_M\\_CONFIG](#)
- DebugInterfaceEnable : [FSP\\_S\\_CONFIG](#) ,

## **FSP\_S\_TEST\_CONFIG**

- DebugInterfaceLockEnable : **FSP\_S\_TEST\_CONFIG**
- DeltaT12PowerCycleDelay : **FSP\_S\_CONFIG**
- Device : **SI\_PCH\_DEVICE\_INTERRUPT\_CONFIG**
- Device4Enable : **FSP\_S\_CONFIG**
- DevicId : **AZALIA\_HEADER**
- DevIntConfigPtr : **FSP\_S\_CONFIG**
- DidInitStat : **FSP\_M\_TEST\_CONFIG**
- DimmCapacity : **DIMM\_INFO**
- DIMMODTT : **FSP\_M\_CONFIG**
- DIMMRONT : **FSP\_M\_CONFIG**
- Direction : **GPIO\_CONFIG**
- DisableCpuReplacedPolling : **FSP\_M\_TEST\_CONFIG**
- DisableD0I3SettingForHeci : **FSP\_S\_TEST\_CONFIG**
- DisableDimmChannel0 : **FSP\_M\_CONFIG**
- DisableDimmChannel1 : **FSP\_M\_CONFIG**
- DisableHeciRetry : **FSP\_M\_TEST\_CONFIG**
- DisableMessageCheck : **FSP\_M\_TEST\_CONFIG**
- DisableMttrProgram : **FSP\_M\_CONFIG**
- DisableProcHotOut : **FSP\_S\_TEST\_CONFIG**
- DisableTurboGt : **FSP\_S\_TEST\_CONFIG**
- DisableVrThermalAlert : **FSP\_S\_TEST\_CONFIG**
- DIIbwEn0 : **FSP\_M\_CONFIG**
- DIIbwEn1 : **FSP\_M\_CONFIG**
- DIIbwEn2 : **FSP\_M\_CONFIG**
- DIIbwEn3 : **FSP\_M\_CONFIG**
- DmiAspm : **FSP\_S\_CONFIG**
- DmiDeEmphasis : **FSP\_M\_CONFIG**
- DmiExtSync : **FSP\_S\_TEST\_CONFIG**
- DmiGen3EndPointHint : **FSP\_M\_CONFIG**
- DmiGen3EndPointPreset : **FSP\_M\_CONFIG**
- DmiGen3EqPh2Enable : **FSP\_M\_TEST\_CONFIG**
- DmiGen3EqPh3Method : **FSP\_M\_TEST\_CONFIG**
- DmiGen3ProgramStaticEq : **FSP\_M\_CONFIG**
- DmiGen3RootPortPreset : **FSP\_M\_CONFIG**
- DmiGen3RxCtlePeaking : **FSP\_M\_CONFIG**
- Dmilot : **FSP\_S\_TEST\_CONFIG**
- DmiMaxLinkSpeed : **FSP\_M\_TEST\_CONFIG**
- DmiSuggestedSetting : **FSP\_S\_CONFIG**
- DmiTS0TW : **FSP\_S\_CONFIG**

- DmiTS1TW : **FSP\_S\_CONFIG**
  - DmiTS2TW : **FSP\_S\_CONFIG**
  - DmiTS3TW : **FSP\_S\_CONFIG**
  - DqByteMapCh0 : **FSP\_M\_CONFIG**
  - DqByteMapCh1 : **FSP\_M\_CONFIG**
  - DqPinsInterleaved : **FSP\_M\_CONFIG**
  - DqsMapCpu2DramCh0 : **FSP\_M\_CONFIG**
  - DqsMapCpu2DramCh1 : **FSP\_M\_CONFIG**
  - DualDimmPerChannelBoardType : **FSP\_M\_CONFIG**
- 

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Here is a list of all documented class members with links to the class documentation for each member:

- e -

- EcCmdLock : [FSP\\_S\\_CONFIG](#)
- EcCmdProvisionEav : [FSP\\_S\\_CONFIG](#)
- EccSupport : [FSP\\_M\\_CONFIG](#)
- ECT : [FSP\\_M\\_CONFIG](#)
- EdramTestMode : [FSP\\_S\\_TEST\\_CONFIG](#)
- EightCoreRatioLimit : [FSP\\_S\\_TEST\\_CONFIG](#)
- Eist : [FSP\\_S\\_TEST\\_CONFIG](#)
- ElectricalConfig : [GPIO\\_CONFIG](#)
- Enable8254ClockGating : [FSP\\_S\\_CONFIG](#)
- Enable8254ClockGatingOnS3 : [FSP\\_S\\_CONFIG](#)
- EnableC6Dram : [FSP\\_M\\_CONFIG](#)
- EnableCltm : [FSP\\_M\\_CONFIG](#)
- EnabledCoreCount : [SMBIOS\\_PROCESSOR\\_INFO](#)
- EnableExtts : [FSP\\_M\\_CONFIG](#)
- EnableItbm : [FSP\\_S\\_TEST\\_CONFIG](#)
- EnableItbmDriver : [FSP\\_S\\_TEST\\_CONFIG](#)
- EnableOltm : [FSP\\_M\\_CONFIG](#)
- EnablePwrDn : [FSP\\_M\\_CONFIG](#)
- EnablePwrDnLpddr : [FSP\\_M\\_CONFIG](#)

- EnableSgx : **FSP\_M\_CONFIG**
- EnableTcoTimer : **FSP\_S\_CONFIG**
- EnBER : **FSP\_M\_CONFIG**
- EnCmdRate : **FSP\_M\_CONFIG**
- EndOfPostMessage : **FSP\_S\_TEST\_CONFIG**
- EnergyEfficientPState : **FSP\_S\_TEST\_CONFIG**
- EnergyEfficientTurbo : **FSP\_S\_TEST\_CONFIG**
- EnergyScaleFact : **FSP\_M\_CONFIG**
- EnhancedInterleave : **FSP\_M\_CONFIG**
- EpgEnable : **FSP\_M\_CONFIG**
- ERDMPRTC2D : **FSP\_M\_CONFIG**
- ERDTC2D : **FSP\_M\_CONFIG**
- ErrorCorrectionType : **SMBIOS\_CACHE\_INFO**
- EsataSpeedLimit : **FSP\_S\_CONFIG**
- EWRDSEQ : **FSP\_M\_CONFIG**
- EWRTC2D : **FSP\_M\_CONFIG**
- ExitOnFailure : **FSP\_M\_CONFIG**
- ExternalClockInMHz : **SMBIOS\_PROCESSOR\_INFO**

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Here is a list of all documented class members with links to the class documentation for each member:

## - f -

- FastPkgCRampDisableFivr : [FSP\\_S\\_CONFIG](#)
- FastPkgCRampDisableGt : [FSP\\_S\\_CONFIG](#)
- FastPkgCRampDisableIa : [FSP\\_S\\_CONFIG](#)
- FastPkgCRampDisableSa : [FSP\\_S\\_CONFIG](#)
- FClkFrequency : [FSP\\_M\\_CONFIG](#)
- FiveCoreRatioLimit : [FSP\\_S\\_TEST\\_CONFIG](#)
- FivrEfficiency : [FSP\\_M\\_CONFIG](#)
- FivrFaults : [FSP\\_M\\_CONFIG](#)
- FivrRfiFrequency : [FSP\\_S\\_CONFIG](#)
- FivrSpreadSpectrum : [FSP\\_S\\_CONFIG](#)
- ForceOltmOrRefresh2x : [FSP\\_M\\_CONFIG](#)
- ForcMebxSyncUp : [FSP\\_S\\_CONFIG](#)
- FourCoreRatioLimit : [FSP\\_S\\_TEST\\_CONFIG](#)
- FreqSaGvLow : [FSP\\_M\\_CONFIG](#)
- FreqSaGvMid : [FSP\\_M\\_CONFIG](#)
- FspmArchUpd : [FSPM\\_UPD](#)
- FspmConfig : [FSPM\\_UPD](#)
- FspmTestConfig : [FSPM\\_UPD](#)
- FspsConfig : [FSPS\\_UPD](#)

- FspsTestConfig : **FSPS\_UPD**
  - FsptConfig : **FSPT\_UPD**
  - FsptCoreUpd : **FSPT\_UPD**
  - FspUpdHeader : **FSPM\_UPD , FSPS\_UPD , FSPT\_UPD**
  - Function : **SI\_PCH\_DEVICE\_INTERRUPT\_CONFIG**
  - FwProgress : **FSP\_S\_CONFIG**
- 

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Here is a list of all documented class members with links to the class documentation for each member:

## - g -

- GdxcEnable : [FSP\\_M\\_CONFIG](#)
- GdxclotSize : [FSP\\_M\\_CONFIG](#)
- GdxcMotSize : [FSP\\_M\\_CONFIG](#)
- Gen3SwEqAlwaysAttempt : [FSP\\_M\\_TEST\\_CONFIG](#)
- Gen3SwEqEnableVocTest : [FSP\\_M\\_TEST\\_CONFIG](#)
- Gen3SwEqJitterDwellTime : [FSP\\_M\\_TEST\\_CONFIG](#)
- Gen3SwEqJitterErrorTarget : [FSP\\_M\\_TEST\\_CONFIG](#)
- Gen3SwEqNumberOfPresets : [FSP\\_M\\_TEST\\_CONFIG](#)
- Gen3SwEqVocDwellTime : [FSP\\_M\\_TEST\\_CONFIG](#)
- Gen3SwEqVocErrorTarget : [FSP\\_M\\_TEST\\_CONFIG](#)
- GmAdr : [FSP\\_M\\_CONFIG](#)
- GnaEnable : [FSP\\_S\\_CONFIG](#)
- GpioIrqRoute : [FSP\\_S\\_CONFIG](#)
- GraphicsConfigPtr : [FSP\\_S\\_CONFIG](#)
- GtExtraTurboVoltage : [FSP\\_M\\_CONFIG](#)
- GtFreqMax : [FSP\\_S\\_TEST\\_CONFIG](#)
- GtMaxOcRatio : [FSP\\_M\\_CONFIG](#)
- GtPiiVoltageOffset : [FSP\\_M\\_CONFIG](#)
- GtPsmiSupport : [FSP\\_M\\_CONFIG](#)

- GttMmAddr : **FSP\_M\_CONFIG**
  - GttSize : **FSP\_M\_CONFIG**
  - GtusExtraTurboVoltage : **FSP\_M\_CONFIG**
  - GtusMaxOcRatio : **FSP\_M\_CONFIG**
  - GtusVoltageMode : **FSP\_M\_CONFIG**
  - GtusVoltageOffset : **FSP\_M\_CONFIG**
  - GtusVoltageOverride : **FSP\_M\_CONFIG**
  - GtVoltageMode : **FSP\_M\_CONFIG**
  - GtVoltageOffset : **FSP\_M\_CONFIG**
  - GtVoltageOverride : **FSP\_M\_CONFIG**
- 

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Here is a list of all documented class members with links to the class documentation for each member:

## - h -

- HdcControl : [FSP\\_S\\_TEST\\_CONFIG](#)
- Header : [AUDIO\\_AZALIA\\_VERB\\_TABLE](#) , [FIRMWARE\\_VERSION\\_INFO\\_HOB](#)
- Heci1BarAddress : [FSP\\_M\\_CONFIG](#)
- Heci2BarAddress : [FSP\\_M\\_CONFIG](#)
- Heci3BarAddress : [FSP\\_M\\_CONFIG](#)
- Heci3Enabled : [FSP\\_S\\_CONFIG](#)
- HeciCommunication2 : [FSP\\_M\\_TEST\\_CONFIG](#)
- HeciTimeouts : [FSP\\_M\\_CONFIG](#)
- HobBufferSize : [FSP\\_M\\_CONFIG](#)
- HostSoftPadOwn : [GPIO\\_CONFIG](#)
- HotBudgetCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- HotBudgetCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- HotBudgetCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- HotBudgetCh1Dimm1 : [FSP\\_M\\_CONFIG](#)
- HotThresholdCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- HotThresholdCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- HotThresholdCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- HotThresholdCh1Dimm1 : [FSP\\_M\\_CONFIG](#)

- Hwp : **FSP\_S\_TEST\_CONFIG**
  - HwPIinterruptControl : **FSP\_S\_TEST\_CONFIG**
  - HyperThreading : **FSP\_M\_CONFIG**
- 

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Here is a list of all documented class members with links to the class documentation for each member:

- i -

- IccMax : [FSP\\_S\\_CONFIG](#)
- Idd3n : [FSP\\_M\\_CONFIG](#)
- Idd3p : [FSP\\_M\\_CONFIG](#)
- IdleEnergyCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- IdleEnergyCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- IdleEnergyCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- IdleEnergyCh1Dimm1 : [FSP\\_M\\_CONFIG](#)
- LedSize : [FSP\\_M\\_CONFIG](#)
- IgDdvmt50PreAlloc : [FSP\\_M\\_CONFIG](#)
- ImonOffset : [FSP\\_S\\_CONFIG](#)
- ImonSlope : [FSP\\_S\\_CONFIG](#)
- ImonSlope1 : [FSP\\_S\\_CONFIG](#)
- ImrRpSelection : [FSP\\_M\\_CONFIG](#)
- InitPcieAspmAfterOprom : [FSP\\_M\\_CONFIG](#)
- InstalledSize : [SMBIOS\\_CACHE\\_INFO](#)
- InstalledSize2 : [SMBIOS\\_CACHE\\_INFO](#)
- InternalGfx : [FSP\\_M\\_CONFIG](#)
- InterruptConfig : [GPIO\\_CONFIG](#)
- IntX : [SI\\_PCH\\_DEVICE\\_INTERRUPT\\_CONFIG](#)

- `Irq` : **SI\_PCH\_DEVICE\_INTERRUPT\_CONFIG**
  - `IsIVrCmd` : **FSP\_S\_CONFIG**
  - `IsTPMPresence` : **FSP\_M\_CONFIG**
  - `IsvtIoPort` : **FSP\_M\_CONFIG**
- 

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Here is a list of all documented class members with links to the class documentation for each member:

- j -

- JtagC10PowerGateDisable : [FSP\\_M\\_CONFIG](#)
- JWRL : [FSP\\_M\\_CONFIG](#)



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Here is a list of all documented class members with links to the class documentation for each member:

- k -

- KtDeviceEnable : [FSP\\_M\\_TEST\\_CONFIG](#)



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Here is a list of all documented class members with links to the class documentation for each member:

- I -

- LCT : [FSP\\_M\\_CONFIG](#)
- LockConfig : [GPIO\\_CONFIG](#)
- LockPTMregs : [FSP\\_M\\_TEST\\_CONFIG](#)
- LogoPtr : [FSP\\_S\\_CONFIG](#)
- LogoSize : [FSP\\_S\\_CONFIG](#)
- LpDdrDqDqsReTraining : [FSP\\_M\\_CONFIG](#)



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Here is a list of all documented class members with links to the class documentation for each member:

## - m -

- MachineCheckEnable : [FSP\\_S\\_TEST\\_CONFIG](#)
- ManageabilityMode : [FSP\\_S\\_CONFIG](#)
- MaxCacheSize : [SMBIOS\\_CACHE\\_INFO](#)
- MaximumCacheSize2 : [SMBIOS\\_CACHE\\_INFO](#)
- MaxRatio : [FSP\\_S\\_TEST\\_CONFIG](#)
- MaxRingRatioLimit : [FSP\\_S\\_TEST\\_CONFIG](#)
- McivrRfiFrequencyAdjust : [FSP\\_S\\_CONFIG](#)
- McivrRfiFrequencyPrefix : [FSP\\_S\\_CONFIG](#)
- McivrSpreadSpectrum : [FSP\\_S\\_CONFIG](#)
- McPIIVoltageOffset : [FSP\\_M\\_CONFIG](#)
- MctpBroadcastCycle : [FSP\\_S\\_TEST\\_CONFIG](#)
- MeChipInitCrc : [CHIPSET\\_INIT\\_INFO](#)
- MemorySpdDataLen : [FSP\\_M\\_CONFIG](#)
- MemorySpdPtr00 : [FSP\\_M\\_CONFIG](#)
- MemorySpdPtr01 : [FSP\\_M\\_CONFIG](#)
- MemorySpdPtr10 : [FSP\\_M\\_CONFIG](#)
- MemorySpdPtr11 : [FSP\\_M\\_CONFIG](#)
- MemoryTrace : [FSP\\_M\\_CONFIG](#)
- MemTestOnWarmBoot : [FSP\\_M\\_CONFIG](#)

- MEmTST : **FSP\_M\_CONFIG**
  - MeUnconfigOnRtcClear : **FSP\_S\_CONFIG**
  - MicrocodeRegionBase : **FSP\_S\_CONFIG** , **FSPT\_CORE\_UPD**
  - MicrocodeRegionSize : **FSP\_S\_CONFIG** , **FSPT\_CORE\_UPD**
  - MinRingRatioLimit : **FSP\_S\_TEST\_CONFIG**
  - MlcSpatialPrefetcher : **FSP\_S\_TEST\_CONFIG**
  - MlcStreamerPrefetcher : **FSP\_S\_TEST\_CONFIG**
  - MmioSize : **FSP\_M\_CONFIG**
  - MmioSizeAdjustment : **FSP\_M\_CONFIG**
  - ModulePartNum : **DIMM\_INFO**
  - MonitorMwaitEnable : **FSP\_S\_TEST\_CONFIG**
  - MrcFastBoot : **FSP\_M\_CONFIG**
  - MrcSafeConfig : **FSP\_M\_CONFIG**
- 

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Here is a list of all documented class members with links to the class documentation for each member:

## - n -

- NModeSupport : [FSP\\_M\\_CONFIG](#)
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- NumberOfEntries : [FSP\\_S\\_TEST\\_CONFIG](#)
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Here is a list of all documented class members with links to the class documentation for each member:

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- OddRatioMode : [FSP\\_M\\_CONFIG](#)
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- PanelPowerEnable : [FSP\\_M\\_TEST\\_CONFIG](#)
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- PcdSerialIoUartDebugEnabled : [FSP\\_T\\_CONFIG](#)
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- PcdSerialIoUartNumber : [FSP\\_M\\_CONFIG](#) , [FSP\\_T\\_CONFIG](#)
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- PchCnviMode : [FSP\\_S\\_CONFIG](#)
- PchCrid : [FSP\\_S\\_CONFIG](#)
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- PchEspiLgmrEnable : **FSP\_S\_CONFIG**
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- PchIshGp3GpioAssign : **FSP\_S\_CONFIG**
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- RankInDimm : [DIMM\\_INFO](#)
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- RdEnergyCh0Dimm1 : **FSP\_M\_CONFIG**
- RdEnergyCh1Dimm0 : **FSP\_M\_CONFIG**
- RdEnergyCh1Dimm1 : **FSP\_M\_CONFIG**
- RDEQT : **FSP\_M\_CONFIG**
- RDMPRT : **FSP\_M\_CONFIG**
- RDODTT : **FSP\_M\_CONFIG**
- RDTC1D : **FSP\_M\_CONFIG**
- RDTC2D : **FSP\_M\_CONFIG**
- RDVC2D : **FSP\_M\_CONFIG**
- RealtimeMemoryTiming : **FSP\_M\_CONFIG**
- RefClk : **FSP\_M\_CONFIG**
- Refresh2X : **FSP\_M\_CONFIG**
- RemapEnable : **FSP\_M\_CONFIG**
- RemoteAssistance : **FSP\_S\_CONFIG**
- RenderStandby : **FSP\_S\_TEST\_CONFIG**
- Reserved : **AZALIA\_HEADER** , **FSPT\_CORE\_UPD**
- Reserved2 : **FSP\_S\_CONFIG**
- ReservedCpuPostMemProduction : **FSP\_S\_CONFIG**
- ReservedCpuPostMemTest : **FSP\_S\_TEST\_CONFIG**
- ReservedForFuture1 : **FSP\_S\_CONFIG**
- ReservedFspmTestUpd : **FSP\_M\_TEST\_CONFIG**
- ReservedFspmUpd : **FSP\_M\_CONFIG**
- ReservedFspmUpdCfl : **FSP\_M\_CONFIG**
- ReservedFspsTestUpd : **FSP\_S\_TEST\_CONFIG**
- ReservedFspsUpd : **FSP\_S\_CONFIG**
- ReservedFsptUpd1 : **FSP\_T\_CONFIG**
- ReservedPchPreMem : **FSP\_M\_CONFIG**
- ReservedSecurityPreMem : **FSP\_M\_CONFIG**
- Revision : **CHIPSET\_INIT\_INFO**
- RevisionId : **AZALIA\_HEADER**
- RhActProbability : **FSP\_M\_CONFIG**
- RhPrevention : **FSP\_M\_CONFIG**
- RhSolution : **FSP\_M\_CONFIG**
- RingDownBin : **FSP\_M\_CONFIG**
- RingMaxOcRatio : **FSP\_M\_CONFIG**
- RingPIIVoltageOffset : **FSP\_M\_CONFIG**

- RingVoltageAdaptive : **FSP\_M\_CONFIG**
  - RingVoltageMode : **FSP\_M\_CONFIG**
  - RingVoltageOffset : **FSP\_M\_CONFIG**
  - RingVoltageOverride : **FSP\_M\_CONFIG**
  - RMC : **FSP\_M\_CONFIG**
  - RMT : **FSP\_M\_CONFIG**
  - RMTLoopCount : **FSP\_M\_CONFIG**
  - RmtPerTask : **FSP\_M\_CONFIG**
  - RootPortIndex : **FSP\_M\_CONFIG**
  - Rsvd : **CHIPSET\_INIT\_INFO**
  - RsvdBits : **GPIO\_CONFIG**
  - RsvdSmbusAddressTablePtr : **FSP\_M\_CONFIG**
  - RTL : **FSP\_M\_CONFIG**
- 

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Here is a list of all documented class members with links to the class documentation for each member:

## - S -

- SafeMode : [FSP\\_M\\_CONFIG](#)
- SaGv : [FSP\\_M\\_CONFIG](#)
- SalpuEnable : [FSP\\_M\\_CONFIG](#)
- SalpulMrConfiguration : [FSP\\_M\\_CONFIG](#)
- SaOcSupport : [FSP\\_M\\_CONFIG](#)
- SaPllVoltageOffset : [FSP\\_M\\_CONFIG](#)
- SaPostMemProductionRsvd : [FSP\\_S\\_CONFIG](#)
- SaPostMemTestRsvd : [FSP\\_S\\_TEST\\_CONFIG](#)
- SaPreMemProductionRsvd : [FSP\\_M\\_CONFIG](#)
- SaPreMemTestRsvd : [FSP\\_M\\_TEST\\_CONFIG](#)
- SaRtd3Pcie0Gpio : [FSP\\_M\\_CONFIG](#)
- SaRtd3Pcie1Gpio : [FSP\\_M\\_CONFIG](#)
- SaRtd3Pcie2Gpio : [FSP\\_M\\_CONFIG](#)
- SaRtd3Pcie3Gpio : [FSP\\_M\\_CONFIG](#)
- SataEnable : [FSP\\_S\\_CONFIG](#)
- SataLedEnable : [FSP\\_S\\_CONFIG](#)
- SataMode : [FSP\\_S\\_CONFIG](#)
- SataP0T1M : [FSP\\_S\\_CONFIG](#)
- SataP0T2M : [FSP\\_S\\_CONFIG](#)

- SataP0T3M : **FSP\_S\_CONFIG**
- SataP0TDisp : **FSP\_S\_CONFIG**
- SataP0TDispFinit : **FSP\_S\_CONFIG**
- SataP0Tinact : **FSP\_S\_CONFIG**
- SataP1T1M : **FSP\_S\_CONFIG**
- SataP1T2M : **FSP\_S\_CONFIG**
- SataP1T3M : **FSP\_S\_CONFIG**
- SataP1TDisp : **FSP\_S\_CONFIG**
- SataP1TDispFinit : **FSP\_S\_CONFIG**
- SataP1Tinact : **FSP\_S\_CONFIG**
- SataPortsDevSlp : **FSP\_S\_CONFIG**
- SataPortsDitoVal : **FSP\_S\_CONFIG**
- SataPortsDmVal : **FSP\_S\_CONFIG**
- SataPortsEnable : **FSP\_S\_CONFIG**
- SataPortsEnableDitoConfig : **FSP\_S\_CONFIG**
- SataPortsExternal : **FSP\_S\_CONFIG**
- SataPortsHotPlug : **FSP\_S\_CONFIG**
- SataPortsInterlockSw : **FSP\_S\_CONFIG**
- SataPortsSolidStateDrive : **FSP\_S\_CONFIG**
- SataPortsSpinUp : **FSP\_S\_CONFIG**
- SataPortsZpOdd : **FSP\_S\_CONFIG**
- SataPwrOptEnable : **FSP\_S\_CONFIG**
- SataRstCpuAttachedStorage : **FSP\_S\_CONFIG**
- SataRstHddUnlock : **FSP\_S\_CONFIG**
- SataRstInterrupt : **FSP\_S\_CONFIG**
- SataRstIrrt : **FSP\_S\_CONFIG**
- SataRstIrrtOnly : **FSP\_S\_CONFIG**
- SataRstLedLocate : **FSP\_S\_CONFIG**
- SataRstLegacyOrom : **FSP\_S\_CONFIG**
- SataRstOptaneMemory : **FSP\_S\_CONFIG**
- SataRstOromUiBanner : **FSP\_S\_CONFIG**
- SataRstOromUiDelay : **FSP\_S\_CONFIG**
- SataRstPcieDeviceResetDelay : **FSP\_S\_CONFIG**
- SataRstPcieEnable : **FSP\_S\_CONFIG**
- SataRstPcieStoragePort : **FSP\_S\_CONFIG**
- SataRstRaid0 : **FSP\_S\_CONFIG**
- SataRstRaid1 : **FSP\_S\_CONFIG**
- SataRstRaid10 : **FSP\_S\_CONFIG**
- SataRstRaid5 : **FSP\_S\_CONFIG**
- SataRstRaidDeviceId : **FSP\_S\_CONFIG**

- SataRstSmartStorage : **FSP\_S\_CONFIG**
- SataSalpSupport : **FSP\_S\_CONFIG**
- SataSpeedLimit : **FSP\_S\_CONFIG**
- SataTestMode : **FSP\_S\_TEST\_CONFIG**
- SataThermalSuggestedSetting : **FSP\_S\_CONFIG**
- SaVoltageOffset : **FSP\_M\_CONFIG**
- ScanExtGfxForLegacyOpRom : **FSP\_M\_TEST\_CONFIG**
- ScilrqSelect : **FSP\_S\_CONFIG**
- ScramblerSupport : **FSP\_M\_CONFIG**
- ScsEmmcEnabled : **FSP\_S\_CONFIG**
- ScsEmmcHs400Enabled : **FSP\_S\_CONFIG**
- ScsSdCardEnabled : **FSP\_S\_CONFIG**
- ScsUfsEnabled : **FSP\_S\_CONFIG**
- SdCardPowerEnableActiveHigh : **FSP\_S\_CONFIG**
- SdiNum : **AZALIA\_HEADER**
- SecurityTestRsvd : **FSP\_M\_TEST\_CONFIG**
- SendDidMsg : **FSP\_M\_TEST\_CONFIG**
- SendEcCmd : **FSP\_S\_CONFIG**
- SendVrMbxCmd : **FSP\_S\_CONFIG**
- SerialloDebugUartNumber : **FSP\_S\_CONFIG**
- SerialloDevMode : **FSP\_S\_CONFIG**
- SerialloEnableDebugUartAfterPost : **FSP\_S\_CONFIG**
- SerialloSpiCsPolarity : **FSP\_S\_CONFIG**
- SerialloUart0PinMUXing : **FSP\_S\_CONFIG**
- SerialloUartHwFlowCtrl : **FSP\_S\_CONFIG**
- SevenCoreRatioLimit : **FSP\_S\_TEST\_CONFIG**
- SgDelayAfterHoldReset : **FSP\_M\_CONFIG**
- SgDelayAfterPwrEn : **FSP\_M\_CONFIG**
- SgxEpoch0 : **FSP\_S\_CONFIG**
- SgxEpoch1 : **FSP\_S\_CONFIG**
- SgxSinitDataFromTpm : **FSP\_S\_TEST\_CONFIG**
- SgxSinitNvsData : **FSP\_S\_CONFIG**
- ShowSpiController : **FSP\_S\_CONFIG**
- SiCsmFlag : **FSP\_S\_CONFIG**
- Signature : **FSP\_M\_TEST\_CONFIG , FSP\_S\_TEST\_CONFIG**
- SinitMemorySize : **FSP\_M\_CONFIG**
- SiNumberOfSsidTableEntry : **FSP\_S\_CONFIG**
- SiSsidTablePtr : **FSP\_S\_CONFIG**
- SixCoreRatioLimit : **FSP\_S\_TEST\_CONFIG**
- SkipExtGfxScan : **FSP\_M\_TEST\_CONFIG**

- SkipMbpHob : **FSP\_M\_TEST\_CONFIG**
- SkipMpInit : **FSP\_M\_CONFIG** , **FSP\_S\_CONFIG**
- SkipPamLock : **FSP\_S\_TEST\_CONFIG**
- SkipPostBootSai : **FSP\_S\_TEST\_CONFIG**
- SkipS3CdClockInit : **FSP\_S\_CONFIG**
- SkipStopPbet : **FSP\_M\_CONFIG**
- SlowSlewRateForFivr : **FSP\_S\_CONFIG**
- SlowSlewRateForGt : **FSP\_S\_CONFIG**
- SlowSlewRateForIa : **FSP\_S\_CONFIG**
- SlowSlewRateForSa : **FSP\_S\_CONFIG**
- SlpS0DisQForDebug : **FSP\_S\_CONFIG**
- SlpS0Override : **FSP\_S\_CONFIG**
- SlpS0WithGbeSupport : **FSP\_S\_CONFIG**
- SmbiosData : **FIRMWARE\_VERSION\_INFO\_HOB**
- SmbusArpEnable : **FSP\_M\_CONFIG**
- SmbusDynamicPowerGating : **FSP\_M\_TEST\_CONFIG**
- SmbusEnable : **FSP\_M\_CONFIG**
- SmbusSpdWriteDisable : **FSP\_M\_TEST\_CONFIG**
- SmramMask : **FSP\_M\_CONFIG**
- SocketDesignationStrIndex : **SMBIOS\_CACHE\_INFO**
- SOT : **FSP\_M\_CONFIG**
- SpdAddressTable : **FSP\_M\_CONFIG**
- SpdDramDeviceType : **DIMM\_INFO**
- SpdModuleMemoryBusWidth : **DIMM\_INFO**
- SpdModuleType : **DIMM\_INFO**
- SpdProfileSelected : **FSP\_M\_CONFIG**
- SpdSave : **DIMM\_INFO**
- Speed : **DIMM\_INFO**
- SrefCfgEna : **FSP\_M\_CONFIG**
- StateRatio : **FSP\_S\_TEST\_CONFIG**
- StateRatioMax16 : **FSP\_S\_TEST\_CONFIG**
- Status : **DIMM\_INFO** , **SMBIOS\_PROCESSOR\_INFO**
- SupportedSramType : **SMBIOS\_CACHE\_INFO**
- SystemCacheType : **SMBIOS\_CACHE\_INFO**



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Here is a list of all documented class members with links to the class documentation for each member:

- t -

- TAT : [FSP\\_M\\_CONFIG](#)
- TccActivationOffset : [FSP\\_S\\_TEST\\_CONFIG](#)
- TccOffsetClamp : [FSP\\_S\\_TEST\\_CONFIG](#)
- TccOffsetLock : [FSP\\_S\\_TEST\\_CONFIG](#)
- TccOffsetTimeWindowForRatl : [FSP\\_S\\_TEST\\_CONFIG](#)
- tCL : [FSP\\_M\\_CONFIG](#)
- TcolrqEnable : [FSP\\_S\\_CONFIG](#)
- TcolrqSelect : [FSP\\_S\\_CONFIG](#)
- tCWL : [FSP\\_M\\_CONFIG](#)
- TdcEnable : [FSP\\_S\\_CONFIG](#)
- TdcLock : [FSP\\_S\\_CONFIG](#)
- TdcPowerLimit : [FSP\\_S\\_CONFIG](#)
- TdcTimeWindow : [FSP\\_S\\_CONFIG](#)
- TetonGlacierCR : [FSP\\_S\\_CONFIG](#)
- TetonGlacierSupport : [FSP\\_S\\_CONFIG](#)
- tFAW : [FSP\\_M\\_CONFIG](#)
- TgaSize : [FSP\\_M\\_CONFIG](#)
- ThermalMonitor : [FSP\\_S\\_TEST\\_CONFIG](#)
- ThreadCount : [SMBIOS\\_PROCESSOR\\_INFO](#)

- ThreeCoreRatioLimit : **FSP\_S\_TEST\_CONFIG**
- ThreeStrikeCounterDisable : **FSP\_S\_TEST\_CONFIG**
- ThrtCkeMinDefeat : **FSP\_M\_CONFIG**
- ThrtCkeMinDefeatLpddr : **FSP\_M\_CONFIG**
- ThrtCkeMinTmr : **FSP\_M\_CONFIG**
- ThrtCkeMinTmrLpddr : **FSP\_M\_CONFIG**
- TimedMwait : **FSP\_S\_TEST\_CONFIG**
- TjMaxOffset : **FSP\_M\_CONFIG**
- TotalFlashSize : **FSP\_M\_TEST\_CONFIG**
- TraceHubMemBase : **FSP\_S\_CONFIG**
- TrainTrace : **FSP\_M\_CONFIG**
- tRAS : **FSP\_M\_CONFIG**
- tRCDtRP : **FSP\_M\_CONFIG**
- tRd2RdDD : **FSP\_M\_TEST\_CONFIG**
- tRd2RdDG : **FSP\_M\_TEST\_CONFIG**
- tRd2RdDR : **FSP\_M\_TEST\_CONFIG**
- tRd2RdSG : **FSP\_M\_TEST\_CONFIG**
- tRd2WrDD : **FSP\_M\_TEST\_CONFIG**
- tRd2WrDG : **FSP\_M\_TEST\_CONFIG**
- tRd2WrDR : **FSP\_M\_TEST\_CONFIG**
- tRd2WrSG : **FSP\_M\_TEST\_CONFIG**
- tREFI : **FSP\_M\_CONFIG**
- tRFC : **FSP\_M\_CONFIG**
- tRRD : **FSP\_M\_CONFIG**
- tRRD\_L : **FSP\_M\_TEST\_CONFIG**
- tRRD\_S : **FSP\_M\_TEST\_CONFIG**
- tRTP : **FSP\_M\_CONFIG**
- TsegSize : **FSP\_M\_CONFIG**
- TsodAlarmwindowLockBit : **FSP\_M\_CONFIG**
- TsodCriticalEventOnly : **FSP\_M\_CONFIG**
- TsodCriticaltripLockBit : **FSP\_M\_CONFIG**
- TsodEventMode : **FSP\_M\_CONFIG**
- TsodEventOutputControl : **FSP\_M\_CONFIG**
- TsodEventPolarity : **FSP\_M\_CONFIG**
- TsodManualEnable : **FSP\_M\_CONFIG**
- TsodShutdownMode : **FSP\_M\_CONFIG**
- TsodTcritMax : **FSP\_M\_CONFIG**
- TsodThigMax : **FSP\_M\_CONFIG**
- TStates : **FSP\_S\_TEST\_CONFIG**
- TTCrossThrottling : **FSP\_S\_CONFIG**

- TTSuggestedSetting : **FSP\_S\_CONFIG**
- TurboMode : **FSP\_S\_CONFIG**
- TurboPowerLimitLock : **FSP\_S\_TEST\_CONFIG**
- TvbRatioClipping : **FSP\_M\_CONFIG**
- TvbVoltageOptimization : **FSP\_M\_CONFIG**
- TwoCoreRatioLimit : **FSP\_S\_TEST\_CONFIG**
- tWR : **FSP\_M\_CONFIG**
- tWr2RdDD : **FSP\_M\_TEST\_CONFIG**
- tWr2RdDG : **FSP\_M\_TEST\_CONFIG**
- tWr2RdDR : **FSP\_M\_TEST\_CONFIG**
- tWr2RdSG : **FSP\_M\_TEST\_CONFIG**
- tWr2WrDD : **FSP\_M\_TEST\_CONFIG**
- tWr2WrDG : **FSP\_M\_TEST\_CONFIG**
- tWr2WrDR : **FSP\_M\_TEST\_CONFIG**
- tWr2WrSG : **FSP\_M\_TEST\_CONFIG**
- tWTR : **FSP\_M\_CONFIG**
- tWTR\_L : **FSP\_M\_TEST\_CONFIG**
- tWTR\_S : **FSP\_M\_TEST\_CONFIG**
- Txt : **FSP\_M\_CONFIG**
- TxtAcheckRequest : **FSP\_M\_TEST\_CONFIG**
- TxtDprMemoryBase : **FSP\_M\_CONFIG**
- TxtDprMemorySize : **FSP\_M\_CONFIG**
- TxtEnable : **FSP\_S\_CONFIG**
- TxtHeapMemorySize : **FSP\_M\_CONFIG**
- TxtImplemented : **FSP\_M\_CONFIG**
- TxtLcpPdBase : **FSP\_M\_CONFIG**
- TxtLcpPdSize : **FSP\_M\_CONFIG**

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Here is a list of all documented class members with links to the class documentation for each member:

## - u -

- UnusedUpdSpace0 : [FSP\\_M\\_CONFIG](#) , [FSP\\_S\\_CONFIG](#) , [FSP\\_T\\_CONFIG](#)
- UnusedUpdSpace1 : [FSP\\_M\\_CONFIG](#) , [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace10 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace11 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace12 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace13 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace14 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace15 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace16 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace17 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace18 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace19 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace2 : [FSP\\_M\\_CONFIG](#) , [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace20 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace21 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace22 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace23 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace24 : [FSP\\_S\\_TEST\\_CONFIG](#)

- UnusedUpdSpace3 : **FSP\_M\_CONFIG**, **FSP\_S\_CONFIG**
- UnusedUpdSpace4 : **FSP\_M\_CONFIG**, **FSP\_S\_CONFIG**
- UnusedUpdSpace5 : **FSP\_M\_CONFIG**, **FSP\_S\_CONFIG**
- UnusedUpdSpace6 : **FSP\_M\_CONFIG**, **FSP\_S\_CONFIG**
- UnusedUpdSpace7 : **FSP\_S\_CONFIG**, **FSPM\_UPD**
- UnusedUpdSpace8 : **FSP\_M\_TEST\_CONFIG**, **FSP\_S\_CONFIG**
- UnusedUpdSpace9 : **FSP\_S\_CONFIG**
- UpdTerminator : **FSPM\_UPD**, **FSPS\_UPD**, **FSPT\_UPD**
- Usb2AfePehalfbit : **FSP\_S\_CONFIG**
- Usb2AfePetxiset : **FSP\_S\_CONFIG**
- Usb2AfePredeemp : **FSP\_S\_CONFIG**
- Usb2AfeTxiset : **FSP\_S\_CONFIG**
- Usb2OverCurrentPin : **FSP\_S\_CONFIG**
- Usb3HsioTxDeEmph : **FSP\_S\_CONFIG**
- Usb3HsioTxDeEmphEnable : **FSP\_S\_CONFIG**
- Usb3HsioTxDownscaleAmp : **FSP\_S\_CONFIG**
- Usb3HsioTxDownscaleAmpEnable : **FSP\_S\_CONFIG**
- Usb3OverCurrentPin : **FSP\_S\_CONFIG**
- UsbPdoProgramming : **FSP\_S\_CONFIG**
- UserBd : **FSP\_M\_CONFIG**
- UserBudgetEnable : **FSP\_M\_CONFIG**
- UserPowerWeightsEn : **FSP\_M\_CONFIG**
- UserThresholdEnable : **FSP\_M\_CONFIG**



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Here is a list of all documented class members with links to the class documentation for each member:

- v -

- VddVoltage : [FSP\\_M\\_CONFIG](#)
- VendorId : [AZALIA\\_HEADER](#)
- Version : [FIRMWARE\\_VERSION\\_INFO](#)
- VersionStringIndex : [FIRMWARE\\_VERSION\\_INFO](#)
- VmxEnable : [FSP\\_M\\_CONFIG](#)
- Voltage : [SMBIOS\\_PROCESSOR\\_INFO](#)
- VoltageOptimization : [FSP\\_S\\_TEST\\_CONFIG](#)
- VrConfigEnable : [FSP\\_S\\_CONFIG](#)
- VrPowerDeliveryDesign : [FSP\\_S\\_CONFIG](#)
- VrVoltageLimit : [FSP\\_S\\_CONFIG](#)
- VtdBaseAddress : [FSP\\_S\\_CONFIG](#)
- VtdDisable : [FSP\\_S\\_TEST\\_CONFIG](#)



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Here is a list of all documented class members with links to the class documentation for each member:

## - W -

- WarmBudgetCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- WarmBudgetCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- WarmBudgetCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- WarmBudgetCh1Dimm1 : [FSP\\_M\\_CONFIG](#)
- WarmThresholdCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- WarmThresholdCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- WarmThresholdCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- WarmThresholdCh1Dimm1 : [FSP\\_M\\_CONFIG](#)
- WatchDog : [FSP\\_S\\_CONFIG](#)
- WatchDogTimerBios : [FSP\\_S\\_CONFIG](#)
- WatchDogTimerOs : [FSP\\_S\\_CONFIG](#)
- WdtDisableAndLock : [FSP\\_M\\_TEST\\_CONFIG](#)
- WRDSEQT : [FSP\\_M\\_CONFIG](#)
- WRDSUDT : [FSP\\_M\\_CONFIG](#)
- WrEnergyCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- WrEnergyCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- WrEnergyCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- WrEnergyCh1Dimm1 : [FSP\\_M\\_CONFIG](#)
- WRSRT : [FSP\\_M\\_CONFIG](#)

- WRTC1D : **FSP\_M\_CONFIG**
  - WRTC2D : **FSP\_M\_CONFIG**
  - WRVC1D : **FSP\_M\_CONFIG**
  - WRVC2D : **FSP\_M\_CONFIG**
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Here is a list of all documented class members with links to the class documentation for each member:

- X -

- X2ApicOptOut : [FSP\\_S\\_CONFIG](#)
- XdciEnable : [FSP\\_S\\_CONFIG](#)



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- a -

- AcLoadline : [FSP\\_S\\_CONFIG](#)
- AcousticNoiseMitigation : [FSP\\_S\\_CONFIG](#)
- ActEnergyCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- ActEnergyCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- ActEnergyCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- ActEnergyCh1Dimm1 : [FSP\\_M\\_CONFIG](#)
- ActiveCoreCount : [FSP\\_M\\_CONFIG](#)
- AesEnable : [FSP\\_S\\_CONFIG](#)
- ALIASCHK : [FSP\\_M\\_CONFIG](#)
- AmtEnabled : [FSP\\_S\\_CONFIG](#)
- AmtKvmEnabled : [FSP\\_S\\_CONFIG](#)
- AmtSolEnabled : [FSP\\_S\\_CONFIG](#)
- ApertureSize : [FSP\\_M\\_CONFIG](#)
- ApIdleManner : [FSP\\_S\\_TEST\\_CONFIG](#)
- ApStartupBase : [FSP\\_M\\_CONFIG](#)
- AsfEnabled : [FSP\\_S\\_CONFIG](#)
- Associativity : [SMBIOS\\_CACHE\\_INFO](#)
- AutoThermalReporting : [FSP\\_S\\_TEST\\_CONFIG](#)
- Avx2RatioOffset : [FSP\\_M\\_CONFIG](#)
- Avx3RatioOffset : [FSP\\_M\\_CONFIG](#)

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- b -

- BclkAdaptiveVoltage : **FSP\_M\_CONFIG**
- BClkFrequency : **FSP\_M\_CONFIG**
- BdatEnable : **FSP\_M\_TEST\_CONFIG**
- BdatTestType : **FSP\_M\_TEST\_CONFIG**
- BgpdtHash : **FSP\_S\_CONFIG**
- BiosAcmBase : **FSP\_M\_CONFIG**
- BiosAcmSize : **FSP\_M\_CONFIG**
- BiosChipInitCrc : **CHIPSET\_INIT\_INFO**
- BiosGuard : **FSP\_M\_CONFIG**
- BiosGuardAttr : **FSP\_S\_CONFIG**
- BiosGuardModulePtr : **FSP\_S\_CONFIG**
- BiosGuardToolsInterface : **FSP\_M\_CONFIG**
- BiosSize : **FSP\_M\_TEST\_CONFIG**
- BiProcHot : **FSP\_S\_TEST\_CONFIG**
- BistOnReset : **FSP\_M\_CONFIG**
- BltBufferAddress : **FSP\_S\_CONFIG**
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- C1StateAutoDemotion : [FSP\\_S\\_TEST\\_CONFIG](#)
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- C3StateAutoDemotion : [FSP\\_S\\_TEST\\_CONFIG](#)
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- CacheConfiguration : [SMBIOS\\_CACHE\\_INFO](#)
- CacheSpeed : [SMBIOS\\_CACHE\\_INFO](#)
- CaVrefConfig : [FSP\\_M\\_CONFIG](#)
- CdClock : [FSP\\_S\\_CONFIG](#)
- CdynmaxClampEnable : [FSP\\_S\\_TEST\\_CONFIG](#)
- ChapDeviceEnable : [FSP\\_S\\_TEST\\_CONFIG](#)
- ChHashEnable : [FSP\\_M\\_CONFIG](#)
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- ChipsetInitBinLen : [FSP\\_S\\_CONFIG](#)
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- ChipsetInitMessage : [FSP\\_M\\_TEST\\_CONFIG](#)
- CkeRankMapping : [FSP\\_M\\_CONFIG](#)
- CleanMemory : [FSP\\_M\\_CONFIG](#)
- CMDDSEQ : [FSP\\_M\\_CONFIG](#)

- CMDNORM : **FSP\_M\_CONFIG**
- CmdRanksTerminated : **FSP\_M\_CONFIG**
- CMDSR : **FSP\_M\_CONFIG**
- CMDVC : **FSP\_M\_CONFIG**
- CodeRegionBase : **FSPT\_CORE\_UPD**
- CodeRegionSize : **FSPT\_CORE\_UPD**
- ComponentNameIndex : **FIRMWARE\_VERSION\_INFO**
- ConfigTdpBios : **FSP\_S\_TEST\_CONFIG**
- ConfigTdpLevel : **FSP\_S\_TEST\_CONFIG**
- ConfigTdpLock : **FSP\_S\_TEST\_CONFIG**
- CoreCount : **SMBIOS\_PROCESSOR\_INFO**
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- CorePllVoltageOffset : **FSP\_M\_CONFIG**
- CoreVoltageAdaptive : **FSP\_M\_CONFIG**
- CoreVoltageMode : **FSP\_M\_CONFIG**
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- Count : **FIRMWARE\_VERSION\_INFO\_HOB**
- CpuBistData : **FSP\_S\_CONFIG**
- CpuMpHob : **FSP\_S\_CONFIG**
- CpuMpPpi : **FSP\_S\_CONFIG**
- CpuRatio : **FSP\_M\_CONFIG**
- CpuTraceHubMemReg0Size : **FSP\_M\_CONFIG**
- CpuTraceHubMemReg1Size : **FSP\_M\_CONFIG**
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- CpuWakeUpTimer : **FSP\_S\_TEST\_CONFIG**
- CridEnable : **FSP\_S\_CONFIG**
- CstateLatencyControl0Irtl : **FSP\_S\_TEST\_CONFIG**
- CstateLatencyControl0TimeUnit : **FSP\_S\_TEST\_CONFIG**
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- CstateLatencyControl5TimeUnit : **FSP\_S\_TEST\_CONFIG**
- CStatePreWake : **FSP\_S\_TEST\_CONFIG**

- CstCfgCtrlIoMwaitRedirection : **FSP\_S\_TEST\_CONFIG**
- CurrentSpeedInMHz : **SMBIOS\_PROCESSOR\_INFO**
- CurrentSramType : **SMBIOS\_CACHE\_INFO**
- Custom1ConfigTdpControl : **FSP\_S\_TEST\_CONFIG**
- Custom1PowerLimit1 : **FSP\_S\_TEST\_CONFIG**
- Custom1PowerLimit1Time : **FSP\_S\_TEST\_CONFIG**
- Custom1PowerLimit2 : **FSP\_S\_TEST\_CONFIG**
- Custom1TurboActivationRatio : **FSP\_S\_TEST\_CONFIG**
- Custom2ConfigTdpControl : **FSP\_S\_TEST\_CONFIG**
- Custom2PowerLimit1 : **FSP\_S\_TEST\_CONFIG**
- Custom2PowerLimit1Time : **FSP\_S\_TEST\_CONFIG**
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- Custom2TurboActivationRatio : **FSP\_S\_TEST\_CONFIG**
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- Data : [AUDIO\\_AZALIA\\_VERB\\_TABLE](#)
- DataDwords : [AZALIA\\_HEADER](#)
- DciUsb3TypecUfpDbg : [FSP\\_M\\_CONFIG](#)
- DcLoadline : [FSP\\_S\\_CONFIG](#)
- DdiPortBDdc : [FSP\\_S\\_CONFIG](#)
- DdiPortBHpd : [FSP\\_S\\_CONFIG](#)
- DdiPortCDdc : [FSP\\_S\\_CONFIG](#)
- DdiPortCHpd : [FSP\\_S\\_CONFIG](#)
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- DdiPortDHpd : [FSP\\_S\\_CONFIG](#)
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- DdiPortFHpd : [FSP\\_S\\_CONFIG](#)
- Ddr4DdpSharedClock : [FSP\\_M\\_CONFIG](#)
- Ddr4DdpSharedZq : [FSP\\_M\\_CONFIG](#)
- Ddr4MixedUDimm2DpcLimit : [FSP\\_M\\_CONFIG](#)
- DdrFreqLimit : [FSP\\_M\\_CONFIG](#)
- DdrThermalSensor : [FSP\\_M\\_CONFIG](#)
- DebugInterfaceEnable : [FSP\\_S\\_CONFIG](#) , [FSP\\_S\\_TEST\\_CONFIG](#)

- DebugInterfaceLockEnable : **FSP\_S\_TEST\_CONFIG**
- DeltaT12PowerCycleDelay : **FSP\_S\_CONFIG**
- Device : **SI\_PCH\_DEVICE\_INTERRUPT\_CONFIG**
- Device4Enable : **FSP\_S\_CONFIG**
- DeviceId : **AZALIA\_HEADER**
- DevIntConfigPtr : **FSP\_S\_CONFIG**
- DidInitStat : **FSP\_M\_TEST\_CONFIG**
- DimmCapacity : **DIMM\_INFO**
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- DIMMRONT : **FSP\_M\_CONFIG**
- Direction : **GPIO\_CONFIG**
- DisableCpuReplacedPolling : **FSP\_M\_TEST\_CONFIG**
- DisableD0I3SettingForHeci : **FSP\_S\_TEST\_CONFIG**
- DisableDimmChannel0 : **FSP\_M\_CONFIG**
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- DisableHeciRetry : **FSP\_M\_TEST\_CONFIG**
- DisableMessageCheck : **FSP\_M\_TEST\_CONFIG**
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- DisableVrThermalAlert : **FSP\_S\_TEST\_CONFIG**
- DII\_BwEn0 : **FSP\_M\_CONFIG**
- DII\_BwEn1 : **FSP\_M\_CONFIG**
- DII\_BwEn2 : **FSP\_M\_CONFIG**
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- DmiAspm : **FSP\_S\_CONFIG**
- DmiDeEmphasis : **FSP\_M\_CONFIG**
- DmiExtSync : **FSP\_S\_TEST\_CONFIG**
- DmiGen3EndPointHint : **FSP\_M\_CONFIG**
- DmiGen3EndPointPreset : **FSP\_M\_CONFIG**
- DmiGen3EqPh2Enable : **FSP\_M\_TEST\_CONFIG**
- DmiGen3EqPh3Method : **FSP\_M\_TEST\_CONFIG**
- DmiGen3ProgramStaticEq : **FSP\_M\_CONFIG**
- DmiGen3RootPortPreset : **FSP\_M\_CONFIG**
- DmiGen3RxCtlePeaking : **FSP\_M\_CONFIG**
- Dmilot : **FSP\_S\_TEST\_CONFIG**
- DmiMaxLinkSpeed : **FSP\_M\_TEST\_CONFIG**
- DmiSuggestedSetting : **FSP\_S\_CONFIG**
- DmiTS0TW : **FSP\_S\_CONFIG**
- DmiTS1TW : **FSP\_S\_CONFIG**

- DmiTS2TW : **FSP\_S\_CONFIG**
  - DmiTS3TW : **FSP\_S\_CONFIG**
  - DqByteMapCh0 : **FSP\_M\_CONFIG**
  - DqByteMapCh1 : **FSP\_M\_CONFIG**
  - DqPinsInterleaved : **FSP\_M\_CONFIG**
  - DqsMapCpu2DramCh0 : **FSP\_M\_CONFIG**
  - DqsMapCpu2DramCh1 : **FSP\_M\_CONFIG**
  - DualDimmPerChannelBoardType : **FSP\_M\_CONFIG**
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- EcCmdLock : [FSP\\_S\\_CONFIG](#)
- EcCmdProvisionEav : [FSP\\_S\\_CONFIG](#)
- EccSupport : [FSP\\_M\\_CONFIG](#)
- ECT : [FSP\\_M\\_CONFIG](#)
- EdramTestMode : [FSP\\_S\\_TEST\\_CONFIG](#)
- EightCoreRatioLimit : [FSP\\_S\\_TEST\\_CONFIG](#)
- Eist : [FSP\\_S\\_TEST\\_CONFIG](#)
- ElectricalConfig : [GPIO\\_CONFIG](#)
- Enable8254ClockGating : [FSP\\_S\\_CONFIG](#)
- Enable8254ClockGatingOnS3 : [FSP\\_S\\_CONFIG](#)
- EnableC6Dram : [FSP\\_M\\_CONFIG](#)
- EnableCltm : [FSP\\_M\\_CONFIG](#)
- EnabledCoreCount : [SMBIOS\\_PROCESSOR\\_INFO](#)
- EnableExtts : [FSP\\_M\\_CONFIG](#)
- EnableItbm : [FSP\\_S\\_TEST\\_CONFIG](#)
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- EnableOltm : [FSP\\_M\\_CONFIG](#)
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- EnableSgx : [FSP\\_M\\_CONFIG](#)

- EnableTcoTimer : **FSP\_S\_CONFIG**
- EnBER : **FSP\_M\_CONFIG**
- EnCmdRate : **FSP\_M\_CONFIG**
- EndOfPostMessage : **FSP\_S\_TEST\_CONFIG**
- EnergyEfficientPState : **FSP\_S\_TEST\_CONFIG**
- EnergyEfficientTurbo : **FSP\_S\_TEST\_CONFIG**
- EnergyScaleFact : **FSP\_M\_CONFIG**
- EnhancedInterleave : **FSP\_M\_CONFIG**
- EpgEnable : **FSP\_M\_CONFIG**
- ERDMPRTC2D : **FSP\_M\_CONFIG**
- ERDTC2D : **FSP\_M\_CONFIG**
- ErrorCorrectionType : **SMBIOS\_CACHE\_INFO**
- EsataSpeedLimit : **FSP\_S\_CONFIG**
- EWRDSEQ : **FSP\_M\_CONFIG**
- EWRTC2D : **FSP\_M\_CONFIG**
- ExitOnFailure : **FSP\_M\_CONFIG**
- ExternalClockInMHz : **SMBIOS\_PROCESSOR\_INFO**

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- FastPkgCRampDisableFivr : [FSP\\_S\\_CONFIG](#)
- FastPkgCRampDisableGt : [FSP\\_S\\_CONFIG](#)
- FastPkgCRampDisableIela : [FSP\\_S\\_CONFIG](#)
- FastPkgCRampDisableSa : [FSP\\_S\\_CONFIG](#)
- FClkFrequency : [FSP\\_M\\_CONFIG](#)
- FiveCoreRatioLimit : [FSP\\_S\\_TEST\\_CONFIG](#)
- FivrEfficiency : [FSP\\_M\\_CONFIG](#)
- FivrFaults : [FSP\\_M\\_CONFIG](#)
- FivrRfiFrequency : [FSP\\_S\\_CONFIG](#)
- FivrSpreadSpectrum : [FSP\\_S\\_CONFIG](#)
- ForceOltmOrRefresh2x : [FSP\\_M\\_CONFIG](#)
- ForcMebxSyncUp : [FSP\\_S\\_CONFIG](#)
- FourCoreRatioLimit : [FSP\\_S\\_TEST\\_CONFIG](#)
- FreqSaGvLow : [FSP\\_M\\_CONFIG](#)
- FreqSaGvMid : [FSP\\_M\\_CONFIG](#)
- FspmArchUpd : [FSPM\\_UPD](#)
- FspmConfig : [FSPM\\_UPD](#)
- FspmTestConfig : [FSPM\\_UPD](#)
- FspsConfig : [FSPS\\_UPD](#)
- FspsTestConfig : [FSPS\\_UPD](#)

- FsptConfig : **FSPT\_UPD**
  - FsptCoreUpd : **FSPT\_UPD**
  - FspUpdHeader : **FSPM\_UPD** , **FSPS\_UPD** , **FSPT\_UPD**
  - Function : **SI\_PCH\_DEVICE\_INTERRUPT\_CONFIG**
  - FwProgress : **FSP\_S\_CONFIG**
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- GdxcEnable : [FSP\\_M\\_CONFIG](#)
- GdxclotSize : [FSP\\_M\\_CONFIG](#)
- GdxcMotSize : [FSP\\_M\\_CONFIG](#)
- Gen3SwEqAlwaysAttempt : [FSP\\_M\\_TEST\\_CONFIG](#)
- Gen3SwEqEnableVocTest : [FSP\\_M\\_TEST\\_CONFIG](#)
- Gen3SwEqJitterDwellTime : [FSP\\_M\\_TEST\\_CONFIG](#)
- Gen3SwEqJitterErrorTarget : [FSP\\_M\\_TEST\\_CONFIG](#)
- Gen3SwEqNumberOfPresets : [FSP\\_M\\_TEST\\_CONFIG](#)
- Gen3SwEqVocDwellTime : [FSP\\_M\\_TEST\\_CONFIG](#)
- Gen3SwEqVocErrorTarget : [FSP\\_M\\_TEST\\_CONFIG](#)
- GmAdr : [FSP\\_M\\_CONFIG](#)
- GnaEnable : [FSP\\_S\\_CONFIG](#)
- GpioIrqRoute : [FSP\\_S\\_CONFIG](#)
- GraphicsConfigPtr : [FSP\\_S\\_CONFIG](#)
- GtExtraTurboVoltage : [FSP\\_M\\_CONFIG](#)
- GtFreqMax : [FSP\\_S\\_TEST\\_CONFIG](#)
- GtMaxOcRatio : [FSP\\_M\\_CONFIG](#)
- GtPllVoltageOffset : [FSP\\_M\\_CONFIG](#)
- GtPsmiSupport : [FSP\\_M\\_CONFIG](#)
- GttMmAdr : [FSP\\_M\\_CONFIG](#)

- GttSize : **FSP\_M\_CONFIG**
  - GtusExtraTurboVoltage : **FSP\_M\_CONFIG**
  - GtusMaxOcRatio : **FSP\_M\_CONFIG**
  - GtusVoltageMode : **FSP\_M\_CONFIG**
  - GtusVoltageOffset : **FSP\_M\_CONFIG**
  - GtusVoltageOverride : **FSP\_M\_CONFIG**
  - GtVoltageMode : **FSP\_M\_CONFIG**
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  - GtVoltageOverride : **FSP\_M\_CONFIG**
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- HdcControl : [FSP\\_S\\_TEST\\_CONFIG](#)
- Header : [AUDIO\\_AZALIA\\_VERB\\_TABLE](#) , [FIRMWARE\\_VERSION\\_INFO\\_HOB](#)
- Heci1BarAddress : [FSP\\_M\\_CONFIG](#)
- Heci2BarAddress : [FSP\\_M\\_CONFIG](#)
- Heci3BarAddress : [FSP\\_M\\_CONFIG](#)
- Heci3Enabled : [FSP\\_S\\_CONFIG](#)
- HeciCommunication2 : [FSP\\_M\\_TEST\\_CONFIG](#)
- HeciTimeouts : [FSP\\_M\\_CONFIG](#)
- HobBufferSize : [FSP\\_M\\_CONFIG](#)
- HostSoftPadOwn : [GPIO\\_CONFIG](#)
- HotBudgetCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- HotBudgetCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- HotBudgetCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- HotBudgetCh1Dimm1 : [FSP\\_M\\_CONFIG](#)
- HotThresholdCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- HotThresholdCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- HotThresholdCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
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- Hwp : [FSP\\_S\\_TEST\\_CONFIG](#)

- HwPIinterruptControl : **FSP\_S\_TEST\_CONFIG**
  - HyperThreading : **FSP\_M\_CONFIG**
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- IccMax : [FSP\\_S\\_CONFIG](#)
- Idd3n : [FSP\\_M\\_CONFIG](#)
- Idd3p : [FSP\\_M\\_CONFIG](#)
- IdleEnergyCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- IdleEnergyCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- IdleEnergyCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- IdleEnergyCh1Dimm1 : [FSP\\_M\\_CONFIG](#)
- ledSize : [FSP\\_M\\_CONFIG](#)
- IgxDvmt50PreAlloc : [FSP\\_M\\_CONFIG](#)
- ImonOffset : [FSP\\_S\\_CONFIG](#)
- ImonSlope : [FSP\\_S\\_CONFIG](#)
- ImonSlope1 : [FSP\\_S\\_CONFIG](#)
- ImrRpSelection : [FSP\\_M\\_CONFIG](#)
- InitPcieAspmAfterOprom : [FSP\\_M\\_CONFIG](#)
- InstalledSize : [SMBIOS\\_CACHE\\_INFO](#)
- InstalledSize2 : [SMBIOS\\_CACHE\\_INFO](#)
- InternalGfx : [FSP\\_M\\_CONFIG](#)
- InterruptConfig : [GPIO\\_CONFIG](#)
- IntX : [SI\\_PCH\\_DEVICE\\_INTERRUPT\\_CONFIG](#)
- Irq : [SI\\_PCH\\_DEVICE\\_INTERRUPT\\_CONFIG](#)

- IsVrCmd : **FSP\_S\_CONFIG**
  - IsTPMPresence : **FSP\_M\_CONFIG**
  - IsvtIoPort : **FSP\_M\_CONFIG**
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- JtagC10PowerGateDisable : **FSP\_M\_CONFIG**
- JWRL : **FSP\_M\_CONFIG**



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- k -

- KtDeviceEnable : **FSP\_M\_TEST\_CONFIG**



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- l -

- LCT : [FSP\\_M\\_CONFIG](#)
- LockConfig : [GPIO\\_CONFIG](#)
- LockPTMregs : [FSP\\_M\\_TEST\\_CONFIG](#)
- LogoPtr : [FSP\\_S\\_CONFIG](#)
- LogoSize : [FSP\\_S\\_CONFIG](#)
- LpDdrDqDqsReTraining : [FSP\\_M\\_CONFIG](#)



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- MachineCheckEnable : [FSP\\_S\\_TEST\\_CONFIG](#)
- ManageabilityMode : [FSP\\_S\\_CONFIG](#)
- MaxCacheSize : [SMBIOS\\_CACHE\\_INFO](#)
- MaximumCacheSize2 : [SMBIOS\\_CACHE\\_INFO](#)
- MaxRatio : [FSP\\_S\\_TEST\\_CONFIG](#)
- MaxRingRatioLimit : [FSP\\_S\\_TEST\\_CONFIG](#)
- McivrRfiFrequencyAdjust : [FSP\\_S\\_CONFIG](#)
- McivrRfiFrequencyPrefix : [FSP\\_S\\_CONFIG](#)
- McivrSpreadSpectrum : [FSP\\_S\\_CONFIG](#)
- McPIIVoltageOffset : [FSP\\_M\\_CONFIG](#)
- MctpBroadcastCycle : [FSP\\_S\\_TEST\\_CONFIG](#)
- MeChipInitCrc : [CHIPSET\\_INIT\\_INFO](#)
- MemorySpdDataLen : [FSP\\_M\\_CONFIG](#)
- MemorySpdPtr00 : [FSP\\_M\\_CONFIG](#)
- MemorySpdPtr01 : [FSP\\_M\\_CONFIG](#)
- MemorySpdPtr10 : [FSP\\_M\\_CONFIG](#)
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- MemoryTrace : [FSP\\_M\\_CONFIG](#)
- MemTestOnWarmBoot : [FSP\\_M\\_CONFIG](#)
- MEMTST : [FSP\\_M\\_CONFIG](#)

- MeUnconfigOnRtcClear : **FSP\_S\_CONFIG**
  - MicrocodeRegionBase : **FSP\_S\_CONFIG** , **FSPT\_CORE\_UPD**
  - MicrocodeRegionSize : **FSP\_S\_CONFIG** , **FSPT\_CORE\_UPD**
  - MinRingRatioLimit : **FSP\_S\_TEST\_CONFIG**
  - MlcSpatialPrefetcher : **FSP\_S\_TEST\_CONFIG**
  - MlcStreamerPrefetcher : **FSP\_S\_TEST\_CONFIG**
  - MmioSize : **FSP\_M\_CONFIG**
  - MmioSizeAdjustment : **FSP\_M\_CONFIG**
  - ModulePartNum : **DIMM\_INFO**
  - MonitorMwaitEnable : **FSP\_S\_TEST\_CONFIG**
  - MrcFastBoot : **FSP\_M\_CONFIG**
  - MrcSafeConfig : **FSP\_M\_CONFIG**
- 

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- RDADPT : **FSP\_M\_CONFIG**
- RdEnergyCh0Dimm0 : **FSP\_M\_CONFIG**
- RdEnergyCh0Dimm1 : **FSP\_M\_CONFIG**
- RdEnergyCh1Dimm0 : **FSP\_M\_CONFIG**
- RdEnergyCh1Dimm1 : **FSP\_M\_CONFIG**
- RDEQT : **FSP\_M\_CONFIG**
- RDMPRT : **FSP\_M\_CONFIG**
- RDODTT : **FSP\_M\_CONFIG**
- RDTC1D : **FSP\_M\_CONFIG**
- RDTC2D : **FSP\_M\_CONFIG**
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- RealtimeMemoryTiming : **FSP\_M\_CONFIG**
- RefClk : **FSP\_M\_CONFIG**
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- RemapEnable : **FSP\_M\_CONFIG**
- RemoteAssistance : **FSP\_S\_CONFIG**
- RenderStandby : **FSP\_S\_TEST\_CONFIG**
- Reserved : **AZALIA\_HEADER , FSPT\_CORE\_UPD**
- Reserved2 : **FSP\_S\_CONFIG**
- ReservedCpuPostMemProduction : **FSP\_S\_CONFIG**
- ReservedCpuPostMemTest : **FSP\_S\_TEST\_CONFIG**
- ReservedForFuture1 : **FSP\_S\_CONFIG**
- ReservedFspmTestUpd : **FSP\_M\_TEST\_CONFIG**
- ReservedFspmUpd : **FSP\_M\_CONFIG**
- ReservedFspmUpdCfl : **FSP\_M\_CONFIG**
- ReservedFspsTestUpd : **FSP\_S\_TEST\_CONFIG**
- ReservedFspsUpd : **FSP\_S\_CONFIG**
- ReservedFsptUpd1 : **FSP\_T\_CONFIG**
- ReservedPchPreMem : **FSP\_M\_CONFIG**
- ReservedSecurityPreMem : **FSP\_M\_CONFIG**
- Revision : **CHIPSET\_INIT\_INFO**
- RevisionId : **AZALIA\_HEADER**
- RhActProbability : **FSP\_M\_CONFIG**
- RhPrevention : **FSP\_M\_CONFIG**
- RhSolution : **FSP\_M\_CONFIG**
- RingDownBin : **FSP\_M\_CONFIG**
- RingMaxOcRatio : **FSP\_M\_CONFIG**
- RingPIIVoltageOffset : **FSP\_M\_CONFIG**
- RingVoltageAdaptive : **FSP\_M\_CONFIG**

- RingVoltageMode : **FSP\_M\_CONFIG**
- RingVoltageOffset : **FSP\_M\_CONFIG**
- RingVoltageOverride : **FSP\_M\_CONFIG**
- RMC : **FSP\_M\_CONFIG**
- RMT : **FSP\_M\_CONFIG**
- RMTLoopCount : **FSP\_M\_CONFIG**
- RmtPerTask : **FSP\_M\_CONFIG**
- RootPortIndex : **FSP\_M\_CONFIG**
- Rsvd : **CHIPSET\_INIT\_INFO**
- RsvdBits : **GPIO\_CONFIG**
- RsvdSmbusAddressTablePtr : **FSP\_M\_CONFIG**
- RTL : **FSP\_M\_CONFIG**

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- SafeMode : [FSP\\_M\\_CONFIG](#)
- SaGv : [FSP\\_M\\_CONFIG](#)
- SalpuEnable : [FSP\\_M\\_CONFIG](#)
- SalpulmrConfiguration : [FSP\\_M\\_CONFIG](#)
- SaOcSupport : [FSP\\_M\\_CONFIG](#)
- SaPllVoltageOffset : [FSP\\_M\\_CONFIG](#)
- SaPostMemProductionRsvd : [FSP\\_S\\_CONFIG](#)
- SaPostMemTestRsvd : [FSP\\_S\\_TEST\\_CONFIG](#)
- SaPreMemProductionRsvd : [FSP\\_M\\_CONFIG](#)
- SaPreMemTestRsvd : [FSP\\_M\\_TEST\\_CONFIG](#)
- SaRtd3Pcie0Gpio : [FSP\\_M\\_CONFIG](#)
- SaRtd3Pcie1Gpio : [FSP\\_M\\_CONFIG](#)
- SaRtd3Pcie2Gpio : [FSP\\_M\\_CONFIG](#)
- SaRtd3Pcie3Gpio : [FSP\\_M\\_CONFIG](#)
- SataEnable : [FSP\\_S\\_CONFIG](#)
- SataLedEnable : [FSP\\_S\\_CONFIG](#)
- SataMode : [FSP\\_S\\_CONFIG](#)
- SataP0T1M : [FSP\\_S\\_CONFIG](#)
- SataP0T2M : [FSP\\_S\\_CONFIG](#)
- SataP0T3M : [FSP\\_S\\_CONFIG](#)

- SataP0TDisp : **FSP\_S\_CONFIG**
- SataP0TDispFinit : **FSP\_S\_CONFIG**
- SataP0TInact : **FSP\_S\_CONFIG**
- SataP1T1M : **FSP\_S\_CONFIG**
- SataP1T2M : **FSP\_S\_CONFIG**
- SataP1T3M : **FSP\_S\_CONFIG**
- SataP1TDisp : **FSP\_S\_CONFIG**
- SataP1TDispFinit : **FSP\_S\_CONFIG**
- SataP1TInact : **FSP\_S\_CONFIG**
- SataPortsDevSlp : **FSP\_S\_CONFIG**
- SataPortsDitoVal : **FSP\_S\_CONFIG**
- SataPortsDmVal : **FSP\_S\_CONFIG**
- SataPortsEnable : **FSP\_S\_CONFIG**
- SataPortsEnableDitoConfig : **FSP\_S\_CONFIG**
- SataPortsExternal : **FSP\_S\_CONFIG**
- SataPortsHotPlug : **FSP\_S\_CONFIG**
- SataPortsInterlockSw : **FSP\_S\_CONFIG**
- SataPortsSolidStateDrive : **FSP\_S\_CONFIG**
- SataPortsSpinUp : **FSP\_S\_CONFIG**
- SataPortsZpOdd : **FSP\_S\_CONFIG**
- SataPwrOptEnable : **FSP\_S\_CONFIG**
- SataRstCpuAttachedStorage : **FSP\_S\_CONFIG**
- SataRstHddUnlock : **FSP\_S\_CONFIG**
- SataRstInterrupt : **FSP\_S\_CONFIG**
- SataRstIrrt : **FSP\_S\_CONFIG**
- SataRstIrrtOnly : **FSP\_S\_CONFIG**
- SataRstLedLocate : **FSP\_S\_CONFIG**
- SataRstLegacyOrom : **FSP\_S\_CONFIG**
- SataRstOptaneMemory : **FSP\_S\_CONFIG**
- SataRstOromUiBanner : **FSP\_S\_CONFIG**
- SataRstOromUiDelay : **FSP\_S\_CONFIG**
- SataRstPcieDeviceResetDelay : **FSP\_S\_CONFIG**
- SataRstPcieEnable : **FSP\_S\_CONFIG**
- SataRstPcieStoragePort : **FSP\_S\_CONFIG**
- SataRstRaid0 : **FSP\_S\_CONFIG**
- SataRstRaid1 : **FSP\_S\_CONFIG**
- SataRstRaid10 : **FSP\_S\_CONFIG**
- SataRstRaid5 : **FSP\_S\_CONFIG**
- SataRstRaidDeviceId : **FSP\_S\_CONFIG**
- SataRstSmartStorage : **FSP\_S\_CONFIG**

- SataSalpSupport : **FSP\_S\_CONFIG**
- SataSpeedLimit : **FSP\_S\_CONFIG**
- SataTestMode : **FSP\_S\_TEST\_CONFIG**
- SataThermalSuggestedSetting : **FSP\_S\_CONFIG**
- SaVoltageOffset : **FSP\_M\_CONFIG**
- ScanExtGfxForLegacyOpRom : **FSP\_M\_TEST\_CONFIG**
- ScilrqSelect : **FSP\_S\_CONFIG**
- ScramblerSupport : **FSP\_M\_CONFIG**
- ScsEmmcEnabled : **FSP\_S\_CONFIG**
- ScsEmmcHs400Enabled : **FSP\_S\_CONFIG**
- ScsSdCardEnabled : **FSP\_S\_CONFIG**
- ScsUfsEnabled : **FSP\_S\_CONFIG**
- SdCardPowerEnableActiveHigh : **FSP\_S\_CONFIG**
- SdiNum : **AZALIA\_HEADER**
- SecurityTestRsvd : **FSP\_M\_TEST\_CONFIG**
- SendDidMsg : **FSP\_M\_TEST\_CONFIG**
- SendEcCmd : **FSP\_S\_CONFIG**
- SendVrMbxCmd : **FSP\_S\_CONFIG**
- SerialIoDebugUartNumber : **FSP\_S\_CONFIG**
- SerialIoDevMode : **FSP\_S\_CONFIG**
- SerialIoEnableDebugUartAfterPost : **FSP\_S\_CONFIG**
- SerialIoSpiCsPolarity : **FSP\_S\_CONFIG**
- SerialIoUart0PinMUXing : **FSP\_S\_CONFIG**
- SerialIoUartHwFlowCtrl : **FSP\_S\_CONFIG**
- SevenCoreRatioLimit : **FSP\_S\_TEST\_CONFIG**
- SgDelayAfterHoldReset : **FSP\_M\_CONFIG**
- SgDelayAfterPwrEn : **FSP\_M\_CONFIG**
- SgxEpoch0 : **FSP\_S\_CONFIG**
- SgxEpoch1 : **FSP\_S\_CONFIG**
- SgxSinitDataFromTpm : **FSP\_S\_TEST\_CONFIG**
- SgxSinitNvsData : **FSP\_S\_CONFIG**
- ShowSpiController : **FSP\_S\_CONFIG**
- SiCsmFlag : **FSP\_S\_CONFIG**
- Signature : **FSP\_M\_TEST\_CONFIG , FSP\_S\_TEST\_CONFIG**
- SinitMemorySize : **FSP\_M\_CONFIG**
- SiNumberOfSsidTableEntry : **FSP\_S\_CONFIG**
- SiSsidTablePtr : **FSP\_S\_CONFIG**
- SixCoreRatioLimit : **FSP\_S\_TEST\_CONFIG**
- SkipExtGfxScan : **FSP\_M\_TEST\_CONFIG**
- SkipMbpHob : **FSP\_M\_TEST\_CONFIG**

- SkipMpInit : **FSP\_M\_CONFIG** , **FSP\_S\_CONFIG**
- SkipPamLock : **FSP\_S\_TEST\_CONFIG**
- SkipPostBootSai : **FSP\_S\_TEST\_CONFIG**
- SkipS3CdClockInit : **FSP\_S\_CONFIG**
- SkipStopPbet : **FSP\_M\_CONFIG**
- SlowSlewRateForFivr : **FSP\_S\_CONFIG**
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- SlpS0DisQForDebug : **FSP\_S\_CONFIG**
- SlpS0Override : **FSP\_S\_CONFIG**
- SlpS0WithGbSupport : **FSP\_S\_CONFIG**
- SmbiosData : **FIRMWARE\_VERSION\_INFO\_HOB**
- SmbusArpEnable : **FSP\_M\_CONFIG**
- SmbusDynamicPowerGating : **FSP\_M\_TEST\_CONFIG**
- SmbusEnable : **FSP\_M\_CONFIG**
- SmbusSpdWriteDisable : **FSP\_M\_TEST\_CONFIG**
- SmramMask : **FSP\_M\_CONFIG**
- SocketDesignationStrIndex : **SMBIOS\_CACHE\_INFO**
- SOT : **FSP\_M\_CONFIG**
- SpdAddressTable : **FSP\_M\_CONFIG**
- SpdDramDeviceType : **DIMM\_INFO**
- SpdModuleMemoryBusWidth : **DIMM\_INFO**
- SpdModuleType : **DIMM\_INFO**
- SpdProfileSelected : **FSP\_M\_CONFIG**
- SpdSave : **DIMM\_INFO**
- Speed : **DIMM\_INFO**
- SrefCfgEna : **FSP\_M\_CONFIG**
- StateRatio : **FSP\_S\_TEST\_CONFIG**
- StateRatioMax16 : **FSP\_S\_TEST\_CONFIG**
- Status : **DIMM\_INFO** , **SMBIOS\_PROCESSOR\_INFO**
- SupportedSramType : **SMBIOS\_CACHE\_INFO**
- SystemCacheType : **SMBIOS\_CACHE\_INFO**



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- TAT : [FSP\\_M\\_CONFIG](#)
- TccActivationOffset : [FSP\\_S\\_TEST\\_CONFIG](#)
- TccOffsetClamp : [FSP\\_S\\_TEST\\_CONFIG](#)
- TccOffsetLock : [FSP\\_S\\_TEST\\_CONFIG](#)
- TccOffsetTimeWindowForRatl : [FSP\\_S\\_TEST\\_CONFIG](#)
- tCL : [FSP\\_M\\_CONFIG](#)
- TcoIrqEnable : [FSP\\_S\\_CONFIG](#)
- TcoIrqSelect : [FSP\\_S\\_CONFIG](#)
- tCWL : [FSP\\_M\\_CONFIG](#)
- TdcEnable : [FSP\\_S\\_CONFIG](#)
- TdcLock : [FSP\\_S\\_CONFIG](#)
- TdcPowerLimit : [FSP\\_S\\_CONFIG](#)
- TdcTimeWindow : [FSP\\_S\\_CONFIG](#)
- TetonGlacierCR : [FSP\\_S\\_CONFIG](#)
- TetonGlacierSupport : [FSP\\_S\\_CONFIG](#)
- tFAW : [FSP\\_M\\_CONFIG](#)
- TgaSize : [FSP\\_M\\_CONFIG](#)
- ThermalMonitor : [FSP\\_S\\_TEST\\_CONFIG](#)
- ThreadCount : [SMBIOS\\_PROCESSOR\\_INFO](#)
- ThreeCoreRatioLimit : [FSP\\_S\\_TEST\\_CONFIG](#)

- ThreeStrikeCounterDisable : **FSP\_S\_TEST\_CONFIG**
- ThrtCkeMinDefeat : **FSP\_M\_CONFIG**
- ThrtCkeMinDefeatLpddr : **FSP\_M\_CONFIG**
- ThrtCkeMinTmr : **FSP\_M\_CONFIG**
- ThrtCkeMinTmrLpddr : **FSP\_M\_CONFIG**
- TimedMwait : **FSP\_S\_TEST\_CONFIG**
- TjMaxOffset : **FSP\_M\_CONFIG**
- TotalFlashSize : **FSP\_M\_TEST\_CONFIG**
- TraceHubMemBase : **FSP\_S\_CONFIG**
- TrainTrace : **FSP\_M\_CONFIG**
- tRAS : **FSP\_M\_CONFIG**
- tRCDtRP : **FSP\_M\_CONFIG**
- tRd2RdDD : **FSP\_M\_TEST\_CONFIG**
- tRd2RdDG : **FSP\_M\_TEST\_CONFIG**
- tRd2RdDR : **FSP\_M\_TEST\_CONFIG**
- tRd2RdSG : **FSP\_M\_TEST\_CONFIG**
- tRd2WrDD : **FSP\_M\_TEST\_CONFIG**
- tRd2WrDG : **FSP\_M\_TEST\_CONFIG**
- tRd2WrDR : **FSP\_M\_TEST\_CONFIG**
- tRd2WrSG : **FSP\_M\_TEST\_CONFIG**
- tREFI : **FSP\_M\_CONFIG**
- tRFC : **FSP\_M\_CONFIG**
- tRRD : **FSP\_M\_CONFIG**
- tRRD\_L : **FSP\_M\_TEST\_CONFIG**
- tRRD\_S : **FSP\_M\_TEST\_CONFIG**
- tRTP : **FSP\_M\_CONFIG**
- TsegSize : **FSP\_M\_CONFIG**
- TsodAlarmwindowLockBit : **FSP\_M\_CONFIG**
- TsodCriticalEventOnly : **FSP\_M\_CONFIG**
- TsodCriticaltripLockBit : **FSP\_M\_CONFIG**
- TsodEventMode : **FSP\_M\_CONFIG**
- TsodEventOutputControl : **FSP\_M\_CONFIG**
- TsodEventPolarity : **FSP\_M\_CONFIG**
- TsodManualEnable : **FSP\_M\_CONFIG**
- TsodShutdownMode : **FSP\_M\_CONFIG**
- TsodTcritMax : **FSP\_M\_CONFIG**
- TsodThigMax : **FSP\_M\_CONFIG**
- TStates : **FSP\_S\_TEST\_CONFIG**
- TTCrossThrottling : **FSP\_S\_CONFIG**
- TT SuggestedSetting : **FSP\_S\_CONFIG**

- TurboMode : **FSP\_S\_CONFIG**
- TurboPowerLimitLock : **FSP\_S\_TEST\_CONFIG**
- TvbRatioClipping : **FSP\_M\_CONFIG**
- TvbVoltageOptimization : **FSP\_M\_CONFIG**
- TwoCoreRatioLimit : **FSP\_S\_TEST\_CONFIG**
- tWR : **FSP\_M\_CONFIG**
- tWr2RdDD : **FSP\_M\_TEST\_CONFIG**
- tWr2RdDG : **FSP\_M\_TEST\_CONFIG**
- tWr2RdDR : **FSP\_M\_TEST\_CONFIG**
- tWr2RdSG : **FSP\_M\_TEST\_CONFIG**
- tWr2WrDD : **FSP\_M\_TEST\_CONFIG**
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- tWr2WrDR : **FSP\_M\_TEST\_CONFIG**
- tWr2WrSG : **FSP\_M\_TEST\_CONFIG**
- tWTR : **FSP\_M\_CONFIG**
- tWTR\_L : **FSP\_M\_TEST\_CONFIG**
- tWTR\_S : **FSP\_M\_TEST\_CONFIG**
- Txt : **FSP\_M\_CONFIG**
- TxtAcheckRequest : **FSP\_M\_TEST\_CONFIG**
- TxtDprMemoryBase : **FSP\_M\_CONFIG**
- TxtDprMemorySize : **FSP\_M\_CONFIG**
- TxtEnable : **FSP\_S\_CONFIG**
- TxtHeapMemorySize : **FSP\_M\_CONFIG**
- TxtImplemented : **FSP\_M\_CONFIG**
- TxtLcpPdBase : **FSP\_M\_CONFIG**
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- UnusedUpdSpace0 : [FSP\\_M\\_CONFIG](#) , [FSP\\_S\\_CONFIG](#) , [FSP\\_T\\_CONFIG](#)
- UnusedUpdSpace1 : [FSP\\_M\\_CONFIG](#) , [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace10 : [FSP\\_S\\_CONFIG](#)
- UnusedUpdSpace11 : [FSP\\_S\\_CONFIG](#)
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- UnusedUpdSpace2 : [FSP\\_M\\_CONFIG](#) , [FSP\\_S\\_CONFIG](#)
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- UnusedUpdSpace24 : [FSP\\_S\\_TEST\\_CONFIG](#)
- UnusedUpdSpace3 : [FSP\\_M\\_CONFIG](#) , [FSP\\_S\\_CONFIG](#)

- UnusedUpdSpace4 : **FSP\_M\_CONFIG** , **FSP\_S\_CONFIG**
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- UnusedUpdSpace9 : **FSP\_S\_CONFIG**
- UpdTerminator : **FSPM\_UPD** , **FSPS\_UPD** , **FSPT\_UPD**
- Usb2AfePehalfbit : **FSP\_S\_CONFIG**
- Usb2AfePetxiset : **FSP\_S\_CONFIG**
- Usb2AfePredeemp : **FSP\_S\_CONFIG**
- Usb2AfeTxiset : **FSP\_S\_CONFIG**
- Usb2OverCurrentPin : **FSP\_S\_CONFIG**
- Usb3HsioTxDeEmph : **FSP\_S\_CONFIG**
- Usb3HsioTxDeEmphEnable : **FSP\_S\_CONFIG**
- Usb3HsioTxDownscaleAmp : **FSP\_S\_CONFIG**
- Usb3HsioTxDownscaleAmpEnable : **FSP\_S\_CONFIG**
- Usb3OverCurrentPin : **FSP\_S\_CONFIG**
- UsbPdoProgramming : **FSP\_S\_CONFIG**
- UserBd : **FSP\_M\_CONFIG**
- UserBudgetEnable : **FSP\_M\_CONFIG**
- UserPowerWeightsEn : **FSP\_M\_CONFIG**
- UserThresholdEnable : **FSP\_M\_CONFIG**



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- VddVoltage : [FSP\\_M\\_CONFIG](#)
- VendorId : [AZALIA\\_HEADER](#)
- Version : [FIRMWARE\\_VERSION\\_INFO](#)
- VersionStringIndex : [FIRMWARE\\_VERSION\\_INFO](#)
- VmxEnable : [FSP\\_M\\_CONFIG](#)
- Voltage : [SMBIOS\\_PROCESSOR\\_INFO](#)
- VoltageOptimization : [FSP\\_S\\_TEST\\_CONFIG](#)
- VrConfigEnable : [FSP\\_S\\_CONFIG](#)
- VrPowerDeliveryDesign : [FSP\\_S\\_CONFIG](#)
- VrVoltageLimit : [FSP\\_S\\_CONFIG](#)
- VtdBaseAddress : [FSP\\_S\\_CONFIG](#)
- VtdDisable : [FSP\\_S\\_TEST\\_CONFIG](#)



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- WarmBudgetCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- WarmBudgetCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- WarmBudgetCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- WarmBudgetCh1Dimm1 : [FSP\\_M\\_CONFIG](#)
- WarmThresholdCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- WarmThresholdCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- WarmThresholdCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- WarmThresholdCh1Dimm1 : [FSP\\_M\\_CONFIG](#)
- WatchDog : [FSP\\_S\\_CONFIG](#)
- WatchDogTimerBios : [FSP\\_S\\_CONFIG](#)
- WatchDogTimerOs : [FSP\\_S\\_CONFIG](#)
- WdtDisableAndLock : [FSP\\_M\\_TEST\\_CONFIG](#)
- WRDSEQT : [FSP\\_M\\_CONFIG](#)
- WRDSUDT : [FSP\\_M\\_CONFIG](#)
- WrEnergyCh0Dimm0 : [FSP\\_M\\_CONFIG](#)
- WrEnergyCh0Dimm1 : [FSP\\_M\\_CONFIG](#)
- WrEnergyCh1Dimm0 : [FSP\\_M\\_CONFIG](#)
- WrEnergyCh1Dimm1 : [FSP\\_M\\_CONFIG](#)
- WRSRT : [FSP\\_M\\_CONFIG](#)
- WRTC1D : [FSP\\_M\\_CONFIG](#)

- WRTC2D : **FSP\_M\_CONFIG**
  - WRVC1D : **FSP\_M\_CONFIG**
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- X2ApicOptOut : **FSP\_S\_CONFIG**
- XdciEnable : **FSP\_S\_CONFIG**

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## File List

Here is a list of all documented files with brief descriptions:

<a href="#"> FirmwareVersionInfoHob.h</a>	Header file for Firmware Version Information
<a href="#"> FspFixedPcds.h</a>	This file lists all FixedAtBuild PCDs referenced in FSP integration guide
<a href="#"> FspInfoHob.h</a>	Header file for FSP Information HOB
<a href="#"> FspmUpd.h</a>	Copyright (c) 2018, Intel Corporation
<a href="#"> FspsUpd.h</a>	Copyright (c) 2018, Intel Corporation
<a href="#"> FsptUpd.h</a>	Copyright (c) 2018, Intel Corporation
<a href="#"> FspUpd.h</a>	Copyright (c) 2018, Intel Corporation
<a href="#"> GpioConfig.h</a>	Header file for GpioConfig structure used by GPIO library
<a href="#"> GpioSampleDef.h</a>	Sample enum definitions for GPIO table
<a href="#"> HobUsageDataHob.h</a>	Definitions for Hob Usage data

	HOB
 <b>MemInfoHob.h</b>	This file contains definitions required for creation of Memory S3 Save data, Memory Info data and Memory Platform data hobs
 <b>SmbiosCacheInfoHob.h</b>	Header file for SMBIOS Cache Info HOB
 <b>SmbiosProcessorInfoHob.h</b>	Header file for SMBIOS Processor Info HOB

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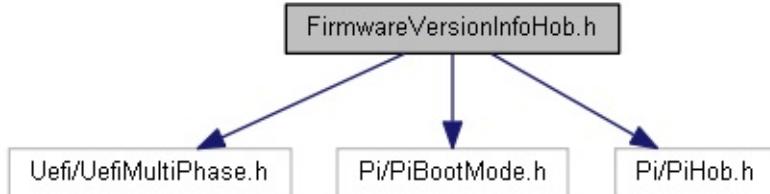
Classes

## FirmwareVersionInfoHob.h File Reference

Header file for Firmware Version Information. [More...](#)

```
#include <Uefi/UefiMultiPhase.h> #include <Pi/PiBootMode.h>
#include <Pi/PiHob.h>
```

Include dependency graph for FirmwareVersionInfoHob.h:



[Go to the source code of this file.](#)

## Classes

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struct **FIRMWARE\_VERSION**

Firmware Version Structure. [More...](#)

struct **FIRMWARE\_VERSION\_INFO**

Firmware Version Information Structure. [More...](#)

struct **SMBIOS\_STRUCTURE**

The Smbios structure header. [More...](#)

struct **FIRMWARE\_VERSION\_INFO\_HOB**

Firmware Version Information HOB Structure. [More...](#)

---

## Detailed Description

---

Header file for Firmware Version Information.

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Definition in file [FirmwareVersionInfoHob.h](#).

---

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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## FspFixedPcds.h File Reference

This file lists all FixedAtBuild PCDs referenced in FSP integration guide. [More...](#)

[Go to the source code of this file.](#)

## Macros

```
#define PcdFspAreaBaseAddress 0xFFFF30000  
FspAreaBaseAddress.
```

```
#define PcdFsplImageIdString $CFLFSP$  
FsplImageIdString.
```

```
#define PcdSiliconInitVersionMajor 0x07  
SiliconInitVersionMajor.
```

```
#define PcdSiliconInitVersionMinor 0x00  
SiliconInitVersionMinor.
```

```
#define PcdSiliconInitVersionRevision 0x3D  
SiliconInitVersionRevision.
```

```
#define PcdSiliconInitVersionBuild 0x60  
SiliconInitVersionBuild.
```

```
#define PcdGlobalDataPointerAddress 0xFED00148  
GlobalDataPointerAddress.
```

```
#define PcdTemporaryRamBase 0xFEFO0000  
TemporaryRamBase.
```

```
#define PcdTemporaryRamSize 0x00040000  
TemporaryRamSize.
```

```
#define PcdFspReservedBufferSize 0x100  
FspReservedBufferSize.
```

## Detailed Description

---

This file lists all FixedAtBuild PCDs referenced in FSP integration guide.

Those value may vary in different FSP revision to meet different requirements.

Definition in file **FspFixedPcds.h**.

---

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## FsplInfoHob.h File Reference

Header file for FSP Information HOB. [More...](#)

Go to the source code of this file.

## Detailed Description

---

Header file for FSP Information HOB.

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### Specification Reference:

Definition in file **FspInfoHob.h**.

---

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

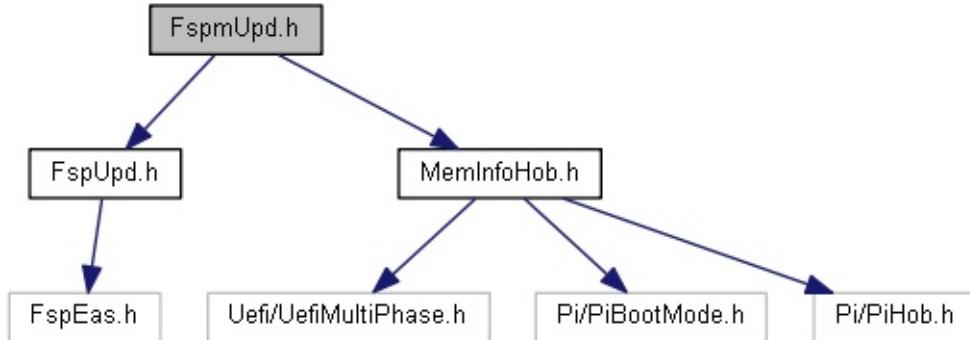
Main Page	Related Pages	Classes	<b>Files</b>
File List	File Members		
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## FspmUpd.h File Reference

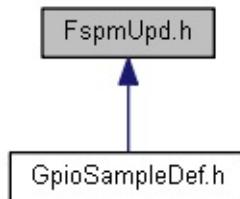
Copyright (c) 2018, Intel Corporation. [More...](#)

#include <[FspUpd.h](#)> #include <[MemInfoHob.h](#)>

Include dependency graph for FspmUpd.h:



This graph shows which files directly or indirectly include this file:



[Go to the source code of this file.](#)

## Classes

---

struct **CHIPSET\_INIT\_INFO**

The ChipsetInit Info structure provides the information of ME  
ChipsetInit CRC and BIOS ChipsetInit CRC. [More...](#)

struct **FSP\_M\_CONFIG**

Fsp M Configuration. [More...](#)

struct **FSP\_M\_TEST\_CONFIG**

Fsp M Test Configuration. [More...](#)

struct **FSPM\_UPD**

Fsp M UPD Configuration. [More...](#)

---

## Detailed Description

---

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## Definition in file **FspmUpd.h**.

---

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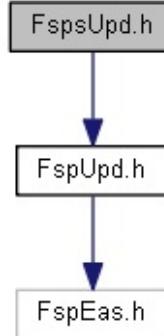
[Classes](#) | [Macros](#) | [Enumerations](#)

## FspUpd.h File Reference

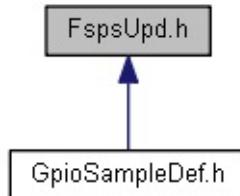
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```
#include <FspUpd.h>
```

Include dependency graph for FspUpd.h:



This graph shows which files directly or indirectly include this file:



[Go to the source code of this file.](#)

## Classes

---

struct **AZALIA\_HEADER**

Azalia Header structure. [More...](#)

struct **AUDIO\_AZALIA\_VERB\_TABLE**

Audio Azalia Verb Table structure. [More...](#)

struct **SI\_PCH\_DEVICE\_INTERRUPT\_CONFIG**

The PCH\_DEVICE\_INTERRUPT\_CONFIG block describes interrupt pin, IRQ and interrupt mode for PCH device. [More...](#)

struct **FSP\_S\_CONFIG**

Fsp S Configuration. [More...](#)

struct **FSP\_S\_TEST\_CONFIG**

Fsp S Test Configuration. [More...](#)

struct **FSPS\_UPD**

Fsp S UPD Configuration. [More...](#)

---

## Macros

---

```
#define SI_PCH_MAX_DEVICE_INTERRUPT_CONFIG 64  
Number of all PCH devices.
```

---

## Enumerations

---

enum **SI\_PCH\_INT\_PIN**

Refer to the definition of PCH\_INT\_PIN. [More...](#)

---

## Detailed Description

---

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Definition in file [FspsUpd.h](#).

# Enumeration Type Documentation

---

## **enum SI\_PCH\_INT\_PIN**

---

Refer to the definition of PCH\_INT\_PIN.

Enumerator
SiPchNoInt No Interrupt Pin.

Definition at line **64** of file **FspSUpd.h**.

---



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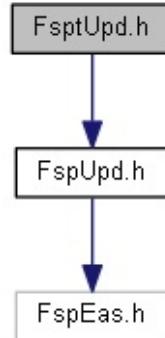
Classes

## FsptUpd.h File Reference

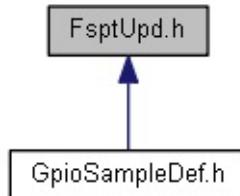
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```
#include <FspUpd.h>
```

Include dependency graph for FsptUpd.h:



This graph shows which files directly or indirectly include this file:



[Go to the source code of this file.](#)

## Classes

---

struct **FSPT\_CORE\_UPD**

Fsp T Core UPD. More...

struct **FSP\_T\_CONFIG**

Fsp T Configuration. More...

struct **FSPT\_UPD**

Fsp T UPD Configuration. More...

---

## Detailed Description

---

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## Definition in file **FsptUpd.h**.

---

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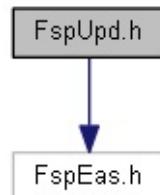
Include >

## FspUpd.h File Reference

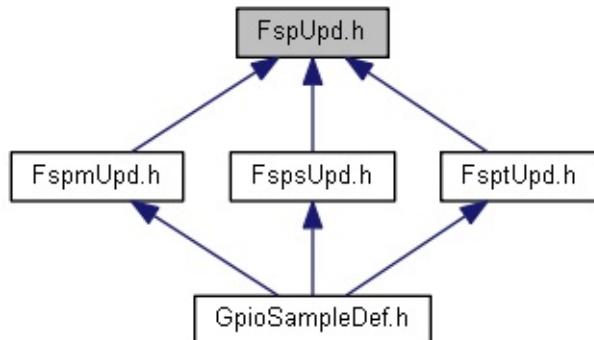
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```
#include <FspEas.h>
```

Include dependency graph for FspUpd.h:



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## Detailed Description

---

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## Definition in file **FspUpd.h**.

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## GpioConfig.h File Reference

Header file for GpioConfig structure used by GPIO library. [More...](#)

[Go to the source code of this file.](#)

## Classes

---

struct **GPIO\_CONFIG**

GPIO configuration structure used for pin programming.  
[More...](#)

---

## Macros

---

```
#define B_GPIO_INT_CONFIG_INT_SOURCE_MASK 0x1F  
Mask for GPIO_INT_CONFIG for interrupt source.
```

```
#define B_GPIO_INT_CONFIG_INT_TYPE_MASK 0xE0  
Mask for GPIO_INT_CONFIG for interrupt type.
```

```
#define B_GPIO_ELECTRICAL_CONFIG_TERMINATION_MASK 0:  
Mask for GPIO_ELECTRICAL_CONFIG for termination value.
```

```
#define B_GPIO_LOCK_CONFIG_PAD_CONF_LOCK_MASK 0x3  
Mask for GPIO_LOCK_CONFIG for Pad Configuration Lock.
```

```
#define B_GPIO_LOCK_CONFIG_OUTPUT_LOCK_MASK 0xC  
Mask for GPIO_LOCK_CONFIG for Pad Output Lock.
```

```
#define B_GPIO_OTHER_CONFIG_RXRAW_MASK 0x3  
Mask for GPIO_OTHER_CONFIG for RxRaw1 setting.
```

---

## Typedefs

---

typedef UINT32 **GPIO\_PAD**

For any GpioPad usage in code use GPIO\_PAD type.

typedef UINT32 **GPIO\_GROUP**

For any GpioGroup usage in code use GPIO\_GROUP type.

---

## Enumerations

enum **GPIO\_HARDWARE\_DEFAULT**

enum **GPIO\_PAD\_MODE**

GPIO Pad Mode Refer to GPIO documentation on native functions available for certain pad. [More...](#)

enum **GPIO\_HOSTSW OWN**

Host Software Pad Ownership modes This setting affects GPIO interrupt status registers. [More...](#)

enum **GPIO\_DIRECTION**

GPIO Direction. [More...](#)

enum **GPIO\_OUTPUT\_STATE**

GPIO Output State This field is relevant only if output is enabled. [More...](#)

enum **GPIO\_INT\_CONFIG**

GPIO interrupt configuration This setting is applicable only if pad is in GPIO mode and has input enabled. [More...](#)

enum **GPIO\_RESET\_CONFIG**

GPIO Power Configuration GPIO\_RESET\_CONFIG allows to set GPIO Reset type (PADCFG\_DW0.PadRstCfg) which will be used to reset certain GPIO settings. [More...](#)

enum **GPIO\_ELECTRICAL\_CONFIG**

GPIO Electrical Configuration Configuration options for GPIO termination setting. [More...](#)

enum **GPIO\_LOCK\_CONFIG**

GPIO LockConfiguration Set GPIO configuration lock and output state lock. [More...](#)

**enum GPIO\_OTHER\_CONFIG**

Other GPIO Configuration GPIO\_OTHER\_CONFIG is used for less often settings and for future extensions Supported settings: [More...](#)

---

## Detailed Description

---

Header file for GpioConfig structure used by GPIO library.

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### Specification Reference:

Definition in file [GpioConfig.h](#).

# Enumeration Type Documentation

---

## **enum GPIO\_DIRECTION**

---

GPIO Direction.

Enumerator	
GpioDirDefault	Leave pad direction setting unmodified.
GpioDirInOut	Set pad for both output and input.
GpioDirInInvOut	Set pad for both output and input with inversion.
GpioDirIn	Set pad for input only.
GpioDirInInv	Set pad for input with inversion.
GpioDirOut	Set pad for output only.
GpioDirNone	Disable both output and input.

Definition at line [149](#) of file **GpioConfig.h**.

## **enum GPIO\_ELECTRICAL\_CONFIG**

---

GPIO Electrical Configuration Configuration options for GPIO termination setting.

Enumerator	
GpioTermDefault	Leave termination setting unmodified.
GpioTermNone	none
GpioTermWpd5K	5kOhm weak pull-down
GpioTermWpd20K	20kOhm weak pull-down
GpioTermWpu1K	1kOhm weak pull-up
GpioTermWpu2K	2kOhm weak pull-up

GpioTermWpu5K	5kOhm weak pull-up
GpioTermWpu20K	20kOhm weak pull-up
GpioTermWpu1K2K	1kOhm & 2kOhm weak pull-up
GpioTermNative	<p>Native function controls pads termination This setting is applicable only to some native modes.</p> <p>Please check EDS to determine which native functionality can control pads termination</p>

Definition at line [264](#) of file [GpioConfig.h](#).

### **enum GPIO\_HARDWARE\_DEFAULT**

Enumerator	
GpioHardwareDefault	Leave setting unmodified.

Definition at line [99](#) of file [GpioConfig.h](#).

### **enum GPIO\_HOSTSW\_OWN**

Host Software Pad Ownership modes This setting affects GPIO interrupt status registers.

Depending on chosen ownership some GPIO Interrupt status register get updated and other masked. Please refer to EDS for HOSTSW\_OWN register description.

Enumerator	
GpioHostOwnDefault	Leave ownership value unmodified.
GpioHostOwnAcpi	<p>Set HOST ownership to ACPI.</p> <p>Use this setting if pad is not going to be used by GPIO OS driver. If GPIO is</p>

	configured to generate SCI/SMI/NMI then this setting must be used for interrupts to work
GpioHostOwnGpio	<p>Set HOST ownership to GPIO Driver mode.</p> <p>Use this setting only if GPIO pad should be controlled by GPIO OS Driver. GPIO OS Driver will be able to control the pad if appropriate entry in ACPI exists (refer to ACPI specification for Gpiolo and GpioInt descriptors)</p>

Definition at line [128](#) of file [GpioConfig.h](#).

## enum GPIO\_INT\_CONFIG

GPIO interrupt configuration This setting is applicable only if pad is in GPIO mode and has input enabled.

GPIO\_INT\_CONFIG allows to choose which interrupt is generated (IOxAPIC/SCI/SMI/NMI) and how it is triggered (edge or level). Refer to PADC<sub>F</sub>G<sub>D</sub>W0 register description in EDS for details on this settings. Field from GpioIntNmi to GpioIntApic can be OR'ed with GpioIntLevel to GpioIntBothEdge to describe an interrupt e.g. GpioIntApic | GpioIntLevel If GPIO is set to cause an SCI then also GPI\_GPE\_EN is enabled for this pad. If GPIO is set to cause an NMI then also GPI\_NMI\_EN is enabled for this pad. Not all GPIO are capable of generating an SMI or NMI interrupt. When routing GPIO to cause an IOxAPIC interrupt care must be taken, as this interrupt cannot be shared and its IRQn number is not configurable. Refer to EDS for GPIO pads IRQ numbers (PADC<sub>F</sub>G<sub>D</sub>W1.IntSel) If GPIO is under GPIO OS driver control and appropriate ACPI GpioInt descriptor exist then use only trigger type setting (from GpioIntLevel to GpioIntBothEdge). This type of GPIO Driver interrupt doesn't have any additional routing setting required to be set by BIOS. Interrupt is handled by GPIO OS Driver.

Enumerator	
GpioIntDefault	Leave value of interrupt routing unmodified.
GpioIntDis	Disable IOxAPIC/SCI/SMI/NMI interrupt generation.
GpioIntNmi	Enable NMI interrupt only.
GpioIntSmi	Enable SMI interrupt only.
GpioIntSci	Enable SCI interrupt only.
GpioIntApic	Enable IOxAPIC interrupt only.
GpioIntLevel	Set interrupt as level triggered.
GpioIntEdge	Set interrupt as edge triggered (type of edge depends on input inversion)
GpioIntLvlEdgDis	Disable interrupt trigger.
GpioIntBothEdge	Set interrupt as both edge triggered.

Definition at line [189](#) of file [GpioConfig.h](#).

## enum GPIO\_LOCK\_CONFIG

GPIO LockConfiguration Set GPIO configuration lock and output state lock.

GpioPadConfigUnlock/Lock and GpioOutputStateUnlock can be OR'ed. By default GPIO pads will be locked unless GPIO lib is explicitly informed that certain pad is to be left unlocked. Lock settings reset is in Powergood domain. Care must be taken when using this setting as fields it locks may be reset by a different signal and can be controlled by what is in GPIO\_RESET\_CONFIG (PADCFG\_DW0.PadRstCfg). GPIO library provides functions which allow to unlock a GPIO pad. If possible each GPIO lib function will try to unlock an already locked pad upon request for reconfiguration

Enumerator	
GpioLockDefault	<p>Perform default action.</p> <ul style="list-style-type: none"> <li>• if pad is an GPO, lock configuration</li> </ul>

	but leave output unlocked <ul style="list-style-type: none"> <li>• if pad is an GPI, lock everything</li> <li>• if pad is in native, lock everything</li> </ul>
GpioPadConfigUnlock	Leave Pad configuration unlocked.
GpioPadConfigLock	Lock Pad configuration.
GpioOutputStateUnlock	Leave Pad output control unlocked.
GpioPadUnlock	Leave both Pad configuration and output control unlocked.
GpioPadLock	Lock both Pad configuration and output control.

Definition at line [297](#) of file [GpioConfig.h](#).

## enum GPIO\_OTHER\_CONFIG

---

Other GPIO Configuration GPIO\_OTHER\_CONFIG is used for less often settings and for future extensions Supported settings:

- RX raw override to '1' - allows to override input value to '1' This setting is applicable only if in input mode (both in GPIO and native usage). The override takes place at the internal pad state directly from buffer and before the RXINV.

Enumerator	
GpioRxRaw1Default	Use default input override value.
GpioRxRaw1Dis	Don't override input.
GpioRxRaw1En	Override input to '1'.

Definition at line [323](#) of file [GpioConfig.h](#).

## enum GPIO\_OUTPUT\_STATE

---

GPIO Output State This field is relevant only if output is enabled.

Enumerator	
GpioOutDefault	Leave output value unmodified.
GpioOutLow	Set output to low.
GpioOutHigh	Set output to high.

Definition at line [163](#) of file **GpioConfig.h**.

## enum GPIO\_PAD\_MODE

---

GPIO Pad Mode Refer to GPIO documentation on native functions available for certain pad.

If GPIO is set to one of NativeX modes then following settings are not applicable and can be skipped:

- Interrupt related settings
- Host Software Ownership
- Output/Input enabling/disabling
- Output lock

Definition at line [113](#) of file **GpioConfig.h**.

## enum GPIO\_RESET\_CONFIG

---

GPIO Power Configuration GPIO\_RESET\_CONFIG allows to set GPIO Reset type (PADCFG\_DW0.PadRstCfg) which will be used to reset certain GPIO settings.

Refer to EDS for settings that are controllable by PadRstCfg.

Enumerator	
GpioResetDefault	Leave value of pad reset unmodified.
GpioResumeReset	Resume Reset (RSMRST) GPP: PadRstCfg = 00b = "Powergood" GPD: PadRstCfg = 11b = "Resume Reset" Pad

	<p>setting will reset on:</p> <ul style="list-style-type: none"> <li>• DeepSx transition</li> <li>• G3 Pad settings will not reset on:</li> <li>• S3/S4/S5 transition</li> <li>• Warm/Cold/Global reset</li> </ul>
GpioHostDeepReset	<p>Host Deep Reset PadRstCfg = 01b = "Deep GPIO Reset" Pad settings will reset on:</p> <ul style="list-style-type: none"> <li>• Warm/Cold/Global reset</li> <li>• DeepSx transition</li> <li>• G3 Pad settings will not reset on:</li> <li>• S3/S4/S5 transition</li> </ul>
GpioPlatformReset	<p>Platform Reset (PLTRST) PadRstCfg = 10b = "GPIO Reset" Pad settings will reset on:</p> <ul style="list-style-type: none"> <li>• S3/S4/S5 transition</li> <li>• Warm/Cold/Global reset</li> <li>• DeepSx transition</li> <li>• G3</li> </ul>
GpioDswReset	<p>Deep Sleep Well Reset (DSW_PWROK)  GPP: not applicable GPD: PadRstCfg = 00b = "Powergood" Pad settings will reset on:</p> <ul style="list-style-type: none"> <li>• G3 Pad settings will not reset on:</li> <li>• S3/S4/S5 transition</li> <li>• Warm/Cold/Global reset</li> <li>• DeepSx transition</li> </ul>

Definition at line [211](#) of file [GpioConfig.h](#).



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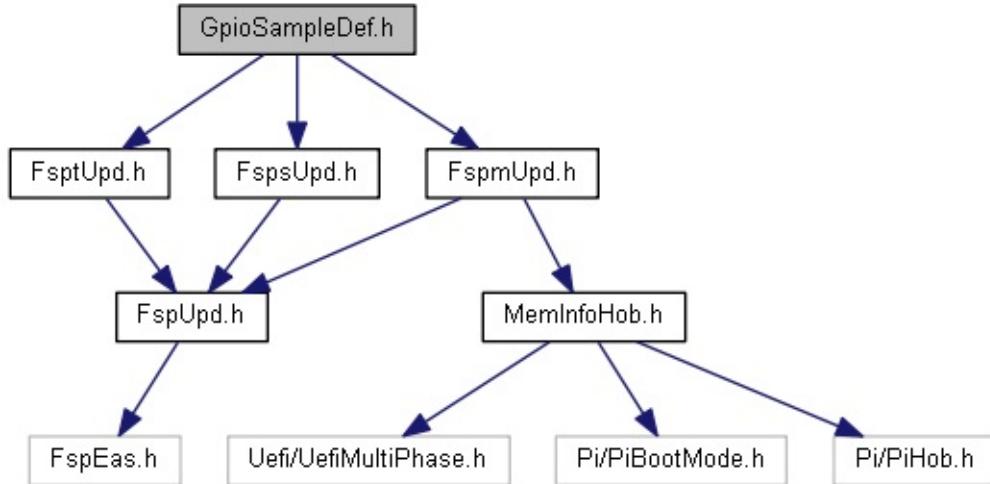
Include >

## GpioSampleDef.h File Reference

Sample enum definitions for GPIO table. More...

```
#include <FsptUpd.h> #include <FspmUpd.h>
#include <FspsUpd.h>
```

Include dependency graph for GpioSampleDef.h:



Go to the source code of this file.

## Detailed Description

---

Sample enum definitions for GPIO table.

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IMPLIED.

### Specification Reference:

Definition in file [GpioSampleDef.h](#).

---

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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Classes

## HobUsageDataHob.h File Reference

Definitions for Hob Usage data HOB. [More...](#)

[Go to the source code of this file.](#)

## Classes

---

struct **HOB\_USAGE\_DATA\_HOB**  
Hob Usage Data Hob. More...

---

## Detailed Description

---

Definitions for Hob Usage data HOB.

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### Specification Reference:

Definition in file **HobUsageDataHob.h**.

---

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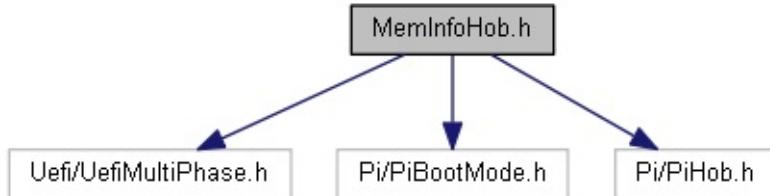
[Classes](#) | [Macros](#)

## MemInfoHob.h File Reference

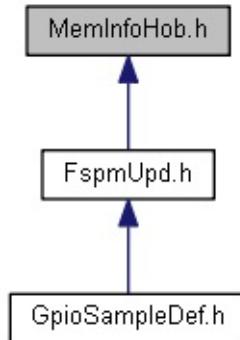
This file contains definitions required for creation of Memory S3 Save data, Memory Info data and Memory Platform data hobs. [More...](#)

```
#include <Uefi/UefiMultiPhase.h> #include <Pi/PiBootMode.h>  
#include <Pi/PiHob.h>
```

Include dependency graph for MemInfoHob.h:



This graph shows which files directly or indirectly include this file:



[Go to the source code of this file.](#)

## Classes

---

struct **DIMM\_INFO**

Memory SMBIOS & OC Memory Data Hob. [More...](#)

struct **MEMORY\_PLATFORM\_DATA**

Memory Platform Data Hob. [More...](#)

---

## Macros

---

```
#define WARM_BOOT 2  
Host reset states from MRC.
```

```
#define MAX_SPD_SAVE 29  
Defines taken from MRC so avoid having to include  
MrclInterface.h.
```

---

## Detailed Description

---

This file contains definitions required for creation of Memory S3 Save data, Memory Info data and Memory Platform data hobs.

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### Specification Reference:

Definition in file **MemInfoHob.h**.



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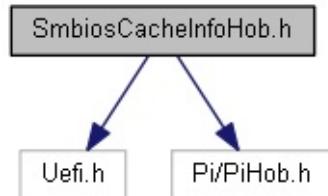
Classes

## SmbiosCacheInfoHob.h File Reference

Header file for SMBIOS Cache Info HOB. [More...](#)

```
#include <Uefi.h> #include <Pi/PiHob.h>
```

Include dependency graph for SmbiosCacheInfoHob.h:



[Go to the source code of this file.](#)

## Classes

---

struct **SMBIOS\_CACHE\_INFO**

SMBIOS Cache Info HOB Structure. [More...](#)

---

## Detailed Description

---

Header file for SMBIOS Cache Info HOB.

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System Management BIOS (SMBIOS) Reference Specification v3.1.0  
dated 2016-Nov-16 (DSP0134)  
[http://www.dmtf.org/sites/default/files/standards/documents/DSP0134\\_3](http://www.dmtf.org/sites/default/files/standards/documents/DSP0134_3).

Definition in file **SmbiosCacheInfoHob.h**.



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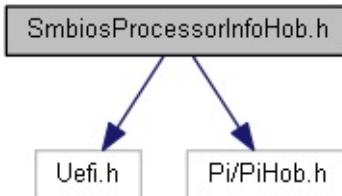
Classes

## SmbiosProcessorInfoHob.h File Reference

Header file for SMBIOS Processor Info HOB. [More...](#)

```
#include <Uefi.h> #include <Pi/PiHob.h>
```

Include dependency graph for SmbiosProcessorInfoHob.h:



[Go to the source code of this file.](#)

## Classes

---

struct **SMBIOS\_PROCESSOR\_INFO**

SMBIOS Processor Info HOB Structure. More...

---

## Detailed Description

---

Header file for SMBIOS Processor Info HOB.

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dated 2016-Nov-16 (DSP0134)  
[http://www.dmtf.org/sites/default/files/standards/documents/DSP0134\\_3](http://www.dmtf.org/sites/default/files/standards/documents/DSP0134_3).

Definition in file **SmbiosProcessorInfoHob.h**.



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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b	g	m	p	s	w

Here is a list of all documented file members with links to the documentation:

## - b -

- B\_GPIO\_ELECTRICAL\_CONFIG\_TERMINATION\_MASK : [GpioConfig.h](#)
- B\_GPIO\_INT\_CONFIG\_INT\_SOURCE\_MASK : [GpioConfig.h](#)
- B\_GPIO\_INT\_CONFIG\_INT\_TYPE\_MASK : [GpioConfig.h](#)
- B\_GPIO\_LOCK\_CONFIG\_OUTPUT\_LOCK\_MASK : [GpioConfig.h](#)
- B\_GPIO\_LOCK\_CONFIG\_PAD\_CONF\_LOCK\_MASK : [GpioConfig.h](#)
- B\_GPIO\_OTHER\_CONFIG\_RXRAW\_MASK : [GpioConfig.h](#)

## - g -

- GPIO\_DIRECTION : [GpioConfig.h](#)
- GPIO\_ELECTRICAL\_CONFIG : [GpioConfig.h](#)
- GPIO\_GROUP : [GpioConfig.h](#)
- GPIO\_HARDWARE\_DEFAULT : [GpioConfig.h](#)
- GPIO\_HOSTSW\_OWN : [GpioConfig.h](#)
- GPIO\_INT\_CONFIG : [GpioConfig.h](#)
- GPIO\_LOCK\_CONFIG : [GpioConfig.h](#)

- GPIO\_OTHER\_CONFIG : [GpioConfig.h](#)
- GPIO\_OUTPUT\_STATE : [GpioConfig.h](#)
- GPIO\_PAD : [GpioConfig.h](#)
- GPIO\_PAD\_MODE : [GpioConfig.h](#)
- GPIO\_RESET\_CONFIG : [GpioConfig.h](#)
- GpioDirDefault : [GpioConfig.h](#)
- GpioDirIn : [GpioConfig.h](#)
- GpioDirInInv : [GpioConfig.h](#)
- GpioDirInInvOut : [GpioConfig.h](#)
- GpioDirInOut : [GpioConfig.h](#)
- GpioDirNone : [GpioConfig.h](#)
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- GpioDswReset : [GpioConfig.h](#)
- GpioHardwareDefault : [GpioConfig.h](#)
- GpioHostDeepReset : [GpioConfig.h](#)
- GpioHostOwnAcpi : [GpioConfig.h](#)
- GpioHostOwnDefault : [GpioConfig.h](#)
- GpioHostOwnGpio : [GpioConfig.h](#)
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- GpioIntBothEdge : [GpioConfig.h](#)
- GpioIntDefault : [GpioConfig.h](#)
- GpioIntDis : [GpioConfig.h](#)
- GpioIntEdge : [GpioConfig.h](#)
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- GpioIntLvlEdgDis : [GpioConfig.h](#)
- GpioIntNmi : [GpioConfig.h](#)
- GpioIntSci : [GpioConfig.h](#)
- GpioIntSmi : [GpioConfig.h](#)
- GpioLockDefault : [GpioConfig.h](#)
- GpioOutDefault : [GpioConfig.h](#)
- GpioOutHigh : [GpioConfig.h](#)
- GpioOutLow : [GpioConfig.h](#)
- GpioOutputStateUnlock : [GpioConfig.h](#)
- GpioPadConfigLock : [GpioConfig.h](#)
- GpioPadConfigUnlock : [GpioConfig.h](#)
- GpioPadLock : [GpioConfig.h](#)
- GpioPadUnlock : [GpioConfig.h](#)
- GpioPlatformReset : [GpioConfig.h](#)
- GpioResetDefault : [GpioConfig.h](#)
- GpioResumeReset : [GpioConfig.h](#)

- GpioRxRaw1Default : [GpioConfig.h](#)
- GpioRxRaw1Dis : [GpioConfig.h](#)
- GpioRxRaw1En : [GpioConfig.h](#)
- GpioTermDefault : [GpioConfig.h](#)
- GpioTermNative : [GpioConfig.h](#)
- GpioTermNone : [GpioConfig.h](#)
- GpioTermWpd20K : [GpioConfig.h](#)
- GpioTermWpd5K : [GpioConfig.h](#)
- GpioTermWpu1K : [GpioConfig.h](#)
- GpioTermWpu1K2K : [GpioConfig.h](#)
- GpioTermWpu20K : [GpioConfig.h](#)
- GpioTermWpu2K : [GpioConfig.h](#)
- GpioTermWpu5K : [GpioConfig.h](#)

- m -

- MAX\_SPD\_SAVE : [MemInfoHob.h](#)

- p -

- PcdFspAreaBaseAddress : [FspFixedPcds.h](#)
- PcdFspImageIdString : [FspFixedPcds.h](#)
- PcdFspReservedBufferSize : [FspFixedPcds.h](#)
- PcdGlobalDataPointerAddress : [FspFixedPcds.h](#)
- PcdSiliconInitVersionBuild : [FspFixedPcds.h](#)
- PcdSiliconInitVersionMajor : [FspFixedPcds.h](#)
- PcdSiliconInitVersionMinor : [FspFixedPcds.h](#)
- PcdSiliconInitVersionRevision : [FspFixedPcds.h](#)
- PcdTemporaryRamBase : [FspFixedPcds.h](#)
- PcdTemporaryRamSize : [FspFixedPcds.h](#)

- s -

- SI\_PCH\_INT\_PIN : [FspsUpd.h](#)
- SI\_PCH\_MAX\_DEVICE\_INTERRUPT\_CONFIG : [FspsUpd.h](#)
- SiPchNolInt : [FspsUpd.h](#)

- w -

- WARM\_BOOT : **MemInfoHob.h**
- 

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- GPIO\_GROUP : [GpioConfig.h](#)
- GPIO\_PAD : [GpioConfig.h](#)

---

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File List	File Members			
All	TypeDefs	Enumerations	Enumerator	Macros

- GPIO\_DIRECTION : [GpioConfig.h](#)
- GPIO\_ELECTRICAL\_CONFIG : [GpioConfig.h](#)
- GPIO\_HARDWARE\_DEFAULT : [GpioConfig.h](#)
- GPIO\_HOSTSW OWN : [GpioConfig.h](#)
- GPIO\_INT\_CONFIG : [GpioConfig.h](#)
- GPIO\_LOCK\_CONFIG : [GpioConfig.h](#)
- GPIO\_OTHER\_CONFIG : [GpioConfig.h](#)
- GPIO\_OUTPUT\_STATE : [GpioConfig.h](#)
- GPIO\_PAD\_MODE : [GpioConfig.h](#)
- GPIO\_RESET\_CONFIG : [GpioConfig.h](#)
- SI\_PCH\_INT\_PIN : [FspsUpd.h](#)



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- GpioDirDefault : [GpioConfig.h](#)
- GpioDirIn : [GpioConfig.h](#)
- GpioDirInInv : [GpioConfig.h](#)
- GpioDirInInvOut : [GpioConfig.h](#)
- GpioDirInOut : [GpioConfig.h](#)
- GpioDirNone : [GpioConfig.h](#)
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- GpioDswReset : [GpioConfig.h](#)
- GpioHardwareDefault : [GpioConfig.h](#)
- GpioHostDeepReset : [GpioConfig.h](#)
- GpioHostOwnAcpi : [GpioConfig.h](#)
- GpioHostOwnDefault : [GpioConfig.h](#)
- GpioHostOwnGpio : [GpioConfig.h](#)
- GpioIntApic : [GpioConfig.h](#)
- GpioIntBothEdge : [GpioConfig.h](#)
- GpioIntDefault : [GpioConfig.h](#)
- GpioIntDis : [GpioConfig.h](#)
- GpioIntEdge : [GpioConfig.h](#)
- GpioIntLevel : [GpioConfig.h](#)
- GpioIntLvlEdgDis : [GpioConfig.h](#)

- GpioIntNmi : [GpioConfig.h](#)
- GpioIntSci : [GpioConfig.h](#)
- GpioIntSmi : [GpioConfig.h](#)
- GpioLockDefault : [GpioConfig.h](#)
- GpioOutDefault : [GpioConfig.h](#)
- GpioOutHigh : [GpioConfig.h](#)
- GpioOutLow : [GpioConfig.h](#)
- GpioOutputStateUnlock : [GpioConfig.h](#)
- GpioPadConfigLock : [GpioConfig.h](#)
- GpioPadConfigUnlock : [GpioConfig.h](#)
- GpioPadLock : [GpioConfig.h](#)
- GpioPadUnlock : [GpioConfig.h](#)
- GpioPlatformReset : [GpioConfig.h](#)
- GpioResetDefault : [GpioConfig.h](#)
- GpioResumeReset : [GpioConfig.h](#)
- GpioRxRaw1Default : [GpioConfig.h](#)
- GpioRxRaw1Dis : [GpioConfig.h](#)
- GpioRxRaw1En : [GpioConfig.h](#)
- GpioTermDefault : [GpioConfig.h](#)
- GpioTermNative : [GpioConfig.h](#)
- GpioTermNone : [GpioConfig.h](#)
- GpioTermWpd20K : [GpioConfig.h](#)
- GpioTermWpd5K : [GpioConfig.h](#)
- GpioTermWpu1K : [GpioConfig.h](#)
- GpioTermWpu1K2K : [GpioConfig.h](#)
- GpioTermWpu20K : [GpioConfig.h](#)
- GpioTermWpu2K : [GpioConfig.h](#)
- GpioTermWpu5K : [GpioConfig.h](#)

- S -

- SiPchNolnt : [FspSUpd.h](#)



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- B\_GPIO\_ELECTRICAL\_CONFIG\_TERMINATION\_MASK : [GpioConfig.h](#)
- B\_GPIO\_INT\_CONFIG\_INT\_SOURCE\_MASK : [GpioConfig.h](#)
- B\_GPIO\_INT\_CONFIG\_INT\_TYPE\_MASK : [GpioConfig.h](#)
- B\_GPIO\_LOCK\_CONFIG\_OUTPUT\_LOCK\_MASK : [GpioConfig.h](#)
- B\_GPIO\_LOCK\_CONFIG\_PAD\_CONF\_LOCK\_MASK : [GpioConfig.h](#)
- B\_GPIO\_OTHER\_CONFIG\_RXRAW\_MASK : [GpioConfig.h](#)
- MAX\_SPD\_SAVE : [MemInfoHob.h](#)
- PcdFspAreaBaseAddress : [FspFixedPcds.h](#)
- PcdFspImageIdString : [FspFixedPcds.h](#)
- PcdFspReservedBufferSize : [FspFixedPcds.h](#)
- PcdGlobalDataPointerAddress : [FspFixedPcds.h](#)
- PcdSiliconInitVersionBuild : [FspFixedPcds.h](#)
- PcdSiliconInitVersionMajor : [FspFixedPcds.h](#)
- PcdSiliconInitVersionMinor : [FspFixedPcds.h](#)
- PcdSiliconInitVersionRevision : [FspFixedPcds.h](#)
- PcdTemporaryRamBase : [FspFixedPcds.h](#)
- PcdTemporaryRamSize : [FspFixedPcds.h](#)
- SI\_PCH\_MAX\_DEVICE\_INTERRUPT\_CONFIG : [FspUpd.h](#)
- WARM\_BOOT : [MemInfoHob.h](#)

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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## Related Pages

Here is a list of all related documentation pages:

[FSP OVERVIEW](#)

# FSP Overview

## 2.1 Technical Overview

The *Intel® Firmware Support Package (FSP)* provides chipset and processor initialization in a format that can easily be incorporated into many existing boot loaders

### **FSP INTEGRATION**

---

# **3 FSP Integration**

## **FSP PORTING RECOMMENDATION**

---

# **4 FSP Porting Recommendation**

Here listed some notes or recommendation when porting with FSP  
**UPD PORTING GUIDE**

---

---

# 5 UPD porting guide

FSP OUTPUT

---

# **6 FSP Output**

The FSP builds a series of data structures called the Hand-Off-Blocks (HOBs) as it progresses through initializing the silicon

## **FSP POSTCODE**

# 7 FSP PostCode

The FSP outputs 16 bit postcode to indicate which API and in which module the execution is happening

[Todo List](#)

[Deprecated List](#)

---

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## AUDIO\_AZALIA\_VERB\_TABLE Member List

This is the complete list of members for [AUDIO\\_AZALIA\\_VERB\\_TABLE](#), including all inherited members.

Data [AUDIO\\_AZALIA\\_VERB\\_TABLE](#)  
Header [AUDIO\\_AZALIA\\_VERB\\_TABLE](#)

---

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## FspSUpd.h

Go to the documentation of this file.

```
1  /** @file
2
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18   other materials provided with the
19   distribution.
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29 CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT
30 LIMITED TO, PROCUREMENT OF
31 SUBSTITUTE GOODS OR SERVICES; LOSS OF USE,
32 DATA, OR PROFITS; OR BUSINESS
33 INTERRUPTION) HOWEVER CAUSED AND ON ANY
34 THEORY OF LIABILITY, WHETHER IN
35 CONTRACT, STRICT LIABILITY, OR TORT
36 (INCLUDING NEGLIGENCE OR OTHERWISE)
37 ARISING IN ANY WAY OUT OF THE USE OF THIS
38 SOFTWARE, EVEN IF ADVISED OF
39 THE POSSIBILITY OF SUCH DAMAGE.
40
41 This file is automatically generated.
42 Please do NOT modify !!!
43
44 */
45
46 #ifndef __FSPSUPD_H__
47 #define __FSPSUPD_H__
48
49
50 #include <FspUpd.h>
```

```
37
38 #pragma pack(1)
39
40
41 /**
42 /// Azalia Header structure
43 /**
44 typedef struct {
45     UINT16 VendorId;           ///< Codec
46     Vendor ID
47     UINT16 DeviceId;          ///< Codec
48     Device ID
49     UINT8 RevisionId;         ///< Revision
50     ID of the codec. 0xFF matches any revision.
51     UINT8 SdiNum;             ///< SDI
52     number, 0xFF matches any SDI.
53     UINT16 DataDwords;        ///< Number of
54     data DWORDS pointed by the codec data buffer.
55     UINT32 Reserved;          ///< Reserved
56     for future use. Must be set to 0.
57 } AZALIA_HEADER;
58
59 /**
60 /// Audio Azalia Verb Table structure
61 /**
62 typedef struct {
63     AZALIA_HEADER Header;      ///< AZALIA PCH
64     header
65     UINT32 *Data;              ///< Pointer to
66     the data buffer. Its length is specified in
67     the header
68 } AUDIO_AZALIA_VERB_TABLE;
69
70 /**
71 /// Refer to the definition of PCH_INT_PIN
72 /**
73 typedef enum {
```

```

65     SiPchNoInt,           ///< No Interrupt Pin
66     SiPchIntA,
67     SiPchIntB,
68     SiPchIntC,
69     SiPchIntD
70 } SI_PCH_INT_PIN;
71 /**
72 /// The PCH_DEVICE_INTERRUPT_CONFIG block
    describes interrupt pin, IRQ and interrupt
    mode for PCH device.
73 /**
74 typedef struct {
75     UINT8      Device;          ///<
    Device number
76     UINT8      Function;       ///<
    Device function
77     UINT8      IntX;          ///<
    Interrupt pin: INTA-INTD (see SI_PCH_INT_PIN)
78     UINT8      Irq;           ///<
    IRQ to be set for device.
79 } SI_PCH_DEVICE_INTERRUPT_CONFIG;
80
81 #define SI_PCH_MAX_DEVICE_INTERRUPT_CONFIG
82     64           ///< Number of all PCH devices
83
84 /**
85 ** Fsp S Configuration
86 */
87 typedef struct {
88 /**
89 ** Offset 0x0020 - Logo Pointer
    Points to PEI Display Logo Image
90 */
91     UINT32      LogoPtr;
92
93 /**
94 ** Offset 0x0024 - Logo Size
    Size of PEI Display Logo Image

```

```
95  */
96 	UINT32 				LogoSize;
97
98 /** Offset 0x0028 - Graphics Configuration
99  Ptr
100 */
101(UINT32
102	GraphicsConfigPtr;
103/** Offset 0x002C - Enable Device 4
104  Enable/disable Device 4
105  $EN_DIS
106 */
107(UINT8
108				Device4Enable;
109/** Offset 0x002D - Enable HD Audio DSP
110  Enable/disable HD Audio DSP feature.
111  $EN_DIS
112 */
113(UINT8
114	PchHdaDspEnable;
115/** Offset 0x002E
116 */
117(UINT8
118UNUSEDUpdSpace0[3];
119/** Offset 0x0031 - Enable eMMC Controller
120  Enable/disable eMMC Controller.
121  $EN_DIS
122 */
123(UINT8
124ScsEmmcEnabled;
125/** Offset 0x0032 - Enable eMMC HS400 Mode
126  Enable eMMC HS400 Mode.
```

```
127     $EN_DIS
128     */
129     UINT8
130     ScsEmmcHs400Enabled;
131     /** Offset 0x0033 - Enable SdCard Controller
132     Enable/disable SD Card Controller.
133     $EN_DIS
134     */
135     UINT8
136     ScsSdCardEnabled;
137     /** Offset 0x0034 - Show SPI controller
138     Enable/disable to show SPI controller.
139     $EN_DIS
140     */
141     UINT8
142     ShowSpiController;
143     /** Offset 0x0035
144     */
145     UINT8
146     UnusedUpdSpace1[3];
147     /** Offset 0x0038 - MicrocodeRegionBase
148     Memory Base of Microcode Updates
149     */
150     UINT32
151     MicrocodeRegionBase;
152     /** Offset 0x003C - MicrocodeRegionSize
153     Size of Microcode Updates
154     */
155     UINT32
156     MicrocodeRegionSize;
157     /** Offset 0x0040 - Turbo Mode
```

```
158     Enable/Disable Turbo mode. 0: disable, 1: enable
159     $EN_DIS
160     */
161     UINT8                               TurboMode;
162
163     /** Offset 0x0041 - Enable SATA SALP Support
164      Enable/disable SATA Aggressive Link Power
165      Management.
166      $EN_DIS
167      */
168      UINT8
169      SataSalpSupport;
170
171      /** Offset 0x0042 - Enable SATA ports
172      Enable/disable SATA ports. One byte for
173      each port, byte0 for port0, byte1 for port1,
174      and so on.
175      */
176      UINT8
177      SataPortsEnable[8];
178
179      /** Offset 0x004A - Enable SATA DEVSLP
180      Feature
181      Enable/disable SATA DEVSLP per port. 0 is
182      disable, 1 is enable. One byte for each
183      port, byte0 for port0, byte1 for port1,
184      and so on.
185      */
186      UINT8
187      SataPortsDevSlp[8];
188
189      /** Offset 0x0052 - Enable USB2 ports
190      Enable/disable per USB2 ports. One byte
191      for each port, byte0 for port0, byte1 for
192      port1, and so on.
193      */
194
```

```
185     UINT8
186     PortUsb20Enable[16];
187 /**
188  ** Offset 0x0062 - Enable USB3 ports
189  ** Enable/disable per USB3 ports. One byte
190  ** for each port, byte0 for port0, byte1 for
191  ** port1, and so on.
192 */
193     UINT8
194     PortUsb30Enable[10];
195 /**
196  ** Offset 0x006C - Enable xDCI controller
197  ** Enable/disable to xDCI controller.
198  ** $EN_DIS
199 */
200     UINT8
201     XdciEnable;
202
203 /**
204  ** Offset 0x006D
205  ** Enable SerialIo Device
206  ** Mode
207  ** 0:Disabled, 1:PCI Mode, 2:Acpi mode,
208  ** 3:Hidden mode (Legacy UART mode) -
209  ** Enable/disable
210  ** SerialIo
211  ** I2C0, I2C1, I2C2, I2C3, I2C4, I2C5, SPI0, SPI1, SPI2, U
212  ** ART0, UART1, UART2 device
213  ** mode respectively. One byte for each
214  ** controller, byte0 for I2C0, byte1 for I2C1,
215  ** and so on.
216 */
217     UINT8
218     SerialIoDevMode[12];
219
220
```

```

211 /** Offset 0x007B - Address of
212   PCH_DEVICE_INTERRUPT_CONFIG table.
213 */
214   UINT32
215     DevIntConfigPtr;
216 /**
217   ** Offset 0x007F - Number of DevIntConfig
218   Entry
219   Number of Device Interrupt Configuration
220   Entry. If this is not zero, the
221   DevIntConfigPtr
222   must not be NULL.
223 */
224   UINT8
225     NumOfDevIntConfig;
226 /**
227   ** Offset 0x0080 - PIRQx to IRQx Map Config
228   PIRQx to IRQx mapping. The valid value is
229   0x00 to 0x0F for each. First byte is for
230   PIRQA, second byte is for PIRQB, and so
231   on. The setting is only available in Legacy
232   8259 PCI mode.
233 */
234   UINT8
235     PxRcConfig[8];
236 /**
237   ** Offset 0x0088 - Select GPIO IRQ Route
238   GPIO IRQ Select. The valid value is 14 or
239   15.
240 */
241   UINT8
242     GpioIrqRoute;
243 /**
244   ** Offset 0x0089 - Select SciIrqSelect
245   SCI IRQ Select. The valid value is 9, 10,
246   11, and 20, 21, 22, 23 for APIC only.
247 */

```

```
237     UINT8           SciIrqSelect;
238
239 /** Offset 0x008A - Select TcoIrqSelect
240   TCO IRQ Select. The valid value is 9, 10,
241   11, 20, 21, 22, 23.
242 */
243     UINT8           TcoIrqSelect;
244
245 /** Offset 0x008B - Enable/Disable Tco IRQ
246   Enable/disable TCO IRQ
247   $EN_DIS
248 */
249     UINT8           TcoIrqEnable;
250
251 /** Offset 0x008C - PCH HDA Verb Table Entry
252   Number
253   Number of Entries in Verb Table.
254 */
255     UINT8           PchHdaVerbTableEntryNum;
256
257 /** Offset 0x008D - PCH HDA Verb Table
258   Pointer
259   Pointer to Array of pointers to Verb
260   Table.
261 */
262     UINT32          PchHdaVerbTablePtr;
263
264 /** Offset 0x0091 - PCH HDA Codec Sx Wake
265   Capability
266   Capability to detect wake initiated by a
267   codec in Sx
268 */
269     UINT8           PchHdaCodecSxWakeCapability;
```

```
265 /** Offset 0x0092 - Enable SATA
266     Enable/disable SATA controller.
267     $EN_DIS
268 */
269     UINT8                     SataEnable;
270
271 /** Offset 0x0093 - SATA Mode
272     Select SATA controller working mode.
273     0:AHCI, 1:RAID
274 */
275     UINT8                     SataMode;
276
277 /** Offset 0x0094 - USB Per Port HS
278     Preemphasis Bias
279     USB Per Port HS Preemphasis Bias. 000b-
280     0mV, 001b-11.25mV, 010b-16.9mV, 011b-28.15mV,
281     100b-28.15mV, 101b-39.35mV, 110b-45mV,
282     111b-56.3mV. One byte for each port.
283 */
284     UINT8
285     Usb2AfePetxiset[16];
286
287 /** Offset 0x00A4 - USB Per Port HS
288     Transmitter Bias
289     USB Per Port HS Transmitter Bias. 000b-
290     0mV, 001b-11.25mV, 010b-16.9mV, 011b-28.15mV,
291     100b-28.15mV, 101b-39.35mV, 110b-45mV,
292     111b-56.3mV, One byte for each port.
293 */
294     UINT8
295     Usb2AfeTxiset[16];
296
297 /** Offset 0x00B4 - USB Per Port HS
298     Transmitter Emphasis
299     USB Per Port HS Transmitter Emphasis. 00b
300     - Emphasis OFF, 01b - De-emphasis ON,
301     10b - Pre-emphasis ON, 11b - Pre-emphasis
```

```
    & De-emphasis ON. One byte for each port.  
292    /**/  
293    UINT8  
        Usb2AfePredeemp[16];  
294  
295    /** Offset 0x00C4 - USB Per Port Half Bit  
        Pre-emphasis  
296    USB Per Port Half Bit Pre-emphasis. 1b -  
        half-bit pre-emphasis, 0b - full-bit pre-  
        emphasis.  
297    One byte for each port.  
298    /**/  
299    UINT8  
        Usb2AfePehalfbit[16];  
300  
301    /** Offset 0x00D4 - Enable the write to USB  
        3.0 TX Output -3.5dB De-Emphasis Adjustment  
302    Enable the write to USB 3.0 TX Output  
        -3.5dB De-Emphasis Adjustment. Each value  
303    in arrary can be between 0-1. One byte for  
        each port.  
304    /**/  
305    UINT8  
        Usb3HsioTxDeEmphEnable[10];  
306  
307    /** Offset 0x00DE - USB 3.0 TX Output -3.5dB  
        De-Emphasis Adjustment Setting  
308    USB 3.0 TX Output -3.5dB De-Emphasis  
        Adjustment Setting, HSI0_TX_DWORD5[21:16],  
309    <b>Default = 29h</b> (approximately -3.5dB  
        De-Emphasis). One byte for each port.  
310    /**/  
311    UINT8  
        Usb3HsioTxDeEmph[10];  
312  
313    /** Offset 0x00E8 - Enable the write to USB  
        3.0 TX Output Downscale Amplitude Adjustment
```

```
314     Enable the write to USB 3.0 TX Output  
315     Downscale Amplitude Adjustment, Each value  
316     in array can be between 0-1. One byte for  
317     each port.  
316     */  
317     UINT8  
318         Usb3HsioTxDownscaleAmpEnable[10];  
318  
319     /** Offset 0x00F2 - USB 3.0 TX Output  
320     Downscale Amplitude Adjustment  
321     USB 3.0 TX Output Downscale Amplitude  
322     Adjustment, HSI0_TX_DWORD8[21:16], <b>Default  
321     = 00h</b>. One byte for each port.  
322     */  
323     UINT8  
323         Usb3HsioTxDownscaleAmp[10];  
324  
325     /** Offset 0x00FC - Enable LAN  
326     Enable/disable LAN controller.  
327     $EN_DIS  
328     */  
329     UINT8                                PchLanEnable;  
330  
331     /** Offset 0x00FD - Enable HD Audio Link  
332     Enable/disable HD Audio Link. Muxed with  
332     SSP0/SSP1/SNDW1.  
333     $EN_DIS  
334     */  
335     UINT8  
335         PchHdaAudioLinkHda;  
336  
337     /** Offset 0x00FE - Enable HD Audio DMIC0  
338     Link  
338     Enable/disable HD Audio DMIC0 link. Muxed  
338     with SNDW4.  
339     $EN_DIS  
340     */
```

```
341     UINT8
342         PchHdaAudioLinkDmic0;
343     /** Offset 0x00FF - Enable HD Audio DMIC1
344      Link
345      Enable/disable HD Audio DMIC1 link. Muxed
346      with SNDW3.
347      $EN_DIS
348      */
349     UINT8
350         PchHdaAudioLinkDmic1;
351     /** Offset 0x0100 - Enable HD Audio SSP0
352      Link
353      Enable/disable HD Audio SSP0/I2S link.
354      Muxed with HDA.
355      $EN_DIS
356      */
357     UINT8
358         PchHdaAudioLinkSsp0;
359     /** Offset 0x0101 - Enable HD Audio SSP1
360      Link
361      Enable/disable HD Audio SSP1/I2S link.
362      Muxed with HDA/SNDW2.
363      $EN_DIS
364      */
365     UINT8
366         PchHdaAudioLinkSsp1;
367     /** Offset 0x0102 - Enable HD Audio SSP2
368      Link
369      Enable/disable HD Audio SSP2/I2S link.
370      $EN_DIS
371      */
372     UINT8
373         PchHdaAudioLinkSsp2;
```

```
366
367 /** Offset 0x0103 - Enable HD Audio
   SoundWire#1 Link
368   Enable/disable HD Audio SNDW1 link. Muxed
   with HDA.
369   $EN_DIS
370 */
371   UINT8
   PchHdaAudioLinkSndw1;
372
373 /** Offset 0x0104 - Enable HD Audio
   SoundWire#2 Link
374   Enable/disable HD Audio SNDW2 link. Muxed
   with SSP1.
375   $EN_DIS
376 */
377   UINT8
   PchHdaAudioLinkSndw2;
378
379 /** Offset 0x0105 - Enable HD Audio
   SoundWire#3 Link
380   Enable/disable HD Audio SNDW3 link. Muxed
   with DMIC1.
381   $EN_DIS
382 */
383   UINT8
   PchHdaAudioLinkSndw3;
384
385 /** Offset 0x0106 - Enable HD Audio
   SoundWire#4 Link
386   Enable/disable HD Audio SNDW4 link. Muxed
   with DMIC0.
387   $EN_DIS
388 */
389   UINT8
   PchHdaAudioLinkSndw4;
390
```

```
391 /** Offset 0x0107 - Soundwire Clock Buffer
   GPIO RCOMP Setting
392   0: non-ACT - 50 Ohm driver impedance, 1:
      ACT - 8 Ohm driver impedance.
393   $EN_DIS
394 */
395   UINT8
396     PchHdaSndwBufferRcomp;
397
398 /**
399  ** Offset 0x0108 - PTM for PCIE RP Mask
400  Enable/disable Precision Time Measurement
401  for PCIE Root Ports. 0: disable, 1: enable.
402  One bit for each port, bit0 for port1,
403  bit1 for port2, and so on.
404 */
405   UINT32
406     PcieRpPtmMask;
407
408 /**
409  ** Offset 0x010C - DPC for PCIE RP Mask
410  Enable/disable Downstream Port Containment
411  for PCIE Root Ports. 0: disable, 1: enable.
412  One bit for each port, bit0 for port1,
413  bit1 for port2, and so on.
414 */
415   UINT32
416     PcieRpDpcMask;
417
418 /**
419  ** Offset 0x0110 - DPC Extensions PCIE RP
420  Mask
421  Enable/disable DPC Extensions for PCIE
422  Root Ports. 0: disable, 1: enable. One bit
423  for each port, bit0 for port1, bit1 for
424  port2, and so on.
425 */
426   UINT32
427     PcieRpDpcExtensionsMask;
428
429 /**
430  ** Offset 0x0114 - USB PDO Programming
431  Enable/disable PDO programming for USB in
```

```
    PEI phase. Disabling will allow for
    programming
417    during later phase. 1: enable, 0: disable
418    $EN_DIS
419    */
420    UINT8
        UsbPdoProgramming;
421
422    /** Offset 0x0115 - Power button debounce
        configuration
423    Debounce time for PWRBTN in microseconds.
        For values not supported by HW, they will
424    be rounded down to closest supported on.
        0: disable, 250-1024000us: supported range
425    */
426    UINT32
        PmcPowerButtonDebounce;
427
428    /** Offset 0x0119 - PCH eSPI Master and
        Slave BME enabled
429    PCH eSPI Master and Slave BME enabled
430    $EN_DIS
431    */
432    UINT8
        PchEspiBmeMasterSlaveEnabled;
433
434    /** Offset 0x011A - PCH SATA use RST Legacy
        OROM
435    Use PCH SATA RST Legacy OROM when CSM is
        Enabled
436    $EN_DIS
437    */
438    UINT8
        SataRstLegacyOrrom;
439
440    /** Offset 0x011B - Trace Hub Memory Base
441    If Trace Hub is enabled and trace to
```

```
memory is desired, BootLoader needs to
allocate
442 |     trace hub memory as reserved and
443 |     uncacheable, set the base to ensure Trace Hub
444 |     memory is configured properly.
445 | */
445 |     UINT32
446 |     TraceHubMemBase;
446 |
447 | /** Offset 0x011F - PMC Debug Message Enable
448 |     When Enabled, PMC HW will send debug
449 |     messages to trace hub; When Disabled, PMC HW
449 |     will never send debug meesages to trace
449 |     hub. Noted: When Enabled, may not enter S0ix
450 |     $EN_DIS
451 | */
452 |     UINT8                         PmcDbgMsgEn;
453 |
454 | /** Offset 0x0120 - Pointer of ChipsetInit
455 |     Binary
455 |     ChipsetInit Binary Pointer.
456 | */
457 |     UINT32
457 |     ChipsetInitBinPtr;
458 |
459 | /** Offset 0x0124 - Length of ChipsetInit
460 |     Binary
460 |     ChipsetInit Binary Length.
461 | */
462 |     UINT32
462 |     ChipsetInitBinLen;
463 |
464 | /** Offset 0x0128 - PchPostMemRsvd
465 |     Reserved for PCH Post-Mem
466 |     $EN_DIS
467 | */
468 |     UINT8
```

```
PchPostMemRsvd[29];  
469  
470 /** Offset 0x0145 - Enable Ufs Controller  
471   Enable/disable Ufs 2.0 Controller.  
472   $EN_DIS  
473 **/  
474             UINT8                      ScsUfsEnabled;  
475  
476 /** Offset 0x0146 - CNVi Configuration  
477   This option allows for automatic detection  
of Connectivity Solution. [Auto Detection]  
478   assumes that CNVi will be enabled when  
available, [Disable] allows for disabling  
CNVi.  
479   0:Disable, 1:Auto  
480 **/  
481             UINT8                      PchCnviMode;  
482  
483 /** Offset 0x0147 - SdCard power enable  
polarity  
484   Choose SD_PWREN# polarity  
485   0: Active low, 1: Active high  
486 **/  
487             UINT8  
SdCardPowerEnableActiveHigh;  
488  
489 /** Offset 0x0148 - PCH USB2 PHY Power  
Gating enable  
490   1: Will enable USB2 PHY SUS Well Power  
Gating, 0: Will not enable PG of USB2 PHY  
491   Sus Well PG  
492   $EN_DIS  
493 **/  
494             UINT8  
PchUsb2PhySusPgEnable;  
495  
496 /** Offset 0x0149 - PCH USB OverCurrent
```

```
mapping enable
497    1: Will program USB OC pin mapping in xHCI
controller memory, 0: Will clear OC pin
498    mapping allow for NOA usage of OC pins
499    $EN_DIS
500 */
501    UINT8
PchUsbOverCurrentEnable;
502 /**
503  ** Offset 0x014A
504 */
505    UINT8
UnusedUpdSpace3;
506 /**
507  ** Offset 0x014B - CNVi MfUart1 Type
508  This option configures Uart type which
connects to MfUart1
509  0:ISH Uart0, 1:SerialIO Uart2, 2:Uart over
external pads
510 */
511    UINT8
PchCnviMfUart1Type;
512 /**
513  ** Offset 0x014C - Espi Lgmr Memory Range
decode
514  This option enables or disables espi lgmr
515  $EN_DIS
516 */
517    UINT8
PchEspiLgmrEnable;
518 /**
519  ** Offset 0x014D - HECI3 state
520  The HECI3 state from Mbp for reference in
S3 path or when MbpHob is not installed.
521  0: disable, 1: enable
522  $EN_DIS
523 */
```

```
524     UINT8                               Heci3Enabled;
525
526     /** Offset 0x014E
527     */
528     UINT8                               UnusedUpdSpace4;
529
530     /** Offset 0x014F - PCHHOT# pin
531     Enable PCHHOT# pin assertion when
532     temperature is higher than PchHotLevel. 0:
533     disable, 1: enable
534         $EN_DIS
535     */
536     UINT8                               PchHotEnable;
537
538     /** Offset 0x0150 - SATA LED
539     SATA LED indicating SATA controller
540     activity. 0: disable, 1: enable
541         $EN_DIS
542     */
543     UINT8                               SataLedEnable;
544
545     /** Offset 0x0151 - VRAlert# Pin
546     When VRAlert# feature pin is enabled and
547     its state is '0', the PMC requests throttling
548     to a T3 Tstate to the PCH throttling
549     unit.. 0: disable, 1: enable
550         $EN_DIS
551     */
552     UINT8                               PchPmVrAlert;
553
554     /** Offset 0x0152 - SLP_S0 VM Dynamic
555     Control
556     SLP_S0 Voltage Margining Runtime Control
557     Policy. 0: disable, 1: enable
558         $EN_DIS
559     */
560
```

```
553     UINT8  
554         PchPmSlpS0VmRuntimeControl;  
555     /** Offset 0x0153 - SLP_S0 VM 0.70V Support  
556         SLP_S0 Voltage Margining 0.70V Support  
557         Policy. 0: disable, 1: enable  
558         $EN_DIS  
559     */  
560     UINT8  
561         PchPmSlpS0Vm070VSupport;  
562     /** Offset 0x0154 - SLP_S0 VM 0.75V Support  
563         SLP_S0 Voltage Margining 0.75V Support  
564         Policy. 0: disable, 1: enable  
565         $EN_DIS  
566     */  
567     UINT8  
568         PchPmSlpS0Vm075VSupport;  
569     /** Offset 0x0155 - AMT Switch  
570         Enable/Disable. 0: Disable, 1: enable,  
571         Enable or disable AMT functionality.  
572         $EN_DIS  
573     */  
574     UINT8                     AmtEnabled;  
575     /** Offset 0x0156 - WatchDog Timer Switch  
576         Enable/Disable. 0: Disable, 1: enable,  
577         Enable or disable WatchDog timer.  
578         $EN_DIS  
579     */  
580     UINT8                     WatchDog;  
581     /** Offset 0x0157 - ASF Switch  
582         Enable/Disable. 0: Disable, 1: enable,  
583         Enable or disable ASF functionality.  
584         $EN_DIS
```

```
582    */
583    UINT8                      AsfEnabled;
584
585    /** Offset 0x0158 - Manageability Mode set
586     * by Mebx
587     * Enable/Disable. 0: Disable, 1: enable,
588     * Enable or disable Manageability Mode.
589
590    $EN_DIS
591    */
592    UINT8
593    ManageabilityMode;
594
595    /** Offset 0x0159 - PET Progress
596     * Enable/Disable. 0: Disable, 1: enable,
597     * Enable/Disable PET Events Progress to receive
598     * PET Events.
599
600    $EN_DIS
601    */
602    UINT8                      FwProgress;
603
604    /** Offset 0x015A - SOL Switch
605     * Enable/Disable. 0: Disable, 1: enable,
606     * Serial Over Lan enable/disable state by Mebx
607
608    $EN_DIS
609    */
610    UINT8                      AmtSolEnabled;
611
612    /** Offset 0x015B - OS Timer
613     * 16 bits Value, Set OS watchdog timer.
614
615    $EN_DIS
616    */
617    UINT16
618    WatchDogTimerOs;
619
620    /** Offset 0x015D - BIOS Timer
621     * 16 bits Value, Set BIOS watchdog timer.
622
623    $EN_DIS
```

```
613 */  
614     UINT16  
615     WatchDogTimerBios;  
616 /** Offset 0x015F - Remote Assistance  
   Trigger Availability  
617   Enable/Disable. 0: Disable, 1: enable,  
   Remote Assistance enable/disable state by Mebx  
618   $EN_DIS  
619 */  
620     UINT8  
621     RemoteAssistance;  
622 /** Offset 0x0160 - KVM Switch  
623   Enable/Disable. 0: Disable, 1: enable, KVM  
   enable/disable state by Mebx  
624   $EN_DIS  
625 */  
626     UINT8           AmtKvmEnabled;  
627  
628 /** Offset 0x0161 - MEBX execution  
629   Enable/Disable. 0: Disable, 1: enable,  
   Force MEBX execution  
630   $EN_DIS  
631 */  
632     UINT8  
633     ForcMebxSyncUp;  
634 /** Offset 0x0162  
635 */  
636     UINT8  
637     UnusedUpdSpace5[1];  
638 /** Offset 0x0163 - PCH PCIe root port  
   connection type  
639   0: built-in device, 1:slot  
640 */
```

```
641     UINT8
642     PcieRpSlotImplemented[24];
643     /** Offset 0x017B - Usage type for ClkSrc
644      0-23: PCH rootport, 0x40-0x43: PEG port,
645      0x70:LAN, 0x80: unspecified but in use
646      (free running), 0xFF: not used
647     */
648     UINT8
649     PcieClkSrcUsage[16];
650     /** Offset 0x018B - ClkReq-to-ClkSrc mapping
651      Number of ClkReq signal assigned to ClkSrc
652     */
653     UINT8
654     PcieClkSrcClkReq[16];
655     /** Offset 0x019B - PCIE RP Access Control
656      Services Extended Capability
657      Enable/Disable PCIE RP Access Control
658      Services Extended Capability
659     */
660     UINT8
661     PcieRpAcsEnabled[24];
662     /** Offset 0x01B3 - PCIE RP Clock Power
663      Management
664      Enable/Disable PCIE RP Clock Power
665      Management, even if disabled, CLKREQ# signal
666      can still be controlled by L1 PM substates
667      mechanism
668     */
669     UINT8
670     PcieRpEnableCpm[24];
671     /** Offset 0x01CB - PCIE RP Detect Timeout
672      Ms
```

```
666     The number of milliseconds within 0~65535  
667     in reference code will wait for link to  
668     exit Detect state for enabled ports before  
669     assuming there is no device and potentially  
670     disabling the port.  
671     */  
672     UINT16  
673     PcieRpDetectTimeoutMs[24];  
674     /** Offset 0x01FB - ModPHY SUS Power Domain  
675     Dynamic Gating  
676     Enable/Disable ModPHY SUS Power Domain  
677     Dynamic Gating. Setting not supported on  
678     PCH-H. 0: disable, 1: enable  
679     $EN_DIS  
680     */  
681     UINT8  
682     PmcModPhySusPgEnable;  
683     /** Offset 0x01FC - SlpS0WithGbeSupport  
684     Enable/Disable SLP_S0 with GBE Support. 0:  
685     disable, 1: enable  
686     $EN_DIS  
687     */  
688     UINT8  
689     SlpS0WithGbeSupport;  
690     /** Offset 0x01FD  
691     */  
692     UnusedUpdSpace6[3];  
693     /** Offset 0x0200 - Enable/Disable SA CRID  
694     Enable: SA CRID, Disable (Default): SA  
695     CRID  
696     $EN_DIS  
697     */
```

```
693     UINT8                         CridEnable;
694
695     /** Offset 0x0201 - DMI ASPM
696      0=Disable, 1:L0s, 2:L1, 3(Default)=L0sL1
697      0:Disable, 1:L0s, 2:L1, 3:L0sL1
698      **/
699     UINT8                         DmiAspm;
700
701     /** Offset 0x0202 - PCIe DeEmphasis control
702      per root port
703      0: -6dB, 1(Default): -3.5dB
704      0:-6dB, 1:-3.5dB
705      **/
706     UINT8
707     PegDeEmphasis[4];
708
709     /** Offset 0x0206 - PCIe Slot Power Limit
710      value per root port
711     Slot power limit value per root port
712     **/
713     UINT8
714     PegSlotPowerLimitValue[4];
715
716     /** Offset 0x020A - PCIe Slot Power Limit
717      scale per root port
718     Slot power limit scale per root port
719     0:1.0x, 1:0.1x, 2:0.01x, 3:0x001x
720     **/
721     UINT8
722     PegSlotPowerLimitScale[4];
723
724     /** Offset 0x020E - PCIe Physical Slot
725      Number per root port
726     Physical Slot Number per root port
727     **/
728     UINT16
729     PegPhysicalSlotNumber[4];
```

```
722
723 /** Offset 0x0216 - Enable/Disable
    PavpEnable
724     Enable(Default): Enable PavpEnable,
    Disable: Disable PavpEnable
725     $EN_DIS
726 */
727     UINT8                     PavpEnable;
728
729 /** Offset 0x0217 - CdClock Frequency
    selection
730     0=337.5 Mhz, 1=450 Mhz, 2=540 Mhz,
    3(Default)=675 Mhz
731     0: 337.5 Mhz, 1: 450 Mhz, 2: 540 Mhz, 3:
    675 Mhz
732 */
733     UINT8                     CdClock;
734
735 /** Offset 0x0218 - Enable/Disable
    PeiGraphicsPeimInit
736     Enable: Enable PeiGraphicsPeimInit,
    Disable(Default): Disable PeiGraphicsPeimInit
737     $EN_DIS
738 */
739     UINT8
    PeiGraphicsPeimInit;
740
741 /** Offset 0x0219
742 */
743     UINT8
    UnusedUpdSpace7;
744
745 /** Offset 0x021A - Enable or disable GNA
    device
746     0=Disable, 1(Default)=Enable
747     $EN_DIS
748 */
```

```
749     UINT8           GnaEnable;
750
751 /** Offset 0x021B - State of X2APIC_OPT_OUT
752   bit in the DMAR table
753   0=Disable/Clear, 1=Enable/Set
754   $EN_DIS
755 */
756
757 /** Offset 0x021C - Base addresses for VT-d
758   function MMIO access
759   Base addresses for VT-d MMIO access per
760   VT-d engine
761 */
762
763 /** Offset 0x0228 - Enable or disable eDP
764   device
765   0=Disable, 1(Default)=Enable
766   $EN_DIS
767 */
768
769 /** Offset 0x0229 - Enable or disable HPD of
770   DDI port B
771   0=Disable, 1(Default)=Enable
772   $EN_DIS
773 */
774
775 /** Offset 0x022A - Enable or disable HPD of
776   DDI port C
777   0=Disable, 1(Default)=Enable
778   $EN_DIS
779 */
780
```

```
779
780 /** Offset 0x022B - Enable or disable HPD of
    DDI port D
781     0=Disable, 1(Default)=Enable
782     $EN_DIS
783 */
784     UINT8                      DdiPortDHpd;
785
786 /** Offset 0x022C - Enable or disable HPD of
    DDI port F
787     0=Disable, 1(Default)=Enable
788     $EN_DIS
789 */
790     UINT8                      DdiPortFHpd;
791
792 /** Offset 0x022D - Enable or disable DDC of
    DDI port B
793     0=Disable, 1(Default)=Enable
794     $EN_DIS
795 */
796     UINT8                      DdiPortBDdc;
797
798 /** Offset 0x022E - Enable or disable DDC of
    DDI port C
799     0=Disable, 1(Default)=Enable
800     $EN_DIS
801 */
802     UINT8                      DdiPortCDdc;
803
804 /** Offset 0x022F - Enable or disable DDC of
    DDI port D
805     0=Disable, 1(Default)=Enable
806     $EN_DIS
807 */
808     UINT8                      DdiPortDDdc;
809
810 /** Offset 0x0230 - Enable or disable DDC of
```

```

        DDI port F
811    0(Default)=Disable, 1=Enable
812    $EN_DIS
813    */
814    UINT8                                DdiPortFDdc;
815
816    /** Offset 0x0231 - Enable/Disable
     SkipS3CdClockInit
817    Enable: Skip Full CD clock initialzaton,
     Disable(Default): Initialize the full
818    CD clock in S3 resume due to GOP absent
819    $EN_DIS
820    */
821    UINT8
     SkipS3CdClockInit;
822
823    /** Offset 0x0232 - Delta T12 Power Cycle
     Delay required in ms
824    Select the value for delay required.
     0(Default)= No delay, 0xFFFF = Auto calculate
825    T12 Delay to max 500ms
826    0 : No Delay, 0xFFFF : Auto Calulate T12
     Delay
827    */
828    UINT16
     DeltaT12PowerCycleDelay;
829
830    /** Offset 0x0234 - Blt Buffer Address
     Address of Blt buffer
832    */
833    UINT32
     BltBufferAddress;
834
835    /** Offset 0x0238 - Blt Buffer Size
     Size of Blt Buffer, is equal to PixelWidth
     * PixelHeight * 4 bytes (the size of
837    EFI_GRAPHICS_OUTPUT_BLT_PIXEL)

```

```
838    */
839    UINT32                                BltBufferSize;
840
841    /** Offset 0x023C - SaPostMemProductionRsvd
842        Reserved for SA Post-Mem Production
843        $EN_DIS
844    */
845    UINT8
846    SaPostMemProductionRsvd[35];
847
848    /** Offset 0x025F - PCIE RP Disable Gen2PLL
849        Shutdown and L1 Clock Gating Enable
850        PCIE RP Disable Gen2PLL Shutdown and L1
851        Clock Gating Enable Workaround needed for
852        Alpine ridge
853    */
854    UINT8
855    PcieRootPortGen2P11L1CgDisable[24];
856
857    /** Offset 0x0277 - Advanced Encryption
858        Standard (AES) feature
859        Enable or Disable Advanced Encryption
860        Standard (AES) feature; <b>0</b>: Disable; <b>1</b>:
861        Enable
862        $EN_DIS
863    */
864    UINT8                                AesEnable;
865
866    /** Offset 0x0278 - Power State 3
867        enable/disable
868        PCODE MMIO Mailbox: Power State 3
869        enable/disable; 0: Disable; <b>1</b>: Enable</b>.
870        For all VR Indexes
871    */
872    UINT8                                Psi3Enable[5];
873
874    /** Offset 0x027D - Power State 4
```

```
    enable/disable
866|  PCODE MMIO Mailbox: Power State 4
    enable/disable; 0: Disable; <b>1:</b>
        Enable</b>.For
867|    all VR Indexes
868|    */
869|    UINT8                                Psi4Enable[5];
870|
871| /** Offset 0x0282 - Imon slope correction
872|  PCODE MMIO Mailbox: Imon slope correction.
    Specified in 1/100 increment values.
873|  Range is 0-200. 125 = 1.25. <b>0:</b>
        Auto</b>.For all VR Indexes
874|    */
875|    UINT8                                ImonSlope[5];
876|
877| /** Offset 0x0287 - Imon offset correction
878|  PCODE MMIO Mailbox: Imon offset
    correction. Value is a 2's complement signed
    integer.
879|  Units 1/1000, Range 0-63999. For an offset
    = 12.580, use 12580. <b>0: Auto</b>
880|    */
881|    UINT8                                ImonOffset[5];
882|
883| /** Offset 0x028C - Enable/Disable BIOS
    configuration of VR
884|  Enable/Disable BIOS configuration of VR;
    <b>0: Disable</b>; 1: Enable.For all VR
    Indexes
885|    */
886|    UINT8                                VrConfigEnable[5];
887|
888| /** Offset 0x0291 - Thermal Design Current
    enable/disable
889|  PCODE MMIO Mailbox: Thermal Design Current
```

```
    enable/disable; <b>0: Disable</b>; 1:  
890        Enable.For all VR Indexes  
891    **/  
892        UINT8                                TdcEnable[5];  
893  
894    /** Offset 0x0296 - HECI3 state  
895    PCODE MMIO Mailbox: Thermal Design Current  
     time window. Defined in milli seconds.  
896    Valid Values 1 - 1ms , 2 - 2ms , 3 - 3ms ,  
     4 - 4ms , 5 - 5ms , 6 - 6ms , 7 - 7ms  
897    , 8 - 8ms , 10 - 10ms. For all VR Indexe  
898    **/  
899        UINT8  
     TdcTimeWindow[5];  
900  
901    /** Offset 0x029B - Thermal Design Current  
     Lock  
902    PCODE MMIO Mailbox: Thermal Design Current  
     Lock; <b>0: Disable</b>; 1: Enable. For  
903    all VR Indexes  
904    **/  
905        UINT8                                TdcLock[5];  
906  
907    /** Offset 0x02A0 - Platform Psys slope  
     correction  
908    PCODE MMIO Mailbox: Platform Psys slope  
     correction. <b>0 - Auto</b> Specified in  
909    1/100 increment values. Range is 0-200.  
     125 = 1.25  
910    **/  
911        UINT8                                PsysSlope;  
912  
913    /** Offset 0x02A1 - Platform Psys offset  
     correction  
914    PCODE MMIO Mailbox: Platform Psys offset  
     correction. <b>0 - Auto</b> Units 1/4,  
915    Range 0-255. Value of 100 = 100/4 = 25
```

```
    offset
916 */  
917     UINT8          PsysOffset;  
918  
919 /** Offset 0x02A2 - Acoustic Noise  
Mitigation feature  
920|   Enable or Disable Acoustic Noise  
Mitigation feature. This has to be enabled to  
program  
921|   slew rate configuration for all VR  
domains, Pre Wake, Ramp Up and, Ramp Down  
times.<b>0:</b>  
922|     Disabled</b>; 1: Enabled  
923|     $EN_DIS  
924 */  
925|     UINT8  
AcousticNoiseMitigation;  
926  
927 /** Offset 0x02A3 - Disable Fast Slew Rate  
for Deep Package C States for VR IA domain  
928|   Disable Fast Slew Rate for Deep Package C  
States based on Acoustic Noise Mitigation  
929|   feature enabled. <b>0: False</b>; 1: True  
930|     $EN_DIS  
931 */  
932|     UINT8  
FastPkgCRampDisableIa;  
933  
934 /** Offset 0x02A4 - Slew Rate configuration  
for Deep Package C States for VR IA domain  
935|   Slew Rate configuration for Deep Package C  
States for VR IA domain based on Acoustic  
936|   Noise Mitigation feature enabled. <b>0:  
Fast/2</b>; 1: Fast/4; 2: Fast/8; 3: Fast/16  
937|   0: Fast/2, 1: Fast/4, 2: Fast/8, 3:  
Fast/16  
938 */
```

```
939 |     UINT8
940 |     SlowSlewRateForIa;
941 | /**
942 |  ** Offset 0x02A5 - Slew Rate configuration
943 |  for Deep Package C States for VR GT domain
944 |  Slew Rate configuration for Deep Package C
945 |  States for VR GT domain based on Acoustic
946 |  Noise Mitigation feature enabled. <b>0:
947 |  Fast/2</b>; 1: Fast/4; 2: Fast/8; 3: Fast/16
948 | 0: Fast/2, 1: Fast/4, 2: Fast/8, 3:
949 |  Fast/16
950 | */
951 |     UINT8
952 |     SlowSlewRateForGt;
953 | /**
954 |  ** Offset 0x02A6 - Slew Rate configuration
955 |  for Deep Package C States for VR SA domain
956 |  Slew Rate configuration for Deep Package C
957 |  States for VR SA domain based on Acoustic
958 |  Noise Mitigation feature enabled. <b>0:
959 |  Fast/2</b>; 1: Fast/4; 2: Fast/8; 3: Fast/16
960 | 0: Fast/2, 1: Fast/4, 2: Fast/8, 3:
961 |  Fast/16
962 | */
963 |     UINT8
964 |     SlowSlewRateForSa;
965 | /**
966 |  ** Offset 0x02A7 - Thermal Design Current
967 |  current limit
968 |  PCODE MMIO Mailbox: Thermal Design Current
969 |  current limit. Specified in 1/8A units.
970 |  Range is 0-4095. 1000 = 125A. <b>0:
971 |  Auto</b>. For all VR Indexes
972 | */
973 |     UINT16
974 |     TdcPowerLimit[5];
975 |
```



```
987 /** Offset 0x02E3 - Power State 3 Threshold
   current
988   PCODE MMIO Mailbox: Power State 3 current
   cuttof in 1/4 Amp increments. Range is 0-128A.
989 */
990   UINT16
   Psi3Threshold[5];
991
992 /** Offset 0x02ED - Icc Max limit
993   PCODE MMIO Mailbox: VR Icc Max limit. 0-
   255A in 1/4 A units. 400 = 100A
994 */
995   UINT16
   IccMax[5];
996
997 /** Offset 0x02F7 - VR Voltage Limit
998   PCODE MMIO Mailbox: VR Voltage Limit.
   Range is 0-7999mV.
999 */
1000  UINT16
   VrVoltageLimit[5];
1001
1002 /** Offset 0x0301 - Disable Fast Slew Rate
   for Deep Package C States for VR GT domain
1003   Disable Fast Slew Rate for Deep Package C
   States based on Acoustic Noise Mitigation
1004   feature enabled. <b>0: False</b>; 1: True
1005   $EN_DIS
1006 */
1007  UINT8
   FastPkgCRampDisableGt;
1008
1009 /** Offset 0x0302 - Disable Fast Slew Rate
   for Deep Package C States for VR SA domain
1010   Disable Fast Slew Rate for Deep Package C
   States based on Acoustic Noise Mitigation
1011   feature enabled. <b>0: False</b>; 1: True
1012   $EN_DIS
```

```
1013 */  
1014     UINT8  
1015     FastPkgCRampDisableSa;  
1016 /** Offset 0x0303 - Enable VR specific  
1017     mailbox command  
1018     VR specific mailbox commands. <b>00b - no  
1019     VR specific command sent.</b> 01b - A  
1020     VR mailbox command specifically for the  
1021     MPS IMPV8 VR will be sent. 10b - VR specific  
1022     command sent for PS4 exit issue. 11b -  
1023     Reserved.  
1024     $EN_DIS  
1025 */  
1026     UINT8                         SendVrMbxCmd;  
1027  
1028 /** Offset 0x0304 - Reserved  
1029     Reserved  
1030 */  
1031     UINT8                         Reserved2;  
1032  
1033 /** Offset 0x0305 - Enable or Disable TXT  
1034     Enable or Disable TXT; 0: Disable; <b>1:  
1035     Enable</b>.  
1036     $EN_DIS  
1037 */  
1038     UINT8                         TxtEnable;  
1039  
1040 /** Offset 0x0306  
1041     UnusedUpdSpace9[6];  
1042  
1043 /** Offset 0x030C - Deprecated DO NOT USE  
1044     Skip Multi-Processor Initialization  
1045     @deprecated SkipMpInit has been moved to  
1046     FspmUpd
```

```
1041     $EN_DIS
1042     */
1043     UINT8                               SkipMpInit;
1044
1045 /** Offset 0x030D - McIVR RFI Frequency
   Prefix
1046   PCODE MMIO Mailbox: McIVR RFI Frequency
   Adjustment Prefix. <b>0: Plus (+)</b>; 1:
1047   Minus (-).
1048 */
1049     UINT8
   McivrRfiFrequencyPrefix;
1050
1051 /** Offset 0x030E - McIVR RFI Frequency
   Adjustment
1052   PCODE MMIO Mailbox: Adjust the RFI
   frequency relative to the nominal frequency in
1053   increments of 100KHz. For subtraction,
   change McivrRfiFrequencyPrefix. <b>0:
   Auto</b>.
1054 */
1055     UINT8
   McivrRfiFrequencyAdjust;
1056
1057 /** Offset 0x030F - FIVR RFI Frequency
1058   PCODE MMIO Mailbox: Set the desired RFI
   frequency, in increments of 100KHz. <b>0:
1059   Auto</b>. Range varies based on XTAL
   clock: 0-1918 (Up to 191.8MHz) for 24MHz
   clock;
1060   0-1535 (Up to 153.5MHz) for 19MHz clock.
1061 */
1062     UINT16
   FivrRfiFrequency;
1063
1064 /** Offset 0x0311 - McIVR RFI Spread
   Spectrum
```

```
1065    PCODE_MMIO_Mailbox: McIVR RFI Spread
      Spectrum. <b>0: 0%</b>; 1: +/- 0.5%; 2: +/- 1%;
1066    3: +/- 1.5%; 4: +/- 2%; 5: +/- 3%; 6: +/- 4%; 7: +/- 5%; 8: +/- 6%.
1067 */
1068     UINT8
      McivrSpreadSpectrum;
1069
1070 /** Offset 0x0312 - FIVR RFI Spread Spectrum
1071   PCODE_MMIO_Mailbox: FIVR RFI Spread
      Spectrum, in 0.1% increments. <b>0: 0%</b>;
1072   Range: 0.0% to 10.0% (0-100).
1073 */
1074     UINT8
      FivrSpreadSpectrum;
1075
1076 /** Offset 0x0313 - Disable Fast Slew Rate
      for Deep Package C States for VR FIVR domain
1077   Disable Fast Slew Rate for Deep Package C
      States based on Acoustic Noise Mitigation
1078   feature enabled. <b>0: False</b>; 1: True
1079   $EN_DIS
1080 */
1081     UINT8
      FastPkgCRampDisableFivr;
1082
1083 /** Offset 0x0314 - Slew Rate configuration
      for Deep Package C States for VR FIVR domain
1084   Slew Rate configuration for Deep Package C
      States for VR FIVR domain based on Acoustic
1085   Noise Mitigation feature enabled. <b>0:
      Fast/2</b>; 1: Fast/4; 2: Fast/8; 3: Fast/16
1086   0: Fast/2, 1: Fast/4, 2: Fast/8, 3:
      Fast/16
1087 */
1088     UINT8
      SlowSlewRateForFivr;
```

```
1089
1090 /** Offset 0x0315 - CpuBistData
1091     Pointer CPU BIST Data
1092 */
1093     UINT32                               CpuBistData;
1094
1095 /** Offset 0x0319 - Activates VR mailbox
1096     command for Intersil VR C-state issues.
1097     Intersil VR mailbox command. <b>0 - no
1098     mailbox command sent.</b> 1 - VR mailbox
1099     command sent for IA/GT rails only. 2 - VR
1100     mailbox command sent for IA/GT/SA rails.
1101 */
1102     UINT8                               IslVrCmd;
1103
1104 /**
1105     UINT16                               ImonSlope1[5];
1106
1107 /** Offset 0x0324 - CPU VR Power Delivery
1108     Design
1109     Used to communicate the power delivery
1110     design capability of the board. This value
1111     is an enum of the available power delivery
1112     segments that are defined in the Platform
1113     Design Guide.
1114 */
1115     UINT32                               VrPowerDeliveryDesign;
1116
1117 /** Offset 0x0328 - Pre Wake Randomization
1118     time
1119     PCODE MMIO Mailbox: Acoustic Mitigation
```

```
    Range.Defines the maximum pre-wake
    randomization
1116|    time in micro ticks.This can be programmed
    only if AcousticNoiseMitigation is enabled.
1117|    Range 0-255 <b>0</b>.
1118|    */
1119|    UINT8                               Prewake;
1120|
1121| /** Offset 0x0329 - Ramp Up Randomization
   time
1122|     PCODE MMIO Mailbox: Acoustic Mitigation
   Range.Defines the maximum Ramp Up
   randomization
1123|     time in micro ticks.This can be programmed
   only if AcousticNoiseMitigation is
   enabled.Range
1124|     0-255 <b>0</b>.
1125|     */
1126|     UINT8                               RampUp;
1127|
1128| /** Offset 0x032A - Ramp Down Randomization
   time
1129|     PCODE MMIO Mailbox: Acoustic Mitigation
   Range.Defines the maximum Ramp Down
   randomization
1130|     time in micro ticks.This can be programmed
   only if AcousticNoiseMitigation is
   enabled.Range
1131|     0-255 <b>0</b>.
1132|     */
1133|     UINT8                               RampDown;
1134|
1135| /** Offset 0x032B - CpuMpPpi
   Pointer for CpuMpPpi
1136|     */
1137|     UINT32                               CpuMpPpi;
1138|
1139|
```

```
1140 /** Offset 0x032F - CpuMpHob
1141   Pointer for CpuMpHob. This is optional
1142   data buffer for CpuMpPpi usage.
1143 */
1144   UINT32                               CpuMpHob;
1145
1146 /** Offset 0x0333 - Enable or Disable
1147   processor debug features
1148   Enable or Disable processor debug
1149   features; <b>0: Disable</b>; 1: Enable.
1150   $EN_DIS
1151 */
1152   UINT8
1153   DebugInterfaceEnable;
1154
1155 /** Offset 0x0334 -
1156   ReservedCpuPostMemProduction
1157   Reserved for CPU Post-Mem Production
1158   $EN_DIS
1159 */
1160   UINT8
1161   ReservedCpuPostMemProduction[18];
1162
1163 /** Offset 0x0346 - Enable DMI ASPM
1164   Deprecated.
1165   $EN_DIS
1166 */
1167   UINT8                               PchDmiAspm;
1168
1169 /** Offset 0x0347 - Enable Power Optimizer
1170   Enable DMI Power Optimizer on PCH side.
1171   $EN_DIS
1172 */
1173   UINT8
1174   PchPwrOptEnable;
1175
1176 /** Offset 0x0348 - PCH Flash Protection
```

```
    Ranges Write Enble
1170    Write or erase is blocked by hardware.
1171    */
1172    UINT8
1173        PchWriteProtectionEnable[5];
1174    /**
1174     ** Offset 0x034D - PCH Flash Protection
1174     Ranges Read Enble
1175     Read is blocked by hardware.
1176     */
1177    UINT8
1178        PchReadProtectionEnable[5];
1179    /**
1179     ** Offset 0x0352 - PCH Protect Range Limit
1180     Left shifted address by 12 bits with
1180     address bits 11:0 are assumed to be FFFh for
1181     limit comparison.
1182     */
1183    UINT16
1183        PchProtectedRangeLimit[5];
1184
1185    /**
1185     ** Offset 0x035C - PCH Protect Range Base
1186     Left shifted address by 12 bits with
1186     address bits 11:0 are assumed to be 0.
1187     */
1188    UINT16
1188        PchProtectedRangeBase[5];
1189
1190    /**
1190     ** Offset 0x0366 - Enable Pme
1191     Enable Azalia wake-on-ring.
1192     $EN_DIS
1193     */
1194    UINT8                                PchHdaPme;
1195
1196    /**
1196     ** Offset 0x0367
1197     */
1198    UINT8
```

```
    UnusedUpdSpace10;

1199  /** Offset 0x0368 - VC Type
1200   Virtual Channel Type Select: 0: VC0, 1:
1201     VC1.
1202     0: VC0, 1: VC1
1203   */
1204   UINT8                               PchHdaVcType;
1205
1206   /** Offset 0x0369 - HD Audio Link Frequency
1207     HDA Link Freq (PCH_HDAUDIO_LINK_FREQUENCY
1208     enum): 0: 6MHz, 1: 12MHz, 2: 24MHz.
1209     0: 6MHz, 1: 12MHz, 2: 24MHz
1210   */
1211   UINT8
1212   PchHdaLinkFrequency;
1213
1214   /** Offset 0x036A - iDisp-Link Frequency
1215     iDisp-Link Freq
1216     (PCH_HDAUDIO_LINK_FREQUENCY enum): 4: 96MHz,
1217     3: 48MHz.
1218     4: 96MHz, 3: 48MHz
1219   */
1220   UINT8
1221   PchHdaIDispLinkFrequency;
1222
1223
1224   /** Offset 0x036B - iDisp-Link T-mode
1225     iDisp-Link T-Mode (PCH_HDAUDIO_IDISP_TMODE
1226     enum): 0: 2T, 1: 1T.
1227     0: 2T, 1: 1T
1228   */
1229   UINT8
1230   PchHdaIDispLinkTmode;
1231
1232
1233   /** Offset 0x036C - Universal Audio
1234     Architecture compliance for DSP enabled system
1235     0: Not-UAA Compliant (Intel SST driver
```

```
        supported only), 1: UAA Compliant (HDA Inbox
1226    driver or SST driver supported).
1227    $EN_DIS
1228    */
1229    UINT8
1230    PchHdaDspUaaCompliance;
1231    /** Offset 0x036D - iDisplay Audio Codec
1232        disconnection
1233        0: Not disconnected, enumerable, 1:
1234        Disconnected SDI, not enumerable.
1235        $EN_DIS
1236        */
1237    UINT8
1238    PchHdaIDispCodecDisconnect;
1239    /** Offset 0x036E - USB LFPS Filter
1240        selection
1241        For each byte bits 2:0 are for p, bits 4:6
1242        are for n. 0h:1.6ns, 1h:2.4ns, 2h:3.2ns,
1243        3h:4.0ns, 4h:4.8ns, 5h:5.6ns, 6h:6.4ns.
1244        */
1245    UINT8
1246    PchUsbHsioFilterSel[10];
1247    /** Offset 0x0378
1248        */
1249    UINT8
1250    UnusedUpdSpace11[5];
1251    /** Offset 0x037D - Enable PCH Io Apic Entry
1252        24-119
1253        0: Disable; 1: Enable.
1254        $EN_DIS
1255        */
1256    UINT8
1257    PchIoApicEntry24_119;
```

```
1252 |
1253 | /** Offset 0x037E - PCH Io Apic ID
1254 |   This member determines IOAPIC ID. Default
1255 |   is 0x02.
1256 | */
1257 |     UINT8                               PchIoApicId;
1258 | /**
1259 | */
1260 |     UINT8
1261 |     UnusedUpdSpace12;
1262 | /**
1263 |   Offset 0x0380 - Enable PCH ISH SPI GPIO
1264 |   pins assigned
1265 |   0: Disable; 1: Enable.
1266 |   $EN_DIS
1267 | */
1268 |     UINT8
1269 |     PchIshSpiGpioAssign;
1270 | /**
1271 |   Offset 0x0381 - Enable PCH ISH UART0
1272 |   GPIO pins assigned
1273 |   0: Disable; 1: Enable.
1274 |   $EN_DIS
1275 | */
1276 |     UINT8
1277 |     PchIshUart0GpioAssign;
1278 | /**
1279 |   Offset 0x0382 - Enable PCH ISH UART1
1280 |   GPIO pins assigned
1281 |   0: Disable; 1: Enable.
1282 |   $EN_DIS
1283 | */
1284 |     UINT8
1285 |     PchIshUart1GpioAssign;
1286 | /**
1287 |   Offset 0x0383 - Enable PCH ISH I2C0 GPIO
1288 |   0: Disable; 1: Enable.
1289 |   $EN_DIS
1290 | */
1291 |     UINT8
1292 |     PchIshI2c0GpioAssign;
```

```
    pins assigned
1281    0: Disable; 1: Enable.
1282    $EN_DIS
1283 /**
1284     UINT8
1285     PchIshI2c0GpioAssign;
1286 /**
1287  ** Offset 0x0384 - Enable PCH ISH I2C1 GPIO
1288  pins assigned
1289  0: Disable; 1: Enable.
1290  $EN_DIS
1291 /**
1292  ** Offset 0x0385 - Enable PCH ISH I2C2 GPIO
1293  pins assigned
1294  0: Disable; 1: Enable.
1295  $EN_DIS
1296 /**
1297  ** Offset 0x0386 - Enable PCH ISH GP_0 GPIO
1298  pin assigned
1299  0: Disable; 1: Enable.
1300  $EN_DIS
1301 /**
1302  UINT8
1303  PchIshGp0GpioAssign;
1304 /**
1305  ** Offset 0x0387 - Enable PCH ISH GP_1 GPIO
1306  pin assigned
1307  0: Disable; 1: Enable.
1308  $EN_DIS
1309 /**
1310  UINT8
```

```
    PchIshGp1GpioAssign;
1309
1310 /** Offset 0x0388 - Enable PCH ISH GP_2 GPIO
1311   pin assigned
1312   0: Disable; 1: Enable.
1313   $EN_DIS
1314 */
1315
1316 /** Offset 0x0389 - Enable PCH ISH GP_3 GPIO
1317   pin assigned
1318   0: Disable; 1: Enable.
1319   $EN_DIS
1320 */
1321
1322 /** Offset 0x038A - Enable PCH ISH GP_4 GPIO
1323   pin assigned
1324   0: Disable; 1: Enable.
1325   $EN_DIS
1326 */
1327
1328 /** Offset 0x038B - Enable PCH ISH GP_5 GPIO
1329   pin assigned
1330   0: Disable; 1: Enable.
1331   $EN_DIS
1332 */
1333
1334 /** Offset 0x038C - Enable PCH ISH GP_6 GPIO
1335   pin assigned
1336   0: Disable; 1: Enable.
```

```
1336     $EN_DIS
1337     */
1338     UINT8
1339         PchIshGp6GpioAssign;
1340     /** Offset 0x038D - Enable PCH ISH GP_7 GPIO
1341      pin assigned
1342      0: Disable; 1: Enable.
1343      $EN_DIS
1344      */
1345     UINT8
1346         PchIshGp7GpioAssign;
1347     /** Offset 0x038E - PCH ISH PDT Unlock Msg
1348      0: False; 1: True.
1349      $EN_DIS
1350      */
1351     UINT8
1352         PchIshPdtUnlock;
1353     /** Offset 0x038F - Enable PCH Lan LTR
1354      capability of PCH internal LAN
1355      0: Disable; 1: Enable.
1356      $EN_DIS
1357      */
1358     UINT8
1359         PchLanLtrEnable;
1360     /** Offset 0x0390
1361      */
1362     UINT8
1363         UnusedUpdSpace13[3];
1364     /** Offset 0x0393 - Enable LOCKDOWN BIOS
1365      LOCK
1366      Enable the BIOS Lock feature and set EISS
1367      bit (D31:F5:RegDCh[5]) for the BIOS region
```

```
1364     protection.  
1365     $EN_DIS  
1366     **/  
1367     UINT8  
1368         PchLockDownBiosLock;  
1369     /** Offset 0x0394 - PCH Compatibility  
1370      Revision ID  
1371      This member describes whether or not the  
1372      CRID feature of PCH should be enabled.  
1373      $EN_DIS  
1374      **/  
1375      UINT8                                     PchCrid;  
1376  
1377     /** Offset 0x0395 - RTC CMOS MEMORY LOCK  
1378      Enable RTC lower and upper 128 byte Lock  
1379      bits to lock Bytes 38h-3Fh in the upper  
1380      and and lower 128-byte bank of RTC RAM.  
1381      $EN_DIS  
1382      **/  
1383      UINT8                                     PchLockDownRtcMemoryLock;  
1384  
1385      /** Offset 0x0396 - Enable PCIE RP HotPlug  
1386      Indicate whether the root port is hot plug  
1387      available.  
1388      **/  
1389      UINT8  
1390          PcieRpHotPlug[24];  
1391  
1392      /** Offset 0x03AE - Enable PCIE RP Pm Sci  
1393      Indicate whether the root port power  
1394      manager SCI is enabled.  
1395      **/  
1396      UINT8  
1397          PcieRpPmSci[24];  
1398
```

```
1392 /** Offset 0x03C6 - Enable PCIE RP Ext Sync
1393   Indicate whether the extended synch is
1394   enabled.
1394 */
1395     UINT8
1396       PcieRpExtSync[24];
1396
1397 /** Offset 0x03DE - Enable PCIE RP
1398   Transmitter Half Swing
1398   Indicate whether the Transmitter Half
1398   Swing is enabled.
1399 */
1400     UINT8
1400       PcieRpTransmitterHalfSwing[24];
1401
1402 /** Offset 0x03F6 - Enable PCIE RP Clk Req
1403   Detect
1403   Probe CLKREQ# signal before enabling
1403   CLKREQ# based power management.
1404 */
1405     UINT8
1405       PcieRpClkReqDetect[24];
1406
1407 /** Offset 0x040E - PCIE RP Advanced Error
1408   Report
1408   Indicate whether the Advanced Error
1408   Reporting is enabled.
1409 */
1410     UINT8
1410       PcieRpAdvancedErrorReporting[24];
1411
1412 /** Offset 0x0426 - PCIE RP Unsupported
1413   Request Report
1413   Indicate whether the Unsupported Request
1413   Report is enabled.
1414 */
1415     UINT8
```

```
    PcieRpUnsupportedRequestReport[24];
1416
1417 /** Offset 0x043E - PCIE RP Fatal Error
   Report
1418 | Indicate whether the Fatal Error Report is
   enabled.
1419 */
1420 |     UINT8
   PcieRpFatalErrorReport[24];
1421
1422 /** Offset 0x0456 - PCIE RP No Fatal Error
   Report
1423 | Indicate whether the No Fatal Error Report
   is enabled.
1424 */
1425 |     UINT8
   PcieRpNoFatalErrorReport[24];
1426
1427 /** Offset 0x046E - PCIE RP Correctable
   Error Report
1428 | Indicate whether the Correctable Error
   Report is enabled.
1429 */
1430 |     UINT8
   PcieRpCorrectableErrorReport[24];
1431
1432 /** Offset 0x0486 - PCIE RP System Error On
   Fatal Error
1433 | Indicate whether the System Error on Fatal
   Error is enabled.
1434 */
1435 |     UINT8
   PcieRpSystemErrorOnFatalError[24];
1436
1437 /** Offset 0x049E - PCIE RP System Error On
   Non Fatal Error
1438 | Indicate whether the System Error on Non
```

```
    Fatal Error is enabled.

1439 */
1440     UINT8
1441     PcieRpSystemErrorOnNonFatalError[24];
1442 /**
1443  ** Offset 0x04B6 - PCIE RP System Error On
1444  Correctable Error
1445  Indicate whether the System Error on
1446  Correctable Error is enabled.
1447 */
1448     UINT8
1449     PcieRpSystemErrorOnCorrectableError[24];
1450 /**
1451  ** Offset 0x04CE - PCIE RP Max Payload
1452  Max Payload Size supported, Default 128B,
1453  see enum PCH_PCIE_MAX_PAYLOAD.
1454 */
1455     UINT8
1456     PcieRpMaxPayload[24];
1457 /**
1458  ** Offset 0x04E6 - PCH USB3 RX HSIO Tuning
1459  parameters
1460  Bits 7:3 are for Signed Magnitude number
1461  added to the CTLE code, Bits 2:0 are for
1462  controlling the input offset
1463 */
1464     UINT8
1465     PchUsbHsioRxTuningParameters[10];
1466 /**
1467  ** Offset 0x04F0 - PCH USB3 HSIO Rx Tuning
1468  Enable
1469  Mask for enabling tuning of HSIO Rx
1470  signals of USB3 ports. Bits: 0 -
1471  HsioCtrlAdaptOffsetCfgEnable,
1472  1 - HsioFilterSelNEnable, 2 -
1473  HsioFilterSelPEnable, 3 -
1474  HsioOlfpsCfgPullUpDwnResEnable
```

```
1461  */
1462  UINT8
1463  PchUsbHsioRxTuningEnable[10];
1464  /** Offset 0x04FA
1465  */
1466  UINT8
1467  UnusedUpdSpace14[4];
1468  /** Offset 0x04FE - PCIE RP Pcie Speed
1469  Determines each PCIE Port speed
1470  capability. 0: Auto; 1: Gen1; 2: Gen2; 3: Gen3
1471  (see:
1472  PCH_PCIE_SPEED).
1473  */
1474  UINT8
1475  PcieRpPcieSpeed[24];
1476  /** Offset 0x0516 - PCIE RP Gen3
1477  Equalization Phase Method
1478  PCIe Gen3 Eq Ph3 Method (see
1479  PCH_PCIE_EQ_METHOD). 0: DEPRECATED, hardware
1480  equalization;
1481  1: hardware equalization; 4: Fixed
1482  Coeficients.
1483  */
1484  UINT8
1485  PcieRpGen3EqPh3Method[24];
1486  /** Offset 0x052E - PCIE RP Physical Slot
1487  Number
1488  Indicates the slot number for the root
1489  port. Default is the value as root port index.
1490  */
1491  UINT8
1492  PcieRpPhysicalSlotNumber[24];
1493  */
1494
```

```
1485 /** Offset 0x0546 - PCIE RP Completion
   Timeout
1486   The root port completion timeout (see:
   PCH_PCIE_COMPLETION_TIMEOUT). Default is
   PchPcieCompletionT0_Default.
1487 */
1488   UINT8
1489   PcieRpCompletionTimeout[24];
1490
1491 /** Offset 0x055E
1492 */
1493   UINT8
1494   UnusedUpdSpace15[106];
1495
1496 /** Offset 0x05C8 - PCIE RP Aspm
   The ASPM configuration of the root port
   (see: PCH_PCIE_ASPM_CONTROL). Default is
   PchPcieAspmAutoConfig.
1497 */
1498   UINT8
1499   PcieRpAspm[24];
1500
1501 /** Offset 0x05E0 - PCIE RP L1 Substates
   The L1 Substates configuration of the root
   port (see: PCH_PCIE_L1SUBSTATES_CONTROL).
   Default is PchPcieL1SubstatesL1_1_2.
1502 */
1503   UINT8
1504   PcieRpL1Substates[24];
1505
1506 /** Offset 0x05F8 - PCIE RP Ltr Enable
   Latency Tolerance Reporting Mechanism.
1507 */
1508   UINT8
1509   PcieRpLtrEnable[24];
1510
1511 /** Offset 0x0610 - PCIE RP Ltr Config Lock
```

```
1512     0: Disable; 1: Enable.
1513 */
1514     UINT8
1515         PcieRpLtrConfigLock[24];
1516 /**
1517  ** Offset 0x0628 - PCIE Eq Ph3 Lane Param
1518  Cm
1519  PCH_PCIE_EQ_LANE_PARAM. Coefficient C-1.
1520 */
1521 /**
1522  ** Offset 0x0640 - PCIE Eq Ph3 Lane Param
1523  Cp
1524  PCH_PCIE_EQ_LANE_PARAM. Coefficient C+1.
1525 */
1526 /**
1527  ** Offset 0x0658 - PCIE Sw Eq CoeffList Cm
1528  PCH_PCIE_EQ_PARAM. Coefficient C-1.
1529 */
1530     UINT8
1531         PcieSwEqCoeffListCm[5];
1532 /**
1533  ** Offset 0x065D - PCIE Sw Eq CoeffList Cp
1534  PCH_PCIE_EQ_PARAM. Coefficient C+1.
1535 */
1536 /**
1537  ** Offset 0x0662 - PCIE Disable RootPort
1538  Clock Gating
1539  Describes whether the PCI Express Clock
     Gating for each root port is enabled by
     platform modules. 0: Disable; 1: Enable.
1540 $EN_DIS
```

```
1540  */
1541  UINT8
1542    PcieDisableRootPortClockGating;
1543  /** Offset 0x0663 - PCIE Enable Peer Memory
1544   Write
1544   This member describes whether Peer Memory
1545   Writes are enabled on the platform.
1545   $EN_DIS
1546  */
1547  UINT8
1548    PcieEnablePeerMemoryWrite;
1549  /** Offset 0x0664
1550  */
1551  UINT8
1552    UnusedUpdSpace16;
1553  /** Offset 0x0665 - PCIE Compliance Test
1554   Mode
1554   Compliance Test Mode shall be enabled when
1555   using Compliance Load Board.
1555   $EN_DIS
1556  */
1557  UINT8
1558    PcieComplianceTestMode;
1559  /** Offset 0x0666 - PCIE Rp Function Swap
1560   Allows BIOS to use root port function
1561   number swapping when root port of function
1562   0 is disabled.
1562   $EN_DIS
1563  */
1564  UINT8
1565    PcieRpFunctionSwap;
1566  /** Offset 0x0667 - Teton Glacier Support
```

```
1567     Enables support for the Teton Glacier
1568     card.
1569     $EN_DIS
1570     */
1570     UINT8
1570     TetonGlacierSupport;
1571
1572     /** Offset 0x0668 - Teton Glacier Cycle
1572      Router
1573     Specify to which cycle router Teton
1573     Glacier is connected, it is valid only when
1574     Teton Glacier support is enabled. Default
1574     is 0 for CNP-H system and 1 for CNP-LP system
1575     */
1575     UINT8
1575     TetonGlacierCR;
1577
1578     /** Offset 0x0669 - PCH Pm PME_B0_S5_DIS
1579     When cleared (default), wake events from
1579     PME_B0_STS are allowed in S5 if PME_B0_EN = 1.
1580     $EN_DIS
1581     */
1582     UINT8
1582     PchPmPmeB0S5Dis;
1583
1584     /** Offset 0x066A - SPI ChipSelect signal
1584     polarity
1585     Selects SPI ChipSelect signal polarity.
1586     */
1587     UINT8
1587     SerialIoSpiCsPolarity[3];
1588
1589     /** Offset 0x066D - PCIE IMR
1590     Enables Isolated Memory Region for PCIe.
1591     $EN_DIS
1592     */
1593     UINT8
```

```
    PcieRpImrEnabled;
1594  /** Offset 0x066E - PCIE IMR port number
1595   Selects PCIE root port number for IMR
1596   feature.
1597 */
1598  UINT8
1599  PcieRpImrSelection;
1600  /** Offset 0x066F
1601  */
1602  UINT8
1603  UnusedUpdSpace17;
1604  /** Offset 0x0670 - PCH Pm WOL Enable
1605   Override
1606   Corresponds to the WOL Enable Override bit
1607   in the General PM Configuration B
1608   (GEN_PMCON_B) register.
1609   $EN_DIS
1610 */
1611  UINT8
1612  PchPmWolEnableOverride;
1613  /** Offset 0x0671 - PCH Pm PCIe Wake From
1614   DeepSx
1615   Determine if enable PCIe to wake from deep
1616   Sx.
1617   $EN_DIS
1618 */
1619  UINT8
1620  PchPmPcieWakeFromDeepSx;
1621  /** Offset 0x0672 - PCH Pm WoW lan Enable
1622   Determine if WLAN wake from Sx,
1623   corresponds to the HOST_WLAN_PP_EN bit in the
1624   PWRM_CFG3 register.
```

```
1618     $EN_DIS
1619     */
1620     UINT8
1621     PchPmWowlanEnable;
1622     /** Offset 0x0673 - PCH Pm Wow lan DeepSx
1623      Enable
1624      Determine if WLAN wake from DeepSx,
1625      corresponds to the DSX_WLAN_PP_EN bit in the
1626      PWRM_CFG3 register.
1627     $EN_DIS
1628     */
1629     UINT8
1630     PchPmWowlanDeepSxEnable;
1631     /** Offset 0x0674 - PCH Pm Lan Wake From
1632      DeepSx
1633      Determine if enable LAN to wake from deep
1634      Sx.
1635     $EN_DIS
1636     */
1637     UINT8
1638     PchPmLanWakeFromDeepSx;
1639     /** Offset 0x0675 - PCH Pm Deep Sx Pol
1640      Deep Sx Policy.
1641      $EN_DIS
1642      */
1643     UINT8
1644     PchPmDeepSxPol;
1645     /** Offset 0x0676 - PCH Pm Slp S3 Min Assert
1646      SLP_S3 Minimum Assertion Width Policy.
1647      Default is PchSlpS350ms.
1648      */
1649     UINT8
1650     PchPmSlpS3MinAssert;
```

```
1645
1646 /** Offset 0x0677 - PCH Pm Slp S4 Min Assert
1647     SLP_S4 Minimum Assertion Width Policy.
1648     Default is PchSlpS4s.
1649 */
1650     UINT8
1651         PchPmSlpS4MinAssert;
1652
1653 /** Offset 0x0678 - PCH Pm Slp Sus Min
1654     Assert
1655     SLP_SUS Minimum Assertion Width Policy.
1656     Default is PchSlpSus4s.
1657 */
1658     UINT8
1659         PchPmSlpSusMinAssert;
1660
1661 /** Offset 0x0679 - PCH Pm Slp A Min Assert
1662     SLP_A Minimum Assertion Width Policy.
1663     Default is PchSlpA2s.
1664 */
1665     UINT8
1666         PchPmSlpAMinAssert;
1667
1668 /**
1669     ** Offset 0x067A - SLP_S0# Override
1670     Select 'Auto', it will be auto-configured
1671     according to probe type. Select 'Enabled'
1672     will disable SLP_S0# assertion whereas
1673     'Disabled' will enable SLP_S0# assertion
1674     when debug is enabled. \n
1675     Note: This BIOS option should keep 'Auto',
1676     other options are intended for advanced
1677     configuration only.
1678     0:Disabled, 1:Enabled, 2:Auto
1679 */
1680     UINT8
1681         SlpS0override;
1682
1683 /**
1684     ** Offset 0x067B - S0ix Override Settings
```

```
1672|     Select 'Auto', it will be auto-configured  
1673|     according to probe type. 'No Change' will  
1673|     keep PMC default settings. Or select the  
1673|     desired debug probe type for S0ix Override  
1674|     settings.\n1675|     Reminder: DCI OOB (aka BSSB) uses CCA  
1675|     probe.\n1676|     Note: This BIOS option should keep 'Auto',  
1676|     other options are intended for advanced  
1677|     configuration only.  
1678|     0:No Change, 1:DCI OOB, 2:USB2 DbC, 3:Auto  
1679|     **/  
1680|     UINT8  
1680|     SlpS0DisQForDebug;  
1681|  
1682|     /** Offset 0x067C - USB Overcurrent Override  
1682|     for DbC  
1683|     This option overrides USB Over Current  
1683|     enablement state that USB OC will be disabled  
1684|     after enabling this option. Enable when  
1684|     DbC is used to avoid signaling conflicts.  
1685|     $EN_DIS  
1686|     **/  
1687|     UINT8  
1687|     PchEnableDbc0bs;  
1688|  
1689|     /** Offset 0x067D  
1690|     **/  
1691|     UINT8  
1691|     UnusedUpdSpace18[3];  
1692|  
1693|     /** Offset 0x0680 - PCH Pm Lpc Clock Run  
1694|     This member describes whether or not the  
1694|     LPC ClockRun feature of PCH should be enabled.  
1695|     Default value is Disabled  
1696|     $EN_DIS  
1697|     **/
```

```
1698 |     UINT8
1699 |     PchPmLpcClockRun;
1700 | /**
1701 |  ** Offset 0x0681 - PCH Pm Slp Strch Sus Up
1701 |  Enable SLP_X Stretching After SUS Well
1701 |  Power Up.
1702 |     $EN_DIS
1703 | */
1704 |     UINT8
1704 |     PchPmSlpStrchSusUp;
1705 |
1706 | /**
1707 |  ** Offset 0x0682 - PCH Pm Slp Lan Low Dc
1707 |  Enable/Disable SLP_LAN# Low on DC Power.
1708 |     $EN_DIS
1709 | */
1710 |     UINT8
1710 |     PchPmSlpLanLowDc;
1711 |
1712 | /**
1713 |  ** Offset 0x0683 - PCH Pm Pwr Btn Override
1713 |  Period
1713 |  PCH power button override period. 000b-4s,
1713 |  001b-6s, 010b-8s, 011b-10s, 100b-12s, 101b-
1713 |  14s.
1714 | */
1715 |     UINT8
1715 |     PchPmPwrBtnOverridePeriod;
1716 |
1717 | /**
1718 |  ** Offset 0x0684 - PCH Pm Disable Dsx Ac
1718 |  Present Pulldown
1718 |  When Disable, PCH will internal pull down
1718 |  AC_PRESENT in deep SX and during G3 exit.
1719 |     $EN_DIS
1720 | */
1721 |     UINT8
1721 |     PchPmDisableDsxAcPresentPulldown;
1722 |
1723 | /**
1723 |  ** Offset 0x0685
```

```
1724  */
1725  UINT8
1726  UnusedUpdSpace19;
1727  /** Offset 0x0686 - PCH Pm Disable Native
1728  Power Button
1729  Power button native mode disable.
1730  $EN_DIS
1731  */
1732  UINT8
1733  PchPmDisableNativePowerButton;
1734  /** Offset 0x0687 - PCH Pm Slp S0 Enable
1735  Indicates whether SLP_S0# is to be
1736  asserted when PCH reaches idle state.
1737  $EN_DIS
1738  */
1739  UINT8
1740  PchPmSlpS0Enable;
1741  /** Offset 0x0688 - PCH Pm ME_WAKE_STS
1742  Clear the ME_WAKE_STS bit in the Power and
1743  Reset Status (PRSTS) register.
1744  $EN_DIS
1745  */
1746  UINT8
1747  PchPmMeWakeSts;
1748  /** Offset 0x0689 - PCH Pm WOL_OVR_WK_STS
1749  Clear the WOL_OVR_WK_STS bit in the Power
and Reset Status (PRSTS) register.
1750  $EN_DIS
1751  */
1752  UINT8
1753  PchPmWolOvrWkSts;
1754  /**
1755  Offset 0x068A - PCH Pm Reset Power Cycle
```

```
    Duration
1752|    Could be customized in the unit of second.
      Please refer to EDS for all support settings.
1753|    0 is default, 1 is 1 second, 2 is 2
      seconds, ...
1754| */
1755|     UINT8
1756|     PchPmPwrCycDur;
1757| /**
1758|     Offset 0x068B - PCH Pm Pcie Pll Ssc
1759|     Specifies the Pcie Pll Spread Spectrum
1760|     Percentage. The default is 0xFF: AUTO - No
1761|     BIOS override.
1762| */
1763|     UINT8
1764|     PchPmPciePllSsc;
1765| /**
1766|     Offset 0x068C
1767|     $EN_DIS
1768|     SATA Power Optimizer on PCH side.
1769|     */
1770| /**
1771|     UINT8
1772|     SataPwrOptEnable;
1773| /**
1774|     Offset 0x068E - PCH Sata eSATA Speed
1775|     Limit
1776|     When enabled, BIOS will configure the
1777|     PxSCTL.SPD to 2 to limit the eSATA port speed.
1778|     $EN_DIS
1779| /**
1780|     UINT8
1781|     EsataSpeedLimit;
```

```
1778
1779 /** Offset 0x068F - PCH Sata Speed Limit
1780   Indicates the maximum speed the SATA
1781   controller can support 0h:
1782   PchSataSpeedDefault.
1783 */
1784   UINT8
1785   SataSpeedLimit;
1786 */
1787   UINT8
1788   SataPortsHotPlug[8];
1789 */
1790   /** Offset 0x0690 - Enable SATA Port HotPlug
1791   Enable SATA Port HotPlug.
1792 */
1793   UINT8
1794   SataPortsInterlockSw[8];
1795 */
1796 */
1797   UINT8
1798   SataPortsExternal[8];
1799 */
1800   /** Offset 0x06A0 - Enable SATA Port External
1801   Enable SATA Port External.
1802 */
1803   UINT8
1804   SataPortsExternal[8];
1805 */
1806 */
1807   /** Offset 0x06A8 - Enable SATA Port SpinUp
1808   Enable the COMRESET initialization
1809   Sequence to the device.
1810 */
1811   UINT8
1812   SataPortsSpinUp[8];
1813 */
1814   /** Offset 0x06B0 - Enable SATA Port Solid
```

```
        State Drive
1805    0: HDD; 1: SSD.
1806    */
1807    UINT8
1808        SataPortsSolidStateDrive[8];
1809    /** Offset 0x06B8 - Enable SATA Port Enable
1810        Dito Config
1811        Enable DEVSLP Idle Timeout settings
1812        (DmVal, DitoVal).
1813    */
1814    /** Offset 0x06C0 - Enable SATA Port DmVal
1815        DITO multiplier. Default is 15.
1816    */
1817    UINT8
1818        SataPortsDmVal[8];
1819    /** Offset 0x06C8 - Enable SATA Port DmVal
1820        DEVSLP Idle Timeout (DITO), Default is
1821        625.
1822    */
1823    /** Offset 0x06D8 - Enable SATA Port ZpOdd
1824        Support zero power ODD.
1825    */
1826    UINT8
1827        SataPortsZpOdd[8];
1828
1829    /** Offset 0x06E0 - PCH Sata Rst Raid Device
1830        Id
1831        Enable RAID Alternate ID.
1832        0:Client, 1:Alternate, 2:Server
```

```
1832  */
1833  UINT8
1834  SataRstRaidDeviceId;
1835  /** Offset 0x06E1 - PCH Sata Rst Raid0
1836  RAID0.
1837  $EN_DIS
1838  */
1839  UINT8                               SataRstRaid0;
1840
1841  /** Offset 0x06E2 - PCH Sata Rst Raid1
1842  RAID1.
1843  $EN_DIS
1844  */
1845  UINT8                               SataRstRaid1;
1846
1847  /** Offset 0x06E3 - PCH Sata Rst Raid10
1848  RAID10.
1849  $EN_DIS
1850  */
1851  UINT8                               SataRstRaid10;
1852
1853  /** Offset 0x06E4 - PCH Sata Rst Raid5
1854  RAID5.
1855  $EN_DIS
1856  */
1857  UINT8                               SataRstRaid5;
1858
1859  /** Offset 0x06E5 - PCH Sata Rst Irrt
1860  Intel Rapid Recovery Technology.
1861  $EN_DIS
1862  */
1863  UINT8                               SataRstIrrt;
1864
1865  /** Offset 0x06E6 - PCH Sata Rst Orom Ui
1866  Banner
1866  OROM UI and BANNER.
```

```
1867     $EN_DIS
1868 */
1869     UINT8
1870         SataRstOromUiBanner;
1871 /**
1872     ** Offset 0x06E7 - PCH Sata Rst Orom Ui
1873     Delay
1874     00b: 2 secs; 01b: 4 secs; 10b: 6 secs; 11:
1875     8 secs (see: PCH_SATA_OROM_DELAY).
1876 */
1877     UINT8
1878         SataRstOromUiDelay;
1879
1880 /**
1881     ** Offset 0x06E8 - PCH Sata Rst Hdd Unlock
1882     Indicates that the HDD password unlock in
1883     the OS is enabled.
1884     $EN_DIS
1885 */
1886     UINT8
1887         SataRstHddUnlock;
1888
1889 /**
1890     ** Offset 0x06E9 - PCH Sata Rst Led Locate
1891     Indicates that the LED/SGPIO hardware is
1892     attached and ping to locate feature is
1893     enabled on the OS.
1894     $EN_DIS
1895 */
1896     UINT8
1897         SataRstLedLocate;
1898
1899 /**
1900     ** Offset 0x06EA - PCH Sata Rst Irrt Only
1901     Allow only IRRT drives to span internal
1902     and external ports.
1903     $EN_DIS
1904 */
1905     UINT8
1906         SataRstIrrtOnly;
```

```
1894
1895 /** Offset 0x06EB - PCH Sata Rst Smart
1896   Storage
1897   RST Smart Storage caching Bit.
1898   $EN_DIS
1899 */
1900
1901 /** Offset 0x06EC - PCH Sata Rst Pcie
1902   Storage Remap enable
1903   Enable Intel RST for PCIe Storage
1904   remapping.
1905 */
1906 /** Offset 0x06EF - PCH Sata Rst Pcie
1907   Storage Port
1908   Intel RST for PCIe Storage remapping -
1909   PCIe Port Selection (1-based, 0 = autodetect).
1910 */
1911 /** Offset 0x06F2 - PCH Sata Rst Pcie Device
1912   Reset Delay
1913   PCIe Storage Device Reset Delay in
1914   milliseconds. Default value is 100ms
1915 */
1916 /** Offset 0x06F5 - Enable eMMC HS400
1917   Training
1918   Deprecated.
1919   $EN_DIS
```

```
1919 */  
1920     UINT8  
1921         PchScsEmmcHs400TuningRequired;  
1922     /** Offset 0x06F6 - Set HS400 Tuning Data  
1923         Valid  
1924             Set if HS400 Tuning Data Valid.  
1925             $EN_DIS  
1926             */  
1927     UINT8  
1928         PchScsEmmcHs400DllDataValid;  
1929     /** Offset 0x06F7 - Rx Strobe Delay Control  
1930         Rx Strobe Delay Control - Rx Strobe Delay  
1931         DLL 1 (HS400 Mode).  
1932     */  
1933     UINT8  
1934         PchScsEmmcHs400RxStrobeDll1;  
1935     /**  
1936     UINT8  
1937         PchScsEmmcHs400TxDataDll;  
1938     /** Offset 0x06F8 - Tx Data Delay Control  
1939         Tx Data Delay Control 1 - Tx Data Delay  
1940         (HS400 Mode).  
1941     */  
1942     UINT8  
1943         PchScsEmmcHs400DriverStrength;  
1944     /** Offset 0x06FA - PCH SerialIo I2C Pads  
1945         Termination  
1946             0x0: Hardware default, 0x1: None, 0x13:  
1947             1kOhm weak pull-up, 0x15: 5kOhm weak pull-up,
```

```
1946    0x19: 20k0hm weak pull-up - Enable/disable
        SerialIo I2C0,I2C1,I2C2,I2C3,I2C4,I2C5
1947    pads termination respectively. One byte
        for each controller, byte0 for I2C0, byte1
1948    for I2C1, and so on.
1949 */
1950     UINT8
        PchSerialIoI2cPadsTermination[6];
1951
1952 /** Offset 0x0700
1953 */
1954     UINT8
        UnusedUpdSpace21;
1955
1956 /** Offset 0x0701 -
        PcdSerialIoUart0PinMuxing
1957 Select SerialIo Uart0 pin muxing. Setting
        applicable only if SerialIO UART0 is enabled.
1958 0:default pins, 1:pins muxed with
        CNV_BRI/RGI
1959 */
1960     UINT8
        SerialIoUart0PinMuxing;
1961
1962 /** Offset 0x0702
1963 */
1964     UINT8
        UnusedUpdSpace22[1];
1965
1966 /** Offset 0x0703 - Enables UART hardware
        flow control, CTS and RTS lines
1967 Enables UART hardware flow control, CTS
        and RTS linesh.
1968 */
1969     UINT8
        SerialIoUartHwFlowCtrl[3];
1970
```

```
1971 /** Offset 0x0706 - UART Number For Debug
1972 Purpose
1973   UART number for debug purpose. 0:UART0, 1:
1974     UART1, 2:UART2. Note: If UART0 is selected
1975     as CNVi BT Core interface, it cannot be
1976     used for debug purpose.
1977   0:UART0, 1:UART1, 2:UART2
1978 */
1979   UINT8
1980   SerialIoDebugUartNumber;
1981
1982 /**
1983   Enable debug UART controller after post.
1984   $EN_DIS
1985 */
1986   UINT8
1987   SerialIoEnableDebugUartAfterPost;
1988
1989 /**
1990   Offset 0x0708 - Enable Serial IRQ
1991   Determines if enable Serial IRQ.
1992   $EN_DIS
1993 */
1994   UINT8
1995   PchSirqEnable;
1996
1997 /**
1998   Offset 0x0709 - Serial IRQ Mode Select
1999   Serial IRQ Mode Select, 0: quiet mode, 1:
2000   continuous mode.
2001   $EN_DIS
2002 */
2003   UINT8
2004   PchSirqMode;
2005
2006 /**
2007   Offset 0x070A - Start Frame Pulse Width
2008   Start Frame Pulse Width, 0: PchSfpw4Clk,
2009   1: PchSfpw6Clk, 2: PchSfpw8Clk.
2010   0: PchSfpw4Clk, 1: PchSfpw6Clk, 2:
2011   PchSfpw8Clk
```

```
1999 */  
2000     UINT8  
2001         PchStartFramePulse;  
2002     /** Offset 0x070B - Reserved  
2003         Reserved  
2004         $EN_DIS  
2005     */  
2006     UINT8  
2007         ReservedForFuture1;  
2008     /** Offset 0x070C - Thermal Device SMI  
2009         Enable  
2010         This locks down SMI Enable on Alert  
2011         Thermal Sensor Trip.  
2012         $EN_DIS  
2013     */  
2014     UINT8                         PchTsmicLock;  
2015  
2016     /** Offset 0x070D - Thermal Throttling  
2017         Custimized T0Level Value  
2018         Custimized T0Level value.  
2019     */  
2020     UINT16                         PchT0Level;  
2021  
2022     /** Offset 0x070F - Thermal Throttling  
2023         Custimized T1Level Value  
2024         Custimized T1Level value.  
2025     */  
2026     UINT16                         PchT1Level;  
2027  
2028     /** Offset 0x0711 - Thermal Throttling  
2029         Custimized T2Level Value  
2030         Custimized T2Level value.  
2031     */  
2032     UINT16                         PchT2Level;
```

```
2029  /** Offset 0x0713 - Enable The Thermal
Throttle
2030  Enable the thermal throttle function.
2031  $EN_DIS
2032  */
2033  UINT8 PchTTEnable;
2034
2035  /** Offset 0x0714 - PMSync State 13
2036  When set to 1 and the programmed GPIO pin
is a 1, then PMSync state 13 will force
2037  at least T2 state.
2038  $EN_DIS
2039  */
2040  UINT8 PchTTState13Enable;
2041
2042  /** Offset 0x0715 - Thermal Throttle Lock
Thermal Throttle Lock.
2043  $EN_DIS
2044  */
2045  UINT8 PchTTLock;
2046
2047
2048  /** Offset 0x0716 - Thermal Throttling
Suggested Setting
2049  Thermal Throttling Suggested Setting.
2050  $EN_DIS
2051  */
2052  UINT8 TTSetting;
2053
2054  /** Offset 0x0717 - Enable PCH Cross
Throttling
2055  Enable/Disable PCH Cross Throttling
2056  $EN_DIS
2057  */
2058  UINT8 TTCrossThrottling;
```

```
2059
2060 /** Offset 0x0718 - DMI Thermal Sensor
   Autonomous Width Enable
2061   DMI Thermal Sensor Autonomous Width
   Enable.
2062   $EN_DIS
2063 */
2064   UINT8                               PchDmiTsawEn;
2065
2066 /** Offset 0x0719 - DMI Thermal Sensor
   Suggested Setting
2067   DMT thermal sensor suggested
   representative values.
2068   $EN_DIS
2069 */
2070   UINT8                               DmiSuggestedSetting;
2071
2072 /** Offset 0x071A - Thermal Sensor 0 Target
   Width
2073   DMT thermal sensor suggested
   representative values.
2074   0:x1, 1:x2, 2:x4, 3:x8, 4:x16
2075 */
2076   UINT8                               DmiTS0TW;
2077
2078 /** Offset 0x071B - Thermal Sensor 1 Target
   Width
2079   Thermal Sensor 1 Target Width.
2080   0:x1, 1:x2, 2:x4, 3:x8, 4:x16
2081 */
2082   UINT8                               DmiTS1TW;
2083
2084 /** Offset 0x071C - Thermal Sensor 2 Target
   Width
2085   Thermal Sensor 2 Target Width.
2086   0:x1, 1:x2, 2:x4, 3:x8, 4:x16
```

```
2087    */
2088    UINT8           DmiTS2TW;
2089
2090 /** Offset 0x071D - Thermal Sensor 3 Target
2091   Width
2092   Thermal Sensor 3 Target Width.
2093   0:x1, 1:x2, 2:x4, 3:x8, 4:x16
2094 */
2095    UINT8           DmiTS3TW;
2096
2097 /** Offset 0x071E - Port 0 T1 Multipler
2098   Port 0 T1 Multipler.
2099 */
2100    UINT8           SataP0T1M;
2101
2102 /** Offset 0x071F - Port 0 T2 Multipler
2103   Port 0 T2 Multipler.
2104 */
2105    UINT8           SataP0T2M;
2106
2107 /** Offset 0x0720 - Port 0 T3 Multipler
2108   Port 0 T3 Multipler.
2109 */
2110    UINT8           SataP0T3M;
2111
2112 /** Offset 0x0721 - Port 0 Tdispatch
2113   Port 0 Tdispatch.
2114 */
2115    UINT8           SataP0TDisp;
2116
2117 /** Offset 0x0722 - Port 1 T1 Multipler
2118   Port 1 T1 Multipler.
2119 */
2120    UINT8           SataP1T1M;
2121
2122 /** Offset 0x0723 - Port 1 T2 Multipler
2123   Port 1 T2 Multipler.
```

```
2123 */  
2124     UINT8           SataP1T2M;  
2125  
2126 /** Offset 0x0724 - Port 1 T3 Multiplier  
2127     Port 1 T3 Multiplier.  
2128 */  
2129     UINT8           SataP1T3M;  
2130  
2131 /** Offset 0x0725 - Port 1 Tdispatch  
2132     Port 1 Tdispatch.  
2133 */  
2134     UINT8           SataP1TDisp;  
2135  
2136 /** Offset 0x0726 - Port 0 Tinactive  
2137     Port 0 Tinactive.  
2138 */  
2139     UINT8           SataP0Tinact;  
2140  
2141 /** Offset 0x0727 - Port 0 Alternate Fast  
2142     Init Tdispatch  
2143     Port 0 Alternate Fast Init Tdispatch.  
2144     $EN_DIS  
2145 */  
2146     UINT8           SataP0TDispFinit;  
2147  
2148 /** Offset 0x0728 - Port 1 Tinactive  
2149     Port 1 Tinactive.  
2150 */  
2151     UINT8           SataP1Tinact;  
2152  
2153 /** Offset 0x0729 - Port 1 Alternate Fast  
2154     Init Tdispatch  
2155     Port 1 Alternate Fast Init Tdispatch.  
2156     $EN_DIS  
2157 */  
2158     UINT8
```

```
        SataP1TDispFinit;
2157
2158 /** Offset 0x072A - Sata Thermal Throttling
2159   Suggested Setting
2160   Sata Thermal Throttling Suggested Setting.
2161   $EN_DIS
2162 */
2163   UINT8
2164     SataThermalSuggestedSetting;
2165
2166 /** Offset 0x072B - Enable Memory Thermal
2167   Throttling
2168   Enable Memory Thermal Throttling.
2169   $EN_DIS
2170 */
2171   UINT8
2172     PchMemoryThrottlingEnable;
2173
2174 /** Offset 0x072C - Memory Thermal
2175   Throttling
2176   Enable Memory Thermal Throttling.
2177 */
2178   UINT8
2179     PchMemoryPmsyncEnable[2];
2180
2181 /** Offset 0x072E - Enable Memory Thermal
2182   Throttling
2183   Enable Memory Thermal Throttling.
2184 */
2185   UINT8
2186     PchMemoryC0TransmitEnable[2];
2187
2188 /** Offset 0x0730 - Enable Memory Thermal
2189   Throttling
2190   Enable Memory Thermal Throttling.
2191 */
2192   UINT8
```

```
        PchMemoryPinSelection[2];  
2184  
2185 /** Offset 0x0732 - Thermal Device  
Temperature  
2186     Decides the temperature.  
2187     **/  
2188     UINT16  
2189  
2190 /** Offset 0x0734 - Enable xHCI Compliance  
Mode  
2191     Compliance Mode can be enabled for testing  
through this option but this is disabled  
2192     by default.  
2193     $EN_DIS  
2194     **/  
2195     UINT8  
2196         PchEnableComplianceMode;  
2197  
2198 /** Offset 0x0735 - USB2 Port Over Current  
Pin  
2199     Describe the specific over current pin  
number of USB 2.0 Port N.  
2200     **/  
2201     UINT8  
2202         Usb2OverCurrentPin[16];  
2203  
2204 /** Offset 0x0745 - USB3 Port Over Current  
Pin  
2205     Describe the specific over current pin  
number of USB 3.0 Port N.  
2206     **/  
2207     UINT8  
2208         Usb30OverCurrentPin[10];  
2209  
2210 /** Offset 0x074F - Enable 8254 Static Clock  
Gating
```

```
2208 |     Set 8254CGE=1 is required for SLP_S0
      | support. However, set 8254CGE=1 in POST time
2209 |     might fail to boot legacy OS using 8254
      | timer. Make sure it is disabled to support
2210 |     boot legacy OS using 8254 timer. Also
      | enable this while S0ix is enabled.
2211 |     $EN_DIS
2212 | */
2213 |     UINT8
      |     Enable8254ClockGating;
2214 |
2215 | /** Offset 0x0750 - PCH Sata Rst Optane
      | Memory
2216 |     Optane Memory
2217 |     $EN_DIS
2218 | */
2219 |     UINT8
      |     SataRstOptaneMemory;
2220 |
2221 | /** Offset 0x0751 - PCH Sata Rst CPU
      | Attached Storage
2222 |     CPU Attached Storage
2223 |     $EN_DIS
2224 | */
2225 |     UINT8
      |     SataRstCpuAttachedStorage;
2226 |
2227 | /** Offset 0x0752 - Enable 8254 Static Clock
      | Gating On S3
2228 |     This is only applicable when
      |     Enable8254ClockGating is disabled. FSP will do
      |     the
2229 |     8254 CGE programming on S3 resume when
      |     Enable8254ClockGatingOnS3 is enabled. This
2230 |     avoids the SMI requirement for the
      |     programming.
2231 |     $EN_DIS
```

```
2232  */
2233  UINT8
2234     Enable8254ClockGatingOnS3;
2234
2235  /** Offset 0x0753
2236  */
2237  UINT8
2238     UnusedUpdSpace23;
2238
2239  /** Offset 0x0754 - Pch PCIE device override
2240   table pointer
2240   The PCIe device table is being used to
2241   override PCIe device ASPM settings. This
2241   is a pointer points to a 32bit address.
2242   And it's only used in PostMem phase. Please
2242   refer to PCH_PCIE_DEVICE_OVERRIDE
2243   structure for the table. Last entry VendorId
2243   must be 0.
2244  */
2245  UINT32
2245     PchPcieDeviceOverrideTablePtr;
2246
2247  /** Offset 0x0758 - Enable TCO timer.
2248   When FALSE, it disables PCH ACPI timer,
2249   and stops TCO timer. NOTE: This will have
2250   huge power impact when it's enabled. If
2251   TCO timer is disabled, uCode ACPI timer
2252   emulation must be enabled, and WDAT table
2253   must not be exposed to the OS.
2251     $EN_DIS
2252  */
2253  UINT8
2253     EnableTcoTimer;
2254
2255  /** Offset 0x0759 - BgpdtHash[4]
2256   BgpdtHash values
2257  */
```

```
2258     UINT64                                BgpdtHash[4];  
2259  
2260     /** Offset 0x0779 - BiosGuardAttr  
2261         BiosGuardAttr default values  
2262     **/  
2263     UINT32                                BiosGuardAttr;  
2264  
2265     /** Offset 0x077D - BiosGuardModulePtr  
2266         BiosGuardModulePtr default values  
2267     **/  
2268     UINT64  
2269         BiosGuardModulePtr;  
2270  
2271     /** Offset 0x0785 - SendEcCmd  
2272         SendEcCmd function pointer. \n  
2273         @code typedef EFI_STATUS (EFIAPI  
2274             *PLATFORM_SEND_EC_COMMAND) (IN EC_COMMAND_TYPE  
2275             EcCmdType, IN UINT8 EcCmd, IN UINT8  
2276             SendData, IN OUT UINT8 *ReceiveData);  
2277         @endcode  
2278     **/  
2279     UINT64                                SendEcCmd;  
2280  
2281     /** Offset 0x078D - EcCmdProvisionEav  
2282         Ephemeral Authorization Value default  
2283         values. Provisions an ephemeral shared secret  
2284         to the EC  
2285     **/  
2286     UINT8  
2287         EcCmdProvisionEav;  
2288  
2289     /** Offset 0x078E - EcCmdLock  
2290         EcCmdLock default values. Locks Ephemeral  
2291         Authorization Value sent previously  
2292     **/  
2293     UINT8  
2294         EcCmdLock;
```

```
2287 /** Offset 0x078F - SgxEpoch0
2288   SgxEpoch0 default values
2289 */
2290     UINT64           SgxEpoch0;
2291
2292 /** Offset 0x0797 - SgxEpoch1
2293   SgxEpoch1 default values
2294 */
2295     UINT64           SgxEpoch1;
2296
2297 /** Offset 0x079F - SgxSinitNvsData
2298   SgxSinitNvsData default values
2299 */
2300     UINT8
2301     SgxSinitNvsData;
2302
2303 /** Offset 0x07A0 - Si Config CSM Flag.
2304   Platform specific common policies that
2305   used by several silicon components. CSM status
2306   flag.
2307   $EN_DIS
2308 */
2309     UINT8           SiCsmFlag;
2310
2311 /** Offset 0x07A1
2312 */
2313     UINT32
2314     SiSsidTablePtr;
2315
2316 /** Offset 0x07A5
2317 */
2318     UINT16
2319     SiNumberOfSsidTableEntry;
2320
2321 /** Offset 0x07A7 - SATA RST Interrupt Mode
2322   Allowes to choose which interrupts will be
2323   implemented by SATA controller in RAID mode.
```

```
2318     0:Msix, 1:Msi, 2:Legacy
2319     */
2320     UINT8
2321     SataRstInterrupt;
2322     /** Offset 0x07A8 - ME Unconfig on RTC clear
2323      0: Disable ME Unconfig On Rtc Clear. <b>1:</b>
2324      Enable ME Unconfig On Rtc Clear</b>.
2325      2: Cmos is clear, status unkown. 3:
2326      Reserved
2327      0: Disable ME Unconfig On Rtc Clear, 1:
2328      Enable ME Unconfig On Rtc Clear, 2: Cmos
2329      is clear, 3: Reserved
2330     */
2331     UINT8
2332     MeUnconfigOnRtcClear;
2333     /** Offset 0x07A9 - Enable PS_ON.
2334      PS_ON is a new C10 state from the CPU on
2335      desktop SKUs that enables a lower power
2336      target that will be required by the
2337      California Energy Commission (CEC). When
2338      FALSE,
2339      PS_ON is to be disabled.
2340      $EN_DIS
2341      */
2342      UINT8                               PsOnEnable;
2343      /** Offset 0x07AA - Pmc Cpu C10 Gate Pin
2344      Enable
2345      Enable/Disable platform support for
2346      CPU_C10_GATE# pin to control gating of CPU
2347      VccIO
2348      and VccSTG rails instead of SLP_S0# pin.
2349      $EN_DIS
2350      */
2351      UINT8
```

```
        PmcCpuC10GatePinEnable;
2344    /** Offset 0x07AB - Pch Dmi Aspm Ctrl
2345     * ASPM configuration on the PCH side of the
2346     * DMI/OPI Link. Default is
2347     * <b>PchPcieAspmAutoConfig</b>
2348     * 0:Disabled, 1:L0s, 2:L1, 3:L0sL1, 4:Auto
2349     */
2350     UINT8
2351     PchDmiAspmCtrl;
2352
2353     /** Offset 0x07AC
2354     */
2355     UINT8
2356     ReservedFspsUpd[1];
2357 } FSP_S_CONFIG;
2358
2359 /**
2360  * Fsp S Test Configuration
2361  */
2362 typedef struct {
2363
2364     /** Offset 0x07AD
2365     */
2366     UINT32                               Signature;
2367
2368     /** Offset 0x07B1 - Enable/Disable Device 7
2369      * Enable: Device 7 enabled, Disable
2370      * (Default): Device 7 disabled
2371      * $EN_DIS
2372      */
2373     UINT8
2374     ChapDeviceEnable;
2375
2376     /** Offset 0x07B2 - Skip PAM register lock
2377      * Enable: PAM register will not be locked by
2378      * RC, platform code should lock it,
2379      * Disable(Default):
```

```
2372 |     PAM registers will be locked by RC
2373 |     $EN_DIS
2374 | */
2375 |     UINT8                     SkipPamLock;
2376 |
2377 | /** Offset 0x07B3 - EDRAM Test Mode
2378 |     Enable: PAM register will not be locked by
2379 |     RC, platform code should lock it,
2380 |     Disable(Default):
2381 |         PAM registers will be locked by RC
2382 |         0: EDRAM SW disable, 1: EDRAM SW Enable,
2383 |         2: EDRAM HW mode
2384 | */
2385 |     UINT8                     EdramTestMode;
2386 |
2387 |
2388 | /**
2389 |     UINT8                     DmiExtSync;
2390 |
2391 | /**
2392 |     Enable: Enable DMI Extended Sync Control,
2393 |     Disable(Default): Disable DMI Extended
2394 |     Sync Control
2395 |     $EN_DIS
2396 | */
2397 |     UINT8                     DmiIot;
2398 |
2399 | /**
2400 |     0xFF(Default):Auto, 0x1: Force 128B, 0x2:
2401 |     Force 256B
2402 |     0xFF: Auto, 0x1: Force 128B, 0x2: Force
2403 |     256B
```

```
2400  */
2401  UINT8
2402    PegMaxPayload[4];
2403 /**
2404  ** Offset 0x07BA - Enable/Disable IGFX
2405  ** RenderStandby
2406  ** Enable(Default): Enable IGFX
2407  ** RenderStandby, Disable: Disable IGFX
2408  ** RenderStandby
2409  */
2410  $EN_DIS
2411  */
2412  UINT8
2413  */
2414  RenderStandby;
2415 /**
2416  ** Offset 0x07BB - Enable/Disable IGFX
2417  ** PmSupport
2418  ** Enable(Default): Enable IGFX PmSupport,
2419  ** Disable: Disable IGFX PmSupport
2420  */
2421  $EN_DIS
2422  */
2423  UINT8
2424  */
2425  PmSupport;
2426 /**
2427  ** Offset 0x07BC - Enable/Disable
2428  ** CdynmaxClamp
2429  ** Enable(Default): Enable CdynmaxClamp,
2430  ** Disable: Disable CdynmaxClamp
2431  */
2432  $EN_DIS
2433  */
2434  UINT8
2435  CdynmaxClampEnable;
2436 /**
2437  ** Offset 0x07BD - Disable VT-d
2438  ** 0=Enable/FALSE(VT-d enabled),
2439  ** 1=Disable/TRUE (VT-d disabled)
2440  */
2441  $EN_DIS
2442  */
2443  UINT8
2444  */
2445  VtdDisable;
2446 */
```

```

2427  /** Offset 0x07BE - GT Frequency Limit
2428  0xFF: Auto(Default), 2: 100 Mhz, 3: 150
2429  Mhz, 4: 200 Mhz, 5: 250 Mhz, 6: 300 Mhz,
2430  7: 350 Mhz, 8: 400 Mhz, 9: 450 Mhz, 0xA:
2431  500 Mhz, 0xB: 550 Mhz, 0xC: 600 Mhz, 0xD:
2432  650 Mhz, 0xE: 700 Mhz, 0xF: 750 Mhz, 0x10:
2433  800 Mhz, 0x11: 850 Mhz, 0x12:900 Mhz,
2434  0x13: 950 Mhz, 0x14: 1000 Mhz, 0x15: 1050
2435  Mhz, 0x16: 1100 Mhz, 0x17: 1150 Mhz,
2436  0x18: 1200 Mhz
2437  0xFF: Auto(Default), 2: 100 Mhz, 3: 150
2438  Mhz, 4: 200 Mhz, 5: 250 Mhz, 6: 300 Mhz,
2439  7: 350 Mhz, 8: 400 Mhz, 9: 450 Mhz, 0xA:
2440  500 Mhz, 0xB: 550 Mhz, 0xC: 600 Mhz, 0xD:
2441  650 Mhz, 0xE: 700 Mhz, 0xF: 750 Mhz, 0x10:
2442  800 Mhz, 0x11: 850 Mhz, 0x12:900 Mhz,
2443  0x13: 950 Mhz, 0x14: 1000 Mhz, 0x15: 1050
2444  Mhz, 0x16: 1100 Mhz, 0x17: 1150 Mhz,
2445  0x18: 1200 Mhz
2446  */
2447  /** Offset 0x07BF - Disable Turbo GT
2448  0=Disable: GT frequency is not limited,
2449  1=Enable: Disables Turbo GT frequency
2450  $EN_DIS
2451  */
2452  UINT8
2453  GtFreqMax;
2454
2455  /**
2456  * @brief Get GT Frequency Limit
2457  *
2458  * @param[in] GtFreqMax GT Frequency Limit
2459  */
2460  void SaGetGtFreqLimit(UINT8 GtFreqMax)
2461  {
2462  #if defined(SA_ENABLE_TURBO_GT)
2463  #if defined(SA_DISABLE_TURBO_GT)
2464  #endif
2465  #endif
2466  }
2467
2468  /**
2469  * @brief Set GT Frequency Limit
2470  *
2471  * @param[in] GtFreqMax GT Frequency Limit
2472  */
2473  void SaSetGtFreqLimit(UINT8 GtFreqMax)
2474  {
2475  #if defined(SA_ENABLE_TURBO_GT)
2476  #if defined(SA_DISABLE_TURBO_GT)
2477  #endif
2478  #endif
2479  }
2480
2481  /**
2482  * @brief Get Turbo GT Status
2483  *
2484  * @return $EN_DIS
2485  */
2486  uint8_t SaGetTurboGtStatus()
2487  {
2488  #if defined(SA_ENABLE_TURBO_GT)
2489  #if defined(SA_DISABLE_TURBO_GT)
2490  #endif
2491  #endif
2492  }
2493
2494  /**
2495  * @brief Set Turbo GT Status
2496  *
2497  * @param[in] $EN_DIS
2498  */
2499  void SaSetTurboGtStatus(uint8_t $EN_DIS)
2500  {
2501  #if defined(SA_ENABLE_TURBO_GT)
2502  #if defined(SA_DISABLE_TURBO_GT)
2503  #endif
2504  #endif
2505  }
2506
2507  /**
2508  * @brief Get SA Post-Mem Test Rsvd
2509  *
2510  * @return SaPostMemTestRsvd[11]
2511  */
2512  uint8_t SaGetPostMemTestRsvd()
2513  {
2514  #if defined(SA_ENABLE_TURBO_GT)
2515  #if defined(SA_DISABLE_TURBO_GT)
2516  #endif
2517  #endif
2518  }
2519
2520  /**
2521  * @brief Set SA Post-Mem Test Rsvd
2522  *
2523  * @param[in] SaPostMemTestRsvd[11]
2524  */
2525  void SaSetPostMemTestRsvd(uint8_t SaPostMemTestRsvd[11])
2526  {
2527  #if defined(SA_ENABLE_TURBO_GT)
2528  #if defined(SA_DISABLE_TURBO_GT)
2529  #endif
2530  #endif
2531  }

```

```
2453 /** Offset 0x07CB - 1-Core Ratio Limit
2454   1-Core Ratio Limit: LFM to Fused, For
2455   overclocking part: LFM to 255. This 1-Core
2456   Ratio Limit Must be greater than or equal
2457   to 2-Core Ratio Limit, 3-Core Ratio Limit,
2458   4-Core Ratio Limit, 5-Core Ratio Limit, 6-
2459   Core Ratio Limit, 7-Core Ratio Limit,
2460   8-Core Ratio Limit. Range is 0 to 255
2461 */
2462   UINT8
2463   OneCoreRatioLimit;
2464
2465 /** Offset 0x07CC - 2-Core Ratio Limit
2466   2-Core Ratio Limit: LFM to Fused, For
2467   overclocking part: LFM to 255. This 2-Core
2468   Ratio Limit Must be Less than or equal to
2469   1-Core Ratio Limit. Range is 0 to 255
2470 */
2471   UINT8
2472   TwoCoreRatioLimit;
2473
2474 /** Offset 0x07CD - 3-Core Ratio Limit
2475   3-Core Ratio Limit: LFM to Fused, For
2476   overclocking part: LFM to 255. This 3-Core
2477   Ratio Limit Must be Less than or equal to
2478   1-Core Ratio Limit. Range is 0 to 255
2479 */
2480   UINT8
2481   ThreeCoreRatioLimit;
2482
2483 /** Offset 0x07CE - 4-Core Ratio Limit
2484   4-Core Ratio Limit: LFM to Fused, For
2485   overclocking part: LFM to 255. This 4-Core
2486   Ratio Limit Must be Less than or equal to
2487   1-Core Ratio Limit. Range is 0 to 255
2488 */
2489   UINT8
```

```
        FourCoreRatioLimit;
2478    /** Offset 0x07CF - Enable or Disable HWP
2480        Enable or Disable HWP(Hardware P states)
2481        Support. 0: Disable; <b>1: Enable;</b>
2482        2-3:Reserved
2483        $EN_DIS
2484        */
2485        UINT8                                Hwp;
2486    /** Offset 0x07D0 - Hardware Duty Cycle
2487        Control
2488        Hardware Duty Cycle Control configuration.
2489        0: Disabled; <b>1: Enabled</b> 2-3:Reserved
2490        $EN_DIS
2491        */
2492        UINT8                                HdcControl;
2493    /** Offset 0x07D1 - Package Long duration
2494        turbo mode time
2495        Package Long duration turbo mode time
2496        window in seconds. 0 = AUTO, uses 28 seconds.
2497        Valid values(Unit in seconds) 1 to 8 , 10
2498        , 12 ,14 , 16 , 20 , 24 , 28 , 32 , 40
2499        , 48 , 56 , 64 , 80 , 96 , 112 , 128
2500        */
2501        UINT8
2502        PowerLimit1Time;
2503    /** Offset 0x07D2 - Short Duration Turbo
2504        Mode
2505        Enable or Disable short duration Turbo
2506        Mode. <b>0 : Disable; <b>1: Enable</b>
2507        $EN_DIS
2508        */
2509        UINT8                                PowerLimit2;
2510
```

```
2505 /** Offset 0x07D3 - Turbo settings Lock
2506   Lock all Turbo settings Enable/Disable;
2507   <b>0: Disable , </b> 1: Enable
2508   $EN_DIS
2509 */
2510   UINT8
2511   TurboPowerLimitLock;
2512
2513 /**
2514   UINT8
2515   PowerLimit3Time;
2516
2517 /**
2518   Package PL3 Duty Cycle
2519   Package PL3 Duty Cycle; Valid Range is 0
2520   to 100
2521 */
2522   UINT8
2523   PowerLimit3DutyCycle;
2524
2525 /**
2526   Package PL3 Lock
2527   Package PL3 Lock Enable/Disable; <b>0:</b>
2528   Disable ; <b>1:</b> Enable
2529   $EN_DIS
2530 */
2531   UINT8
2532   PowerLimit3Lock;
2533
2534 /**
2535   Package PL4 Lock
2536   Package PL4 Lock Enable/Disable; <b>0:</b>
2537   Disable ; <b>1:</b> Enable
2538   $EN_DIS
2539 */
2540   UINT8
2541   PowerLimit4Lock;
```

```
2532
2533 /** Offset 0x07D8 - TCC Activation Offset
2534   TCC Activation Offset. Offset from factory
2535   set TCC activation temperature at which
2536   the Thermal Control Circuit must be
2537   activated. TCC will be activated at TCC
2538   Activation
2539   Temperature, in volts. For Y SKU, the
2540   recommended default for this policy is
2541   <b>15</b>,
2542   For all other SKUs the recommended default
2543   are <b>0</b>
2544 */
2545   UINT8
2546   TccActivationOffset;
2547
2548 /**
2549   ** Offset 0x07D9 - Tcc Offset Clamp
2550   Enable/Disable
2551   Tcc Offset Clamp for Runtime Average
2552   Temperature Limit (RATL) allows CPU to
2553   throttle
2554   below P1. For Y SKU, the recommended
2555   default for this policy is <b>1: Enabled</b>,
2556   For all other SKUs the recommended default
2557   are <b>0: Disabled</b>.
2558
2559   $EN_DIS
2560 */
2561   UINT8
2562   TccOffsetClamp;
2563
2564 /**
2565   ** Offset 0x07DA - Tcc Offset Lock
2566   Tcc Offset Lock for Runtime Average
2567   Temperature Limit (RATL) to lock temperature
2568   target; <b>0: Disabled</b>; 1: Enabled.
2569   $EN_DIS
2570 */
2571   UINT8
2572   TccOffsetLock;
```

```
2555
2556 /** Offset 0x07DB - Custom Ratio State
Entries
2557 The number of custom ratio state entries,
ranges from 0 to 40 for a valid custom
2558 ratio table.Sets the number of custom P-
states. At least 2 states must be present
2559 */
2560     UINT8
2561     NumberOfEntries;
2562
2563 /** Offset 0x07DC - Custom Short term Power
Limit time window
2564 Short term Power Limit time window value
for custom CTDP level 1. Valid Range 0
2565 to 128, 0 = AUTO
2566 */
2567     UINT8
2568     Custom1PowerLimit1Time;
2569
2570 /** Offset 0x07DD - Custom Turbo Activation
Ratio
2571 Turbo Activation Ratio for custom cTDP
level 1. Valid Range 0 to 255
2572 */
2573     UINT8
2574     Custom1TurboActivationRatio;
2575
2576 /** Offset 0x07DE - Custom Config Tdp
Control
2577 Config Tdp Control (0/1/2) value for
custom cTDP level 1. Valid Range is 0 to 2
2578 */
2579     UINT8
2580     Custom1ConfigTdpControl;
2581
2582 /** Offset 0x07DF - Custom Short term Power
```

```
    Limit time window
2579|    Short term Power Limit time window value
      for custom CTDP level 2. Valid Range 0
2580|        to 128, 0 = AUTO
2581|    */
2582|    UINT8
2583|        Custom2PowerLimit1Time;
2584|    /** Offset 0x07E0 - Custom Turbo Activation
      Ratio
2585|        Turbo Activation Ratio for custom cTDP
      level 2. Valid Range 0 to 255
2586|    */
2587|    UINT8
2588|        Custom2TurboActivationRatio;
2589|    /** Offset 0x07E1 - Custom Config Tdp
      Control
2590|        Config Tdp Control (0/1/2) value for
      custom cTDP level 1. Valid Range is 0 to 2
2591|    */
2592|    UINT8
2593|        Custom2ConfigTdpControl;
2594|    /** Offset 0x07E2 - Custom Short term Power
      Limit time window
2595|        Short term Power Limit time window value
      for custom CTDP level 3. Valid Range 0
2596|        to 128, 0 = AUTO
2597|    */
2598|    UINT8
2599|        Custom3PowerLimit1Time;
2600|    /** Offset 0x07E3 - Custom Turbo Activation
      Ratio
2601|        Turbo Activation Ratio for custom cTDP
      level 3. Valid Range 0 to 255
```

```
2602  */
2603  UINT8
2604  Custom3TurboActivationRatio;
2605  /** Offset 0x07E4 - Custom Config Tdp
2606  Control
2607  Config Tdp Control (0/1/2) value for
2608  custom cTDP level 1. Valid Range is 0 to 2
2609  */
2610  /** Offset 0x07E5 - ConfigTdp mode settings
2611  Lock
2612  Lock the ConfigTdp mode settings from
2613  runtime changes; <b>0: Disable</b>; 1: Enable
2614  $EN_DIS
2615  */
2616  /** Offset 0x07E6 - Load Configurable TDP
2617  SSDT
2618  Configure whether to load Configurable TDP
2619  SSDT; <b>0: Disable</b>; 1: Enable.
2620  $EN_DIS
2621  */
2622  /** Offset 0x07E7 - PL1 Enable value
2623  PL1 Enable value to limit average platform
2624  power. <b>0: Disable</b>; 1: Enable.
2625  $EN_DIS
2626  */
2627  /** Offset 0x07E8 - PL1 timewindow
2628  PsysPowerLimit1;
```

```
2629     PL1 timewindow in seconds. 0 = AUTO, uses
2630     28 seconds. Valid values(Unit in seconds)
2630     1 to 8 , 10 , 12 ,14 , 16 , 20 , 24 , 28 ,
2630     32 , 40 , 48 , 56 , 64 , 80 , 96 , 112 , 128
2631 */
2632     UINT8
2632     PsysPowerLimit1Time;
2633
2634 /** Offset 0x07E9 - PL2 Enable Value
2635     PL2 Enable activates the PL2 value to
2635     limit average platform power.<b>0:</b>
2635     Disable</b>;
2636     1: Enable.
2637     $EN_DIS
2638 */
2639     UINT8
2639     PsysPowerLimit2;
2640
2641 /** Offset 0x07EA - Enable or Disable MLC
2641     Streamer Prefetcher
2642     Enable or Disable MLC Streamer Prefetcher;
2642     0: Disable; <b>1: Enable</b>.
2643     $EN_DIS
2644 */
2645     UINT8
2645     MlcStreamerPrefetcher;
2646
2647 /** Offset 0x07EB - Enable or Disable MLC
2647     Spatial Prefetcher
2648     Enable or Disable MLC Spatial Prefetcher;
2648     0: Disable; <b>1: Enable</b>
2649     $EN_DIS
2650 */
2651     UINT8
2651     MlcSpatialPrefetcher;
2652
2653 /** Offset 0x07EC - Enable or Disable
```

```
    Monitor /MWAIT instructions
2654|   Enable or Disable Monitor /MWAIT
      instructions; 0: Disable; <b>1: Enable</b>.
2655|   $EN_DIS
2656| /**
2657|   UINT8
      MonitorMwaitEnable;
2658|
2659| /** Offset 0x07ED - Enable or Disable
      initialization of machine check registers
2660|   Enable or Disable initialization of
      machine check registers; 0: Disable; <b>1:
      Enable</b>.
2661|   $EN_DIS
2662| /**
2663|   UINT8
      MachineCheckEnable;
2664|
2665| /** Offset 0x07EE - Deprecated DO NOT USE
      Enable or Disable processor debug features
2666|   @deprecated Enable or Disable processor
      debug features; <b>0: Disable</b>; 1: Enable.
2667|   $EN_DIS
2668| /**
2669|   UINT8
      DebugInterfaceEnable;
2670|
2671| /** Offset 0x07EF - Lock or Unlock debug
      interface features
2672|   Lock or Unlock debug interface features;
      0: Disable; <b>1: Enable</b>.
2673|   $EN_DIS
2674| /**
2675|   UINT8
      DebugInterfaceLockEnable;
2676|
2677| /** Offset 0x07F0 - AP Idle Manner of
```

```
    waiting for SIPI
2678|    AP Idle Manner of waiting for SIPI; 1:
      HALT loop; <b>2: MWAIT loop</b>; 3: RUN loop.
2679|    1: HALT loop, 2: MWAIT loop, 3: RUN loop
2680| */
2681|     UINT8                               ApIdleManner;
2682|
2683| /** Offset 0x07F1 - Control on Processor
      Trace output scheme
2684|     Control on Processor Trace output scheme;
      <b>0: Single Range Output</b>; 1: ToPA Output.
2685|     0: Single Range Output, 1: ToPA Output
2686| */
2687|     UINT8
2688|     ProcessorTraceOutputScheme;
2689| /**
2690|     Processor Trace feature
2691|     Enable or Disable Processor Trace feature;
      <b>0: Disable</b>; 1: Enable.
2692|     $EN_DIS
2693| */
2694|     UINT8
2695|     ProcessorTraceEnable;
2696| /**
2697|     Base of memory region
      allocated for Processor Trace
2698|     Base address of memory region allocated
      for Processor Trace. Processor Trace requires
2699|     2^N alignment and size in bytes per
      thread, from 4KB to 128MB. <b>0: Disable</b>
2700| */
2701|     UINT64
2702|     ProcessorTraceMemBase;
2703| /**
2704|     Memory region allocation
      for Processor Trace
```

```
2702 |     Length in bytes of memory region allocated
|         for Processor Trace. Processor Trace
2703 |     requires 2^N alignment and size in bytes
|         per thread, from 4KB to 128MB. <b>0:
|             Disable</b>
2704 | */
2705 |     UINT32
|         ProcessorTraceMemLength;
2706 |
2707 | /** Offset 0x07FF - Enable or Disable
|     Voltage Optimization feature
2708 |     Enable or Disable Voltage Optimization
|         feature 0: Disable; <b>1: Enable</b>
2709 |     $EN_DIS
2710 | */
2711 |     UINT8
|         VoltageOptimization;
2712 |
2713 | /** Offset 0x0800 - Enable or Disable Intel
|     SpeedStep Technology
2714 |     Enable or Disable Intel SpeedStep
|         Technology. 0: Disable; <b>1: Enable</b>
2715 |     $EN_DIS
2716 | */
2717 |     UINT8                           Eist;
2718 |
2719 | /** Offset 0x0801 - Enable or Disable Energy
|     Efficient P-state
2720 |     Enable or Disable Energy Efficient P-state
|         will be applied in Turbo mode. Disable;
|             <b>1: Enable</b>
2721 |     $EN_DIS
2722 | */
2723 |     UINT8
|         EnergyEfficientPState;
2724 |
2725 | /** Offset 0x0802 - Enable or Disable Energy
```

```
    Efficient Turbo
2727|     Enable or Disable Energy Efficient Turbo,
      will be applied in Turbo mode. Disable;
2728|     <b>1: Enable</b>
2729|     $EN_DIS
2730|     */
2731|     UINT8
2732|     EnergyEfficientTurbo;
2733| /**
2733|  ** Offset 0x0803 - Enable or Disable T
2733|  states
2734|     Enable or Disable T states; <b>0:</b>
2734|     Disable</b>; 1: Enable.
2735|     $EN_DIS
2736|     */
2737|     UINT8                      TStates;
2738|
2739| /**
2739|  ** Offset 0x0804 - Enable or Disable Bi-
2739|  Directional PROCHOT#
2740|     Enable or Disable Bi-Directional PROCHOT#;
2740|     0: Disable; <b>1: Enable</b>
2741|     $EN_DIS
2742|     */
2743|     UINT8                      BiProcHot;
2744|
2745| /**
2745|  ** Offset 0x0805 - Enable or Disable
2745|  PROCHOT# signal being driven externally
2746|     Enable or Disable PROCHOT# signal being
2746|     driven externally; 0: Disable; <b>1:
2746|     Enable</b>.
2747|     $EN_DIS
2748|     */
2749|     UINT8
2749|     DisableProcHotOut;
2750|
2751| /**
2751|  ** Offset 0x0806 - Enable or Disable
2751|  PROCHOT# Response
```

```
2752 |     Enable or Disable PROCHOT# Response; <b>0:</b>
      |         Disable</b>; 1: Enable.
2753 |     $EN_DIS
2754 | */
2755 |     UINT8
2756 |     ProHotResponse;
2757 | /**
2758 |     ** Offset 0x0807 - Enable or Disable VR
2759 |     Thermal Alert
2760 |     Enable or Disable VR Thermal Alert; <b>0:</b>
2761 |         Disable</b>; 1: Enable.
2762 |         $EN_DIS
2763 | /**
2764 |         UINT8
2765 |         DisableVrThermalAlert;
2766 | /**
2767 |         ** Offset 0x0808 - Enable or Disable
2768 |         Thermal Reporting
2769 |         Enable or Disable Thermal Reporting
2770 |             through ACPI tables; 0: Disable; <b>1:</b>
2771 |                 Enable</b>.
2772 |                 $EN_DIS
2773 | /**
2774 |                 UINT8
2775 |                 AutoThermalReporting;
2776 | /**
2777 |                 ** Offset 0x0809 - Enable or Disable
2778 |                 Thermal Monitor
2779 |                 Enable or Disable Thermal Monitor; 0:
2780 |                     Disable; <b>1:</b> Enable</b>
2781 |                     $EN_DIS
2782 | /**
2783 |                     UINT8
2784 |                     ThermalMonitor;
2785 | /**
2786 |                     ** Offset 0x080A - Enable or Disable CPU
2787 |                         power states (C-states)
```

```
2776    Enable or Disable CPU power states (C-
states). 0: Disable; <b>1: Enable</b>
2777    $EN_DIS
2778    */
2779    UINT8                               Cx;
2780
2781 /** Offset 0x080B - Configure C-State
Configuration Lock
2782 Configure C-State Configuration Lock; 0:
Disable; <b>1: Enable</b>.
2783 $EN_DIS
2784 */
2785 UINT8
PmgCstCfgCtrlLock;
2786
2787 /** Offset 0x080C - Enable or Disable
Enhanced C-states
2788 Enable or Disable Enhanced C-states. 0:
Disable; <b>1: Enable</b>
2789 $EN_DIS
2790 */
2791 UINT8                               C1e;
2792
2793 /** Offset 0x080D - Enable or Disable
Package Cstate Demotion
2794 Enable or Disable Package Cstate Demotion.
<b>0: Disable</b>; 1: Enable
2795 $EN_DIS
2796 */
2797 UINT8
PkgCStateDemotion;
2798
2799 /** Offset 0x080E - Enable or Disable
Package Cstate UnDemotion
2800 Enable or Disable Package Cstate
UnDemotion. <b>0: Disable</b>; 1: Enable
2801 $EN_DIS
```

```
2802    /**/
2803    UINT8
2804    PkgCStateUnDemotion;
2805    /** Offset 0x080F - Enable or Disable
2806    CState-Pre wake
2807    Enable or Disable CState-Pre wake. 0:
2808    Disable; <b>1: Enable</b>
2809    $EN_DIS
2810    **/
2811    UINT8                      CStatePrewake;
2812
2813    /** Offset 0x0810 - Enable or Disable
2814    TimedMwait Support.
2815    Enable or Disable TimedMwait Support.
2816    <b>0: Disable</b>; 1: Enable
2817    $EN_DIS
2818    **/
2819    UINT8                      TimedMwait;
2820
2821
2822    /** Offset 0x0811 - Enable or Disable IO to
2823    MWAIT redirection
2824    Enable or Disable IO to MWAIT redirection;
2825    <b>0: Disable</b>; 1: Enable.
2826    $EN_DIS
2827    **/
2828    UINT8
2829    CstCfgCtrIoMwaitRedirection;
2830
2831
2832    /** Offset 0x0812 - Set the Max Pkg Cstate
2833    Set the Max Pkg Cstate. Default set to
2834    Auto which limits the Max Pkg Cstate to deep
2835    C-state. Valid values 0 - C0/C1 , 1 - C2 ,
2836    2 - C3 , 3 - C6 , 4 - C7 , 5 - C7S ,
2837    6 - C8 , 7 - C9 , 8 - C10 , 254 - CPU
2838    Default , 255 - Auto
2839    **/
2840
```

```
2828 |     UINT8
2829 |     PkgCStateLimit;
2830 | /** Offset 0x0813 - TimeUnit for C-State
2831 |     Latency Control0
2832 |     TimeUnit for C-State Latency Control0;
2833 |     Valid values 0 - 1ns , 1 - 32ns , 2 - 1024ns
2834 |     , 3 - 32768ns , 4 - 1048576ns , 5 -
2835 |     33554432ns
2836 | */
2837 |     UINT8
2838 |     CstateLatencyControl0TimeUnit;
2839 |
2840 | /** Offset 0x0814 - TimeUnit for C-State
2841 |     Latency Control1
2842 |     TimeUnit for C-State Latency
2843 |     Control1;Valid values 0 - 1ns , 1 - 32ns , 2 -
2844 |     1024ns
2845 |     , 3 - 32768ns , 4 - 1048576ns , 5 -
2846 |     33554432ns
2847 | */
2848 |     UINT8
2849 |     CstateLatencyControl1TimeUnit;
2850 |
2851 | /** Offset 0x0815 - TimeUnit for C-State
2852 |     Latency Control2
2853 |     TimeUnit for C-State Latency
2854 |     Control2;Valid values 0 - 1ns , 1 - 32ns , 2 -
2855 |     1024ns
2856 |     , 3 - 32768ns , 4 - 1048576ns , 5 -
2857 |     33554432ns
2858 | */
2859 |     UINT8
2860 |     CstateLatencyControl2TimeUnit;
2861 |
2862 | /** Offset 0x0816 - TimeUnit for C-State
2863 |     Latency Control3
```

```
2849 |     TimeUnit for C-State Latency
      |     Control3;Valid values 0 - 1ns , 1 - 32ns , 2 -
      |     1024ns
2850 |     , 3 - 32768ns , 4 - 1048576ns , 5 -
      |     33554432ns
2851 |     */
2852 |     UINT8
      |     CstateLatencyControl3TimeUnit;
2853 |
2854 |     /** Offset 0x0817 - TimeUnit for C-State
      |     Latency Control4
2855 |     Time - 1ns , 1 - 32ns , 2 - 1024ns , 3 -
      |     32768ns , 4 - 1048576ns , 5 - 33554432ns
2856 |     */
2857 |     UINT8
      |     CstateLatencyControl4TimeUnit;
2858 |
2859 |     /** Offset 0x0818 - TimeUnit for C-State
      |     Latency Control5
2860 |     TimeUnit for C-State Latency
      |     Control5;Valid values 0 - 1ns , 1 - 32ns , 2 -
      |     1024ns
2861 |     , 3 - 32768ns , 4 - 1048576ns , 5 -
      |     33554432ns
2862 |     */
2863 |     UINT8
      |     CstateLatencyControl5TimeUnit;
2864 |
2865 |     /** Offset 0x0819 - Interrupt Redirection
      |     Mode Select
2866 |     Interrupt Redirection Mode Select.0: Fixed
      |     priority; 1: Round robin;2: Hash vector;4:
2867 |     PAIR with fixed priority;5: PAIR with
      |     round robin;6: PAIR with hash vector;7: No
      |     change.
2868 |     */
2869 |     UINT8                                     PpmIrmSetting;
```

```
2870
2871 /** Offset 0x081A - Lock prochot
2872   configuration
2873   Lock prochot configuration Enable/Disable;
2874   <b>0: Disable</b>; 1: Enable
2875   $EN_DIS
2876   */
2877   UINT8                               ProcHotLock;
2878
2879 /** Offset 0x081B - Configuration for boot
2880   TDP selection
2881   Configuration for boot TDP selection;
2882   <b>0: TDP Nominal</b>; 1: TDP Down; 2: TDP
2883   Up; 0xFF : Deactivate
2884   */
2885   UINT8                               ConfigTdpLevel;
2886
2887 /** Offset 0x081C - Race To Halt
2888   Enable/Disable Race To Halt feature. RTH
2889   will dynamically increase CPU frequency
2890   in order to enter pkg C-State faster to
2891   reduce overall power. (RTH is controlled
2892   through MSR 1FC bit 20)Disable; <b>1:
2893   Enable</b>
2894   $EN_DIS
2895   */
2896   UINT8                               RaceToHalt;
2897
2898 /** Offset 0x081D - Max P-State Ratio
2899   Max P-State Ratio, Valid Range 0 to 0x7F
2900   */
2901   UINT8                               MaxRatio;
2902
2903 /** Offset 0x081E - P-state ratios for
2904   custom P-state table
2905   P-state ratios for custom P-state table.
```

```
        NumberOfEntries has valid range between
2898|    0 to 40. For no. of P-States
      supported(NumberOfEntries) ,
      StateRatio[NumberOfEntries]
2899|    are configurable. Valid Range of each
      entry is 0 to 0x7F
2900| */
2901|     UINT8
      StateRatio[40];
2902|
2903| /** Offset 0x0846 - P-state ratios for max
      16 version of custom P-state table
2904|     P-state ratios for max 16 version of
      custom P-state table. This table is used for
2905|     OS versions limited to a max of 16 P-
      States. If the first entry of this table is
2906|     0, or if Number of Entries is 16 or less,
      then this table will be ignored, and
2907|     up to the top 16 values of the StateRatio
      table will be used instead. Valid Range
2908|     of each entry is 0 to 0x7F
2909| */
2910|     UINT8
      StateRatioMax16[16];
2911|
2912| /** Offset 0x0856 - Platform Power Pmax
2913|     PCODE MMIO Mailbox: Platform Power Pmax.
      <b>0 - Auto</b> Specified in 1/8 Watt
      increments.
2914|     Range 0-1024 Watts. Value of 800 = 100W
2915| */
2916|     UINT16                                PsysPmax;
2917|
2918| /** Offset 0x0858 - Interrupt Response Time
      Limit of C-State LatencyControl0
2919|     Interrupt Response Time Limit of C-State
      LatencyControl0.Range of value 0 to 0x3FF
```

```
2920  */
2921  UINT16
2922    CstateLatencyControl0Irtl;
2923 /**
2924   ** Offset 0x085A - Interrupt Response Time
2925   Limit of C-State LatencyContol1
2926   Interrupt Response Time Limit of C-State
2927   LatencyContol1.Range of value 0 to 0x3FF
2928 */
2929  UINT16
2930    CstateLatencyControl1Irtl;
2931 /**
2932   ** Offset 0x085C - Interrupt Response Time
2933   Limit of C-State LatencyContol2
2934   Interrupt Response Time Limit of C-State
2935   LatencyContol2.Range of value 0 to 0x3FF
2936 */
2937  UINT16
2938    CstateLatencyControl2Irtl;
2939 /**
2940   ** Offset 0x085E - Interrupt Response Time
2941   Limit of C-State LatencyContol3
2942   Interrupt Response Time Limit of C-State
2943   LatencyContol3.Range of value 0 to 0x3FF
2944 */
2945  UINT16
2946    CstateLatencyControl3Irtl;
2947 /**
2948   ** Offset 0x0860 - Interrupt Response Time
2949   Limit of C-State LatencyContol4
2950   Interrupt Response Time Limit of C-State
2951   LatencyContol4.Range of value 0 to 0x3FF
2952 */
2953  UINT16
2954    CstateLatencyControl4Irtl;
2955 /**
2956   ** Offset 0x0862 - Interrupt Response Time
```

```
    Limit of C-State LatencyControl5
2944|    Interrupt Response Time Limit of C-State
        LatencyControl5.Range of value 0 to 0x3FF
2945| */
2946|     UINT16
        CstateLatencyControl5Irtl;
2947|
2948| /** Offset 0x0864 - Package Long duration
        turbo mode power limit
2949|     Package Long duration turbo mode power
        limit. Units are based on
        POWER_MGMT_CONFIG.CustomPowerUnit.
2950|     Valid Range 0 to 4095875 in Step size of
        125
2951| */
2952|     UINT32                           PowerLimit1;
2953|
2954| /** Offset 0x0868 - Package Short duration
        turbo mode power limit
2955|     Package Short duration turbo mode power
        limit. Units are based on
        POWER_MGMT_CONFIG.CustomPowerUnit.Valid
2956|     Range 0 to 4095875 in Step size of 125
2957| */
2958|     UINT32                           PowerLimit2Power;
2959|
2960| /** Offset 0x086C - Package PL3 power limit
2961|     Package PL3 power limit. Units are based
        on POWER_MGMT_CONFIG.CustomPowerUnit.Valid
2962|     Range 0 to 4095875 in Step size of 125
2963| */
2964|     UINT32                           PowerLimit3;
2965|
2966| /** Offset 0x0870 - Package PL4 power limit
2967|     Package PL4 power limit. Units are based
        on POWER_MGMT_CONFIG.CustomPowerUnit.Valid
```

```
2968 |     Range 0 to 1023875 in Step size of 125
2969 | */
2970 |     UINT32                                     PowerLimit4;
2971 |
2972 | /** Offset 0x0874 - Tcc Offset Time Window
2973 |   for RATL
2974 |   Package PL4 power limit. Units are based
2975 |   on POWER_MGMT_CONFIG.CustomPowerUnit.Valid
2976 |   Range 0 to 1023875 in Step size of 125
2977 | */
2978 |     UINT32                                     TccOffsetTimeWindowForRatl;
2979 |
2980 | /** Offset 0x0878 - Short term Power Limit
2981 |   value for custom cTDP level 1
2982 |   Short term Power Limit value for custom
2983 |   cTDP level 1. Units are based on
2984 |   POWER_MGMT_CONFIG.CustomPowerUnit.Valid
2985 |   Range 0 to 4095875 in Step size of 125
2986 | */
2987 |     UINT32                                     Custom1PowerLimit1;
2988 |
2989 | /** Offset 0x087C - Long term Power Limit
2990 |   value for custom cTDP level 1
2991 |   Long term Power Limit value for custom
2992 |   cTDP level 1. Units are based on
2993 |   POWER_MGMT_CONFIG.CustomPowerUnit.Valid
2994 |   Range 0 to 4095875 in Step size of 125
2995 | */
2996 |     UINT32                                     Custom1PowerLimit2;
2997 |
2998 | /** Offset 0x0880 - Short term Power Limit
2999 |   value for custom cTDP level 2
3000 |   Short term Power Limit value for custom
3001 |   cTDP level 2. Units are based on
```

```
    POWER_MGMT_CONFIG.CustomPowerUnit.Valid
2992|      Range 0 to 4095875 in Step size of 125
2993|  */
2994|  UINT32
2995|  Custom2PowerLimit1;
2996|  /** Offset 0x0884 - Long term Power Limit
2997|   value for custom cTDP level 2
2998|   Long term Power Limit value for custom
2999|   cTDP level 2. Units are based on
3000|   POWER_MGMT_CONFIG.CustomPowerUnit.Valid
3001|   Range 0 to 4095875 in Step size of 125
3002|  */
3003|  UINT32
3004|  Custom2PowerLimit2;
3005|  /** Offset 0x0888 - Short term Power Limit
3006|   value for custom cTDP level 3
3007|   Short term Power Limit value for custom
3008|   cTDP level 3. Units are based on
3009|   POWER_MGMT_CONFIG.CustomPowerUnit.Valid
3010|   Range 0 to 4095875 in Step size of 125
3011|  */
3012|  UINT32
3013|  Custom3PowerLimit1;
3014|  /** Offset 0x088C - Long term Power Limit
3015|   value for custom cTDP level 3
3016|   Long term Power Limit value for custom
3017|   cTDP level 3. Units are based on
3018|   POWER_MGMT_CONFIG.CustomPowerUnit.Valid
3019|   Range 0 to 4095875 in Step size of 125
3020|  */
3021|  UINT32
3022|  Custom3PowerLimit2;
3023|
3024|  /** Offset 0x0890 - Platform PL1 power
```

```
3015     Platform PL1 power. Units are based on
          POWER_MGMT_CONFIG.CustomPowerUnit.Valid Range
3016     0 to 4095875 in Step size of 125
3017 */
3018     UINT32
          PsysPowerLimit1Power;
3019
3020 /** Offset 0x0894 - Platform PL2 power
3021     Platform PL2 power. Units are based on
          POWER_MGMT_CONFIG.CustomPowerUnit.Valid Range
3022     0 to 4095875 in Step size of 125
3023 */
3024     UINT32
          PsysPowerLimit2Power;
3025
3026 /** Offset 0x0898 - Set Three Strike Counter
          Disable
3027     False (default): Three Strike counter will
          be incremented and True: Prevents Three
3028     Strike counter from incrementing; <b>0:</b>
          False</b>; 1: True.
3029     0: False, 1: True
3030 */
3031     UINT8
          ThreeStrikeCounterDisable;
3032
3033 /** Offset 0x0899 - Set HW P-State
          Interrupts Enabled for for MISC_PWR_MGMT
3034     Set HW P-State Interrupts Enabled for for
          MISC_PWR_MGMT; <b>0:</b> Disable</b>; 1: Enable.
3035     $EN_DIS
3036 */
3037     UINT8
          HwpInterruptControl;
3038
3039 /** Offset 0x089A - 5-Core Ratio Limit
          5-Core Ratio Limit: LFM to Fused, For
```

```
    overclocking part: LFM to 255. This 5-Core
3041    Ratio Limit Must be Less than or equal to
1-Core Ratio Limit.Range is 0 to 255
3042    0x0:0xFF
3043    */
3044    UINT8
      FiveCoreRatioLimit;
3045
3046    /** Offset 0x089B - 6-Core Ratio Limit
3047    6-Core Ratio Limit: LFM to Fused, For
      overclocking part: LFM to 255. This 6-Core
3048    Ratio Limit Must be Less than or equal to
1-Core Ratio Limit.Range is 0 to 255
3049    0x0:0xFF
3050    */
3051    UINT8
      SixCoreRatioLimit;
3052
3053    /** Offset 0x089C - 7-Core Ratio Limit
3054    7-Core Ratio Limit: LFM to Fused, For
      overclocking part: LFM to 255. This 7-Core
3055    Ratio Limit Must be Less than or equal to
1-Core Ratio Limit.Range is 0 to 255
3056    0x0:0xFF
3057    */
3058    UINT8
      SevenCoreRatioLimit;
3059
3060    /** Offset 0x089D - 8-Core Ratio Limit
3061    8-Core Ratio Limit: LFM to Fused, For
      overclocking part: LFM to 255. This 8-Core
3062    Ratio Limit Must be Less than or equal to
1-Core Ratio Limit.Range is 0 to 255
3063    0x0:0xFF
3064    */
3065    UINT8
      EightCoreRatioLimit;
```

```
3066
3067 /** Offset 0x089E - Intel Turbo Boost Max
Technology 3.0
3068 Intel Turbo Boost Max Technology 3.0. 0:
Disabled; <b>1: Enabled</b>
3069 $EN_DIS
3070 */
3071     UINT8           EnableItbm;
3072
3073 /** Offset 0x089F - Intel Turbo Boost Max
Technology 3.0 Driver
3074 Intel Turbo Boost Max Technology 3.0
Driver <b>0: Disabled</b>; 1: Enabled
3075 $EN_DIS
3076 */
3077     UINT8           EnableItbmDriver;
3078
3079 /** Offset 0x08A0 - Enable or Disable C1
Cstate Demotion
3080 Enable or Disable C1 Cstate Demotion.
Disable; <b>1: Enable</b>
3081 $EN_DIS
3082 */
3083     UINT8           C1StateAutoDemotion;
3084
3085 /** Offset 0x08A1 - Enable or Disable C1
Cstate UnDemotion
3086 Enable or Disable C1 Cstate UnDemotion.
Disable; <b>1: Enable</b>
3087 $EN_DIS
3088 */
3089     UINT8           C1StateUndemotion;
3090
3091 /** Offset 0x08A2 - CpuWakeUpTimer
```

```
3092    Enable long CPU Wakeup Timer. When
      enabled, the cpu internal wakeup time is
      increased
3093    to 180 seconds. 0: Disable; <b>1:</b>
      Enable</b>
3094    $EN_DIS
3095  */
3096    UINT8
      CpuWakeUpTimer;
3097
3098 /** Offset 0x08A3 - Minimum Ring ratio limit
      override
3099    Minimum Ring ratio limit override. <b>0:</b>
      Hardware defaults.</b> Range: 0 - Max turbo
3100    ratio limit
3101  */
3102    UINT8
      MinRingRatioLimit;
3103
3104 /** Offset 0x08A4 - Minimum Ring ratio limit
      override
3105    Maximum Ring ratio limit override. <b>0:</b>
      Hardware defaults.</b> Range: 0 - Max turbo
3106    ratio limit
3107  */
3108    UINT8
      MaxRingRatioLimit;
3109
3110 /** Offset 0x08A5 - Enable or Disable C3
      Cstate Demotion
3111    Enable or Disable C3 Cstate Demotion.
      Disable; <b>1:</b> Enable</b>
3112    $EN_DIS
3113  */
3114    UINT8
      C3StateAutoDemotion;
3115
```

```
3116 /** Offset 0x08A6 - Enable or Disable C3
Cstate UnDemotion
3117   Enable or Disable C3 Cstate UnDemotion.
Disable; <b>1: Enable</b>
3118   $EN_DIS
3119 */
3120   UINT8
3121     C3StateUnDemotion;
3122
3123 /** Offset 0x08A7 - ReservedCpuPostMemTest
3124   Reserved for CPU Post-Mem Test
3125   $EN_DIS
3126 */
3127   UINT8
3128   ReservedCpuPostMemTest[19];
3129
3130 /** Offset 0x08BA - SgxSinitDataFromTpm
3131   SgxSinitDataFromTpm default values
3132 */
3133   UINT8
3134   SgxSinitDataFromTpm;
3135
3136 /** Offset 0x08BB - End of Post message
3137   Test, Send End of Post message.
Disable(0x0): Disable EOP message, Send in
PEI(0x1):
3138   EOP send in PEI, Send in DXE(0x2)
(Default): EOP send in PEI
3139   0:Disable, 1:Send in PEI, 2:Send in DXE,
3:Reserved
3140 */
3141   UINT8
3142   EndOfPostMessage;
3143
3144 /** Offset 0x08BC - DOI3 Setting for HECI
3145   Disable
3146   Test, 0: disable, 1: enable, Setting this
```

```
        option disables setting D0I3 bit for all
3142    $EN_DIS
3143    */
3144    */
3145    UINT8
        DisableD0I3SettingForHeci;
3146
3147 /** Offset 0x08BD - HD Audio Reset Wait
3148   Timer
3149   The delay timer after Azalia reset, the
3150   value is number of microseconds. Default is
3151   600.
3152 */
3153   UINT16
        PchHdaResetWaitTimer;
3154
3155 /** Offset 0x08BF - Enable LOCKDOWN SMI
3156   Enable SMI_LOCK bit to prevent writes to
3157   the Global SMI Enable bit.
3158 $EN_DIS
3159 */
3160   UINT8
        PchLockDownGlobalSmi;
3161
3162 */
3163   UINT8
        PchLockDownBiosInterface;
3164
3165 /** Offset 0x08C1 - Unlock all GPIO pads
3166   Force all GPIO pads to be unlocked for
3167   debug purpose.
3168 $EN_DIS
```

```
3167  */
3168  UINT8
3169  PchUnlockGpioPads;
3170 /**
3171  ** Offset 0x08C2 - PCH Unlock SBI access
3172  Deprecated
3173  $EN_DIS
3174  */
3175  UINT8 PchSbiUnlock;
3176 /**
3177  ** Offset 0x08C3 - PCH Unlock SideBand
3178  access
3179  The SideBand PortID mask for certain end
3180  point (e.g. PSFx) will be locked before
3181  3rd party code execution. 0: Lock SideBand
3182  access; 1: Unlock SideBand access.
3183  $EN_DIS
3184  */
3185  UINT8
3186  PchSbAccessUnlock;
3187 /**
3188  ** Offset 0x08C4 - PCIE RP Ltr Max Snoop
3189  Latency
3190  Latency Tolerance Reporting, Max Snoop
3191  Latency.
3192  */
3193  /**
3194  ** Offset 0x08F4 - PCIE RP Ltr Max No Snoop
3195  Latency
3196  Latency Tolerance Reporting, Max Non-Snoop
3197  Latency.
3198  */
3199  /**
3200  ** Offset 0x08F5 - PCIE RP Ltr Max No Snoop
3201  Latency
3202  Latency Tolerance Reporting, Max Non-Snoop
3203  Latency.
3204  */
3205  /**
3206  ** Offset 0x08F6 - PCIE RP Ltr Max No Snoop
3207  Latency
3208  Latency Tolerance Reporting, Max Non-Snoop
3209  Latency.
3210  */
3211  /**
3212  ** Offset 0x08F7 - PCIE RP Ltr Max No Snoop
3213  Latency
3214  Latency Tolerance Reporting, Max Non-Snoop
3215  Latency.
3216  */
3217  /**
3218  ** Offset 0x08F8 - PCIE RP Ltr Max No Snoop
3219  Latency
3220  Latency Tolerance Reporting, Max Non-Snoop
3221  Latency.
3222  */
3223  /**
3224  ** Offset 0x08F9 - PCIE RP Ltr Max No Snoop
3225  Latency
3226  Latency Tolerance Reporting, Max Non-Snoop
3227  Latency.
3228  */
3229  /**
3230  ** Offset 0x08FA - PCIE RP Ltr Max No Snoop
3231  Latency
3232  Latency Tolerance Reporting, Max Non-Snoop
3233  Latency.
3234  */
3235  /**
3236  ** Offset 0x08FB - PCIE RP Ltr Max No Snoop
3237  Latency
3238  Latency Tolerance Reporting, Max Non-Snoop
3239  Latency.
3240  */
3241  /**
3242  ** Offset 0x08FC - PCIE RP Ltr Max No Snoop
3243  Latency
3244  Latency Tolerance Reporting, Max Non-Snoop
3245  Latency.
3246  */
3247  /**
3248  ** Offset 0x08FD - PCIE RP Ltr Max No Snoop
3249  Latency
3250  Latency Tolerance Reporting, Max Non-Snoop
3251  Latency.
3252  */
3253  /**
3254  ** Offset 0x08FE - PCIE RP Ltr Max No Snoop
3255  Latency
3256  Latency Tolerance Reporting, Max Non-Snoop
3257  Latency.
3258  */
3259  /**
3260  ** Offset 0x08FF - PCIE RP Ltr Max No Snoop
3261  Latency
3262  Latency Tolerance Reporting, Max Non-Snoop
3263  Latency.
```

```
3193 /** Offset 0x0924 - PCIE RP Snoop Latency
Override Mode
3194   Latency Tolerance Reporting, Snoop Latency
Override Mode.
3195 */
3196   UINT8
PcieRpSnoopLatencyOverrideMode[24];
3197
3198 /** Offset 0x093C - PCIE RP Snoop Latency
Override Multiplier
3199   Latency Tolerance Reporting, Snoop Latency
Override Multiplier.
3200 */
3201   UINT8
PcieRpSnoopLatencyOverrideMultiplier[24];
3202
3203 /** Offset 0x0954 - PCIE RP Snoop Latency
Override Value
3204   Latency Tolerance Reporting, Snoop Latency
Override Value.
3205 */
3206   UINT16
PcieRpSnoopLatencyOverrideValue[24];
3207
3208 /** Offset 0x0984 - PCIE RP Non Snoop
Latency Override Mode
3209   Latency Tolerance Reporting, Non-Snoop
Latency Override Mode.
3210 */
3211   UINT8
PcieRpNonSnoopLatencyOverrideMode[24];
3212
3213 /** Offset 0x099C - PCIE RP Non Snoop
Latency Override Multiplier
3214   Latency Tolerance Reporting, Non-Snoop
Latency Override Multiplier.
3215 */
```

```
3216 |     UINT8
      |     PcieRpNonSnoopLatencyOverrideMultiplier[24];
3217 |
3218 | /** Offset 0x09B4 - PCIE RP Non Snoop
      | Latency Override Value
3219 |     Latency Tolerance Reporting, Non-Snoop
      |     Latency Override Value.
3220 | */
3221 |     UINT16
      |     PcieRpNonSnoopLatencyOverrideValue[24];
3222 |
3223 | /** Offset 0x09E4 - PCIE RP Slot Power Limit
      | Scale
3224 |     Specifies scale used for slot power limit
      | value. Leave as 0 to set to default.
3225 | */
3226 |     UINT8
      |     PcieRpSlotPowerLimitScale[24];
3227 |
3228 | /** Offset 0x09FC - PCIE RP Slot Power Limit
      | Value
3229 |     Specifies upper limit on power supply by
      | slot. Leave as 0 to set to default.
3230 | */
3231 |     UINT16
      |     PcieRpSlotPowerLimitValue[24];
3232 |
3233 | /** Offset 0x0A2C - PCIE RP Upstream Port
      | Transmiter Preset
3234 |     Used during Gen3 Link Equalization. Used
      | for all lanes. Default is 5.
3235 | */
3236 |     UINT8
      |     PcieRpUptp[24];
3237 |
3238 | /** Offset 0x0A44 - PCIE RP Downstream Port
      | Transmiter Preset
```

```
3239    Used during Gen3 Link Equalization. Used
        for all lanes. Default is 7.
3240 */
3241     UINT8
3242         PcieRpDptp[24];
3243 /**
3244     ** Offset 0xA5C - PCIE RP Enable Port8xh
3245     Decode
3246     This member describes whether PCIE root
3247     port Port 8xh Decode is enabled. 0: Disable;
3248     1: Enable.
3249     $EN_DIS
3250 */
3251     UINT8
3252         PcieEnablePort8xhDecode;
3253 /**
3254     ** Offset 0xA5D - PCIE Port8xh Decode Port
3255     Index
3256     The Index of PCIe Port that is selected
3257     for Port8xh Decode (0 Based).
3258 */
3259     UINT8
3260         PchPciePort8xhDecodePortIndex;
3261 /**
3262     ** Offset 0xA5E - PCH Energy Reporting
3263     Disable/Enable PCH to CPU energy report
3264     feature.
3265     $EN_DIS
3266 */
3267     UINT8
3268         PchPmDisableEnergyReport;
3269 /**
3270     ** Offset 0xA5F - PCH Sata Test Mode
3271     Allow entrance to the PCH SATA test modes.
3272     $EN_DIS
3273 */
3274     UINT8
3275         SataTestMode;
```

```
3266
3267 /** Offset 0xA60 - PCH USB OverCurrent
   mapping lock enable
3268   If this policy option is enabled then BIOS
   will program OCCFDONE bit in xHCI meaning
3269   that OC mapping data will be consumed by
   xHCI and OC mapping registers will be locked.
3270   $EN_DIS
3271 */
3272   UINT8                               PchXhciOcLock;
3273
3274 /** Offset 0xA61
3275 */
3276   UINT8
   UnusedUpdSpace24[17];
3277
3278 /** Offset 0xA72 - Skip POSTBOOT SAI
   Deprecated
   $EN_DIS
3279 */
3280   UINT8
   SkipPostBootSai;
3281
3282 /** Offset 0xA73 - Mctp Broadcast Cycle
   Test, Determine if MCTP Broadcast is
   enabled <b>0: Disable</b>; 1: Enable.
3283   $EN_DIS
3284 */
3285   UINT8
   MctpBroadcastCycle;
3286
3287 /**
3288   UINT8
   ReservedFspsTestUpd[12];
3289
3290 /** Offset 0xA74
3291 */
3292   UINT8
   ReservedFspsTestUpd[12];
3293 } FSP_S_TEST_CONFIG;
3294
```

```
3295 /** Fsp S UPD Configuration
3296 */
3297 typedef struct {
3298
3299 /** Offset 0x0000
3300 */
3301     FSP_UPD_HEADER           FspUpdHeader;
3302
3303 /** Offset 0x0020
3304 */
3305     FSP_S_CONFIG FspSConfig;
3306
3307 /** Offset 0x07AD
3308 */
3309     FSP_S_TEST_CONFIG FspSTestConfig;
3310
3311 /** Offset 0x0A80
3312 */
3313     UINT16                 UpdTerminator;
3314 } FSPPS_UPD;
3315
3316 #pragma pack()
3317
3318 #endif
```



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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## Graph Legend

This page explains how to interpret the graphs that are generated by doxygen.

Consider the following example:

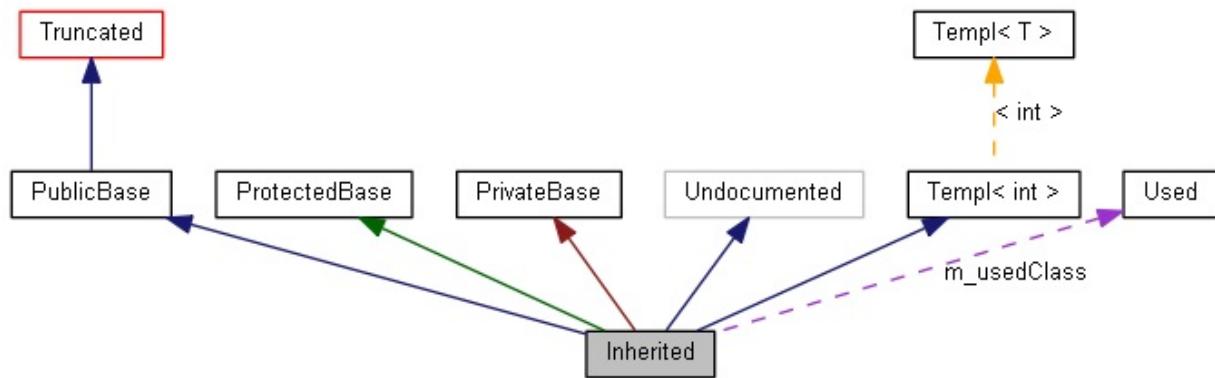
```
1  /*! Invisible class because of truncation */
2  class Invisible { };
3
4  /*! Truncated class, inheritance relation is
   hidden */
5  class Truncated : public Invisible { };
6
7  /* Class not documented with doxygen
   comments */
8  class Undocumented { };
9
10 /*! Class that is inherited using public
    inheritance */
11 class PublicBase : public Truncated { };
12
13 /*! A template class */
14 template<class T> class Templ { };
15
16 /*! Class that is inherited using protected
```

```

    inheritance */
17 class ProtectedBase { };
18
19 /*! Class that is inherited using private
   inheritance */
20 class PrivateBase { };
21
22 /*! Class that is used by the Inherited
   class */
23 class Used { };
24
25 /*! Super class that inherits a number of
   other classes */
26 class Inherited : public PublicBase,
27                     protected ProtectedBase,
28                     private PrivateBase,
29                     public Undocumented,
30                     public Templ<int>
31 {
32     private:
33     Used *m_usedClass;
34 }

```

This will result in the following graph:



The boxes in the above graph have the following meaning:

- A filled gray box represents the struct or class for which the graph

is generated.

- A box with a black border denotes a documented struct or class.
- A box with a gray border denotes an undocumented struct or class.
- A box with a red border denotes a documented struct or class for which not all inheritance/containment relations are shown. A graph is truncated if it does not fit within the specified boundaries.

The arrows have the following meaning:

- A dark blue arrow is used to visualize a public inheritance relation between two classes.
- A dark green arrow is used for protected inheritance.
- A dark red arrow is used for private inheritance.
- A purple dashed arrow is used if a class is contained or used by another class. The arrow is labeled with the variable(s) through which the pointed class or struct is accessible.
- A yellow dashed arrow denotes a relation between a template instance and the template class it was instantiated from. The arrow is labeled with the template parameters of the instance.



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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Class List	Class Index	Class Members	

## AZALIA\_HEADER Member List

This is the complete list of members for [AZALIA\\_HEADER](#), including all inherited members.

DataDwords	<a href="#">AZALIA_HEADER</a>
DeviceId	<a href="#">AZALIA_HEADER</a>
Reserved	<a href="#">AZALIA_HEADER</a>
RevisionId	<a href="#">AZALIA_HEADER</a>
SdiNum	<a href="#">AZALIA_HEADER</a>
VendorId	<a href="#">AZALIA_HEADER</a>

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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Class List	Class Index	Class Members	

## **CHIPSET\_INIT\_INFO Member List**

This is the complete list of members for **CHIPSET\_INIT\_INFO**, including all inherited members.

BiosChipInitCrc	<b>CHIPSET_INIT_INFO</b>
MeChipInitCrc	<b>CHIPSET_INIT_INFO</b>
Revision	<b>CHIPSET_INIT_INFO</b>
Rsvd	<b>CHIPSET_INIT_INFO</b>

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

Main Page

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Classes

Files

File List

File Members

Include >

## FspmUpd.h

Go to the documentation of this file.

```
1  /** @file
2
3  Copyright (c) 2018, Intel Corporation. All
4  rights reserved.<BR>
5
6  Redistribution and use in source and binary
7  forms, with or without modification,
8  are permitted provided that the following
9  conditions are met:
10
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19   other materials provided with the
20   distribution.
```

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26 COPYRIGHT OWNER OR CONTRIBUTORS BE
27 LIABLE FOR ANY DIRECT, INDIRECT,
28 INCIDENTAL, SPECIAL, EXEMPLARY, OR
29 CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT
30 LIMITED TO, PROCUREMENT OF
31 SUBSTITUTE GOODS OR SERVICES; LOSS OF USE,
32 DATA, OR PROFITS; OR BUSINESS
33 INTERRUPTION) HOWEVER CAUSED AND ON ANY
34 THEORY OF LIABILITY, WHETHER IN
35 CONTRACT, STRICT LIABILITY, OR TORT
36 (INCLUDING NEGLIGENCE OR OTHERWISE)
37 ARISING IN ANY WAY OUT OF THE USE OF THIS
38 SOFTWARE, EVEN IF ADVISED OF
39 THE POSSIBILITY OF SUCH DAMAGE.
40
41 This file is automatically generated.
42 Please do NOT modify !!!
43
44 */
45
46 #ifndef __FSPMUPD_H__
47 #define __FSPMUPD_H__
48
49
50 #include <FspUpd.h>
```

```
37
38 #pragma pack(1)
39
40
41 #include <MemInfoHob.h>
42
43 /**
44  /// The ChipsetInit Info structure provides
45  /// the information of ME ChipsetInit CRC and BIOS
46  /// ChipsetInit CRC.
47 /**
48  typedef struct {
49      UINT8             Revision;           ///<-
50      UINT8             Rsvd[3];           ///<-
51      Reserved
52      UINT16            MeChipInitCrc;    ///<-
53      16 bit CRC value of MeChipInit Table
54      UINT16            BiosChipInitCrc;  ///<-
55      16 bit CRC value of PchChipInit Table
56  } CHIPSET_INIT_INFO;
57
58 /**
59  ** Fsp M Configuration
60  */
61  typedef struct {
62      /** Offset 0x0040 - Platform Reserved Memory
63      Size
64      The minimum platform memory size required
65      to pass control into DXE
66      */
67      UINT64             PlatformMemorySize;
68
69      /** Offset 0x0048 - Memory SPD Pointer
70      Channel 0 Dimm 0
```

```
64 |     Pointer to SPD data, will be used only
|      when SpdAddressTable SPD Address are marked as
|      00
65 | */
66 |     UINT32
|     MemorySpdPtr00;
67 |
68 | /** Offset 0x004C - Memory SPD Pointer
|      Channel 0 Dimm 1
69 |     Pointer to SPD data, will be used only
|      when SpdAddressTable SPD Address are marked as
|      00
70 | */
71 |     UINT32
|     MemorySpdPtr01;
72 |
73 | /** Offset 0x0050 - Memory SPD Pointer
|      Channel 1 Dimm 0
74 |     Pointer to SPD data, will be used only
|      when SpdAddressTable SPD Address are marked as
|      00
75 | */
76 |     UINT32
|     MemorySpdPtr10;
77 |
78 | /** Offset 0x0054 - Memory SPD Pointer
|      Channel 1 Dimm 1
79 |     Pointer to SPD data, will be used only
|      when SpdAddressTable SPD Address are marked as
|      00
80 | */
81 |     UINT32
|     MemorySpdPtr11;
82 |
83 | /** Offset 0x0058 - SPD Data Length
|      Length of SPD Data
84 |      0x100:256 Bytes, 0x200:512 Bytes
```

```
86  */
87  UINT16
88  MemorySpdDataLen;
89 /**
90  ** Offset 0x005A - Dq Byte Map CH0
91  Dq byte mapping between CPU and DRAM,
92  Channel 0: board-dependent
93 /**
94  /**
95  ** Offset 0x0066 - Dq Byte Map CH1
96  Dq byte mapping between CPU and DRAM,
97  Channel 1: board-dependent
98 /**
99  /**
100 ** Offset 0x0072 - Dqs Map CPU to DRAM CH 0
101 Set Dqs mapping relationship between CPU
102 and DRAM, Channel 0: board-dependent
103 /**
104 /**
105 ** Offset 0x007A - Dqs Map CPU to DRAM CH 1
106 Set Dqs mapping relationship between CPU
107 and DRAM, Channel 1: board-dependent
108 /**
109 /**
110 ** Offset 0x0082 - RcompResister settings
111 Indicates RcompResister settings: CNL -
112 0's means MRC auto configured based on Design
113 Guidelines, otherwise input an Ohmic value
114 per segment. CFL will need to provide
```

```

112     the appropriate values.
113 */
114     UINT16
115     RcompResistor[3];
116 /**
117     RcompTarget settings: CNL - 0's mean MRC
118     auto configured based on Design Guidelines,
119     otherwise input an Ohmic value per
120     segment. CFL will need to provide the
121     appropriate values.
122 */
123     UINT16
124     RcompTarget[5];
125 /**
126     /** Offset 0x0092 - Dqs Pins Interleaved
127     Setting
128     Indicates DqPinsInterleaved setting:
129     board-dependent
130     $EN_DIS
131 */
132     UINT8
133     DqPinsInterleaved;
134 /**
135     /** Offset 0x0093 - VREF_CA
136     CA Vref routing: board-dependent
137     0:VREF_CA goes to both CH_A and CH_B, 1:
138     VREF_CA to CH_A and VREF_DQ_A to CH_B,
139     2:VREF_CA to CH_A and VREF_DQ_B to CH_B
140 */
141     UINT8
142     CaVrefConfig;
143 /**
144     /** Offset 0x0094 - Smram Mask
145     The SMM Regions AB-SEG and/or H-SEG
146     reserved
147     0: Neither, 1:AB-SEG, 2:H-SEG, 3: Both
148 */

```

```
139     UINT8                         SmramMask;
140
141 /** Offset 0x0095 - MRC Fast Boot
142    Enables/Disable the MRC fast path thru the
143    MRC
144    $EN_DIS
145    */
146    UINT8                         MrcFastBoot;
147
148 /** Offset 0x0096 - Rank Margin Tool per
149    Task
150    This option enables the user to execute
151    Rank Margin Tool per major training step
152    in the MRC.
153    $EN_DIS
154    */
155    UINT8                         RmtPerTask;
156
157 /** Offset 0x0097 - Training Trace
158    This option enables the trained state
159    tracing feature in MRC. This feature will
160    print out the key training parameters
161    state across major training steps.
162    $EN_DIS
163    */
164    UINT8                         TrainTrace;
165
166 /** Offset 0x0098 - Intel Enhanced Debug
167    Intel Enhanced Debug (IED): 0=Disabled,
168    0x400000=Enabled and 4MB SMRAM occupied
169    0 : Disable, 0x400000 : Enable
170    */
171    UINT32                        IedSize;
172
173 /** Offset 0x009C - Tseg Size
174    Size of SMRAM memory reserved. 0x400000
175    for Release build and 0x1000000 for Debug
```

```

    build
169     0x0400000:4MB, 0x01000000:16MB
170     */
171     UINT32                         TsegSize;
172
173     /** Offset 0x00A0 - MMIO Size
174      Size of MMIO space reserved for devices.
175      0(Default)=Auto, non-Zero=size in MB
176     */
177
178     /** Offset 0x00A2 - Probeless Trace
179      Probeless Trace: 0=Disabled, 1=Enable.
180      Enabling Probeless Trace will reserve 128MB.
181      This also requires IED to be enabled.
182      $EN_DIS
183     */
184
185     /** Offset 0x00A3 - GDXC IOT SIZE
186      Size of IOT and MOT is in 8 MB chunks
187     */
188     UINT8                           GdxcIotSize;
189
190     /** Offset 0x00A4 - GDXC MOT SIZE
191      Size of IOT and MOT is in 8 MB chunks
192     */
193     UINT8                           GdxcMotSize;
194
195     /** Offset 0x00A5 - Enable SMBus
196      Enable/disable SMBus controller.
197      $EN_DIS
198     */
199     UINT8                           SmbusEnable;
200
201     /** Offset 0x00A6 - Spd Address Tabl

```

```
202     Specify SPD Address table for  
203     CH0D0/CH0D1/CH1D0&CH1D1. MemorySpdPtr will be  
204     used  
205     if SPD Address is 00  
206     **/  
207     UINT8  
208     SpdAddressTable[4];  
209     /** Offset 0x00AA - Platform Debug Consent  
210     To 'opt-in' for debug, please select  
211     'Enabled' with the desired debug probe type.  
212     Enabling this BIOS option may alter the  
213     default value of other debug-related BIOS  
214     options. Note: DCI OOB (aka BSSB) uses CCA  
215     probe; [DCI OOB+DbC] and [USB2 DbC]  
216     have the same setting  
217     0:Disabled, 1:Enabled (DCI OOB+[DbC]),  
218     2:Enabled (DCI OOB), 3:Enabled (USB3 DbC),  
219     4:Enabled (XDP/MIPI60), 5:Enabled (USB2  
220     DbC)  
221     **/  
222     UINT8  
223     PlatformDebugConsent;  
224     /** Offset 0x00AB - USB3 Type-C UFP2DFP  
225     Kernel/Platform Debug Support  
226     This BIOS option enables kernel and  
227     platform debug for USB3 interface over a UFP  
228     Type-C receptacle, select 'No Change' will  
229     do nothing to UFP2DFP setting.  
230     0:Disabled, 1:Enabled, 2>No Change  
231     **/  
232     UINT8  
233     DciUsb3TypecUfpDbg;  
234     /** Offset 0x00AC - PCH Trace Hub Mode  
235     Select 'Host Debugger' if Trace Hub is
```

```
    used with host debugger tool or 'Target
    Debugger'
226|    if Trace Hub is used by target debugger
    software or 'Disable' trace hub functionality.
227|    0: Disable, 1: Target Debugger Mode, 2:
    Host Debugger Mode
228| /**
229|     UINT8
    PchTraceHubMode;
230|
231| /** Offset 0x00AD - PCH Trace Hub Memory
    Region 0 buffer Size
232|     Specify size of Pch trace memory region 0
    buffer, the size can be 0, 1MB, 8MB, 64MB,
233|     128MB, 256MB, 512MB. Note : Limitation of
    total buffer size (PCH + CPU) is 512MB.
234|     0:0, 1:1MB, 2:8MB, 3:64MB, 4:128MB,
    5:256MB, 6:512MB
235| /**
236|     UINT8
    PchTraceHubMemReg0Size;
237|
238| /** Offset 0x00AE - PCH Trace Hub Memory
    Region 1 buffer Size
239|     Specify size of Pch trace memory region 1
    buffer, the size can be 0, 1MB, 8MB, 64MB,
240|     128MB, 256MB, 512MB. Note : Limitation of
    total buffer size (PCH + CPU) is 512MB.
241|     0:0, 1:1MB, 2:8MB, 3:64MB, 4:128MB,
    5:256MB, 6:512MB
242| /**
243|     UINT8
    PchTraceHubMemReg1Size;
244|
245| /** Offset 0x00AF - PchPreMemRsvd
246|     Reserved for PCH Pre-Mem Reserved
247|     $EN_DIS
```

```
248  */
249  UINT8
PchPreMemRsvd[9];
250
251 /** Offset 0x00B8 - Internal Graphics Pre-
allocated Memory
252   Size of memory preallocated for internal
graphics.
253   0x00:0 MB, 0x01:32 MB, 0x02:64 MB
254 */
255  UINT8
IgdDvmt50PreAlloc;
256
257 /** Offset 0x00B9 - Internal Graphics
258   Enable/disable internal graphics.
259   $EN_DIS
260 */
261  UINT8           InternalGfx;
262
263 /** Offset 0x00BA - Aperture Size
264   Select the Aperture Size.
265   0:128 MB, 1:256 MB, 2:512 MB
266 */
267  UINT8           ApertureSize;
268
269 /** Offset 0x00BB - Board Type
270   MrcBoardType, Options are 0=Mobile/Mobile
Halo, 1=Desktop/DT Halo, 5=ULT/ULX/Mobile
271   Halo, 7=UP Server
272   0:Mobile/Mobile Halo, 1:Desktop/DT Halo,
5:ULT/ULX/Mobile Halo, 7:UP Server
273 */
274  UINT8           UserBd;
275
276 /** Offset 0x00BC - SA GV
277   System Agent dynamic frequency support and
when enabled memory will be training
```

```

278    at two different frequencies. Only effects
279    ULX/ULT CPUs. 0=Disabled, 1=FixedLow,
280    2=FixedHigh, and 3=Enabled.
281    0:Disabled, 1:FixedLow, 2:FixedHigh,
282    3:Enabled
283    */
284    UINT8                                SaGv;
285
286    /** Offset 0x00BD
287    */
288    UINT8
289    UnusedUpdSpace0;
290
291    /** Offset 0x00BE - DDR Frequency Limit
292    Maximum Memory Frequency Selections in
293    Mhz. Valid values should match the refclk,
294    i.e. divide by 133 or 100
295    1067:1067, 1333:1333, 1400:1400,
296    1600:1600, 1800:1800, 1867:1867, 2000:2000,
297    2133:2133,
298    2200:2200, 2400:2400, 2600:2600,
299    2667:2667, 2800:2800, 2933:2933, 3000:3000,
300    3200:3200, 0:Auto
301    */
302    UINT16                                DdrFreqLimit;
303
304    /** Offset 0x00C0 - Low Frequency
305    SAGV Low Frequency Selections in Mhz.
306    Options are 1067, 1333, 1600, 1867, 2133,
307    2400, 2667, 2933 and 0 for Auto.
308    1067:1067, 1333:1333, 1600:1600,
309    1867:1867, 2133:2133, 2400:2400, 2667:2667,
310    2933:2933, 0:Auto
311    */
312    UINT16                                FreqSaGvLow;
313
314    /** Offset 0x00C2 - Mid Frequency

```

```
304     SAGV Mid Frequency Selections in Mhz.  
305     Options are 1067, 1333, 1600, 1867, 2133,  
306     2400, 2667, 2933 and 0 for Auto.  
307     1067:1067, 1333:1333, 1600:1600,  
308     1867:1867, 2133:2133, 2400:2400, 2667:2667,  
309     2933:2933, 0:Auto  
310     /**/  
311     UINT16                                FreqSaGvMid;  
312  
313     /** Offset 0x00C4 - Rank Margin Tool  
314     Enable/disable Rank Margin Tool.  
315     $EN_DIS  
316     */  
317     UINT8                                 RMT;  
318  
319     /** Offset 0x00C5 - Channel A DIMM Control  
320     Channel A DIMM Control Support - Enable or  
321     Disable Dimms on Channel A.  
322     0:Enable both DIMMs, 1:Disable DIMM0,  
323     2:Disable DIMM1, 3:Disable both DIMMs  
324     */  
325     UINT8  
326     DisableDimmChannel0;  
327  
328     /** Offset 0x00C6 - Channel B DIMM Control  
329     Channel B DIMM Control Support - Enable or  
330     Disable Dimms on Channel B.  
331     0:Enable both DIMMs, 1:Disable DIMM0,  
332     2:Disable DIMM1, 3:Disable both DIMMs  
333     */  
334     UINT8  
335     DisableDimmChannel1;  
336  
337     /** Offset 0x00C7 - Scrambler Support  
338     This option enables data scrambling in  
339     memory.  
340     $EN_DIS
```

```
331  */
332  UINT8
333  ScramblerSupport;
334  /** Offset 0x00C8 - Skip Multi-Processor
335  Initialization
336  When this is skipped, boot loader must
337  initialize processors before SilicionInit
338  API. </b>0: Initialize; <b>1: Skip
339  $EN_DIS
340  */
341  /** Offset 0x00C9
342  */
343  UINT8
344  UnusedUpdSpace1[15];
345  /** Offset 0x00D8 - SPD Profile Selected
346  Select DIMM timing profile. Options are
347  0=Default profile, 1=Custom profile, 2=XMP
348  Profile 1, 3=XMP Profile 2
349  0:Default profile, 1:Custom profile, 2:XMP
350  profile 1, 3:XMP profile 2
351  */
352  /** Offset 0x00D9 - Memory Reference Clock
353  100MHz, 133MHz.
354  0:133MHz, 1:100MHz
355  */
356  UINT8
357  RefClk;
358  /** Offset 0x00DA - Memory Voltage
359  Memory Voltage Override (Vddq). Default =
no override
```

```

360    0:Default, 1200:1.20 Volts, 1250:1.25
      Volts, 1300:1.30 Volts, 1350:1.35 Volts,
      1400:1.40
361    Volts, 1450:1.45 Volts, 1500:1.50 Volts,
      1550:1.55 Volts, 1600:1.60 Volts, 1650:1.65
      Volts
362    */
363    UINT16                                VddVoltage;
364
365    /** Offset 0x00DC - Memory Ratio
366     Automatic or the frequency will equal
     ratio times reference clock. Set to Auto to
367     recalculate memory timings listed below.
368     0:Auto, 4:4, 5:5, 6:6, 7:7, 8:8, 9:9,
     10:10, 11:11, 12:12, 13:13, 14:14, 15:15
369    */
370    UINT8                                Ratio;
371
372    /** Offset 0x00DD - QCLK Odd Ratio
373     Adds 133 or 100 MHz to QCLK frequency,
     depending on RefClk
374     $EN_DIS
375    */
376    UINT8                                OddRatioMode;
377
378    /** Offset 0x00DE - tCL
379     CAS Latency, 0: AUTO, max: 31
380    */
381    UINT8                                tCL;
382
383    /** Offset 0x00DF - tCWL
384     Min CAS Write Latency Delay Time, 0: AUTO,
     max: 34
385    */
386    UINT8                                tCWL;
387
388    /** Offset 0x00E0 - tRCD/tRP

```

```
389     RAS to CAS delay time and Row Precharge  
     delay time, 0: AUTO, max: 63  
390     **/  
391     UINT8                      tRCDtRP;  
392  
393     /** Offset 0x00E1 - tRRD  
394         Min Row Active to Row Active Delay Time,  
         0: AUTO, max: 15  
395     **/  
396     UINT8                      tRRD;  
397  
398     /** Offset 0x00E2 - tFAW  
399         Min Four Activate Window Delay Time, 0:  
         AUTO, max: 63  
400     **/  
401     UINT16                     tFAW;  
402  
403     /** Offset 0x00E4 - tRAS  
404         RAS Active Time, 0: AUTO, max: 64  
405     **/  
406     UINT16                     tRAS;  
407  
408     /** Offset 0x00E6 - tREFI  
409         Refresh Interval, 0: AUTO, max: 65535  
410     **/  
411     UINT16                     tREFI;  
412  
413     /** Offset 0x00E8 - tRFC  
414         Min Refresh Recovery Delay Time, 0: AUTO,  
         max: 1023  
415     **/  
416     UINT16                     tRFC;  
417  
418     /** Offset 0x00EA - tRTP  
419         Min Internal Read to Precharge Command  
         Delay Time, 0: AUTO, max: 15. DDR4 legal  
420         values: 5, 6, 7, 8, 9, 10, 12
```

```
421  */
422  UINT8 tRTP;
423
424 /** Offset 0x00EB - tWR
425   Min Write Recovery Time, 0: AUTO, legal
426   values: 5, 6, 7, 8, 10, 12, 14, 16, 18,
427   20, 24, 30, 34, 40
428   0:Auto, 5:5, 6:6, 7:7, 8:8, 10:10, 12:12,
429   14:14, 16:16, 18:18, 20:20, 24:24, 30:30,
430   34:34, 40:40
431 /**
432  */
433  UINT8 tWR;
434
435 /**
436  */
437  /** Offset 0x00EC - tWTR
438   Min Internal Write to Read Command Delay
439   Time, 0: AUTO, max: 28
440 /**
441  */
442  /** Offset 0x00ED - NMode
443   System command rate, range 0-2, 0 means
444   auto, 1 = 1N, 2 = 2N
445 /**
446  */
447  /** Offset 0x00EE - DllBwEn[0]
448   DllBwEn[0], for 1067 (0..7)
449 /**
450  */
451  /** Offset 0x00EF - DllBwEn[1]
452   DllBwEn[1], for 1333 (0..7)
453 /**
454  */
455  /** Offset 0x00F0 - DllBwEn[2]
456   DllBwEn[2], for 1600 (0..7)
```

```
454    */
455    UINT8           DllBwEn2;
456
457 /** Offset 0x00F1 - DllBwEn[3]
458   DllBwEn[3], for 1867 and up (0..7)
459 */
460    UINT8           DllBwEn3;
461
462 /** Offset 0x00F2 - ISVT IO Port Address
463   ISVT IO Port Address. 0=Minimal,
464   0xFF=Maximum, 0x99=Default
465 */
466    UINT8           IsvtIoPort;
467
468 /** Offset 0x00F3 - CPU Trace Hub Mode
469   Select 'Target Debugger' if Trace Hub is
470   used by target debugger software or 'Disable'
471   trace hub functionality.
472   0: Disable, 1:Target Debugger Mode
473 */
474    UINT8
475      CpuTraceHubMode;
476
477 /** Offset 0x00F4 - CPU Trace Hub Memory
478   Region 0
479   CPU Trace Hub Memory Region 0, The
480   available memory size is : 0MB, 1MB, 8MB,
481   64MB,
```

```
    Region 1
482|    CPU Trace Hub Memory Region 1. The
483|    available memory size is : 0MB, 1MB, 8MB,
484|    64MB,
485|    128MB, 256MB, 512MB. Note : Limitation of
486|    total buffer size (CPU + PCH) is 512MB.
487|    0:0, 1:1MB, 2:8MB, 3:64MB, 4:128MB,
488|    5:256MB, 6:512MB
489|    */
490|    UINT8
491|    CpuTraceHubMemReg1Size;
492|
493|    /**
494|    ** Offset 0x00F6 - Enable or Disable Peci
495|    C10 Reset command
496|    Enable or Disable Peci C10 Reset command.
497|    If Enabled, BIOS will send the CPU message
498|    to disable peci reset on C10 exit. The
499|    default value is <b>0: Disable</b> for CNL,
500|    and <b>1: Enable</b> for all other CPU's
501|    $EN_DIS
502|    */
503|    UINT8
504|    PeciC10Reset;
505|
506|    /**
507|    ** Offset 0x00F7 - Enable or Disable Peci
508|    Sx Reset command
509|    Enable or Disable Peci Sx Reset command;
510|    <b>0: Disable;</b> 1: Enable.
511|    $EN_DIS
512|    */
513|    UINT8
514|    PeciSxReset;
515|
516|    /**
517|    ** Offset 0x00F8
518|    */
519|    UnusedUpdSpace2[4];
520|
521|    /**
522|    ** Offset 0x00FC - Enable Intel HD Audio
```

```
        (Azalia)
507    0: Disable, 1: Enable (Default) Azalia
      controller
508    $EN_DIS
509    */
510    UINT8                                PchHdaEnable;
511
512 /** Offset 0x00FD - Enable PCH ISH
      Controller
513 0: Disable, 1: Enable (Default) ISH
      Controller
514  $EN_DIS
515  */
516  UINT8                                PchIshEnable;
517
518 /** Offset 0x00FE - HECL Timeouts
519 0: Disable, 1: Enable (Default) timeout
      check for HECL
520  $EN_DIS
521  */
522  UINT8                                HeciTimeouts;
523
524 /** Offset 0x00FF
525 */
526  UINT8
      UnusedUpdSpace3;
527
528 /** Offset 0x0100 - HECL1 BAR address
      BAR address of HECL1
529 */
530  UINT32
      Heci1BarAddress;
531
532 /** Offset 0x0104 - HECL2 BAR address
      BAR address of HECL2
533 */
534  UINT32
```

```
        Heci2BarAddress;
537     /** Offset 0x0108 - HECI3 BAR address
539         BAR address of HECI3
540     **/
541     UINT32
      Heci3BarAddress;
542
543     /** Offset 0x010C - SG dGPU Power Delay
544         SG dGPU delay interval after power
545         enabling: 0=Minimal, 1000=Maximum, default is
546         300=300 microseconds
547     **/
548     UINT16
      SgDelayAfterPwrEn;
549
550     /** Offset 0x010E - SG dGPU Reset Delay
551         SG dGPU delay interval for Reset complete:
552         0=Minimal, 1000=Maximum, default is 100=100
553         microseconds
554     **/
555     UINT16
      SgDelayAfterHoldReset;
556
557     /** Offset 0x0110 - MMIO size adjustment for
558         AUTO mode
559         Positive number means increasing MMIO
560         size, Negative value means decreasing MMIO
561         size: 0 (Default)=no change to AUTO mode
562         MMIO size
563     **/
564     UINT16
      MmioSizeAdjustment;
565
566     /** Offset 0x0112 - Enable/Disable DMI GEN3
567         Static EQ Phase1 programming
568         Program DMI Gen3 EQ Phase1 Static Presets.
```

```
        Disabled(0x0): Disable EQ Phase1 Static
563    Presets Programming, Enabled(0x1)
        (Default): Enable EQ Phase1 Static Presets
        Programming
564    $EN_DIS
565    */
566    UINT8
        DmiGen3ProgramStaticEq;
567
568    /** Offset 0x0113 - Enable/Disable PEG 0
569    Disabled(0x0): Disable PEG Port,
        Enabled(0x1): Enable PEG Port (If Silicon SKU
        permits
570    it), Auto(0x2)(Default): If an endpoint is
        present, enable the PEG Port, Disable
        otherwise
571    0:Disable, 1:Enable, 2:AUTO
572    */
573    UINT8                                Peg0Enable;
574
575    /** Offset 0x0114 - Enable/Disable PEG 1
576    Disabled(0x0): Disable PEG Port,
        Enabled(0x1): Enable PEG Port (If Silicon SKU
        permits
577    it), Auto(0x2)(Default): If an endpoint is
        present, enable the PEG Port, Disable
        otherwise
578    0:Disable, 1:Enable, 2:AUTO
579    */
580    UINT8                                Peg1Enable;
581
582    /** Offset 0x0115 - Enable/Disable PEG 2
583    Disabled(0x0): Disable PEG Port,
        Enabled(0x1): Enable PEG Port (If Silicon SKU
        permits
584    it), Auto(0x2)(Default): If an endpoint is
        present, enable the PEG Port, Disable
```

```
        otherwise
585         0:Disable, 1:Enable, 2:AUTO
586     */
587     UINT8                         Peg2Enable;
588
589 /** Offset 0x0116 - Enable/Disable PEG 3
590     Disabled(0x0): Disable PEG Port,
591     Enabled(0x1): Enable PEG Port (If Silicon SKU
592     permits
593     it), Auto(0x2)(Default): If an endpoint is
594     present, enable the PEG Port, Disable
595     otherwise
596     0:Disable, 1:Enable, 2:AUTO
597 */
598     UINT8                         Peg3Enable;
599
600 /**
601     UINT8
602     Peg0MaxLinkSpeed;
603
604 /**
605     UINT8
606     Peg1MaxLinkSpeed;
607
608 /**
609     UINT8
610     Peg2MaxLinkSpeed;
```

```
611     Auto (Default)(0x0): Maximum possible link
       speed, Gen1(0x1): Limit Link to Gen1
612     Speed, Gen2(0x2): Limit Link to Gen2
       Speed, Gen3(0x3):Limit Link to Gen3 Speed
613     0:Auto, 1:Gen1, 2:Gen2, 3:Gen3
614   */
615   UINT8
616
617   /** Offset 0x011A - PEG 3 Max Link Speed
618     Auto (Default)(0x0): Maximum possible link
       speed, Gen1(0x1): Limit Link to Gen1
619     Speed, Gen2(0x2): Limit Link to Gen2
       Speed, Gen3(0x3):Limit Link to Gen3 Speed
620     0:Auto, 1:Gen1, 2:Gen2, 3:Gen3
621   */
622   UINT8
623
624   /** Offset 0x011B - PEG 0 Max Link Width
625     Auto (Default)(0x0): Maximum possible link
       width, (0x1): Limit Link to x1, (0x2):
626     Limit Link to x2, (0x3):Limit Link to x4,
       (0x4): Limit Link to x8
627     0:Auto, 1:x1, 2:x2, 3:x4, 4:x8
628   */
629   UINT8
630
631   /** Offset 0x011C - PEG 1 Max Link Width
632     Auto (Default)(0x0): Maximum possible link
       width, (0x1): Limit Link to x1, (0x2):
633     Limit Link to x2, (0x3):Limit Link to x4
634     0:Auto, 1:x1, 2:x2, 3:x4
635   */
636   UINT8
637
638   Peg2MaxLinkSpeed;
639
640   Peg3MaxLinkSpeed;
641
642   Peg0MaxLinkWidth;
643
644   Peg1MaxLinkWidth;
```

```
637
638 /** Offset 0x011D - PEG 2 Max Link Width
639   Auto (Default)(0x0): Maximum possible link
   width, (0x1): Limit Link to x1, (0x2):
640   Limit Link to x2
641   0:Auto, 1:x1, 2:x2
642 */
643   UINT8
   Peg2MaxLinkWidth;
644
645 /** Offset 0x011E - PEG 3 Max Link Width
646   Auto (Default)(0x0): Maximum possible link
   width, (0x1): Limit Link to x1, (0x2):
647   Limit Link to x2
648   0:Auto, 1:x1, 2:x2
649 */
650   UINT8
   Peg3MaxLinkWidth;
651
652 /** Offset 0x011F - Power down unused lanes
   on PEG 0
653   (0x0): Do not power down any lane, (0x1):
   Bios will power down unused lanes based
654   on the max possible link width
655   0:No power saving, 1:Auto
656 */
657   UINT8
   Peg0PowerDownUnusedLanes;
658
659 /** Offset 0x0120 - Power down unused lanes
   on PEG 1
660   (0x0): Do not power down any lane, (0x1):
   Bios will power down unused lanes based
661   on the max possible link width
662   0:No power saving, 1:Auto
663 */
664   UINT8
```

```
    Peg1PowerDownUnusedLanes;
665
666 /** Offset 0x0121 - Power down unused lanes
   on PEG 2
667   (0x0): Do not power down any lane, (0x1):
   Bios will power down unused lanes based
668   on the max possible link width
669   0:No power saving, 1:Auto
670 */
671     UINT8
   Peg2PowerDownUnusedLanes;
672
673 /** Offset 0x0122 - Power down unused lanes
   on PEG 3
674   (0x0): Do not power down any lane, (0x1):
   Bios will power down unused lanes based
675   on the max possible link width
676   0:No power saving, 1:Auto
677 */
678     UINT8
   Peg3PowerDownUnusedLanes;
679
680 /** Offset 0x0123 - PCIe ASPM programming
   will happen in relation to the Oeprom
681   Select when PCIe ASPM programming will
   happen in relation to the Oeprom. Before(0x0)
   (Default):
682   Do PCIe ASPM programming before Oeprom,
   After(0x1): Do PCIe ASPM programming after
683   Oeprom, requires an SMI handler to
   save/restore ASPM settings during S3 resume
684   0:Before, 1:After
685 */
686     UINT8
   InitPcieAspmAfterOeprom;
687
688 /** Offset 0x0124 - PCIe Disable Spread
```

```
    Spectrum Clocking
689 |    PCIe Disable Spread Spectrum Clocking.
690 |    Normal Operation(0x0)(Default) - SSC enabled,
690 |    Disable SSC(0X1) - Disable SSC per
691 |    platform design or for compliance testing
691 |    0:Normal Operation, 1:Disable SSC
692 |    */
693 |    UINT8
693 |    PegDisableSpreadSpectrumClocking;
694 |
695 |    /** Offset 0x0125
696 |    */
697 |    UINT8
697 |    UnusedUpdSpace4[3];
698 |
699 |    /** Offset 0x0128 - DMI Gen3 Root port
700 |    preset values per lane
700 |    Used for programming DMI Gen3 preset
700 |    values per lane. Range: 0-9, 8 is default for
700 |    each lane
701 |    */
702 |    UINT8
702 |    DmiGen3RootPortPreset[8];
703 |
704 |    /** Offset 0x0130 - DMI Gen3 End port preset
705 |    values per lane
705 |    Used for programming DMI Gen3 preset
705 |    values per lane. Range: 0-9, 7 is default for
705 |    each lane
706 |    */
707 |    UINT8
707 |    DmiGen3EndPointPreset[8];
708 |
709 |    /** Offset 0x0138 - DMI Gen3 End port Hint
710 |    values per lane
710 |    Used for programming DMI Gen3 Hint values
710 |    per lane. Range: 0-6, 2 is default for each
```

```
    lane
711  */
712  UINT8
    DmiGen3EndPointHint[8];
713
714 /** Offset 0x0140 - DMI Gen3 RxCTLEp per-
    Bundle control
715     Range: 0-15, 0 is default for each bundle,
    must be specified based upon platform design
716 */
717  UINT8
    DmiGen3RxCtlePeaking[4];
718
719 /** Offset 0x0144 - Thermal Velocity Boost
    Ratio clipping
720     0(Default): Disabled, 1: Enabled. This
    service controls Core frequency reduction
721     caused by high package temperatures for
    processors that implement the Intel Thermal
722     Velocity Boost (TVB) feature
723     0: Disabled, 1: Enabled
724 */
725  UINT8
    TvbRatioClipping;
726
727 /** Offset 0x0145 - Thermal Velocity Boost
    voltage optimization
728     0: Disabled, 1: Enabled(Default). This
    service controls thermal based voltage
    optimizations
729     for processors that implement the Intel
    Thermal Velocity Boost (TVB) feature.
730     0: Disabled, 1: Enabled
731 */
732  UINT8
    TvbVoltageOptimization;
733
```

```
734 /** Offset 0x0146
735 */
736     UINT8
    UnusedUpdSpace5[2];
737
738 /** Offset 0x0148 - PEG Gen3 RxCTLEp per-
    Bundle control
739     Range: 0-15, 12 is default for each
        bundle, must be specified based upon platform
        design
740 */
741     UINT8
    PegGen3RxCtlePeaking[10];
742
743 /** Offset 0x0152 - Memory data pointer for
    saved preset search results
744     The reference code will store the Gen3
        Preset Search results in the SaDataHob's
745     PegData structure (SA_PEG_DATA) and
        platform code can save/restore this data to
746     skip preset search in the following boots.
        Range: 0-0xFFFFFFFF, default is 0
747 */
748     UINT32                               PegDataPtr;
749
750 /** Offset 0x0156 - PEG PERST# GPIO
    information
751     The reference code will use the
        information in this structure in order to
        reset
752     PCIe Gen3 devices during equalization, if
        necessary
753 */
754     UINT8
    PegGpioData[28];
755
756 /** Offset 0x0172 - PCIe Hot Plug
```

```
    Enable/Disable per port
757    0(Default): Disable, 1: Enable
758    */
759    UINT8
PegRootPortHPE[4];
760
761 /** Offset 0x0176 - DeEmphasis control for
DMI
762    DeEmphasis control for DMI. 0=-6dB,
1(Default)=-3.5 dB
763    0: -6dB, 1: -3.5dB
764    */
765    UINT8                                DmiDeEmphasis;
766
767 /** Offset 0x0177 - Selection of the primary
display device
768    0=iGFX, 1=PEG, 2=PCIe Graphics on PCH,
3(Default)=AUTO, 4=Switchable Graphics
769    0:iGFX, 1:PEG, 2:PCIe Graphics on PCH,
3:AUTO, 4:Switchable Graphics
770    */
771    UINT8
PrimaryDisplay;
772
773 /** Offset 0x0178 - Selection of iGFX GTT
Memory size
774    1=2MB, 2=4MB, 3=8MB, Default is 3
775    1:2MB, 2:4MB, 3:8MB
776    */
777    UINT16                                GttSize;
778
779 /** Offset 0x017A - Temporary MMIO address
for GMADR
780    The reference code will use this as
Temporary MMIO address space to access GMADR
781    Registers.Platform should provide conflict
free Temporary MMIO Range: GmAdr to
```

```

782     (GmAddr + ApertureSize). Default is
783     (PciExpressBaseAddress - ApertureSize) to
784     (PciExpressBaseAddress
785         - 0x1) (Where ApertureSize = 256MB)
786     */
787     UINT32                               GmAddr;
788
789     /** Offset 0x017E - Temporary MMIO address
790      for GTTMMADR
791      The reference code will use this as
792      Temporary MMIO address space to access
793      GTTMMADR
794
795      Registers.Platform should provide conflict
796      free Temporary MMIO Range: GttMmAddr
797      to (GttMmAddr + 2MB MMIO + 6MB Reserved +
798      GttSize). Default is (GmAddr - (2MB MMIO
799      + 6MB Reserved + GttSize)) to (GmAddr -
0x1) (Where GttSize = 8MB)
800
801     */
802     UINT32                               GttMmAddr;
803
804     /** Offset 0x0182 - Selection of PSMI Region
size
805      0=32MB, 1=288MB, 2=544MB, 3=800MB,
806      4=1024MB Default is 0
807      0:32MB, 1:288MB, 2:544MB, 3:800MB,
808      4:1024MB
809     */
810     UINT8
811     PsmiRegionSize;
812
813     /** Offset 0x0183 - Switchable Graphics GPIO
information for PEG 0
814      Switchable Graphics GPIO information for
815      PEG 0, for Reset, power and wake GPIOs
816     */
817     UINT8

```

```
    SaRtd3Pcie0Gpio[24];
805
806 /** Offset 0x019B - Switchable Graphics GPIO
   information for PEG 1
807   Switchable Graphics GPIO information for
   PEG 1, for Reset, power and wake GPIOs
808 */
809   UINT8
   SaRtd3Pcie1Gpio[24];
810
811 /** Offset 0x01B3 - Switchable Graphics GPIO
   information for PEG 2
812   Switchable Graphics GPIO information for
   PEG 2, for Reset, power and wake GPIOs
813 */
814   UINT8
   SaRtd3Pcie2Gpio[24];
815
816 /** Offset 0x01CB - Switchable Graphics GPIO
   information for PEG 3
817   Switchable Graphics GPIO information for
   PEG 3, for Reset, power and wake GPIOs
818 */
819   UINT8
   SaRtd3Pcie3Gpio[24];
820
821 /** Offset 0x01E3 - Enable/Disable MRC TXT
   dependency
822   When enabled MRC execution will wait for
   TXT initialization to be done first.
   Disabled(0x0)(Default):
823   MRC will not wait for TXT initialization,
   Enabled(0x1): MRC will wait for TXT
   initialization
824   $EN_DIS
825 */
826   UINT8
```

```
    TxtImplemented;
827
828 /** Offset 0x01E4 - Enable/Disable SA
829   OcSupport
830   Enable: Enable SA OcSupport,
831   Disable(Default): Disable SA OcSupport
832   $EN_DIS
833 */
834   UINT8                               SaOcSupport;
835
836 /**
837   ** Offset 0x01E5 - GT slice Voltage Mode
838   0(Default): Adaptive, 1: Override
839   0: Adaptive, 1: Override
840 */
841   UINT8                               GtVoltageMode;
842
843 /**
844   ** Offset 0x01E6 - Maximum GTs turbo ratio
845   override
846   0(Default)=Minimal/Auto, 60=Maximum
847 */
848   UINT8                               GtMaxOcRatio;
849
850 /**
851   ** Offset 0x01E7 - The voltage offset
852   applied to GT slice
853   0(Default)=Minimal, 1000=Maximum
854 */
855   UINT16
856   GtVoltageOffset;
857
858 /**
859   ** Offset 0x01E9 - The GT slice voltage
860   override which is applied to the entire range
861   of GT frequencies
862   0(Default)=Minimal, 2000=Maximum
863 */
864   UINT16
865   GtVoltageOverride;
866
```

```
855 /** Offset 0x01EB - adaptive voltage applied
   during turbo frequencies
856   0(Default)=Minimal, 2000=Maximum
857 */
858   UINT16
859     GtExtraTurboVoltage;
860
860 /** Offset 0x01ED - voltage offset applied
   to the SA
861   0(Default)=Minimal, 1000=Maximum
862 */
863   UINT16
864     SaVoltageOffset;
865
865 /** Offset 0x01EF - PCIe root port Function
   number for Switchable Graphics dGPU
866   Root port Index number to indicate which
   PCIe root port has dGPU
867 */
868   UINT8
869
870 /** Offset 0x01F0 - Realtime Memory Timing
871   0(Default): Disabled, 1: Enabled. When
   enabled, it will allow the system to perform
872   realtime memory timing changes after
   MRC_DONE.
873   0: Disabled, 1: Enabled
874 */
875   UINT8
876     RealtimeMemoryTiming;
877
877 /** Offset 0x01F1 - Enable/Disable SA IPU
878   Enable(Default): Enable SA IPU, Disable:
   Disable SA IPU
879   $EN_DIS
880 */
881   UINT8
881     SaIpueEnable;
```

```
882
883     /** Offset 0x01F2 - IPU IMR Configuration
884      0:IPU Camera, 1:IPU Gen Default is 0
885      0:IPU Camera, 1:IPU Gen
886   */
887     UINT8
888     SaIpumrConfiguration;
889
889     /** Offset 0x01F3 - Selection of PSMI
890      Support On/Off
891      0(Default) = FALSE, 1 = TRUE. When TRUE,
892      it will allow the PSMI Support
893      $EN_DIS
894
894   */
895     /** Offset 0x01F4 - GT unslice Voltage Mode
896      0(Default): Adaptive, 1: Override
897      0: Adaptive, 1: Override
898   */
899     UINT8
900     GtusVoltageMode;
901
901     /** Offset 0x01F5 - voltage offset applied
902      to GT unslice
903      0(Default)=Minimal, 2000=Maximum
904   */
904     UINT16
905     GtusVoltageOffset;
906
906     /** Offset 0x01F7 - GT unslice voltage
907      override which is applied to the entire range
908      of GT frequencies
909      0(Default)=Minimal, 2000=Maximum
910   */
910     UINT16
911     GtusVoltageOverride;
```

```
910
911 /** Offset 0x01F9 - adaptive voltage applied
   during turbo frequencies
912   0(Default)=Minimal, 2000=Maximum
913 */
914   UINT16
915     GtusExtraTurboVoltage;
916 /**
917   Offset 0x01FB - Maximum GTus turbo ratio
   override
918   0(Default)=Minimal, 60=Maximum
919 */
920   UINT8
921     GtusMaxOcRatio;
922 /**
923   Offset 0x01FC - SaPreMemProductionRsvd
   Reserved for SA Pre-Mem Production
924   $EN_DIS
925 */
926   UINT8
927     SaPreMemProductionRsvd[4];
928 /**
929   Offset 0x0200 - BIST on Reset
   Enable or Disable BIST on Reset; <b>0:</b>
   Disable</b>; 1: Enable.
930   $EN_DIS
931 */
932   UINT8
933 /**
934   Offset 0x0201 - Skip Stop PBET Timer
   Enable/Disable
935   Skip Stop PBET Timer; <b>0:</b> Disable</b>;
   1: Enable
936   $EN_DIS
937 */
938   UINT8
939     BistOnReset;
940
941 /**
942   Offset 0x0202 - Skip Stop PBET Timer
   Enable/Disable
943   Skip Stop PBET Timer; <b>0:</b> Disable</b>;
   1: Enable
944   $EN_DIS
945 */
946   UINT8
947     SkipStopPbet;
948
```

```
939 /** Offset 0x0202 - C6DRAM power gating
   feature
940 This policy indicates whether or not BIOS
   should allocate PRMRR memory for C6DRAM
941 power gating feature.- 0: Don't allocate
   any PRMRR memory for C6DRAM power gating
942 feature.- <b>1: Allocate PRMRR memory for
   C6DRAM power gating feature</b>.
943 $EN_DIS
944 */
945 UINT8                           EnableC6Dram;
946
947 /** Offset 0x0203 - Over clocking support
   Over clocking support; <b>0: Disable</b>;
   1: Enable
948 $EN_DIS
949 */
950 UINT8                           OcSupport;
951
952 /** Offset 0x0204 - Over clocking Lock
   Over clocking Lock Enable/Disable; <b>0:
   Disable</b>; 1: Enable.
953 $EN_DIS
954 */
955 UINT8                           OcLock;
956
957
958 /**
959 ** Offset 0x0205 - Maximum Core Turbo Ratio
   Override
960 Maximum core turbo ratio override allows
   to increase CPU core frequency beyond the
961 fused max turbo ratio limit. <b>0:
   Hardware defaults.</b> Range: 0-255
962 */
963 UINT8                           CoreMaxOcRatio;
964
965 /** Offset 0x0206 - Core voltage mode
```

```
966     Core voltage mode; <b>0: Adaptive</b>; 1: Override.
967     $EN_DIS
968 */
969     UINT8
970     CoreVoltageMode;
971 /**
972     Program Cache Attributes
973     Program Cache Attributes; <b>0: Program</b>; 1: Disable Program.
974     $EN_DIS
975 */
976     UINT8
977     DisableMtrrProgram;
978 /**
979     Maximum clr turbo ratio override
980     Maximum clr turbo ratio override allows to
981     increase CPU clr frequency beyond the
982     fused max turbo ratio limit. <b>0: Hardware defaults.</b> Range: 0-255
983 */
984     UINT8
985     RingMaxOcRatio;
986 /**
987     Hyper Threading
988     Enable/Disable
989     Enable or Disable Hyper Threading; 0:
990     Disable; <b>1: Enable</b>
991     $EN_DIS
992 */
993     UINT8
994     HyperThreading;
995 /**
996     CPU ratio value
997     CPU ratio value. Valid Range 0 to 63. CPU
998     Ratio is 0 when disabled.
```

```

991  */
992  UINT8          CpuRatio;
993
994 /** Offset 0x020B - Boot frequency
995   Sets the boot frequency starting from
996   reset vector.- 0: Maximum battery
997   performance.-
```

1: Maximum non-turbo performance

2: Turbo performance. @note If Turbo

is selected BIOS will start in max non-turbo mode and switch to Turbo mode.

```

998  0:0, 1:1, 2:2
999 */
1000 UINT8          BootFrequency;
1001
1002 /** Offset 0x020C - Number of active cores
1003   Number of active cores(Depends on Number
1004   of cores). <b>0: All</b>;<b>1: 1 </b>;<b>2:
1005   2 </b>;<b>3: 3 </b>
1006   0:All, 1:1, 2:2, 3:3
1007 */
1008 UINT8          ActiveCoreCount;
1009 /**
1010  ** Offset 0x020D - Processor Early Power On
1011  Configuration FCLK setting
1012  <b>0: 800 MHz (ULT/ULX)</b>. <b>1: 1 GHz
1013  (DT/Halo)</b>. Not supported on ULT/ULX.-
```

2: 400 MHz. - 3: Reserved

```

1014  0:800 MHz, 1: 1 GHz, 2: 400 MHz, 3:
1015  Reserved
1016 */
1017  UINT8          FClkFrequency;
1018
1019 /**
1020  ** Offset 0x020E - Set JTAG power in C10
1021  and deeper power states
1022  False: JTAG is power gated in C10 state.
1023 */

```

```
    True: keeps the JTAG power up during C10
1018|    and deeper power states for debug purpose.
    <b>0: False</b>; 1: True.
1019|    0: False, 1: True
1020|    */
1021|    UINT8
1022|        JtagC10PowerGateDisable;
1023|    /** Offset 0x020F - Enable or Disable VMX
1024|        Enable or Disable VMX; 0: Disable; <b>1:</b>
    Enable</b>.
1025|        $EN_DIS
1026|    */
1027|    UINT8                                VmxEnable;
1028|
1029|    /** Offset 0x0210 - AVX2 Ratio Offset
1030|        0(Default)= No Offset. Range 0 - 31.
    Specifies number of bins to decrease AVX ratio
1031|        vs. Core Ratio. Uses Mailbox MSR 0x150,
    cmd 0x1B.
1032|    */
1033|    UINT8
1034|        Avx2RatioOffset;
1035|    /** Offset 0x0211 - AVX3 Ratio Offset
1036|        0(Default)= No Offset. Range 0 - 31.
    Specifies number of bins to decrease AVX ratio
1037|        vs. Core Ratio. Uses Mailbox MSR 0x150,
    cmd 0x1B.
1038|    */
1039|    UINT8
1040|        Avx3RatioOffset;
1041|    /** Offset 0x0212 - BCLK Adaptive Voltage
    Enable
1042|        When enabled, the CPU V/F curves are aware
        of BCLK frequency when calculated. </b>0:
```

```
1043     Disable; <b> 1: Enable
1044     $EN_DIS
1045     */
1046     UINT8
1047     BclkAdaptiveVoltage;
1048     /** Offset 0x0213 - Core PLL voltage offset
1049      Core PLL voltage offset. <b>0: No
1050      offset</b>. Range 0-63
1051     */
1052     UINT8
1053     CorePllVoltageOffset;
1054     /** Offset 0x0214 - core voltage override
1055      The core voltage override which is applied
1056      to the entire range of cpu core frequencies.
1057      Valid Range 0 to 2000
1058      */
1059     UINT16
1060     CoreVoltageOverride;
1061     /** Offset 0x0216 - Core Turbo voltage
1062      Adaptive
1063      Extra Turbo voltage applied to the cpu
1064      core when the cpu is operating in turbo mode.
1065      Valid Range 0 to 2000
1066      */
1067     UINT16
1068     CoreVoltageAdaptive;
1069     /** Offset 0x0218 - Core Turbo voltage
1070      Offset
1071      The voltage offset applied to the core
1072      while operating in turbo mode. Valid Range 0 to
1073      1000
1074      */
1075     UINT16
```

```
    CoreVoltageOffset;

1069
1070 /** Offset 0x021A - Ring Downbin
1071   Ring Downbin enable/disable. When enabled,
1072   CPU will ensure the ring ratio is always
1073   lower than the core ratio.0: Disable;
1074   <b>1: Enable.</b>
1075   $EN_DIS
1076 */
1077   UINT8                               RingDownBin;

1078 /** Offset 0x021B - Ring voltage mode
1079   Ring voltage mode; <b>0: Adaptive</b>; 1:
1080   Override.
1081   $EN_DIS
1082 */
1083   UINT8
1084   RingVoltageMode;

1085 /** Offset 0x021C - Ring voltage override
1086   The ring voltage override which is applied
1087   to the entire range of cpu ring frequencies.
1088   Valid Range 0 to 2000
1089 */
1090   UINT16
1091   RingVoltageOverride;

1092 /** Offset 0x021E - Ring Turbo voltage
1093   Adaptive
1094   Extra Turbo voltage applied to the cpu
1095   ring when the cpu is operating in turbo mode.
1096   Valid Range 0 to 2000
1097 */
1098   UINT16
1099   RingVoltageAdaptive;

1100 /** Offset 0x0220 - Ring Turbo voltage
```

```
Offset
1096    The voltage offset applied to the ring
        while operating in turbo mode. Valid Range 0
        to 1000
1097 */
1098     UINT16
1099     RingVoltageOffset;
1100 /**
1101     ** Offset 0x0222 - TjMax Offset
1102     TjMax offset.Specified value here is
        clipped by pCode (125 - TjMax Offset) to
        support
1103     TjMax in the range of 62 to 115 deg
        Celsius. Valid Range 10 - 63
1104 */
1105     UINT8
1106 /**
1107     ** Offset 0x0223 - BiosGuard
1108     Enable/Disable. 0: Disable, Enable/Disable
        BIOS Guard feature, 1: enable
1109     $EN_DIS
1110 */
1111     UINT8
1112 /**
1113 */
1114     UINT8
        BiosGuardToolsInterface;
1115 /**
1116     ** Offset 0x0225 - EnableSgx
1117     Enable/Disable. 0: Disable, Enable/Disable
        SGX feature, 1: enable, 2: Software Control
1118     0: Disable, 1: Enable, 2: Software Control
1119 */
1120     UINT8
        EnableSgx;
1121
1122 /**
1123     ** Offset 0x0226 - Txt
```

```
1123     Enable/Disable. 0: Disable, Enable/Disable  
1124     Txt feature, 1: enable  
1125     $EN_DIS  
1126     */
1127     UINT8                                     Txt;  
1128     /** Offset 0x0227  
1129     **/  
1130     UINT8  
1131     UnusedUpdSpace6;  
1132     /** Offset 0x0228 - PrmrrSize  
1133     0=Invalid, 32MB=0x2000000, 64MB=0x4000000,  
1134     128MB=0x8000000, 256MB=0x10000000  
1135     */
1136     UINT32                                     PrmrrSize;  
1137     /** Offset 0x022C - SinitMemorySize  
1138     Enable/Disable. 0: Disable, define default  
1139     value of SinitMemorySize , 1: enable  
1140     */
1141     UINT32                                     SinitMemorySize;  
1142     /** Offset 0x0230 - TxtHeapMemorySize  
1143     Enable/Disable. 0: Disable, define default  
1144     value of TxtHeapMemorySize , 1: enable  
1145     */
1146     UINT32                                     TxtHeapMemorySize;  
1147     /** Offset 0x0234 - TxtDprMemorySize  
1148     Enable/Disable. 0: Disable, define default  
1149     value of TxtDprMemorySize , 1: enable  
1150     */
1151     UINT32                                     TxtDprMemorySize;
```

```
1151
1152 /** Offset 0x0238 - TxtDprMemoryBase
1153   Enable/Disable. 0: Disable, define default
1154   value of TxtDprMemoryBase , 1: enable
1155 */
1156     UINT64
1157     TxtDprMemoryBase;
1158
1159 /**
1160   UINT32
1161
1162 /** Offset 0x0240 - BiosAcmBase
1163   Enable/Disable. 0: Disable, define default
1164   value of BiosAcmBase , 1: enable
1165 */
1166     BiosAcmBase;
1167
1168 /**
1169   UINT32
1170   ApStartupBase;
1171
1172 /** Offset 0x024C - TgaSize
1173   Enable/Disable. 0: Disable, define default
1174   value of TgaSize , 1: enable
1175 */
1176     TgaSize;
1177
1178 /**
1179   UINT64
1180   TxtLcpPdBase;
```

```
1181
1182  /** Offset 0x0258 - TxtLcpPdSize
1183   Enable/Disable. 0: Disable, define default
1184   value of TxtLcpPdSize , 1: enable
1185   */
1186   UINT64                      TxtLcpPdSize;
1187
1188  /** Offset 0x0260 - IsTPMPresence
1189   IsTPMPresence default values
1190   */
1191   UINT8                      IsTPMPresence;
1192
1193  /** Offset 0x0261 - ReservedSecurityPreMem
1194   Reserved for Security Pre-Mem
1195   $EN_DIS
1196   */
1197   UINT8
1198   ReservedSecurityPreMem[15];
1199
1200  /** Offset 0x0270 - Enable PCH HSIO PCIE RX
1201   Set Ctle
1202   Enable PCH PCIe Gen 3 Set CTLE Value.
1203   */
1204   UINT8
1205   PchPcieHsioRxSetCtleEnable[24];
1206
1207  /** Offset 0x0288 - PCH HSIO PCIE Rx Set
1208   Ctle Value
1209   PCH PCIe Gen 3 Set CTLE Value.
1210   */
1211   UINT8
1212   PchPcieHsioRxSetCtle[24];
1213
1214  /** Offset 0x02A0 - Enble PCH HSIO PCIE TX
1215   Gen 1 Downscale Amplitude Adjustment value
1216   override
1217   0: Disable; 1: Enable.
```

```
1210 /**/
1211     UINT8
1212         PchPcieHsioTxGen1DownscaleAmpEnable[24];
1213 /**
1214  ** Offset 0x02B8 - PCH HSIO PCIE Gen 2 TX
1215  Output Downscale Amplitude Adjustment value
1216  PCH PCIe Gen 2 TX Output Downscale
1217  Amplitude Adjustment value.
1218 /**
1219  ** Offset 0x02D0 - Enable PCH HSIO PCIE TX
1220  Gen 2 Downscale Amplitude Adjustment value
1221  override
1222  0: Disable; 1: Enable.
1223 /**
1224     UINT8
1225         PchPcieHsioTxGen2DownscaleAmpEnable[24];
1226 /**
1227  ** Offset 0x02E8 - PCH HSIO PCIE Gen 2 TX
1228  Output Downscale Amplitude Adjustment value
1229  PCH PCIe Gen 2 TX Output Downscale
1230  Amplitude Adjustment value.
1231 /**
1232     UINT8
1233         PchPcieHsioTxGen2DownscaleAmp[24];
1234 /**
1235  ** Offset 0x0300 - Enable PCH HSIO PCIE TX
1236  Gen 3 Downscale Amplitude Adjustment value
1237  override
1238  0: Disable; 1: Enable.
1239 /**
1240     UINT8
1241         PchPcieHsioTxGen3DownscaleAmpEnable[24];
1242 /**
1243  ** Offset 0x0318 - PCH HSIO PCIE Gen 3 TX
```

```
        Output Downscale Amplitude Adjustment value
1234    PCH PCIe Gen 3 TX Output Downscale
           Amplitude Adjustment value.
1235 */
1236     UINT8
           PchPcieHsioTxGen3DownscaleAmp[24];
1237
1238 /** Offset 0x0330 - Enable PCH HSIO PCIE Gen
   1 TX Output De-Emphasis Adjustment Setting
   value override
1239     0: Disable; 1: Enable.
1240 */
1241     UINT8
           PchPcieHsioTxGen1DeEmphEnable[24];
1242
1243 /** Offset 0x0348 - PCH HSIO PCIE Gen 1 TX
   Output De-Emphasis Adjustment value
1244     PCH PCIe Gen 1 TX Output De-Emphasis
   Adjustment Setting.
1245 */
1246     UINT8
           PchPcieHsioTxGen1DeEmph[24];
1247
1248 /** Offset 0x0360 - Enable PCH HSIO PCIE Gen
   2 TX Output -3.5dB De-Emphasis Adjustment
   Setting value override
1249     0: Disable; 1: Enable.
1250 */
1251     UINT8
           PchPcieHsioTxGen2DeEmph3p5Enable[24];
1252
1253 /** Offset 0x0378 - PCH HSIO PCIE Gen 2 TX
   Output -3.5dB De-Emphasis Adjustment value
1254     PCH PCIe Gen 2 TX Output -3.5dB De-
   Emphasis Adjustment Setting.
1255 */
1256     UINT8
```

```
    PchPcieHsioTxGen2DeEmph3p5[24];  
1257  
1258 /** Offset 0x0390 - Enable PCH HSIO PCIE Gen  
2 TX Output -6.0dB De-Emphasis Adjustment  
Setting value override  
1259 0: Disable; 1: Enable.  
1260 **/  
1261     UINT8  
    PchPcieHsioTxGen2DeEmph6p0Enable[24];  
1262  
1263 /** Offset 0x03A8 - PCH HSIO PCIE Gen 2 TX  
Output -6.0dB De-Emphasis Adjustment value  
1264 PCH PCIe Gen 2 TX Output -6.0dB De-  
Emphasis Adjustment Setting.  
1265 **/  
1266     UINT8  
    PchPcieHsioTxGen2DeEmph6p0[24];  
1267  
1268 /** Offset 0x03C0 - Enable PCH HSIO SATA  
Receiver Equalization Boost Magnitude  
Adjustment Value override  
1269 0: Disable; 1: Enable.  
1270 **/  
1271     UINT8  
    PchSataHsioRxGen1EqBoostMagEnable[8];  
1272  
1273 /** Offset 0x03C8 - PCH HSIO SATA 1.5 Gb/s  
Receiver Equalization Boost Magnitude  
Adjustment value  
1274 PCH HSIO SATA 1.5 Gb/s Receiver  
Equalization Boost Magnitude Adjustment value.  
1275 **/  
1276     UINT8  
    PchSataHsioRxGen1EqBoostMag[8];  
1277  
1278 /** Offset 0x03D0 - Enable PCH HSIO SATA  
Receiver Equalization Boost Magnitude
```

```
    Adjustment Value override
1279    0: Disable; 1: Enable.
1280 /**
1281     UINT8
1282     PchSataHsioRxGen2EqBoostMagEnable[8];
1283 /**
1284     ** Offset 0x03D8 - PCH HSIO SATA 3.0 Gb/s
1285     Receiver Equalization Boost Magnitude
1286     Adjustment value
1287     PCH HSIO SATA 3.0 Gb/s Receiver
1288     Equalization Boost Magnitude Adjustment value.
1289 /**
1290     0: Disable; 1: Enable.
1291 /**
1292     UINT8
1293     PchSataHsioRxGen2EqBoostMag[8];
1294 /**
1295     ** Offset 0x03E0 - Enable PCH HSIO SATA
1296     Receiver Equalization Boost Magnitude
1297     Adjustment Value override
1298 /**
1299     0: Disable; 1: Enable.
1300 /**
```

```
1301     UINT8  
1302         PchSataHsioTxGen1DownscaleAmpEnable[8];  
1303     /** Offset 0x03F8 - PCH HSIO SATA 1.5 Gb/s  
1304      TX Output Downscale Amplitude Adjustment value  
1305      PCH HSIO SATA 1.5 Gb/s TX Output Downscale  
1306      Amplitude Adjustment value.  
1307      **/  
1308     UINT8  
1309         PchSataHsioTxGen1DownscaleAmp[8];  
1310     /** Offset 0x0400 - Enable PCH HSIO SATA 3.0  
1311      Gb/s TX Output Downscale Amplitude Adjustment  
1312      value override  
1313      0: Disable; 1: Enable.  
1314      **/  
1315     UINT8  
1316         PchSataHsioTxGen2DownscaleAmpEnable[8];  
1317     /** Offset 0x0408 - PCH HSIO SATA 3.0 Gb/s  
1318      TX Output Downscale Amplitude Adjustment value  
1319      PCH HSIO SATA 3.0 Gb/s TX Output Downscale  
1320      Amplitude Adjustment value.  
1321      **/  
1322     UINT8  
1323         PchSataHsioTxGen2DownscaleAmp[8];  
1324     /** Offset 0x0410 - Enable PCH HSIO SATA 6.0  
1325      Gb/s TX Output Downscale Amplitude Adjustment  
1326      value override  
1327      0: Disable; 1: Enable.  
1328      **/  
1329     UINT8  
1330         PchSataHsioTxGen3DownscaleAmpEnable[8];  
1331     /** Offset 0x0418 - PCH HSIO SATA 6.0 Gb/s  
1332      TX Output Downscale Amplitude Adjustment value
```

```
1324     PCH HSIO SATA 6.0 Gb/s TX Output Downscale  
1325     Amplitude Adjustment value.  
1325     **/  
1326     UINT8  
1326     PchSataHsioTxGen3DownscaleAmp[8];  
1327  
1328     /** Offset 0x0420 - Enable PCH HSIO SATA 1.5  
1328     Gb/s TX Output De-Emphasis Adjustment Setting  
1328     value override  
1329     0: Disable; 1: Enable.  
1330     **/  
1331     UINT8  
1331     PchSataHsioTxGen1DeEmphEnable[8];  
1332  
1333     /** Offset 0x0428 - PCH HSIO SATA 1.5 Gb/s  
1333     TX Output De-Emphasis Adjustment Setting  
1334     PCH HSIO SATA 1.5 Gb/s TX Output De-  
1334     Emphasis Adjustment Setting.  
1335     **/  
1336     UINT8  
1336     PchSataHsioTxGen1DeEmph[8];  
1337  
1338     /** Offset 0x0430 - Enable PCH HSIO SATA 3.0  
1338     Gb/s TX Output De-Emphasis Adjustment Setting  
1338     value override  
1339     0: Disable; 1: Enable.  
1340     **/  
1341     UINT8  
1341     PchSataHsioTxGen2DeEmphEnable[8];  
1342  
1343     /** Offset 0x0438 - PCH HSIO SATA 3.0 Gb/s  
1343     TX Output De-Emphasis Adjustment Setting  
1344     PCH HSIO SATA 3.0 Gb/s TX Output De-  
1344     Emphasis Adjustment Setting.  
1345     **/  
1346     UINT8  
1346     PchSataHsioTxGen2DeEmph[8];
```

```
1347
1348 /** Offset 0x0440 - Enable PCH HSIO SATA 6.0
   Gb/s TX Output De-Emphasis Adjustment Setting
   value override
1349     0: Disable; 1: Enable.
1350 */
1351     UINT8
1352         PchSataHsioTxGen3DeEmphEnable[8];
1353
1354 /** Offset 0x0448 - PCH HSIO SATA 6.0 Gb/s
   TX Output De-Emphasis Adjustment Setting
1355     PCH HSIO SATA 6.0 Gb/s TX Output De-
   Emphasis Adjustment Setting.
1356 */
1357     UINT8
1358         PchSataHsioTxGen3DeEmph[8];
1359
1360     /** Offset 0x0450 - PCH LPC Enhance the port
   8xh decoding
1361     Original LPC only decodes one byte of port
   80h.
1362     $EN_DIS
1363 */
1364     UINT8
1365         PchLpcEnhancePort8xhDecoding;
1366
1367     /** Offset 0x0451 - PCH Port80 Route
   Control where the Port 80h cycles are
   sent, 0: LPC; 1: PCI.
1368     $EN_DIS
1369 */
1370     UINT8
1371         PchPort80Route;
1372
1373     /** Offset 0x0452 - Enable SMBus ARP support
   Enable SMBus ARP support.
1374     $EN_DIS
```

```
1373 */  
1374     UINT8  
    SmbusArpEnable;  
1375  
1376 /** Offset 0x0453 - Number of  
    RsvdSmbusAddressTable.  
1377     The number of elements in the  
    RsvdSmbusAddressTable.  
1378 */  
1379     UINT8  
    PchNumRsvdSmbusAddresses;  
1380  
1381 /** Offset 0x0454 - SMBUS Base Address  
    SMBUS Base Address (IO space).  
1383 */  
1384     UINT16  
    PchSmbusIoBase;  
1385  
1386 /** Offset 0x0456 - Size of PCIe IMR.  
    Size of PCIe IMR in megabytes  
1388 */  
1389     UINT16                      PcieImrSize;  
1390  
1391 /** Offset 0x0458 - Point of  
    RsvdSmbusAddressTable  
1392     Array of addresses reserved for non-ARP-  
    capable SMBus devices.  
1393 */  
1394     UINT32  
    RsvdSmbusAddressTablePtr;  
1395  
1396 /** Offset 0x045C - Enable PCIE RP Mask  
1397     Enable/disable PCIE Root Ports. 0:  
        disable, 1: enable. One bit for each port,  
        bit0  
1398     for port1, bit1 for port2, and so on.  
1399 */
```

```
1400    UINT32
1401        PcieRpEnableMask;
1402    /** Offset 0x0460 - Enable PCIe IMR
1403        0:Disable, 1:Enable
1404        $EN_DIS
1405    */
1406    UINT8
1407        PcieImrEnabled;
1408    /** Offset 0x0461 - Root port number for
1409        IMR.
1410        Root port number for IMR.
1411    */
1412    UINT8
1413    ImrRpSelection;
1414    /** Offset 0x0462 - Enable SMBus Alert Pin
1415        Enable SMBus Alert Pin.
1416        $EN_DIS
1417    */
1418    UINT8
1419    PchSmbAlertEnable;
1420    /** Offset 0x0463 - ReservedPchPreMem
1421        Reserved for Pch Pre-Mem
1422        $EN_DIS
1423    */
1424    UINT8
1425    ReservedPchPreMem[13];
1426    /** Offset 0x0470 - Debug Interfaces
1427        Debug Interfaces. BIT0-RAM, BIT1-UART,
1428        BIT3-USB3, BIT4-Serial IO, BIT5-TraceHub,
1429        BIT2 - Not used.
1430    */
1431    UINT8
```

```
    PcdDebugInterfaceFlags;  
1430  
1431 /** Offset 0x0471 - PcdSerialIoUartNumber  
1432     Select SerialIo Uart Controller for debug.  
1433     0:SerialIoUart0, 1:SerialIoUart1,  
1434     2:SerialIoUart2  
1435     **/  
1436     UINT8  
1437     PcdSerialIoUartNumber;  
1438  
1439 /** Offset 0x0472 - ISA Serial Base  
1440     selection  
1441     Select ISA Serial Base address. Default is  
1442     0x3F8.  
1443     0:0x3F8, 1:0x2F8  
1444     **/  
1445     UINT8  
1446     PcdIsaSerialUartBase;  
1447  
1448 /** Offset 0x0473 - GT PLL voltage offset  
1449     Core PLL voltage offset. <b>0: No  
1450     offset</b>. Range 0-63  
1451     **/  
1452     UINT8  
1453     GtPllVoltageOffset;  
1454  
1455 /** Offset 0x0474 - Ring PLL voltage offset  
1456     Core PLL voltage offset. <b>0: No  
1457     offset</b>. Range 0-63  
1458     **/  
1459     UINT8  
1460     RingPllVoltageOffset;  
1461  
1462 /** Offset 0x0475 - System Agent PLL voltage  
1463     offset  
1464     Core PLL voltage offset. <b>0: No  
1465     offset</b>. Range 0-63
```

```
1455  */
1456  UINT8
1457    SaPllVoltageOffset;
1458 /**
1459  ** Offset 0x0476 - Memory Controller PLL
1460  ** voltage offset
1461  ** Core PLL voltage offset. <b>0: No
1462  ** offset</b>. Range 0-63
1463  */
1464  UINT8
1465    McPllVoltageOffset;
1466 /**
1467  ** Offset 0x0477 - MRC Safe Config
1468  ** Enables/Disable MRC Safe Config
1469  ** $EN_DIS
1470  */
1471  UINT8                                MrcSafeConfig;
1472 /**
1473  ** Offset 0x0478 - PcdSerialDebugBaudRate
1474  ** Baud Rate for Serial Debug Messages.
1475  ** 3:9600, 4:19200, 6:56700, 7:115200.
1476  ** 3:9600, 4:19200, 6:56700, 7:115200
1477  */
1478  UINT8
1479    PcdSerialDebugBaudRate;
1480 /**
1481  ** Offset 0x0479 - HobBufferSize
1482  ** Size to set HOB Buffer. 0:Default, 1: 1
1483  ** Byte, 2: 1 KB, 3: Max value(assuming 63KB
1484  ** total HOB size).
1485  ** 0:Default, 1: 1 Byte, 2: 1 KB, 3: Max
1486  ** value
1487  */
1488  UINT8                                HobBufferSize;
1489 /**
1490  ** Offset 0x047A - Early Command Training
1491  ** Enables/Disable Early Command Training
```

```
1484     $EN_DIS
1485     */
1486     UINT8                           ECT;
1487
1488 /** Offset 0x047B - SenseAmp Offset Training
1489   Enables/Disable SenseAmp Offset Training
1490   $EN_DIS
1491 */
1492     UINT8                           SOT;
1493
1494 /** Offset 0x047C - Early ReadMPR Timing
1495   Centering 2D
1496   Enables/Disable Early ReadMPR Timing
1497   Centering 2D
1498   $EN_DIS
1499 */
1500     UINT8                           ERDMPRTC2D;
1501
1502 /** Offset 0x047D - Read MPR Training
1503   Enables/Disable Read MPR Training
1504   $EN_DIS
1505 */
1506     UINT8                           RDMPRT;
1507
1508 /** Offset 0x047E - Receive Enable Training
1509   Enables/Disable Receive Enable Training
1510   $EN_DIS
1511 */
1512     UINT8                           RCVET;
1513
1514 /** Offset 0x047F - Jedec Write Leveling
1515   Enables/Disable Jedec Write Leveling
1516   $EN_DIS
1517 */
1518     UINT8                           JWRL;
```

```
    Centering 2D
1519    Enables/Disable Early Write Time Centering
2D
1520    $EN_DIS
1521    */
1522    UINT8                                EWRTC2D;
1523
1524    /** Offset 0x0481 - Early Read Time
     Centering 2D
1525    Enables/Disable Early Read Time Centering
2D
1526    $EN_DIS
1527    */
1528    UINT8                                ERDTC2D;
1529
1530    /** Offset 0x0482 - Write Timing Centering
     1D
1531    Enables/Disable Write Timing Centering 1D
$EN_DIS
1532    */
1533    UINT8                                WRTC1D;
1534
1535
1536    /** Offset 0x0483 - Write Voltage Centering
     1D
1537    Enables/Disable Write Voltage Centering 1D
$EN_DIS
1538    */
1539    UINT8                                WRVC1D;
1540
1541
1542    /** Offset 0x0484 - Read Timing Centering 1D
     Enables/Disable Read Timing Centering 1D
$EN_DIS
1543    */
1544    UINT8                                RDTC1D;
1545
1546
1547
1548    /** Offset 0x0485 - Dimm ODT Training
     Enables/Disable Dimm ODT Training
```

```
1550     $EN_DIS
1551     */
1552     UINT8           DIMMODTT;
1553
1554 /** Offset 0x0486 - DIMM RON Training
1555   Enables/Disable DIMM RON Training
1556   $EN_DIS
1557 */
1558     UINT8           DIMMRONT;
1559
1560 /** Offset 0x0487 - Write Drive
1561   Strength/Equalization 2D
1562   Enables/Disable Write Drive
1563   Strength/Equalization 2D
1564     $EN_DIS
1565     */
1566     UINT8           WRDSEQT;
1567
1568 /** Offset 0x0488 - Write Slew Rate Training
1569   Enables/Disable Write Slew Rate Training
1570   $EN_DIS
1571 */
1572     UINT8           WRSRT;
1573
1574 /** Offset 0x0489 - Read ODT Training
1575   Enables/Disable Read ODT Training
1576   $EN_DIS
1577 */
1578     UINT8           RDODTT;
1579
1580 /** Offset 0x048A - Read Equalization
1581   Training
1582   Enables/Disable Read Equalization Training
1583   $EN_DIS
1584 */
1585     UINT8           RDEQT;
```

```
1584 /** Offset 0x048B - Read Amplifier Training
1585     Enables/Disable Read Amplifier Training
1586     $EN_DIS
1587 */
1588     UINT8                     RDAPT;
1589
1590 /** Offset 0x048C - Write Timing Centering
1591 2D
1591     Enables/Disable Write Timing Centering 2D
1592     $EN_DIS
1593 */
1594     UINT8                     WRTC2D;
1595
1596 /** Offset 0x048D - Read Timing Centering 2D
1597     Enables/Disable Read Timing Centering 2D
1598     $EN_DIS
1599 */
1600     UINT8                     RDTC2D;
1601
1602 /** Offset 0x048E - Write Voltage Centering
1602 2D
1603     Enables/Disable Write Voltage Centering 2D
1604     $EN_DIS
1605 */
1606     UINT8                     WRVC2D;
1607
1608 /** Offset 0x048F - Read Voltage Centering
1608 2D
1609     Enables/Disable Read Voltage Centering 2D
1610     $EN_DIS
1611 */
1612     UINT8                     RDVC2D;
1613
1614 /** Offset 0x0490 - Command Voltage
1614     Centering
1615     Enables/Disable Command Voltage Centering
1616     $EN_DIS
```

```
1617    */
1618    UINT8                      CMDVC;
1619
1620 /** Offset 0x0491 - Late Command Training
1621   Enables/Disable Late Command Training
1622   $EN_DIS
1623 */
1624    UINT8                      LCT;
1625
1626 /** Offset 0x0492 - Round Trip Latency
1627   Training
1628   Enables/Disable Round Trip Latency
1629   Training
1630   $EN_DIS
1631 */
1632    UINT8                      RTL;
1633
1634 /** Offset 0x0493 - Turn Around Timing
1635   Training
1636   Enables/Disable Turn Around Timing
1637   Training
1638   $EN_DIS
1639 */
1640    UINT8                      TAT;
1641
1642 /** Offset 0x0494 - Memory Test
1643   Enables/Disable Memory Test
1644   $EN_DIS
1645 */
1646    UINT8                      MEMTST;
1647
1648 /** Offset 0x0495 - DIMM SPD Alias Test
1649   Enables/Disable DIMM SPD Alias Test
1650   $EN_DIS
1651 */
1652    UINT8                      ALIASCHK;
1653
```

```

1650  /** Offset 0x0496 - Receive Enable Centering
1D
1651  Enables/Disable Receive Enable Centering
1D
1652  $EN_DIS
1653  */
1654  UINT8                                RCVENC1D;
1655
1656  /** Offset 0x0497 - Retrain Margin Check
1657  Enables/Disable Retrain Margin Check
1658  $EN_DIS
1659  */
1660  UINT8                                RMC;
1661
1662  /** Offset 0x0498 - Write Drive Strength
Up/Dn independently
1663  Enables/Disable Write Drive Strength Up/Dn
independently
1664  $EN_DIS
1665  */
1666  UINT8                                WRDSUDT;
1667
1668  /** Offset 0x0499 - ECC Support
1669  Enables/Disable ECC Support
1670  $EN_DIS
1671  */
1672  UINT8                                EccSupport;
1673
1674  /** Offset 0x049A - Memory Remap
1675  Enables/Disable Memory Remap
1676  $EN_DIS
1677  */
1678  UINT8                                RemapEnable;
1679
1680  /** Offset 0x049B - Rank Interleave support
1681  Enables/Disable Rank Interleave support.
NOTE: RI and HORI can not be enabled at

```

```
1682     the same time.
1683     $EN_DIS
1684     */
1685     UINT8
1686     RankInterleave;
1687     /** Offset 0x049C - Enhanced Interleave
1688      support
1689      Enables/Disable Enhanced Interleave
1690      support
1691      $EN_DIS
1692      */
1693      /**
1694      Enable Memory Trace of Ch 0 to Ch 1 using
1695      Stacked Mode. Both channels must be of
1696      equal size. This option may change TOLUD
1697      and REMAP values as needed.
1698      $EN_DIS
1699      */
1700      /**
1701      Enable/Disable Channel Hash Support. NOTE:
1702      ONLY if Memory interleaved Mode
1703      $EN_DIS
1704      */
1705      /**
1706      Enable/Disable Extern Therm Status
1707      $EN_DIS
1708      */
1709      /**
1710      $EN_DIS
1711      */
```

```
1712 /** Offset 0x04A0 - Closed Loop Therm Manage  
1713     Enables/Disable Closed Loop Therm Manage  
1714     $EN_DIS  
1715 */
1716     UINT8                     EnableCltm;  
1717
1718 /** Offset 0x04A1 - Open Loop Therm Manage  
1719     Enables/Disable Open Loop Therm Manage  
1720     $EN_DIS  
1721 */
1722     UINT8                     EnableOltm;  
1723
1724 /** Offset 0x04A2 - DDR PowerDown and idle  
counter
1725     Enables/Disable DDR PowerDown and idle  
counter
1726     $EN_DIS
1727 */
1728     UINT8                     EnablePwrDn;  
1729
1730 /** Offset 0x04A3 - DDR PowerDown and idle  
counter - LPDDR
1731     Enables/Disable DDR PowerDown and idle  
counter(For LPDDR Only)
1732     $EN_DIS
1733 */
1734     UINT8                     EnablePwrDnLpddr;  
1735
1736 /** Offset 0x04A4 - Use user provided power  
weights, scale factor, and channel power floor  
values
1737     Enables/Disable Use user provided power  
weights, scale factor, and channel power
1738     floor values
1739     $EN_DIS
1740 */
```

```
1741     UINT8  
1742     UserPowerWeightsEn;  
1743     /** Offset 0x04A5 - RAPL PL Lock  
1744      Enables/Disable RAPL PL Lock  
1745      $EN_DIS  
1746      **/  
1747     UINT8                      RaplLim2Lock;  
1748  
1749     /** Offset 0x04A6 - RAPL PL 2 enable  
1750      Enables/Disable RAPL PL 2 enable  
1751      $EN_DIS  
1752      **/  
1753     UINT8                      RaplLim2Ena;  
1754  
1755     /** Offset 0x04A7 - RAPL PL 1 enable  
1756      Enables/Disable RAPL PL 1 enable  
1757      $EN_DIS  
1758      **/  
1759     UINT8                      RaplLim1Ena;  
1760  
1761     /** Offset 0x04A8 - SelfRefresh Enable  
1762      Enables/Disable SelfRefresh Enable  
1763      $EN_DIS  
1764      **/  
1765     UINT8                      SrefCfgEna;  
1766  
1767     /** Offset 0x04A9 - Throttler CKEMin  
1768      Defeature - LPDDR  
1769      Enables/Disable Throttler CKEMin  
1770      Defeature(For LPDDR Only)  
1771      $EN_DIS  
1772      **/  
1773     UINT8                      ThrtCkeMinDefeatLpddr;  
1774  
1775     /** Offset 0x04AA - Throttler CKEMin
```

```
Defeature
1774    Enables/Disable Throttler CKEMin Defeature
1775    $EN_DIS
1776    */
1777    UINT8
    ThrtCkeMinDefeat;

1778    /**
1779     ** Offset 0x04AB - Enable RH Prevention
1780     Enables/Disable RH Prevention
1781     $EN_DIS
1782     */
1783    UINT8                           RhPrevention;

1784
1785    /**
1786     ** Offset 0x04AC - Exit On Failure (MRC)
1787     Enables/Disable Exit On Failure (MRC)
1788     $EN_DIS
1789     */
1790    UINT8                           ExitOnFailure;

1791    /**
1792     ** Offset 0x04AD - LPDDR Thermal Sensor
1793     Enables/Disable LPDDR Thermal Sensor
1794     $EN_DIS
1795     */
1796    UINT8
    DdrThermalSensor;

1797    /**
1798     ** Offset 0x04AE - Select if CLK0 is shared
1799     between Rank0 and Rank1 in DDR4 DDP
1800     Select if CLK0 is shared between Rank0 and
1801     Rank1 in DDR4 DDP
1802     $EN_DIS
1803     */
1804    UINT8
    Ddr4DdpSharedClock;

1805    /**
1806     ** Offset 0x04AF - Select if ZQ pin is
1807     shared between Rank0 and Rank1 in DDR4 DDP
```

```
1804     ESelect if ZQ pin is shared between Rank0  
1805     and Rank1 in DDR4 DDP  
1806     **/  
1807     UINT8  
1808         Ddr4DdpSharedZq;  
1809     /** Offset 0x04B0 - Ch Hash Mask  
1810     Set the BIT(s) to be included in the XOR  
1811     function. NOTE BIT mask corresponds to  
1812     BITS [19:6  
1813     **/  
1814     UINT16                                     ChHashMask;  
1815     /** Offset 0x04B2 - Base reference clock  
1816     value  
1817     Base reference clock value, in  
1818     Hertz(Default is 125Hz)  
1819     100000000:100Hz, 125000000:125Hz,  
1820     167000000:167Hz, 250000000:250Hz  
1821     **/  
1822     UINT32                                     BClkFrequency;  
1823     /** Offset 0x04B6 - Ch Hash Interleaved Bit  
1824     Select the BIT to be used for Channel  
1825     Interleaved mode. NOTE: BIT7 will interlace  
1826     the channels at a 2 cacheline granularity,  
1827     BIT8 at 4 and BIT9 at 8. Default is BIT8  
1828     0:BIT6, 1:BIT7, 2:BIT8, 3:BIT9, 4:BIT10,  
1829     5:BIT11, 6:BIT12, 7:BIT13  
1830     **/  
1831     UINT8  
1832         ChHashInterleaveBit;  
1833     /** Offset 0x04B7 - Energy Scale Factor  
1834     Energy Scale Factor, Default is 4  
1835     **/
```

```
1831     UINT8  
1832     EnergyScaleFact;  
1833  
1834     /** Offset 0x04B8 - EPG DIMM Idd3N  
1834      Active standby current (Idd3N) in  
1834      millamps from datasheet. Must be calculated  
1834      on  
1835      a per DIMM basis. Default is 26  
1836      **/  
1837     UINT16                                Idd3n;  
1838  
1839     /** Offset 0x04BA - EPG DIMM Idd3P  
1840      Active power-down current (Idd3P) in  
1840      millamps from datasheet. Must be calculated  
1841      on a per DIMM basis. Default is 11  
1842      **/  
1843     UINT16                                Idd3p;  
1844  
1845     /** Offset 0x04BC - CMD Slew Rate Training  
1846      Enable/Disable CMD Slew Rate Training  
1847      $EN_DIS  
1848      **/  
1849     UINT8                                 CMDSR;  
1850  
1851     /** Offset 0x04BD - CMD Drive Strength and  
1851      Tx Equalization  
1852      Enable/Disable CMD Drive Strength and Tx  
1852      Equalization  
1853      $EN_DIS  
1854      **/  
1855     UINT8                                 CMDDSEQ;  
1856  
1857     /** Offset 0x04BE - CMD Normalization  
1858      Enable/Disable CMD Normalization  
1859      $EN_DIS  
1860      **/  
1861     UINT8                                 CMDNORM;
```

```
1862
1863 /** Offset 0x04BF - Early DQ Write Drive
   Strength and Equalization Training
1864   Enable/Disable Early DQ Write Drive
   Strength and Equalization Training
1865   $EN_DIS
1866 */
1867   UINT8           EWRDSEQ;
1868
1869 /** Offset 0x04C0 - RH Activation
   Probability
1870   RH Activation Probability, Probability
   value is 1/2^(inputvalue)
1871 */
1872   UINT8
   RhActProbability;
1873
1874 /** Offset 0x04C1 - RAPL PL 2 WindowX
   Power PL 2 time window X value, (1/1024)*
   (1+(x/4))*(2^y) (1=Def)
1875 */
1876   UINT8           RaplLim2WindX;
1877
1878
1879 /** Offset 0x04C2 - RAPL PL 2 WindowY
   Power PL 2 time window Y value, (1/1024)*
   (1+(x/4))*(2^y) (1=Def)
1880 */
1881   UINT8           RaplLim2WindY;
1882
1883
1884 /** Offset 0x04C3 - RAPL PL 1 WindowX
   Power PL 1 time window X value, (1/1024)*
   (1+(x/4))*(2^y) (0=Def)
1885 */
1886   UINT8           RaplLim1WindX;
1887
1888
1889 /** Offset 0x04C4 - RAPL PL 1 WindowY
   Power PL 1 time window Y value, (1/1024)*
1890 */
```

```
(1+(x/4))*(2^y) (0=Def)
1891 */
1892     UINT8                         Rap1Lim1WindY;
1893
1894 /** Offset 0x04C5 - RAPL PL 2 Power
1895     range[0;2^14-1]=[2047.875;0]in W, (222=
1896     Def)
1897 */
1898     UINT16                        Rap1Lim2Pwr;
1899
1900 /** Offset 0x04C7 - RAPL PL 1 Power
1901     range[0;2^14-1]=[2047.875;0]in W, (0=
1902     Def)
1903 */
1904     UINT16                        Rap1Lim1Pwr;
1905
1906 /** Offset 0x04C9 - Warm Threshold Ch0 Dimm0
1907     range[255;0]=[31.875;0] in W for OLTM,
1908     [127.5;0] in C for CLTM. Default is 255
1909 */
1910     UINT8                         WarmThresholdCh0Dimm0;
1911
1912     /** Offset 0x04CA - Warm Threshold Ch0 Dimm1
1913     range[255;0]=[31.875;0] in W for OLTM,
1914     [127.5;0] in C for CLTM. Default is 255
1915 */
1916     UINT8                         WarmThresholdCh0Dimm1;
1917
1918     /** Offset 0x04CB - Warm Threshold Ch1 Dimm0
1919     range[255;0]=[31.875;0] in W for OLTM,
1920     [127.5;0] in C for CLTM. Default is 255
1921 */
1922     UINT8                         WarmThresholdCh1Dimm0;
1923
1924     /** Offset 0x04CC - Warm Threshold Ch1 Dimm1
1925     range[255;0]=[31.875;0] in W for OLTM,
1926     [127.5;0] in C for CLTM. Default is 255
1927 */
1928     UINT8                         WarmThresholdCh1Dimm1;
```

```
1919 /** Offset 0x04CC - Warm Threshold Ch1 Dimm1
1920     range[255;0]=[31.875;0] in W for OLTM,
1921     [127.5;0] in C for CLTM. Default is 255
1921 */
1922     UINT8
1923         WarmThresholdCh1Dimm1;
1924
1924 /** Offset 0x04CD - Hot Threshold Ch0 Dimm0
1925     range[255;0]=[31.875;0] in W for OLTM,
1926     [127.5;0] in C for CLTM. Default is 255
1926 */
1927     UINT8
1928         HotThresholdCh0Dimm0;
1929
1929 /** Offset 0x04CE - Hot Threshold Ch0 Dimm1
1930     range[255;0]=[31.875;0] in W for OLTM,
1931     [127.5;0] in C for CLTM. Default is 255
1931 */
1932     UINT8
1933         HotThresholdCh0Dimm1;
1934
1934 /** Offset 0x04CF - Hot Threshold Ch1 Dimm0
1935     range[255;0]=[31.875;0] in W for OLTM,
1936     [127.5;0] in C for CLTM. Default is 255
1936 */
1937     UINT8
1938         HotThresholdCh1Dimm0;
1939
1939 /** Offset 0x04D0 - Hot Threshold Ch1 Dimm1
1940     range[255;0]=[31.875;0] in W for OLTM,
1941     [127.5;0] in C for CLTM. Default is 255
1941 */
1942     UINT8
1943         HotThresholdCh1Dimm1;
1944
1944 /** Offset 0x04D1 - Warm Budget Ch0 Dimm0
1945     range[255;0]=[31.875;0] in W for OLTM,
```

```
    [127.5;0] in C for CLTM
1946    */
1947    UINT8
        WarmBudgetCh0Dimm0;
1948
1949    /** Offset 0x04D2 - Warm Budget Ch0 Dimm1
1950        range[255;0]=[31.875;0] in W for OLTM,
        [127.5;0] in C for CLTM
1951    */
1952    UINT8
        WarmBudgetCh0Dimm1;
1953
1954    /** Offset 0x04D3 - Warm Budget Ch1 Dimm0
1955        range[255;0]=[31.875;0] in W for OLTM,
        [127.5;0] in C for CLTM
1956    */
1957    UINT8
        WarmBudgetCh1Dimm0;
1958
1959    /** Offset 0x04D4 - Warm Budget Ch1 Dimm1
1960        range[255;0]=[31.875;0] in W for OLTM,
        [127.5;0] in C for CLTM
1961    */
1962    UINT8
        WarmBudgetCh1Dimm1;
1963
1964    /** Offset 0x04D5 - Hot Budget Ch0 Dimm0
1965        range[255;0]=[31.875;0] in W for OLTM,
        [127.5;0] in C for CLTM
1966    */
1967    UINT8
        HotBudgetCh0Dimm0;
1968
1969    /** Offset 0x04D6 - Hot Budget Ch0 Dimm1
1970        range[255;0]=[31.875;0] in W for OLTM,
        [127.5;0] in C for CLTM
1971    */
```

```
1972     UINT8
1973         HotBudgetCh0Dimm1;
1974 /**
1975     ** Offset 0x04D7 - Hot Budget Ch1 Dimm0
1976     range[255;0]=[31.875;0] in W for OLTM,
1977     [127.5;0] in C for CLTM
1978 */
1979     UINT8
1980         HotBudgetCh1Dimm0;
1981 /**
1982     ** Offset 0x04D8 - Hot Budget Ch1 Dimm1
1983     range[255;0]=[31.875;0] in W for OLTM,
1984     [127.5;0] in C for CLTM
1985 */
1986     UINT8
1987         HotBudgetCh1Dimm1;
1988 /**
1989     ** Offset 0x04D9 - Idle Energy Ch0Dimm0
1990     Idle Energy Consumed for 1 clk w/dimm
1991     idle/cke on, range[63;0], (10= Def)
1992 */
1993     UINT8
1994         IdleEnergyCh0Dimm0;
1995 /**
1996     ** Offset 0x04DA - Idle Energy Ch0Dimm1
1997     Idle Energy Consumed for 1 clk w/dimm
1998     idle/cke on, range[63;0], (10= Def)
1999 */
2000     UINT8
2001         IdleEnergyCh0Dimm1;
2002 /**
2003     ** Offset 0x04DB - Idle Energy Ch1Dimm0
2004     Idle Energy Consumed for 1 clk w/dimm
2005     idle/cke on, range[63;0], (10= Def)
2006 */
2007     UINT8
2008         IdleEnergyCh1Dimm0;
```

```
1998
1999 /** Offset 0x04DC - Idle Energy Ch1Dimm1
2000   Idle Energy Consumed for 1 clk w/dimm
2001   idle/cke on, range[63;0],(10= Def)
2001 */
2002   UINT8
2003   IdleEnergyCh1Dimm1;
2003
2004 /** Offset 0x04DD - PowerDown Energy
2005   Ch0Dimm0
2006   PowerDown Energy Consumed w/dimm idle/cke
2006   off, range[63;0],(5= Def)
2006 */
2007   UINT8
2007   PdEnergyCh0Dimm0;
2008
2009 /** Offset 0x04DE - PowerDown Energy
2010   Ch0Dimm1
2011   PowerDown Energy Consumed w/dimm idle/cke
2011   off, range[63;0],(5= Def)
2011 */
2012   UINT8
2012   PdEnergyCh0Dimm1;
2013
2014 /** Offset 0x04DF - PowerDown Energy
2015   Ch1Dimm0
2016   PowerDown Energy Consumed w/dimm idle/cke
2016   off, range[63;0],(5= Def)
2016 */
2017   UINT8
2017   PdEnergyCh1Dimm0;
2018
2019 /** Offset 0x04E0 - PowerDown Energy
2020   Ch1Dimm1
2021   PowerDown Energy Consumed w/dimm idle/cke
2021   off, range[63;0],(5= Def)
2021 */
2021 */
```

```
2022 |     UINT8
      |     PdEnergyCh1Dimm1;
2023 |
2024 | /** Offset 0x04E1 - Activate Energy Ch0Dimm0
2025 |     Activate Energy Contribution,
2025 |     range[255;0], (172= Def)
2026 | */
2027 |     UINT8
      |     ActEnergyCh0Dimm0;
2028 |
2029 | /** Offset 0x04E2 - Activate Energy Ch0Dimm1
2030 |     Activate Energy Contribution,
2030 |     range[255;0], (172= Def)
2031 | */
2032 |     UINT8
      |     ActEnergyCh0Dimm1;
2033 |
2034 | /** Offset 0x04E3 - Activate Energy Ch1Dimm0
2035 |     Activate Energy Contribution,
2035 |     range[255;0], (172= Def)
2036 | */
2037 |     UINT8
      |     ActEnergyCh1Dimm0;
2038 |
2039 | /** Offset 0x04E4 - Activate Energy Ch1Dimm1
2040 |     Activate Energy Contribution,
2040 |     range[255;0], (172= Def)
2041 | */
2042 |     UINT8
      |     ActEnergyCh1Dimm1;
2043 |
2044 | /** Offset 0x04E5 - Read Energy Ch0Dimm0
2045 |     Read Energy Contribution, range[255;0],
2045 |     (212= Def)
2046 | */
2047 |     UINT8
      |     RdEnergyCh0Dimm0;
```

```
2048
2049 /** Offset 0x04E6 - Read Energy Ch0Dimm1
2050     Read Energy Contribution, range[255;0],
2051     (212= Def)
2051 */
2052     UINT8
2053         RdEnergyCh0Dimm1;
2054
2054 /** Offset 0x04E7 - Read Energy Ch1Dimm0
2055     Read Energy Contribution, range[255;0],
2056     (212= Def)
2056 */
2057     UINT8
2058         RdEnergyCh1Dimm0;
2059
2059 /** Offset 0x04E8 - Read Energy Ch1Dimm1
2060     Read Energy Contribution, range[255;0],
2061     (212= Def)
2061 */
2062     UINT8
2063         RdEnergyCh1Dimm1;
2064
2064 /** Offset 0x04E9 - Write Energy Ch0Dimm0
2065     Write Energy Contribution, range[255;0],
2066     (221= Def)
2066 */
2067     UINT8
2068         WrEnergyCh0Dimm0;
2069
2069 /** Offset 0x04EA - Write Energy Ch0Dimm1
2070     Write Energy Contribution, range[255;0],
2071     (221= Def)
2071 */
2072     UINT8
2073         WrEnergyCh0Dimm1;
2074
2074 /** Offset 0x04EB - Write Energy Ch1Dimm0
```

```

2075     Write Energy Contribution, range[255;0],
2076     (221= Def)
2077     */
2078     UINT8
2079     WrEnergyCh1Dimm0;
2080
2081     /** Offset 0x04EC - Write Energy Ch1Dimm1
2082     Write Energy Contribution, range[255;0],
2083     (221= Def)
2084     */
2085     UINT8
2086     WrEnergyCh1Dimm1;
2087
2088     /** Offset 0x04ED - Throttler CKEMin Timer
2089     Timer value for CKEMin, range[255;0].
2090     Req'd min of SC_ROUND_T + BYTE_LENGTH (4).
2091     Default is 0x30
2092     */
2093     UINT8
2094     ThrtCkeMinTmr;
2095
2096     /** Offset 0x04EE - Cke Rank Mapping
2097     Bits [7:4] - Channel 1, bits [3:0] -
2098     Channel 0. <b>0xAA=Default</b> Bit [i]
2099     specifies
2100     which rank CKE[i] goes to.
2101     */
2102     UINT8
2103     CkeRankMapping;
2104
2105     /** Offset 0x04EF - Rapl Power Floor Ch0
2106     Power budget ,range[255;0],(0= 5.3W Def)
2107     */
2108     UINT8
2109     RaplPwrFlCh0;
2110
2111     /** Offset 0x04F0 - Rapl Power Floor Ch1
2112     Power budget ,range[255;0],(0= 5.3W Def)
2113     */

```

```

2104    UINT8                               Rap1PwrFlCh1;
2105
2106    /** Offset 0x04F1 - Command Rate Support
2107        CMD Rate and Limit Support Option. NOTE:
2108        ONLY supported in 1N Mode, Default is 3 CMDs
2109        0:Disable, 1:1 CMD, 2:2 CMDS, 3:3 CMDS,
2110        4:4 CMDS, 5:5 CMDS, 6:6 CMDS, 7:7 CMDS
2111    */
2112    UINT8                               EnCmdRate;
2113
2114    /** Offset 0x04F2 - REFRESH_2X_MODE
2115        0- (Default)Disabled 1-iMC enables 2xRef
2116        when Warm and Hot 2- iMC enables 2xRef when
2117        Hot
2118        0:Disable, 1:Enabled for WARM or HOT,
2119        2:Enabled HOT only
2120    */
2121    UINT8                               Refresh2X;
2122
2123    /** Offset 0x04F3 - Energy Performance Gain
2124        Enable/disable(default) Energy Performance
2125        Gain.
2126        $EN_DIS
2127    */
2128    UINT8                               EpgEnable;
2129
2130    /** Offset 0x04F4 - Row Hammer Solution
2131        Type of method used to prevent Row Hammer.
2132        Default is Hardware RHP
2133        0:Hardware RHP, 1:2x Refresh
2134    */
2135    UINT8                               RhSolution;
2136
2137    /** Offset 0x04F5 - User Manual Threshold
2138        Disabled: Predefined threshold will be
2139        used.\n
2140        Enabled: User Input will be used.

```

```
2133     $EN_DIS
2134  */
2135     UINT8
2136     UserThresholdEnable;
2137 /**
2138  ** Offset 0x04F6 - User Manual Budget
2139  ** Disabled: Configuration of memories will
2140  ** defined the Budget value.\n
2141  ** Enabled: User Input will be used.
2142  */
2143     $EN_DIS
2144 /**
2145  ** Offset 0x04F7 - TcritMax
2146  ** Maximum Critical Temperature in Centigrade
2147  ** of the On-DIMM Thermal Sensor. TCRITMax
2148  ** has to be greater than THIGHMax .\n
2149  ** Critical temperature will be TcritMax
2150 /**
2151     UINT8                               TsodTcritMax;
2152 /**
2153  ** Offset 0x04F8 - Event mode
2154  ** Disable:Comparator mode.\n
2155  ** Enable:Interrupt mode
2156  */
2157     UINT8                               TsodEventMode;
2158 /**
2159  ** Offset 0x04F9 - EVENT polarity
2160  ** Disable:Active LOW.\n
2161  ** Enable:Active HIGH
2162  */
2163     UINT8
2164     TsodEventPolarity;
```

```
2165 /** Offset 0x04FA - Critical event only
2166     Disable:Trips on alarm or critical.\n
2167     Enable:Trips only if criticaal temperature
2168     is reached
2169     $EN_DIS
2170 */
2171     UINT8
2172     TsodCriticalEventOnly;
2173
2174 /** Offset 0x04FB - Event output control
2175     Disable:Event output disable.\n
2176     Enable:Event output enabled
2177     $EN_DIS
2178 */
2179     UINT8
2180     TsodEventOutputControl;
2181
2182 /** Offset 0x04FC - Alarm window lock bit
2183     Disable:Alarm trips are not locked and can
2184     be changed.\n
2185     Enable:Alarm trips are locked and cannot
2186     be changed
2187     $EN_DIS
2188 */
2189     UINT8
2190     TsodAlarmwindowLockBit;
2191
2192 /** Offset 0x04FD - Critical trip lock bit
2193     Disable:Critical trip is not locked and
2194     can be changed.\n
2195     Enable:Critical trip is locked and cannot
2196     be changed
2197     $EN_DIS
2198 */
2199     UINT8
2200     TsodCriticaltripLockBit;
2201
2202
```

```
2193 /** Offset 0x04FE - Shutdown mode
2194 Disable:Temperature sensor enable.\n
2195 Enable:Temperature sensor disable
2196 $EN_DIS
2197 */
2198     UINT8
2199     TsodShutdownMode;
2200 /**
2201 ** Offset 0x04FF - ThighMax
2202 Thigh = ThighMax (Default is 93)
2203 */
2204     UINT8
2205     TsodThigMax;
2206 /**
2207 ** Offset 0x0500 - User Manual Thig and
2208 Tcrit
2209 Disabled(Default): Temperature will be
2210 given by the configuration of memories and
2211 1x or 2xrefresh rate.\n
2212 Enabled: User Input will define for Thigh
2213 and Tcrit.
2214 $EN_DIS
2215 */
2216     UINT8
2217     TsodManualEnable;
2218 /**
2219 ** Offset 0x0501 - Force OLTM or 2X Refresh
when needed
2220 Disabled(Default): = Force OLTM.\n
2221 Enabled: = Force 2x Refresh.
2222 $EN_DIS
2223 */
2224     UINT8
2225     ForceOltmOrRefresh2x;
2226 /**
2227 ** Offset 0x0502 - Pwr Down Idle Timer
2228 The minimum value should = to the worst
case Roundtrip delay + Burst_Length. 0 means
```

```
2222    AUTO: 64 for ULX/ULT, 128 for DT/Halo
2223 */
2224     UINT8
2225         PwdwnIdleCounter;
2226 /**
2227  ** Offset 0x0503 - Bitmask of ranks that
2228  ** have CA bus terminated
2229  ** Offset 225 LPDDR4: Bitmask of ranks that
2230  ** have CA bus terminated. <b>0x01=Default,
2231  ** Rank0 is terminating and Rank1 is non-
2232  ** terminating</b>
2233 */
2234     UINT8
2235         CmdRanksTerminated;
2236 /**
2237  ** Offset 0x0504 - GDXC MOT enable
2238  ** GDXC MOT enable.
2239  ** $EN_DIS
2240 /**
2241  ** Offset 0x0505 - PcdSerialDebugLevel
2242  ** Serial Debug Message Level. 0:Disable,
2243  ** 1:Error Only, 2:Error & Warnings, 3:Load,
2244  ** Error, Warnings & Info, 4:Load, Error,
2245  ** Warnings, Info & Event, 5:Load, Error,
2246  ** Warnings,
2247 /**
2248  ** Info & Verbose.
2249  ** 0:Disable, 1:Error Only, 2:Error and
2250  ** Warnings, 3:Load Error Warnings and Info,
2251  ** 4:Load
2252  ** Error Warnings and Info, 5:Load Error
2253  ** Warnings Info and Verbose
2254 /**
2255     UINT8
2256         PcdSerialDebugLevel;
2257
```

```
2247 /** Offset 0x0506 - Fivr Faults
2248   Fivr Faults; 0: Disabled; <b>1: Enabled.
2249   </b>
2250   $EN_DIS
2251   */
2252   UINT8           FivrFaults;
2253
2254 /** Offset 0x0507 - Fivr Efficiency
2255   Fivr Efficiency Management; 0: Disabled;
2256   <b>1: Enabled.</b>
2257   $EN_DIS
2258   */
2259   UINT8           FivrEfficiency;
2260
2261 /** Offset 0x0508 - Safe Mode Support
2262   This option configures the varous items in
2263   the IO and MC to be more conservative.
2264   (def=Disable)
2265   $EN_DIS
2266   */
2267   UINT8           SafeMode;
2268
2269 /** Offset 0x0509 - Ask MRC to clear memory
2270   content
2271   Ask MRC to clear memory content <b>0: Do
2272   not Clear Memory;</b> 1: Clear Memory.
2273   $EN_DIS
2274   */
2275   UINT8           CleanMemory;
2276
2277 /** Offset 0x050A - LpDdrDqDqsReTraining
2278   Enables/Disable LpDdrDqDqsReTraining
2279   $EN_DIS
2280   */
2281   UINT8           LpDdrDqDqsReTraining;
```

```
2276
2277 /** Offset 0x050B - Post Code Output Port
2278   This option configures Post Code Output
2279   Port
2280 */
2281   UINT16
2282     PostCodeOutputPort;
2283
2284 /**
2285   UINT8
2286
2287 /** Offset 0x050D - RMTLoopCount
2288   Specifies the Loop Count to be used during
2289   Rank Margin Tool Testing. 0 - AUTO
2290 */
2291   RMTLoopCount;
2292
2293 /**
2294   UINT8
2295   EnBER;
2296
2297 /**
2298   UINT8
2299   DualDimmPerChannelBoardType;
2300
2301 /**
2302   UINT8
2303   to limit maximum frequency for some SKUs.
2304   0:1DPC, 1:2DPC
2305 */
2306   DualDimmPerChannelBoardType;
2307
2308 /**
2309   UINT8
2310   DDR4 Mixed U-DIMM 2DPC
2311   Limitation
2312 */
2313   Enable/Disable 2667 Frequency Limitation
2314   for DDR4 U-DIMM Mixed Dimm 2DPC population.
2315
2316 /**
2317   Disable(Default)=0, Enable=1
```

```
2303     $EN_DIS
2304     */
2305     UINT8
2306     Ddr4MixedUDimm2DpcLimit;
2307     /** Offset 0x0511 - CFL Reserved
2308         Reserved FspmConfig CFL
2309         $EN_DIS
2310     */
2311     UINT8
2312     ReservedFspmUpdCfl[2];
2313     /** Offset 0x0513 - Memory Test on Warm Boot
2314         Run Base Memory Test on Warm Boot
2315         0:Disable, 1:Enable
2316     */
2317     UINT8
2318     MemTestOnWarmBoot;
2319     /** Offset 0x0514 - Throttler CKEMin Timer -
2320         LPDDR
2321         Timer value for CKEMin (For LPDDR Only),
2322         range[255;0]. Req'd min of SC_ROUND_T +
2323         BYTE_LENGTH (4). Default is 0x40
2324     */
2325     UINT8
2326     ThrtCkeMinTmrLpddr;
2327     /** Offset 0x0515
2328     */
2329     UINT8
2330     ReservedFspmUpd[10];
2331 } FSP_M_CONFIG;
2332 /**
2333     ** Fsp M Test Configuration
2334 */
2335 typedef struct {
```

```
2333
2334     /** Offset 0x0520
2335     */
2336     UINT32                         Signature;
2337
2338     /** Offset 0x0524 - Skip external display
2339      device scanning
2340      Enable: Do not scan for external display
2341      device, Disable (Default): Scan external
2342      display devices
2343      $EN_DIS
2344      */
2345
2346     UINT8                           SkipExtGfxScan;
2347
2348     /** Offset 0x0525 - Generate BIOS Data ACPI
2349      Table
2350      Enable: Generate BDAT for MRC RMT or SA
2351      PCIe data. Disable (Default): Do not generate
2352      it
2353      $EN_DIS
2354      */
2355
2356     UINT8                           BdatEnable;
2357
2358     /** Offset 0x0526 - Detect External Graphics
2359      device for LegacyOpROM
2360      Detect and report if external graphics
2361      device only support LegacyOpROM or not (to
2362      support CSM auto-enable).
2363      Enable(Default)=1, Disable=0
2364      $EN_DIS
2365      */
2366
2367     UINT8                           ScanExtGfxForLegacyOpRom;
2368
2369     /** Offset 0x0527 - Lock PCU Thermal
2370      Management registers
```

```
2359     Lock PCU Thermal Management registers.  
2360     Enable(Default)=1, Disable=0  
2360     $EN_DIS  
2361     **/  
2362     UINT8                                     LockPTMregs;  
2363  
2364     /** Offset 0x0528 - DMI Max Link Speed  
2365         Auto (Default)(0x0): Maximum possible link  
2365         speed, Gen1(0x1): Limit Link to Gen1  
2366         Speed, Gen2(0x2): Limit Link to Gen2  
2366         Speed, Gen3(0x3):Limit Link to Gen3 Speed  
2367         0:Auto, 1:Gen1, 2:Gen2, 3:Gen3  
2368     **/  
2369     UINT8  
2369     DmiMaxLinkSpeed;  
2370  
2371     /** Offset 0x0529 - DMI Equalization Phase 2  
2372         DMI Equalization Phase 2. (0x0): Disable  
2372         phase 2, (0x1): Enable phase 2, (0x2)  
2372         (Default):  
2373         AUTO - Use the current default method  
2374         0:Disable phase2, 1:Enable phase2, 2:Auto  
2375     **/  
2376     UINT8  
2376     DmiGen3EqPh2Enable;  
2377  
2378     /** Offset 0x052A - DMI Gen3 Equalization  
2378     Phase3  
2379     DMI Gen3 Equalization Phase3. Auto(0x0)  
2379     (Default): Use the current default method,  
2380     HwEq(0x1): Use Adaptive Hardware  
2380     Equalization, SwEq(0x2): Use Adaptive Software  
2381     Equalization (Implemented in BIOS  
2381     Reference Code), Static(0x3): Use the Static  
2382     EQs provided in DmiGen3EndPointPreset  
2382     array for Phase1 AND Phase3 (Instead of just  
2383     Phase1), Disabled(0x4): Bypass
```

```
    Equalization Phase 3
2384    0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq,
        4:BypassPhase3
2385 */
2386     UINT8
2387     DmiGen3EqPh3Method;
2388 /**
2389  ** Offset 0x052B - Phase2 EQ enable on the
2390  ** PEG 0:1:0.
2391  ** Phase2 EQ enable on the PEG 0:1:0.
2392  ** Disabled(0x0): Disable phase 2, Enabled(0x1):
2393  ** Enable phase 2, Auto(0x2)(Default): Use
2394  ** the current default method
2395  ** 0:Disable, 1:Enable, 2:Auto
2396 /**
2397  ** 0:Disable, 1:Enable, 2:Auto
2398 /**
2399 /**
2400     UINT8
2401     Peg0Gen3EqPh2Enable;
2402 /**
2403  ** Offset 0x052C - Phase2 EQ enable on the
2404  ** PEG 0:1:1.
2405  ** Phase2 EQ enable on the PEG 0:1:0.
2406  ** Disabled(0x0): Disable phase 2, Enabled(0x1):
2407  ** Enable phase 2, Auto(0x2)(Default): Use
2408  ** the current default method
2409  ** 0:Disable, 1:Enable, 2:Auto
2410 /**
2411 /**
2412  ** 0:Disable, 1:Enable, 2:Auto
2413 /**
2414 /**
2415  ** Offset 0x052D - Phase2 EQ enable on the
2416  ** PEG 0:1:2.
2417  ** Phase2 EQ enable on the PEG 0:1:0.
2418  ** Disabled(0x0): Disable phase 2, Enabled(0x1):
2419  ** Enable phase 2, Auto(0x2)(Default): Use
2420  ** the current default method
2421  ** 0:Disable, 1:Enable, 2:Auto
2422 /**
2423 /**
2424  ** 0:Disable, 1:Enable, 2:Auto
```

```
2407 |     UINT8
2408 |     Peg2Gen3EqPh2Enable;
2409 | /**
2410 | ** Offset 0x052E - Phase2 EQ enable on the
2411 | PEG 0:1:3.
2412 |     Phase2 EQ enable on the PEG 0:1:0.
2413 |     Disabled(0x0): Disable phase 2, Enabled(0x1):
2414 |     Enable phase 2, Auto(0x2)(Default): Use
2415 |     the current default method
2416 |     0:Disable, 1:Enable, 2:Auto
2417 | */
2418 |     UINT8
2419 |     Peg3Gen3EqPh2Enable;
2420 | /**
2421 | ** Offset 0x052F - Phase3 EQ method on the
2422 | PEG 0:1:0.
2423 |     PEG Gen3 Equalization Phase3. Auto(0x0)
2424 |     (Default): Use the current default method,
2425 |     HwEq(0x1): Use Adaptive Hardware
2426 |     Equalization, SwEq(0x2): Use Adaptive Software
2427 |     Equalization (Implemented in BIOS
2428 |     Reference Code), Static(0x3): Use the Static
2429 |     EQs provided in DmiGen3EndPointPreset
2430 |     array for Phase1 AND Phase3 (Instead of just
2431 |     Phase1), Disabled(0x4): Bypass
2432 |     Equalization Phase 3
2433 |     0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq,
2434 |     4:BypassPhase3
2435 | */
2436 |     UINT8
2437 |     Peg0Gen3EqPh3Method;
2438 | /**
2439 | ** Offset 0x0530 - Phase3 EQ method on the
2440 | PEG 0:1:1.
2441 |     PEG Gen3 Equalization Phase3. Auto(0x0)
2442 |     (Default): Use the current default method,
2443 |     HwEq(0x1): Use Adaptive Hardware
```

```
    Equalization, SwEq(0x2): Use Adaptive Software
2429 |    Equalization (Implemented in BIOS
      Reference Code), Static(0x3): Use the Static
2430 |    EQs provided in DmiGen3EndPointPreset
      array for Phase1 AND Phase3 (Instead of just
2431 |    Phase1), Disabled(0x4): Bypass
      Equalization Phase 3
2432 |    0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq,
      4:BypassPhase3
2433 |    */
2434 |    UINT8
      Peg1Gen3EqPh3Method;
2435 |
2436 |    /** Offset 0x0531 - Phase3 EQ method on the
      PEG 0:1:2.
2437 |    PEG Gen3 Equalization Phase3. Auto(0x0)
      (Default): Use the current default method,
2438 |    HwEq(0x1): Use Adaptive Hardware
      Equalization, SwEq(0x2): Use Adaptive Software
2439 |    Equalization (Implemented in BIOS
      Reference Code), Static(0x3): Use the Static
2440 |    EQs provided in DmiGen3EndPointPreset
      array for Phase1 AND Phase3 (Instead of just
2441 |    Phase1), Disabled(0x4): Bypass
      Equalization Phase 3
2442 |    0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq,
      4:BypassPhase3
2443 |    */
2444 |    UINT8
      Peg2Gen3EqPh3Method;
2445 |
2446 |    /** Offset 0x0532 - Phase3 EQ method on the
      PEG 0:1:3.
2447 |    PEG Gen3 Equalization Phase3. Auto(0x0)
      (Default): Use the current default method,
2448 |    HwEq(0x1): Use Adaptive Hardware
      Equalization, SwEq(0x2): Use Adaptive Software
```

```
2449 |     Equalization (Implemented in BIOS
      |     Reference Code), Static(0x3): Use the Static
2450 |     EQs provided in DmiGen3EndPointPreset
      |     array for Phase1 AND Phase3 (Instead of just
2451 |     Phase1), Disabled(0x4): Bypass
      |     Equalization Phase 3
2452 |     0:Auto, 1:HwEq, 2:SwEq, 3:StaticEq,
      |     4:BypassPhase3
2453 |     */
2454 |     UINT8
      |     Peg3Gen3EqPh3Method;
2455 |
2456 |     /** Offset 0x0533 - Enable/Disable PEG GEN3
      |     Static EQ Phase1 programming
2457 |     Program PEG Gen3 EQ Phase1 Static Presets.
      |     Disabled(0x0): Disable EQ Phase1 Static
2458 |     Presets Programming, Enabled(0x1)
      |     (Default): Enable EQ Phase1 Static Presets
      |     Programming
2459 |     $EN_DIS
2460 |     */
2461 |     UINT8
      |     PegGen3ProgramStaticEq;
2462 |
2463 |     /** Offset 0x0534 - PEG Gen3 SwEq Always
      |     Attempt
2464 |     Gen3 Software Equalization will be
      |     executed every boot. Disabled(0x0)(Default):
2465 |     Reuse EQ settings saved/restored from
      |     NVRAM whenever possible, Enabled(0x1): Re-test
2466 |     and generate new EQ values every boot, not
      |     recommended
2467 |     0:Disable, 1:Enable
2468 |     */
2469 |     UINT8
      |     Gen3SwEqAlwaysAttempt;
2470 |
```

```
2471 /** Offset 0x0535 - Select number of TxEq  
presets to test in the PCIe/DMI SwEq  
2472 Select number of TxEq presets to test in  
the PCIe/DMI SwEq. P7,P3,P5(0x0): Test  
2473 Presets 7, 3, and 5, P0-P9(0x1): Test  
Presets 0-9, Auto(0x2)(Default): Use the  
2474 current default method (Default)Auto will  
test Presets 7, 3, and 5. It is possible  
2475 for this default to change over time;using  
Auto will ensure Reference Code always  
2476 uses the latest default settings  
2477 0:P7 P3 P5, 1:P0 to P9, 2:Auto  
2478 */  
2479 UINT8  
Gen3SwEqNumberOfPresets;  
2480  
2481 /** Offset 0x0536 - Enable use of the  
Voltage Offset and Centering Test in the PCIe  
SwEq  
2482 Enable use of the Voltage Offset and  
Centering Test in the PCIe Software  
Equalization  
2483 Algorithm. Disabled(0x0): Disable VOC  
Test, Enabled(0x1): Enable VOC Test, Auto(0x2)  
(Default):  
2484 Use the current default  
2485 0:Disable, 1:Enable, 2:Auto  
2486 */  
2487 UINT8  
Gen3SwEqEnableVocTest;  
2488  
2489 /** Offset 0x0537 - PCIe Rx Compliance  
Testing Mode  
2490 Disabled(0x0)(Default): Normal Operation -  
Disable PCIe Rx Compliance testing,  
Enabled(0x1):  
2491 PCIe Rx Compliance Test Mode - PEG
```

```
    controller is in Rx Compliance Testing Mode;
2492|    it should only be set when doing PCIe
compliance testing
2493|    $EN_DIS
2494| /**
2495|     UINT8
PegRxCemTestingMode;
2496|
2497/** Offset 0x0538 - PCIe Rx Compliance
Loopback Lane When PegRxCemTestingMode is
Enabled
2498|    the specified Lane (0 - 15) will be
used for RxCEMLoopback. Default is Lane 0
2499| /**
2500|     UINT8
PegRxCemLoopbackLane;
2501|
2502/** Offset 0x0539 - Generate PCIe BDAT
Margin Table
2503|    Set this policy to enable the generation
and addition of PCIe margin data to the
2504|    BDAT table. Disabled(0x0)(Default): Normal
Operation - Disable PCIe BDAT margin
2505|    data generation, Enable(0x1): Generate
PCIe BDAT margin data
2506|    $EN_DIS
2507| /**
2508|     UINT8
PegGenerateBdatMarginTable;
2509|
2510/** Offset 0x053A - PCIe Non-Protocol
Awareness for Rx Compliance Testing
2511|    Set this policy to enable the generation
and addition of PCIe margin data to the
2512|    BDAT table. Disabled(0x0)(Default): Normal
Operation - Disable non-protocol awareness,
2513|    Enable(0x1): Non-Protocol Awareness
```

```
        Enabled - Enable non-protocol awareness for
2514    compliance testing
2515    $EN_DIS
2516    */
2517    UINT8
2518    PegRxCemNonProtocolAwareness;
2519    /** Offset 0x053B - PCIe Override RxCTLE
2520        Disable(0x0)(Default): Normal Operation -
2521        RxCTLE adaptive behavior enabled, Enable(0x1):
2522        Override RxCTLE - Disable RxCTLE adaptive
2523        behavior to keep the configured RxCTLE
2524        peak values unmodified
2525        $EN_DIS
2526        */
2527        */
2528        UINT8
2529        PegGen3RxCtleOverride;
2530
2531    /** Offset 0x053C - Rsvd
2532        Disable(0x0)(Default): Normal Operation -
2533        RxCTLE adaptive behavior enabled, Enable(0x1):
2534        Override RxCTLE - Disable RxCTLE adaptive
2535        behavior to keep the configured RxCTLE
2536        peak values unmodified
2537        $EN_DIS
2538        */
2539        PegGen3Rsvd;
2540
2541    /** Offset 0x053D - PEG Gen3 Root port
2542        preset values per lane
2543        Used for programming PEG Gen3 preset
2544        values per lane. Range: 0-9, 8 is default for
2545        each lane
2546    */
2547    */
2548    UINT8
2549    PegGen3RootPortPreset[20];
2550
```

```
2540 /** Offset 0x0551 - PEG Gen3 End port preset
   values per lane
2541 Used for programming PEG Gen3 preset
   values per lane. Range: 0-9, 7 is default for
   each lane
2542 */
2543 UINT8
   PegGen3EndPointPreset[20];
2544
2545 /** Offset 0x0565 - PEG Gen3 End port Hint
   values per lane
2546 Used for programming PEG Gen3 Hint values
   per lane. Range: 0-6, 2 is default for each
   lane
2547 */
2548 UINT8
   PegGen3EndPointHint[20];
2549
2550 /** Offset 0x0579
2551 */
2552 UINT8
   UnusedUpdSpace8;
2553
2554 /** Offset 0x057A - Jitter Dwell Time for
   PCIe Gen3 Software Equalization
2555 Range: 0-65535, default is 1000. @warning
   Do not change from the default
2556 */
2557 UINT16
   Gen3SwEqJitterDwellTime;
2558
2559 /** Offset 0x057C - Jitter Error Target for
   PCIe Gen3 Software Equalization
2560 Range: 0-65535, default is 1. @warning Do
   not change from the default
2561 */
2562 UINT16
```

```
        Gen3SwEqJitterErrorTarget;
2563
2564 /** Offset 0x057E - VOC Dwell Time for PCIe
2565   Gen3 Software Equalization
2566   Range: 0-65535, default is 10000. @warning
2567   Do not change from the default
2568 */
2569     UINT16
2570     Gen3SwEqVocDwellTime;
2571
2572 /** Offset 0x0580 - VOC Error Target for
2573   PCIe Gen3 Software Equalization
2574   Range: 0-65535, default is 2. @warning Do
2575   not change from the default
2576 */
2577     UINT16
2578     Gen3SwEqVocErrorTarget;
2579
2580 /** Offset 0x0582 - Panel Power Enable
2581   Control for enabling/disabling VDD force
2582   bit (Required only for early enabling of
2583   eDP panel). 0=Disable, 1(Default)=Enable
2584   $EN_DIS
2585 */
2586     UINT8
2587     PanelPowerEnable;
2588
2589 /** Offset 0x0583 - BdatTestType
2590   Indicates the type of Memory Training data
2591   to populate into the BDAT ACPI table.
2592   0:Rank Margin Tool, 1:Margin2D
2593 */
2594     BdatTestType;
2595
2596
2597 /** Offset 0x0584 - SaPreMemTestRsvd
2598   Reserved for SA Pre-Mem Test
2599   $EN_DIS
```

```
2590  */
2591  UINT8
2592  SaPreMemTestRsvd[12];
2593 /**
2594  ** Offset 0x0590 - TotalFlashSize
2594  ** Enable/Disable. 0: Disable, define default
2594  ** value of TotalFlashSize , 1: enable
2595 */
2596  UINT16
2597  TotalFlashSize;
2598 /**
2599  ** Offset 0x0592 - BiosSize
2600  ** Enable/Disable. 0: Disable, define default
2600  ** value of BiosSize , 1: enable
2601 */
2602  UINT16
2603 /**
2604  ** Offset 0x0594 - TxtAcheckRequest
2604  ** Enable/Disable. When Enabled, it will
2604  ** forcing calling TXT Acheck once.
2605  $EN_DIS
2606 */
2607  UINT8
2608  TxtAcheckRequest;
2609 /**
2610  ** Offset 0x0595 - SecurityTestRsvd
2611  ** Reserved for SA Pre-Mem Test
2612  ** $EN_DIS
2613 */
2614  UINT8
2615  SecurityTestRsvd[3];
2616 /**
2617  ** Offset 0x0598 - Smbus dynamic power
2617  ** gating
2618  ** Disable or Enable Smbus dynamic power
2618  ** gating.
2619  ** $EN_DIS
```

```
2618 */  
2619     UINT8  
2620     SmbusDynamicPowerGating;  
2621 /** Offset 0x0599 - Disable and Lock Watch  
2622     Dog Register  
2623     Set 1 to clear WDT status, then disable  
2624     and lock WDT registers.  
2625     $EN_DIS  
2626 */  
2627     UINT8  
2628     WdtDisableAndLock;  
2629  
2630     /** Offset 0x059A - SMBUS SPD Write Disable  
2631     Set/Clear Smbus SPD Write Disable. 0:  
2632     leave SPD Write Disable bit; 1: set SPD Write  
2633     Disable bit. For security recommendations,  
2634     SPD write disable bit must be set.  
2635     $EN_DIS  
2636 */  
2637     UINT8  
2638     SmbusSpdWriteDisable;  
2639  
2640     /** Offset 0x059B - ChipsetInit HECI message  
2641     DEPRECATED  
2642     $EN_DIS  
2643 */  
2644     UINT8  
2645     ChipsetInitMessage;  
2646  
2647     /** Offset 0x059C - Bypass ChipsetInit sync  
2648     reset.  
2649     DEPRECATED  
2650     $EN_DIS  
2651 */  
2652     UINT8  
2653     BypassPhySyncReset;
```

```
2645
2646 /** Offset 0x059D - Force ME DID Init Status
2647     Test, 0: disable, 1: Success, 2: No Memory
2648     in Channels, 3: Memory Init Error, Set
2649         ME DID init stat value
2650         $EN_DIS
2651     */
2652         UINT8                               DidInitStat;
2653
2654 /** Offset 0x059E - CPU Replaced Polling
2655     Disable
2656     Test, 0: disable, 1: enable, Setting this
2657     option disables CPU replacement polling loop
2658         $EN_DIS
2659     */
2660         UINT8                               DisableCpuReplacedPolling;
2661
2662 /** Offset 0x059F - ME DID Message
2663     Test, 0: disable, 1: enable,
2664     Enable/Disable ME DID Message (disable will
2665     prevent
2666         the DID message from being sent)
2667         $EN_DIS
2668     */
2669         UINT8                               SendDidMsg;
2670
2671 /** Offset 0x05A0 - Retry mechanism for HECI
2672     APIs
2673     Test, 0: disable, 1: enable,
2674     Enable/Disable HECI retry.
2675         $EN_DIS
2676     */
2677         UINT8                               DisableHeciRetry;
2678
2679 /** Offset 0x05A1 - Check HECI message
```

```
    before send
2673 |     Test, 0: disable, 1: enable,
2674 |     Enable/Disable message check.
2674 |     $EN_DIS
2675 |     */
2676 |     UINT8
2676 |     DisableMessageCheck;
2677 |
2678 |     /** Offset 0x05A2 - Skip MBP HOB
2679 |     Test, 0: disable, 1: enable,
2679 |     Enable/Disable MOB HOB.
2680 |     $EN_DIS
2681 |     */
2682 |     UINT8                         SkipMbpHob;
2683 |
2684 |     /** Offset 0x05A3 - HECl2 Interface
2684 |     Communication
2685 |     Test, 0: disable, 1: enable, Adds or
2685 |     Removes HECl2 Device from PCI space.
2686 |     $EN_DIS
2687 |     */
2688 |     UINT8
2688 |     HeciCommunication2;
2689 |
2690 |     /** Offset 0x05A4 - Enable KT device
2691 |     Test, 0: disable, 1: enable, Enable or
2691 |     Disable KT device.
2692 |     $EN_DIS
2693 |     */
2694 |     UINT8
2694 |     KtDeviceEnable;
2695 |
2696 |     /** Offset 0x05A5 - tRd2RdSG
2697 |     Delay between Read-to-Read commands in the
2697 |     same Bank Group. 0-Auto, Range 4-54.
2698 |     */
2699 |     UINT8                         tRd2RdSG;
```

```
2700
2701 /** Offset 0x05A6 - tRd2RdDG
2702     Delay between Read-to-Read commands in
2703     different Bank Group for DDR4. All other
2704     DDR technologies should set this equal to
2705     SG. 0-Auto, Range 4-54.
2706 */
2707     UINT8                     tRd2RdDG;
2708
2709 /**
2710     UINT8                     tRd2RdDR;
2711
2712 /**
2713     Delay between Read-to-Read commands in
2714     different DIMMs. 0-Auto, Range 4-54.
2715 */
2716     UINT8                     tRd2RdDD;
2717
2718 /**
2719     Delay between Write-to-Read commands in
2720     the same Bank Group. 0-Auto, Range 4-86.
2721 */
2722 /**
2723     Delay between Write-to-Read commands in
2724     different Bank Group for DDR4. All other
2725     DDR technologies should set this equal to
2726     SG. 0-Auto, Range 4-54.
2727 */
2728 /**
2729     Delay between Write-to-Read commands in
```

```
    different Ranks. 0-Auto, Range 4-54.
2730  */
2731  UINT8                      tWr2RdDR;
2732
2733 /** Offset 0x05AC - tWr2RdDD
2734   Delay between Write-to-Read commands in
2735   different DIMMs. 0-Auto, Range 4-54.
2736 */
2737  UINT8                      tWr2RdDD;
2738
2739 /** Offset 0x05AD - tWr2WrSG
2740   Delay between Write-to-Write commands in
2741   the same Bank Group. 0-Auto, Range 4-54.
2742 */
2743 /**
2744   Delay between Write-to-Write commands in
2745   different Bank Group for DDR4. All other
2746   DDR technologies should set this equal to
2747   SG. 0-Auto, Range 4-54.
2748 */
2749 /**
2750   Delay between Write-to-Write commands in
2751   different Ranks. 0-Auto, Range 4-54.
2752 */
2753
2754 /**
2755   Delay between Write-to-Write commands in
2756   different DIMMs. 0-Auto, Range 4-54.
2757 */
2758
2759 /** Offset 0x05B1 - tRd2WrSG
```

```
2760    Delay between Read-to-Write commands in  
        the same Bank Group. 0-Auto, Range 4-54.  
2761    **/  
2762    UINT8                                tRd2WrSG;  
2763  
2764    /** Offset 0x05B2 - tRd2WrDG  
2765    Delay between Read-to-Write commands in  
        different Bank Group for DDR4. All other  
2766    DDR technologies should set this equal to  
        SG. 0-Auto, Range 4-54.  
2767    **/  
2768    UINT8                                tRd2WrDG;  
2769  
2770    /** Offset 0x05B3 - tRd2WrDR  
2771    Delay between Read-to-Write commands in  
        different Ranks. 0-Auto, Range 4-54.  
2772    **/  
2773    UINT8                                tRd2WrDR;  
2774  
2775    /** Offset 0x05B4 - tRd2WrDD  
2776    Delay between Read-to-Write commands in  
        different DIMMs. 0-Auto, Range 4-54.  
2777    **/  
2778    UINT8                                tRd2WrDD;  
2779  
2780    /** Offset 0x05B5 - tRRD_L  
2781    Min Row Active to Row Active Delay Time  
        for Same Bank Group, DDR4 Only. 0: AUTO, max:  
        31  
2782    **/  
2783    UINT8                                tRRD_L;  
2784  
2785    /** Offset 0x05B6 - tRRD_S  
2786    Min Row Active to Row Active Delay Time  
        for Different Bank Group, DDR4 Only. 0:  
        AUTO, max: 31  
2787  
2788    **/
```

```
2789     UINT8                               tRRD_S;
2790
2791 /** Offset 0x05B7 - tWTR_L
2792   Min Internal Write to Read Command Delay
2793   Time for Same Bank Group, DDR4 Only. 0:
2794   AUTO, max: 60
2795 */
2796     UINT8                               tWTR_L;
2797
2798 /** Offset 0x05B8 - tWTR_S
2799   Min Internal Write to Read Command Delay
2800   Time for Different Bank Group, DDR4 Only.
2801   0: AUTO, max: 28
2802 */
2803     UINT8                               tWTR_S;
2804
2805     UINT8
2806     ReservedFspmTestUpd[3];
2807 } FSP_M_TEST_CONFIG;
2808
2809 /** Fsp M UPD Configuration
2810 */
2811 typedef struct {
2812
2813 /** Offset 0x0000
2814 */
2815     FSP_UPD_HEADER                      FspUpdHeader;
2816
2817 /** Offset 0x0020
2818 */
2819     FSPM_ARCH_UPD                       FspmArchUpd;
2820
2821 /** Offset 0x0040
2822 */
2823     FSP_M_CONFIG FspmConfig;
```

```
2823
2824     /** Offset 0x051F
2825     */
2826     UINT8
2827     UnusedUpdSpace7;
2828
2829     /** Offset 0x0520
2830     */
2831     FSP_M_TEST_CONFIG FspmTestConfig;
2832
2833     /** Offset 0x05BC
2834     */
2835     UINT32                                UpdTerminator;
2836 } FSPM_UPD;
2837
2838 #pragma pack()
2839
2840#endif
```

---

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(FSP) Integration Guide by [doxygen](#) 1.8.10



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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Class List	Class Index	Class Members	

## DIMM\_INFO Member List

This is the complete list of members for **DIMM\_INFO**, including all inherited members.

DimmCapacity	<b>DIMM_INFO</b>
ModulePartNum	<b>DIMM_INFO</b>
RankInDimm	<b>DIMM_INFO</b>
SpdDramDeviceType	<b>DIMM_INFO</b>
SpdModuleMemoryBusWidth	<b>DIMM_INFO</b>
SpdModuleType	<b>DIMM_INFO</b>
SpdSave	<b>DIMM_INFO</b>
Speed	<b>DIMM_INFO</b>
Status	<b>DIMM_INFO</b>



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

Main Page

Related Pages

Classes

Files

File List

File Members

Include >

## MemInfoHob.h

Go to the documentation of this file.

```
1  /** @file
2   This file contains definitions required
3   for creation of
4   Memory S3 Save data, Memory Info data and
5   Memory Platform
6   data hobs.
7
8   @copyright
9   Copyright (c) 1999 - 2018, Intel
10  Corporation. All rights reserved.<BR>
11  This program and the accompanying
12  materials are licensed and made available
13  under
14  the terms and conditions of the BSD
15  License that accompanies this distribution.
16  The full text of the license may be found
17  at
18  http://opensource.org/licenses/bsd-
19  license.php.
20  THE PROGRAM IS DISTRIBUTED UNDER THE BSD
```

```
LICENSE ON AN "AS IS" BASIS,  
13  
14 WITHOUT WARRANTIES OR REPRESENTATIONS OF  
ANY KIND, EITHER EXPRESS OR IMPLIED.  
15  
16 @par Specification Reference:  
17 */
18 #ifndef _MEM_INFO_HOB_H_
19 #define _MEM_INFO_HOB_H_  
20
21 #include <Uefi/UefiMultiPhase.h>
22 #include <Pi/PiBootMode.h>
23 #include <Pi/PiHob.h>
24
25 #pragma pack (push, 1)
26
27 extern EFI_GUID gSiMemoryS3DataGuid;
28 extern EFI_GUID gSiMemoryInfoDataGuid;
29 extern EFI_GUID gSiMemoryPlatformDataGuid;
30
31 #define MAX_NODE          1
32 #define MAX_CH            2
33 #define MAX_DIMM          2
34
35 /**
36 /// Host reset states from MRC.
37 /**
38 #define WARM_BOOT         2
39
40 #define R_MC_CHNL_RANK_PRESENT 0x7C
41 #define B_RANK0_PRS        BIT0
42 #define B_RANK1_PRS        BIT1
43 #define B_RANK2_PRS        BIT4
44 #define B_RANK3_PRS        BIT5
45
46 /**
47 /// Defines taken from MRC so avoid having
```

```
    to include MrcInterface.h
48 ///
49 //
50 // Matches MAX_SPD_SAVE define in MRC
52 //
53 #ifndef MAX_SPD_SAVE
54 #define MAX_SPD_SAVE 29
55 #endif
56 //
57 // MRC version description.
58 //
59 //
60 typedef struct {
61     UINT8 Major;      ///< Major version
62     UINT8 Minor;     ///< Minor version
63     UINT8 Rev;       ///< Revision number
64     UINT8 Build;    ///< Build number
65 } SiMrcVersion;
66 //
67 // Matches MrcChannelSts enum in MRC
68 //
69 //
70 #ifndef CHANNEL_NOT_PRESENT
71 #define CHANNEL_NOT_PRESENT 0 // There
72     is no channel present on the controller.
73 #endif
74 #ifndef CHANNEL_DISABLED
75 #define CHANNEL_DISABLED 1 // There is
76     a channel present but it is disabled.
77 #endif
78 #ifndef CHANNEL_PRESENT
79 #define CHANNEL_PRESENT 2 // There is a
80     channel present and it is enabled.
81 #endif
```

```
79 //
80 // Matches MrcDimmSts enum in MRC
81 //
82 #ifndef DIMM_ENABLED
83 #define DIMM_ENABLED 0 // DIMM/rank
84     Pair is enabled, presence will be detected.
85 #endif
86 #ifndef DIMM_DISABLED
87 #define DIMM_DISABLED 1 // DIMM/rank
88     Pair is disabled, regardless of presence.
89 #endif
90 #ifndef DIMM_PRESENT
91 #define DIMM_PRESENT 2 // There is a
92     DIMM present in the slot/rank pair and it will
93     be used.
94 #endif
95
96 //
97 // Matches MrcBootMode enum in MRC
98 //
99 #ifndef bmCold
100 #define bmCold 0 // Cold boot
101 #endif
102 #ifndef bmWarm
103 #define bmWarm 1 // Warm boot
104 #endif
105 #ifndef bmS3
106 #define bmS3 2 // S3 resume
107 #endif
108 #ifndef bmFast
109 #define bmFast 3 // Fast boot
110 #endif
```

```
111 //
112 // 
113 // Matches MrcDdrType enum in MRC
114 //
115 #ifndef MRC_DDR_TYPE_DDR4
116 #define MRC_DDR_TYPE_DDR4      0
117 #endif
118 #ifndef MRC_DDR_TYPE_DDR3
119 #define MRC_DDR_TYPE_DDR3      1
120 #endif
121 #ifndef MRC_DDR_TYPE_LPDDR3
122 #define MRC_DDR_TYPE_LPDDR3    2
123 #endif
124 #ifndef CPU_CFL//CNL
125 #ifndef MRC_DDR_TYPE_LPDDR4
126 #define MRC_DDR_TYPE_LPDDR4    3
127 #endif
128 #else//CFL
129 #ifndef MRC_DDR_TYPE_UNKNOWN
130 #define MRC_DDR_TYPE_UNKNOWN   3
131 #endif
132 #endif//CPU_CFL-endif
133
134 #define MAX_PROFILE_NUM        4 // number of
     memory profiles supported
135 #define MAX_XMP_PROFILE_NUM   2 // number of
     XMP profiles supported
136
137 //
138 // DIMM timings
139 //
140 typedef struct {
141     UINT32 tCK;           ///< Memory cycle time,
     in femtoseconds.
142     UINT16 NMode;         ///< Number of tCK
     cycles for the channel DIMM's command rate
     mode.
```

```
143|     UINT16 tCL;           ///< Number of tCK  
cycles for the channel DIMM's CAS latency.  
144|     UINT16 tCWL;           ///< Number of tCK  
cycles for the channel DIMM's minimum CAS  
write latency time.  
145|     UINT16 tFAW;           ///< Number of tCK  
cycles for the channel DIMM's minimum four  
activate window delay time.  
146|     UINT16 tRAS;           ///< Number of tCK  
cycles for the channel DIMM's minimum active  
to precharge delay time.  
147|     UINT16 tRCDtRP;        ///< Number of tCK  
cycles for the channel DIMM's minimum RAS# to  
CAS# delay time and Row Precharge delay time.  
148|     UINT16 tREFI;          ///< Number of tCK  
cycles for the channel DIMM's minimum Average  
Periodic Refresh Interval.  
149|     UINT16 tRFC;           ///< Number of tCK  
cycles for the channel DIMM's minimum refresh  
recovery delay time.  
150|     UINT16 tRFCpb;         ///< Number of tCK  
cycles for the channel DIMM's minimum per bank  
refresh recovery delay time.  
151|     UINT16 tRFC2;          ///< Number of tCK  
cycles for the channel DIMM's minimum refresh  
recovery delay time.  
152|     UINT16 tRFC4;          ///< Number of tCK  
cycles for the channel DIMM's minimum refresh  
recovery delay time.  
153|     UINT16 tRPab;          ///< Number of tCK  
cycles for the channel DIMM's minimum row  
precharge delay time for all banks.  
154|     UINT16 tRRD;           ///< Number of tCK  
cycles for the channel DIMM's minimum row  
active to row active delay time.  
155|     UINT16 tRRD_L;         ///< Number of tCK  
cycles for the channel DIMM's minimum row
```

```
    active to row active delay time for same bank
    groups.

156|     UINT16 tRRD_S;      ///< Number of tCK
cycles for the channel DIMM's minimum row
active to row active delay time for different
bank groups.

157|     UINT16 tRTP;        ///< Number of tCK
cycles for the channel DIMM's minimum internal
read to precharge command delay time.

158|     UINT16 tWR;         ///< Number of tCK
cycles for the channel DIMM's minimum write
recovery time.

159|     UINT16 tWTR;        ///< Number of tCK
cycles for the channel DIMM's minimum internal
write to read command delay time.

160|     UINT16 tWTR_L;      ///< Number of tCK
cycles for the channel DIMM's minimum internal
write to read command delay time for same bank
groups.

161|     UINT16 tWTR_S;      ///< Number of tCK
cycles for the channel DIMM's minimum internal
write to read command delay time for different
bank groups.

162|     UINT16 tCCD_L;      ///< Number of tCK cycles
for the channel DIMM's minimum CAS-to-CAS
delay for same bank group.

163| } MRC_CH_TIMING;
164|
165| typedef struct {
166|     UINT8 SG;           ///< Number of tCK
cycles between transactions in the same bank
group.

167|     UINT8 DG;          ///< Number of tCK
cycles between transactions when switching
bank groups.

168|     UINT8 DR;          ///< Number of tCK
cycles between transactions when switching
```

```
    between Ranks (in the same DIMM).
169 |     UINT8 DD;           ///< Number of tCK
   |     cycles between transactions when switching
   |     between DIMMs.
170 | } MRC_TA_TIMING;
171 |
172 | /**
173 | /// Memory SMBIOS & OC Memory Data Hob
174 | /**
175 | typedef struct {
176 |     UINT8             Status;
   |     ///< See MrcDimmStatus for the definition of
   |     this field.
177 |     UINT8             DimmId;
178 |     UINT32            DimmCapacity;
   |     ///< DIMM size in MBytes.
179 |     UINT16            MfgId;
180 |     UINT8             ModulePartNum[20];
   |     ///< Module part number for DDR3 is 18 bytes
   |     however for DRR4 20 bytes as per JEDEC Spec,
   |     so reserving 20 bytes
181 |     UINT8             RankInDimm;
   |     ///< The number of ranks in this DIMM.
182 |     UINT8             SpdDramDeviceType;
   |     ///< Save SPD DramDeviceType information
   |     needed for SMBIOS structure creation.
183 |     UINT8             SpdModuleType;
   |     ///< Save SPD ModuleType information needed
   |     for SMBIOS structure creation.
184 |     UINT8             SpdModuleMemoryBusWidth;
   |     ///< Save SPD ModuleMemoryBusWidth information
   |     needed for SMBIOS structure creation.
185 |     UINT8             SpdSave[MAX_SPD_SAVE];
   |     ///< Save SPD Manufacturing information needed
   |     for SMBIOS structure creation.
186 |     UINT16            Speed;
   |     ///< The maximum capable speed of the device,
```

```

        in MHz.
187 } DIMM_INFO;
188
189 typedef struct {
190     UINT8             Status;
///< Indicates whether this channel should be
used.
191     UINT8             ChannelId;
192     UINT8             DimmCount;
///< Number of valid DIMMs that exist in the
channel.
193     MRC_CH_TIMING    Timing[MAX_PROFILE_NUM];
///< The channel timing values.
194     DIMM_INFO         DimmInfo[MAX_DIMM];
///< Save the DIMM output characteristics.
195     MRC_TA_TIMING   tRd2Rd;
///< Read-to-Read Turn Around Timings
196     MRC_TA_TIMING   tRd2Wr;
///< Read-to-Write Turn Around Timings
197     MRC_TA_TIMING   tWr2Rd;
///< Write-to-Read Turn Around Timings
198     MRC_TA_TIMING   tWr2Wr;
///< Write-to-Write Turn Around Timings
199 } CHANNEL_INFO;
200
201 typedef struct {
202     UINT8             Status;
///< Indicates whether this controller should
be used.
203     UINT16            DeviceId;
///< The PCI device id of this memory
controller.
204     UINT8             RevisionId;
///< The PCI revision id of this memory
controller.
205     UINT8             ChannelCount;
///< Number of valid channels that exist on

```

```
    the controller.

206 |     CHANNEL_INFO          ChannelInfo[MAX_CH];
    //;< The following are channel level
    definitions.

207 |     MRC_TA_TIMING      tRd2Rd;
    //;< Deprecated and moved to CHANNEL_INFO.
    Read-to-Read Turn Around Timings

208 |     MRC_TA_TIMING      tRd2Wr;
    //;< Deprecated and moved to CHANNEL_INFO.
    Read-to-Write Turn Around Timings

209 |     MRC_TA_TIMING      tWr2Rd;
    //;< Deprecated and moved to CHANNEL_INFO.
    Write-to-Read Turn Around Timings

210 |     MRC_TA_TIMING      tWr2Wr;
    //;< Deprecated and moved to CHANNEL_INFO.
    Write-to-Write Turn Around Timings

211 | } CONTROLLER_INFO;

212 |

213 | typedef struct {
214 |     UINT8                  Revision;
215 |     UINT16                 DataWidth;
    //;< Data width, in bits, of this memory
    device
216 |     /** As defined in SMBIOS 3.0 spec
217 |         Section 7.18.2 and Table 75
218 |     */
219 |     UINT8                  MemoryType;
    //;< DDR type: DDR3, DDR4, or LPDDR3
220 |     UINT16
        MaximumMemoryClockSpeed; //;< The maximum
        capable speed of the device, in megahertz
        (MHz)

221 |     UINT16
        ConfiguredMemoryClockSpeed; //;< The
        configured clock speed to the memory device,
        in megahertz (MHz)

222 |     /** As defined in SMBIOS 3.0 spec
```

```

223     Section 7.17.3 and Table 72
224     */
225     UINT8           ErrorCorrectionType;
226
227     SiMrcVersion    Version;
228     BOOLEAN         EccSupport;
229     UINT8           MemoryProfile;
230     UINT32          TotalPhysicalMemorySize;
231     UINT32
232     DefaultXmptCK[MAX_XMP_PROFILE_NUM]; //< Stores
233     //< the tCK value read from SPD XMP profiles if
234     //< they exist.
235     UINT8           XmpProfileEnable;
236     //< If XMP capable DIMMs are detected, this
237     //< will indicate which XMP Profiles are common
238     //< among all DIMMs.
239
240     UINT8           Ratio;
241     UINT8           RefClk;
242     UINT32
243     VddVoltage[MAX_PROFILE_NUM];
244     CONTROLLER_INFO Controller[MAX_NODE];
245 } MEMORY_INFO_DATA_HOB;
246
247 /**
248 * Memory Platform Data Hob
249 *
250 * <b>Revision 1:</b>
251 * - Initial version.
252 * <b>Revision 2:</b>
253 * - Added TsegBase, PrmrrSize, PrmrrBase,
254 *   Gtibase, MmioSize, PciEBaseAddress fields
255 */
256
257 typedef struct {
258     UINT8           Revision;
259     UINT8           Reserved[3];
260     UINT32          BootMode;
261     UINT32          TsegSize;

```

```

252     UINT32           TsegBase;
253     UINT32           PrmrrSize;
254     UINT32           PrmrrBase;
255     UINT32           GttBase;
256     UINT32           MmioSize;
257     UINT32           PciEBaseAddress;
258 #ifdef CPU_CFL
259     UINT32           GdxcIotBase;
260     UINT32           GdxcIotSize;
261     UINT32           GdxcMotBase;
262     UINT32           GdxcMotSize;
263 #endif //CPU_CFL
264 } MEMORY_PLATFORM_DATA;
265
266 typedef struct {
267     EFI_HOB_GUID_TYPE   EfiHobGuidType;
268     MEMORY_PLATFORM_DATA Data;
269     UINT8              *Buffer;
270 } MEMORY_PLATFORM_DATA_HOB;
271
272 #pragma pack (pop)
273
274 #endif // _MEM_INFO_H_

```



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## **FIRMWARE\_VERSION Member List**

This is the complete list of members for **FIRMWARE\_VERSION**, including all inherited members.

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## FirmwareVersionInfoHob.h

Go to the documentation of this file.

```
1  /** @file
2   Header file for Firmware Version
3   Information
4
5   @copyright
6   Copyright (c) 2015 - 2018, Intel
7   Corporation. All rights reserved.<BR>
8
9   This program and the accompanying
10  materials are licensed and made available
11  under
12  the terms and conditions of the BSD
13  License which accompanies this distribution.
14  The full text of the license may be found
15  at
16  http://opensource.org/licenses/bsd-
17  license.php
18
19  THE PROGRAM IS DISTRIBUTED UNDER THE BSD
20  LICENSE ON AN "AS IS" BASIS,
```

```
13 WITHOUT WARRANTIES OR REPRESENTATIONS OF
14 ANY KIND, EITHER EXPRESS OR IMPLIED.
15 /**
16
17 #ifndef _FIRMWARE_VERSION_INFO_HOB_H_
18 #define _FIRMWARE_VERSION_INFO_HOB_H_
19
20 #include <Uefi/UefiMultiPhase.h>
21 #include <Pi/PiBootMode.h>
22 #include <Pi/PiHob.h>
23
24 #pragma pack(1)
25 /**
26 /// Firmware Version Structure
27 /**
28 typedef struct {
29     UINT8
30         MajorVersion;
31     UINT8
32         MinorVersion;
33     UINT8
34             Revision;
35     UINT16
36         BuildNumber;
37 } FIRMWARE_VERSION;
38
39 /**
40 /// Firmware Version Information Structure
41 /**
42 typedef struct {
43     UINT8
44         ComponentNameIndex;           ///< Offset 0
45             Index of Component Name
46     UINT8
47         VersionStringIndex;         ///< Offset 1
48             Index of Version String
49 } FIRMWARE_VERSION Version;
```

```

    ///< Offset 2-6 Firmware version
42 } FIRMWARE_VERSION_INFO;
43
44 #ifndef __SMBIOS_STANDARD_H__
45 /**
46 /// The Smbios structure header.
47 /**
48 typedef struct {
49     UINT8                         Type;
50     UINT8                         Length;
51     UINT16                        Handle;
52 } SMBIOS_STRUCTURE;
53 #endif
54
55 /**
56 /// Firmware Version Information HOB
57 Structure
58 /**
59 typedef struct {
60     EFI_HOB_GUID_TYPE             Header;
61     //Offset 0-23 The header of FVI HOB
62     SMBIOS_STRUCTURE SmbiosData;
63     //Offset 24-27 The SMBIOS header of FVI
64     HOB
65     UINT8                         Count;
66     //Offset 28 Number of FVI elements
67     included.
68 /**
69 /// FIRMWARE_VERSION_INFO structures
70 followed by the null terminated string buffer
71 /**
72 } FIRMWARE_VERSION_INFO_HOB;
73 #pragma pack()
74
75 #endif // _FIRMWARE_VERSION_INFO_HOB_

```

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<b>VersionStringIndex</b>	<b>FIRMWARE_VERSION_INFO</b>

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# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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This is the complete list of members for [FSP\\_S\\_TEST\\_CONFIG](#), including all inherited members.

ApIdleManner	<a href="#">FSP_S_TEST_CONFIG</a>
AutoThermalReporting	<a href="#">FSP_S_TEST_CONFIG</a>
BiProcHot	<a href="#">FSP_S_TEST_CONFIG</a>
C1e	<a href="#">FSP_S_TEST_CONFIG</a>
C1StateAutoDemotion	<a href="#">FSP_S_TEST_CONFIG</a>
C1StateUnDemotion	<a href="#">FSP_S_TEST_CONFIG</a>
C3StateAutoDemotion	<a href="#">FSP_S_TEST_CONFIG</a>
C3StateUnDemotion	<a href="#">FSP_S_TEST_CONFIG</a>
CdynmaxClampEnable	<a href="#">FSP_S_TEST_CONFIG</a>
ChapDeviceEnable	<a href="#">FSP_S_TEST_CONFIG</a>
ConfigTdpBios	<a href="#">FSP_S_TEST_CONFIG</a>
ConfigTdpLevel	<a href="#">FSP_S_TEST_CONFIG</a>
ConfigTdpLock	<a href="#">FSP_S_TEST_CONFIG</a>
CpuWakeUpTimer	<a href="#">FSP_S_TEST_CONFIG</a>
CstateLatencyControl0Irtl	<a href="#">FSP_S_TEST_CONFIG</a>
CstateLatencyControl0TimeUnit	<a href="#">FSP_S_TEST_CONFIG</a>

CstateLatencyControl1Irtl	FSP_S_TEST_CONFIG
CstateLatencyControl1TimeUnit	FSP_S_TEST_CONFIG
CstateLatencyControl2Irtl	FSP_S_TEST_CONFIG
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Custom1PowerLimit1	FSP_S_TEST_CONFIG
Custom1PowerLimit1Time	FSP_S_TEST_CONFIG
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PchPmDisableEnergyReport	FSP_S_TEST_CONFIG
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PchSbiUnlock	FSP_S_TEST_CONFIG
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PcieRpNonSnoopLatencyOverrideMultiplier	FSP_S_TEST_CONFIG
PcieRpNonSnoopLatencyOverrideValue	FSP_S_TEST_CONFIG
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PcieRpSlotPowerLimitValue	FSP_S_TEST_CONFIG
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PcieRpSnoopLatencyOverrideMultiplier	FSP_S_TEST_CONFIG
PcieRpSnoopLatencyOverrideValue	FSP_S_TEST_CONFIG
PcieRpUptp	FSP_S_TEST_CONFIG
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PowerLimit1	FSP_S_TEST_CONFIG
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PowerLimit3	FSP_S_TEST_CONFIG

PowerLimit3DutyCycle	FSP_S_TEST_CONFIG
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PsysPowerLimit2	FSP_S_TEST_CONFIG
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<b>TccActivationOffset</b>	<b>FSP_S_TEST_CONFIG</b>
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<b>TccOffsetLock</b>	<b>FSP_S_TEST_CONFIG</b>
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<b>ThreeStrikeCounterDisable</b>	<b>FSP_S_TEST_CONFIG</b>
<b>TimedMwait</b>	<b>FSP_S_TEST_CONFIG</b>
<b>TStates</b>	<b>FSP_S_TEST_CONFIG</b>
<b>TurboPowerLimitLock</b>	<b>FSP_S_TEST_CONFIG</b>
<b>TwoCoreRatioLimit</b>	<b>FSP_S_TEST_CONFIG</b>
<b>UnusedUpdSpace24</b>	<b>FSP_S_TEST_CONFIG</b>
<b>VoltageOptimization</b>	<b>FSP_S_TEST_CONFIG</b>
<b>VtdDisable</b>	<b>FSP_S_TEST_CONFIG</b>

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(FSP) Integration Guide by  1.8.10



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## FSP\_T\_CONFIG Member List

This is the complete list of members for **FSP\_T\_CONFIG**, including all inherited members.

PcdPciExpressBaseAddress	<b>FSP_T_CONFIG</b>
PcdPciExpressRegionLength	<b>FSP_T_CONFIG</b>
PcdSerialIoUart0PinMuxing	<b>FSP_T_CONFIG</b>
PcdSerialIoUartDebugEnable	<b>FSP_T_CONFIG</b>
PcdSerialIoUartInputClock	<b>FSP_T_CONFIG</b>
PcdSerialIoUartNumber	<b>FSP_T_CONFIG</b>
ReservedFsptUpd1	<b>FSP_T_CONFIG</b>
UnusedUpdSpace0	<b>FSP_T_CONFIG</b>



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Include >

## FsptUpd.h

Go to the documentation of this file.

```
1  /** @file
2
3  Copyright (c) 2018, Intel Corporation. All
4  rights reserved.<BR>
5
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9  conditions are met:
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32 DATA, OR PROFITS; OR BUSINESS
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34 THEORY OF LIABILITY, WHETHER IN
35 CONTRACT, STRICT LIABILITY, OR TORT
36 (INCLUDING NEGLIGENCE OR OTHERWISE)
37 ARISING IN ANY WAY OUT OF THE USE OF THIS
38 SOFTWARE, EVEN IF ADVISED OF
39 THE POSSIBILITY OF SUCH DAMAGE.
40
41 This file is automatically generated.
42 Please do NOT modify !!!
43
44 */
45
46 #ifndef __FSPTUPD_H__
47 #define __FSPTUPD_H__
48
49
50 #include <FspUpd.h>
```

```
37
38 #pragma pack(1)
39
40
41 /** Fsp T Core UPD
42 */
43 typedef struct {
44
45     /** Offset 0x0020
46 */
47     UINT32
48         MicrocodeRegionBase;
49
50     /** Offset 0x0024
51 */
52     UINT32
53         MicrocodeRegionSize;
54
55     /** Offset 0x0028
56 */
57     UINT32
58         CodeRegionBase;
59
60     /** Offset 0x002C
61 */
62     UINT32
63         CodeRegionSize;
64 } FSPT_CORE_UPD;
65
66 /** Fsp T Configuration
67 */
68 typedef struct {
69
```

```
70  /** Offset 0x0040 -
    PcdSerialIoUartDebugEnable
71  Enable SerialIo Uart debug library
    with/without initializing SerialIo Uart device
    in FSP.
72  0:Disable, 1:Enable and Initialize,
    2:Enable without Initializing
73  */
74  UINT8
    PcdSerialIoUartDebugEnable;
75
76  /** Offset 0x0041 - PcdSerialIoUartNumber -
    FSPT
77  Select SerialIo Uart Controller for debug.
    Note: If UART0 is selected as CNVi BT
78  Core interface, it cannot be used for
    debug purpose.
79  0:SerialIoUart0, 1:SerialIoUart1,
    2:SerialIoUart2
80  */
81  UINT8
    PcdSerialIoUartNumber;
82
83  /** Offset 0x0042 -
    PcdSerialIoUart0PinMuxing - FSPT
84  Select SerialIo Uart0 pin muxing. Setting
    valid only if PcdSerialIoUartNumber is
85  set to UART0.
86  0:default pins, 1:pins muxed with
    CNV_BRI/RGI
87  */
88  UINT8
    PcdSerialIoUart0PinMuxing;
89
90  /** Offset 0x0043
91  */
92  UINT8
```

```
    UnusedUpdSpace0;
93 |    /** Offset 0x0044
94 |    */
95 |
96 |    UINT32
97 |    PcdSerialIoUartInputClock;
98 |    /** Offset 0x0048 - Pci Express Base Address
99 |     Base address to be programmed for Pci
100 |     Express
101 |    */
102 |    UINT64
103 |    PcdPciExpressBaseAddress;
104 |    /** Offset 0x0050 - Pci Express Region
105 |     Length
106 |     Region Length to be programmed for Pci
107 |     Express
108 |    */
109 |
110 |    UINT8
111 |    ReservedFsptUpd1[44];
112 |} FSP_T_CONFIG;
113 /**
114 */
115 typedef struct {
116
117 /** Offset 0x0000
118 */
119     FSP_UPD_HEADER           FspUpdHeader;
120
121 /** Offset 0x0020
```

```
122 */  
123     FSPT_CORE_UPD FsptCoreUpd;  
124  
125 /** Offset 0x0040  
126 **/  
127     FSP_T_CONFIG FsptConfig;  
128  
129 /** Offset 0x0080  
130 **/  
131     UINT16 UpdTerminator;  
132 } FSPT_UPD;  
133  
134 #pragma pack()  
135  
136 #endif
```



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## **FSPM\_UPD Member List**

This is the complete list of members for **FSPM\_UPD**, including all inherited members.

<a href="#">FspmArchUpd</a>	<b>FSPM_UPD</b>
<a href="#">FspmConfig</a>	<b>FSPM_UPD</b>
<a href="#">FspmTestConfig</a>	<b>FSPM_UPD</b>
<a href="#">FspUpdHeader</a>	<b>FSPM_UPD</b>
<a href="#">UnusedUpdSpace7</a>	<b>FSPM_UPD</b>
<a href="#">UpdTerminator</a>	<b>FSPM_UPD</b>



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## **FSPS\_UPD Member List**

This is the complete list of members for **FSPS\_UPD**, including all inherited members.

**FspsConfig** [FSPS\\_UPD](#)  
**FspsTestConfig** [FSPS\\_UPD](#)  
**FspUpdHeader** [FSPS\\_UPD](#)  
**UpdTerminator** [FSPS\\_UPD](#)



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## **FSPT\_CORE\_UPD Member List**

This is the complete list of members for **FSPT\_CORE\_UPD**, including all inherited members.

CodeRegionBase	<a href="#">FSPT_CORE_UPD</a>
CodeRegionSize	<a href="#">FSPT_CORE_UPD</a>
MicrocodeRegionBase	<a href="#">FSPT_CORE_UPD</a>
MicrocodeRegionSize	<a href="#">FSPT_CORE_UPD</a>
Reserved	<a href="#">FSPT_CORE_UPD</a>



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## **FSPT\_UPD Member List**

This is the complete list of members for **FSPT\_UPD**, including all inherited members.

<a href="#">FsptConfig</a>	<b><u>FSPT_UPD</u></b>
<a href="#">FsptCoreUpd</a>	<b><u>FSPT_UPD</u></b>
<a href="#">FspUpdHeader</a>	<b><u>FSPT_UPD</u></b>
<a href="#">UpdTerminator</a>	<b><u>FSPT_UPD</u></b>



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## GPIO\_CONFIG Member List

This is the complete list of members for **GPIO\_CONFIG**, including all inherited members.

Direction	GPIO_CONFIG
ElectricalConfig	GPIO_CONFIG
HostSoftPadOwn	GPIO_CONFIG
InterruptConfig	GPIO_CONFIG
LockConfig	GPIO_CONFIG
OtherSettings	GPIO_CONFIG
OutputState	GPIO_CONFIG
PadMode	GPIO_CONFIG
PowerConfig	GPIO_CONFIG
RsvdBits	GPIO_CONFIG



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Include >

## GpioConfig.h

Go to the documentation of this file.

```
1  /** @file
2   Header file for GpioConfig structure used
3   by GPIO library.
4
5  @copyright
6  Copyright (c) 2014 - 2017, Intel
7  Corporation. All rights reserved.<BR>
8  This program and the accompanying
9  materials are licensed and made available
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11 the terms and conditions of the BSD
12 License that accompanies this distribution.
13 The full text of the license may be found
14 at
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16 license.php.
17
18 THE PROGRAM IS DISTRIBUTED UNDER THE BSD
19 LICENSE ON AN "AS IS" BASIS,
20 WITHOUT WARRANTIES OR REPRESENTATIONS OF
```

```
    ANY KIND, EITHER EXPRESS OR IMPLIED.  
13  
14 @par Specification Reference:  
15 /**/  
16 #ifndef _GPIO_CONFIG_H_  
17 #define _GPIO_CONFIG_H_  
18  
19 #pragma pack(push, 1)  
20  
21 ////  
22 /// For any GpioPad usage in code use  
23     GPIO_PAD type  
24 ////  
25     typedef UINT32 GPIO_PAD;  
26  
27 ////  
28 /// For any GpioGroup usage in code use  
29     GPIO_GROUP type  
30 ////  
31     typedef UINT32 GPIO_GROUP;  
32 /**  
33     GPIO configuration structure used for pin  
34     programming.  
35     Structure contains fields that can be used  
36     to configure pad.  
37     **/  
38     typedef struct {  
39         /**  
40         Pad Mode  
41         Pad can be set as GPIO or one of its  
42             native functions.  
43         When in native mode setting Direction  
44             (except Inversion), OutputState,  
45             InterruptConfig, Host Software Pad  
46             Ownership and OutputStateLock are unnecessary.
```

```
42 |     Refer to definition of GPIO_PAD_MODE.
43 |     Refer to EDS for each native mode
44 |     according to the pad.
45 |     */
46 |     UINT32 PadMode          : 5;
47 |     /**
48 |     Host Software Pad Ownership
49 |     Set pad to ACPI mode or GPIO Driver Mode.
50 |     Refer to definition of GPIO_HOSTSW_OWN.
51 |     */
52 |     UINT32 HostSoftPadOwn   : 2;
53 |     /**
54 |     GPIO Direction
55 |     Can choose between In, In with inversion,
56 |     Out, both In and Out, both In with inversion
57 |     and out or disabling both.
58 |     Refer to definition of GPIO_DIRECTION for
59 |     supported settings.
60 |     */
61 |     UINT32 Direction        : 6;
62 |     /**
63 |     Output State
64 |     Set Pad output value.
65 |     Refer to definition of GPIO_OUTPUT_STATE
66 |     for supported settings.
67 |     This setting takes place when output is
68 |     enabled.
69 |     */
70 |     UINT32 OutputState       : 2;
71 |     /**
72 |     GPIO Interrupt Configuration
73 |     Set Pad to cause one of interrupts
74 |     (IOxAPIC/SCI/SMI/NMI).
75 |     This setting is applicable only if GPIO is
76 |     in GpioMode with input enabled.
77 |     Refer to definition of GPIO_INT_CONFIG for
78 |     supported settings.
```

```

70  */
71  UINT32 InterruptConfig      : 9;
72  /**
73  GPIO Power Configuration.
74  This setting controls Pad Reset
    Configuration.
75  Refer to definition of GPIO_RESET_CONFIG
    for supported settings.
76  */
77  UINT32 PowerConfig         : 8;
78  /**
79  GPIO Electrical Configuration
80  This setting controls pads termination.
81  Refer to definition of
    GPIO_ELECTRICAL_CONFIG for supported settings.
82  */
83  UINT32 ElectricalConfig   : 9;
84  /**
85  GPIO Lock Configuration
86  This setting controls pads lock.
87  Refer to definition of GPIO_LOCK_CONFIG
    for supported settings.
88  */
89  UINT32 LockConfig          : 4;
90  /**
91  Additional GPIO configuration
92  Refer to definition of GPIO_OTHER_CONFIG
    for supported settings.
93  */
94  UINT32 OtherSettings       : 9;
95  UINT32 RsvdBits            : 10;      ///<
    Reserved bits for future extension
96 } GPIO_CONFIG;
97
98
99 typedef enum {
100    GpioHardwareDefault        = 0x0      ///<

```

```

        Leave setting unmodified
101 } GPIO_HARDWARE_DEFAULT;
102
103 /**
104     GPIO Pad Mode
105     Refer to GPIO documentation on native
106     functions available for certain pad.
107     If GPIO is set to one of NativeX modes
108     then following settings are not applicable
109     and can be skipped:
110     - Interrupt related settings
111     - Host Software Ownership
112     - Output/Input enabling/disabling
113     - Output lock
114 */
115
116     typedef enum {
117         GpioPadModeGpio      = 0x1,
118         GpioPadModeNative1   = 0x3,
119         GpioPadModeNative2   = 0x5,
120         GpioPadModeNative3   = 0x7,
121         GpioPadModeNative4   = 0x9,
122         GpioPadModeNative5   = 0xB
123     } GPIO_PAD_MODE;
124
125 /**
126     Host Software Pad Ownership modes
127     This setting affects GPIO interrupt status
128     registers. Depending on chosen ownership
129     some GPIO Interrupt status register get
130     updated and other masked.
131
132     Please refer to EDS for HOSTSW_OWN
133     register description.
134 */
135
136     typedef enum {
137         GpioHostOwnDefault = 0x0,    ///< Leave
138         ownership value unmodified
139     /**

```

```

131    Set HOST ownership to ACPI.
132    Use this setting if pad is not going to be
133    used by GPIO OS driver.
134    If GPIO is configured to generate
135    SCI/SMI/NMI then this setting must be
136    used for interrupts to work
137    */
138    GpioHostOwnAcpi      = 0x1,
139    /**
140    Set HOST ownership to GPIO Driver mode.
141    Use this setting only if GPIO pad should
142    be controlled by GPIO OS Driver.
143    GPIO OS Driver will be able to control the
144    pad if appropriate entry in
145    ACPI exists (refer to ACPI specification
146    for GpioIo and GpioInt descriptors)
147    */
148    GpioHostOwnGpio      = 0x3
149 } GPIO_HOSTSW OWN;
150
151 /**
152 /// GPIO Direction
153 /**
154 typedef enum {
155     GpioDirDefault          = 0x0,
156     ///< Leave pad direction setting unmodified
157     GpioDirInOut            = (0x1 | (0x1 <<
158         3)), ///< Set pad for both output and input
159     GpioDirInInvOut          = (0x1 | (0x3 <<
160         3)), ///< Set pad for both output and input
161         with inversion
162     GpioDirIn                = (0x3 | (0x1 <<
163         3)), ///< Set pad for input only
164     GpioDirInInv              = (0x3 | (0x3 <<
165         3)), ///< Set pad for input with inversion
166     GpioDirOut                = 0x5,
167     ///< Set pad for output only

```

```

156 | GpioDirNone           = 0x7
    | //< Disable both output and input
157 | } GPIO_DIRECTION;
158 |
159 | /**
160 |   GPIO Output State
161 |   This field is relevant only if output is
162 |   enabled
163 | */
164 | typedef enum {
165 |   GpioOutDefault      = 0x0,  //< Leave
166 |   output value unmodified
167 |   GpioOutLow          = 0x1,  //< Set
168 |   output to low
169 |   GpioOutHigh         = 0x3  //< Set
170 |   output to high
171 | } GPIO_OUTPUT_STATE;
172 |
173 | /**
174 |   GPIO interrupt configuration
175 |   This setting is applicable only if pad is
176 |   in GPIO mode and has input enabled.
177 |   GPIO_INT_CONFIG allows to choose which
178 |   interrupt is generated (IOxAPIC/SCI/SMI/NMI)
179 |   and how it is triggered (edge or level).
180 |   Refer to PADCFG_DW0 register description in
181 |   EDS for details on this settings.
182 |   Field from GpioIntNmi to GpioIntApic can
183 |   be OR'ed with GpioIntLevel to GpioIntBothEdge
184 |   to describe an interrupt e.g. GpioIntApic
185 |   | GpioIntLevel
186 |   If GPIO is set to cause an SCI then also
187 |   GPI_GPE_EN is enabled for this pad.
188 |   If GPIO is set to cause an NMI then also
189 |   GPI_NMI_EN is enabled for this pad.
190 |   Not all GPIO are capable of generating an
191 |   SMI or NMI interrupt.

```

```

180 |     When routing GPIO to cause an IOxAPIC
181 |     interrupt care must be taken, as this
182 |     interrupt cannot be shared and its IRQn
183 |     number is not configurable.
184 |     Refer to EDS for GPIO pads IRQ numbers
185 |     (PADCFG_DW1.IntSel)
186 |     If GPIO is under GPIO OS driver control
187 |     and appropriate ACPI GpioInt descriptor
188 |     exist then use only trigger type setting
189 |     (from GpioIntLevel to GpioIntBothEdge).
190 |     This type of GPIO Driver interrupt doesn't
191 |     have any additional routing setting
192 |     required to be set by BIOS. Interrupt is
193 |     handled by GPIO OS Driver.
194 |
195 |     /**
196 |
197 |     typedef enum {
198 |         GpioIntDefault          = 0x0,    ///<-
199 |             Leave value of interrupt routing unmodified
200 |         GpioIntDis               = 0x1,    ///<-
201 |             Disable IOxAPIC/SCI/SMI/NMI interrupt
202 |             generation
203 |         GpioIntNmi               = 0x3,    ///<-
204 |             Enable NMI interrupt only
205 |         GpioIntSmi               = 0x5,    ///<-
206 |             Enable SMI interrupt only
207 |         GpioIntSci               = 0x9,    ///<-
208 |             Enable SCI interrupt only
209 |         GpioIntApic              = 0x11,   ///<-
210 |             Enable IOxAPIC interrupt only
211 |         GpioIntLevel              = (0x1 << 5), //-
212 |             Set interrupt as level triggered
213 |         GpioIntEdge               = (0x3 << 5), //-
214 |             Set interrupt as edge triggered (type of edge
215 |             depends on input inversion)
216 |         GpioIntLvlEdgDis          = (0x5 << 5), //-
217 |             Disable interrupt trigger

```

```

199 GpioIntBothEdge      = (0x7 << 5)  ///< Set
    interrupt as both edge triggered
200 } GPIO_INT_CONFIG;
201
202 #define B_GPIO_INT_CONFIG_INT_SOURCE_MASK
    0x1F ///< Mask for GPIO_INT_CONFIG for
    interrupt source
203 #define B_GPIO_INT_CONFIG_INT_TYPE_MASK
    0xE0 ///< Mask for GPIO_INT_CONFIG for
    interrupt type
204 /**
205  * GPIO Power Configuration
206  * GPIO_RESET_CONFIG allows to set GPIO Reset
207  * type (PADCCFG_DW0.PadRstCfg) which will
208  * be used to reset certain GPIO settings.
209  * Refer to EDS for settings that are
210  * controllable by PadRstCfg.
211 */
212 typedef enum {
213     GpioResetDefault      = 0x00,           ///<
    Leave value of pad reset unmodified
214     /**
215     Resume Reset (RSMRST)
216     GPP: PadRstCfg = 00b = "Powergood"
217     GPD: PadRstCfg = 11b = "Resume Reset"
218     Pad setting will reset on:
219     - DeepSx transition
220     - G3
221     Pad settings will not reset on:
222     - S3/S4/S5 transition
223     - Warm/Cold/Global reset
224     */
225     GpioResumeReset       = 0x01,
226     /**
227     Host Deep Reset
228     PadRstCfg = 01b = "Deep GPIO Reset"

```

```

228 Pad settings will reset on:
229 - Warm/Cold/Global reset
230 - DeepSx transition
231 - G3
232 Pad settings will not reset on:
233 - S3/S4/S5 transition
234 */
235 GpioHostDeepReset      = 0x03,
236 /**
237 Platform Reset (PLTRST)
238     PadRstCfg = 10b = "GPIO Reset"
239 Pad settings will reset on:
240 - S3/S4/S5 transition
241 - Warm/Cold/Global reset
242 - DeepSx transition
243 - G3
244 */
245 GpioPlatformReset      = 0x05,
246 /**
247 Deep Sleep Well Reset (DSW_PWROK)
248     GPP: not applicable
249     GPD: PadRstCfg = 00b = "Powergood"
250 Pad settings will reset on:
251 - G3
252 Pad settings will not reset on:
253 - S3/S4/S5 transition
254 - Warm/Cold/Global reset
255 - DeepSx transition
256 */
257 GpioDswReset          = 0x07
258 } GPIO_RESET_CONFIG;
259
260 /**
261 GPIO Electrical Configuration
262 Configuration options for GPIO termination
263 setting
264 */

```

```

264 | typedef enum {
265 |     GpioTermDefault          = 0x0,    ///<-
266 |     Leave termination setting unmodified
267 |     GpioTermNone            = 0x1,    ///<- none
268 |     GpioTermWpd5K           = 0x5,    ///<- 5kOhm
269 |     weak pull-down
270 |     GpioTermWpd20K          = 0x9,    ///<-
271 |     20kOhm weak pull-down
272 |     GpioTermWpu1K           = 0x13,   ///<- 1kOhm
273 |     weak pull-up
274 |     GpioTermWpu2K           = 0x17,   ///<- 2kOhm
275 |     weak pull-up
276 |     GpioTermWpu5K           = 0x15,   ///<- 5kOhm
277 |     weak pull-up
278 |     GpioTermWpu20K          = 0x19,   ///<-
279 |     20kOhm weak pull-up
280 |     GpioTermWpu1K2K          = 0x1B,   ///<- 1kOhm
281 |     & 2kOhm weak pull-up
282 |     /**
283 |     Native function controls pads termination
284 |     This setting is applicable only to some
285 |     native modes.
286 |     Please check EDS to determine which native
287 |     functionality
288 |     can control pads termination
289 |     */
290 |     GpioTermNative           = 0x1F
291 | } GPIO_ELECTRICAL_CONFIG;
292 |
293 #define
294     B_GPIO_ELECTRICAL_CONFIG_TERMINATION_MASK
295     0x1F    ///<- Mask for GPIO_ELECTRICAL_CONFIG
296     for termination value
297 |
298 /**
299     GPIO LockConfiguration
300     Set GPIO configuration lock and output

```

```
    state lock.  
288|  GpioPadConfigUnlock/Lock and  
     GpioOutputStateUnlock can be OR'ed.  
289|  By default GPIO pads will be locked unless  
     GPIO lib is explicitly  
290|  informed that certain pad is to be left  
     unlocked.  
291|  Lock settings reset is in Powergood  
     domain. Care must be taken when using this  
     setting  
292|  as fields it locks may be reset by a  
     different signal and can be controlled  
293|  by what is in GPIO_RESET_CONFIG  
     (PADCFG_DW0.PadRstCfg). GPIO library provides  
294|  functions which allow to unlock a GPIO  
     pad. If possible each GPIO lib function will  
     try to unlock  
295|  an already locked pad upon request for  
     reconfiguration  
296|  */
297|  typedef enum {
298|  /**
299|   Perform default action
300|   - if pad is an GPO, lock configuration
     but leave output unlocked
301|   - if pad is an GPI, lock everything
302|   - if pad is in native, lock everything
303|  */
304|  GpioLockDefault      = 0x0,
305|  GpioPadConfigUnlock = 0x3,  ///< Leave
     Pad configuration unlocked
306|  GpioPadConfigLock   = 0x1,  ///< Lock Pad
     configuration
307|  GpioOutputStateUnlock = 0xC,  ///< Leave
     Pad output control unlocked
308|  GpioPadUnlock       = 0xF,  ///< Leave
     both Pad configuration and output control
```

```

        unlocked
309 | GpioPadLock          = 0x5    ///< Lock
      both Pad configuration and output control
310 | } GPIO_LOCK_CONFIG;
311 |
312 | #define
      B_GPIO_LOCK_CONFIG_PAD_CONF_LOCK_MASK 0x3
      ///< Mask for GPIO_LOCK_CONFIG for Pad
      Configuration Lock
313 | #define B_GPIO_LOCK_CONFIG_OUTPUT_LOCK_MASK
      0xC   ///< Mask for GPIO_LOCK_CONFIG for Pad
      Output Lock
314 |
315 | /**
316 |     Other GPIO Configuration
317 |     GPIO_OTHER_CONFIG is used for less often
      settings and for future extensions
318 |     Supported settings:
319 |         - RX raw override to '1' - allows to
      override input value to '1'
320 |             This setting is applicable only if in
      input mode (both in GPIO and native usage).
321 |             The override takes place at the
      internal pad state directly from buffer and
      before the RXINV.
322 | */
323 | typedef enum {
324 |     GpioRxRaw1Default          = 0x0,  ///<
      Use default input override value
325 |     GpioRxRaw1Dis              = 0x1,  ///<
      Don't override input
326 |     GpioRxRaw1En              = 0x3  ///<
      Override input to '1'
327 | } GPIO_OTHER_CONFIG;
328 |
329 | #define B_GPIO_OTHER_CONFIG_RXRAW_MASK
      0x3   ///< Mask for GPIO_OTHER_CONFIG for

```

```
RxRaw1 setting
330
331 #pragma pack(pop)
332
333 #endif // _GPIO_CONFIG_H_
```

---

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## **HOB\_USAGE\_DATA\_HOB Member List**

This is the complete list of members for **HOB\_USAGE\_DATA\_HOB**, including all inherited members.

---

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Include >

## HobUsageDataHob.h

Go to the documentation of this file.

```
1  /** @file
2   Definitions for Hob Usage data HOB
3
4   @copyright
5   Copyright (c) 2017 - 2018, Intel
6   Corporation. All rights reserved.<BR>
7   This program and the accompanying
8   materials are licensed and made available
9   under
10  the terms and conditions of the BSD
11  License that accompanies this distribution.
12  The full text of the license may be found
13  at
14  http://opensource.org/licenses/bsd-
15  license.php.
16  THE PROGRAM IS DISTRIBUTED UNDER THE BSD
17  LICENSE ON AN "AS IS" BASIS,
18
19  WITHOUT WARRANTIES OR REPRESENTATIONS OF
20  ANY KIND, EITHER EXPRESS OR IMPLIED.
```

```

13
14 @par Specification Reference:
15 /**
16
17 #ifndef _HOB_USAGE_DATA_H_
18 #define _HOB_USAGE_DATA_H_
19
20 extern EFI_GUID gHobUsageDataGuid;
21
22 #pragma pack (push, 1)
23
24 /**
25   Hob Usage Data Hob
26
27   <b>Revision 1:</b>
28   - Initial version.
29 */
30 typedef struct {
31   EFI_PHYSICAL_ADDRESS EfiMemoryTop;
32   EFI_PHYSICAL_ADDRESS EfiMemoryBottom;
33   EFI_PHYSICAL_ADDRESS EfiFreeMemoryTop;
34   EFI_PHYSICAL_ADDRESS EfiFreeMemoryBottom;
35   UINTN               FreeMemory;
36 } HOB_USAGE_DATA_HOB;
37
38 #pragma pack (pop)
39
40#endif // _HOB_USAGE_DATA_H_

```



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## **MEMORY\_PLATFORM\_DATA Member List**

This is the complete list of members for **MEMORY\_PLATFORM\_DATA**, including all inherited members.

---

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<h2>SI_PCH_DEVICE_INTERRUPT_CONFIG Member List</h2>			

This is the complete list of members for [SI\\_PCH\\_DEVICE\\_INTERRUPT\\_CONFIG](#), including all inherited members.

Device    [SI\\_PCH\\_DEVICE\\_INTERRUPT\\_CONFIG](#)

Function    [SI\\_PCH\\_DEVICE\\_INTERRUPT\\_CONFIG](#)

IntX    [SI\\_PCH\\_DEVICE\\_INTERRUPT\\_CONFIG](#)

Irq    [SI\\_PCH\\_DEVICE\\_INTERRUPT\\_CONFIG](#)



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## SMBIOS\_CACHE\_INFO Member List

This is the complete list of members for **SMBIOS\_CACHE\_INFO**, including all inherited members.

Associativity	<a href="#">SMBIOS_CACHE_INFO</a>
CacheConfiguration	<a href="#">SMBIOS_CACHE_INFO</a>
CacheSpeed	<a href="#">SMBIOS_CACHE_INFO</a>
CurrentSramType	<a href="#">SMBIOS_CACHE_INFO</a>
ErrorCorrectionType	<a href="#">SMBIOS_CACHE_INFO</a>
InstalledSize	<a href="#">SMBIOS_CACHE_INFO</a>
InstalledSize2	<a href="#">SMBIOS_CACHE_INFO</a>
MaxCacheSize	<a href="#">SMBIOS_CACHE_INFO</a>
MaximumCacheSize2	<a href="#">SMBIOS_CACHE_INFO</a>
NumberOfCacheLevels	<a href="#">SMBIOS_CACHE_INFO</a>
SocketDesignationStrIndex	<a href="#">SMBIOS_CACHE_INFO</a>
SupportedSramType	<a href="#">SMBIOS_CACHE_INFO</a>
SystemCacheType	<a href="#">SMBIOS_CACHE_INFO</a>



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Include >

## SmbiosCacheInfoHob.h

Go to the documentation of this file.

```
1  /** @file
2   Header file for SMBIOS Cache Info HOB
3
4  @copyright
5  Copyright (c) 2015 - 2018, Intel
Corporation. All rights reserved.<BR>
6
7  This program and the accompanying
materials are licensed and made available
under
8  the terms and conditions of the BSD
License which accompanies this distribution.
9  The full text of the license may be found
at
10 http://opensource.org/licenses/bsd-
license.php
11
12 THE PROGRAM IS DISTRIBUTED UNDER THE BSD
LICENSE ON AN "AS IS" BASIS,
13 WITHOUT WARRANTIES OR REPRESENTATIONS OF
```

```
    ANY KIND, EITHER EXPRESS OR IMPLIED.  
14  
15     System Management BIOS (SMBIOS) Reference  
      Specification v3.1.0  
16     dated 2016-Nov-16 (DSP0134)  
17  
      http://www.dmtf.org/sites/default/files/standa  
      rds/documents/DSP0134_3.1.0.pdf  
18     **/  
19  
20 #ifndef _SMBIOS_CACHE_INFO_HOB_H_  
21 #define _SMBIOS_CACHE_INFO_HOB_H_  
22  
23 #include <Uefi.h>  
24 #include <Pi/PiHob.h>  
25  
26 #pragma pack(1)  
27 ///  
28 /// SMBIOS Cache Info HOB Structure  
29 ///  
30 typedef struct {  
31     UINT16      ProcessorSocketNumber;  
32     UINT16      NumberOfCacheLevels;  
    //;< Based on Number of Cache Types L1/L2/L3  
33     UINT8      SocketDesignationStrIndex;  
    //;< String Index in the string Buffer.  
    Example "L1-CACHE"  
34     UINT16      CacheConfiguration;  
    //;< Format defined in SMBIOS Spec v3.1  
    Section7.8 Table36  
35     UINT16      MaxCacheSize;  
    //;< Format defined in SMBIOS Spec v3.1  
    Section7.8.1  
36     UINT16      InstalledSize;  
    //;< Format defined in SMBIOS Spec v3.1  
    Section7.8.1  
37     UINT16      SupportedSramType;
```

```
    ///< Format defined in SMBIOS Spec v3.1
    Section7.8.2
38|     UINT16      CurrentSramType;
    ///< Format defined in SMBIOS Spec v3.1
    Section7.8.2
39|     UINT8       CacheSpeed;
    ///< Cache Speed in nanoseconds. 0 if speed is
    unknown.
40|     UINT8       ErrorCorrectionType;
    ///< ENUM Format defined in SMBIOS Spec v3.1
    Section 7.8.3
41|     UINT8       SystemCacheType;
    ///< ENUM Format defined in SMBIOS Spec v3.1
    Section 7.8.4
42|     UINT8       Associativity;
    ///< ENUM Format defined in SMBIOS Spec v3.1
    Section 7.8.5
43|     //
44|     // Add for smbios 3.1.0
45|     //
46|     UINT32      MaximumCacheSize2;
    ///< Format defined in SMBIOS Spec v3.1
    Section7.8.1
47|     UINT32      InstalledSize2;
    ///< Format defined in SMBIOS Spec v3.1
    Section7.8.1
48|     /**
49|     String Buffer - each string terminated by
        NULL "0x00"
50|     String buffer terminated by double NULL
        "0x0000"
51|     */
52| } SMBIOS_CACHE_INFO;
53| #pragma pack()
54|
55| #endif // _SMBIOS_CACHE_INFO_H_
```

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## SMBIOS\_PROCESSOR\_INFO Member List

This is the complete list of members for [SMBIOS\\_PROCESSOR\\_INFO](#), including all inherited members.

CoreCount	<a href="#">SMBIOS_PROCESSOR_INFO</a>
CurrentSpeedInMHz	<a href="#">SMBIOS_PROCESSOR_INFO</a>
EnabledCoreCount	<a href="#">SMBIOS_PROCESSOR_INFO</a>
ExternalClockInMHz	<a href="#">SMBIOS_PROCESSOR_INFO</a>
ProcessorCharacteristics	<a href="#">SMBIOS_PROCESSOR_INFO</a>
ProcessorFamily	<a href="#">SMBIOS_PROCESSOR_INFO</a>
ProcessorId	<a href="#">SMBIOS_PROCESSOR_INFO</a>
ProcessorManufacturerStrIndex	<a href="#">SMBIOS_PROCESSOR_INFO</a>
ProcessorType	<a href="#">SMBIOS_PROCESSOR_INFO</a>
ProcessorUpgrade	<a href="#">SMBIOS_PROCESSOR_INFO</a>
ProcessorVersionStrIndex	<a href="#">SMBIOS_PROCESSOR_INFO</a>
Status	<a href="#">SMBIOS_PROCESSOR_INFO</a>
ThreadCount	<a href="#">SMBIOS_PROCESSOR_INFO</a>
Voltage	<a href="#">SMBIOS_PROCESSOR_INFO</a>



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Include >

## SmbiosProcessorInfoHob.h

Go to the documentation of this file.

```
1  /** @file
2   Header file for SMBIOS Processor Info HOB
3
4  @copyright
5  Copyright (c) 2015 - 2018, Intel
6  Corporation. All rights reserved.<BR>
7  This program and the accompanying
8  materials are licensed and made available
9  under
10 the terms and conditions of the BSD
11 License that accompanies this distribution.
12 The full text of the license may be found
13 at
14 http://opensource.org/licenses/bsd-
15 license.php.
16
17 THE PROGRAM IS DISTRIBUTED UNDER THE BSD
18 LICENSE ON AN "AS IS" BASIS,
19 WITHOUT WARRANTIES OR REPRESENTATIONS OF
20 ANY KIND, EITHER EXPRESS OR IMPLIED.
```

```
13
14 System Management BIOS (SMBIOS) Reference
15 Specification v3.1.0
16 dated 2016-Nov-16 (DSP0134)
17 /**
18
19 #ifndef _SMBIOS_PROCESSOR_INFO_HOB_H_
20 #define _SMBIOS_PROCESSOR_INFO_HOB_H_
21
22 #include <Uefi.h>
23 #include <Pi/PiHob.h>
24
25 #pragma pack(1)
26 /**
27 /// SMBIOS Processor Info HOB Structure
28 /**
29 typedef struct {
30     UINT16      TotalNumberOfSockets;
31     UINT16      CurrentSocketNumber;
32     UINT8       ProcessorType;
33     /** This info is used for both
34      ProcessorFamily and ProcessorFamily2 fields
35      See ENUM defined in SMBIOS Spec v3.1
36      Section 7.5.2
37     */
38     UINT16      ProcessorFamily;
39     UINT8       ProcessorManufacturerStrIndex;
40     /**< Index of the String in the String Buffer
41     */
42     UINT64      ProcessorId;
43     /**< ENUM defined in SMBIOS Spec v3.1 Section
44     7.5.3
45     */
46     UINT8       ProcessorVersionStrIndex;
```

```
    ///< Index of the String in the String Buffer
40|     UINT8      Voltage;
    ///< Format defined in SMBIOS Spec v3.1
    Section 7.5.4
41|     UINT16      ExternalClockInMHz;
    ///< External Clock Frequency. Set to 0 if
    unknown.
42|     UINT16      CurrentSpeedInMHz;
    ///< Snapshot of current processor speed
    during boot
43|     UINT8      Status;
    ///< Format defined in the SMBIOS Spec v3.1
    Table 21
44|     UINT8      ProcessorUpgrade;
    ///< ENUM defined in SMBIOS Spec v3.1 Section
    7.5.5
45|     /** This info is used for both CoreCount &
    CoreCount2 fields
46|         See detailed description in SMBIOS
    Spec v3.1 Section 7.5.6
47|     */
48|     UINT16      CoreCount;
49|     /** This info is used for both CoreEnabled
    & CoreEnabled2 fields
50|         See detailed description in SMBIOS
    Spec v3.1 Section 7.5.7
51|     */
52|     UINT16      EnabledCoreCount;
53|     /** This info is used for both ThreadCount
    & ThreadCount2 fields
54|         See detailed description in SMBIOS
    Spec v3.1 Section 7.5.8
55|     */
56|     UINT16      ThreadCount;
57|     UINT16      ProcessorCharacteristics;
    ///< Format defined in SMBIOS Spec v3.1
    Section 7.5.9
```

```
58  /**
59   String Buffer - each string terminated by
60   NULL "0x00"
60   String buffer terminated by double NULL
60   "0x0000"
61 */
62 } SMBIOS_PROCESSOR_INFO;
63 #pragma pack()
64
65 #endif // _SMBIOS_PROCESSOR_INFO_H_
```

---

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## **SMBIOS\_STRUCTURE Member List**

This is the complete list of members for **SMBIOS\_STRUCTURE**, including all inherited members.

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## FspFixedPcds.h

Go to the documentation of this file.

```
1  /** @file
2
3  This file lists all FixedAtBuild PCDs
4  referenced in FSP integration guide.
5  Those value may vary in different FSP
6  revision to meet different requirements.
7
8  #ifndef __FSPFIXEDPCDS_H__
9  #define __FSPFIXEDPCDS_H__
10
11 #pragma pack(1)
12
13 #define PcdFspAreaBaseAddress 0xFFFF30000
14 //;< FspAreaBaseAddress
15 #define PcdFspImageIdString $CFLFSP$ //;<
16 FspImageIdString
17 #define PcdSiliconInitVersionMajor 0x07
18 //;< SiliconInitVersionMajor
19 #define PcdSiliconInitVersionMinor 0x00
20 //;< SiliconInitVersionMinor
```

```
17 #define PcdSiliconInitVersionRevision 0x3D
    ///< SiliconInitVersionRevision
18 #define PcdSiliconInitVersionBuild 0x60
    ///< SiliconInitVersionBuild
19 #define PcdGlobalDataPointerAddress
    0xFED00148  ///< GlobalDataPointerAddress
20 #define PcdTemporaryRamBase 0xFEF00000  ///<
    TemporaryRamBase
21 #define PcdTemporaryRamSize 0x00040000  ///<
    TemporaryRamSize
22 #define PcdFspReservedBufferSize 0x100  ///<
    FspReservedBufferSize
23 #pragma pack()
24
25 #endif
```

---

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Include >

## FsplInfoHob.h

Go to the documentation of this file.

```
1  /** @file
2   Header file for FSP Information HOB.
3
4  @copyright
5  Copyright (c) 2017 - 2018, Intel
6  Corporation. All rights reserved.<BR>
7  This program and the accompanying
8  materials are licensed and made available
9  under
10 the terms and conditions of the BSD
11 License that accompanies this distribution.
12 The full text of the license may be found
13 at
14 http://opensource.org/licenses/bsd-
15 license.php.
16 THE PROGRAM IS DISTRIBUTED UNDER THE BSD
17 LICENSE ON AN "AS IS" BASIS,
18 WITHOUT WARRANTIES OR REPRESENTATIONS OF
19 ANY KIND, EITHER EXPRESS OR IMPLIED.
20
21
```

```
13 @par Specification Reference:  
14 /**/  
15  
16 #ifndef _FSP_INFO_HOB_H_  
17 #define _FSP_INFO_HOB_H_  
18  
19 extern EFI_GUID gFspInfoGuid;  
20  
21 #pragma pack (push, 1)  
22  
23 typedef struct {  
24     UINT8           SiliconInitVersionMajor;  
25     UINT8           SiliconInitVersionMinor;  
26     UINT8           SiliconInitVersionRevision;  
27     UINT8           SiliconInitVersionBuild;  
28     UINT8           FspVersionRevision;  
29     UINT8           FspVersionBuild;  
30     UINT8           TimeStamp [12];  
31 } FSP_INFO_HOB;  
32  
33 #pragma pack (pop)  
34  
35 #endif // _FSP_INFO_HOB_H_
```



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## FspUpd.h

Go to the documentation of this file.

```
1  /** @file
2
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38 SOFTWARE, EVEN IF ADVISED OF
39 THE POSSIBILITY OF SUCH DAMAGE.
40
41 This file is automatically generated.
42 Please do NOT modify !!!
43
44 */
45
46 #ifndef __FSPUPD_H__
47 #define __FSPUPD_H__
48
49
50 #include <FspEas.h>
```

```
37
38 #pragma pack(1)
39
40 #define FSPT_UPD_SIGNATURE
41     0x545F4450554C4643 /* 'CFLUPD_T' */
42
43 #define FSPM_UPD_SIGNATURE
44     0x4D5F4450554C4643 /* 'CFLUPD_M' */
45
46 #pragma pack()
47
48 #endif
```



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

Main Page

Related Pages

Classes

Files

File List

File Members

Include >

## GpioSampleDef.h

Go to the documentation of this file.

```
1  /** @file
2   Sample enum definitions for GPIO table.
3
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8   materials are licensed and made available
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19  ANY KIND, EITHER EXPRESS OR IMPLIED.
20
21
```

```

13 @par Specification Reference:  

14 */
15  

16 #ifndef __GPIOCONFIG_H__  

17 #define __GPIOCONFIG_H__  

18 #include <FspUpd.h>  

19 #include <FspmUpd.h>  

20 #include <FspUpd.h>  

21  

22 /*
23     SKL LP GPIO pins
24     Use below for functions from PCH GPIO Lib
25     which
26         require GpioPad as argument. Encoding used
27         here
28         has all information required by library
29         functions
30 */
31  

32 #define GPIO_SKL_LP_GPP_A0          0x02000000  

33 #define GPIO_SKL_LP_GPP_A1          0x02000001  

34 #define GPIO_SKL_LP_GPP_A2          0x02000002  

35 #define GPIO_SKL_LP_GPP_A3          0x02000003  

36 #define GPIO_SKL_LP_GPP_A4          0x02000004  

37 #define GPIO_SKL_LP_GPP_A5          0x02000005  

38 #define GPIO_SKL_LP_GPP_A6          0x02000006  

39 #define GPIO_SKL_LP_GPP_A7          0x02000007  

40 #define GPIO_SKL_LP_GPP_A8          0x02000008  

41 #define GPIO_SKL_LP_GPP_A9          0x02000009  

42 #define GPIO_SKL_LP_GPP_A10         0x0200000A  

43 #define GPIO_SKL_LP_GPP_A11         0x0200000B  

44 #define GPIO_SKL_LP_GPP_A12         0x0200000C  

45 #define GPIO_SKL_LP_GPP_A13         0x0200000D  

46 #define GPIO_SKL_LP_GPP_A14         0x0200000E  

47 #define GPIO_SKL_LP_GPP_A15         0x0200000F  

48 #define GPIO_SKL_LP_GPP_A16         0x02000010  

49 #define GPIO_SKL_LP_GPP_A17         0x02000011  

50 #define GPIO_SKL_LP_GPP_A18         0x02000012

```

47	#define GPIO_SKL_LP_GPP_A19	0x02000013
48	#define GPIO_SKL_LP_GPP_A20	0x02000014
49	#define GPIO_SKL_LP_GPP_A21	0x02000015
50	#define GPIO_SKL_LP_GPP_A22	0x02000016
51	#define GPIO_SKL_LP_GPP_A23	0x02000017
52	#define GPIO_SKL_LP_GPP_B0	0x02010000
53	#define GPIO_SKL_LP_GPP_B1	0x02010001
54	#define GPIO_SKL_LP_GPP_B2	0x02010002
55	#define GPIO_SKL_LP_GPP_B3	0x02010003
56	#define GPIO_SKL_LP_GPP_B4	0x02010004
57	#define GPIO_SKL_LP_GPP_B5	0x02010005
58	#define GPIO_SKL_LP_GPP_B6	0x02010006
59	#define GPIO_SKL_LP_GPP_B7	0x02010007
60	#define GPIO_SKL_LP_GPP_B8	0x02010008
61	#define GPIO_SKL_LP_GPP_B9	0x02010009
62	#define GPIO_SKL_LP_GPP_B10	0x0201000A
63	#define GPIO_SKL_LP_GPP_B11	0x0201000B
64	#define GPIO_SKL_LP_GPP_B12	0x0201000C
65	#define GPIO_SKL_LP_GPP_B13	0x0201000D
66	#define GPIO_SKL_LP_GPP_B14	0x0201000E
67	#define GPIO_SKL_LP_GPP_B15	0x0201000F
68	#define GPIO_SKL_LP_GPP_B16	0x02010010
69	#define GPIO_SKL_LP_GPP_B17	0x02010011
70	#define GPIO_SKL_LP_GPP_B18	0x02010012
71	#define GPIO_SKL_LP_GPP_B19	0x02010013
72	#define GPIO_SKL_LP_GPP_B20	0x02010014
73	#define GPIO_SKL_LP_GPP_B21	0x02010015
74	#define GPIO_SKL_LP_GPP_B22	0x02010016
75	#define GPIO_SKL_LP_GPP_B23	0x02010017
76	#define GPIO_SKL_LP_GPP_C0	0x02020000
77	#define GPIO_SKL_LP_GPP_C1	0x02020001
78	#define GPIO_SKL_LP_GPP_C2	0x02020002
79	#define GPIO_SKL_LP_GPP_C3	0x02020003
80	#define GPIO_SKL_LP_GPP_C4	0x02020004
81	#define GPIO_SKL_LP_GPP_C5	0x02020005
82	#define GPIO_SKL_LP_GPP_C6	0x02020006
83	#define GPIO_SKL_LP_GPP_C7	0x02020007

84	#define GPIO_SKL_LP_GPP_C8	0x02020008
85	#define GPIO_SKL_LP_GPP_C9	0x02020009
86	#define GPIO_SKL_LP_GPP_C10	0x0202000A
87	#define GPIO_SKL_LP_GPP_C11	0x0202000B
88	#define GPIO_SKL_LP_GPP_C12	0x0202000C
89	#define GPIO_SKL_LP_GPP_C13	0x0202000D
90	#define GPIO_SKL_LP_GPP_C14	0x0202000E
91	#define GPIO_SKL_LP_GPP_C15	0x0202000F
92	#define GPIO_SKL_LP_GPP_C16	0x02020010
93	#define GPIO_SKL_LP_GPP_C17	0x02020011
94	#define GPIO_SKL_LP_GPP_C18	0x02020012
95	#define GPIO_SKL_LP_GPP_C19	0x02020013
96	#define GPIO_SKL_LP_GPP_C20	0x02020014
97	#define GPIO_SKL_LP_GPP_C21	0x02020015
98	#define GPIO_SKL_LP_GPP_C22	0x02020016
99	#define GPIO_SKL_LP_GPP_C23	0x02020017
100	#define GPIO_SKL_LP_GPP_D0	0x02030000
101	#define GPIO_SKL_LP_GPP_D1	0x02030001
102	#define GPIO_SKL_LP_GPP_D2	0x02030002
103	#define GPIO_SKL_LP_GPP_D3	0x02030003
104	#define GPIO_SKL_LP_GPP_D4	0x02030004
105	#define GPIO_SKL_LP_GPP_D5	0x02030005
106	#define GPIO_SKL_LP_GPP_D6	0x02030006
107	#define GPIO_SKL_LP_GPP_D7	0x02030007
108	#define GPIO_SKL_LP_GPP_D8	0x02030008
109	#define GPIO_SKL_LP_GPP_D9	0x02030009
110	#define GPIO_SKL_LP_GPP_D10	0x0203000A
111	#define GPIO_SKL_LP_GPP_D11	0x0203000B
112	#define GPIO_SKL_LP_GPP_D12	0x0203000C
113	#define GPIO_SKL_LP_GPP_D13	0x0203000D
114	#define GPIO_SKL_LP_GPP_D14	0x0203000E
115	#define GPIO_SKL_LP_GPP_D15	0x0203000F
116	#define GPIO_SKL_LP_GPP_D16	0x02030010
117	#define GPIO_SKL_LP_GPP_D17	0x02030011
118	#define GPIO_SKL_LP_GPP_D18	0x02030012
119	#define GPIO_SKL_LP_GPP_D19	0x02030013
120	#define GPIO_SKL_LP_GPP_D20	0x02030014

121	#define GPIO_SKL_LP_GPP_D21	0x02030015
122	#define GPIO_SKL_LP_GPP_D22	0x02030016
123	#define GPIO_SKL_LP_GPP_D23	0x02030017
124	#define GPIO_SKL_LP_GPP_E0	0x02040000
125	#define GPIO_SKL_LP_GPP_E1	0x02040001
126	#define GPIO_SKL_LP_GPP_E2	0x02040002
127	#define GPIO_SKL_LP_GPP_E3	0x02040003
128	#define GPIO_SKL_LP_GPP_E4	0x02040004
129	#define GPIO_SKL_LP_GPP_E5	0x02040005
130	#define GPIO_SKL_LP_GPP_E6	0x02040006
131	#define GPIO_SKL_LP_GPP_E7	0x02040007
132	#define GPIO_SKL_LP_GPP_E8	0x02040008
133	#define GPIO_SKL_LP_GPP_E9	0x02040009
134	#define GPIO_SKL_LP_GPP_E10	0x0204000A
135	#define GPIO_SKL_LP_GPP_E11	0x0204000B
136	#define GPIO_SKL_LP_GPP_E12	0x0204000C
137	#define GPIO_SKL_LP_GPP_E13	0x0204000D
138	#define GPIO_SKL_LP_GPP_E14	0x0204000E
139	#define GPIO_SKL_LP_GPP_E15	0x0204000F
140	#define GPIO_SKL_LP_GPP_E16	0x02040010
141	#define GPIO_SKL_LP_GPP_E17	0x02040011
142	#define GPIO_SKL_LP_GPP_E18	0x02040012
143	#define GPIO_SKL_LP_GPP_E19	0x02040013
144	#define GPIO_SKL_LP_GPP_E20	0x02040014
145	#define GPIO_SKL_LP_GPP_E21	0x02040015
146	#define GPIO_SKL_LP_GPP_E22	0x02040016
147	#define GPIO_SKL_LP_GPP_E23	0x02040017
148	#define GPIO_SKL_LP_GPP_F0	0x02050000
149	#define GPIO_SKL_LP_GPP_F1	0x02050001
150	#define GPIO_SKL_LP_GPP_F2	0x02050002
151	#define GPIO_SKL_LP_GPP_F3	0x02050003
152	#define GPIO_SKL_LP_GPP_F4	0x02050004
153	#define GPIO_SKL_LP_GPP_F5	0x02050005
154	#define GPIO_SKL_LP_GPP_F6	0x02050006
155	#define GPIO_SKL_LP_GPP_F7	0x02050007
156	#define GPIO_SKL_LP_GPP_F8	0x02050008
157	#define GPIO_SKL_LP_GPP_F9	0x02050009

158	#define GPIO_SKL_LP_GPP_F10	0x0205000A
159	#define GPIO_SKL_LP_GPP_F11	0x0205000B
160	#define GPIO_SKL_LP_GPP_F12	0x0205000C
161	#define GPIO_SKL_LP_GPP_F13	0x0205000D
162	#define GPIO_SKL_LP_GPP_F14	0x0205000E
163	#define GPIO_SKL_LP_GPP_F15	0x0205000F
164	#define GPIO_SKL_LP_GPP_F16	0x02050010
165	#define GPIO_SKL_LP_GPP_F17	0x02050011
166	#define GPIO_SKL_LP_GPP_F18	0x02050012
167	#define GPIO_SKL_LP_GPP_F19	0x02050013
168	#define GPIO_SKL_LP_GPP_F20	0x02050014
169	#define GPIO_SKL_LP_GPP_F21	0x02050015
170	#define GPIO_SKL_LP_GPP_F22	0x02050016
171	#define GPIO_SKL_LP_GPP_F23	0x02050017
172	#define GPIO_SKL_LP_GPP_G0	0x02060000
173	#define GPIO_SKL_LP_GPP_G1	0x02060001
174	#define GPIO_SKL_LP_GPP_G2	0x02060002
175	#define GPIO_SKL_LP_GPP_G3	0x02060003
176	#define GPIO_SKL_LP_GPP_G4	0x02060004
177	#define GPIO_SKL_LP_GPP_G5	0x02060005
178	#define GPIO_SKL_LP_GPP_G6	0x02060006
179	#define GPIO_SKL_LP_GPP_G7	0x02060007
180	#define GPIO_SKL_LP_GPD0	0x02070000
181	#define GPIO_SKL_LP_GPD1	0x02070001
182	#define GPIO_SKL_LP_GPD2	0x02070002
183	#define GPIO_SKL_LP_GPD3	0x02070003
184	#define GPIO_SKL_LP_GPD4	0x02070004
185	#define GPIO_SKL_LP_GPD5	0x02070005
186	#define GPIO_SKL_LP_GPD6	0x02070006
187	#define GPIO_SKL_LP_GPD7	0x02070007
188	#define GPIO_SKL_LP_GPD8	0x02070008
189	#define GPIO_SKL_LP_GPD9	0x02070009
190	#define GPIO_SKL_LP_GPD10	0x0207000A
191	#define GPIO_SKL_LP_GPD11	0x0207000B
192		
193	#define END_OF_GPIO_TABLE	0xFFFFFFFF
194		

```
195 //Sample GPIO Table
196
197 static GPIO_INIT_CONFIG
    mGpioTableLpDdr3Rvp3[] =
198 {
199 //skip for eSPI function
    {GPIO_SKL_LP_GPP_A0, {GpioPadModeNative1,
        GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
        GpioIntDis, GpioHostDeepReset,
        GpioTermNone}},//H_RCIN_N
200 //skip for eSPI function
    {GPIO_SKL_LP_GPP_A1, {GpioPadModeNative1,
        GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
        GpioIntDis, GpioHostDeepReset,
        GpioTermWpd20K}},//LPC_AD0_ESPI_I00
201 //skip for eSPI function
    {GPIO_SKL_LP_GPP_A2, {GpioPadModeNative1,
        GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
        GpioIntDis, GpioHostDeepReset,
        GpioTermWpd20K}},//LPC_AD1_ESPI_I01
202 //skip for eSPI function
    {GPIO_SKL_LP_GPP_A3, {GpioPadModeNative1,
        GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
        GpioIntDis, GpioHostDeepReset,
        GpioTermWpd20K}},//LPC_AD2_ESPI_I02
203 //skip for eSPI function
    {GPIO_SKL_LP_GPP_A4, {GpioPadModeNative1,
        GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
        GpioIntDis, GpioHostDeepReset,
        GpioTermWpd20K}},//LPC_AD3_ESPI_I03
204 //skip for eSPI function
    {GPIO_SKL_LP_GPP_A5, {GpioPadModeNative1,
        GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
        GpioIntDis, GpioHostDeepReset,
        GpioTermNone}},//LPC_FRAME_ESPI_CS_N
205 //skip for eSPI function
    {GPIO_SKL_LP_GPP_A6, {GpioPadModeNative1,
```

```
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}}},//INT_SERIRQ
206| //skip for eSPI function
{GPIO_SKL_LP_GPP_A7, {GpioPadModeGpio,
GpioHostOwnGpio, GpioDirOut, GpioOutHigh,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}},//PM_SLP_S0ix_R_N
207| {GPIO_SKL_LP_GPP_A8, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}},//PM_CLKRUN_N
208| //skip for eSPI function
{GPIO_SKL_LP_GPP_A9, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermWpd20K}},//LPC_CLK_ESPI_CLK
209| {GPIO_SKL_LP_GPP_A10, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermWpd20K}},//PCH_CLK_PCI TPM
210| {GPIO_SKL_LP_GPP_A11, {GpioPadModeGpio,
GpioHostOwnGpio, GpioDirIn, GpioOutDefault,
GpioIntLevel | GpioIntApic, GpioHostDeepReset,
GpioTermNone}},//EC_HID_INTR
211| {GPIO_SKL_LP_GPP_A12, {GpioPadModeGpio,
GpioHostOwnGpio, GpioDirOut, GpioOutHigh,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}},//M.2_WWAN_GNSS_UART_RST_N
212| {GPIO_SKL_LP_GPP_A13, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}},//SUS_PWR_ACK_R
213| //skip for eSPI function
{GPIO_SKL_LP_GPP_A14, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
```

```
    GpioTermNone}}, //PM_SUS_STAT_ESPI_RST_N
214| {GPIO_SKL_LP_GPP_A15, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermWpd20K}}, //SUSACK_R_N
215| {GPIO_SKL_LP_GPP_A16, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirIn, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SD_1P8_SEL
216| {GPIO_SKL_LP_GPP_A17, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SD_PWR_EN_N
217| {GPIO_SKL_LP_GPP_A18, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //ISH_GP_0_SENSOR
218| {GPIO_SKL_LP_GPP_A19, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //ISH_GP_1_SENSOR
219| {GPIO_SKL_LP_GPP_A20, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //ISH_GP_2_SENSOR
220| {GPIO_SKL_LP_GPP_A21, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //GNSS_CHUB_IRQ
221| {GPIO_SKL_LP_GPP_A22, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirOut, GpioOutHigh,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //FPS_SLP_N
222| {GPIO_SKL_LP_GPP_A23, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirIn, GpioOutDefault,
    GpioIntLevel | GpioIntApic, GpioHostDeepReset,
    GpioTermNone}}, //FPS_DRDY
```

```
223 {GPIO_SKL_LP_GPP_B0, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//V0.85A_VID0
224 {GPIO_SKL_LP_GPP_B1, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//V0.85A_VID1
225 {GPIO_SKL_LP_GPP_B2, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//GP_VRALERTB
226 {GPIO_SKL_LP_GPP_B3, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirIn, GpioOutDefault,
    GpioIntLevel | GpioIntApic, GpioPlatformReset,
    GpioTermNone}},//TCH_PAD_INTR_R_N
227 {GPIO_SKL_LP_GPP_B4, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirOut, GpioOutHigh,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//BT_RF_KILL_N
228 {GPIO_SKL_LP_GPP_B5, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirIn, GpioOutDefault,
    GpioIntLevel | GpioIntApic, GpioHostDeepReset,
    GpioTermNone}},//M.2_BT_UART_WAKE_N
229 // {GPIO_SKL_LP_GPP_B6,
{GpioPadModeNative1, GpioHostOwnGpio,
    GpioDirNone, GpioOutDefault, GpioIntDis,
    GpioHostDeepReset,
    GpioTermNone}},//CLK_REQ_SLOT1_N
230 // {GPIO_SKL_LP_GPP_B7,
{GpioPadModeNative1, GpioHostOwnGpio,
    GpioDirNone, GpioOutDefault, GpioIntDis,
    GpioHostDeepReset,
    GpioTermNone}},//CLK_REQ_SLOT2_LAN_N
231 // {GPIO_SKL_LP_GPP_B8,
{GpioPadModeNative1, GpioHostOwnGpio,
    GpioDirNone, GpioOutDefault, GpioIntDis,
```

```
GpioHostDeepReset,
GpioTermNone}}},//CLK_REQ_M.2_SSD_SLOT3_N
232| {GPIO_SKL_LP_GPP_B9,
{GpioPadModeNative1, GpioHostOwnGpio,
GpioDirNone, GpioOutDefault, GpioIntDis,
GpioHostDeepReset,
GpioTermNone}}},//CLK_REQ_M.2_WIGIG_N
233| {GPIO_SKL_LP_GPP_B10,
{GpioPadModeNative1, GpioHostOwnGpio,
GpioDirNone, GpioOutDefault, GpioIntDis,
GpioHostDeepReset,
GpioTermNone}}},//CLK_REQ_M.2_WLAN_N
234| {GPIO_SKL_LP_GPP_B11, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}}},//MPHY_EXT_PWR_GATEB
235| {GPIO_SKL_LP_GPP_B12, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}}},//PCH_SLP_S0_N
236| {GPIO_SKL_LP_GPP_B13, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}}},//PLT_RST_N
237| {GPIO_SKL_LP_GPP_B14, {GpioPadModeGpio,
GpioHostOwnGpio, GpioDirOut, GpioOutHigh,
GpioIntDis, GpioHostDeepReset,
GpioTermWpd20K}}},//TCH_PNL_PWREN
238| {GPIO_SKL_LP_GPP_B15, {GpioPadModeGpio,
GpioHostOwnGpio, GpioDirOut, GpioOutLow,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}}},//PCH_NFC_DFU
239| {GPIO_SKL_LP_GPP_B16, {GpioPadModeGpio,
GpioHostOwnAcpi, GpioDirInInv, GpioOutDefault,
GpioIntLevel | GpioIntSci, GpioPlatformReset,
GpioTermNone}}},//M.2_WLAN_WIFI_WAKE_N
240| {GPIO_SKL_LP_GPP_B17, {GpioPadModeGpio,
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    GpioHostOwnAcpi, GpioDirInInv, GpioOutDefault,
    GpioIntEdge | GpioIntSci, GpioHostDeepReset,
    GpioTermWpd20K}}, //TBT_CIO_PLUG_EVENT_N
241| {GPIO_SKL_LP_GPP_B18, {GpioPadModeGpio,
    GpioHostOwnAcpi, GpioDirInInv, GpioOutDefault,
    GpioIntLevel | GpioIntSci, GpioPlatformReset,
    GpioTermWpu20K}}, //PCH_SLOT1_WAKE_N
242| {GPIO_SKL_LP_GPP_B19, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //FPS_GSPI1_CS_R1_N
243| {GPIO_SKL_LP_GPP_B20, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermWpd20K}}, //FPS_GSPI1_CLK_R1
244| {GPIO_SKL_LP_GPP_B21, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermWpd20K}}, //FPS_GSPI1_MISO_R1
245| {GPIO_SKL_LP_GPP_B22, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermWpd20K}}, //FPS_GSPI1_MOSI_R1
246| {GPIO_SKL_LP_GPP_B23, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirOut, GpioOutHigh,
    GpioIntDis, GpioHostDeepReset,
    GpioTermWpd20K}}, //DISCRETE_GNSS_RESET_N
247| {GPIO_SKL_LP_GPP_C0, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SMB_CLK
248| {GPIO_SKL_LP_GPP_C1, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermWpd20K}}, //SMB_DATA
249| {GPIO_SKL_LP_GPP_C2, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirOut, GpioOutHigh,
```

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    GpioIntDis, GpioHostDeepReset,
    GpioTermWpd20K}}, //SKIN_THRM_SNSR_ALERT_N
250| {GPIO_SKL_LP_GPP_C3, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SML0_CLK
251| {GPIO_SKL_LP_GPP_C4, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SML0_DATA
252| {GPIO_SKL_LP_GPP_C5, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirInInv, GpioOutDefault,
    GpioIntLevel | GpioIntApic, GpioHostDeepReset,
    GpioTermWpd20K}}, //M.2_WIGIG_WAKE_N
253| {GPIO_SKL_LP_GPP_C6, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SML1_CLK
254| {GPIO_SKL_LP_GPP_C7, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermWpd20K}}, //SML1_DATA
255| {GPIO_SKL_LP_GPP_C8, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SERIALIO_UART0_RXD
256| {GPIO_SKL_LP_GPP_C9, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SERIALIO_UART0_TXD
257| {GPIO_SKL_LP_GPP_C10, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SERIALIO_UART0_RTS_N
258| {GPIO_SKL_LP_GPP_C11, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
```

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        GpioTermNone}}},//SERIALIO_UART0_CTS_N  
259| {GPIO_SKL_LP_GPP_C12, {GpioPadModeNative1,  
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,  
    GpioIntDis, GpioHostDeepReset,  
    GpioTermNone}}},//SERIALIO_UART1_ISH_UART1_RXD  
260| {GPIO_SKL_LP_GPP_C13, {GpioPadModeNative1,  
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,  
    GpioIntDis, GpioHostDeepReset,  
    GpioTermNone}}},//SERIALIO_UART1_ISH_UART1_TXD  
261| {GPIO_SKL_LP_GPP_C14, {GpioPadModeNative1,  
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,  
    GpioIntDis, GpioHostDeepReset,  
    GpioTermNone}}},//SERIALIO_UART1_ISH_UART1_RTS_  
N  
262| {GPIO_SKL_LP_GPP_C15, {GpioPadModeNative1,  
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,  
    GpioIntDis, GpioHostDeepReset,  
    GpioTermNone}}},//SERIALIO_UART1_ISH_UART1_CTS_  
N  
263| {GPIO_SKL_LP_GPP_C16, {GpioPadModeNative1,  
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,  
    GpioIntDis, GpioHostDeepReset,  
    GpioTermNone}}},//SERIALIO_I2C0_SDA  
264| {GPIO_SKL_LP_GPP_C17, {GpioPadModeNative1,  
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,  
    GpioIntDis, GpioHostDeepReset,  
    GpioTermNone}}},//SERIALIO_I2C0_SCL  
265| {GPIO_SKL_LP_GPP_C18, {GpioPadModeNative1,  
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,  
    GpioIntDis, GpioHostDeepReset,  
    GpioTermNone}}},//SERIALIO_I2C1_SDA  
266| {GPIO_SKL_LP_GPP_C19, {GpioPadModeNative1,  
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,  
    GpioIntDis, GpioHostDeepReset,  
    GpioTermNone}}},//SERIALIO_I2C1_SCL  
267| {GPIO_SKL_LP_GPP_C20, {GpioPadModeNative1,  
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
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    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SERIALIO_UART2_RXD
268| {GPIO_SKL_LP_GPP_C21, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SERIALIO_UART2_RXD
269| {GPIO_SKL_LP_GPP_C22, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SERIALIO_UART2_RTS_N
270| {GPIO_SKL_LP_GPP_C23, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SERIALIO_UART2_CTS_N
271| {GPIO_SKL_LP_GPP_D0, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SPI1_TCHPNL_CS_N
272| {GPIO_SKL_LP_GPP_D1, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SPI1_TCHPNL_CLK
273| {GPIO_SKL_LP_GPP_D2, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SPI1_TCHPNL_MISO
274| {GPIO_SKL_LP_GPP_D3, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SPI1_TCHPNL_MOSI
275| {GPIO_SKL_LP_GPP_D4, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//CSI2_FLASH_STROBE
276| {GPIO_SKL_LP_GPP_D5, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
```

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    GpioTermNone}}},//ISH_I2C0_SDA
277| {GPIO_SKL_LP_GPP_D6, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//ISH_I2C0_SCL
278| {GPIO_SKL_LP_GPP_D7, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//ISH_I2C1_SDA
279| {GPIO_SKL_LP_GPP_D8, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//ISH_I2C1_SCL
280| {GPIO_SKL_LP_GPP_D9, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirIn, GpioOutDefault,
    GpioIntLevel | GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//HOME_BTN
281| {GPIO_SKL_LP_GPP_D10, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirIn, GpioOutDefault,
    GpioIntLevel | GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SCREEN_LOCK_PCH
282| {GPIO_SKL_LP_GPP_D11, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirIn, GpioOutDefault,
    GpioIntLevel | GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//VOL_UP_PCH
283| {GPIO_SKL_LP_GPP_D12, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirIn, GpioOutDefault,
    GpioIntLevel | GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//VOL_DOWN_PCH
284| {GPIO_SKL_LP_GPP_D13, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//ISH_UART0_RXD_SML0B_DATA
285| {GPIO_SKL_LP_GPP_D14, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//ISH_UART0_TXD_SML0B_CLK
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286 {GPIO_SKL_LP_GPP_D15, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//ISH_UART0_RTS_N
287 {GPIO_SKL_LP_GPP_D16, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//ISH_UART0_CTS_SML0B_ALERT_N
288 {GPIO_SKL_LP_GPP_D17, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//DMIC_CLK_1
289 {GPIO_SKL_LP_GPP_D18, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//DMIC_DATA_1
290 {GPIO_SKL_LP_GPP_D19, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//DMIC_CLK_0
291 {GPIO_SKL_LP_GPP_D20, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//DMIC_DATA_0
292 {GPIO_SKL_LP_GPP_D21, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//SPI1_TCHPNL_IO2
293 {GPIO_SKL_LP_GPP_D22, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//SPI1_TCHPNL_IO3
294 {GPIO_SKL_LP_GPP_D23, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}},//SSP_MCLK
295 {GPIO_SKL_LP_GPP_E0, {GpioPadModeGpio,
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GpioHostOwnGpio, GpioDirInInv, GpioOutDefault,
GpioIntEdge | GpioIntApic, GpioHostDeepReset,
GpioTermNone}}},//SPI TPM_HDR_IRQ_N
296| {GPIO_SKL_LP_GPP_E1, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}},//SATA_ODD_PRSNT_N
297| {GPIO_SKL_LP_GPP_E2, {GpioPadModeGpio,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntLvlEdgDis | GpioIntApic,
GpioHostDeepReset,
GpioTermNone}},//M.2_SSD_SATA2_PCIE3_DET_N
298| {GPIO_SKL_LP_GPP_E3, {GpioPadModeGpio,
GpioHostOwnGpio, GpioDirOut, GpioOutHigh,
GpioIntDis, GpioResumeReset,
GpioTermNone}},//EINK_SSR_DFU_N
299| {GPIO_SKL_LP_GPP_E4, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}},//PCH_NFC_RESET
300| {GPIO_SKL_LP_GPP_E5, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}},//SATA1_PHYSLP1_DIRECT_R
301| {GPIO_SKL_LP_GPP_E6, {GpioPadModeGpio,
GpioHostOwnGpio, GpioDirOut, GpioOutLow,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}},//SATA2_PHYSLP2_M.2SSD_R
302| {GPIO_SKL_LP_GPP_E8, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}},//PCH_SATA_LED_N
303| {GPIO_SKL_LP_GPP_E9, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}},//USB_OC_0_WP1_OTG_N
304| {GPIO_SKL_LP_GPP_E10, {GpioPadModeNative1,
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GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}}},//USB_OC_1_WP4_N
305| {GPIO_SKL_LP_GPP_E11, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}}},//USB_OC_2_WP2_WP3_WP5_R_N
306| {GPIO_SKL_LP_GPP_E12, {GpioPadModeGpio,
GpioHostOwnGpio, GpioDirIn, GpioOutDefault,
GpioIntLevel | GpioIntDis, GpioHostDeepReset,
GpioTermNone}}},//PCH_NFC_IRQ
307| {GPIO_SKL_LP_GPP_E13, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}}},//DDI1_HPD_Q
308| {GPIO_SKL_LP_GPP_E14, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}}},//DDI2_HPD_Q
309| {GPIO_SKL_LP_GPP_E15, {GpioPadModeGpio,
GpioHostOwnAcpi, GpioDirInInv, GpioOutDefault,
GpioIntEdge | GpioIntSmi, GpioHostDeepReset,
GpioTermNone}}},//SMC_EXTSMI_R_N
310| {GPIO_SKL_LP_GPP_E16, {GpioPadModeGpio,
GpioHostOwnAcpi, GpioDirInInv, GpioOutDefault,
GpioIntLevel | GpioIntSci, GpioPlatformReset,
GpioTermNone}}},//SMC_RUNTIME_SCI_R_N
311| {GPIO_SKL_LP_GPP_E17, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}}},//EDP_HPD
312| {GPIO_SKL_LP_GPP_E18, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTermNone}}},//DDI1_CTRL_CLK
313| {GPIO_SKL_LP_GPP_E19, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
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    GpioIntDis, GpioHostDeepReset,
    GpioTermWpd20K}}, //DDI1_CTRL_DATA
314 | {GPIO_SKL_LP_GPP_E20, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //DDI2_CTRL_CLK
315 | {GPIO_SKL_LP_GPP_E21, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //DDI2_CTRL_DATA
316 | {GPIO_SKL_LP_GPP_E22, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirInInv, GpioOutDefault,
    GpioIntLevel | GpioIntApic, GpioHostDeepReset,
    GpioTermNone}}, //PCH_CODEC_IRQ
317 | {GPIO_SKL_LP_GPP_E23, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirOut, GpioOutHigh,
    GpioIntDis, GpioHostDeepReset,
    GpioTermWpd20K}}, //TCH_PNL_RST_N
318 | {GPIO_SKL_LP_GPP_F0, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SSP2_SCLK
319 | {GPIO_SKL_LP_GPP_F1, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SSP2_SFRM
320 | {GPIO_SKL_LP_GPP_F2, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SSP2_TXD
321 | {GPIO_SKL_LP_GPP_F3, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //SSP2_RXD
322 | {GPIO_SKL_LP_GPP_F4, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
```

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GpioTolerance1v8 |
GpioTermNone}}},//SERIALIO_I2C2_SDA
323| {GPIO_SKL_LP_GPP_F5, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTolerance1v8 |
GpioTermNone}}},//SERIALIO_I2C2_SCL
324| {GPIO_SKL_LP_GPP_F6, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTolerance1v8 |
GpioTermNone}}},//SERIALIO_I2C3_SDA
325| {GPIO_SKL_LP_GPP_F7, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTolerance1v8 |
GpioTermNone}}},//SERIALIO_I2C3_SCL
326| {GPIO_SKL_LP_GPP_F8, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTolerance1v8 |
GpioTermNone}}},//SERIALIO_I2C4_SDA
327| {GPIO_SKL_LP_GPP_F9, {GpioPadModeNative1,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTolerance1v8 |
GpioTermNone}}},//SERIALIO_I2C4_SCL
328| {GPIO_SKL_LP_GPP_F10, {GpioPadModeNative2,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTolerance1v8 |
GpioTermNone}}},//SERIALIO_I2C5_ISH_12C2_SDA
329| {GPIO_SKL_LP_GPP_F11, {GpioPadModeNative2,
GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
GpioIntDis, GpioHostDeepReset,
GpioTolerance1v8 |
GpioTermNone}}},//SERIALIO_I2C5_ISH_12C2_SCL
```

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330 {GPIO_SKL_LP_GPP_F12, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //EMMC_CMD
331 {GPIO_SKL_LP_GPP_F13, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //EMMC_DATA0
332 {GPIO_SKL_LP_GPP_F14, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //EMMC_DATA1
333 {GPIO_SKL_LP_GPP_F15, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //EMMC_DATA2
334 {GPIO_SKL_LP_GPP_F16, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //EMMC_DATA3
335 {GPIO_SKL_LP_GPP_F17, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //EMMC_DATA4
336 {GPIO_SKL_LP_GPP_F18, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //EMMC_DATA5
337 {GPIO_SKL_LP_GPP_F19, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //EMMC_DATA6
338 {GPIO_SKL_LP_GPP_F20, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}, //EMMC_DATA7
339 {GPIO_SKL_LP_GPP_F21, {GpioPadModeNative1,
```

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    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//EMMC_RCLK
340| {GPIO_SKL_LP_GPP_F22, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//EMMC_CLK
341| {GPIO_SKL_LP_GPP_F23, {GpioPadModeGpio,
    GpioHostOwnGpio, GpioDirIn, GpioOutDefault,
    GpioIntLevel | GpioIntApic, GpioHostDeepReset,
    GpioTermNone}}},//PCH_M.2_WWAN_UIM_SIM_DET
342| {GPIO_SKL_LP_GPP_G0, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SD_CMD
343| {GPIO_SKL_LP_GPP_G1, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SD_DATA0
344| {GPIO_SKL_LP_GPP_G2, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SD_DATA1
345| {GPIO_SKL_LP_GPP_G3, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SD_DATA2
346| {GPIO_SKL_LP_GPP_G4, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SD_DATA3
347| {GPIO_SKL_LP_GPP_G5, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SD_CDB
348| {GPIO_SKL_LP_GPP_G6, {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone, GpioOutDefault,
```

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    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SD_CLK
349 | {GPIO_SKL_LP_GPP_G7,   {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
    GpioIntDis, GpioHostDeepReset,
    GpioTermNone}}},//SD_WP
350 | {GPIO_SKL_LP_GPD0,   {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
    GpioIntDis, GpioDswReset,
    GpioTermNone}}},//PM_BATLOW_R_N
351 | {GPIO_SKL_LP_GPD1,   {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
    GpioIntDis, GpioDswReset,
    GpioTermNone}}},//AC_PRESENT_R
352 | {GPIO_SKL_LP_GPD2,   {GpioPadModeNative1,
    GpioHostOwnAcpi, GpioDirIn,   GpioOutDefault,
    GpioIntLevel | GpioIntSci, GpioDswReset,
    GpioTermNone}}},//LANWAKE_SMC_WAKE_SCI_N
353 | {GPIO_SKL_LP_GPD3,   {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
    GpioIntDis, GpioDswReset,
    GpioTermWpu20K}}},//PM_PWRBTN_R_N
354 | {GPIO_SKL_LP_GPD4,   {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
    GpioIntDis, GpioDswReset,
    GpioTermNone}}},//SLP_S3_R_N
355 | {GPIO_SKL_LP_GPD5,   {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
    GpioIntDis, GpioDswReset,
    GpioTermNone}}},//SLP_S4_R_N
356 | {GPIO_SKL_LP_GPD6,   {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
    GpioIntDis, GpioDswReset,
    GpioTermNone}}},//SLP_M_R_N
357 | {GPIO_SKL_LP_GPD7,   {GpioPadModeNative1,
    GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
    GpioIntDis, GpioDswReset,
```

```
        GpioTermNone}}},//USB_WAKEOUT_INTRUDET_N
358 | {GPIO_SKL_LP_GPD8,    {GpioPadModeNative1,
  GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
  GpioIntDis, GpioDswReset,
  GpioTermNone}}},//SUS_CLK
359 | {GPIO_SKL_LP_GPD9,    {GpioPadModeNative1,
  GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
  GpioIntDis, GpioDswReset,
  GpioTermNone}}},//PCH_SLP_WLAN_N
360 | {GPIO_SKL_LP_GPD10,   {GpioPadModeNative1,
  GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
  GpioIntDis, GpioDswReset,
  GpioTermNone}}},//SLP_S5_R_N
361 | {GPIO_SKL_LP_GPD11,   {GpioPadModeNative1,
  GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
  GpioIntDis, GpioDswReset,
  GpioTermNone}}},//PM_LANPHY_ENABLE
362 | {END_OF_GPIO_TABLE,   {GpioPadModeGpio,
  GpioHostOwnGpio, GpioDirNone,  GpioOutDefault,
  GpioIntDis, GpioDswReset,
  GpioTermNone}}},//Marking End of Table
363 };
364
365 #endif // _GPIO_CONFIG_H_
```



# CoffeeLake Intel(R) Firmware Support Package (FSP) Integration Guide

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## Include Directory Reference

Directory dependency graph for Include:



## Files

file [\*\*FirmwareVersionInfoHob.h\*\*](#) [code]

Header file for Firmware Version Information.

file [\*\*FspInfoHob.h\*\*](#) [code]

Header file for FSP Information HOB.

file [\*\*FspmUpd.h\*\*](#) [code]

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file [\*\*FspsUpd.h\*\*](#) [code]

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file [\*\*FsptUpd.h\*\*](#) [code]

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file [\*\*FspUpd.h\*\*](#) [code]

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file [\*\*GpioConfig.h\*\*](#) [code]

Header file for GpioConfig structure used by GPIO library.

file [\*\*GpioSampleDef.h\*\*](#) [code]

Sample enum definitions for GPIO table.

file [\*\*HobUsageDataHob.h\*\*](#) [code]

Definitions for Hob Usage data HOB.

file [\*\*MemInfoHob.h\*\*](#) [code]

This file contains definitions required for creation of Memory S3 Save data, Memory Info data and Memory Platform data hobs.

file [\*\*SmbiosCacheInfoHob.h\*\*](#) [code]

Header file for SMBIOS Cache Info HOB.

file **SmbiosProcessorInfoHob.h** [code]

Header file for SMBIOS Processor Info HOB.

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