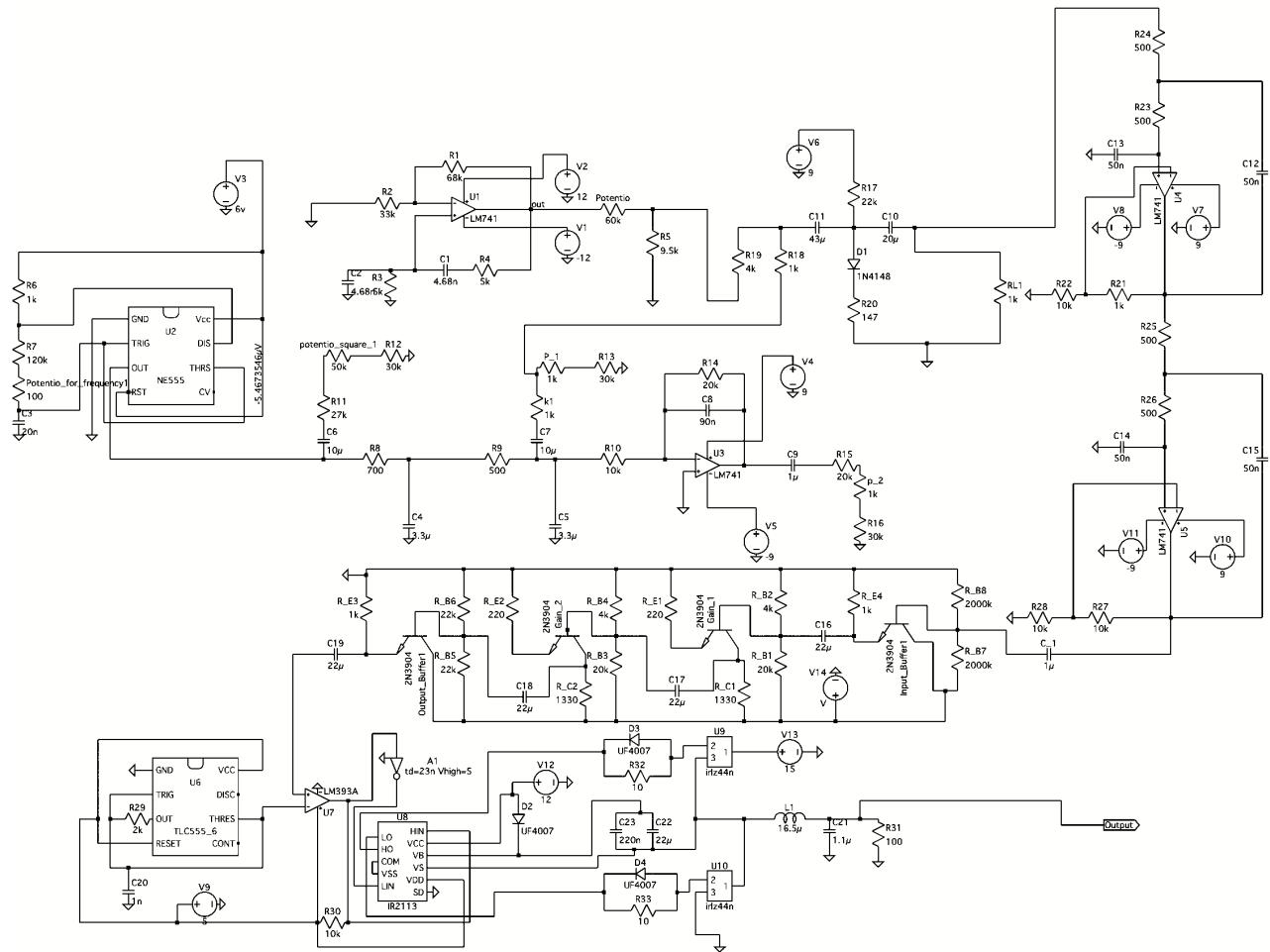


Audio Synthesizer

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Abstract

The goal of this project is to design, test, and develop an Audio Synthesizer. This report is an overview of the design and validation process. Here we cover 6 parts of this project, the oscillator, the low frequency oscillator, the mixer, the low pass filter, the preamplifier, and the class d amplifier. The oscillator creates a sine wave at 6.8Khz while the low frequency version creates different signal patterns at lower frequencies. The mixer is a simple single diode mixer that combines the oscillators and creates additional harmonic distortion. The low pass filter is a 4th order Sallen-Key filter that uses two OpAmps to achieve a dc gain of 12 dB with a cut off frequency of 6 KHz. Finally, the preamplifier stage is comprised of two BJT gain stages and an input / output BJT buffer that achieves 26dB gain from 120 Hz to 12 KHz and from 10 mV to 100 mV peak to peak. Finally, a class d amplifier is used at the output stage.

Introduction

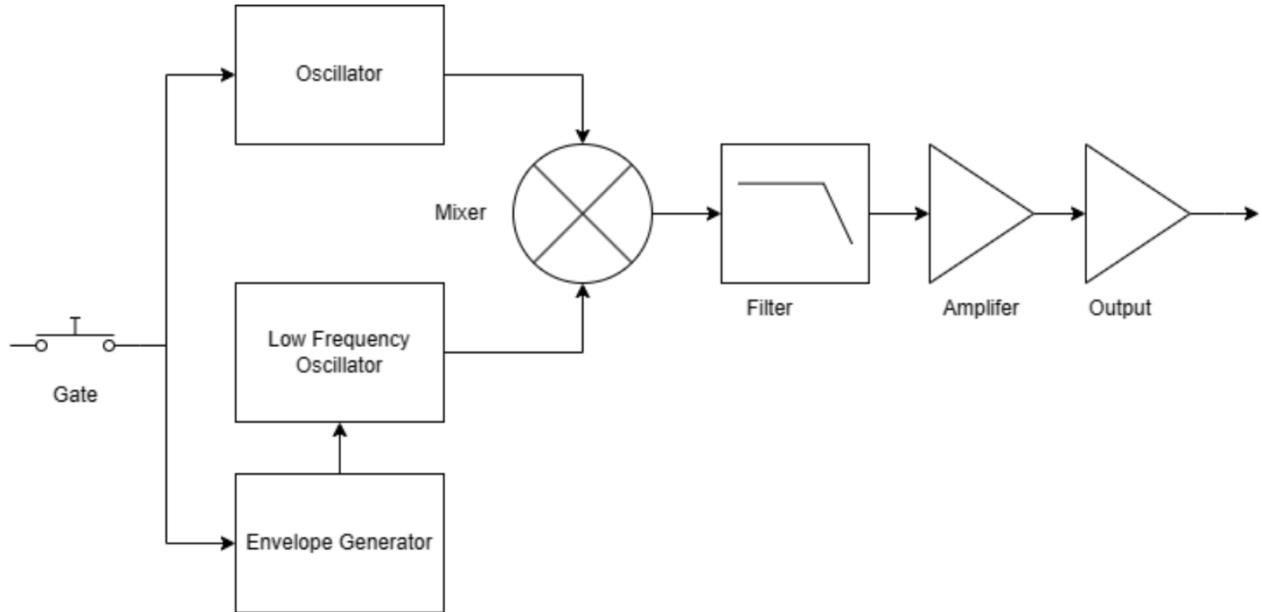


Figure 1: Project audio synthesizer overview.

Initially when we created an audio synthesizer, we focused on three sections mixer, filter and amplifier. A mixer is generally used to alter the frequency of a signal. It takes two signals and creates new ones based on the addition and subtraction of the initial signals. In our case, we want to take advantage of this property to increase the number of signals produced effectively increasing harmonic distortion. This will allow us to create new sounds from two signals. In order to keep all the signals in the audible range, we use a low pass filter to remove any signals that are not audible. The Sallen-key fourth order low pass filter is an active filter that boost the DC signal by 12dB and removes signals above a specified cutoff frequency. It is important to use an active filter because we want to also preserve the harmonic distortion under the filter's 6 KHz cutoff frequency. After removing the excess signals, we amplify what is left over and prepare it for an output stage. The amplifier has a dual gain stage with and output buffer that lowers the output resistance to about 65 ohms.

Our next goal was focused on the remaining 3 stages. The Oscillator, the low frequency oscillator and the output stage. The oscillator is used to create a 6.8 KHz sine signal, this signal will be the backbone of our audio synthesizer. The low frequency oscillator will generate 3 different signals that will each be combine with the 6.8 KHz signal. This will give us unique sounds as they are combined in the mixer. Lastly, our output stage is a class D amplifier that will further boost our output signals power.

List of Components:

Oscillator

5 Resistors	1 Potentiometer	2 Capacitors	1 OpAmp
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Low Frequency Oscillator

8 Resistors	1 555 Timer	7 Capacitors	3 Potentiometers
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Mixer

4 Resistors	2 Capacitors	1 Diode
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Filter

8 Resistors	4 Capacitors	2 OpAmps
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Pre-Amplifier

14 Resistors	5 Capacitors	4 BJTs
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Class D Amplifier

1 555 Timer	3 Diodes	1 Comparator	4 Capacitors	1 Inductor
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4 Resistors	2 Power Mosfets	1 Mosfet Driver	2 Voltage Regulators
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Oscillator

Before proceeding with construction, we ensured that our circuit could effectively simulate and meet our design specifications for the oscillator. The objective is to generate a sinusoidal output signal with a frequency of 6.8 kHz, maintaining an error margin of no more or less than 34 Hz. Additionally, the output amplitude should fall within the range of 0.2 to 1.2 volts. To achieve these requirements, we opted to employ a Wein bridge oscillator.

The oscillator design incorporates an LM741 operational amplifier connected to a feedback resistor, denoted as R1 in the circuit diagram. R1 is specified with a value of $68\text{k}\Omega$, while R2 is set at $33\text{k}\Omega$. R1 and R2 influence the gain of the oscillator. The gain needs to be precisely set to 3 to achieve sustained oscillations. The value of R1 is kept higher than R2 so that we can achieve sustained oscillations. This condition ensures that the positive feedback from the amplifier compensates for the energy lost in the feedback network, thereby sustaining oscillation.

To produce a frequency of 6.8 kHz, we use the formula $f = \frac{1}{2\pi RC}$ where the values of $R = R3 = R4$ and the capacitor $C = C1 = C2$. When we plug in the value of our desired frequency, we can calculate the value of our desired frequency.

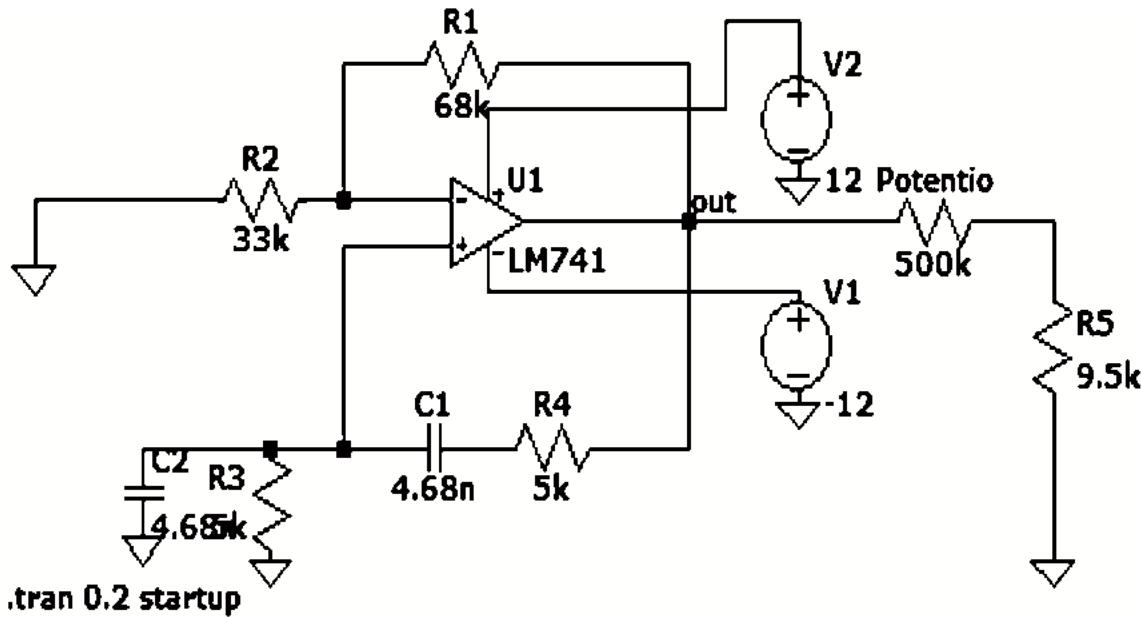


Figure 2: LT Spice Circuit of Oscillator

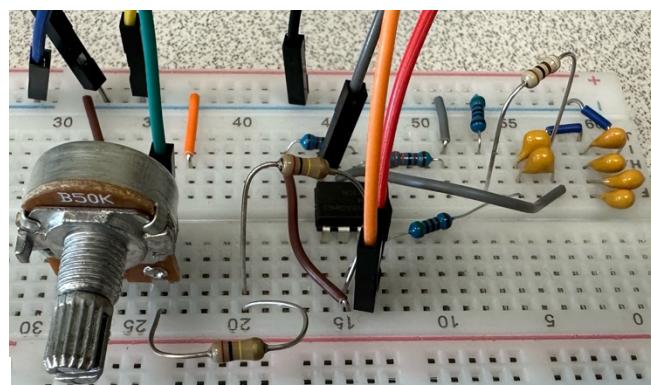


Figure 3: Oscillator on Breadboard for Testing.

Component	R1	R2	R3	R4	Potentio	C1	C2
Simulated	68k Ω	33k Ω	5k Ω	5k Ω	500k	4.68n	4.68n
Measured	67.8K Ω	33.1K Ω	4.94K Ω	4.91k Ω	490k Ω	4.7n	4.7n

Table 1 The Table shows stimulated and measured values for oscillator circuit.

Simulation results:

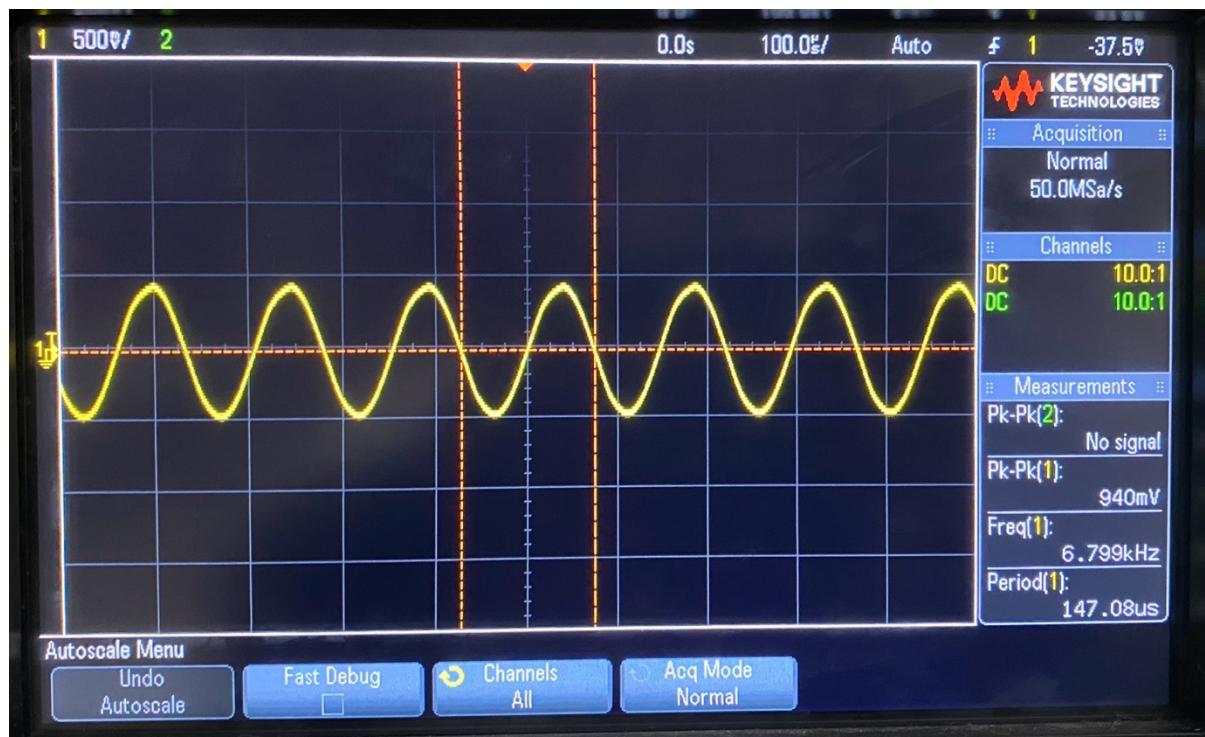


Figure 4: 6.8Khz Sine Wave Output Yellow

The output signal in Figure 3 shows the sine wave that is equal to 6.8 KHz. The error in the wave is less than 34 Hz.

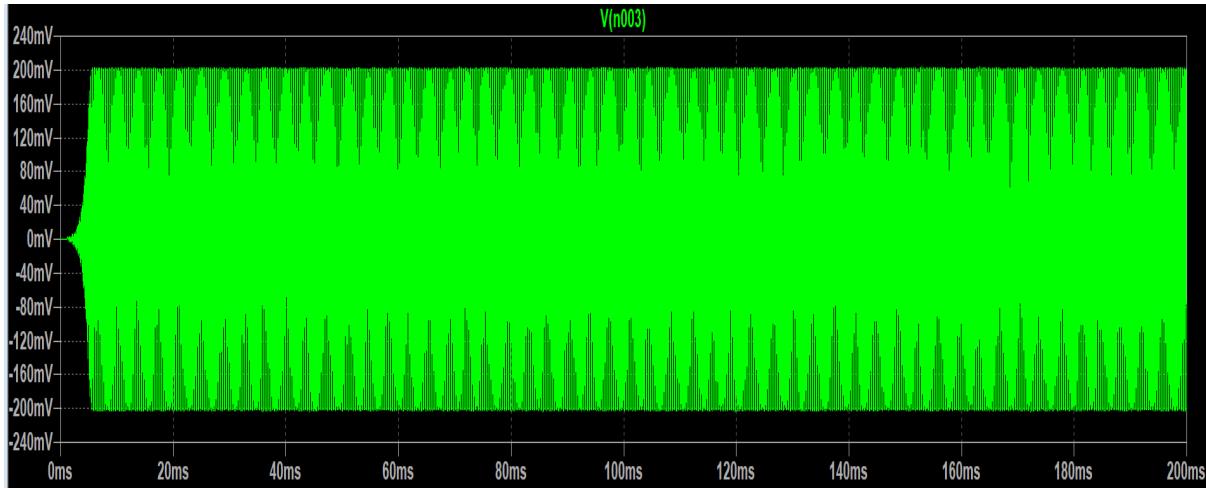


Figure 5: Amplitude compressed when the Potentiometer is set to 500 ohms.

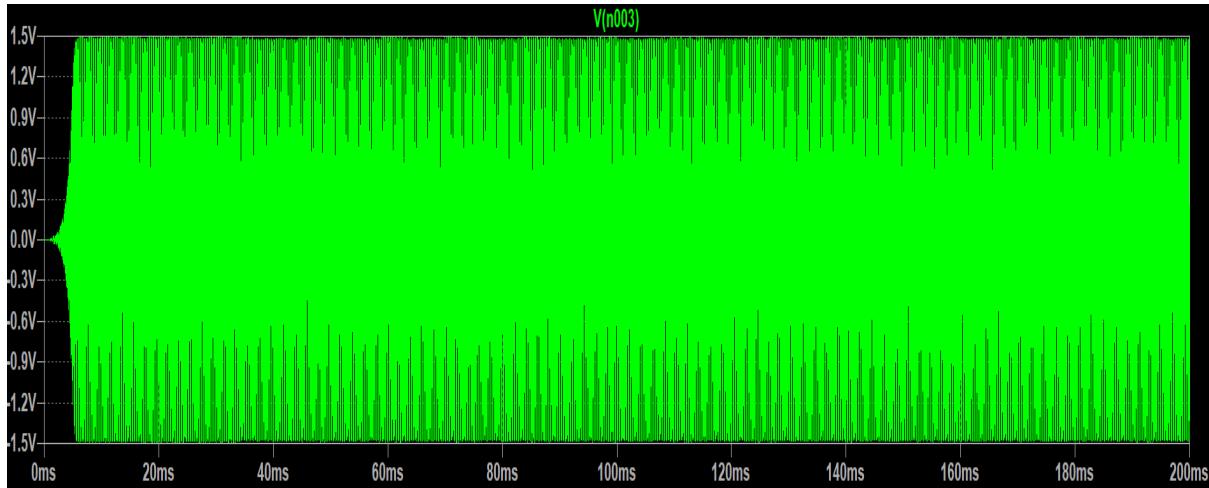


Figure 6: The amplitude of the wave when Potentiometer is lowered down to 100 ohms

The output wave in the figures above show the 6.8 KHz signal can vary its amplitude from 0.2V to 1.5V by turning the potentiometer.

Calculations:

Frequency = 6.8 KHz

Resistor R = 5k ohms selected to get the desired capacitor value that is easily available in the market.

Formula used:

$$C = \frac{1}{2 \times \pi \times 5k \times 6.8k}, \quad f = \frac{1}{2\pi RC}$$

$$C = 4.68 \text{ nF}$$

Low Frequency Oscillator

To achieve low-frequency oscillation, we utilize a 555 timer IC. R1 is set to 300 ohms, and R2 varies depending on the desired frequency: 142900 ohms for 5 Hz, 8850 ohms for 80 Hz, and 3850 ohms for 180 Hz. Instead of a fixed resistor for R2, a 1 megaohm potentiometer is used to adjust the circuit's frequency.

R1 is deliberately chosen to be very low so that a duty cycle of 50% can be easily attained because when R1 is very small, its value becomes negligible in the duty cycle formula: Duty Cycle = $(R1 + R2) / (R1 + 2R2) \times 100$. The resultant output waveform from the 555 timer is a square wave. Later, as depicted further in the figure, the RC network is utilized to obtain a triangular and sine output waveforms.

The amplitude of the square, triangular, and sine waves is controlled with the help of a potentiometer. By implementing these adjustments, we can achieve a clean output: a sine wave of 180 Hz, a square wave of 5 Hz, and a triangular wave of 80 Hz.

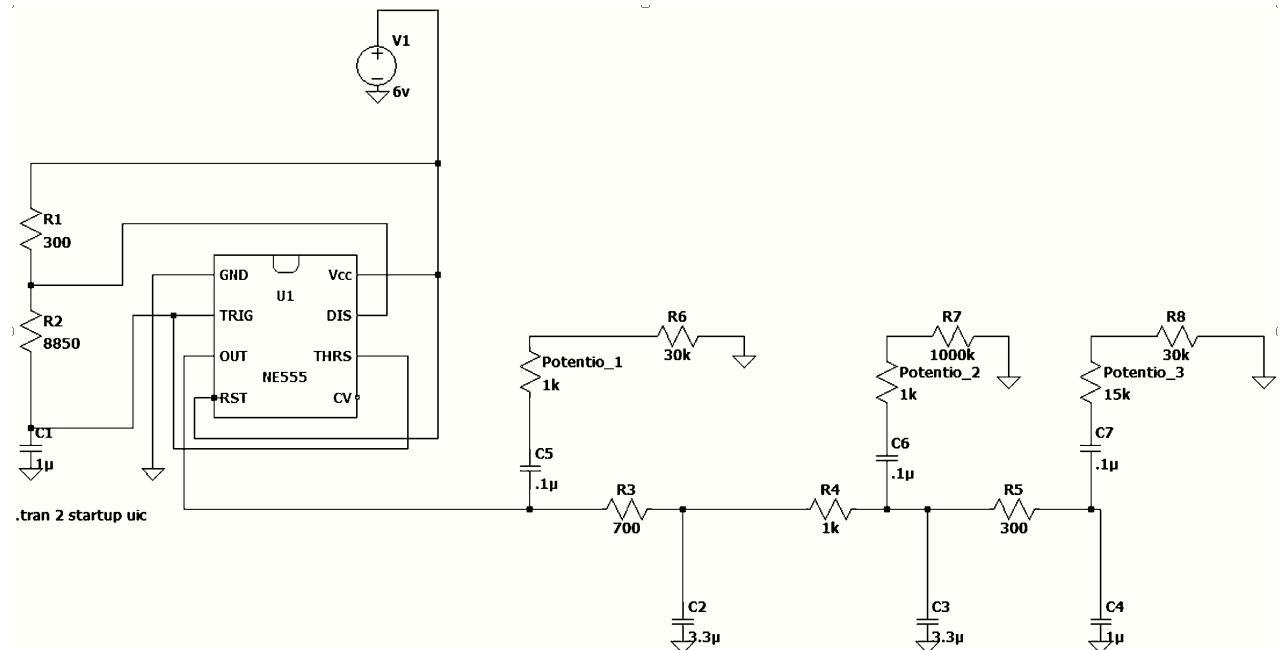


Figure 7: LT Spice circuit of Low frequency oscillator

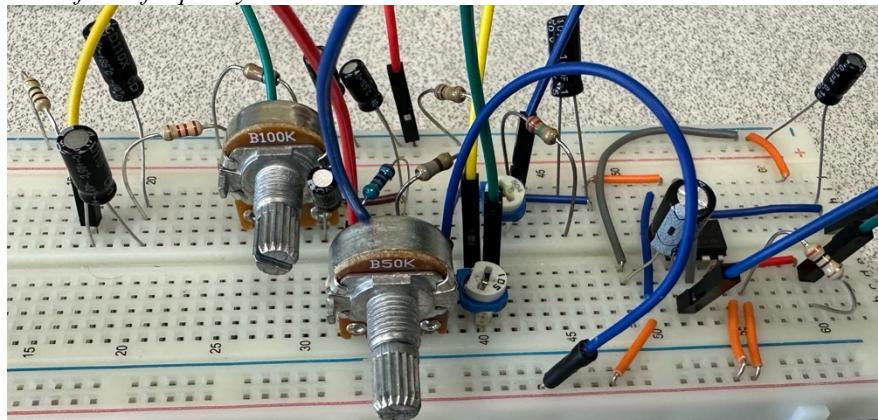


Figure 8: Low Frequency Oscillator on Breadboard for Testing.

Component	R1	R2	R3	R4	R5	R6	R7	R8	P_1	P_2	P_3
Simulated	300 Ω	8850 Ω	300 Ω	1 KΩ	300 Ω	30k KΩ	1000 KΩ	30k KΩ	500 KΩ	1 M Ω	500 KΩ
Measured	298 Ω	8840 Ω	295 Ω	990 Ω	301 Ω	29.98 KΩ	993 KΩ	29.4 KΩ	492 KΩ	0.989 M Ω	488 KΩ

Table 2

Component	C1/F	C2/F	C3/F	C4/F	C5/F	C6/F	C7/F
Simulated	1u	0.1u	3.3u	0.1u	3.3u	0.1u	1u
Measured	1u	0.99 u	3.32 u	0.1u	3.23u	0.99u	0.97u

Table 3

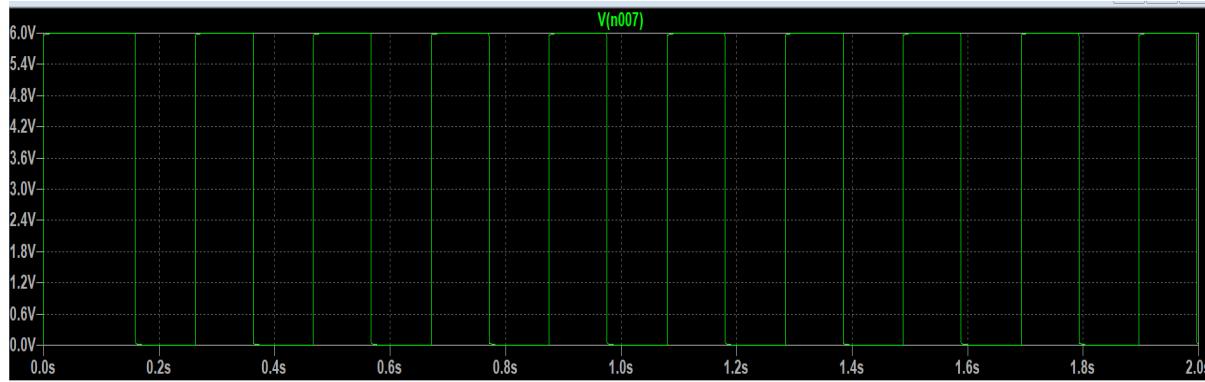


Figure 9: The output of the square wave on LT Spice.

In the figure 9 square wave produce is a nice clean output. The duty cycle in the figure also seems to be of 50%. Resultantly it would be producing a nice triangular and sine wave.

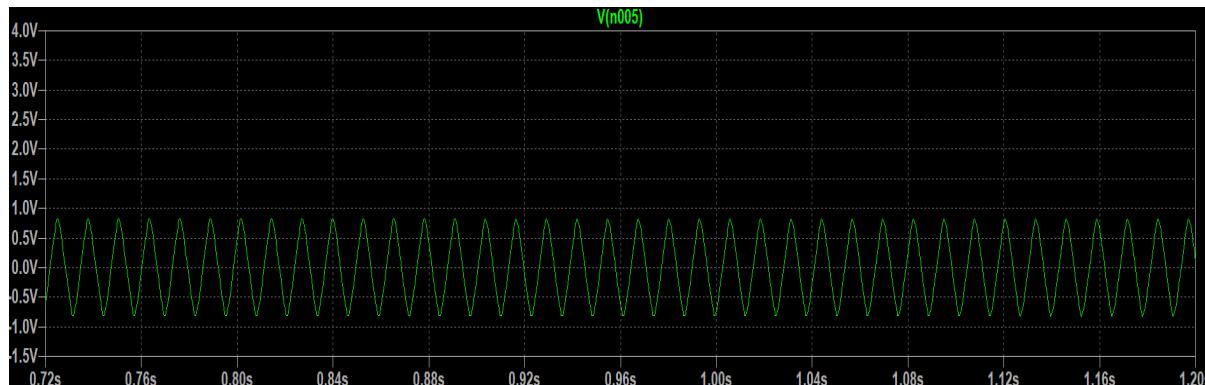


Figure 10: The Output of the triangular Lt Spice

The triangular wave produced seems to be perfect triangle. The right choice of capacitor and resistor has produced a triangular output. It took one RC circuit to achieve this wave form



Figure 11: The output of the sine wave on IT spice

To achieve the sine output, it was necessary to employ two RC circuits. Initially, a lower capacitor value resulted in the generation of a triangular wave once again. Thus, it was imperative to make adjustments. Subsequently, a higher capacitor value was utilized for the final sine wave stage. This modification likely contributed to refining the waveform, ensuring its accurate representation as a sinusoidal oscillation. The iterative process of fine-tuning component values underscores the intricacies involved in waveform generation and emphasizes the importance of meticulous circuit design to achieve desired outputs.

Results

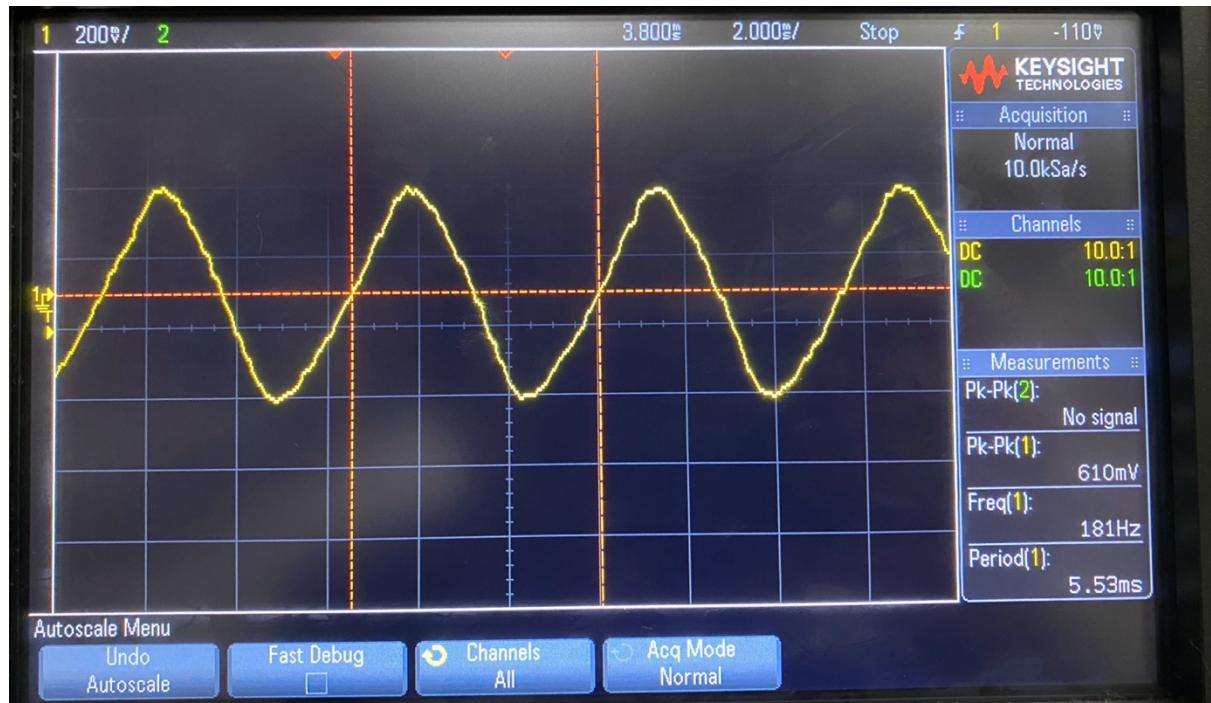


Figure 12: Sine Waveform

The output wave form on the oscillator is shown in the figure above. Some noise can be seen in the figure above as the sine wave is the last output stage of the RC filter otherwise the sine wave looks perfect.

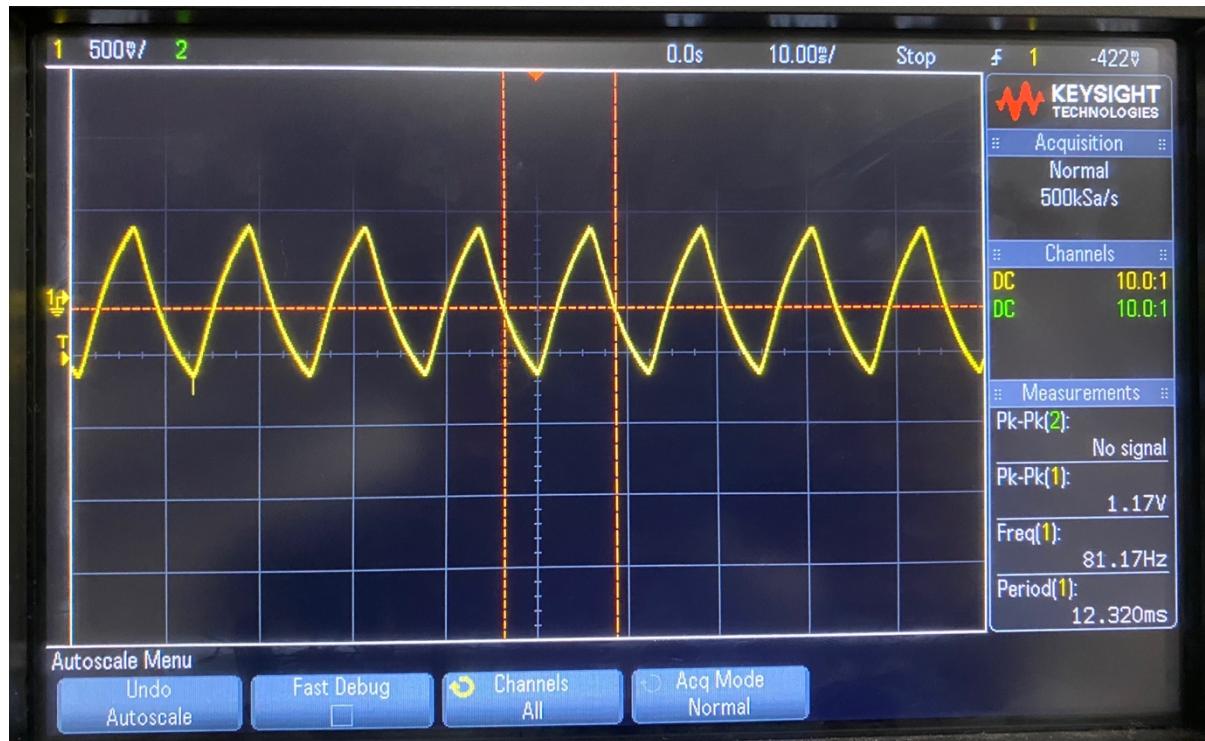


Figure 13: Triangular waveform

In Figure 13, the triangular wave appears in the second stage of the RC setup. Notably, no noise is visible in this stage. The wave's amplitude is controlled by a potentiometer.



Figure 14: The triangular wave is adjusted to the lowest point of 5 Hz.

Calculations:

R2 value at a frequency of 5 Hz:

$$f = \frac{1.44}{(R1 + 2R2)C1}$$

$$R2 = \frac{1.44 - fC1R1}{2fC1}$$

$$R2 = \frac{1.44 - 5}{2 \times 5 \times 1 \times 10^{-6}}$$

$$R2 = 143850 \Omega$$

The value of R2 should be increased to 143850Ω to get a square wave of 5 Hz. Using this resistance value, our duty cycle will closely follow this formula: $f = \frac{1.44}{(R1+2R2)C1}$

Duty Cycle for 5 Hz Triangle

$$DC = \frac{R1 + R2}{R1 + 2R2} \times 100$$

$$DC = \frac{300 + 143850}{300 + 2 \times 143850} \times 100$$

$$DC = 50\%$$

The output of a 555 timer IC has a duty cycle of 50%. By adjusting a potentiometer to a value of 143850Ω , we can produce a nice and clean triangular waveform. Additionally, to generate both sine and triangular waves, we can utilize an integrator circuit. Since we have a 50% duty cycle, it is possible to get our desired output this way. But we decided to use an RC filter in our circuit.

R2 Value at a frequency of 80 HZ:

$$f = \frac{1.44}{(R1 + 2R2)C1}$$

$$R2 = \frac{1.44 - fC1R1}{2fC1}$$

$$R2 = \frac{1.44 - 80}{2 \times 80 \times 1 \times 10^{-6}}$$

$$R2 = 8850 \Omega$$

Duty Cycle for 80 Hz Triangle

$$DC = \frac{R1 + R2}{R1 + 2R2} \times 100$$

$$DC = \frac{300 + 8850}{300 + 2 \times 8850} \times 100$$

$$DC = 50\%$$

The same case lies here the duty cycle is 50% and we got a good triangular wave as shown in figure 13.

R2 value at a frequency of 180 Hz

$$f = \frac{1.44}{(R1 + 2R2)C1}$$

$$R2 = \frac{1.44 - fC1R1}{2fC1}$$

$$R2 = \frac{1.44 - 180}{2 \times 180 \times 1 \times 10^{-6}}$$

$$R2 = 3850 \Omega$$

Duty Cycle for 180 Hz Sine

$$DC = \frac{R1 + R2}{R1 + 2R2} \times 100$$

$$DC = \frac{300 + 3850}{300 + 2 \times 3850} \times 100$$

$$DC = 51\%$$

The duty cycle shifts slightly to 51% due to the R1 value not being negligible compared to R2. However, despite this adjustment, we are still able to generate a sine wave as shown in Figure 12.

Mixer

The Mixer is a widely used component used to shift signals around in the frequency spectrum. This is important because it allows us to change a signal frequency. The mixer by itself does not change frequency, it simply creates many variations of the original signal and the local oscillator that need to be filtered out. The filter is what allows you to choose what signals we will be taking from the mixer's output.

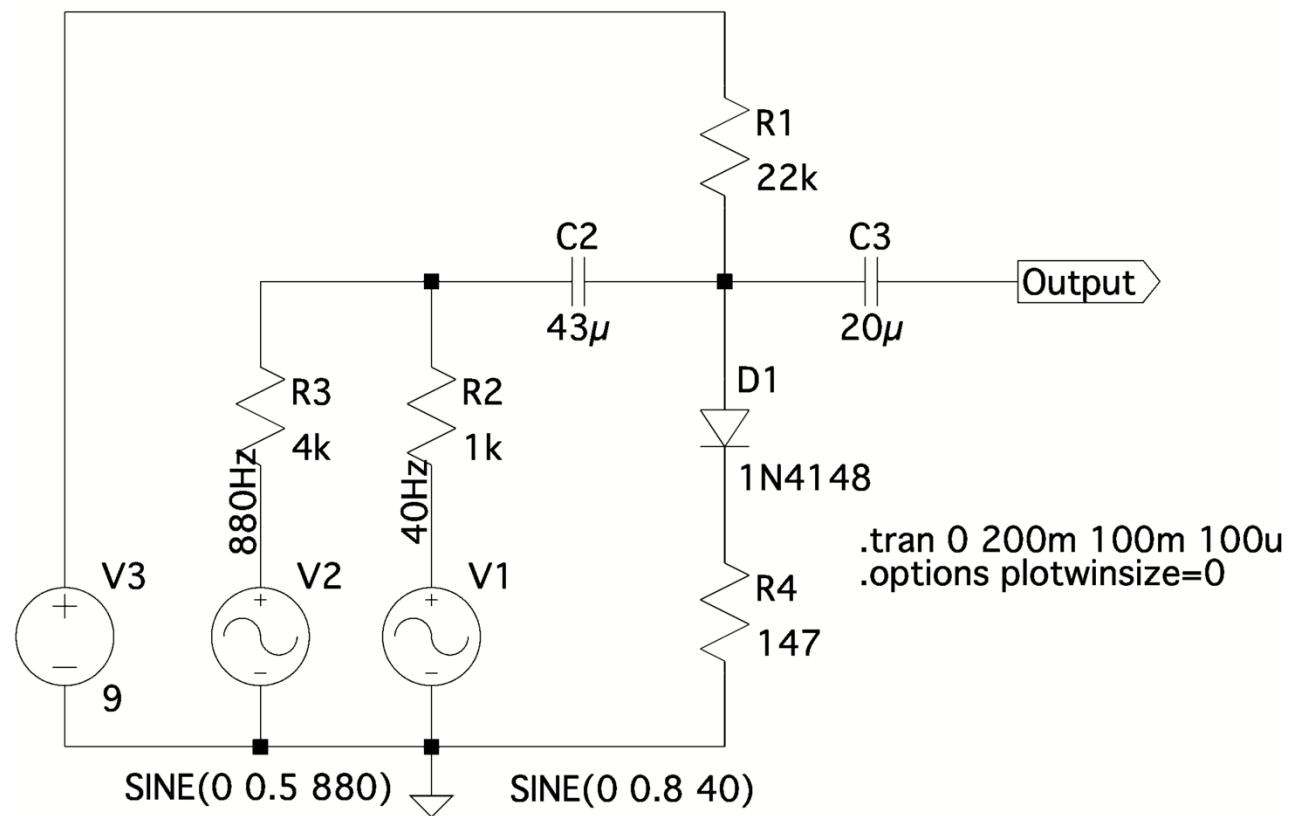


Figure 15: Simulated Circuit Diagram for Mixer on LTspice.

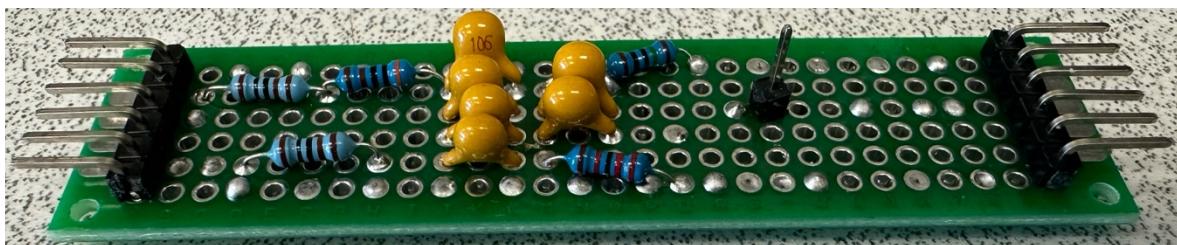


Figure 16: Mixer PCB Board

Component	R1	R2	R3	R4	C2	C3
Simulated	22K Ω	1K Ω	4K Ω	147 Ω	43u F	20u F
Measured	21.5K Ω	996 Ω	3.926K Ω	147.8 Ω	42.39u F	20.48u F

Table 4: Simulated Values Compared to Measured Values

Simulation results:

Before building our circuit, we wanted to make sure that we could simulate and meet our design criteria. This circuit must use 880 Hz 2-V peak-to-peak signal and a 40 Hz 2-V peak-to-peak signal. It must also have a conversion loss less than 23 dB. Based on these requirements we have a lot of liberty to choose resistance and capacitance values that will generate the most harmonic distortion. The figure above shows the circuit we simulated, and the figures below shows its inputs and output signals.

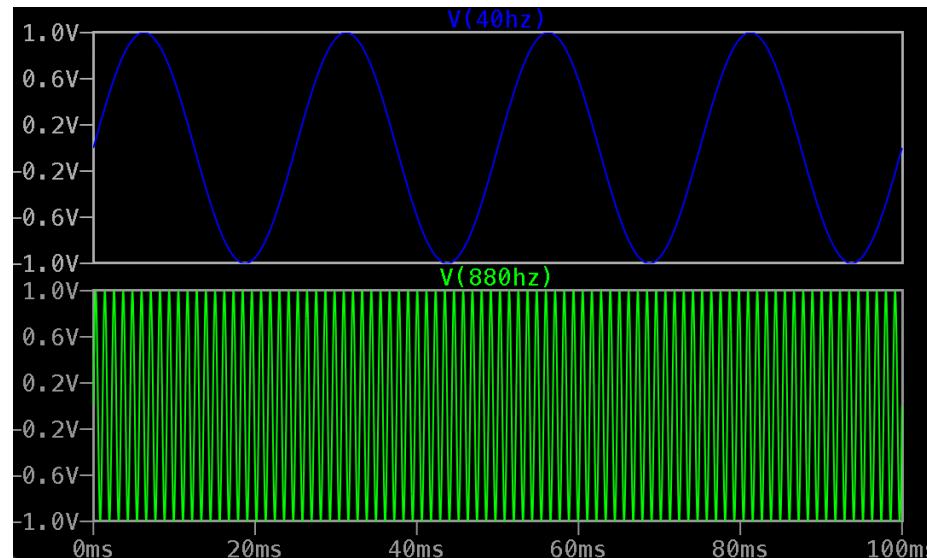


Figure 17: Input Signals, Blue 40 Hz and Green 880 Hz.

Since the 880 Hz rides on top of the 40 Hz, we found a sweet spot using $1 \text{ K}\Omega$ and $4 \text{ K}\Omega$ resistors. These resistors allow us to adjust the strength of each signal's intensity.

This output signal contains more frequencies than just 40 Hz and 880 Hz. It was purposely designed to create as many additional harmonic frequencies.

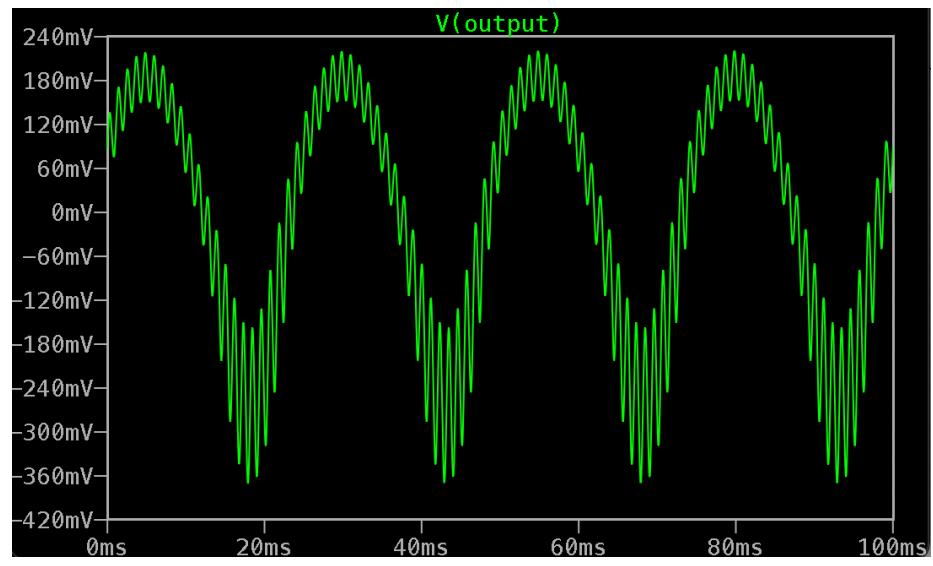


Figure 18: Mixer Output Signal

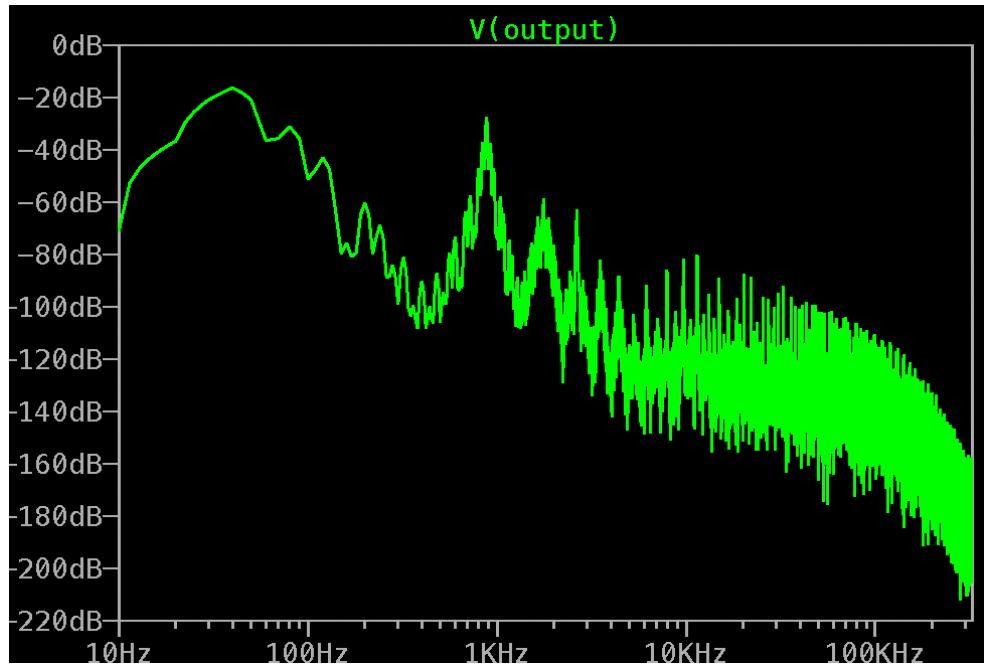


Figure 19: Mixer Output Signal FFT w/Blackman Window.

This plot shows the frequency content of the signal. You can see that additional signals were created but most are not powerful enough for considerable contribution to our signal. Our input signals have the highest strength while the rest are derived from 40 and 880 Hz.

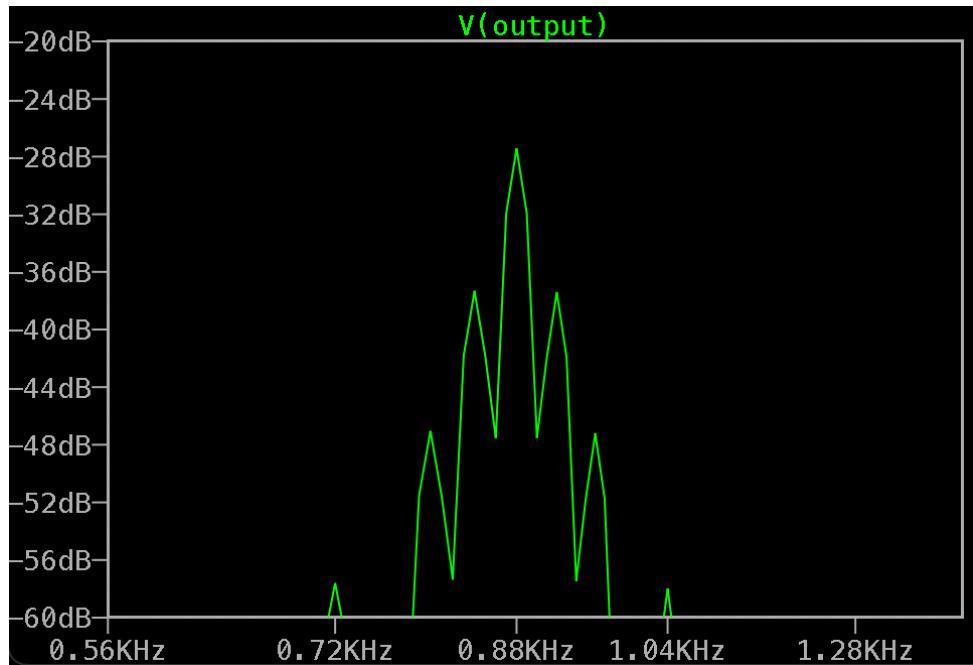


Figure 20: Mixer Output Signal FFT 880 Hz Zoomed In.

In order to determine our conversion loss, we take a close look at the 880 Hz signal and see how the 40 Hz signal creates distortion at 920 Hz and 840 Hz. The difference in dB at these points is considered the conversion loss. In our case, we have about 10dB loss.

Measurement results:

Setting up our simulation in the lab provided us with extremely similar results.

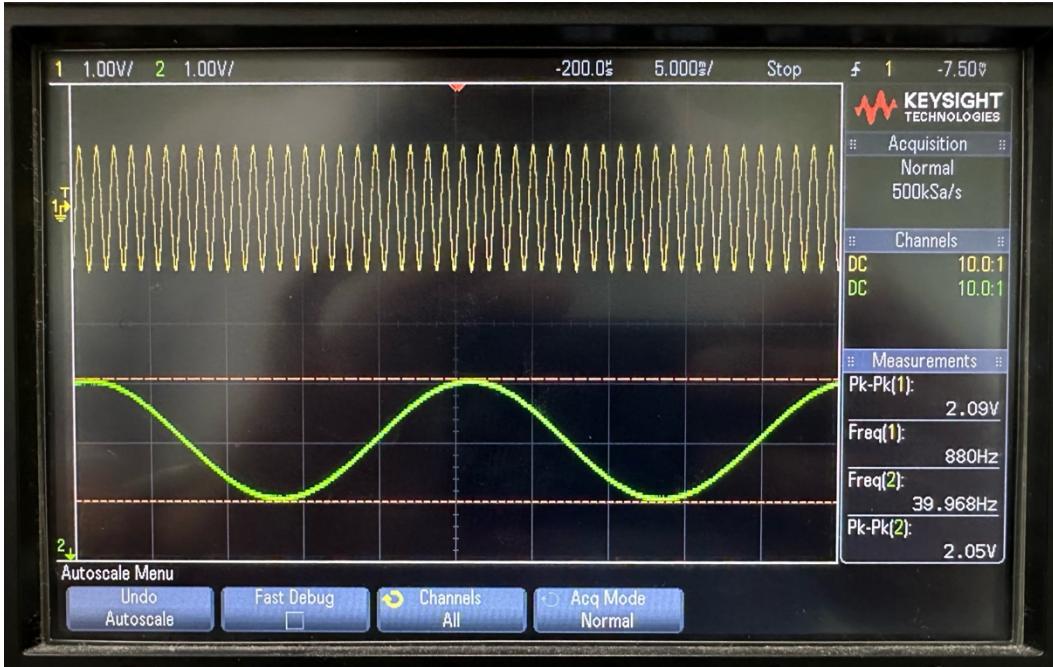


Figure 21: Actual Input Signals.

The same input signal used for our simulations.

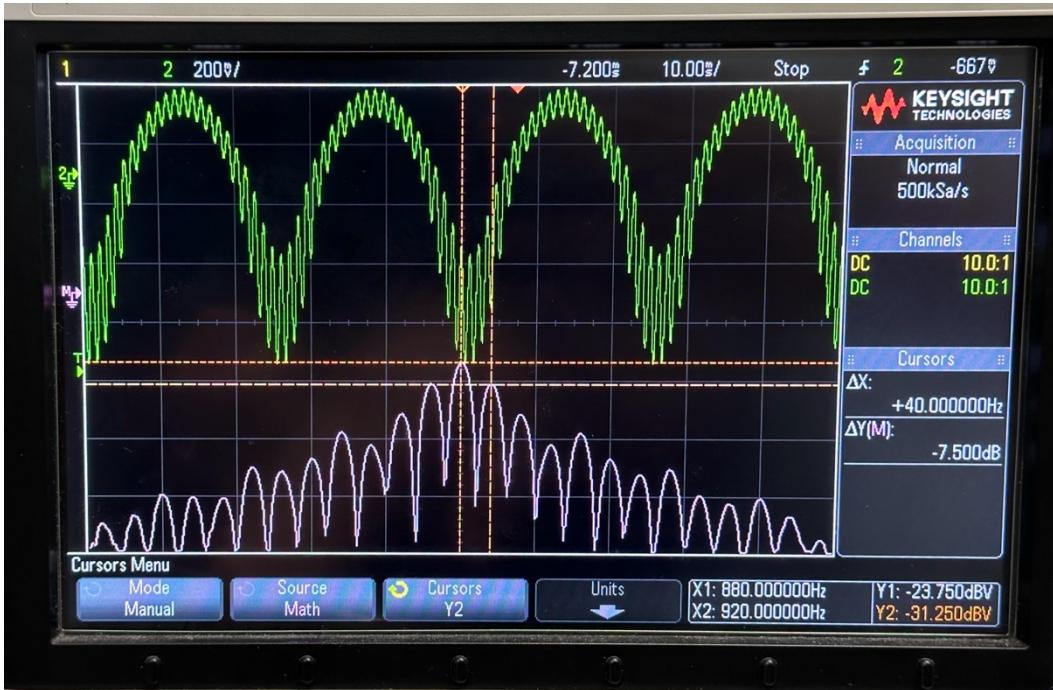


Figure 22: Output Signal and FFT

Here we can see our output signal and the frequency spectrum at the same time. We can measure that our next peak from 880 Hz is 40 Hz away with a conversion loss of 7.5dB.

Filter

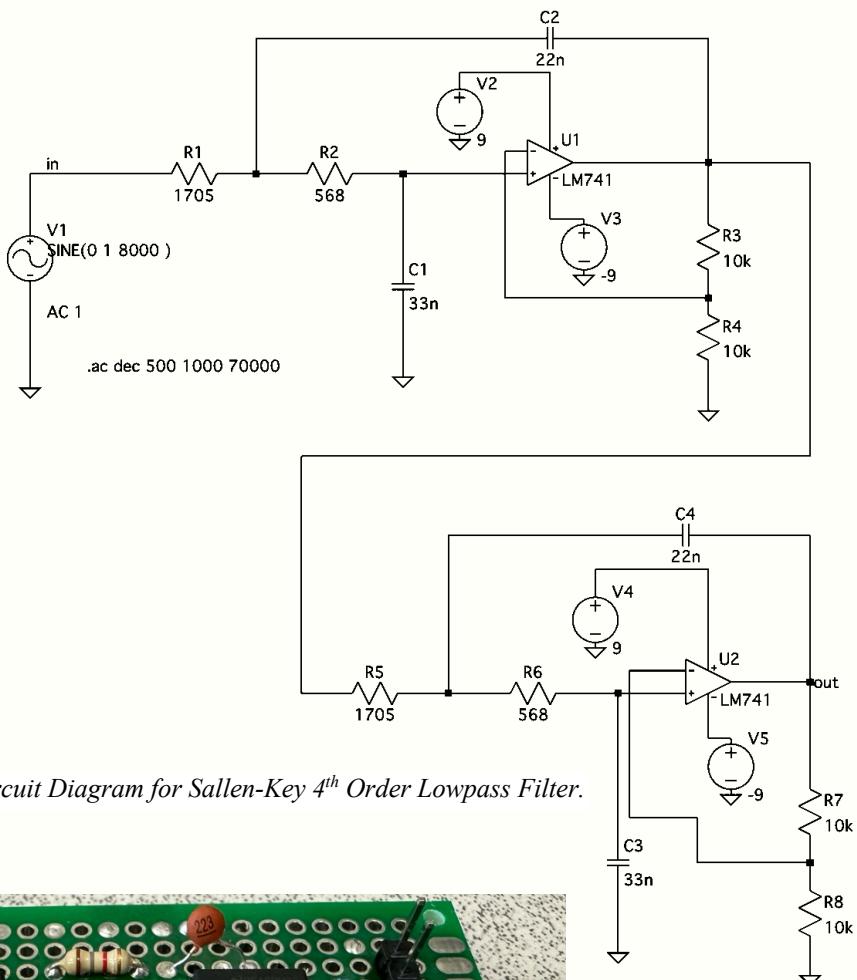


Figure 23: Simulated Circuit Diagram for Sallen-Key 4th Order Lowpass Filter.



Figure 24: Filter PCB Board

Component	R1	R2	R3	R4	R5	R6	R7	R8
Simulated	1705 Ω	568 Ω	10K Ω	10 K Ω	1705 Ω	568 Ω	10K Ω	10K Ω
Measured	1778 Ω	552 Ω	9.95K Ω	9.95K Ω	1778 Ω	552 Ω	9.96K Ω	9.93K Ω

Table 5: Simulated Resistance Values vs. Measured Values

Component	C1	C2	C3	C4
Simulated	33nF	22nF	33nF	22nF
Measured	22.6nF	33.2nF	24.8nF	22nF

Table 6: Simulated Capacitance Values vs. Measured Values

Theoretical analysis:

An active low-pass filter was designed to meet the project requirements. It was intended to be a 4th-order filter, so the Sallen-Key topology was employed, also known as the voltage-controlled voltage source configuration.

The design of the Sallen-Key filter is straightforward. For a first-order filter, it consists of two poles, meaning one capacitor and resistor pair. To achieve a second-order filter, additional poles can be added by incorporating another pair of capacitors and resistors. Consequently, increasing the number of resistor and capacitor pairs enhances the roll-off.

Two resistors, R3 and R4, connected in the feedback network, as illustrated in the figure below, they determine the gain of the filter. By adjusting their values, the gain can be either increased or decreased.

Two second-order filters can be cascaded to obtain a 4th-order low-pass filter. The operational amplifier 741 is utilized to amplify the output voltage to a level higher than the input voltage making this an active filter.

Transfer Function Derivation

To make a fourth order filter low pass filter, we cascade two second order Sallen-Key low pass filter stages. The transfer function of each stage can be derived separately, and their product will give the output of the 4th order filter. The equation below in the figure 9 is the transfer function of low pass 2nd order filter. By taking the square of this equation we can also get the transfer function of 4th order filter.

$$\frac{v_o}{v_i} = \frac{\frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s\left(\frac{1}{C_1}\right)\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) + \frac{1}{R_2 R_3 C_1 C_2}}$$

Figure 25: Transfer Function of 2nd Order Sallen-Key Lowpass Filter

Component Selection.

Referring to the figure below, choosing an appropriate value for the resistor and R3 and C1 to find the values for R4, C2, R2 and R1 is important. Furthermore, the value for Q (quality factor) and fc (cut off frequency) are also decided at the start. Following formulas in the figure 10 allow us to get the values of every component in the circuit.

- Choose R_3, C_1
- $R_4 = R_3/(K - 1)$
- Define $\alpha = \omega_0 C_1, \beta = \frac{1}{4Q^2} + (K - 1)$
- $C_2 = \beta C_1$
- $R_1 = 2Q/\alpha$
- $R_2 = 1/(2Q\alpha\beta)$

Figure 26: Filter Design Equations

R3 value chosen 10k and C1 was chosen 22nf with a cut off frequency of 6 KHz. Qualtiy factor was selected as 0.707.

The Value of R4 was calculated and value of k was chosen to be 2 .

$$R4 = R3/(k-1)$$

$$R4 = 10k/1$$

$$R4 = 10k$$

Beta (B)is calculated:

$$B = [1/4 * (Q^2)] + K - 1$$

$$B = [1/4 * (0.707^2)] + 2 - 1$$

$$B = 1.5$$

$$C2 = B * C1$$

$$C2 = 1.5 * 22\text{nf}$$

$$C2 = 33\text{nf}$$

Alpha(A) is calculated

$$W_o = 2 * \pi * f_c$$

$$W_o = 2 * \pi * 6k$$

$$W_o = 37699 \text{ rad/sec}$$

$$\text{Alpha} = W_o * C1$$

$$\text{Alpha} = 37699 * 22\text{nf}$$

$$\text{Alpha} = 829\mu$$

$$R1 = 2 * Q / \text{Alpha}$$

$$R1 = 2 * 0.707 / 829\mu$$

$$R1 = 1705 \text{ ohms}$$

$$R2 = (1/2 * Q) * \text{Alpha} * B$$

$$R2 = (1/2 * 0.707) * 829\mu * 1.5$$

$$R2 = 568 \text{ ohms}$$

$$\text{Gain} = 20 * \log(20) * 2$$

$$\text{Gain} = 12 \text{ dB}$$

Simulation results:

In order to test our filter, we want to see how it performs across a sweep of frequencies. In the figure below, we measure our output as we increment the input frequency signal from 1k Hz to 40K Hz. This test can validate two of our design parameters. We need to have a DC gain of at least 6 dB and a cutoff frequency between 4K Hz and 8K Hz. Below you can see how the filter output is above 6 dB on the top left. Focusing on the green dotted line, we can see how our phase changes as our input frequency increases. The cut off frequency for a low pass filter is said to be when the phase reaches 180 degrees. Looking under the graph, the measurement at -180 degrees is reached when the input frequency is 5.84K Hz. This somewhat verifies our design since we had accounted for a 6 KHz cut off frequency.

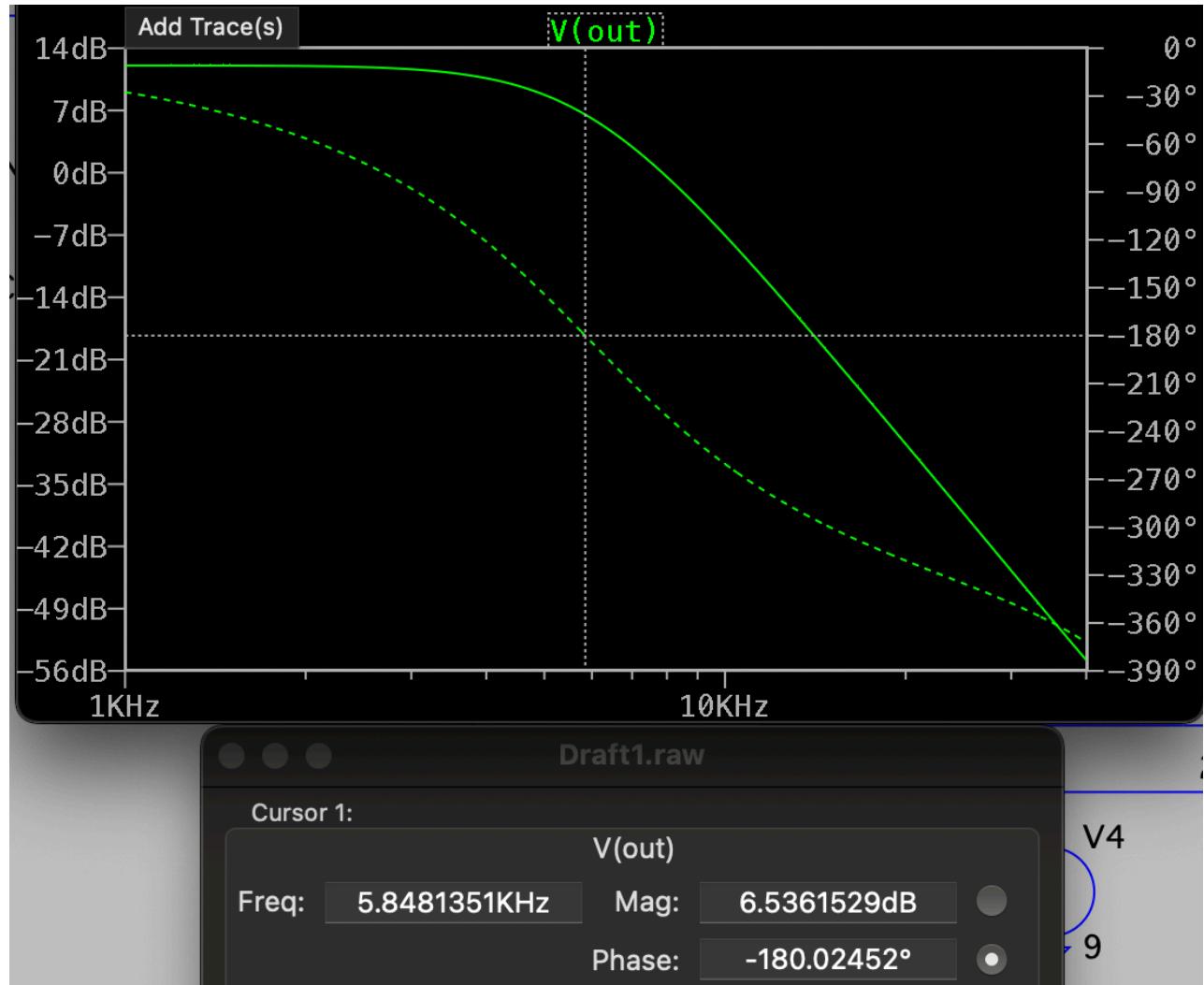


Figure 27: Simulation Lowpass Filter LTspice

Measurement results:

In order to test our filter in the lab, we need to sweep the input frequency. Unfortunately, we did not know how to do that on the oscilloscope wave generator, so we decided to take some points and measure our output voltage.

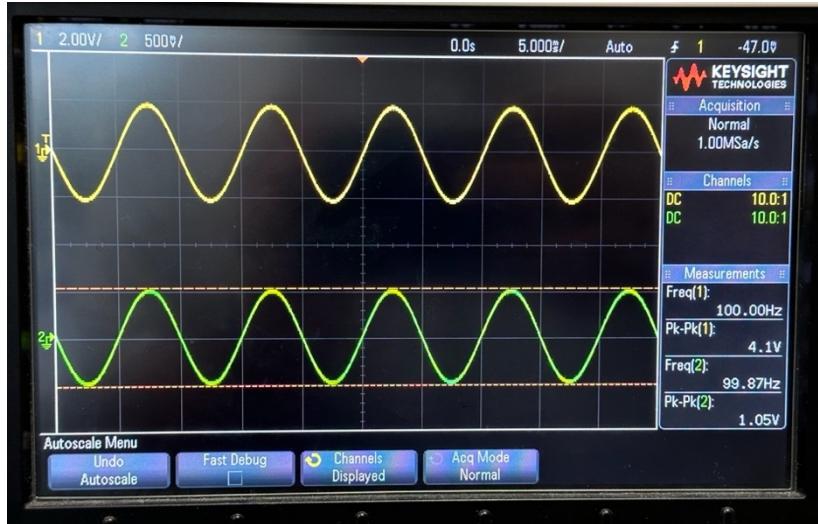


Figure 28: Filter Test at 100 Hz and Pk - Pk Values.

The yellow sine wave in Figure 12 shows the output of the low-pass filter, while the green wave represents the input waveform from the wave generator. It's clear that when a 100 Hz input with a Vpp of 1 volt is supplied to the filter, the output is amplified to 4.7 volts, and the signal passes through.



Figure 29: Filter Test at 7 KHz and Pk - Pk Values

When the frequency is increased to 7 kHz, it surpasses the cutoff frequency, and the Vpp starts to decline. This indicates that the signal begins to attenuate, as this low-pass filter was designed with a cutoff frequency of 6 kHz.

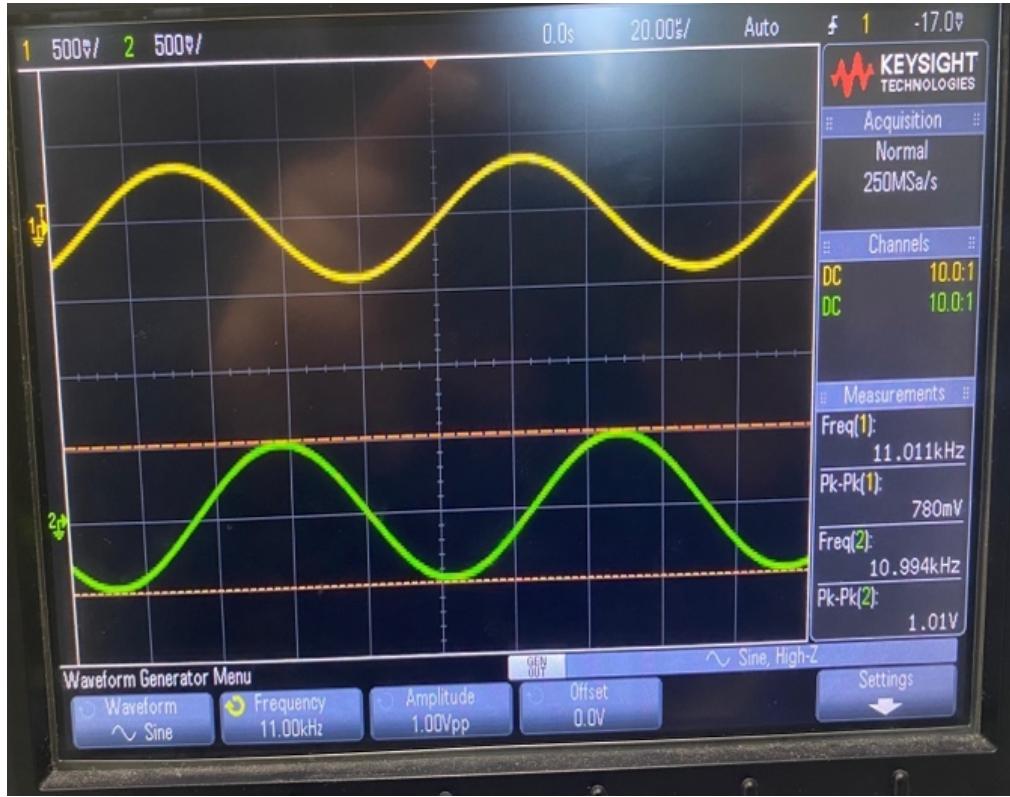


Figure 30: Filter Test at 11 KHz and Pk - Pk Values

As the frequency increases beyond the cutoff frequency of the low-pass filter, the attenuation becomes more pronounced. At 11 kHz, the signal's peak-to-peak voltage dropping to 780 mV suggests significant filtering action, where higher frequency components are being effectively suppressed. Observing this attenuation highlights the filter's effectiveness in shaping the frequency response according to its design parameters.

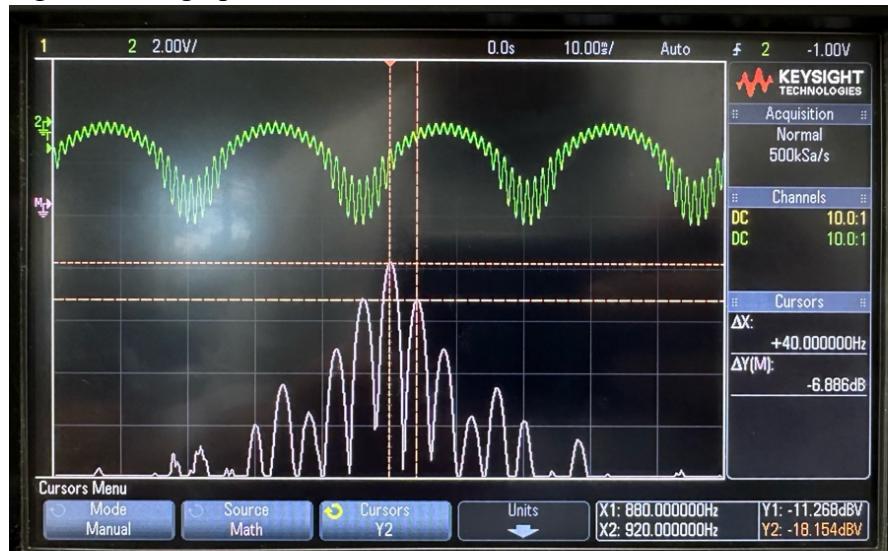


Figure 31: Filter Output with 880Hz and 40Hz Mixer Input.

Finally, we showcase out signals intended output during this stage. Since the FFT is centered around 880Hz we do not expect any loss of signal.

Pre-Amplifier

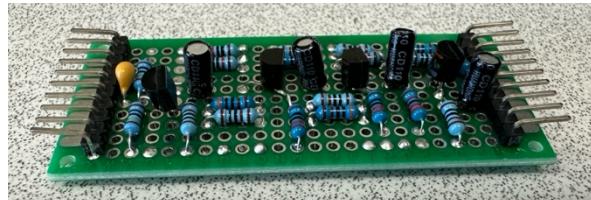


Figure 32: Pre-Amplifier PCB Board

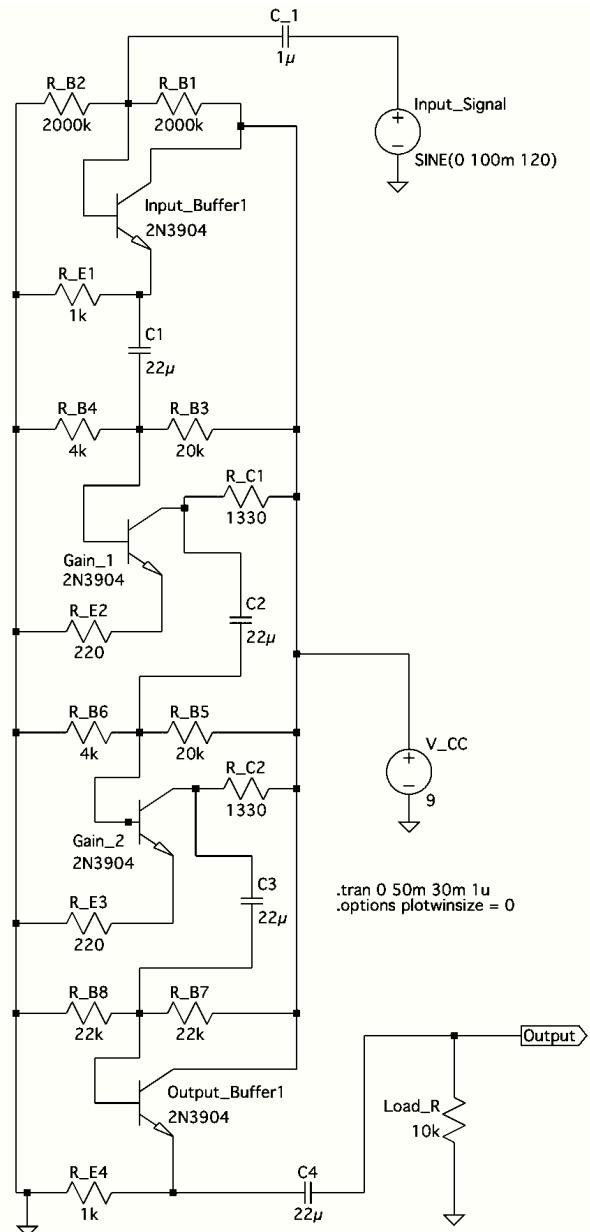


Figure 33: Simulated Amplifier Circuit Design on LTspice.

Component	R_B1	R_B2	R_E1	R_B3	R_B4	R_C1	R_E2
Simulated	2MΩ	2MΩ	1KΩ	20KΩ	4KΩ	1330Ω	220Ω
Measured	1894KΩ	1927KΩ	1.17KΩ	19.4KΩ	3.91KΩ	1403Ω	217Ω

Table 7: Simulated Vs. Measured Resistance Values

Component	R_B5	R_B6	R_C2	R_E3	R_B7	R_B8	R_E4
Simulated	20KΩ	4KΩ	1330Ω	220Ω	22KΩ	22KΩ	1KΩ
Measured	19.6KΩ	4.11KΩ	1297Ω	228Ω	22.01KΩ	22.01KΩ	986Ω

Table 8: Simulated Vs. Measured Resistance Values

Component	C_1	C1	C2	C3	C4
Simulated	1uF	22uF	22uF	22uF	22uF
Measured	1.056uF	22.156uF	22.097uF	22.045	1.073uF

Table 9: Simulated Vs. Measured Capacitance Values

Theoretical analysis:

The purpose for an amplifier is to increase the power of a signal without adding distortion. When it comes to this project we need to take into account a couple of considerations. Our audio amplifier must:

- Utilize a gain and buffer stage.
- Amplify input voltage signals with amplitudes between 10 and 100 millivolts.
- Amplify input signals between 120 Hz and 12K Hz.
- Produce a voltage gain of about 26 dB.
- Have a minimum input resistance of at least 100 KΩ.
- Have a maximum output resistance of 100 Ω.
- Consume less than 15 mA.

BJT Input Buffer:

Input buffers are used to isolate one section to another. They rely on their property of high input impedance and low output impedance to relieve stress on the signal source. In return, the signal is not really affected as it travels between different stages in the circuitry. In this case, we will use an input buffer to increase the input impedance of our pre-amplification circuit in order to meet our requirements of at least 100 KΩ resistance.

In order to determine the input resistance, we need to find a few parameters. To start I will determine r_e , this is the small signal emitter resistance.

$$r_e = \frac{25mV}{I_E},$$

Now we need to find I_E , which is the emitter current.

$$I_E = \frac{V_E}{R_{E1}} = \frac{V_B - V_{BE}}{R_{E1}} = \frac{\frac{9V}{2} - 0.7V}{R_{E1}} = 3.8mA$$

$$r_e = \frac{25mV}{3.8mA} = 6.58\Omega$$

Now we need to determine our equivalent emitter resistance with load. In this case, our load will be the input resistance to our next stage but for now we will just use the biasing resistors R_{B3} and R_{B4} as our load.

$$R_e = R_E || R_{B3} || R_{B4} = 1K\Omega || 20K\Omega || 4K\Omega = 769.23\Omega$$

Now we can determine the transistor base impedance. We will assume our transistor beta value is 150.

$$Z_{base} = \beta(R_e + r_e) = 150(769.23 + 6.58) = 116372\Omega$$

Finally, we can determine our input impedance:

$$\begin{aligned} Z_{IN} &= R_{bias} || R_{base} = 1M\Omega || 116372\Omega \\ Z_{IN} &= 103,942\Omega \end{aligned}$$

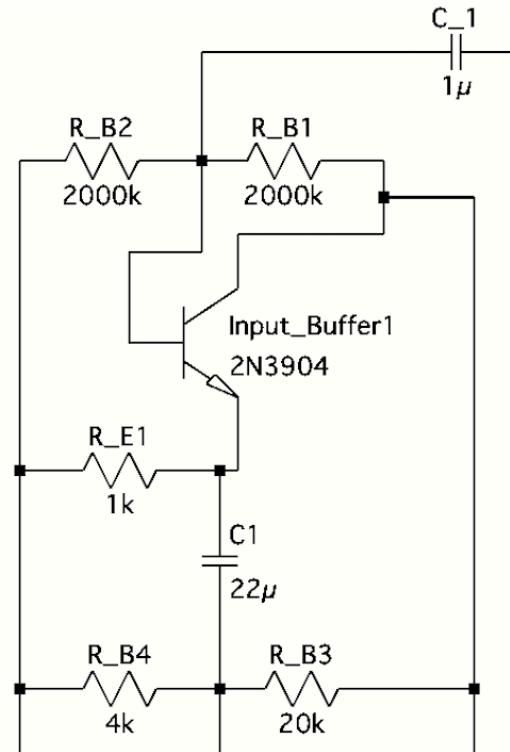


Figure 34: Pre-amplifier Input Buffer

BJT Dual Gain Stage

This part of the amplifier provides gain to the circuit. Both gain cells are identical providing slightly more than 26 dB gain. Each gain cell is designed to provide half of the gain. Ideally, we are looking for a voltage gain of negative 5.78 for each cell.

For Gain 1 we can see our gain as:

$$Gain = \frac{R_C}{r_e + R_E}$$

But our gain can be affected by the biasing resistors in the next cell. Assuming r_e is in the order of a couple ohms it is not that necessary to calculate it, so I use an arbitrary value such as 10. Without considering the resistors in the biasing network in the following stage our gain closely follows the equation above.

Stage 1:

Not considering the load resistance

$$Gain = \frac{1330}{220+10} = -5.78$$

Considering the load resistance

$$Gain = \frac{R_{C1} \parallel R_{B5} \parallel R_{B6}}{220+10} = -4.13$$

Stage 2:

Not considering the load resistance

$$Gain = \frac{1330}{220+10} = -5.78$$

Considering the load resistance

$$Gain = \frac{R_{C2} \parallel R_{B7} \parallel R_{B8}}{330+10} = -5.16$$

Total Gain	$-5.78 * -5.78 = 33.4$	$-4.13 * -5.16 = 21.31$
Stage 1 X Stage 2	no load	w/ load

26dB is equivalent to gain of 20V/V.

This means that our realized gain is substantially smaller than we thought, but this is a tradeoff necessary in order to establish the following buffer stage which uses smaller biasing resistors. Even so, we were barely able to meet this requirement since the buffer stage takes up a little of the gain.

This method that we used allowed us to determine the collector and emitter resistors.

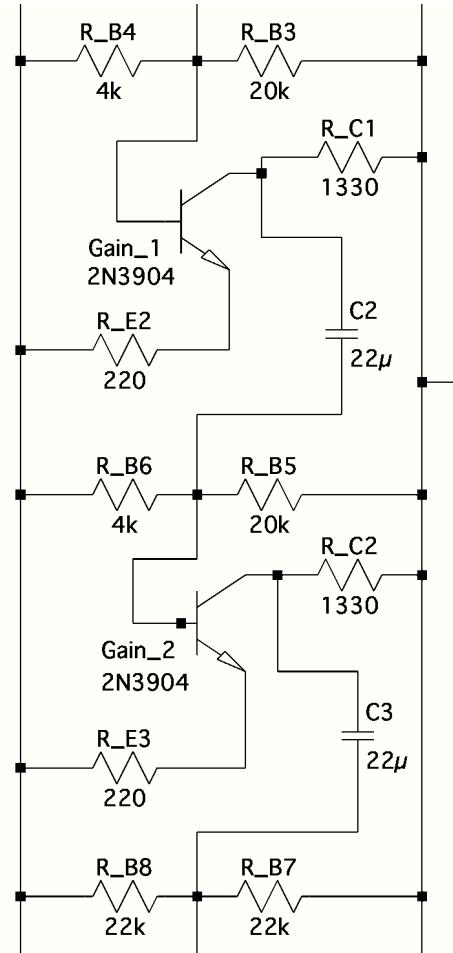


Figure 35: Pre-Amp Gain Stage

Biasing Network

When it came to determining what resistors to use in our biasing network, we took a guess and check approach. Initially we did the analysis and found that it worked for the 120 Hz case with 10 mV but did not for the 100mV case. After struggling some time with it, we decided to use LTspice to help us find a resistor combination that could satisfy all the requirements.

Q-Point

The q point is determined during DC analysis. It is what helps us track how much swing we can have in our transistor amplification. In this case, we decided to set the beta to 150.

First, we determine the base voltage:

$$V_{BB} = V_{CC} \frac{R_{B4}}{R_{B3} + R_{B4}}$$

$$V_{BB} = 9 \frac{4K\Omega}{4K\Omega + 20K\Omega} = 1.5V$$

Now we determine the parallel bias resistance:

$$R_B = R_{B3} \parallel R_{B4}$$

$$R_B = 4K\Omega \parallel 20K\Omega = 3333\Omega$$

Now we can determine the current q point:

$$I_{EQ} = \frac{V_{BB} - V_{BE}}{\frac{R_B}{\beta + 1} + R_E}$$

$$I_{EQ} = \frac{1.5 - 0.7}{\frac{3333}{151} + 220} = 3.3mA$$

Finally, we can find the voltage q point:

$$V_{CEQ} = V_{CC} - I_{EQ}(R_C + R_E)$$

$$V_{CEQ} = 9 - 3.3mA(1330 + 220) = 3.89V$$

The q point voltage ranges from 0 to 9 volts. If we were to run into an issue, it would be on the lower bounds where 3.89V is close to 0V. I would assume this means our lowest voltage swing can only spare an additional 3.89V.

The q point current ranges from 0 to 6.77mA (V_{CC} / R_C).

BJT Output Buffer

The purpose of the output buffer is to isolate the gain stage from the output stage. If this isolation does not exist, the impedance from the output stage will affect the gain of the amplifier. One of our design parameters is to have an output impedance of less than $100\ \Omega$.

In order to determine the output resistance of the buffer, we need to determine the beta value of the transistor. The 2N3904 transistor datasheet says it has a beta value between 70 and 300 at 1mA collector current. In our case the collector current is about the same as the emitter current.

The base current can be found using the input voltage and the biasing resistors R_{B7} and R_{B8} .

$$I_B = \frac{9V}{22K + 22K} = 0.205mA$$

The emitter current is the current that travels through R_E4 while the emitter voltage is active. Using KVL, the emitter voltage is:

$$V_E = V_B - V_{BE}$$

In order to find the base voltage, we multiply R_{B8} by the base current and assume the base emitter voltage to be 0.7.

$$V_B = I_B * R_{B8} = 205\mu A * 22K\Omega = 4.51V$$

$$V_E = 4.51V - 0.7V = 3.81V$$

Now we can determine the emitter current.

$$I_E = \frac{V_E}{R_{E4}} = \frac{3.81V}{1K\Omega} = 3.81\ mA$$

Since we can assume the beta value is between 70 and 300. I will take the midpoint of 185.

$$\beta = 185$$

Now that we have found the emitter current, we can also find the emitter's internal resistance.

$$r_e = \frac{25mV}{I_E} = \frac{25mV}{3.81mA} = 6.56\Omega$$

Finally in order to determine the output impedance we can use the following equation.

$$\text{Output Resistance} = R_E \parallel (r_e + \frac{R_{B7} \parallel R_{B8}}{\beta+1})$$

$$1K\Omega \parallel \left(6.56 + \frac{22K\Omega \parallel 22K\Omega}{185+1} \right) = 65.70\Omega$$

Now this circuit can handle any output resistance load. We can simulate a $10K\Omega$ load to see how the output resistance is affected.

$$Z_{out} = R_{LOAD} \parallel R_{Output}$$

$$10K\Omega \parallel 65.70\Omega = 65.27\Omega$$

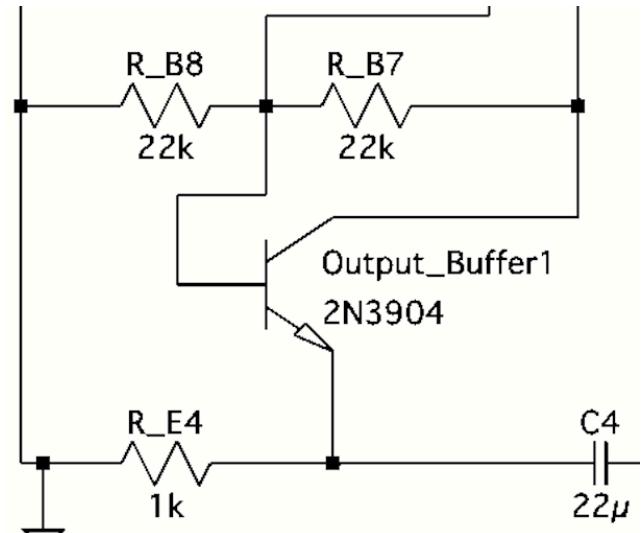


Figure 36: Amplifier Buffer Stage

Simulation results:

Using LTspice we are able to show how we meet the following design criteria.

- Amplify input voltage signals with amplitudes between 10 and 100 millivolts.
- Amplify input signals between 120 Hz and 12K Hz.
- Produce a voltage gain of about 26 dB.
- Consume less than 15 mA.

120 Hz test:

10 mV peak

Here we can see the max current draw is 12.7mA and the gain is at 26 dB.

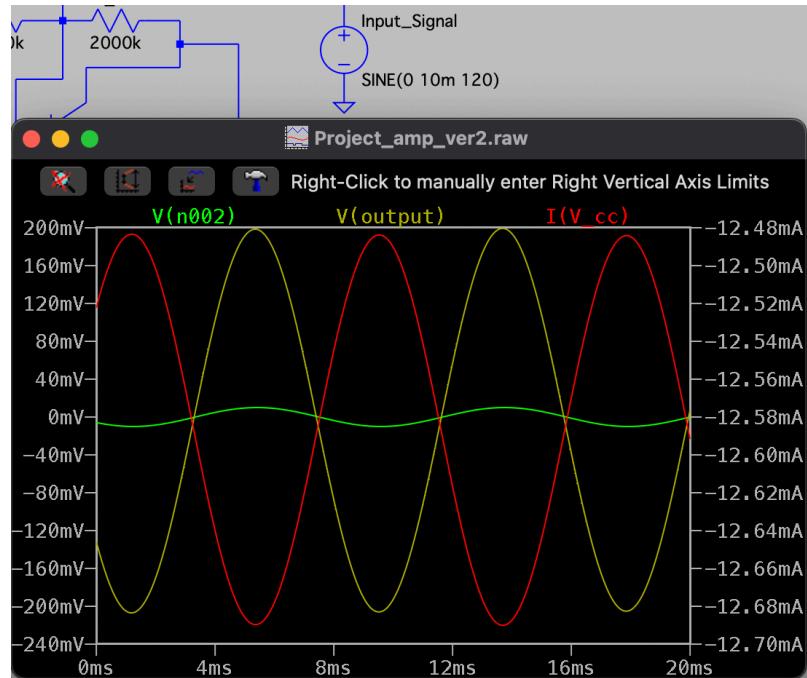


Figure 37: 120 Hz simulation test at 10mV.

100 mV peak

Here we can see the max current draw is 13.6mA and the gain is at 26 dB.

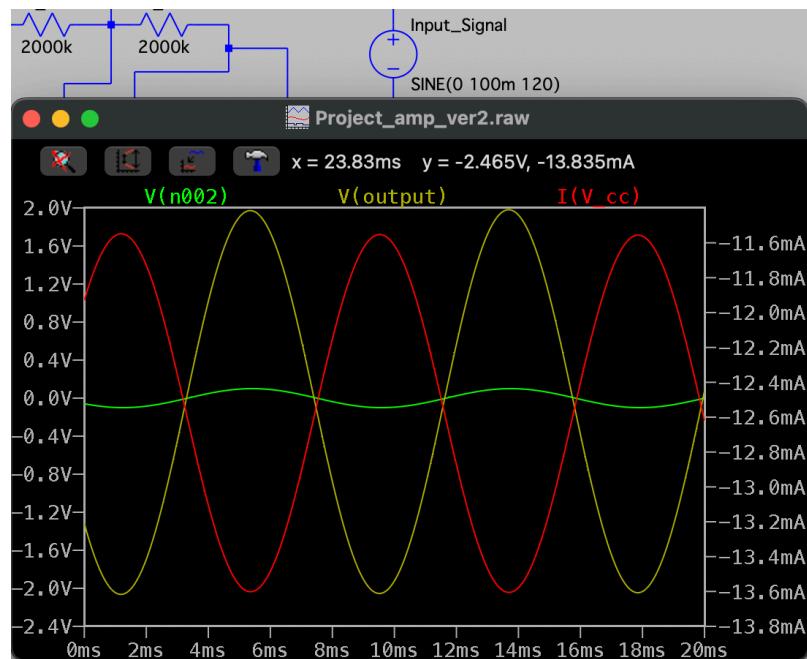


Figure 38: 120 Hz simulation test at 100mV.

12 KHz test:

10 mV peak

Here, the max current draw is 12.69mA and the gain is at 26 dB.

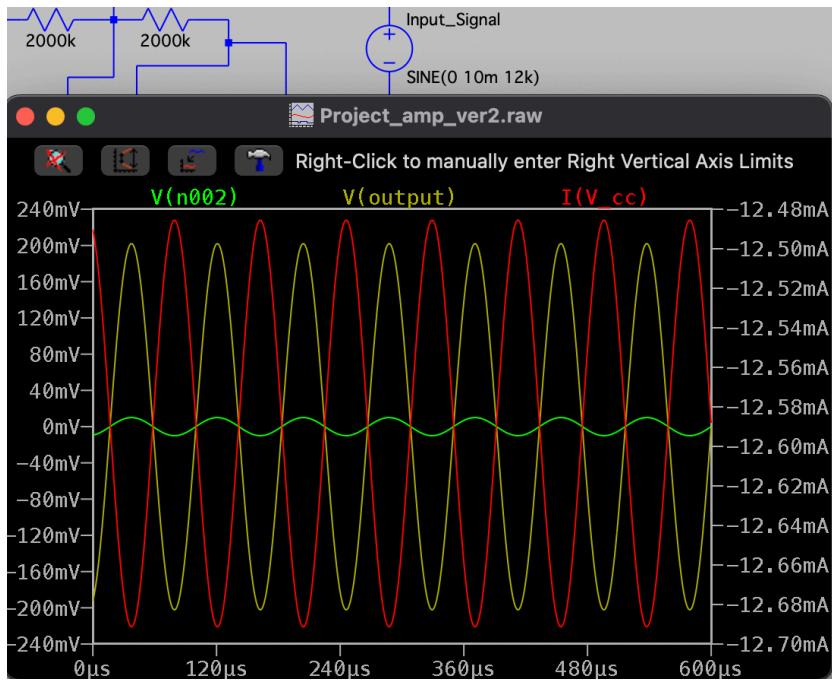


Figure 39: 12 KHz simulation test at 10mV.

100 mV peak

The max current draw is 13.6mA and the gain is at 26 dB.

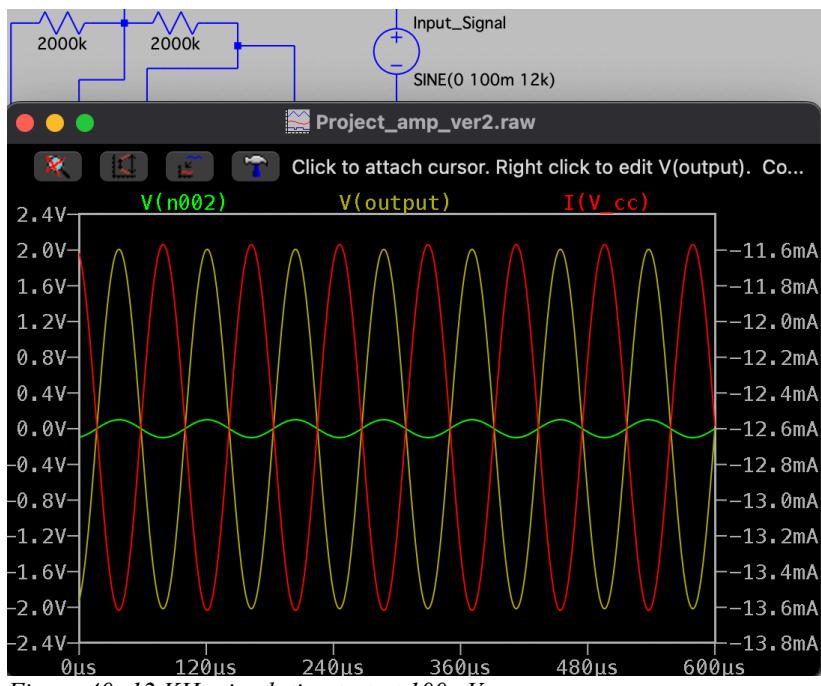


Figure 40: 12 KHz simulation test at 100mV.

Overall, our current draw hoovered around 13mA, and the gain was sustained at 26 dB.

Measurement results:

We perform similar test as the ones done on LTspice. Since the wave generator did not produce 10 mV peak sine wave, we only tested the 100-mV signal and its current draw.

This test is the 100mV signal with 120 Hz. We can see how signal goes over 2V.



Figure 41: Oscilloscope 120 Hz test at 100 mV

This test is the 100mV signal with 12 KHz. The results are similar, and the gain is close to 26 dB.



Figure 42: Oscilloscope 12 kHz test at 100 mV

The DC power supply lets us know how much current our circuit is drawing. In this case, it is drawing 12mA.



Figure 43: Power Supply Reading while Circuit under test.

Class D Amplifier

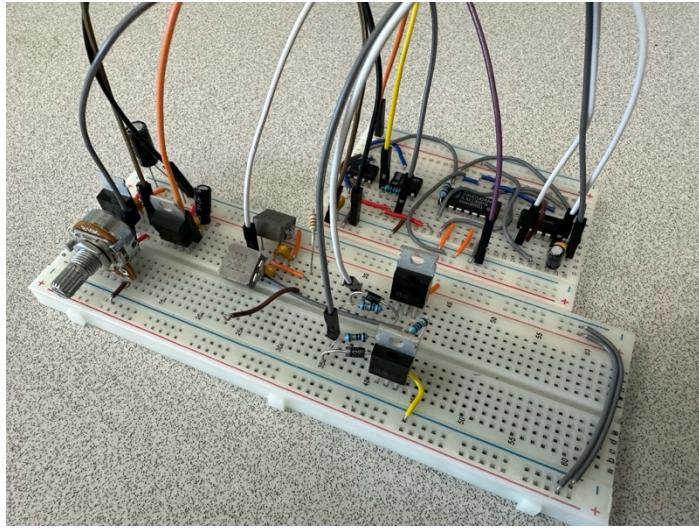


Figure 44: Class D Amplifier Breadboard Testing

The purpose of this amplifier is to further boost the signal. This type of amplifier is known for its high energy efficiency typically greater than 85%. These types of amplifiers work on the basis that they are switched on and off when needed. Meaning that they do not waste energy when an input signal is not present. In this case, the TLC555 provides the switching frequency of 240 KHz, which is well out of the audible hearing range. Next, the triangular switching frequency is combined with the input signal and fed to the LM393 comparator. This comparator creates a digital signal depending on which signal is larger. Then this digital signal is inverted by a 74HC04 inverter. Now that we have our digital signal and an inverted version, we feed these to our IR2113 which is a mosfet driver. This driver is responsible for setting proper voltage and current requirements for the IRLZ44N a power mosfet. This driver drives the mosfet in the most efficient and effective way while preserving high switching speed capability. Lastly, there is a simple LC low pass filter to remove the high frequency components generated by the amplification process.

Simulation:

Unfortunately, I was not able to get the simulation to work. I was able to find all the components necessary to run the simulation but there must have been a hiccup in the installation process.

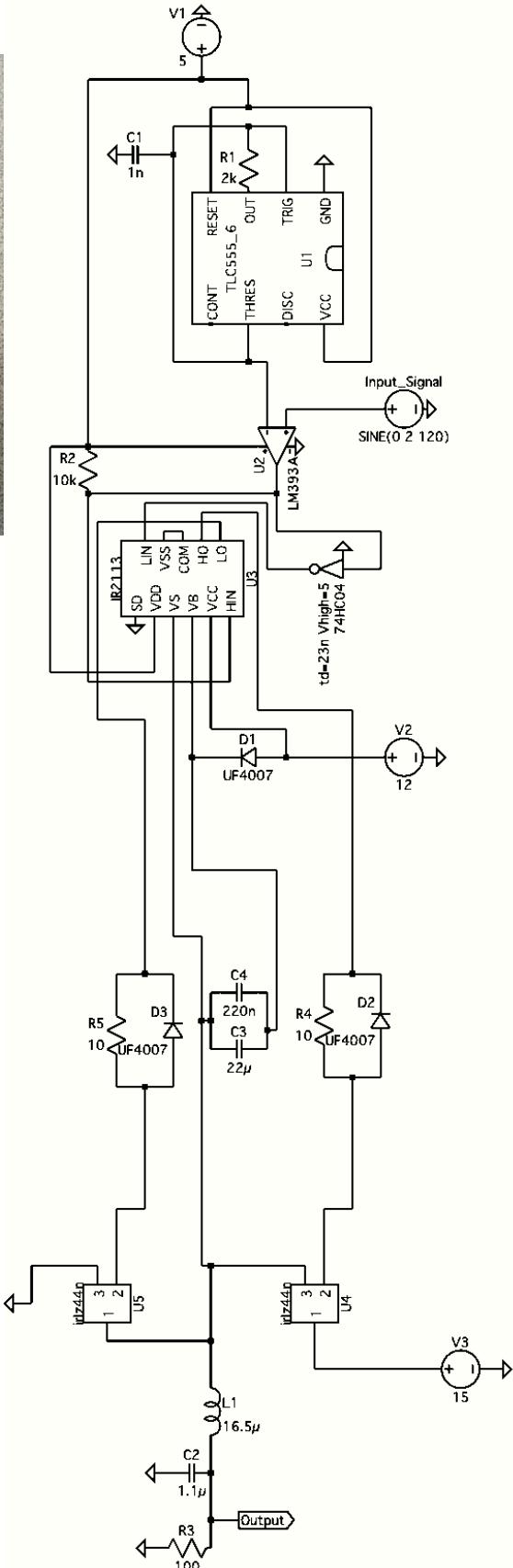


Figure 45: Class D Amplifier on LTspice.

Component	R1	R2	R3	R4	R5
Simulated	2KΩ	10KΩ	100Ω	10Ω	10Ω
Measured	1.97KΩ	10.04KΩ	108Ω	9.6Ω	9.6Ω

Table 10: Measured Vs. Simulated Resistance Values

Component	C1	C2	C3	C4	L1
Simulated	1n	1.1μ	22μ	220n	16.5μ
Measured	0.98n	1.17μ	21.75μ	228n	16.1μ

Table 11: Measured Vs. Theoretical Capacitance and Inductance Values

Measurement results:

The following are results taken from directly feeding the amplifier with a sine wave of 2 volts peak to peak with various frequencies.



Figure 46: 100 Hz test (yellow) and output (green).



1 KHz input signal with 2V peak to peak has a gain of 3.67.

Figure 47: 1 KHz test (yellow) and output (green).

5 KHz input signal with 2V peak to peak has a gain of 2.41.



15 KHz input signal with 2V peak to peak has a gain of 1.74.

Conclusion:

After spending some time trying to figure out the cause of the noise, I found the driver to be the cause. I can only assume the driver was not properly set. I did try replacing the driver and the power mosfets but that did not solve the issue. Another thing to mention is that as I increase the frequency, the amplitude of the signal drops. The more I increased it past 15 KHz it actually maintained about a 2V increase over the initial signal. Similarly, the more I increased the frequency, the more the noise increased. I believe this amplifier is more suited for a mid-bass application because it amplifies better at the lower range in a cleaner fashion.

10 KHz input signal with 2V peak to peak has a gain of 2.05.



Complete Implementation

In the demonstration, the oscillator and the low frequency oscillator output signals are fed into the mixer. There are three cases we want to investigate at each output of every stage. We will keep one input of the mixer set at 6.8 KHz using the oscillator, and the other input will vary. The low frequency oscillator will output 3 signals and we want to see how those signals change as they move throughout our circuit. The first signal is a 180Hz sine wave, the second is an 80Hz triangular wave and the last is a 5Hz square wave. All of our input signals to our mixer must be greater than 500mV.

Case 1:

Oscillator: 6.8 KHz sine

Low frequency Oscillator : 180 Hz sine

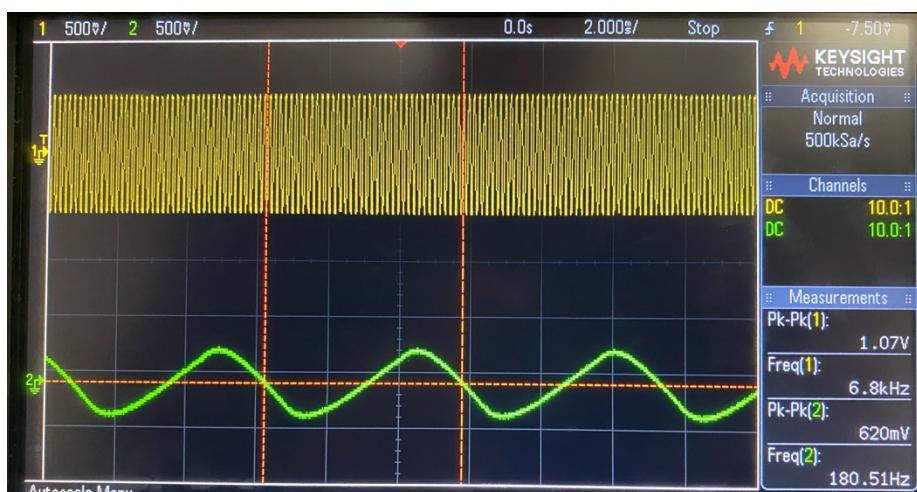


Figure 51: Input Signals into Mixer.

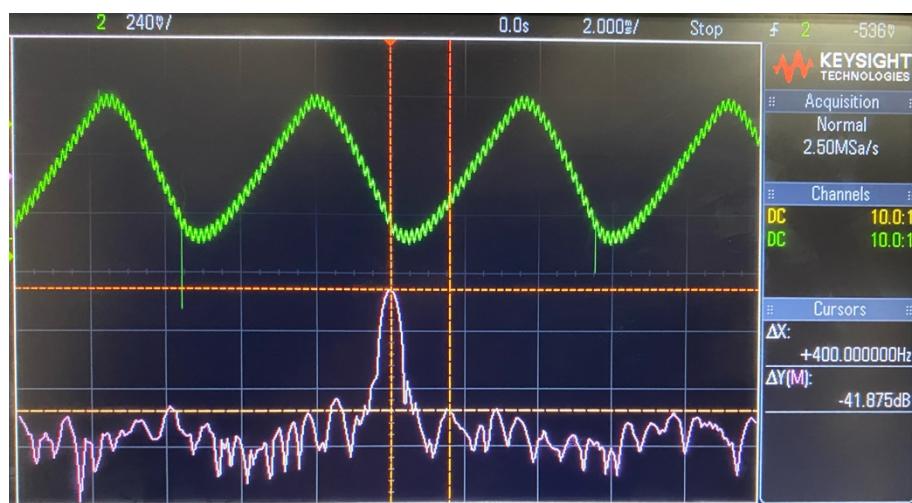


Figure 52: Mixer Output.



Figure 53: Filter Output

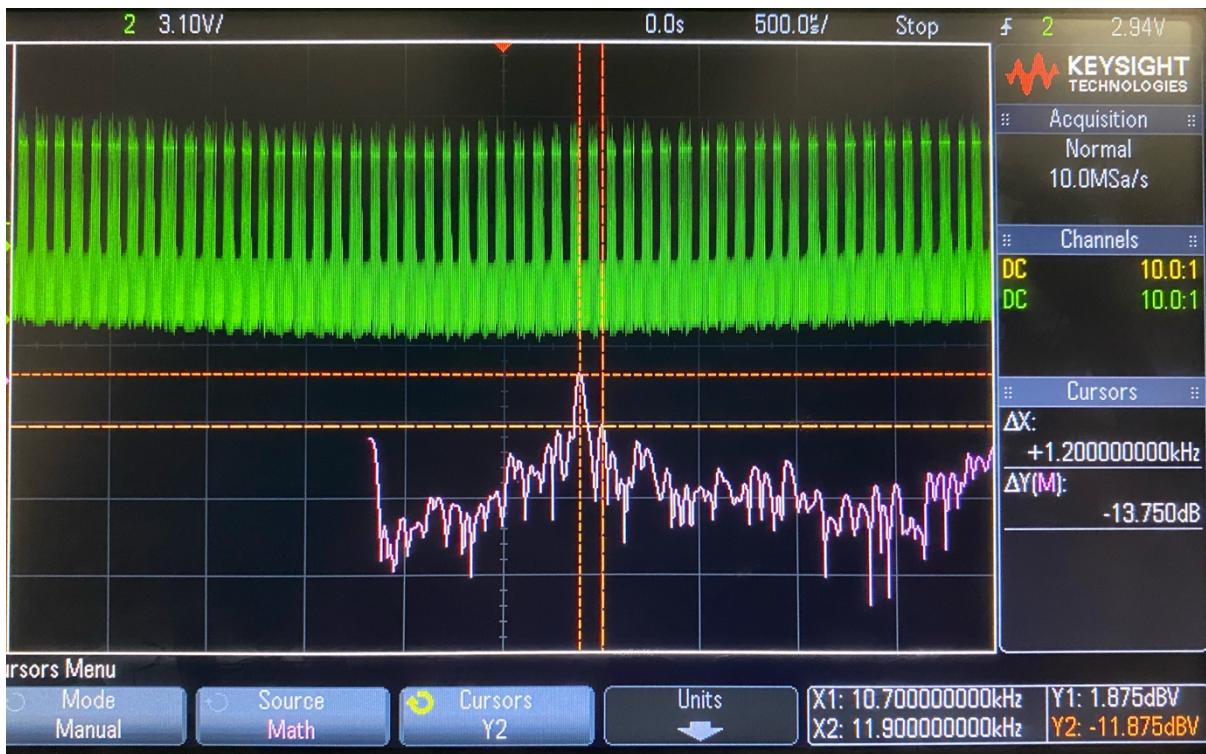


Figure 54: Pre-Amplifier Output.

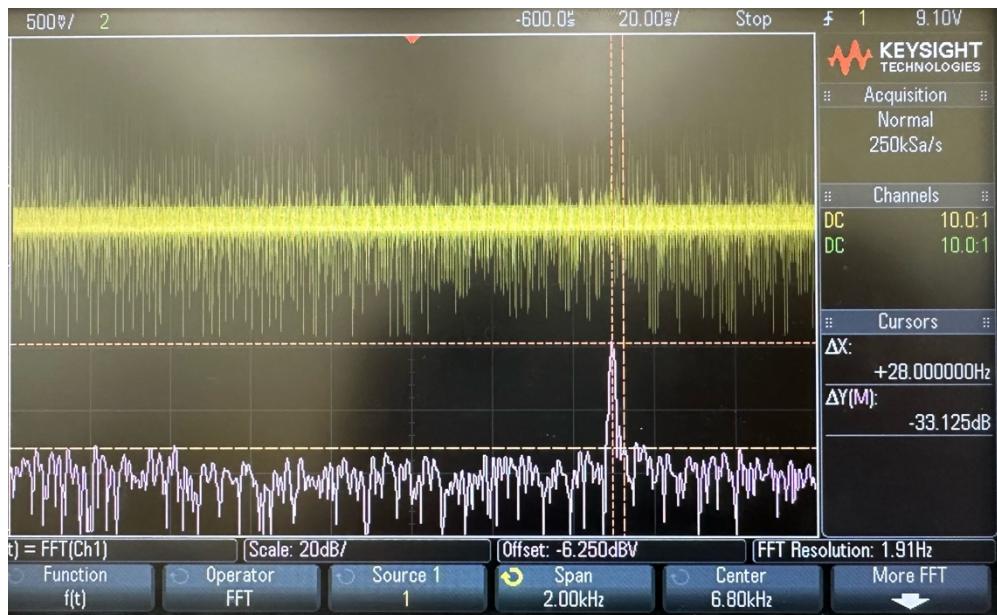


Figure 55: Class D Amplifier Output.

Case 2:

Oscillator: 6.8 KHz sine

Low frequency Oscillator : 80 Hz triangular wave



Figure 56: Mixer Input.

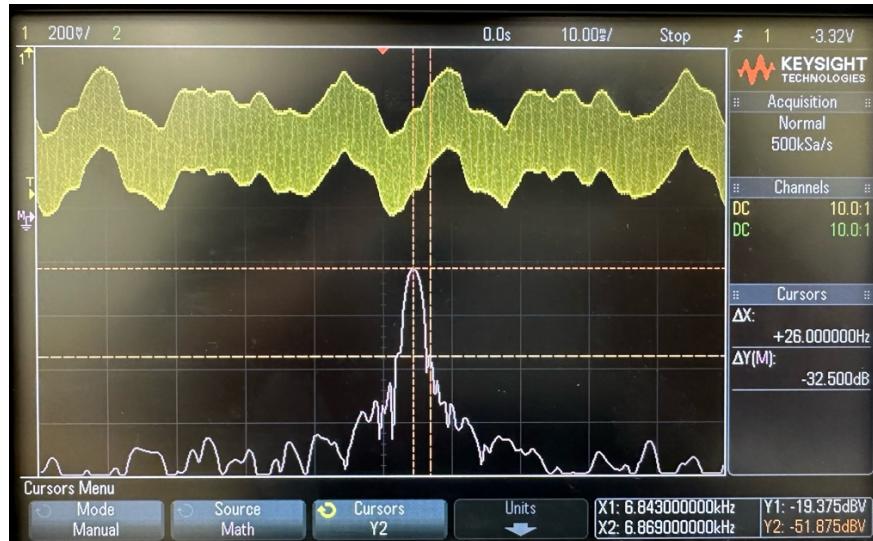




Figure 60: Class D Amplifier Output

Case 3:

Oscillator: 6.8 KHz sine

Low frequency Oscillator : 5 Hz square wave

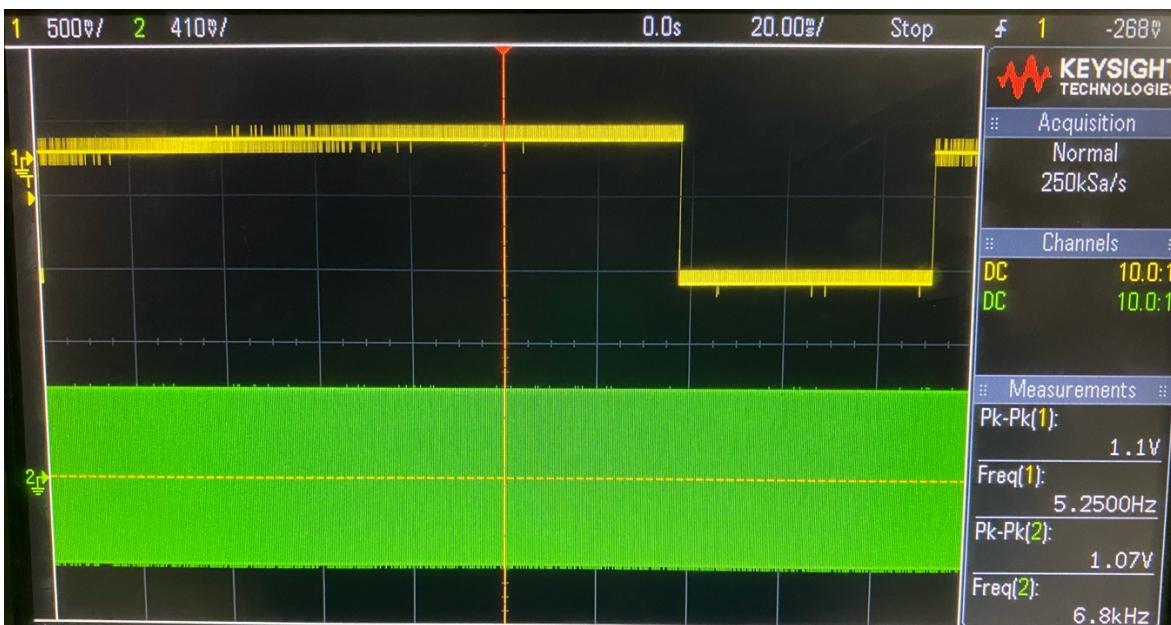


Figure 61: Mixer Input

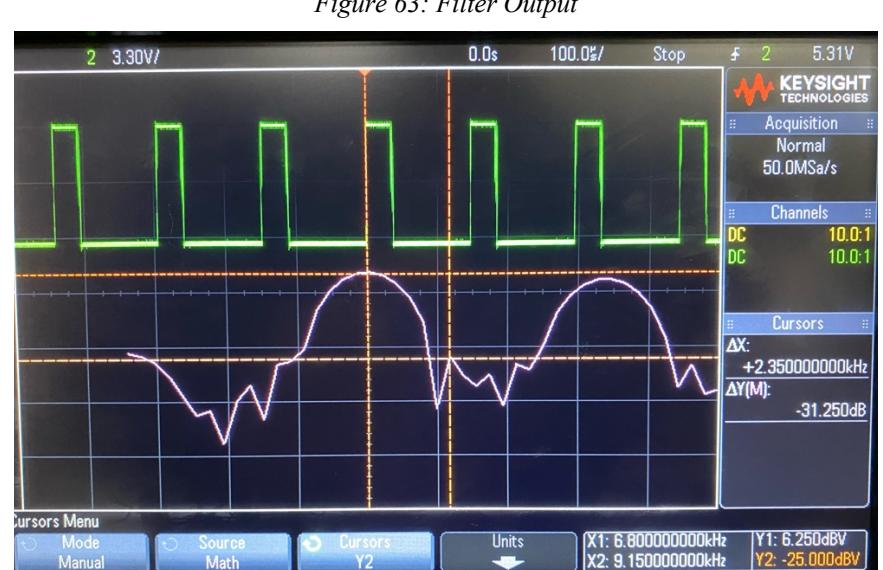
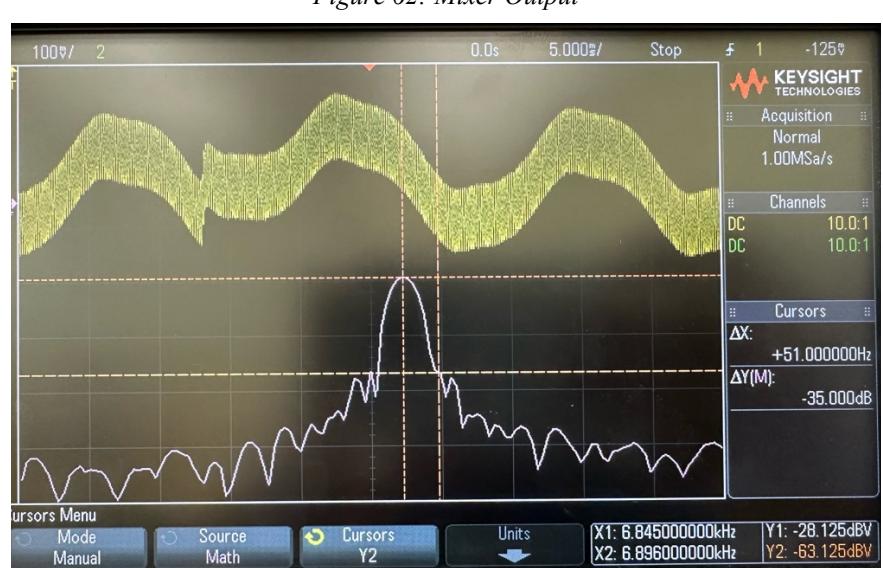
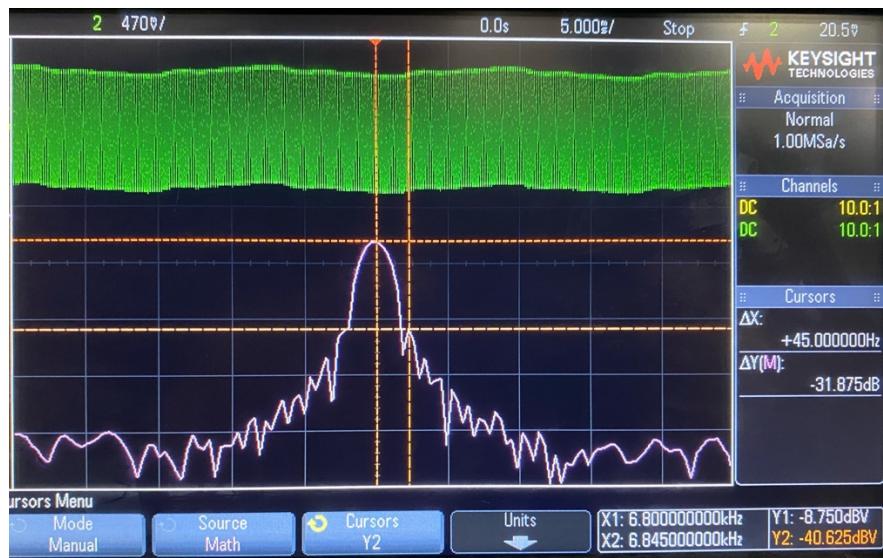




Figure 65: Class D Amplifier Output

Discussion

Every block of the circuit was designed to meet the specific requirements of the project. The oscillator was designed to perfectly output 6.8 KHz in order for us to test the effectiveness of our 6 KHz low pass filter. Additionally, the low frequency oscillator was used to experiment with the effects of different types of signals and how they combine in the mixer with a sine wave. The mixer was used to combine two signals effectively. Through careful adjustments of component values in LTspice, we successfully achieved this objective, ensuring the seamless integration of multiple input signals.

In the case of the filter, our goal was to achieve a gain greater than 6dB while providing flexibility in selecting the cutoff frequency. We were afforded the freedom to choose the cutoff frequency within the range of 4 KHz to 8 KHz, and after careful consideration, we opted for the mid-value of 6 KHz. Additionally, to ensure optimal performance, we selected a quality factor of 0.707.

To simplify the design and implementation process of the low-pass 4th order filter, we employed the Sallen-Key topology. This topology offers sharp roll-off and accurate frequency control.

Similarly, the choice of a dual-gain stage amplifier with an output buffer was made to ensure sufficient signal strength while minimizing output impedance. We were not able to meet the input impedance criteria, but it is something that can be easily fixed. Another thing to note, would be if we could slightly increase the gain on the amplifier to overcome the losses from the buffer.

In terms of implementation trade-offs, we carefully balanced the need for signal fidelity with complexity. For example, the decision to use the Sallen-Key topology for the low-pass filter was

driven by its ability to achieve sharp roll-off and accurate frequency control, despite the added complexity compared to simpler filter designs. Similarly, the choice of a dual-gain stage amplifier with an output buffer was made to ensure sufficient signal strength while minimizing output impedance.

Lastly, our Class D Amplifier was meant to take an already sufficient signal and power it even more. In this case, it showed promising results under 1 KHz. If I were to keep this design, I would make a proper low pass filter with a 800 Hz cut off frequency.

Overall, our design and experimentation process involved a careful balance of trade-offs to achieve a part of synthesizer circuit capable of meeting the specified signal processing requirements while remaining adaptable for future enhancements and applications.

Conclusion

Through the design and implementation of 6 blocks synthesizer circuit comprising an oscillator, low frequency oscillator, mixer, low-pass filter, amplifier and output stage we have gained valuable knowledge related complexities of signal processing and circuit design. Our experience has reinforced the importance of balancing design choices, considering trade-offs, and conducting thorough experimentation on both breadboard and simulation software like LTspice.

We have learned that each component of the circuit plays a critical role in achieving the desired signal processing objectives, and careful consideration must be given when changing the values for components in the circuit like resistors and capacitors. For instance, a slight change in the value of the of any component could give unexpected results at the output.

Overall, this experience has deepened our understanding of circuit design principles and provided a solid foundation for further exploration and development in the field of circuit designing.