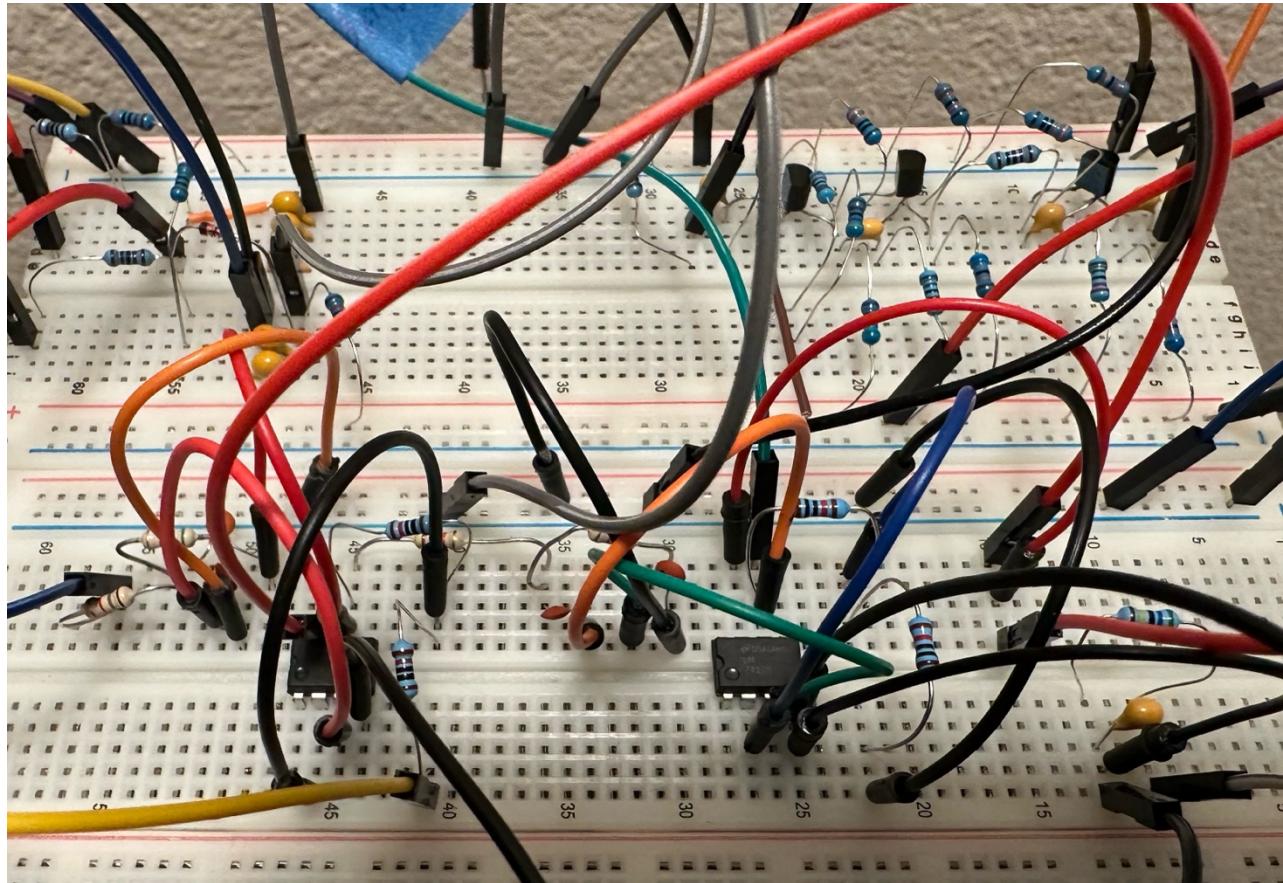


Synthesizer Halfway Point

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Abstract

The goal of this project is to design, test, and develop an Audio Synthesizer. This report is an overview of the first half of the design and validation process. Here we cover 3 parts of this project, the mixer, the low pass filter, and the amplifier. The mixer is a simple single diode mixer with 40 Hz and 880 Hz inputs for testing. The low pass filter is a 4th order Sallen-Key filter that uses two opamps to achieve a dc gain of 12 dB with a cut off frequency of 6 KHz. Finally, the amplifier stage is comprised of two BJT gain stages and a single output BJT buffer that achieves 26dB gain from 120 Hz to 12 KHz and from 10 mV to 100 mV peak to peak.

Introduction

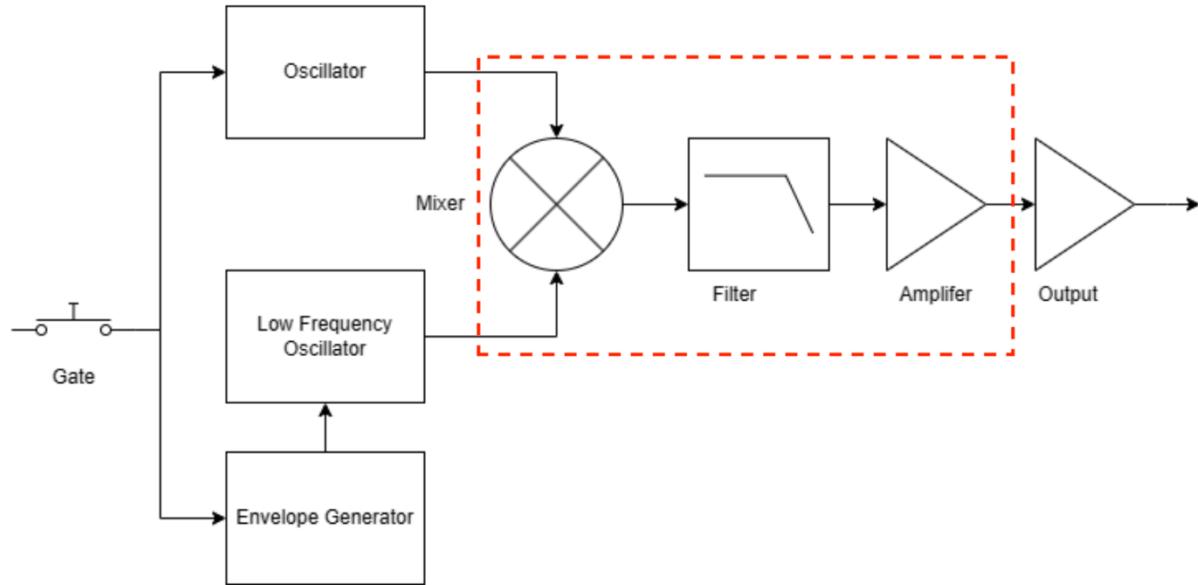


Figure 1: Project audio synthesizer overview. Red lines indicate the sections this report will focus on.

In order to create an audio synthesizer, we initially focused on these three sections. A mixer is generally used to alter the frequency of a signal. It takes two signals and creates new ones based on the addition and subtraction of the initial signals. In our case, we want to take advantage of this property to increase the number of signals produced effectively increasing harmonic distortion. This will allow us to create new sounds from two signals. In order to keep all the signals in the audible range, we use a low pass filter to remove any signals that are not audible. The Sallen-key fourth order low pass filter is an active filter that boost the DC signal by 12dB and removes signals above a specified cutoff frequency. It is important to use an active filter because we want to also preserve the harmonic distortion under the filter's 6 KHz cutoff frequency. After removing the excess signals, we amplify what is left over and prepare it for an output stage. The amplifier has a dual gain stage with an output buffer that lowers the output resistance to about 40 ohms.

Components Used:

Mixer

1 1N4148 Diode	4 Resistors	2 capacitors
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Filter

2 LM741 OpAmp	8 Resistors	4 capacitors
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Amplifier

3 2N3904 NPN
Transistor 13 Resistors 4 capacitors

Mixer

The Mixer is a widely used component used to shift signals around in the frequency spectrum. This is important because it allows us to change a signal frequency. The mixer by itself does not change frequency, it simply creates many variations of the original signal and the local oscillator that need to be filtered out. The filter is what allows you to choose what signals we will be taking from the mixer's output.

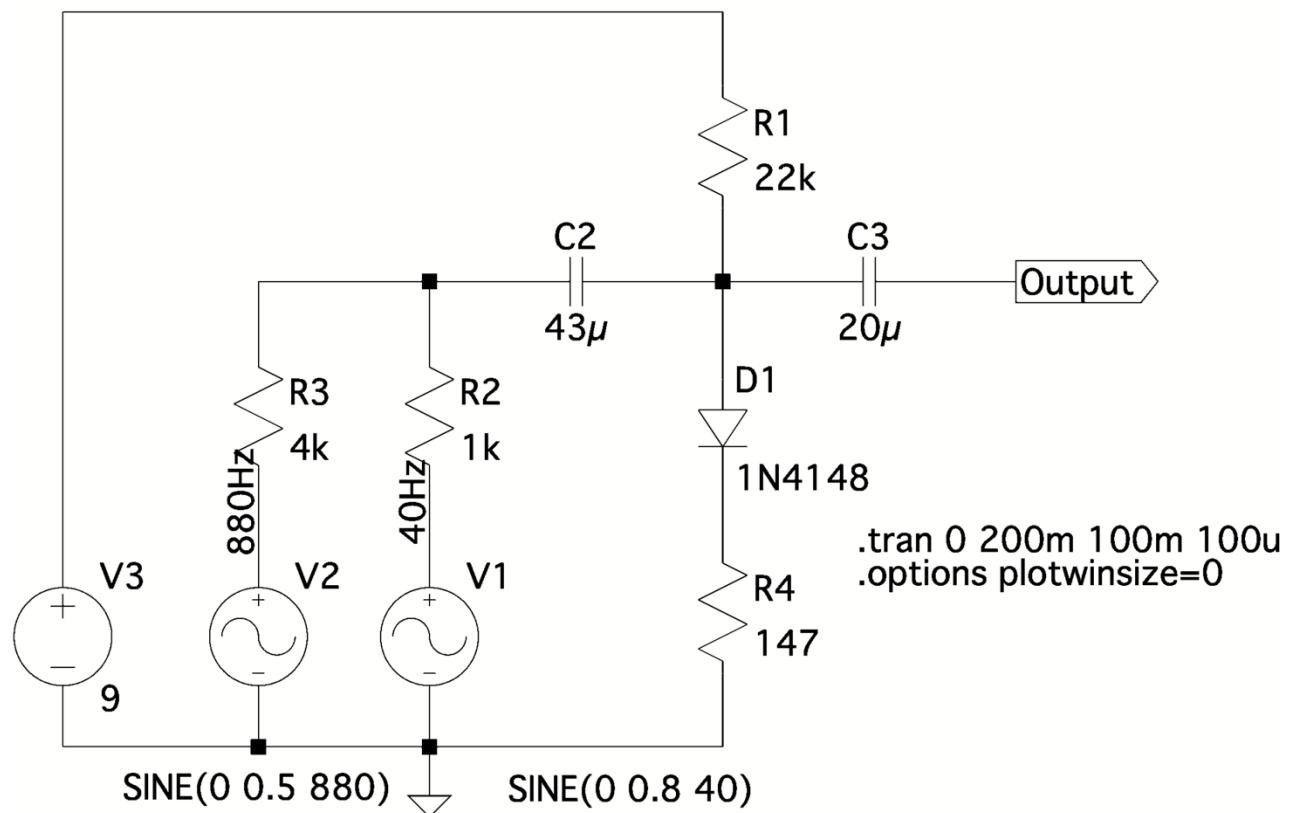


Figure 2: Simulated Circuit Diagram for Mixer on LTspice.

Component	R1	R2	R3	R4	C2	C3
Simulated	22K Ω	1K Ω	4K Ω	147 Ω	43u F	20u F
Measured	21.5K Ω	996 Ω	3.926K Ω	147.8 Ω	42.39u F	20.48u F

Table 1: Simulated Values Compared to Measured Values

Simulation results:

Before building our circuit, we wanted to make sure that we could simulate and meet our design criteria. This circuit must use 880 Hz 2-V peak-to-peak signal and a 40 Hz 2-V peak-to-peak signal. It must also have a conversion loss less than 23 dB. Based on these requirements we have a lot of liberty to choose resistance and capacitance values that will generate the most harmonic distortion. The figure above shows the circuit we simulated, and the figures below shows its inputs and output signals.

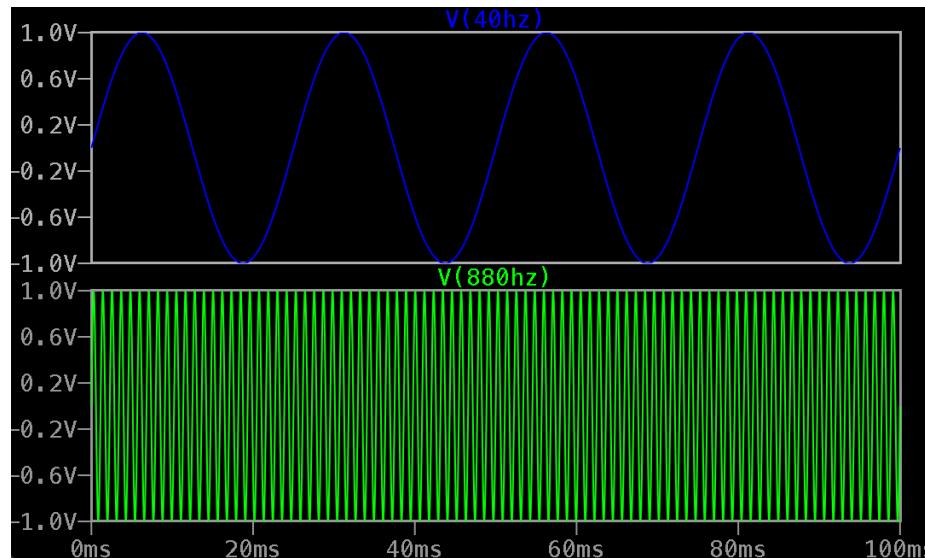


Figure 3: Input Signals, Blue 40 Hz and Green 880 Hz.

Since the 880 Hz rides on top of the 40 Hz, we found a sweet spot using $1 \text{ K}\Omega$ and $4 \text{ K}\Omega$ resistors. These resistors allow us to adjust the strength of each signal's intensity.

This output signal contains more frequencies than just 40 Hz and 880 Hz. It was purposely designed to create as many additional harmonic frequencies.

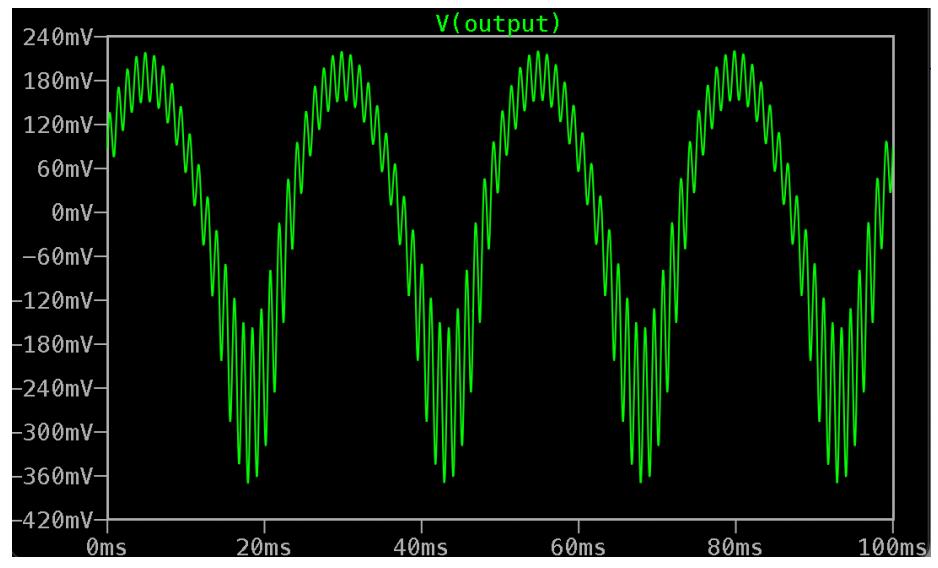


Figure 4: Mixer Output Signal

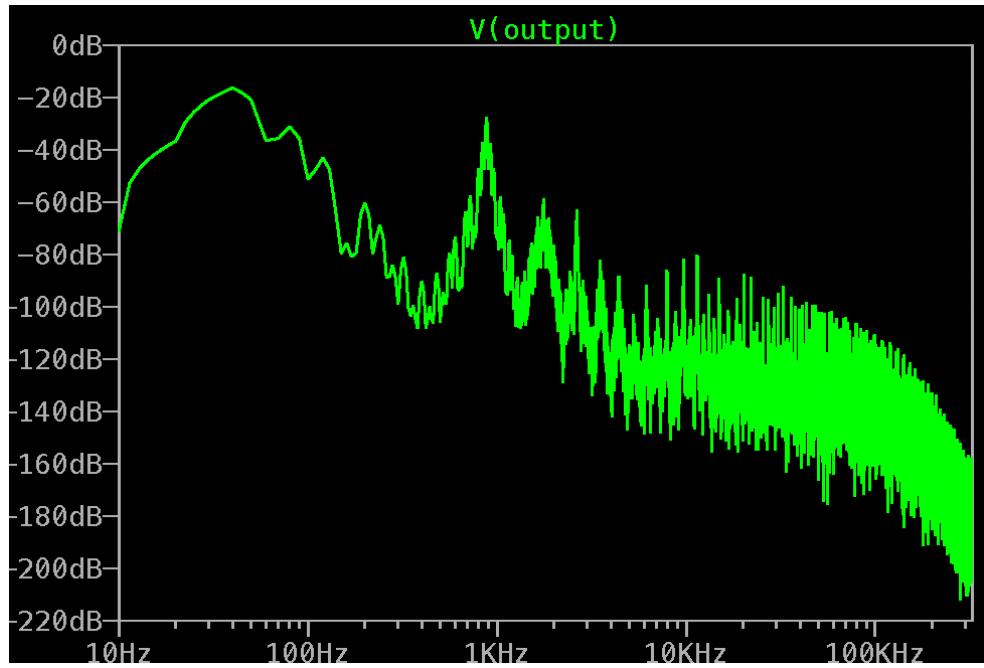


Figure 5: Mixer Output Signal FFT w/Blackman Window.

This plot shows the frequency content of the signal. You can see that additional signals were created but most are not powerful enough for considerable contribution to our signal. Our input signals have the highest strength while the rest are derived from 40 and 880 Hz.

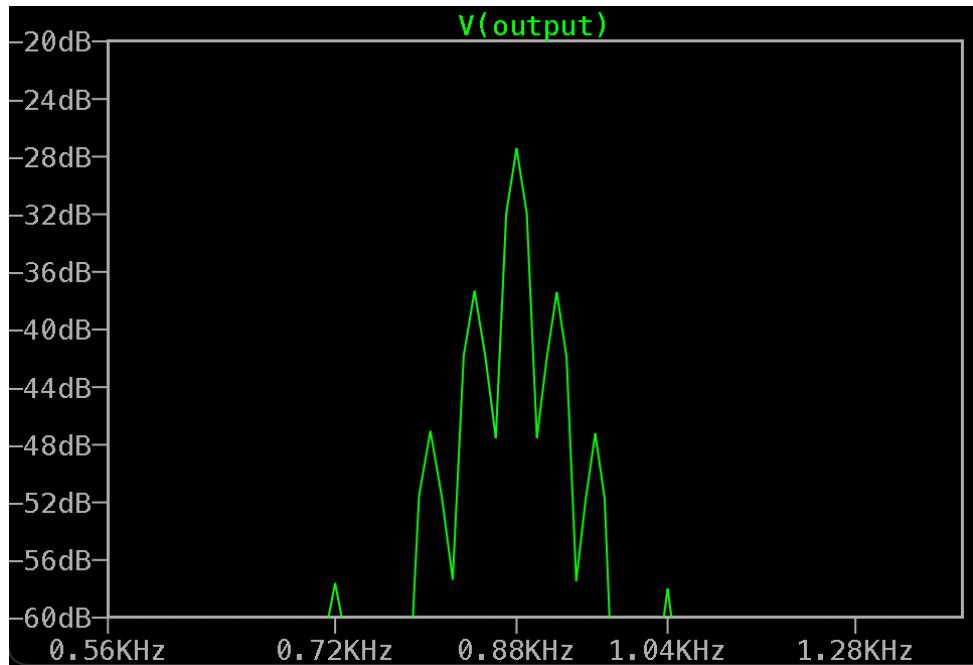


Figure 6: Mixer Output Signal FFT 880 Hz Zoomed In.

In order to determine our conversion loss, we take a close look at the 880 Hz signal and see how the 40 Hz signal creates distortion at 920 Hz and 840 Hz. The difference in dB at these points is considered the conversion loss. In our case, we have about 10dB loss.

Measurement results:

Setting up our simulation in the lab provided us with extremely similar results.

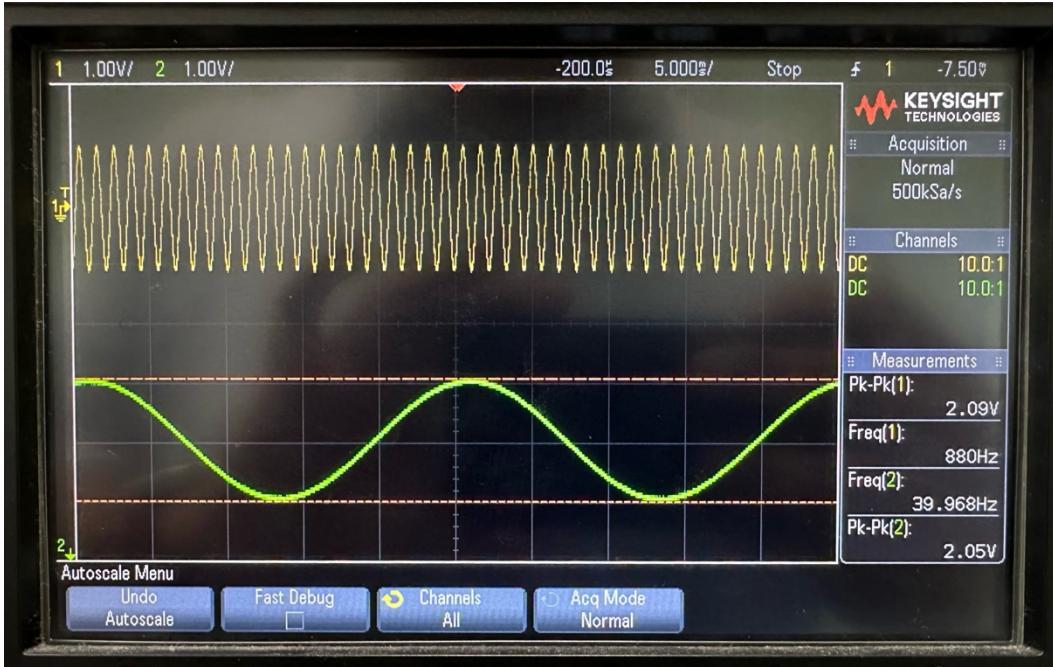


Figure 7: Actual Input Signals.

The same input signal used for our simulations.

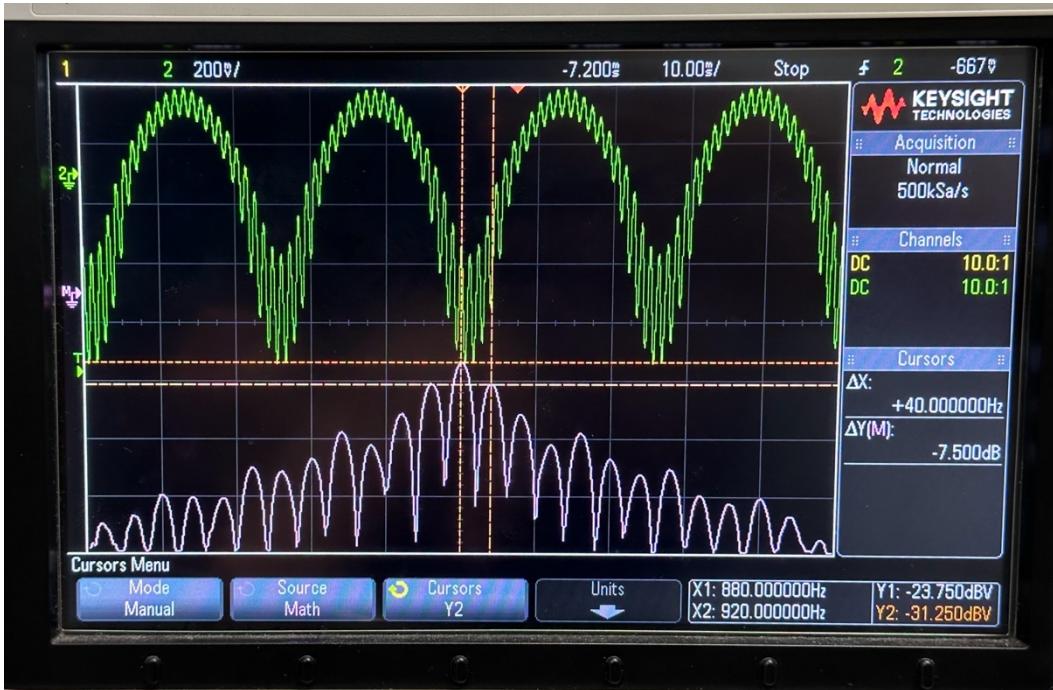


Figure 8: Output Signal and FFT

Here we can see our output signal and the frequency spectrum at the same time. We can measure that our next peak from 880 Hz is 40 Hz away with a conversion loss of 7.5dB.

Filter

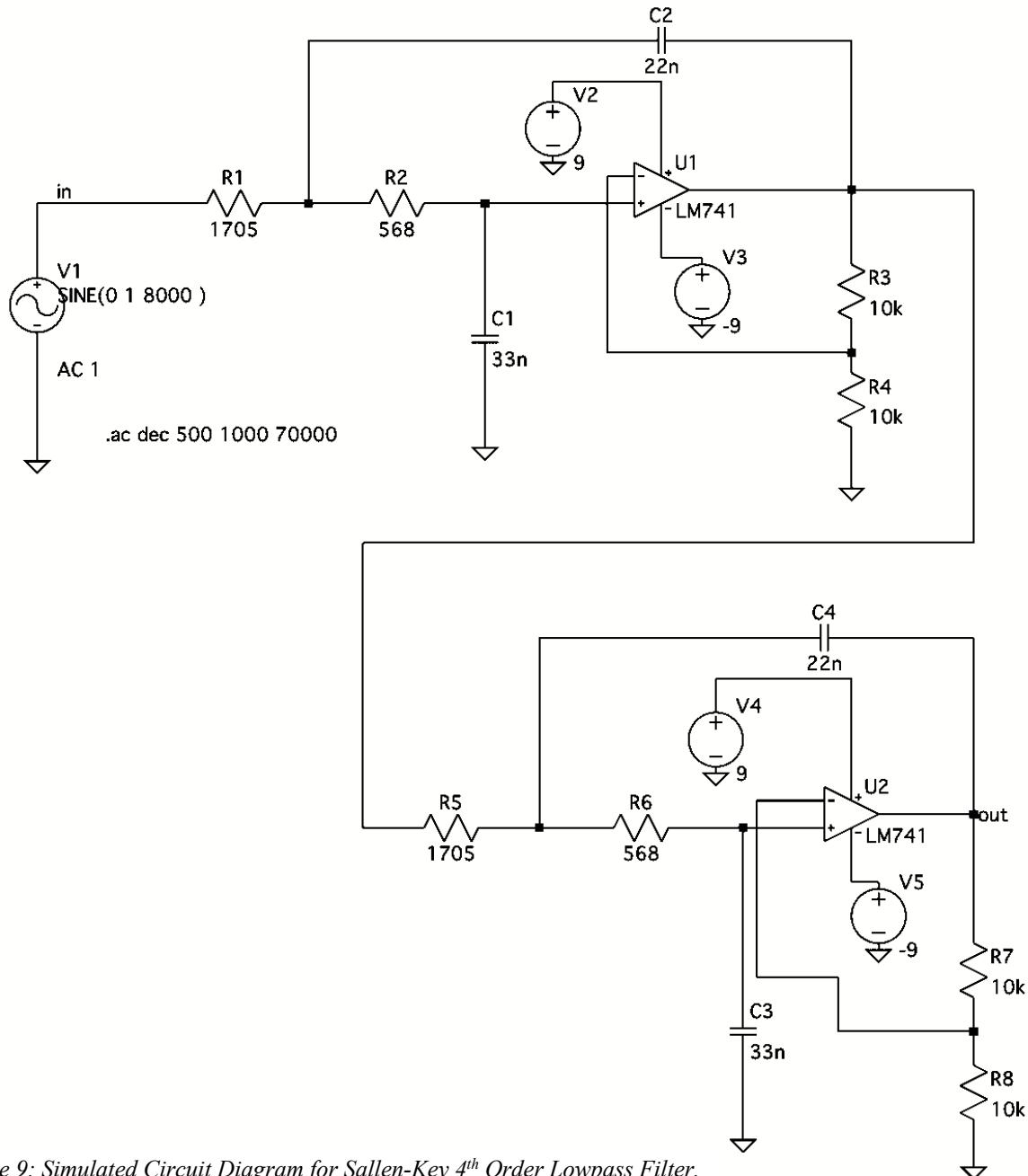


Figure 9: Simulated Circuit Diagram for Sallen-Key 4th Order Lowpass Filter.

Component	R1	R2	R3	R4	R5	R6	R7	R8
Simulated	1705 Ω	568 Ω	10K Ω	10 K Ω	1705 Ω	568 Ω	10K Ω	10K Ω
Measured	1778 Ω	552 Ω	9.95K Ω	9.95K Ω	1778 Ω	552 Ω	9.96K Ω	9.93K Ω

Table 2: Simulated Resistance Values vs. Measured Values

Component	C1	C2	C3	C4
Simulated	33nF	22nF	33nF	22nF
Measured	22.6nF	33.2nF	24.8nF	22nF

Table 3: Simulated Capacitance Values vs. Measured Values

Theoretical analysis:

An active low-pass filter was designed to meet the project requirements. It was intended to be a 4th-order filter, so the Sallen-Key topology was employed, also known as the voltage-controlled voltage source configuration.

The design of the Sallen-Key filter is straightforward. For a first-order filter, it consists of two poles, meaning one capacitor and resistor pair. To achieve a second-order filter, additional poles can be added by incorporating another pair of capacitors and resistors. Consequently, increasing the number of resistor and capacitor pairs enhances the roll-off.

Two resistors, R3 and R4, connected in the feedback network, as illustrated in the figure below, they determine the gain of the filter. By adjusting their values, the gain can be either increased or decreased.

Two second-order filters can be cascaded to obtain a 4th-order low-pass filter. The operational amplifier 741 is utilized to amplify the output voltage to a level higher than the input voltage making this an active filter.

Transfer Function Derivation

To make a fourth order filter low pass filter, we cascade two second order Sallen-Key low pass filter stages. The transfer function of each stage can be derived separately, and their product will give the output of the 4th order filter. The equation below in the figure 9 is the transfer function of low pass 2nd order filter. By taking the square of this equation we can also get the transfer function of 4th order filter.

$$\frac{v_o}{v_i} = \frac{\frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s\left(\frac{1}{C_1}\right)\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) + \frac{1}{R_2 R_3 C_1 C_2}}$$

Figure 9: Transfer Function of 2nd Order Sallen-Key Lowpass Filter

Component Selection.

Referring to the figure below, choosing an appropriate value for the resistor and R3 and C1 to find the values for R4, C2, R2 and R1 is important. Furthermore, the value for Q (quality factor) and fc (cut off frequency) are also decided at the start. Following formulas in the figure 10 allow us to get the values of every component in the circuit.

- Choose R_3, C_1
- $R_4 = R_3/(K - 1)$
- Define $\alpha = \omega_0 C_1, \beta = \frac{1}{4Q^2} + (K - 1)$
- $C_2 = \beta C_1$
- $R_1 = 2Q/\alpha$
- $R_2 = 1/(2Q\alpha\beta)$

Figure 10: Filter Design Equations

R3 value chosen 10k and C1 was chosen 22nf with a cut off frequency of 6 KHz. Qualtiy factor was selected as 0.707.

The Value of R4 was calculated and value of k was chosen to be 2 .

$$R4 = R3/(k-1)$$

$$R4 = 10k/1$$

$$R4 = 10k$$

Beta (B)is calculated:

$$B = [1/4 * (Q^2)] + K - 1$$

$$B = [1/4 * (0.707^2)] + 2 - 1$$

$$B = 1.5$$

$$C2 = B * C1$$

$$C2 = 1.5 * 22\text{nf}$$

$$C2 = 33\text{nf}$$

Alpha(A) is calculated

$$W_o = 2 * \pi * f_c$$

$$W_o = 2 * \pi * 6k$$

$$W_o = 37699 \text{ rad/sec}$$

$$\text{Alpha} = W_o * C1$$

$$\text{Alpha} = 37699 * 22\text{nf}$$

$$\text{Alpha} = 829\mu$$

$$R1 = 2 * Q / \text{Alpha}$$

$$R1 = 2 * 0.707 / 829\mu$$

$$R1 = 1705 \text{ ohms}$$

$$R2 = (1/2 * Q) * \text{Alpha} * B$$

$$R2 = (1/2 * 0.707) * 829\mu * 1.5$$

$$R2 = 568 \text{ ohms}$$

$$\text{Gain} = 20 * \log(20) * 2$$

$$\text{Gain} = 12 \text{ dB}$$

Simulation results:

In order to test our filter, we want to see how it performs across a sweep of frequencies. In the figure below, we measure our output as we increment the input frequency signal from 1k Hz to 40K Hz. This test can validate two of our design parameters. We need to have a DC gain of at least 6 dB and a cutoff frequency between 4K Hz and 8K Hz. Below you can see how the filter output is above 6 dB on the top left. Focusing on the green dotted line, we can see how our phase changes as our input frequency increases. The cut off frequency for a low pass filter is said to be when the phase reaches 180 degrees. Looking under the graph, the measurement at -180 degrees is reached when the input frequency is 5.84K Hz. This somewhat verifies our design since we had accounted for a 6 KHz cut off frequency.

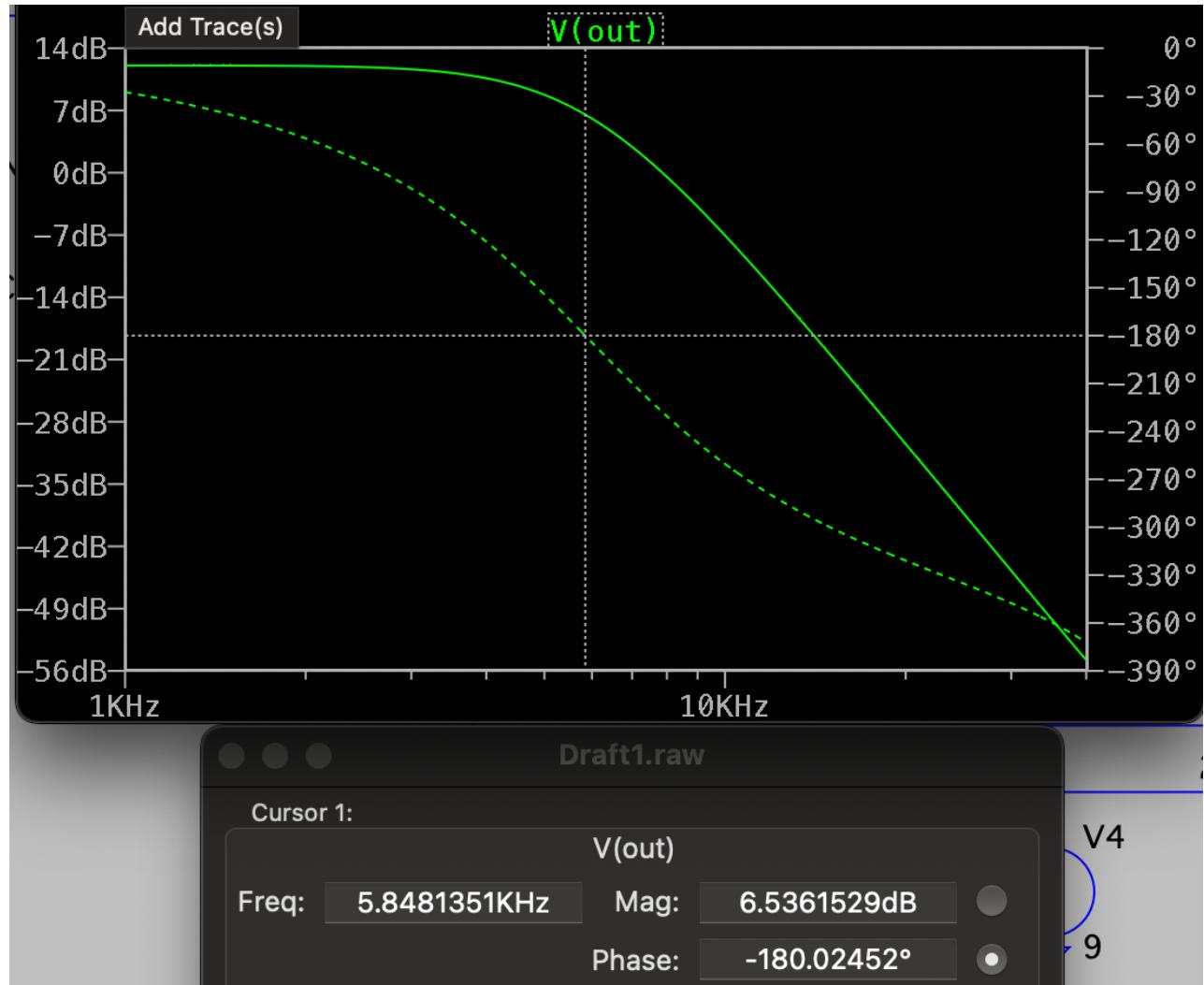


Figure 11: Simulation Lowpass Filter LTspice

Measurement results:

In order to test our filter in the lab, we need to sweep the input frequency. Unfortunately, we did not know how to do that on the oscilloscope wave generator, so we decided to take some points and measure our output voltage.

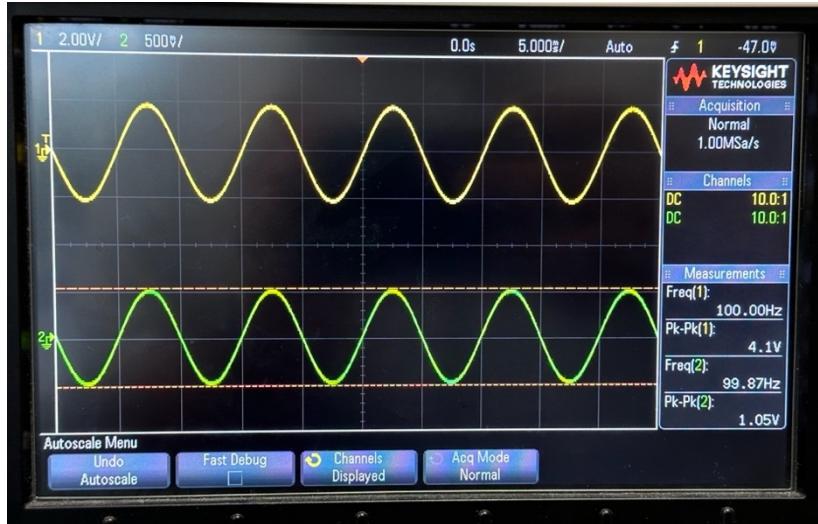


Figure 12: Filter Test at 100 Hz and Pk - Pk Values.

The yellow sine wave in Figure 12 shows the output of the low-pass filter, while the green wave represents the input waveform from the wave generator. It's clear that when a 100 Hz input with a Vpp of 1 volt is supplied to the filter, the output is amplified to 4.7 volts, and the signal passes through.



Figure 13: Filter Test at 7 KHz and Pk - Pk Values

When the frequency is increased to 7 kHz, it surpasses the cutoff frequency, and the Vpp starts to decline. This indicates that the signal begins to attenuate, as this low-pass filter was designed with a cutoff frequency of 6 kHz.

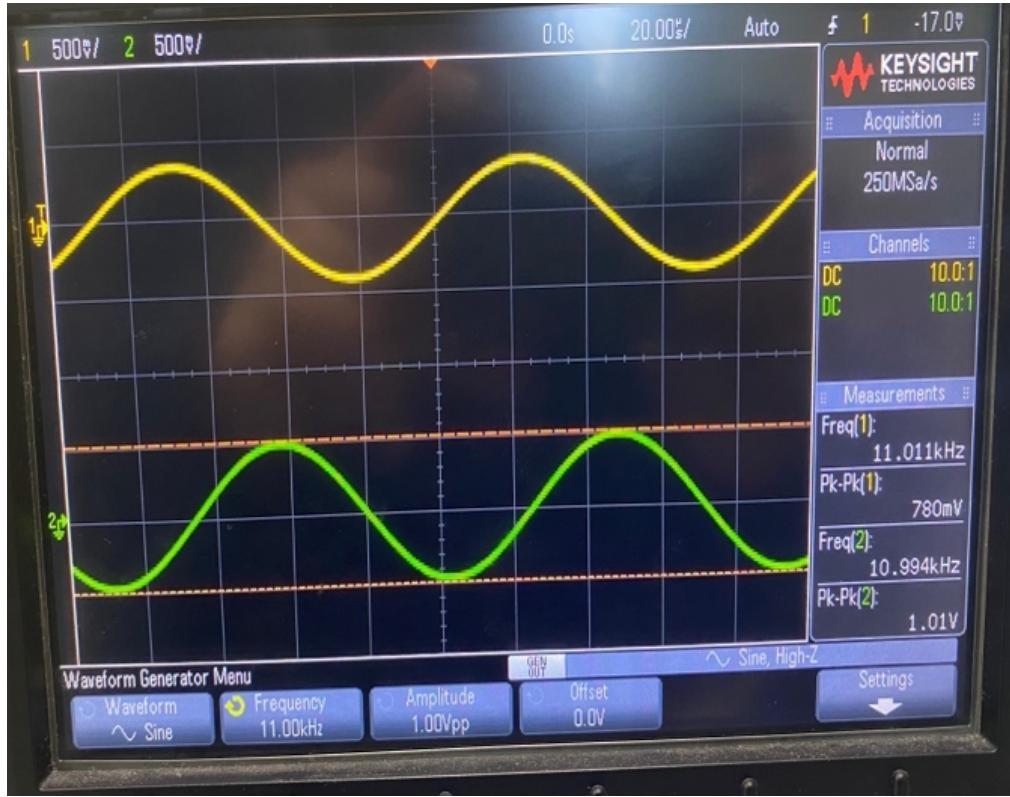


Figure 14: Filter Test at 11 KHz and Pk - Pk Values

As the frequency increases beyond the cutoff frequency of the low-pass filter, the attenuation becomes more pronounced. At 11 kHz, the signal's peak-to-peak voltage dropping to 780 mV suggests significant filtering action, where higher frequency components are being effectively suppressed. Observing this attenuation highlights the filter's effectiveness in shaping the frequency response according to its design parameters.

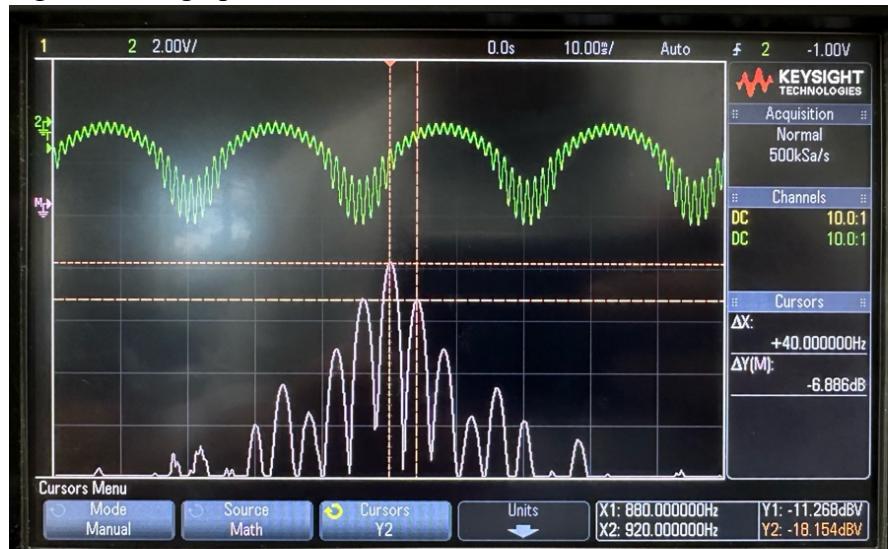


Figure 15: Filter Output with 880Hz and 40Hz Mixer Input.

Finally, we showcase out signals intended output during this stage. Since the FFT is centered around 880Hz we do not expect any loss of signal.

Amplifier

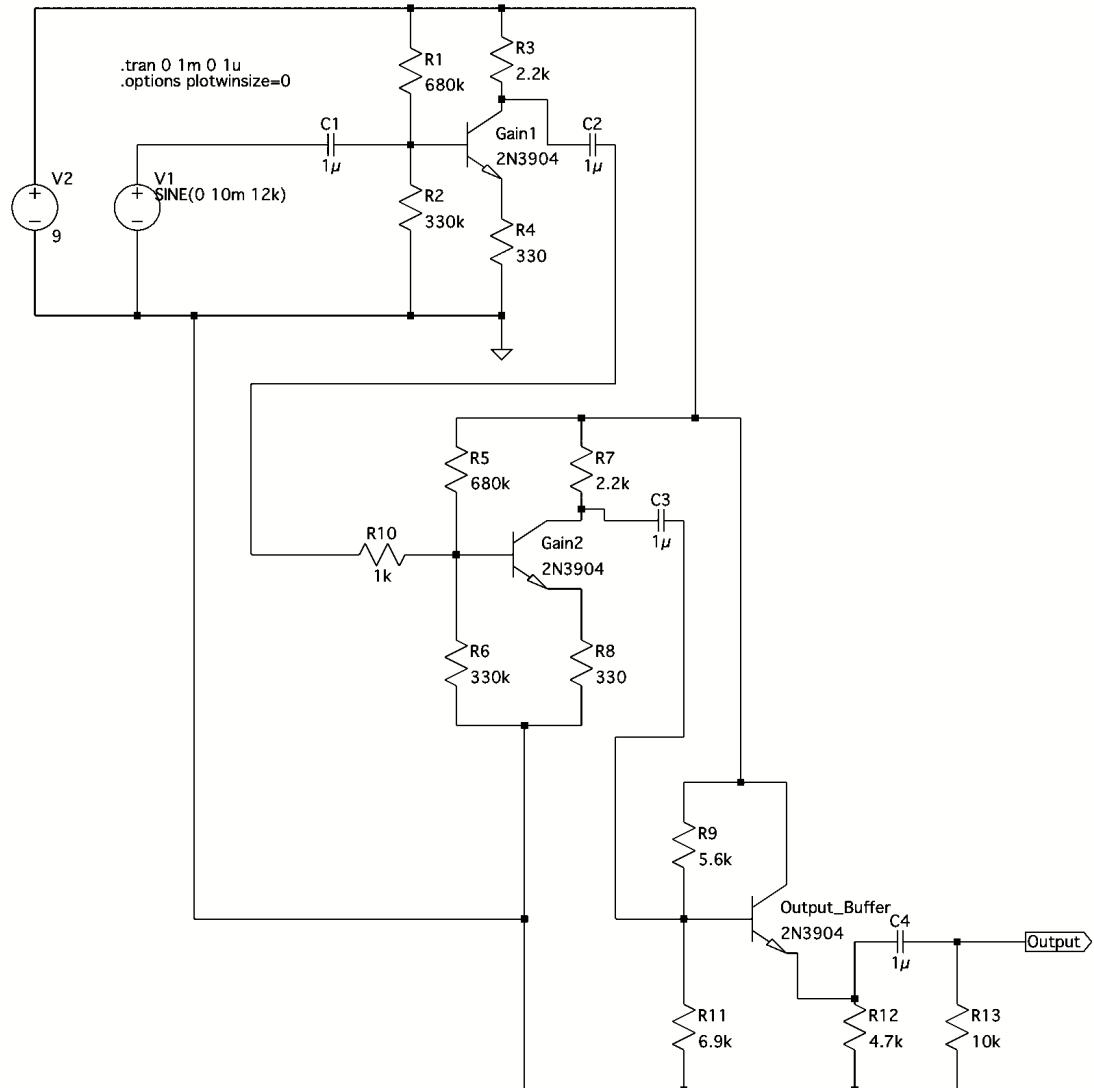


Figure 16: Simulated Amplifier Circuit Design on LTspice.

Component	R1	R2	R3	R4	R5	R6	R7
Simulated	680KΩ	330KΩ	2.2KΩ	330Ω	680KΩ	330KΩ	2.2KΩ
Measured	229KΩ	226KΩ	2.17KΩ	321Ω	226KΩ	222KΩ	2.17KΩ

Table 4: Simulated Vs. Measured Resistance Values

Component	R8	R9	R10	R11	R12
Simulated	330Ω	5.6KΩ	1KΩ	6.9KΩ	4.7KΩ
Measured	323Ω	4.91KΩ	997Ω	5.98KΩ	4.62KΩ

Table 5: Simulated Vs. Measured Resistance Values

Component	C1	C2	C3	C4
Simulated	1uF	1uF	1uF	1uF
Measured	1.056uF	1.076uF	1.097uF	1.073uF

Table 6: Simulated Vs. Measured Capacitance Values

Theoretical analysis:

The purpose for an amplifier is to increase the power of a signal without adding distortion. When it comes to this project we need to take into account a couple of considerations. Our audio amplifier must:

- Utilize a gain and buffer stage.
- Amplify input voltage signals with amplitudes between 10 and 100 millivolts.
- Amplify input signals between 120 Hz and 12K Hz.
- Produce a voltage gain of about 26 dB.
- Have a minimum input resistance of at least 100 KΩ.
- Have a maximum output resistance of 100 Ω.
- Consume less than 15 mA.

BJT Dual Gain Stage

This part of the amplifier provides gain to the circuit. Both gain cells are identical providing slightly more than 26 dB gain. Each gain cell is designed to provide half of the gain. Ideally, we are looking for a voltage gain of negative 6.66 for each cell.

For Gain 1 we can see our gain as:

$$Gain = \frac{R3}{r_e + R4}$$

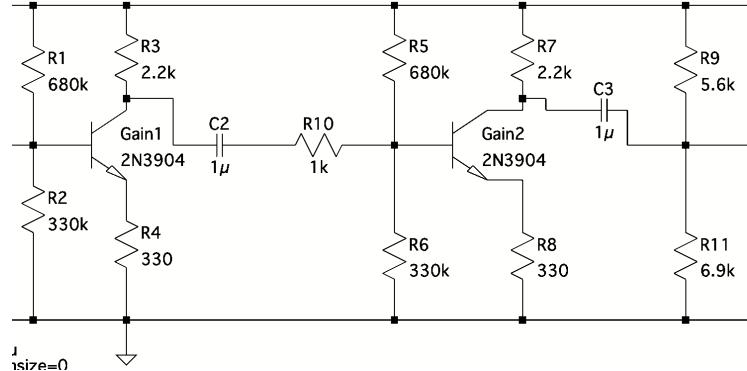


Figure 17: Dual BJT Gain Stages

But our gain can be affected by the biasing resistors in the next cell. Assuming r_e is in the order of a couple ohms it is not that necessary to calculate it, so I use an arbitrary value such as 10. Without considering the resistors in the biasing network in the following stage our gain closely follows the equation above.

$$\text{Stage 1: } Gain = \frac{2200}{330+10} = -6.47 \quad Gain = \frac{R3 || R5 || R6}{330+10} = -6.4$$

$$\text{Stage 2: } Gain = \frac{2200}{330+10} = -6.47 \quad Gain = \frac{R7 || R9 || R11}{330+10} = -3.78$$

$$\begin{array}{lll} \text{Total Gain} & -6.47 * -6.47 = 41.86 & -6.4 * -3.78 = 24.192 \\ \text{Stage 1 X Stage 2} & & \end{array}$$

26dB is equivalent to gain of 20V/V.

This means that our realized gain is substantially smaller than we thought, but this is a tradeoff necessary in order to establish the following buffer stage which uses smaller biasing resistors. Even so, we were barely able to meet this requirement since the buffer stage takes up a little of the gain.

This method that we used allowed us to determine the collector and emitter resistors.

Biasing Network

When it came to determining what resistors to use in our biasing network, we took a guess and check approach. Initially we did the analysis and found that it worked for the 120 Hz case with 10 mV but did not for the 100mV case. After struggling some time with it, we decided to use LTspice to help us find a resistor combination that could satisfy all the requirements.

Q-Point

The q point is determined during DC analysis. It is what helps us track how much swing we can have in our transistor amplification. In this case, we decided to set the beta to 150.

First, we determine the base voltage:

$$V_{BB} = V_{CC} \frac{R2}{R1 + R2}$$

$$V_{BB} = 9 \frac{330K\Omega}{330K\Omega + 680K\Omega} = 2.94V$$

Now we determine the parallel bias resistance:

$$R_B = R1 \parallel R2$$

$$R_B = 330K\Omega \parallel 680K\Omega = 222178\Omega$$

Now we can determine the current q point:

$$I_{EQ} = \frac{V_{BB} - V_{BE}}{\frac{R_B}{\beta + 1} + R_E}$$

$$I_{EQ} = \frac{2.94 - 0.7}{\frac{222178}{151} + 330} = 1.243mA$$

Finally, we can find the voltage q point:

$$V_{CEQ} = V_{CC} - I_{EQ}(R_C + R_E)$$

$$V_{CEQ} = 9 - 1.243mA(2200 + 330) = 5.85V$$

The q point voltage ranges from 0 to 9 volts. If we were to run into an issue, it would be on the upper bounds where 5.85V is close to 9V. I would assume this means our max positive voltage swing is 3.15V.

The q point current ranges from 0 to 4.09mA (V_{CC} / R_L).

Input Impedance

The input impedance is the resistance seen at the base terminal of the transistor.

$$Z_{IN} = R_B \parallel (\beta + 1)(R_E + r_e)$$

$$Z_{IN} = 222178 \parallel (150 + 1)(330 + 10)$$

$$Input\ Impedance = 41703\Omega$$

In order to meet this requirement, we need to increase our R_E to at least 1350Ω .

BJT Output Buffer

The purpose of the output buffer is to isolate the gain stage from the output stage. If this isolation does not exist, the impedance from the output stage will affect the gain of the amplifier. One of our design parameters is to have an output impedance of less than $100\ \Omega$.

In order to determine the output resistance of the buffer, we need to determine the beta value of the transistor. The 2N3904 transistor datasheet says it has a beta value between 70 and 300 at 1mA collector current. In our case the collector current is about the same as the emitter current.

The base current can be found using the input voltage and the biasing resistors R9 and R11.

$$I_B = \frac{9V}{5.6k + 6.9k} = 0.72mA$$

The emitter current is the current that travels through R12 while the emitter voltage is active. Using KVL, the emitter voltage is:

$$V_E = V_B - V_{BE}$$

In order to find the base voltage, we multiply R11 by the base current and assume the base emitter voltage to be 0.7.

$$V_B = I_B * R11 = 720\mu A * 6.9K\Omega = 4.968V$$

$$V_E = 4.968V - 0.7V = 4.268V$$

Now we can determine the emitter current.

$$I_E = \frac{V_E}{R_E} = \frac{4.268V}{4.7K\Omega} = 0.908\ mA$$

Since we can assume the beta value is between 70 and 300. I will take the midpoint of 185.

$$\beta = 185$$

Now that we have found the emitter current, we can also find the emitter's internal resistance.

$$r_e = \frac{25mV}{I_E} = \frac{25mV}{0.908mA} = 27.53\Omega$$

Finally in order to determine the output impedance we can use the following equation.

$$\begin{aligned} \text{Output Resistance} &= R_E \parallel (r_e + \frac{R9 \parallel R11}{\beta+1}) \\ &4.7K\Omega \parallel \left(27.53 + \frac{5.6K\Omega \parallel 6.9K\Omega}{185+1} \right) = 43.74\Omega \end{aligned}$$

Now this circuit can handle any output resistance load. We can simulate a $10K\Omega$ load to see how the output resistance is affected.

$$Z_{out} = R_{LOAD} \parallel R_{Output}$$

$$10K\Omega \parallel 43.74\Omega = 43.55\Omega$$

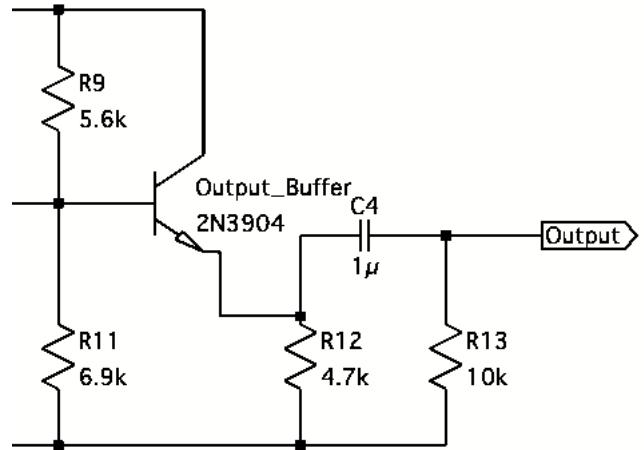


Figure 18: Amplifier Buffer Stage

Simulation results:

Using LTspice we are able to show how we meet the following design criteria.

- Amplify input voltage signals with amplitudes between 10 and 100 millivolts.
- Amplify input signals between 120 Hz and 12K Hz.
- Produce a voltage gain of about 26 dB.
- Consume less than 15 mA.

120 Hz test:

10 mV peak

Here we can see the max current draw is 6.02mA and the gain is slightly over 26 dB.

100 mV peak

Here we can see the max current draw is 6.6mA and the gain is slightly over 26 dB.

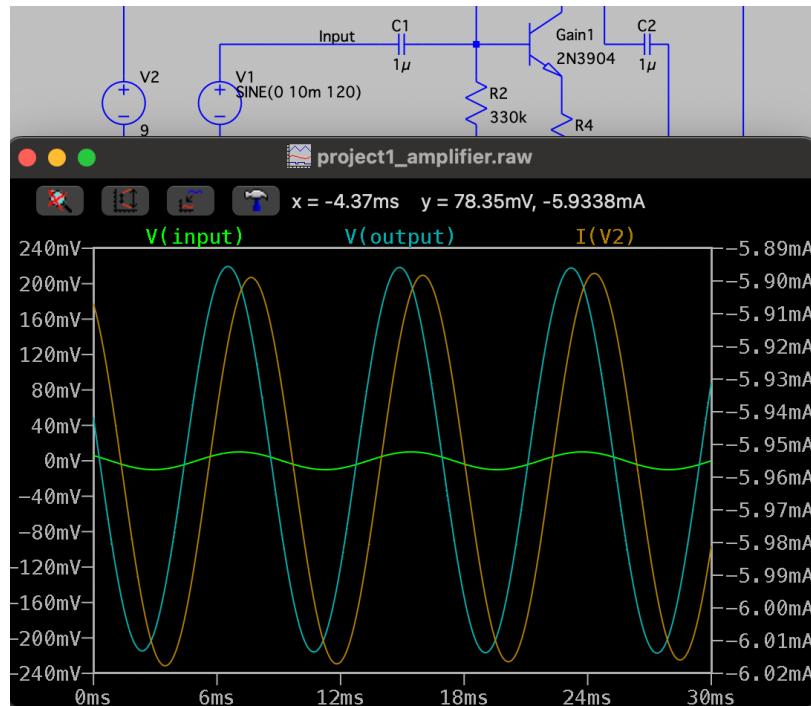


Figure 19: 120 Hz simulation test at 10mV.

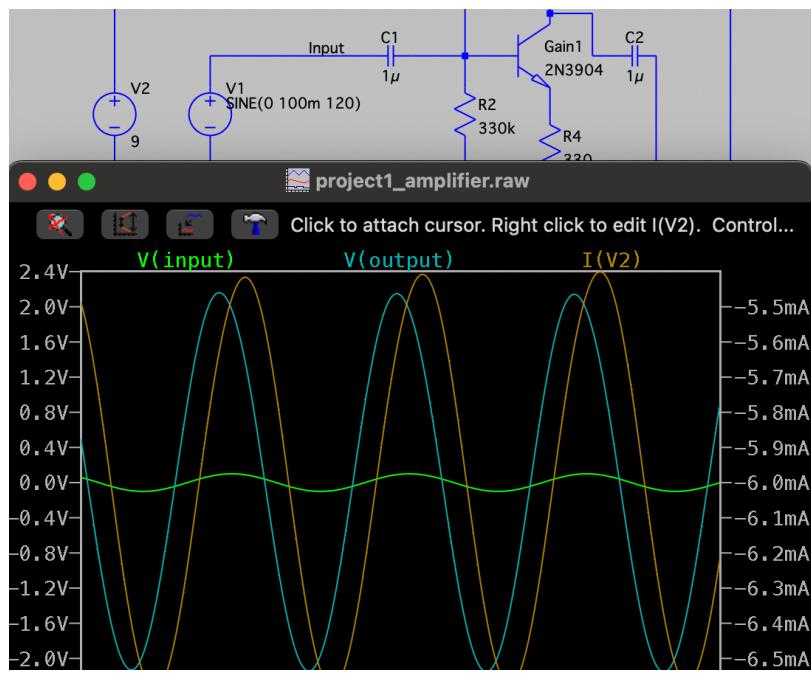


Figure 20: 120 Hz simulation test at 100mV.

12 KHz test:

10 mV peak

Here, the max current draw is 6mA and the gain is slightly over 26 dB.

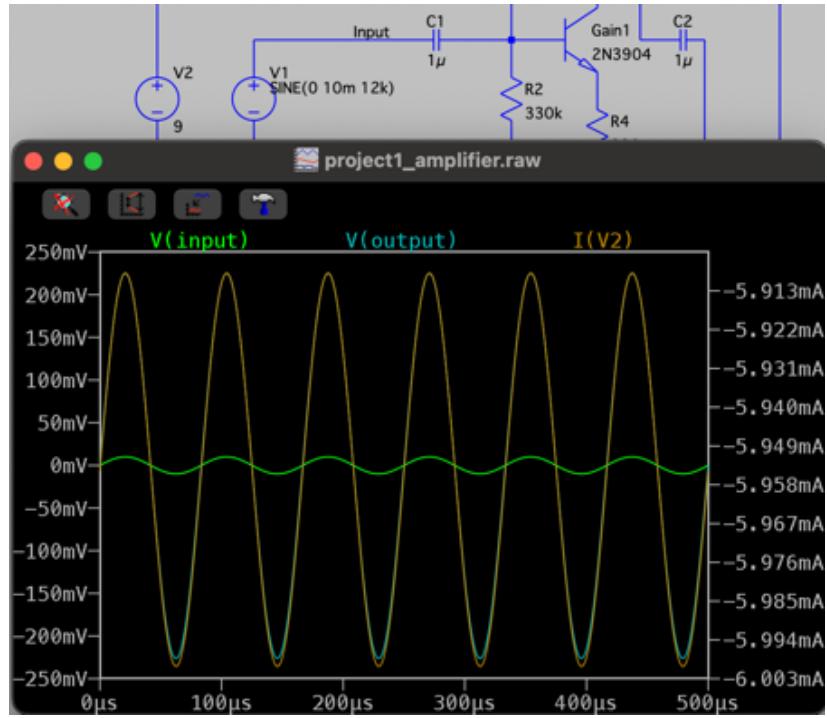


Figure 21: 12 KHz simulation test at 10mV.

100 mV peak

The max current draw is 6.48mA and the gain is slightly over 26 dB.

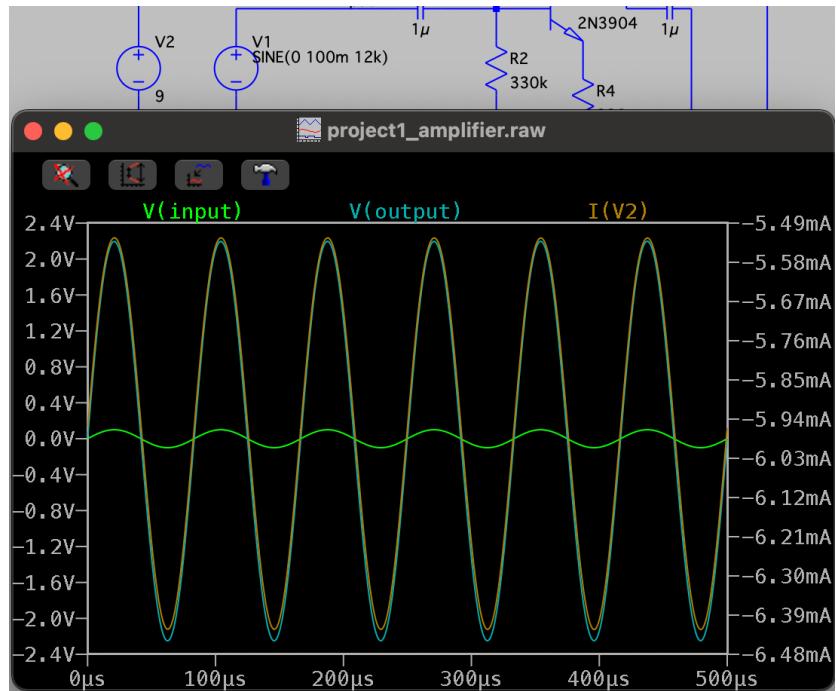


Figure 22: 12 KHz simulation test at 100mV.

Overall, our current draw hoovered around 6.5mA and the gain was sustained at 26 dB.

Measurement results:

We perform similar test as the ones done on LTspice. Since the wave generator did not produce 10 mV peak sine wave, we only tested the 100-mV signal and its current draw.

This test is the 100mV signal with 120 Hz. We can see how signal goes over 2V.

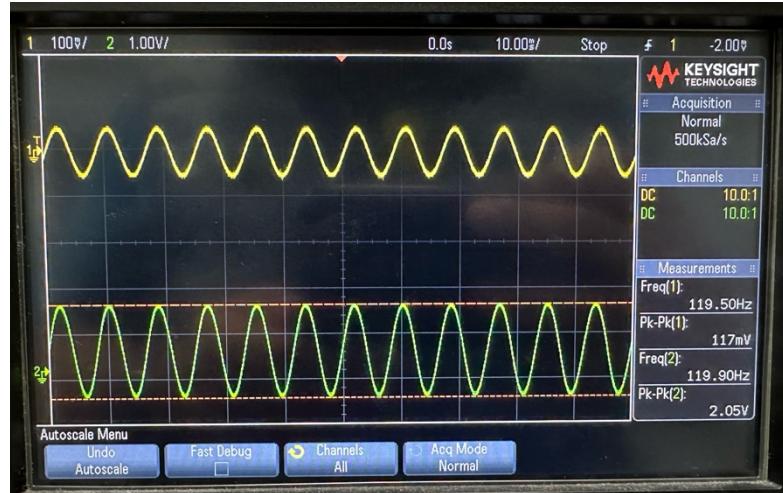


Figure 23: Oscilloscope 120 Hz test at 100 mV

This test is the 100mV signal with 12 KHz. The results are similar, and the gain is close to 26 dB.

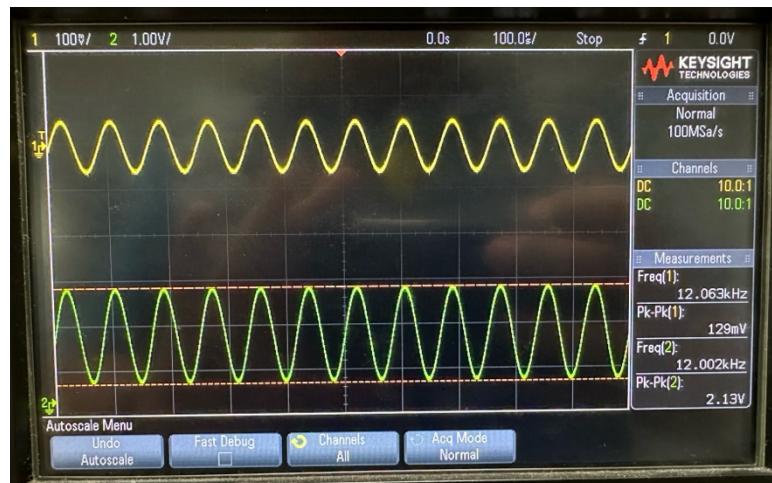


Figure 24: Oscilloscope 12 kHz test at 100 mV

The DC power supply lets us know how much current our circuit is drawing. In this case, it is drawing 5mA.



Figure 25: Power Supply Reading while Circuit under test.

Complete Implementation

In the demonstration, two waveform generators were utilized to supply signals to the mixer. In the first setup, the mixer received an output of an 880Hz sine wave with a voltage peak-to-peak (Vpp) of 0.5V and a 40Hz sine wave with a Vpp of 0.8V. Both of these input signals were combined by the mixer at its output, which was then fed into a Low Pass 4th order filter with a cutoff frequency of 6kHz. After the signal was filtered, it was amplified by the amplifier at the end, and the output was analyzed by the oscilloscope at the mixer, filter, and amplifier stages. Furthermore, the Fast Fourier Transform (FFT) was observed.

This process was repeated for sets 2 and 3, but the values of the input waveforms were changed. In set 2, the input waves consisted of a 1.32kHz sine wave with a Vpp of 0.3V and a 20Hz triangular wave with a Vpp of 1.0V. In the last set, a 4.5kHz sine wave with a Vpp of 0.2V and a 10Hz square wave with a Vpp of 1.2V were generated.

Set 1 880Hz sine wave with a voltage peak-to-peak (Vpp) of 0.5V and a 40Hz sine wave with a Vpp of 0.8V

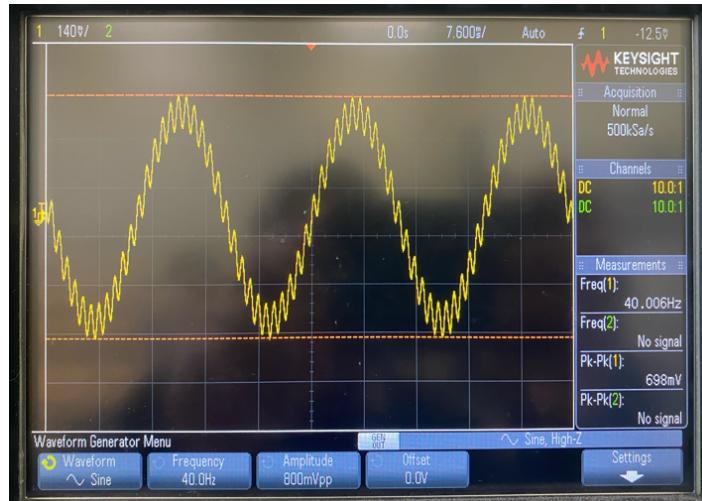


Figure 26: Super Imposed Input Signal at Mixer Input.



Figure 27: Mixer Signal Output.



Set 2 Input waves consist of a 1.32kHz sine wave with a Vpp of 0.3V and a 20Hz triangular wave with a Vpp of 1.0V.

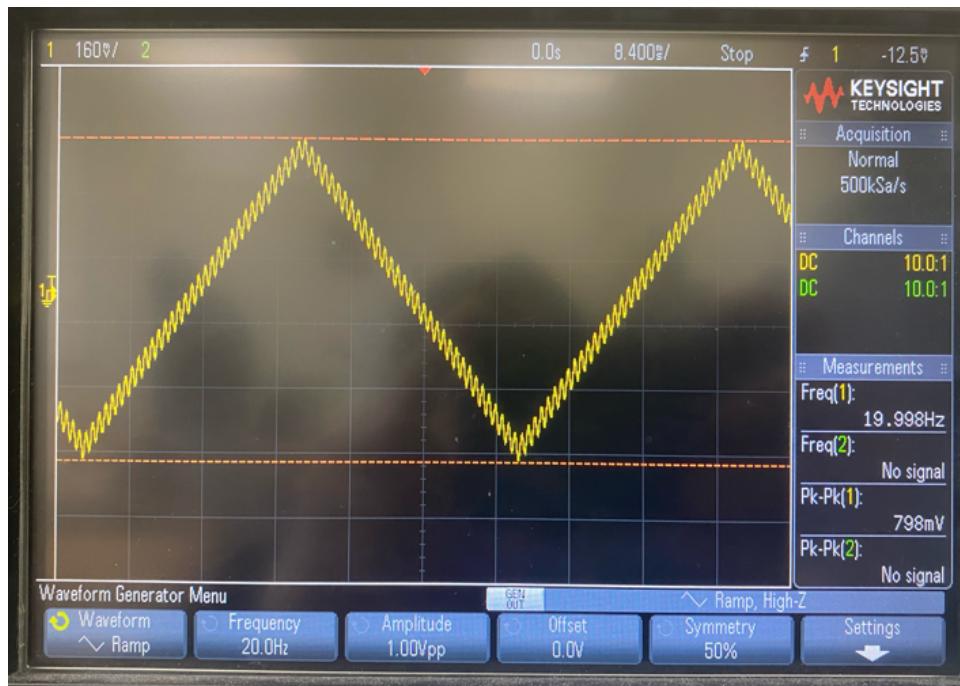


Figure 30: Set 2 Input Signal.



Figure 31: Set 2 Mixer Output Signal.

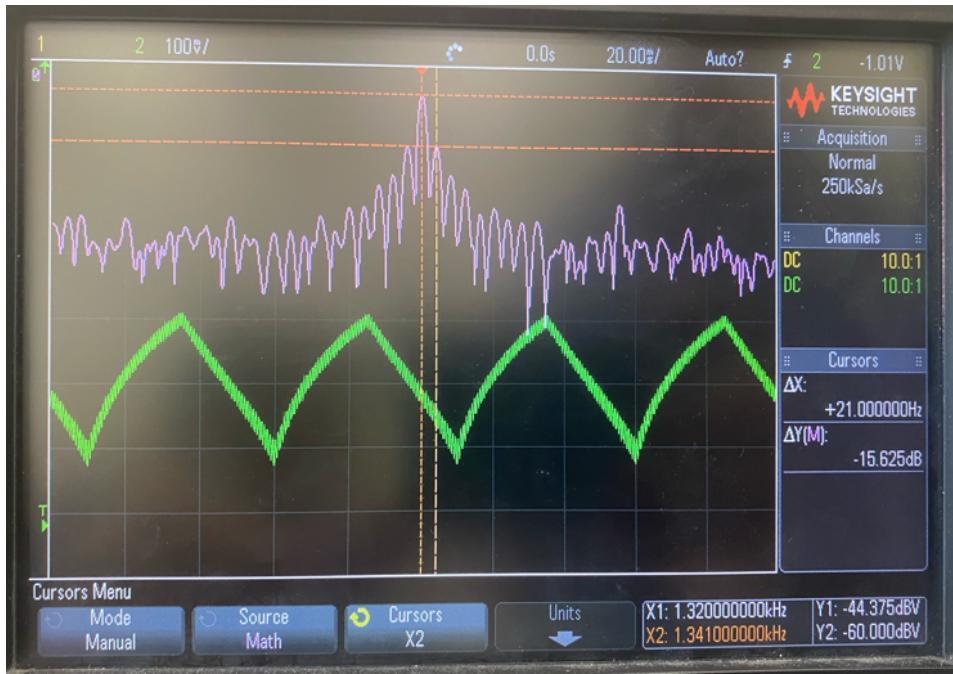


Figure 32: Set 2 Filter Output Signal.



Figure 33: Set 2 Amplifier Output Signal.

Set 3 A 4.5kHz sine wave with a Vpp of 0.2V and a 10 Hz square wave with a Vpp of 1.2V were used as inputs.



Figure 34: Set 3 Input Signal.



Figure 35: Set 3 Mixer Output Signal.



Figure 36: Set 3 Filter Output.



Figure 37: Set 3 Amplifier Output.

Discussion

Every block of the circuit was designed to meet the specific requirements of the project. For the mixer, the task was to combine two signals effectively. Through careful adjustments of component values in LTspice, we successfully achieved this objective, ensuring the seamless integration of multiple input signals.

In the case of the filter, our goal was to achieve a gain greater than 6dB while providing flexibility in selecting the cutoff frequency. We were afforded the freedom to choose the cutoff frequency within the range of 4 KHz to 8 KHz, and after careful consideration, we opted for the mid-value of 6 KHz. Additionally, to ensure optimal performance, we selected a quality factor of 0.707.

To simplify the design and implementation process of the low-pass 4th order filter, we employed the Sallen-Key topology. This topology offers sharp roll-off and accurate frequency control.

Similarly, the choice of a dual-gain stage amplifier with an output buffer was made to ensure sufficient signal strength while minimizing output impedance. We were not able to meet the input impedance criteria, but it is something that can be easily fixed. Another thing to note, would be if we could slightly increase the gain on the amplifier to overcome the losses from the buffer.

In terms of implementation trade-offs, we carefully balanced the need for signal fidelity with complexity. For example, the decision to use the Sallen-Key topology for the low-pass filter was driven by its ability to achieve sharp roll-off and accurate frequency control, despite the added complexity compared to simpler filter designs. Similarly, the choice of a dual-gain stage amplifier with an output buffer was made to ensure sufficient signal strength while minimizing output impedance.

Overall, our design and experimentation process involved a careful balance of trade-offs to achieve a part of synthesizer circuit capable of meeting the specified signal processing requirements while remaining adaptable for future enhancements and applications.

Conclusion

Through the design and implementation of three blocks synthesizer circuit comprising a mixer, low-pass filter, and amplifier stage we have gained valuable knowledge related complexities of signal processing and circuit design. Our experience has reinforced the importance of balancing design choices, considering trade-offs, and conducting thorough experimentation on both breadboard and simulation software like LTspice.

We have learned that each component of the circuit plays a critical role in achieving the desired signal processing objectives, and careful consideration must be given when changing the values for components in the circuit like resistors and capacitors. For instance, a slight change in the value of the of any component could give unexpected results at the output.

Overall, this experience has deepened our understanding of circuit design principles and provided a solid foundation for further exploration and development in the field of circuit designing.