南方科技大学
SOUTHERN UNIVERSITY OF SCIENCE AND TECHNOLOGY

# Embedded System and Microcomputer Principle

## LAB11 Pulse Width Modulation

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南方科技大学
SOUTHERN UNIVERSITY OF SCIENCE AND TECHNOLOGY

# CONTENTS

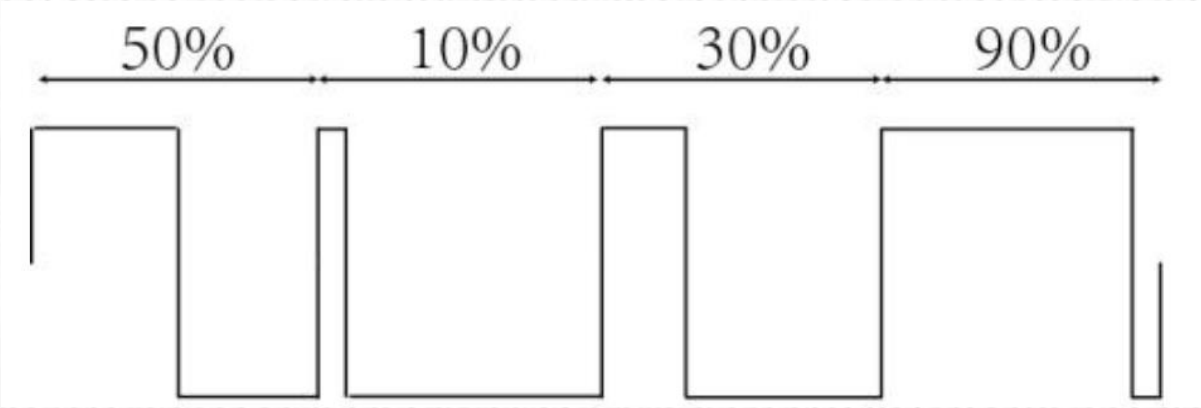
01

# PWM Mode Description

# 1. PWM Mode Description

## -- What is PWM

- Pulse width modulation
- By changing the period of the pulse, the frequency can be adjusted, and the voltage can be adjusted by changing the pulse width or duty cycle.
- The voltage and frequency can be changed harmoniously by adopting appropriate control methods

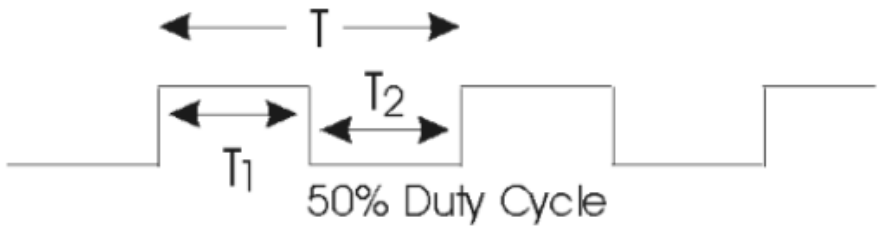



PWM waveform

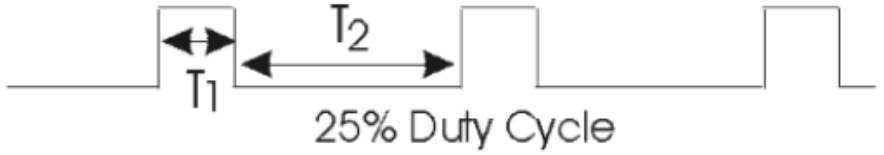
# 1. PWM Mode Description
## -- What is Duty Cycle

T = *period* of waveform (constant)
T1 = duration of pulse (T2 = T – T1)
*Duty Cycle* = T1/T = T1/(T1+T2)

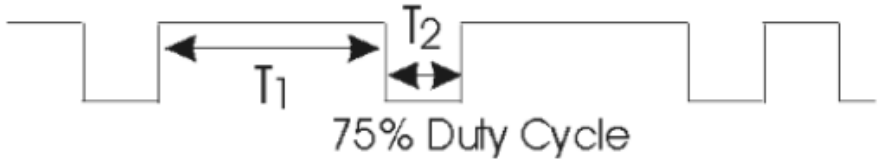
$$V_{avg} = V_{max} \times Duty\ Cycle$$




$V_{avg} = 0.5V_{max}$




$V_{avg} = 0.25V_{max}$

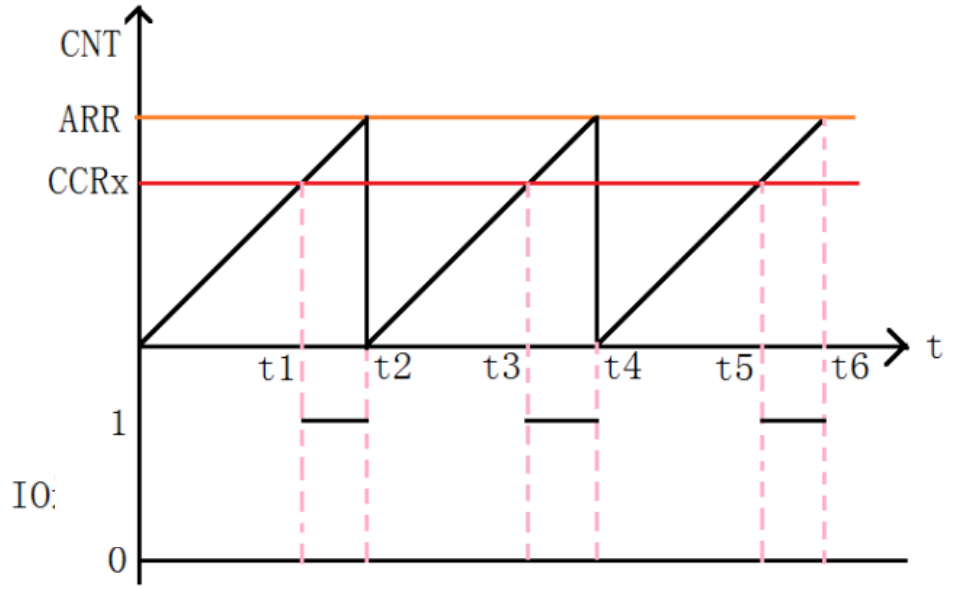



$V_{avg} = 0.75V_{max}$

# 1. PWM Mode Description

## -- PWM working principle

- **Timer** will be used.
- Assume the timer is in up-counting mode, when CNT<CCRx, output is “0”, and when CNT>=CCRx, output is “1”
- When CNT register counts from 0 to the content of the ARR register, then restarts from 0
- By changing the value of **CCRx** can change the **duty cycle** of PWM output
- By changing the value of **ARR** can change the **frequency** of PWM output

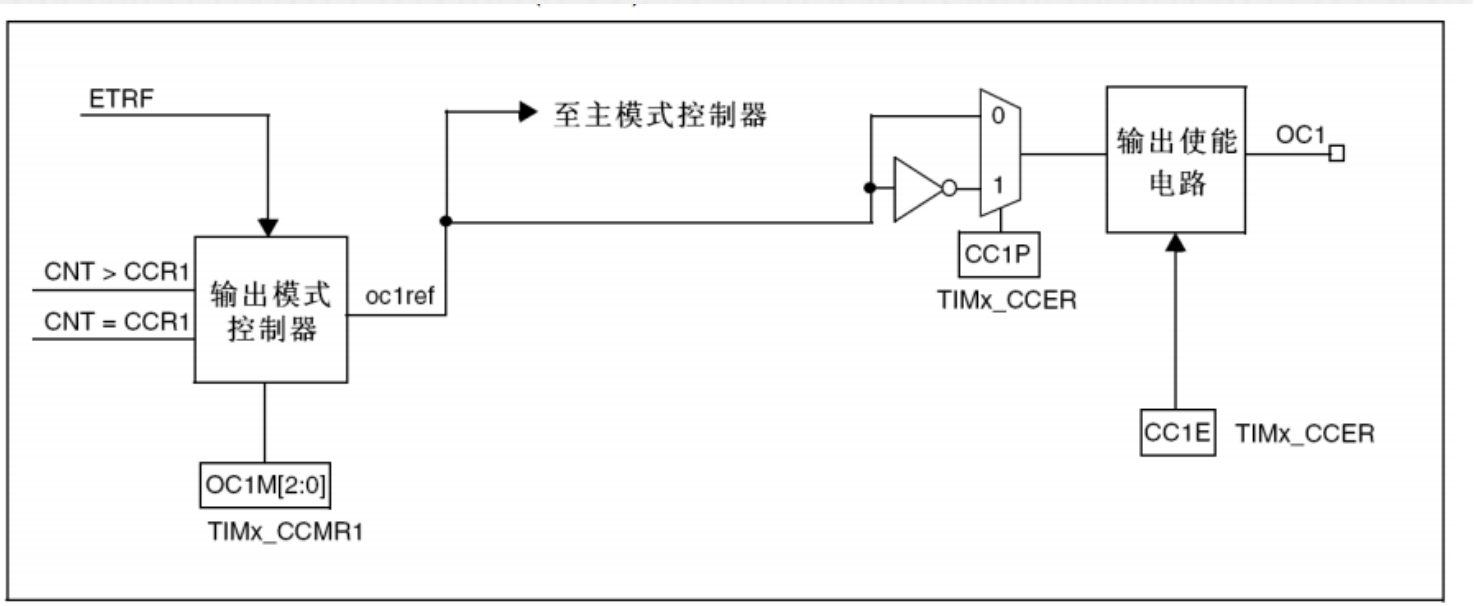



Schematic diagram of PWM

# 1. PWM Mode Description

## -- PWM working process

- Two stages
  - Compare value
  - Control output
- Involving registers
  - TIMx_ARR
  - TIMx_PSC
  - TIMx_CNT
  - TIMx_CCRx
  - TIMx_CCMRx
  - TIMx_CCER
  - TIMx_BDTR(only TIM1 and TIM8 need this register)

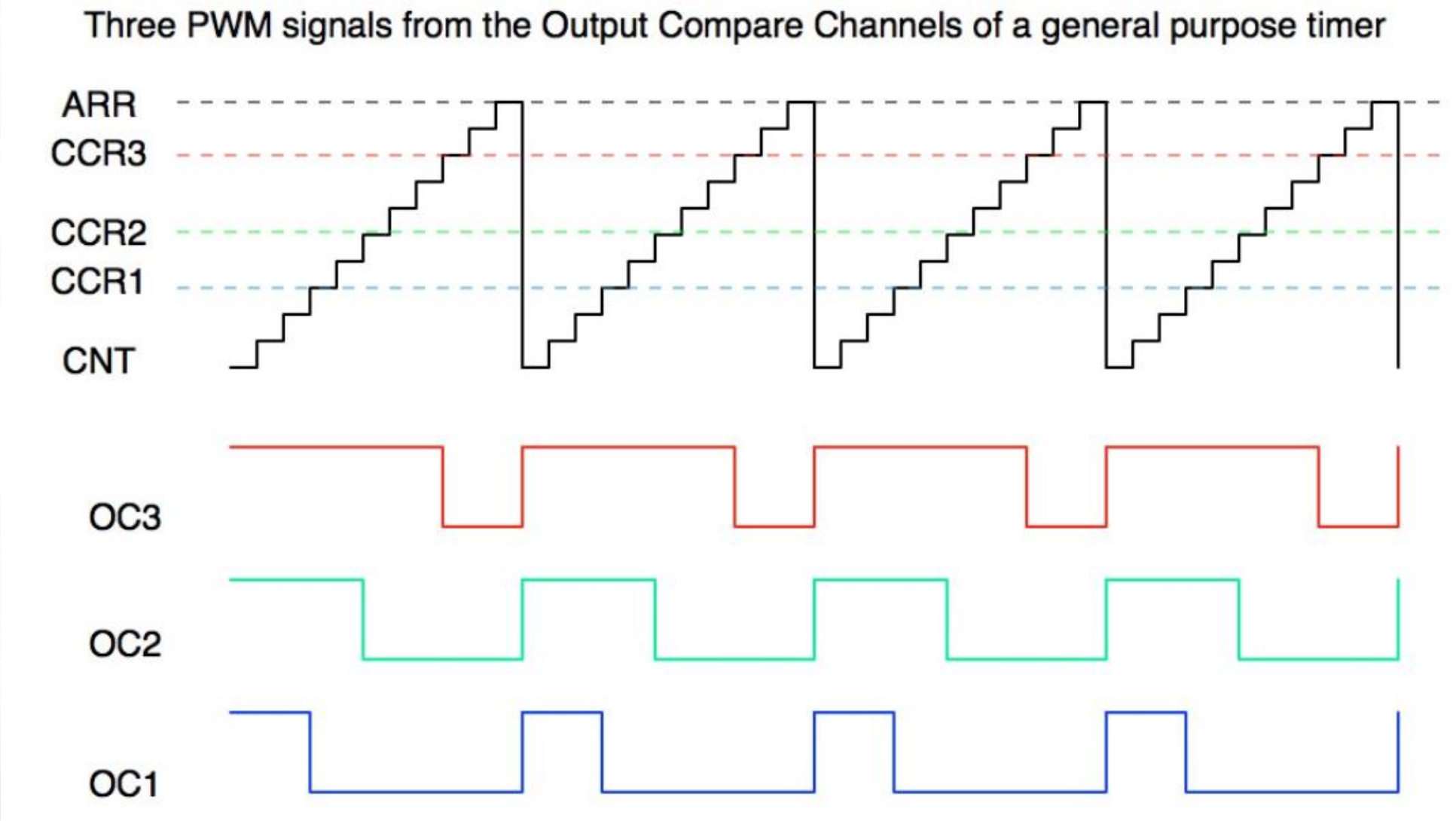



PWM working process
(take channel 1 as an example)

# 1. PWM Mode Description
## -- PWM working process(continued)

| Register | Bit | Description | Example |
|---|---|---|---|
| TIM1_CR1 | DIR | 0: up-counting mode<br>1: down-counting mode | **(1)** DIR = 0 -> OC1M = 110 -> TIM1_CNT < TIM1_CCR1 -> CH1 is active (OC1REF=1) -> CCIP = 0 -> OC1 output high;<br>**(2)** DIR = 1 -> OC1M = 110 -> TIM1_CNT > TIM1_CCR1 -> CH1 is inactive (OC1REF=0) -> CCIP = 1 -> OC1 output high;<br>**(3)** DIR = 0 -> OC1M = 111 -> TIM1_CNT < TIM1_CCR1 -> CH1 is inactive (OC1REF=0) -> CCIP = 0 -> OC1 output low;<br>**(4)** DIR = 1 -> OC1M = 111 -> TIM1_CNT > TIM1_CCR1 -> CH1 is active (OC1REF=1) -> CCIP = 1 -> OC1 output low; |
| TIM1_CCMR1 | OC1M | 110: PWM mode 1<br>111: PWM mode 2 | |
| TIM1_CCER | CCIP | 0: OC1 active high<br>1: OC1 active low | |
| TIM1_CCER | CC1E | 0: Off - OC1 is not active<br>1: On - OC1 signal is output on the corresponding output pin | |

# 1. PWM Mode Description
## -- PWM waveform examples



# 1. PWM Mode Description

## -- PWM configuration steps

- Enable timer and related IO port clock
- Initialization timer: ARR, PSC
- Initialize output comparison parameters
- Enable preload register
- Enable timer
- Continuously change the value of CCRx to obtain PWM output with different duty cycle

02

# TIM1 Registers

# 2. TIM1 Registers
## -- TIM1_CR1

- TIM1 control register 1

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | CKD[1:0] | | ARPE | CMS[1:0] | | DIR | OPM | URS | UDIS | CEN |
| | | | | | | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

Bits 6:5 **CMS[1:0]**: Center-aligned mode selection

00: Edge-aligned mode. The counter counts up or down depending on the direction bit (DIR).

01: Center-aligned mode 1. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in TIMx_CCMRx register) are set only when the counter is counting down.

10: Center-aligned mode 2. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in TIMx_CCMRx register) are set only when the counter is counting up.

11: Center-aligned mode 3. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in TIMx_CCMRx register) are set both when the counter is counting up or down.

*Note: It is not allowed to switch from edge-aligned mode to center-aligned mode as long as the counter is enabled (CEN=1)*

Bit 4 **DIR**: Direction

0: Counter used as upcounter

1: Counter used as downcounter

*Note: This bit is read only when the timer is configured in Center-aligned mode or Encoder mode.*

# 2. TIM1 Registers
## -- TIM1_CCRx

- TIM1 capture/compare register (x = 1/2/3/4)
- There are 4 registers in total, corresponding to 4 output channels CH1 ~ 4
- In output mode, the content of CCRx is compared with the content of CNT, and the corresponding action is generated according to the comparison result. Using this, we can control the output pulse width by modifying the value of this register

# 2. TIM1 Registers
## -- TIM1_CCR1

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CCR1[15:0] | | | | | | | | | | | | | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

Bits 15:0 **CCR1[15:0]**: Capture/Compare 1 value

**If channel CC1 is configured as output**:

CCR1 is the value to be loaded in the actual capture/compare 1 register (preload value).

It is loaded permanently if the preload feature is not selected in the TIMx_CCMR1 register (bit OC1PE). Else the preload value is copied in the active capture/compare 1 register when an update event occurs.

The active capture/compare register contains the value to be compared to the counter TIMx_CNT and signaled on OC1 output.

**If channel CC1 is configured as input**:

CCR1 is the counter value transferred by the last input capture 1 event (IC1).

# 2. TIM1 Registers

## -- TIM1_CCMR1/2

- TIM1 capture/compare mode register 1/2
- TIM1_CCMR1 controls CH1 and CH2
- TIM1_CCMR2 controls CH3 and CH4
- The channel can be used for input (capture mode) or output (comparison mode), and the direction of the channel is defined by the corresponding CCxS bit. The functions of other bits of this register are different in input and output modes
- OCxx describes the functions of the channel in the output mode and ICxx describes the functions of the channel in the input mode. Therefore, it must be noted that the functions of the same bit in output mode and input mode are different

# 2. TIM1 Registers
## -- TIM1_CCMR1

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OC2 CE | OC2M[2:0] | | | OC2 PE | OC2 FE | CC2S[1:0] | | OC1 CE | OC1M[2:0] | | | OC1 PE | OC1 FE | CC1S[1:0] | |
| IC2F[3:0] | | | | IC2PSC[1:0] | | | | IC1F[3:0] | | | | IC1PSC[1:0] | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

**Output compare mode:**

Bit 15 **OC2CE:** Output Compare 2 clear enable

Bits 14:12 **OC2M[2:0]**: Output Compare 2 mode

Bit 11 **OC2PE**: Output Compare 2 preload enable

Bit 10 **OC2FE**: Output Compare 2 fast enable

Bits 9:8 **CC2S[1:0]**: Capture/Compare 2 selection

This bit-field defines the direction of the channel (input/output) as well as the used input.
00: CC2 channel is configured as output
01: CC2 channel is configured as input, IC2 is mapped on TI2
10: CC2 channel is configured as input, IC2 is mapped on TI1
11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is working only if an internal trigger input is selected through the TS bit (TIMx_SMCR register)

*Note: CC2S bits are writable only when the channel is OFF (CC2E = '0' in TIMx_CCER).*

# 2. TIM1 Registers
## -- TIM1_CCMR1(continued)

Bit 7 **OC1CE:** Output Compare 1 clear enable

OC1CE: Output Compare 1 Clear Enable
0: OC1Ref is not affected by the ETRF Input
1: OC1Ref is cleared as soon as a High level is detected on ETRF input

Bits 6:4 **OC1M**: Output Compare 1 mode

These bits define the behavior of the output reference signal OC1REF from which OC1 and OC1N are derived. OC1REF is active high whereas OC1 and OC1N active level depends on CC1P and CC1NP bits.
000: Frozen - The comparison between the output compare register TIMx_CCR1 and the counter TIMx_CNT has no effect on the outputs.(this mode is used to generate a timing base).
001: Set channel 1 to active level on match. OC1REF signal is forced high when the counter TIMx_CNT matches the capture/compare register 1 (TIMx_CCR1).
010: Set channel 1 to inactive level on match. OC1REF signal is forced low when the counter TIMx_CNT matches the capture/compare register 1 (TIMx_CCR1).
011: Toggle - OC1REF toggles when TIMx_CNT=TIMx_CCR1.
100: Force inactive level - OC1REF is forced low.
101: Force active level - OC1REF is forced high.
110: PWM mode 1 - In upcounting, channel 1 is active as long as TIMx_CNT<TIMx_CCR1 else inactive. In downcounting, channel 1 is inactive (OC1REF='0') as long as TIMx_CNT>TIMx_CCR1 else active (OC1REF='1').
111: PWM mode 2 - In upcounting, channel 1 is inactive as long as TIMx_CNT<TIMx_CCR1 else active. In downcounting, channel 1 is active as long as TIMx_CNT>TIMx_CCR1 else inactive.

*Note:* ***1:*** *These bits can not be modified as long as LOCK level 3 has been programmed (LOCK bits in TIMx_BDTR register) and CC1S='00' (the channel is configured in output).*

***2:*** *In PWM mode 1 or 2, the OCREF level changes only when the result of the comparison changes or when the output compare mode switches from "frozen" mode to "PWM" mode.*

Bit 3 **OC1PE**: Output Compare 1 preload enable

0: Preload register on TIMx_CCR1 disabled. TIMx_CCR1 can be written at anytime, the new value is taken in account immediately.
1: Preload register on TIMx_CCR1 enabled. Read/Write operations access the preload register. TIMx_CCR1 preload value is loaded in the active register at each update event.

*Note:* ***1:*** *These bits can not be modified as long as LOCK level 3 has been programmed (LOCK bits in TIMx_BDTR register) and CC1S='00' (the channel is configured in output).*

***2:*** *The PWM mode can be used without validating the preload register only in one pulse mode (OPM bit set in TIMx_CR1 register). Else the behavior is not guaranteed.*

Bit 2 **OC1FE**: Output Compare 1 fast enable

This bit is used to accelerate the effect of an event on the trigger in input on the CC output.
0: CC1 behaves normally depending on counter and CCR1 values even when the trigger is ON. The minimum delay to activate CC1 output when an edge occurs on the trigger input is 5 clock cycles.
1: An active edge on the trigger input acts like a compare match on CC1 output. Then, OC is set to the compare level independently from the result of the comparison. Delay to sample the trigger input and to activate CC1 output is reduced to 3 clock cycles. OCFE acts only if the channel is configured in PWM1 or PWM2 mode.

Bits 1:0 **CC1S**: Capture/Compare 1 selection

This bit-field defines the direction of the channel (input/output) as well as the used input.
00: CC1 channel is configured as output
01: CC1 channel is configured as input, IC1 is mapped on TI1
10: CC1 channel is configured as input, IC1 is mapped on TI2
11: CC1 channel is configured as input, IC1 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (TIMx_SMCR register)

# 2. TIM1 Registers
## -- TIM1_CCER

- TIM1 capture/compare enable register
- This register controls the switches of each input and output channel

# 2. TIM1 Registers
## -- TIM1_CCER(continued)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | CC4P | CC4E | CC3NP | CC3NE | CC3P | CC3E | CC2NP | CC2NE | CC2P | CC2E | CC1NP | CC1NE | CC1P | CC1E |
| | | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

Bits 15:14 Reserved, must be kept at reset value.

Bit 13 **CC4P**: Capture/Compare 4 output polarity
refer to CC1P description

Bit 12 **CC4E**: Capture/Compare 4 output enable
refer to CC1E description

Bit 11 **CC3NP**: Capture/Compare 3 complementary output polarity
refer to CC1NP description

Bit 10 **CC3NE**: Capture/Compare 3 complementary output enable
refer to CC1NE description

Bit 9 **CC3P**: Capture/Compare 3 output polarity
refer to CC1P description

Bit 8 **CC3E**: Capture/Compare 3 output enable
refer to CC1E description

# 2. TIM1 Registers
## -- TIM1_CCER(continued)

Bit 7 **CC2NP**: Capture/Compare 2 complementary output polarity
refer to CC1NP description

Bit 6 **CC2NE**: Capture/Compare 2 complementary output enable
refer to CC1NE description

Bit 5 **CC2P**: Capture/Compare 2 output polarity
refer to CC1P description

Bit 4 **CC2E**: Capture/Compare 2 output enable
refer to CC1E description

Bit 3 **CC1NP**: Capture/Compare 1 complementary output polarity
0: OC1N active high.
1: OC1N active low.
*Note: This bit is not writable as soon as LOCK level 2 or 3 has been programmed (LOCK bits in TIMx_BDTR register) and CC1S="00" (the channel is configured in output).*

Bit 2 **CC1NE**: Capture/Compare 1 complementary output enable
0: Off - OC1N is not active. OC1N level is then function of MOE, OSSI, OSSR, OIS1, OIS1N and CC1E bits.
1: On - OC1N signal is output on the corresponding output pin depending on MOE, OSSI, OSSR, OIS1, OIS1N and CC1E bits.

Bit 1 **CC1P**: Capture/Compare 1 output polarity
**CC1 channel configured as output:**
0: OC1 active high
1: OC1 active low
**CC1 channel configured as input:**
This bit selects whether IC1 or IC1 is used for trigger or capture operations.
0: non-inverted: capture is done on a rising edge of IC1. When used as external trigger, IC1 is non-inverted.
1: inverted: capture is done on a falling edge of IC1. When used as external trigger, IC1 is inverted.
*Note: This bit is not writable as soon as LOCK level 2 or 3 has been programmed (LOCK bits in TIMx_BDTR register).*

Bit 0 **CC1E**: Capture/Compare 1 output enable
**CC1 channel configured as output:**
0: Off - OC1 is not active. OC1 level is then function of MOE, OSSI, OSSR, OIS1, OIS1N and CC1NE bits.
1: On - OC1 signal is output on the corresponding output pin depending on MOE, OSSI, OSSR, OIS1, OIS1N and CC1NE bits.
**CC1 channel configured as input:**
This bit determines if a capture of the counter value can actually be done into the input capture/compare register 1 (TIMx_CCR1) or not.
0: Capture disabled.
1: Capture enabled.

# 2. TIM1 Registers
## -- TIM1_BDTR

- TIM1 break and dead-time register
- No need to configure this register when using general-purpose timers
- Need  to configure this register when using advanced timers

# 2. TIM1 Registers
## -- TIM1_BDTR(continued)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MOE | AOE | BKP | BKE | OSSR | OSSI | LOCK[1:0] | | DTG[7:0] | | | | | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

*Note: As the bits AOE, BKP, BKE, OSSI, OSSR and DTG[7:0] can be write-locked depending on the LOCK configuration, it can be necessary to configure all of them during the first write access to the TIMx_BDTR register.*

Bit 15 **MOE**: Main output enable

This bit is cleared asynchronously by hardware as soon as the break input is active. It is set by software or automatically depending on the AOE bit. It is acting only on the channels which are configured in output.
0: OC and OCN outputs are disabled or forced to idle state.
1: OC and OCN outputs are enabled if their respective enable bits are set (CCxE, CCxNE in TIMx_CCER register).
See OC/OCN enable description for more details (*Section 14.4.9: TIM1&TIM8 capture/compare enable register (TIMx_CCER) on page 348*).

Bit 14 **AOE**: Automatic output enable

0: MOE can be set only by software
1: MOE can be set by software or automatically at the next update event (if the break input is not be active)

*Note: This bit can not be modified as long as LOCK level 1 has been programmed (LOCK bits in TIMx_BDTR register).*

# 2. TIM1 Registers
# -- TIM1_BDTR(continued)

Bit 13 **BKP**: Break polarity

0: Break input BRK is active low
1: Break input BRK is active high

*Note: This bit can not be modified as long as LOCK level 1 has been programmed (LOCK bits in TIMx_BDTR register).*

*Note: Any write operation to this bit takes a delay of 1 APB clock cycle to become effective.*

Bit 12 **BKE**: Break enable

0: Break inputs (BRK and CSS clock failure event) disabled
1; Break inputs (BRK and CSS clock failure event) enabled

*Note: This bit cannot be modified when LOCK level 1 has been programmed (LOCK bits in TIMx_BDTR register).*

*Note: Any write operation to this bit takes a delay of 1 APB clock cycle to become effective.*

Bit 11 **OSSR**: Off-state selection for Run mode

This bit is used when MOE=1 on channels having a complementary output which are configured as outputs. OSSR is not implemented if no complementary output is implemented in the timer.
See OC/OCN enable description for more details (*Section 14.4.9: TIM1&TIM8 capture/compare enable register (TIMx_CCER) on page 348*).
0: When inactive, OC/OCN outputs are disabled (OC/OCN enable output signal=0).
1: When inactive, OC/OCN outputs are enabled with their inactive level as soon as CCxE=1 or CCxNE=1. Then, OC/OCN enable output signal=1

*Note: This bit can not be modified as soon as the LOCK level 2 has been programmed (LOCK bits in TIMx_BDTR register).*

Bit 10 **OSSI**: Off-state selection for Idle mode

This bit is used when MOE=0 on channels configured as outputs.
See OC/OCN enable description for more details (*Section 14.4.9: TIM1&TIM8 capture/compare enable register (TIMx_CCER) on page 348*).
0: When inactive, OC/OCN outputs are disabled (OC/OCN enable output signal=0).
1: When inactive, OC/OCN outputs are forced first with their idle level as soon as CCxE=1 or CCxNE=1. OC/OCN enable output signal=1)

*Note: This bit can not be modified as soon as the LOCK level 2 has been programmed (LOCK bits in TIMx_BDTR register).*

Bits 9:8 **LOCK[1:0]**: Lock configuration

These bits offer a write protection against software errors.
00: LOCK OFF - No bit is write protected.
01: LOCK Level 1 = DTG bits in TIMx_BDTR register, OISx and OISxN bits in TIMx_CR2 register and BKE/BKP/AOE bits in TIMx_BDTR register can no longer be written.
10: LOCK Level 2 = LOCK Level 1 + CC Polarity bits (CCxP/CCxNP bits in TIMx_CCER register, as long as the related channel is configured in output through the CCxS bits) as well as OSSR and OSSI bits can no longer be written.
11: LOCK Level 3 = LOCK Level 2 + CC Control bits (OCxM and OCxPE bits in TIMx_CCMRx registers, as long as the related channel is configured in output through the CCxS bits) can no longer be written.

Bits 7:0 **DTG[7:0]**: Dead-time generator setup

This bit-field defines the duration of the dead-time inserted between the complementary outputs. DT correspond to this duration.
DTG[7:5]=0xx => DT=DTG[7:0]x $t_{dtg}$ with $t_{dtg}=t_{DTS}$.
DTG[7:5]=10x => DT=(64+DTG[5:0])x$t_{dtg}$ with $T_{dtg}=2xt_{DTS}$.
DTG[7:5]=110 => DT=(32+DTG[4:0])x$t_{dtg}$ with $T_{dtg}=8xt_{DTS}$.
DTG[7:5]=111 => DT=(32+DTG[4:0])x$t_{dtg}$ with $T_{dtg}=16xt_{DTS}$.
Example if $T_{DTS}$=125ns (8MHz), dead-time possible values are:
0 to 15875 ns by 125 ns steps,
16 us to 31750 ns by 250 ns steps,
32 us to 63us by 1 us steps,
64 us to 126 us by 2 us steps

*Note: This bit-field can not be modified as long as LOCK level 1, 2 or 3 has been programmed (LOCK bits in TIMx_BDTR register).*

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# 03

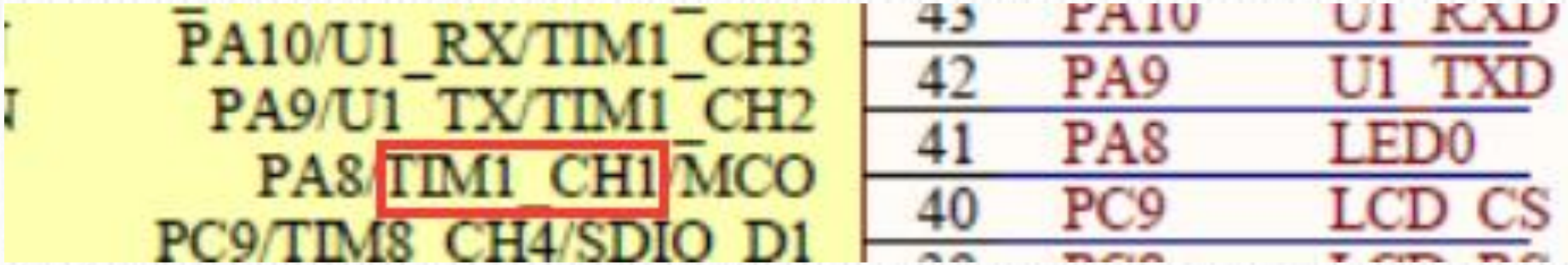
# How to Program

# 3. How to Program

- Our Goal
  - Use PWM signal to change the brightness of LED0
  - If we change the duty cycle of the PWM signal, we can change the average voltage, so as to change the brightness of the LED0

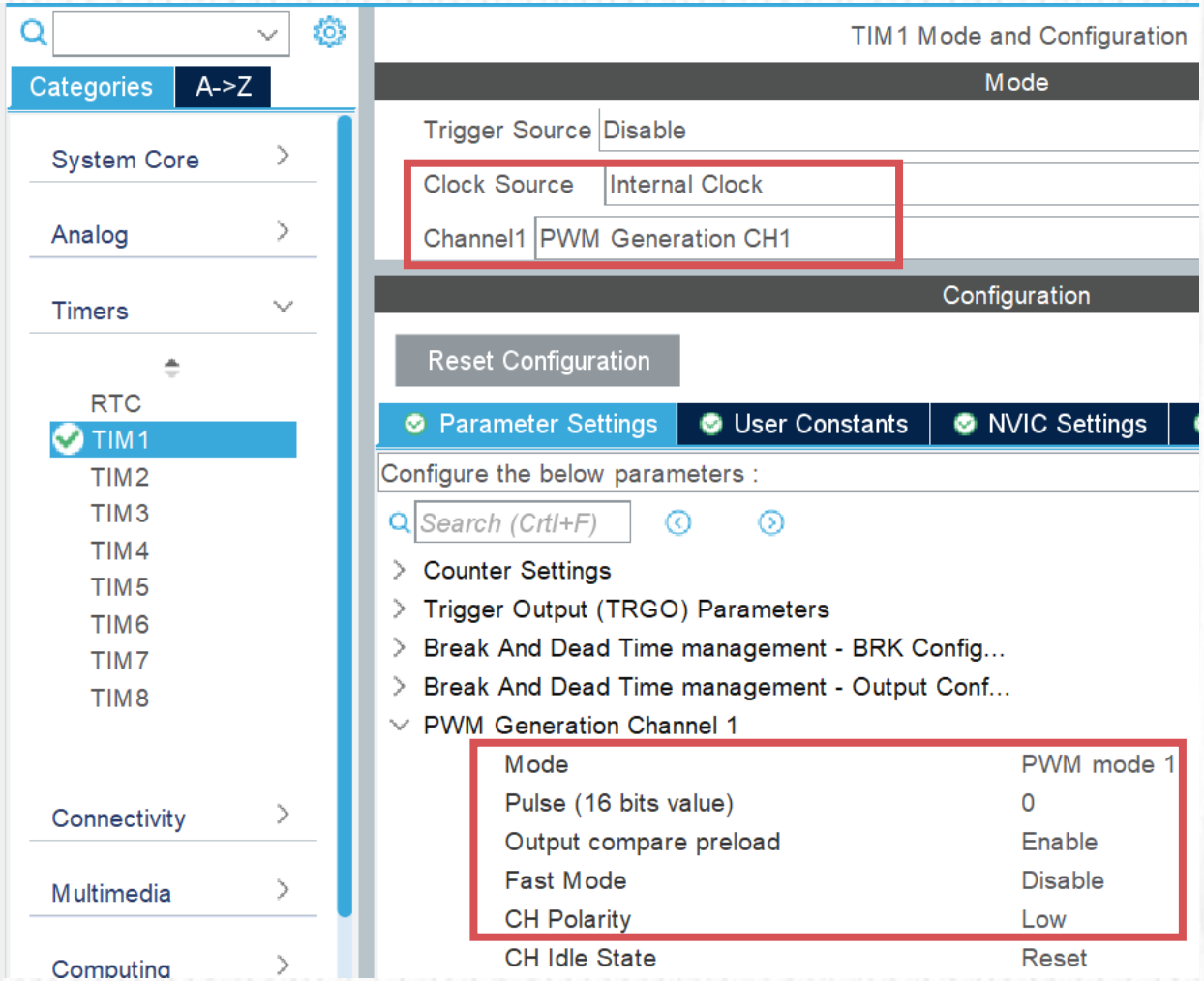
# 3. How to Program

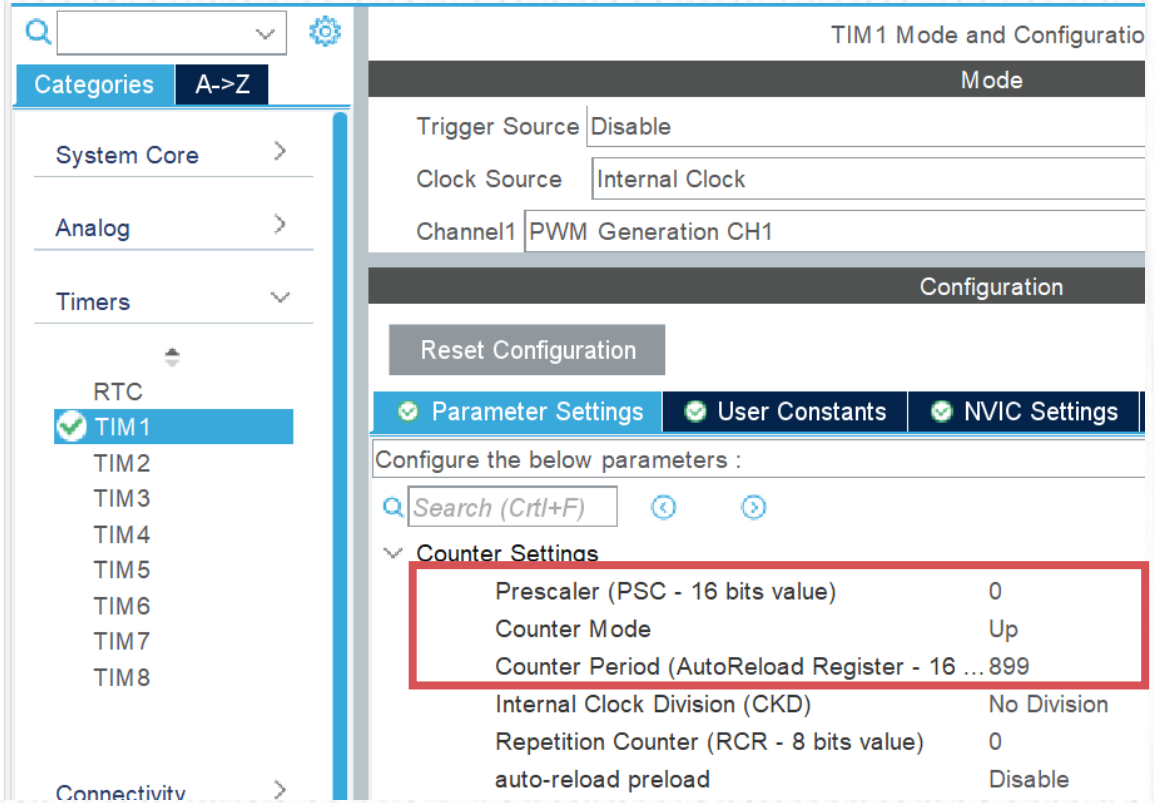
- Choose the TIMER
  - Since LED0 is connected to TIM1_CH1, we should enable TIM1 and configure the channel 1 of TIM1 as PWM Generation CH1
  - Set the CH Polarity as low, because the LED is on only when the voltage is low



# 3. How to Program

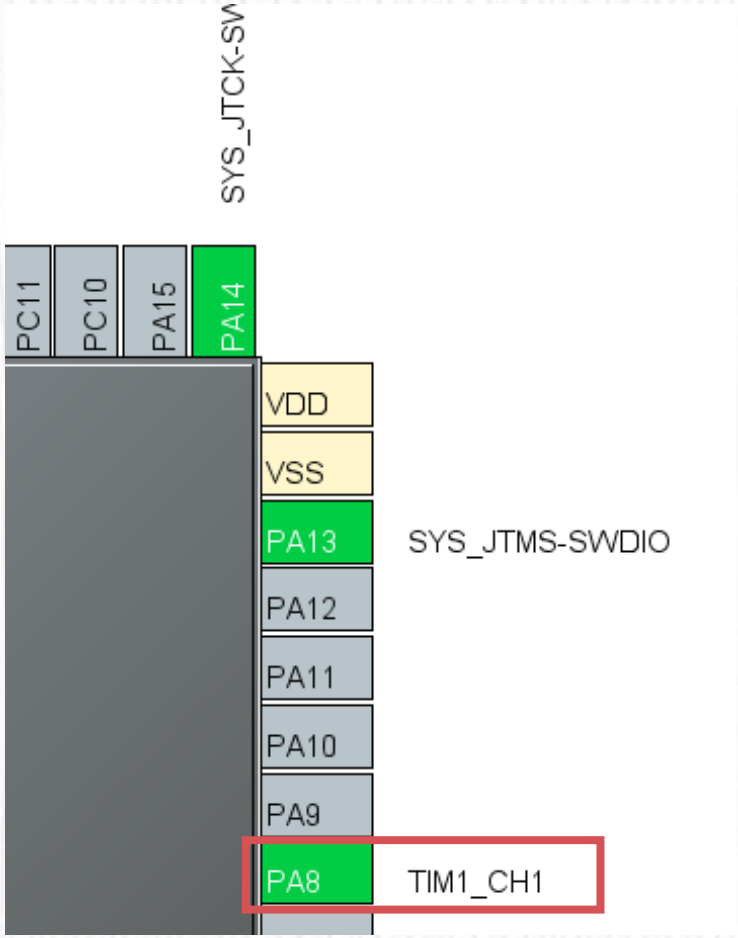
- Configure TIM1



# 3. How to Program

- Configure GPIO
  - After we set TIM1_CH1 as PWM Generation CH1, we can see that PA8 pin will be set as TIM1_CH1 in Pinout View.



# 3. How to Program

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- Some functions we used
  - Call HAL_TIM_PWM_Start() function to start the PWM signal generation in main.c (after the initialization of TIM1)
  - Change CCR1 value to change the duty cycle of TIM1_CH1 output

```
HAL_StatusTypeDef HAL_TIM_PWM_Start(TIM_HandleTypeDef *htim, uint32_t Channel)
```

# 3. How to Program

- Run the demo, the LED0 will gradually brighten and darken periodically
- The maximum duty cycle is set to 33% is because the relationship of brightness and voltage is not linear and when the duty cycle is 33%, the LED is bright enough.

```c
int main(void)
{
  /* MCU Configuration--------------------------
  /* Reset of all peripherals, Initializes the
  HAL_Init();
  /* Configure the system clock */
  SystemClock_Config();
  /* Initialize all configured peripherals */
  MX_GPIO_Init();
  MX_TIM1_Init();
  /* USER CODE BEGIN 2 */
  HAL_TIM_PWM_Start(&htim1, TIM_CHANNEL_1);
  int mode = 1;
  int pulse = 0;
  /* USER CODE END 2 */

  /* Infinite loop */
  while (1)
  {
    /* USER CODE BEGIN 3 */
    HAL_Delay(10);
    if (mode) {
      pulse++;
    } else {
      pulse--;
    }
    if (pulse > 300) {
      mode = 0;
    }
    if (pulse <= 0) {
      mode = 1;
    }
    TIM1->CCR1 = pulse;
  }
  /* USER CODE END 3 */
}
```

# 04

# Practice

# 4. Practice



- Design a desk lamp whose brightness can be adjusted manually.
- Use LED0 as the display component, and KEY0 and KEY1 as the adjustment buttons for the desk lamp.
- When KEY0 is pressed, the brightness of the desk lamp will become brighter. Press KEY0 again, and the brightness will continue to become brighter. Each time KEY0 is pressed, the lamp will become brighter until it reaches its maximum brightness (at least three brightness stages should be set). At the same time, LED1 flashes once to indicate that the maximum brightness has been reached.
- When KEY1 is pressed, the brightness of the desk lamp decreases. Each time KEY1 is pressed, the brightness will decrease until the desk lamp is completely turned off. At the same time, LED1 flashes once to indicate that the desk lamp has been turned off.

# 4. Practice



- 设计一个可手动调节亮度的台灯。
- 使用LED0作为台灯的显示单元，KEY0和KEY1作为台灯的调节按钮。
- 当按下KEY0时，台灯亮度变亮一些，再次按下KEY0，亮度继续变亮一些，直至达到最大亮度（台灯亮度至少设置出3个亮度阶段），同时LED1闪烁1次提示已经到达最大亮度。
- 当按下KEY1时，台灯亮度变暗一些，再次按下KEY1，亮度继续变暗一些，直至台灯完全关闭，同时LED1闪烁1次提示台灯已关闭。