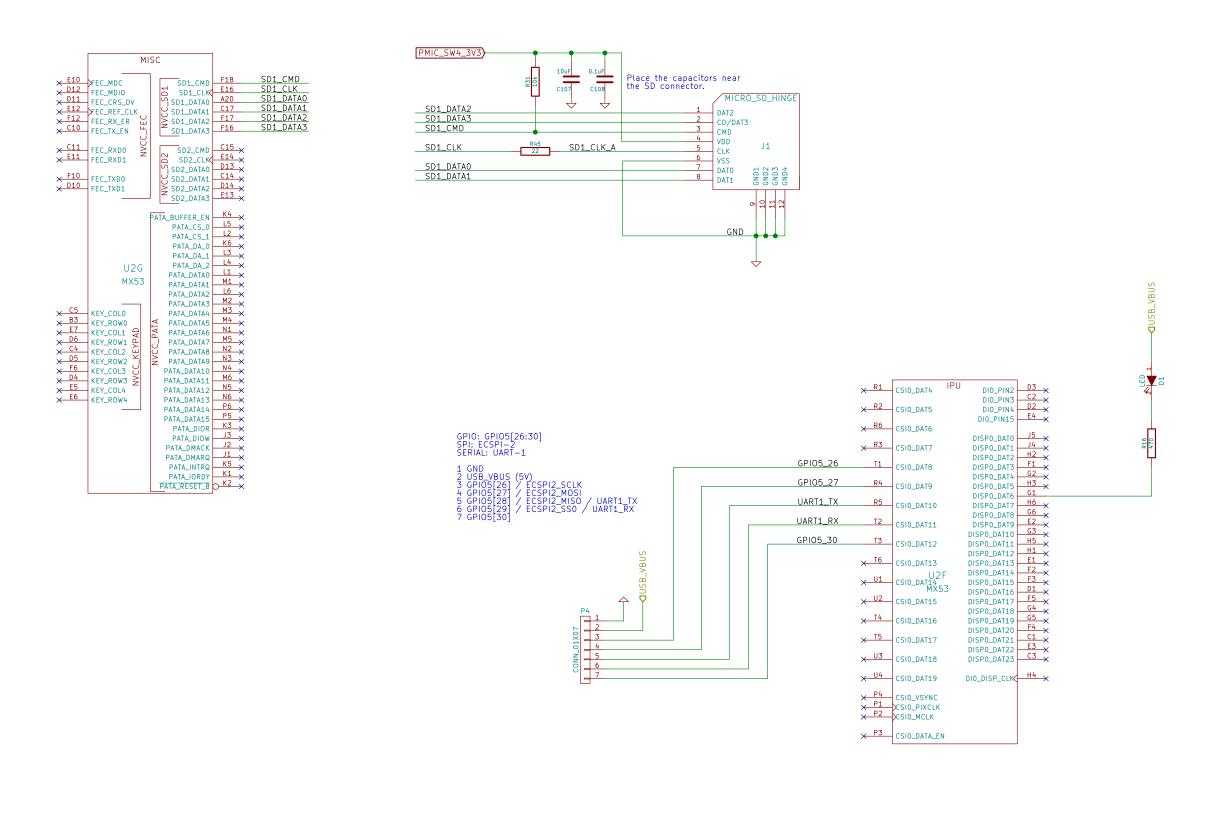


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Sheet: /i.MX53 MISC/
File: imx53-misc.sch

Title: USB ARMORY — i.MX53 GPIOs

 Size: A3
 Date: 10 Nov 2014
 Rev: MARK I

 KiCad E.D.A. eeschema (2014-jan-25)-product
 Id: 4/9



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Sheet: /Interfaces/ File: interfaces.sch

Title: USB ARMORY - i.MX53 SD INTERFACE

 Size: A3
 Date: 10 Nov 2014
 Rev: MARK I

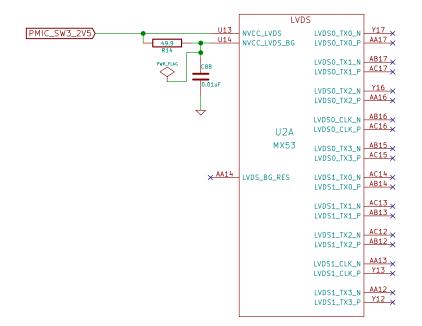
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floating: LVDSO_*, LVDS1_* Freescale QSB and SABRE reference schematics

floating: LVDS_BG_RES MX53UG Rev. 1, 3/2011, pg 30 Design checklist, Recommendation 21

LVDSO_* and LVDS1_* pads are muxed, NVCC_LVDS, NVCC_LVDS_BG, LVDS_BG_RES are not.

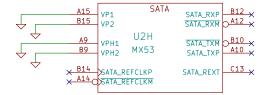


floating: SATA_REFCLKP, SATA_REFCLKM, SATA_RXP, SATA_RXM, SATA_TXM, SATA_TXP, SATA_REXT IMX53IEC Rev. 6, 03/2013, pg 117 4.7.13.4 SATA Connectivity when not in use

grounded: VP1, VP2, VPH1, VPH2 IMX53IEC Rev. 6, 03/2013, pg 117 4.7.13.4 SATA Connectivity when not in use

All the SATA pads are not muxed.

Warning: The temperature sensor is disabled when SATA module is not powered.



floating: TVDAC_VREF https://community.freescale.com/thread/309316

floating: TVDAC_COMP MX53UG Rev. 1, 3/2011, pg 29 Design checklist, Recommendation 14

Design checklist, Recommendation 14 floating: TVDAC_IO*, TVCDC_IO* MX53UG Rev. 1, 3/2011, pg 29 Design checklist, Recommendation 15

floating: TVDAC_DHVDD, TVDAC_AHVDDRGB* IMX53IEC Rev. 6, 03/2013, pg 26 4.2.3 Power Supplies Usage

All the TVE pads are not muxed.

× AB19		TVDAC_VREF	Y18 ×
× AC19	TVCDC_IOB_BACK TVDAC_IOB	TVDAC_COMP	AA19 ×
× AC20 × AB20	TVCDC_IOG_BACK M TVDAC_IOG	X53 TVDAC_DHVDD	U16 ×
× AB21 × AC21	TVCDC_IOR_BACK TVDAC_IOR TVDAC	J21 _AHVDDRGB_2	V16 🗸
^		_AHVDDRGB_1	U17 ×

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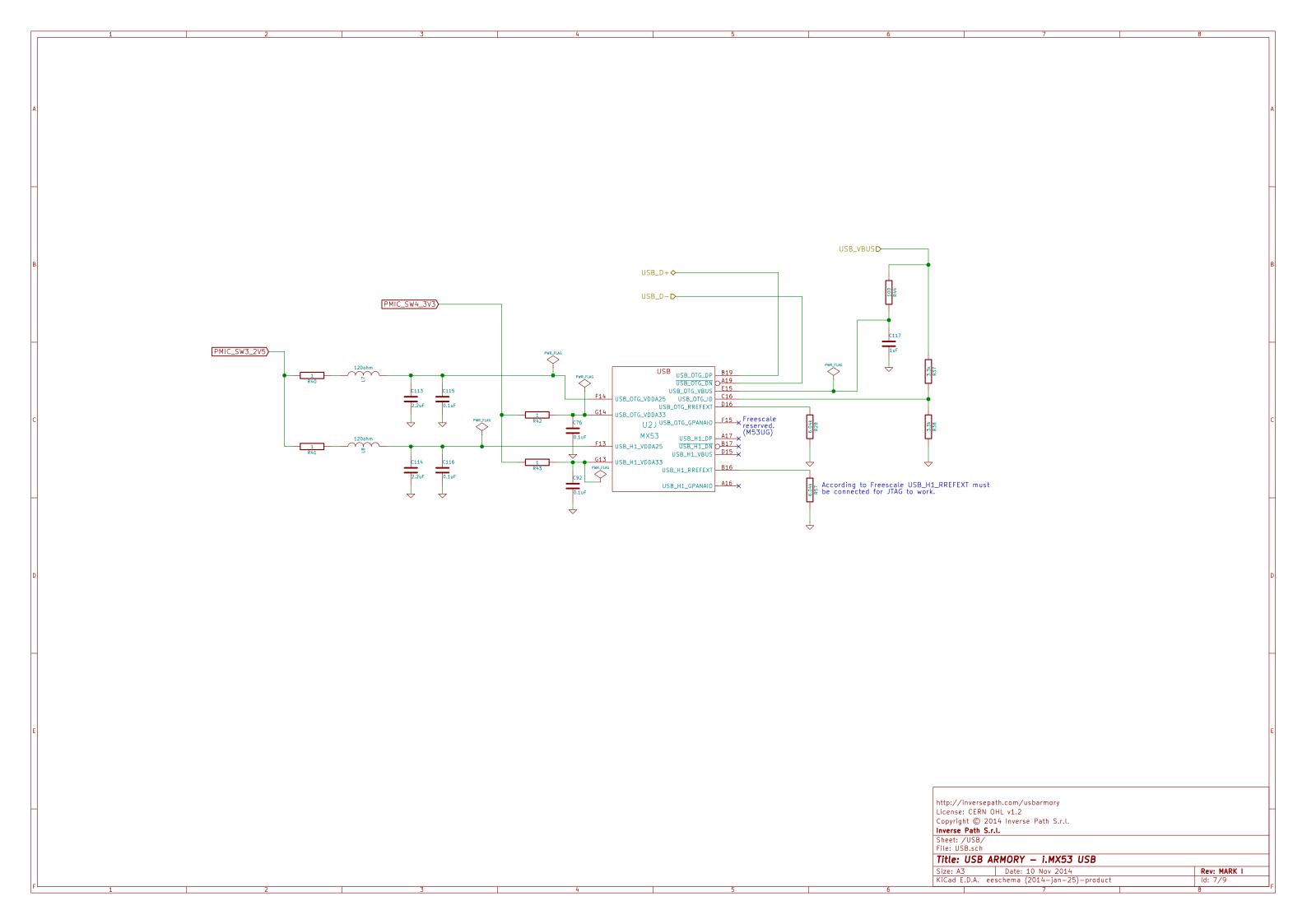
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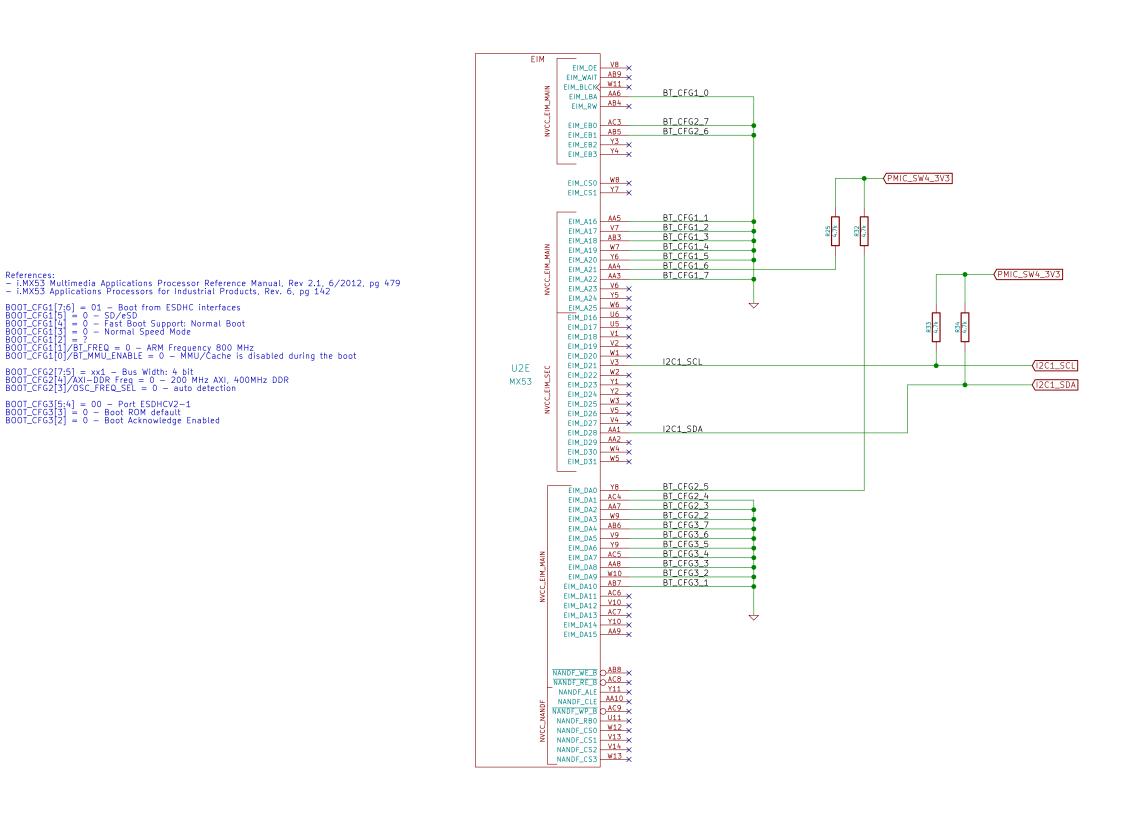
Sheet: /Unused/ File: unused.sch

Title: USB ARMORY - i.MX53 UNUSED

 Size: A3
 Date: 10 Nov 2014
 Rev: MARK I

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 Id: 6/9





BOOT_CFG1[7:6] = 01 - Boot from ESDHC interfaces
BOOT_CFG1[5] = 0 - SD/eSD
BOOT_CFG1[4] = 0 - Fast Boot Support: Normal Boot
BOOT_CFG1[4] = 0 - Normal Speed Mode
BOOT_CFG1[3] = 0 - Normal Speed Mode
BOOT_CFG1[2] = 7
BOOT_CFG1[1] / BT_FREQ = 0 - ARM Frequency 800 MHz
BOOT_CFG1[0] / BT_MMU_ENABLE = 0 - MMU/Cache is disabled during the boot

BOOT_CFG2[7:5] = xx1 - Bus Width: 4 bit BOOT_CFG2[4]/AXI-DDR Freq = 0 - 200 MHz AXI, 400MHz DDR BOOT_CFG2[3]/OSC_FREQ_SEL = 0 - auto detection

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Sheet: /Boot/ File: boot.sch

Title: USB ARMORY - BOOT

Size: A3 Date: 10 Nov 2014
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