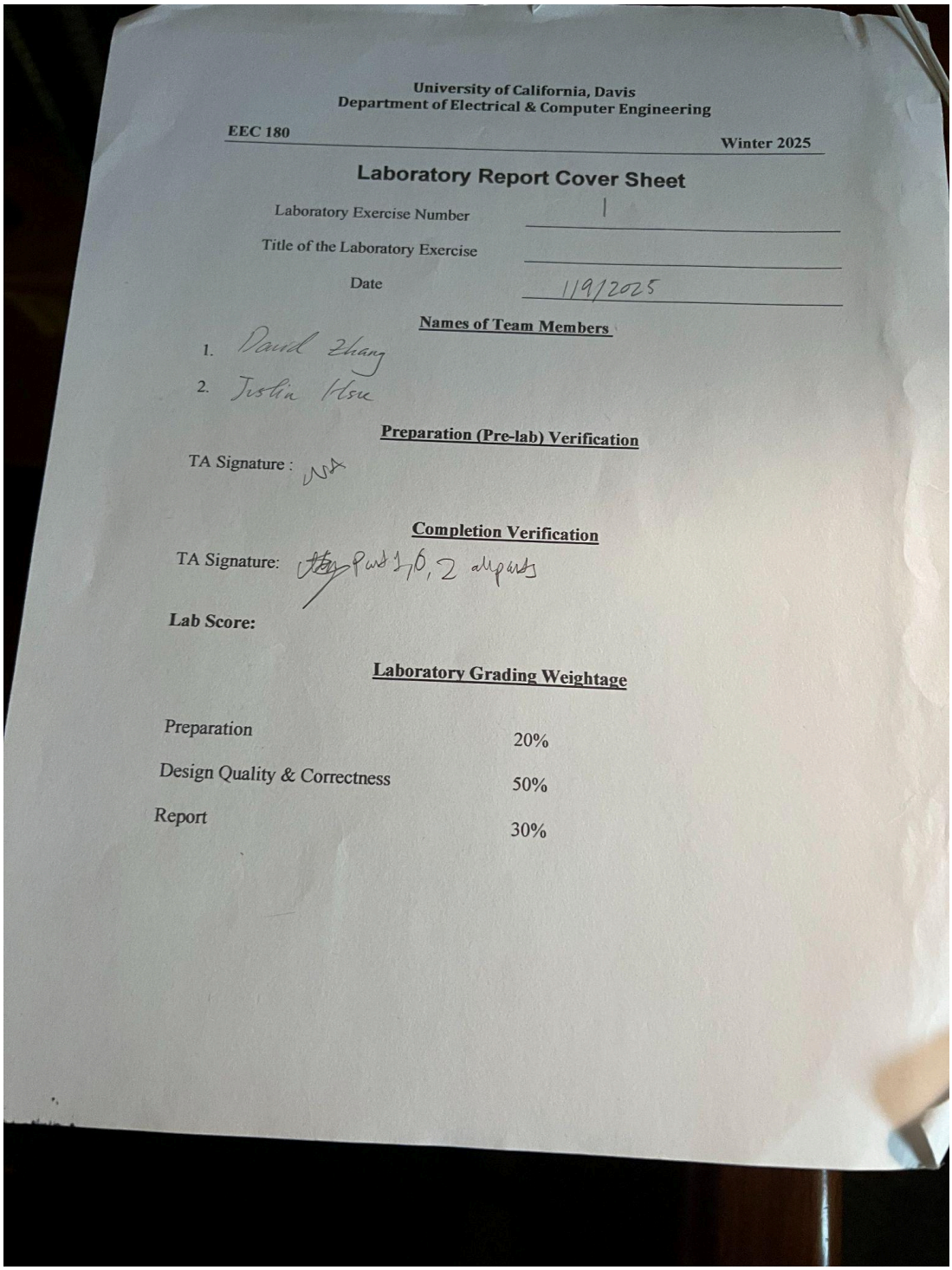
EEC 180 Lab 1
David Zhang and Justin Hsu
1/12/25

Sign off sheet:



University of California, Davis
Department of Electrical & Computer Engineering

EEC 180 Winter 2025

Laboratory Report Cover Sheet

Laboratory Exercise Number 1

Title of the Laboratory Exercise

Date 1/9/2025

Names of Team Members

1. David Zhang
2. Justin Hsu

Preparation (Pre-lab) Verification

TA Signature : NA

Completion Verification

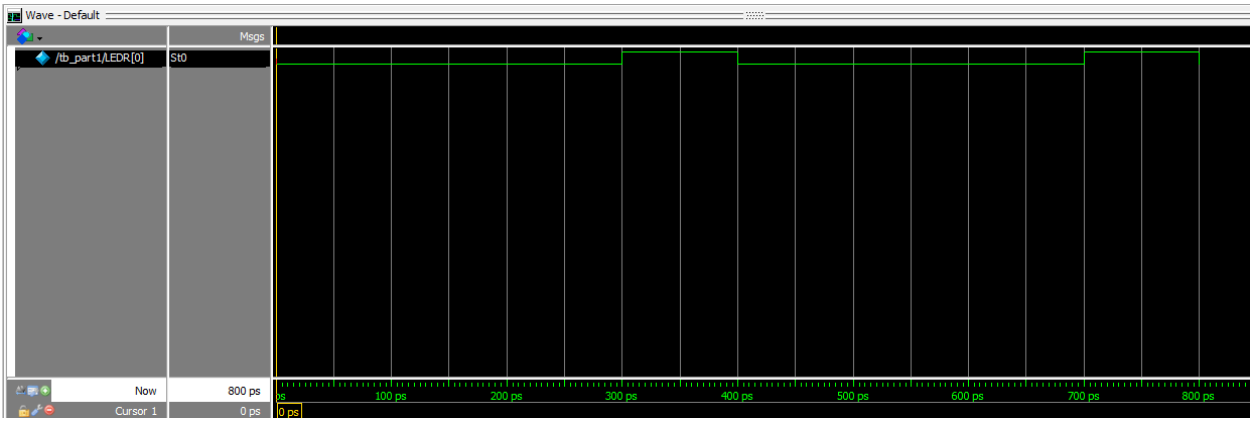
TA Signature: Pass 1,0,2 all parts

Lab Score:

Laboratory Grading Weightage

Preparation	20%
Design Quality & Correctness	50%
Report	30%

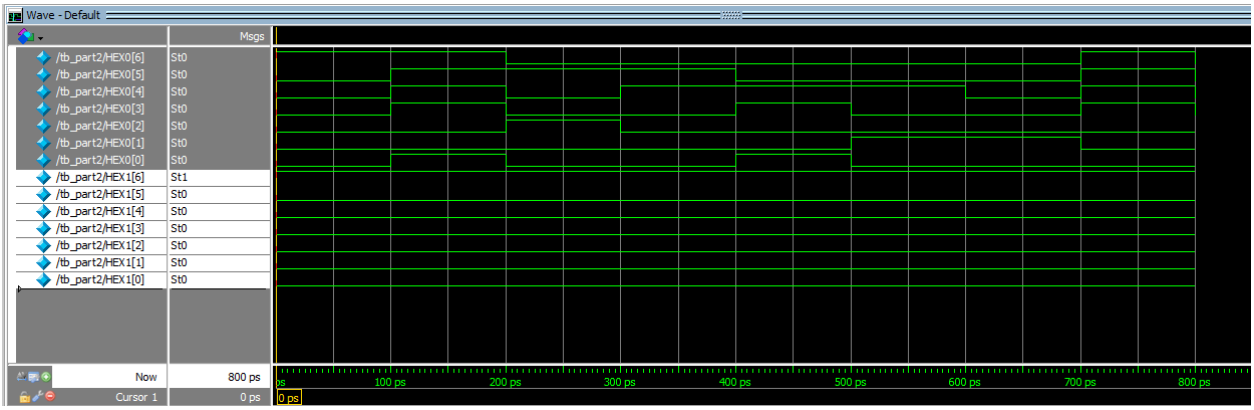
Part 1 testbench output:




```
ModelSim> vsim -gui work.tb_part1
# vsim -gui work.tb_part1
# Start time: 15:39:24 on Jan 12,2025
# Loading work.tb_part1
# Loading work.part1
add wave -position insertpoint  \
{sim:/tb_part1/LEDR[0]}
VSIM 3> run
# in = 000, out = 0
# in = 001, out = 0
# in = 010, out = 0
# in = 011, out = 1
# in = 100, out = 0
# in = 101, out = 0
# in = 110, out = 0
# in = 111, out = 1

VSIM 4>
```

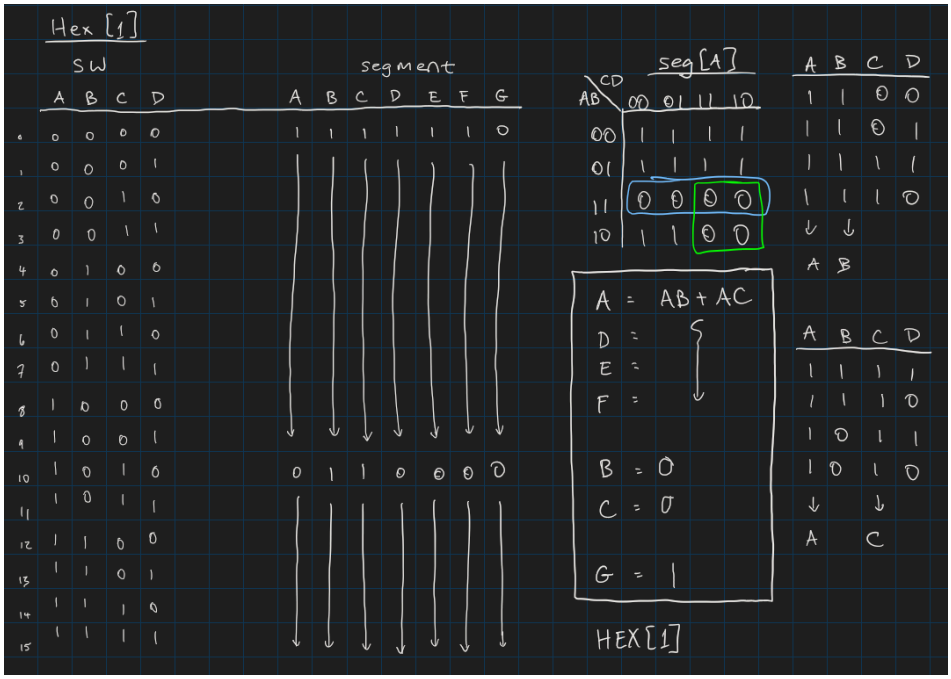
Part 2 testbench output:

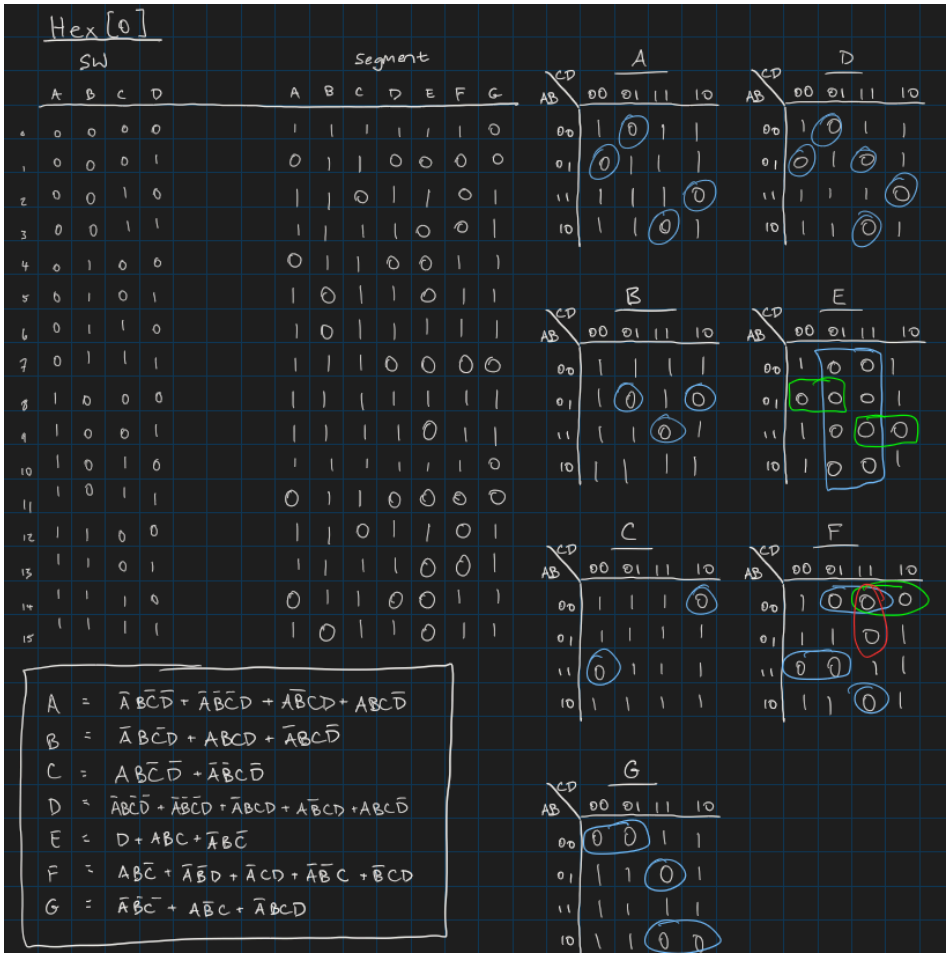


Transcript

```
# Loading work.part2
add wave -position insertpoint  \
{sim:/tb_part2/HEX0[6]} \
{sim:/tb_part2/HEX0[5]} \
{sim:/tb_part2/HEX0[4]} \
{sim:/tb_part2/HEX0[3]} \
{sim:/tb_part2/HEX0[2]} \
{sim:/tb_part2/HEX0[1]} \
{sim:/tb_part2/HEX0[0]}
add wave -position insertpoint  \
{sim:/tb_part2/HEX1[6]} \
{sim:/tb_part2/HEX1[5]} \
{sim:/tb_part2/HEX1[4]} \
{sim:/tb_part2/HEX1[3]} \
{sim:/tb_part2/HEX1[2]} \
{sim:/tb_part2/HEX1[1]} \
{sim:/tb_part2/HEX1[0]}
VSIM 4> run
# in = 0000, out = z1000000 z1000000
# in = 0001, out = z1000000 z1111001
# in = 0010, out = z1000000 z0100100
# in = 0011, out = z1000000 z0110000
# in = 0100, out = z1000000 z0011001
# in = 0101, out = z1000000 z0010010
# in = 0110, out = z1000000 z0000010
# in = 0111, out = z1000000 z1111000
```

Part II Truth Table and Karnaugh Maps:





Description of design:

Part 1 Design Description:
Our design consisted of turning on LEDR[0] when both switch[0] and switch[1] were flipped on. This was done using the module SW[0] & SW[1]. Our board behaved like expected, with LEDR[0] only turning on if those two specific switches were on. As we can see from our modelsim results, the simulated results also agree with our test results and expected results, and as we can see from the terminal, whenever the final two digits were 1, symbolizing switch 0 and 1 being turned on, the output of the LED would go high.

Part 2 Design Description:
The design goal of the second part of the lab is to enable decimal counting on the FPGA board. To do this, hexadecimal displays HEX[0] and HEX[1] were used to actually display the numbers in standard form, and switches SW[0]-SW[3] were used to count up to 4-bits. The difficulty with this goal was setting up the Karnaugh maps correctly, as each segment of the hexadecimal display needed a separate Karnaugh mapping to function. The finished and correct truth table and Karnaugh maps are shown in the section above. The testbench verified the validity of our design, as the results of the simulation for each hex-display segment matches the findings of the truth table.

Statement of contribution:
Evenly split between the two lab mates. Collaborated together on solving the k-maps, one typed up the half the code on quartus while the other typed up the other half on a text file and sent it over to the partner on quartus to paste into the project. Lab report was also evenly distributed, we each took half of the write ups.

Project organization:

All of our designs are under the /synthesis folder. They are grouped in /majority /part1 /part2 to go along with the different sections of the lab. The 7 segment decoder file is under /lab1/hdl. All of our modelsim projects are under /simulations/[part], with the work folder and the testbench files being within those folders.