

EEC 180 Lab 3

David Zhang and Justin Hsu

1/28/25

Check off:

University of California, Davis
Department of Electrical & Computer Engineering
Winter 2025

EEC 180

Laboratory Report Cover Sheet

Laboratory Exercise Number 3

Title of the Laboratory Exercise _____

Date 1/23/25

Names of Team Members

1. David Zhang

2. Justin Hsu

Preparation (Pre-lab) Verification

TA Signature: [Signature] Jan 23rd

Completion Verification

TA Signature: [Signature] Jan 23rd

Lab Score: + all parts [Signature] Jan 30th

Laboratory Grading Weightage

Preparation	20%
Design Quality & Correctness	50%
Report	30%

Description of design:

For the 4 bit leading zero detector, it was small enough in number of possible inputs that we were able to use a truth table and k-maps to design the logic for the leading zero detector.

For the 8 bit leading zero detector, since there could be $2^8=256$ possible input combinations, it is quickly apparent that using a truth table to solve and design the circuitry is extremely impractical. As a result, we had to create a module to combine 2 leading zero detector outputs. As a result, we came up with the logic that if the first 4 bits of the 8 bit number are 0, to add up the number of 0s in from both the leading zero detector outputs, and if the first 4 bits of the number are not 0 (there is a 1 in the first 4 bits of the number), to only look at the number of 0s from the first leading zero detector output.

Statement of Contribution:

Justin wrote the LZD code for part I and II, David wrote up the LED display code. Testbenches were split between both members. Contributions were evenly split between both members, while the actual code was written by only one member, coming up with the solutions for each part was done equally. The Report write up was split evenly between both members.

Prelab:

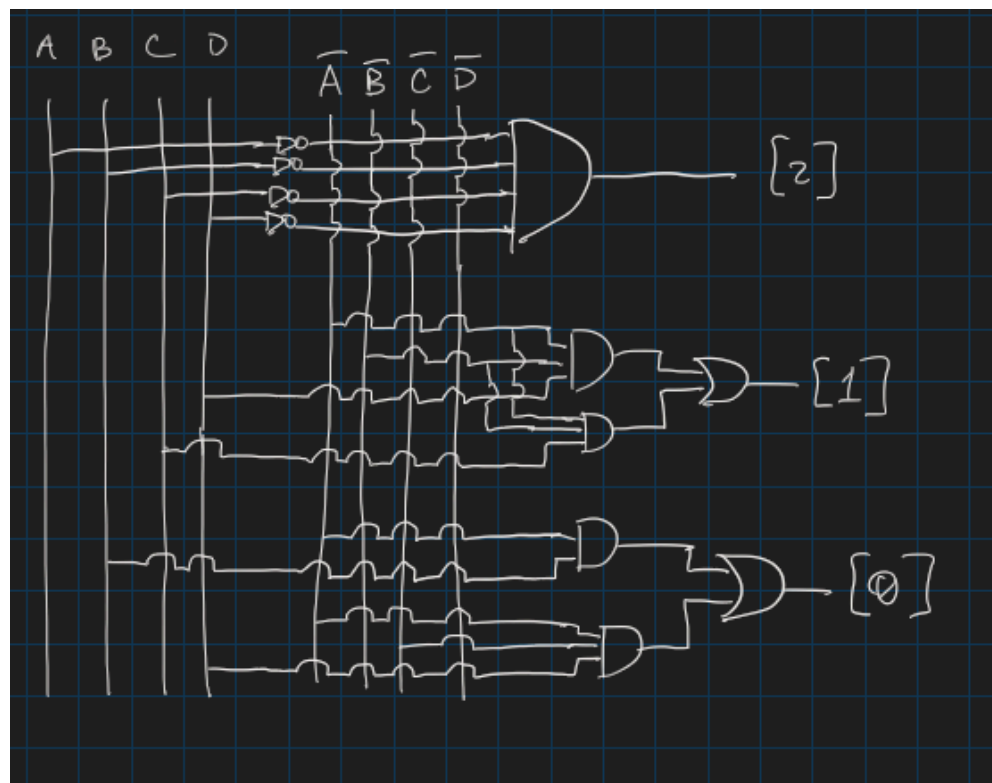
Prelab Leading zero detector

Input	Number of leading 0s		
S ₄ S ₃ S ₂ S ₁ S ₀	$\frac{Z}{2} \frac{1}{1} \frac{0}{0}$		
0 0 0 0	1 0 0	<u>2</u>	<u>1</u>
0 0 0 1	0 1 1		
0 0 1 0	0 1 0		
0 0 1 1	0 1 0		
0 1 0 0	0 0 1		
0 1 0 1	0 0 1		
0 1 1 0	0 0 1		
0 1 1 1	0 0 1		
1 0 0 0	0 0 0		
1 0 0 1	0 0 0		
1 0 1 0	0 0 0		
1 0 1 1	0 0 0		
1 1 0 0	0 0 0		
1 1 0 1	0 0 0		
1 1 1 0	0 0 0		
1 1 1 1	0 0 0		

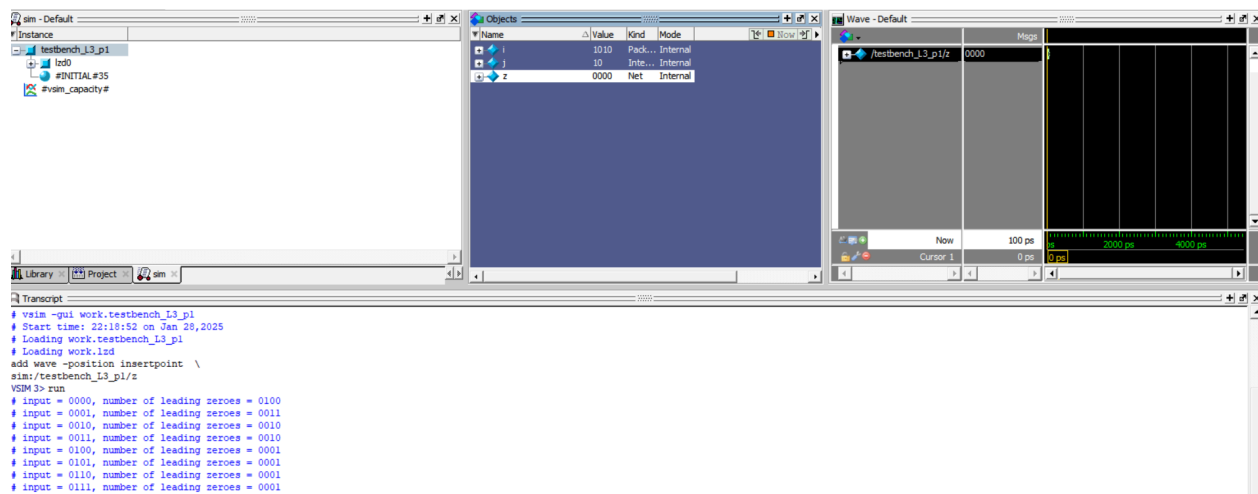
AB	CD		
00	00	1	0
00	01	0	0
00	11	0	0
00	10	0	0
01	00	0	0
01	01	0	0
01	11	0	0
01	10	0	0
10	00	0	0
10	01	0	0
10	11	0	0
10	10	0	0

$$Z = \overline{A}\overline{B}\overline{C}\overline{D}$$

$$1 = \overline{A}\overline{B}D + \overline{A}\overline{B}C$$

$$0 = \overline{A}B + \overline{A}\overline{C}D$$


Part I:



Part II:

