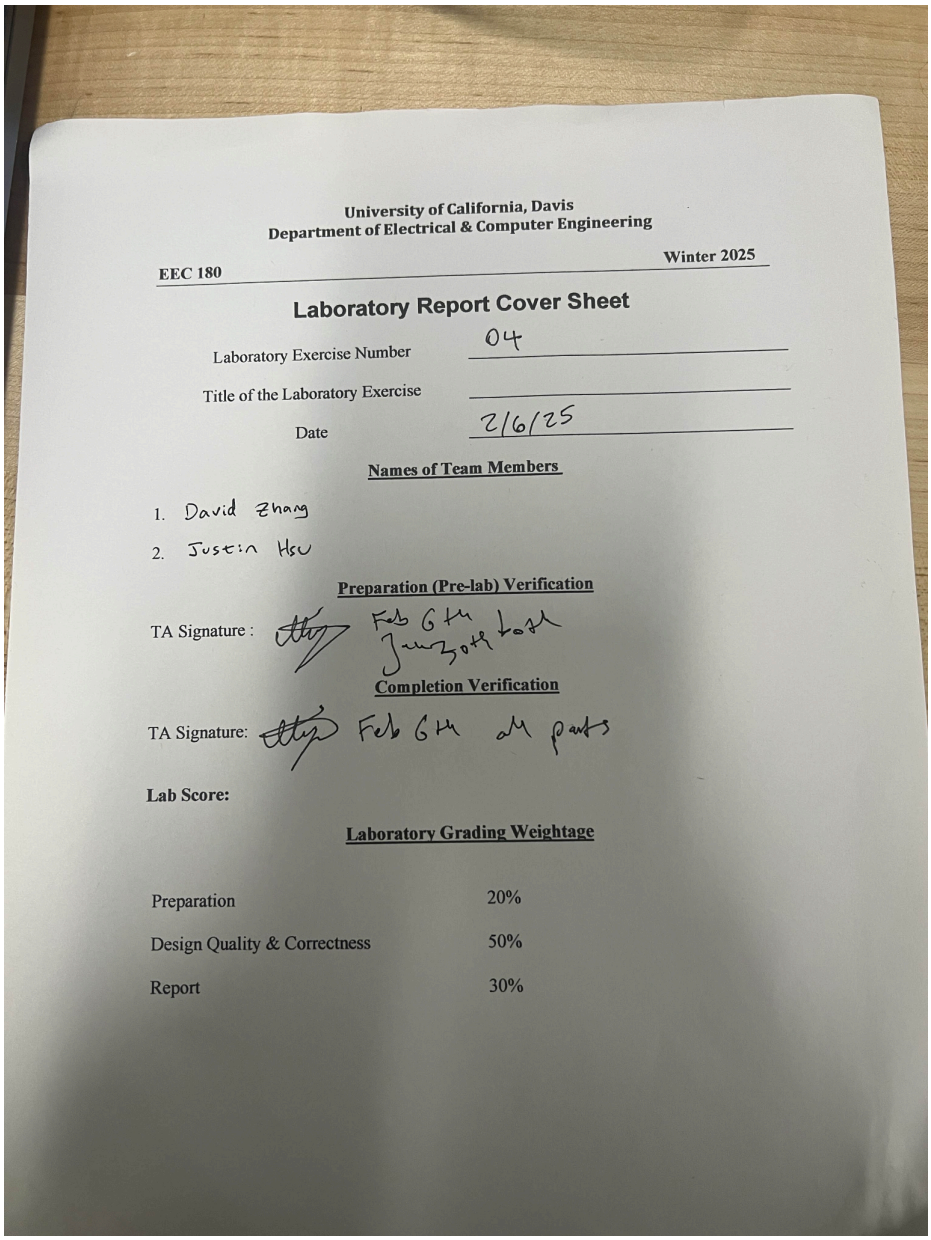
David Zhang and Justin Hsu
EEC 180
Lab 4
2/6/25

Sign off



University of California, Davis
Department of Electrical & Computer Engineering

EEC 180 Winter 2025

Laboratory Report Cover Sheet

Laboratory Exercise Number 04

Title of the Laboratory Exercise

Date 2/6/25

Names of Team Members

1. David Zhang
2. Justin Hsu

Preparation (Pre-lab) Verification

TA Signature : Feb 6th Jun 30th Last

Completion Verification

TA Signature: Feb 6th all parts

Lab Score:

Laboratory Grading Weightage

Preparation	20%
Design Quality & Correctness	50%
Report	30%

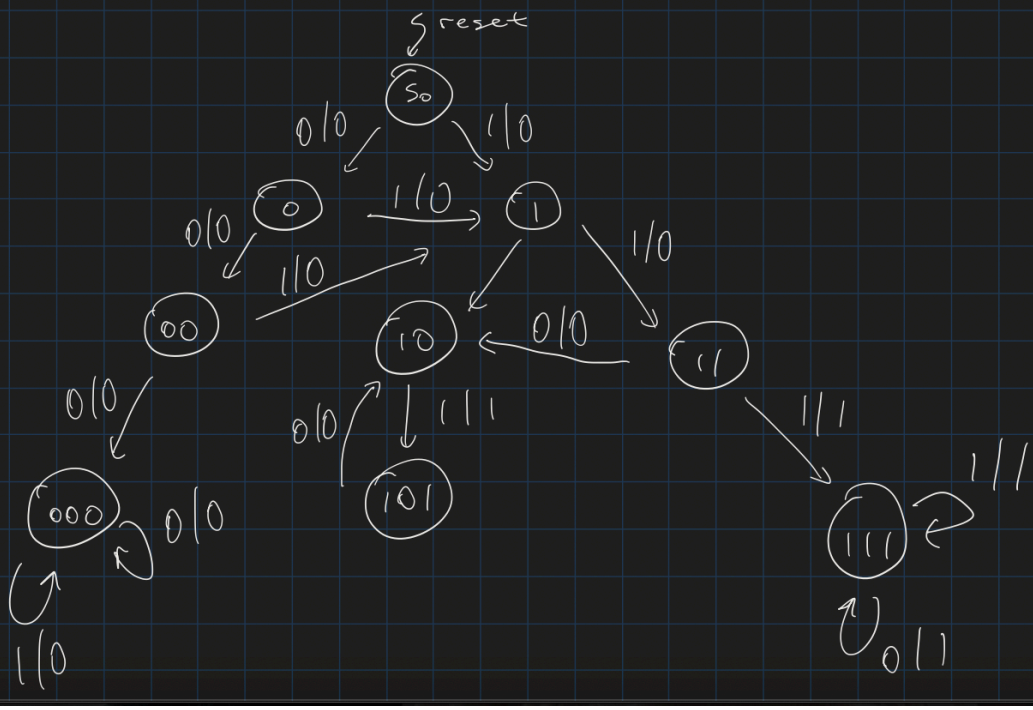
Prelab

3 bit sequence detector

Z = 1 when x = 101 if 000 and 111 not appear on x yet

Z = 0 when x = 000 indefinitely

Z = 1 when x = 111 indefinitely



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Test case 1
Time = 10 | X = 0 | State = 0100 | Z = 0
Time = 30 | X = 1 | State = 0101 | Z = 0
Time = 50 | X = 0 | State = 0001 | Z = 0
Time = 70 | X = 1 | State = 0010 | Z = 0
Time = 90 | X = 0 | State = 0011 | Z = 1
Time = 110 | X = 1 | State = 0010 | Z = 0
Time = 130 | X = 0 | State = 0011 | Z = 1
Time = 150 | X = 0 | State = 0010 | Z = 0
Time = 170 | X = 1 | State = 0101 | Z = 0
Time = 190 | X = 0 | State = 0001 | Z = 0
Time = 210 | X = 1 | State = 0010 | Z = 0
Time = 230 | X = 0 | State = 0011 | Z = 1
Time = 250 | X = 0 | State = 0010 | Z = 0
Time = 270 | X = 0 | State = 0101 | Z = 0
Time = 290 | X = 1 | State = 0110 | Z = 0
Time = 310 | X = 0 | State = 0110 | Z = 0
Time = 330 | X = 1 | State = 0110 | Z = 0
```

```
reset occurs, test case 2
Time = 380 | X = 1 | State = 0000 | Z = 0
Time = 390 | X = 0 | State = 0001 | Z = 0
Time = 410 | X = 1 | State = 0010 | Z = 0
Time = 430 | X = 0 | State = 0011 | Z = 1
Time = 450 | X = 1 | State = 0010 | Z = 0
Time = 470 | X = 0 | State = 0011 | Z = 1
Time = 490 | X = 1 | State = 0010 | Z = 0
Time = 510 | X = 0 | State = 0011 | Z = 1
Time = 530 | X = 1 | State = 0010 | Z = 0
Time = 550 | X = 0 | State = 0011 | Z = 1
Time = 570 | X = 1 | State = 0010 | Z = 0
Time = 590 | X = 1 | State = 0011 | Z = 1
Time = 610 | X = 1 | State = 0111 | Z = 0
Time = 630 | X = 0 | State = 1000 | Z = 1
Time = 650 | X = 1 | State = 1000 | Z = 1
Time = 670 | X = 0 | State = 1000 | Z = 1
Time = 690 | X = 1 | State = 1000 | Z = 1
Time = 710 | X = 0 | State = 1000 | Z = 1
```

Description of design

Our FSM is described by our state machine diagram. We input a specific value, and it will go through the state machine diagram. Whenever 101 is detected in a row, output will become 1. Whenever 111 is asserted, the output stays at 1, and whenever 000 is asserted, output stays at 0. We achieved this by manually setting our next states so this way we could control what would be output depending on the input.

Statements of Contribution

Members split work evenly. Both members developed versions for the mealy machine separately at first. Justin's worked first, so testing began with that version. That implementation worked with a random generator input, but had issues dealing with the lab inputs. David developed two, one similar to Justins and a brute force version. The brute force version proved effective. Debugging the brute force version and the testbench was done equally by both members during lab hours.