Sequential Circuit Design

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The Design Problem

A Mealy synchronous sequential circuit has one input and one output. The circuit examines a string of 0's and 1's applied to its input and generates an output when the sequence 1101 is detected at the input. Design the circuit described above using JK flip-flops. The circuit should be non-overlapping.

Introduction

A sequence detector accepts as input a string of bits: either 0 or 1. Its output goes to 1 when a target sequence has been detected. There are two basic types: overlap and non-overlap. In a sequence detector that allows overlap, the final bits of one sequence can be the start of another sequence. The sequence detector with no overlap allowed resets itself to the start state when the sequence has been detected.

Write the input sequence as 00110101101101. After the initial sequence 1101 has been detected, the detector with non-overlap resets and starts searching for the initial 1 of the next sequence. The detector with overlap allowed begins with the final 1 of the previous sequence as ready to be applied as the first 1 of the next sequence; the next bit it is looking for is the 0.

	Input	00110101101101
1101 sequence detector with overlap	Output	00000100001001
1101 sequence detector with non-overlap	Output	00000100001000

Digital Design

Design Procedure [1]

1. From the word description and specifications of the desired operation, derive a state diagram for the circuit.
2. Reduce the number of states if necessary.
3. Do state assignment.
4. Obtain the state table.

5. Choose the type of flip-flops to be used.
6. Derive the simplified flip-flop input equations and output equations.
7. Draw the logic diagram.

Step 1: Derive the State Diagram and the State Table

Step 1a: Determine the Number of States

This is a four-bit sequence detector, so the Finite State Machine (FSM) has four states. As indicated in the assignment, we label the states as A, B, C, and D.

Step 1b: Characterize Each State

Each state is characterized by what has been input and what is expected.

State	Has	Awaits
A	---	1101
B	1	101
C	11	01
D	110	1

Step 1c: Derive the State Diagram

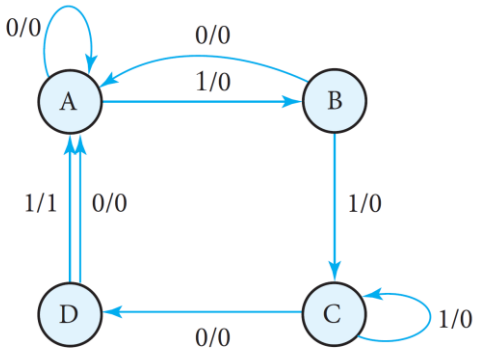
State A needs a 1 to cause a transition to state B. Given a 0 in state A, the FSM remains in state A.

State B has a 1 and needs a 1 to transition to state C. If state B gets a 0, the last two bits input are 10 – not a part of the sequence. Given a 0 in state B, the FSM returns to state A.

State C has the last two bits input as 11 and needs a 0 to transition to state D. If state C gets a 1, the last three bits input are 111 and the last two inputs are 11. Given a 1 in state C, the FSM remains in state C.

State D has the last three bits input as 110 and needs a 1 to complete the sequence. If state D gets a 0, the last four bits input are 1100 – not a part of the sequence. Given a 0 in state D, the FSM returns to state A.

The complete state diagram for the detector is thus as shown in Fig.1.



(Figure1 State Diagram for 1101 Sequence Detector without Overlap)

Step 1d: Generate the State Table

The state table as shown below is in the minimum form, there is no requirement for state reduction.

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
A	A	B	0	0
B	A	C	0	0
C	D	C	0	0
D	A	A	0	1

(State Table)

Step2: State Assignment [2]

State	Assignment 1, Binary	Assignment 2, Gray Code	Assignment 3, One-Hot
A	00	00	0001
B	01	01	0010
C	10	11	0100
D	11	10	1000

Step3: Obtain the Binary-coded State Table

Present State		Input	Next State		Output
A	B	x	A^+	B^+	y
0	0	0	0	0	0
0	0	1	0	1	0

0	**1**	**0**	**0**	**0**	**0**
0	**1**	**1**	**1**	**0**	**0**
1	**0**	**0**	**1**	**1**	**0**
1	**0**	**1**	**1**	**0**	**0**
1	**1**	**0**	**0**	**0**	**0**
1	**1**	**1**	**0**	**0**	**1**

Step4: Determine the number of Flip-Flops required

To get the number of flip-flops required, the following equation should be solved.

$$2^{P-1} < N \leq 2^{P}, where\ N\ is\ the\ number\ of\ states$$

For $N = 4$,

$$2^{P-1} < 4 \leq 2^{P}$$

$P = 2$ is the solution. Hence, we need two flip-flops.

Setp5: Decide the Type of Flip-Flops to Use[3]

The problem specifies that JK flip-flops be used. For JK flip-flops, the input equation can not be obtained directly from the next state. To determine the input equations for the flip-flops, it is necessary to derive a functional relationship between the state table and the input equations for analyzing sequential circuits and for defining the operation of the flip-flops. For this reason, we shall need to use the excitation table as shown below to deduce the inputs to each flip-flop that will make the circuit behave in the desired manner.

$Q(t)$	$Q(t=1)$	J	K
0	**0**	**0**	***X***
0	**1**	**1**	***X***
1	**0**	***X***	**1**
1	**1**	***X***	**0**

(JK Flip-Flop Excitation Table)

Step6: Synthesis Using JK Flip-Flops

Step6a: Generate the State Table and JK Flip-Flop Inputs[3]

Present State		**Input**	**Next State**		**Flip-Flop Inputs**			
A	B	x	A^+	B^+	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X

0	1	0	0	0	0	X	X	1
0	1	1	1	0	1	X	X	1
1	0	0	1	1	X	0	1	X
1	0	1	1	0	X	0	0	X
1	1	0	0	0	X	1	X	1
1	1	1	0	0	X	1	X	1

(State Table with JK Flip-Flop Inputs)

Step6b: Derive and simplify flip-flop input equations[3]

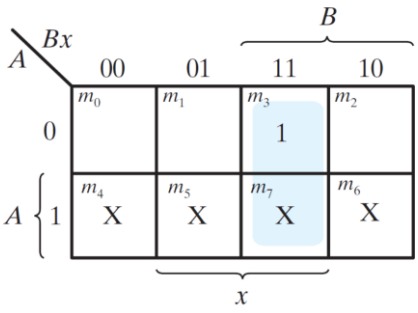
The state table with JK flip-flop inputs is separated into four different tables, one for each input of JK flip-flops.

A	B	x	J_A
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	X
1	0	1	X
1	1	0	X
1	1	1	X

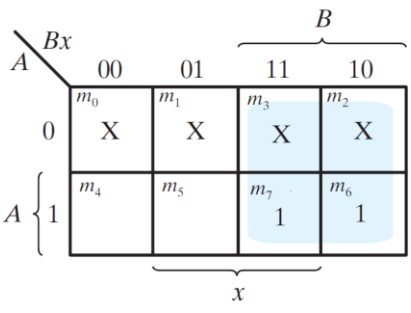
A	B	x	K_A
0	0	0	X
0	0	1	X
0	1	0	X
0	1	1	X
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

A	B	x	J_B
0	0	0	0
0	0	1	1
0	1	0	X
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	X
1	1	1	X

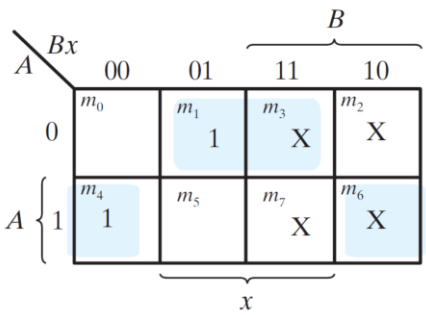
A	B	x	K_B
0	0	0	X
0	0	1	X
0	1	0	1
0	1	1	1
1	0	0	X
1	0	1	X
1	1	0	1
1	1	1	1



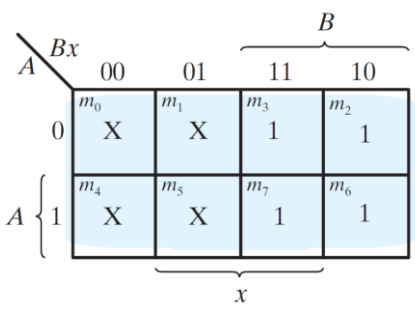
$J_A = Bx$



$K_A = B$



$J_B = A \oplus x$



$K_B = 1$

(Figure2 Maps for J and K Input Equations)

Step6c: Generate the Output Table and Output Equation

Present State		Input	Output
A	B	x	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

The only output occurs when $x = 1$, $A = 1$ and $B = 1$
The output equation is thus :

$$y = xAB$$

Step6d: Summarize the Equations

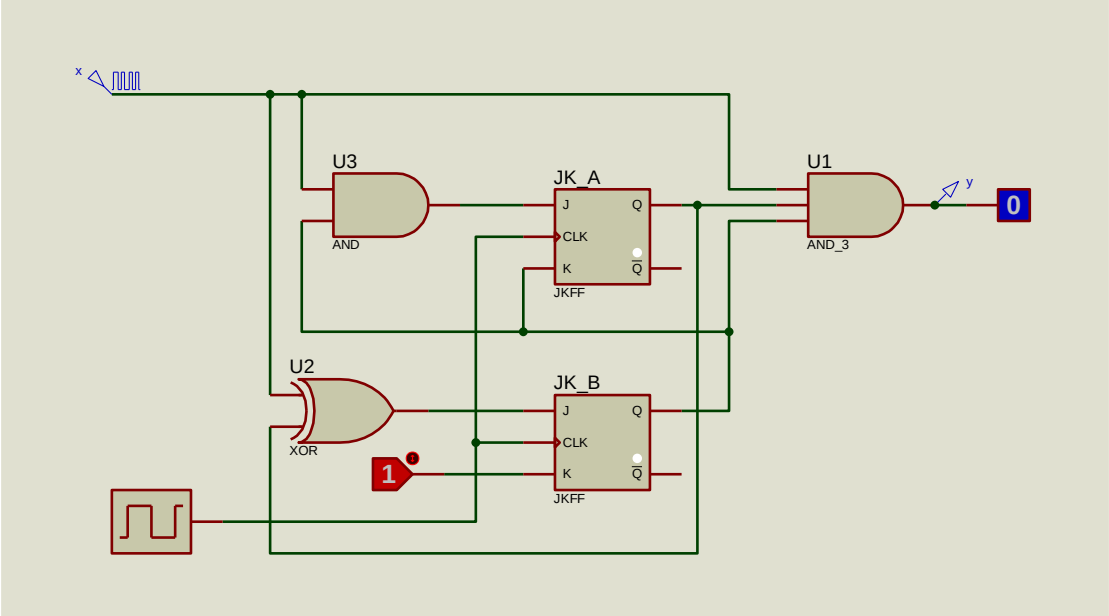
The output equation is:

$$y = xAB$$

For the inputs of the JK flip-flops:

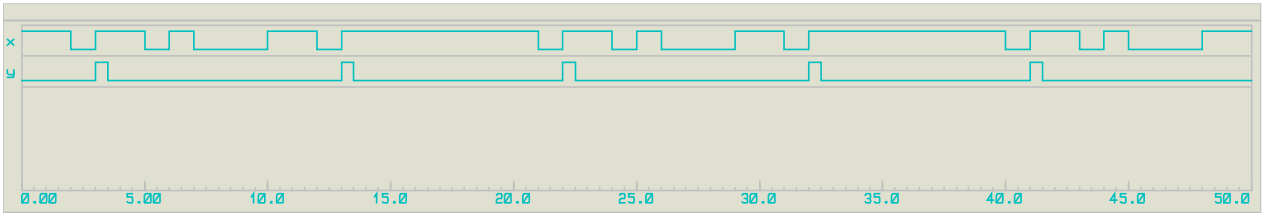
$$J_A = Bx \qquad J_B = A \oplus x$$
$$K_A = B \qquad K_B = 1$$

Step7: Draw the logic diagram



(Figure3 Logic diagram for 1101 Sequence Detector without Overlap with JK flip-flops)

Verification



(Figure4 Input and Output Graph for the Designed 1101 Sequence Detector)

Reference

[1] Mano, M., Ciletti, M. and Chandavarkar, B., n.d. *Digital design*. 5th ed. pp.236-237.
[2] Mano, M., Ciletti, M. and Chandavarkar, B., n.d. *Digital design*. 5th ed. p.235.
[3] Mano, M., Ciletti, M. and Chandavarkar, B., n.d. *Digital design*. 5th ed. pp.241-242.