Company Confidential 3/14
DATASHEET Revision 0.1 AD19SDMUXLP\_36to24\_M10
\*all “Digital Inputs” And “Digital Outputs”
Level Are 0-1.2v
\*all “Analog Inputs” And “Analog Outputs”
Level Are 0-3.3v
SEMODE DIGITAL INPUT SINGLE ENDED MODE SELECTION BIT.
IF SEMODE=0 , THE ADC OPERATES AS DIFFERENTIAL
INPUT ADC.
IF SEMODE=1 , AINM<0> IS TAKEN AS NEGATIVE INPUT.
AINP<9:0> IS SELECTED AS POSITIVE INPUT DEPENDING ON
S<3:0>.
LPMODE<1:0> DIGITAL INPUT SPEED/POWER CONTROL BITS FOR ADC. PLEASE REFER TO
SECTION 3.0 FOR DETAIL.
RESETN DIGITAL INPUT ACTIVE LOW RESET.MUST BE APPLIED ONCE AT THE
BEGINNING OF OPERATION AFTER POWER UP.
START DIGITAL INPUT POSITIVE LEVEL AT START INPUT INITIATES THE CONVER-
SION PROCESS.
OKIN ANALOG INPUT WHEN OKIN = 0V (DENOTES vdd 1.2v IS NOT PRESENT)
ANALOG IS IN POWER DOWN
WHEN OKIN = A VDD (DENOTES vdd 1.2v IS PRESENT)
ANALOG IS FUNCTIONAL
THIS PIN HAS GOT HIGHER PRIORITY OVER “EN” PIN.
EN DIGITAL INPUT ENABLE SIGNAL FOR ADC, IF EN=1 ADC IS FUNCTIONAL
MODE
EN=0 IS POWER DOWN MODE
SLEEP DIGITAL INPUT IF EN=1 AND SLEEP =0 ADC IS FUNCTIONAL MODE;
EN=1 AND SLEEP= 1 ADC IS IN SLEEP MODE;
EN=0 AND SLEEP=X ADC IS IN POWER DOWN
EOC DIGITAL OUTPUT END OF CONVERSION SIGNAL. EOC IS PULLED HIGH AFTER
CONVERSION.
EOC=1 DENOTES THAT DIGITAL DATA IS READY
D<18:0> DIGITAL OUTPUT 19 BIT DIGITAL DATA.THIS BUS CONTAINS V ALID DATA
ONLY IF “EOC” IS HIGH
TEST IN/OUT
PINS
TBD TBD
SCAN IN/OUT
PINS
TBD TBD
Name I/O Function

4/14 Company Confidential
AD19SDMUXLP\_36to24\_M10 Revision 0.1 DATASHEET
3.0 ELECTRICAL PARAMETERS
Parameters MIN TYP MAX
ANALOG INPUT
RANGE
Single Ended
AINM = dc (0 to
avdd)
AINP
GAIN is set by
PGA>=1
GAIN set by PGA <1
VREFP/GAIN
VREFP
ANALOG INPUT
RANGE
Differential
(AINP-AINM)
GAIN is set by
PGA>=1
GAIN is set by
PGA<1
+/- VREFP/GAIN
+/- VREFP
ANALOG INPUT
COMMON MODE
(AINP+AINM)/2 AGND A VDD/2 A VDD
DIFFERENTIAL
INPUT
IMPEDENCE
Zd
For Gain=1
For Gain=2
For Gain=4,8,16,32
Fclk= Input Clock
frequency in MHz
-20% from Typ 960/Fclk KOhm
480/Fclk Kohm
240/Fclk Kohm
+20 % from Typ
COMMON MODE
INPUT
IMPEDENCE
Zc
For Gain=1
For Gain=2
For Gain=4,8,16,32
Fclk= Input Clock
frequency in MHz
-20% from Typ 800/Fclk K Ohm
400/Fclk Kohm
200/Fclk Kohm
+20 % from Typ
CURRENT
DRAWN FROM
INPUT
From AINP
From AINM
(AINP-AINM)/Zd + (INCM-VCM)/Zc
(AINM-AINP)/Zd + (INCM-VCM)/Zc
INCM=(AINP+AINM)/2 , VCM=A VDD/2
IMPEDENCE AT
VREFP
For
Gain=1,2,4,8,16,32
Gain=1/2
Gain=1/3
Fclk= Input Clock in
MHz
-20% from Typ
(384/Fclk
KOhm)||200Kohm
192/Fclk Kohm ||
200Kohm
130/Fclk
Kohm||200Kohm
+20 % from Typ

Company Confidential 5/14
DATASHEET Revision 0.1 AD19SDMUXLP\_36to24\_M10
POWER SUPPLY ANALOG SUPPLY 2.4V/2.2V\* 3.3V 3.6V
DIGITAL SUPPLY 0.8V 1.2V 1.32V
EXTERNAL REF-
ERENCE VOLT-
AGES
VREFP 1.1 A VDD A VDD
VREFN 0V 0V 0V
RESOLUTION 19 bit
OUTPUT DATA
FORMAT
GAIN\*(AINP-AINM)
=0
GAIN\*(AINP-AINM)
=VREFP
GAIN\*(AINP-AINM)
=-VREFP
Parallel
Unsigned
Binary
1000000000000000000
1111111111111111111
0000000000000000000
CLOCK
REQUIREMENT
FREQUENCY
LPMODE<1:0>=00
=01
=10
=11
2.56MHz
1.28MHz
640KHz
0
6.4MHz
2.56MHz
1.28MHz
640KHz
6.4MHz
2.56MHz
1.28MHz
640KHz
DUTY CYCLE 40% 50% 60%
RMS JITTER
(LONG TREM)
250pS
CONVERSION
TIME
NORMAL MODE 640 Cycles
OUTPUT RATE LPMODE<1:0>=00
=01
=10
=11
4 Ksps
2 Ksps
1Ksps
0
10Ksps
4Ksps
2Ksps
1Ksps
10Ksps
4ksps
2Ksps
1Ksps
START UP TIME FROM POWER
DOWN
FROM SLEEP
100uS
2uS
Parameters MIN TYP MAX

6/14 Company Confidential
AD19SDMUXLP\_36to24\_M10 Revision 0.1 DATASHEET
PERFORMANCE
PARAMETERS
(Differential
Mode)
With A VDD=
VREFP=3.3V
In Single Ended
Mode: SNR and
THD would be
6 dB worse
At 2.4V
(Avdd=Vrefp) SNR
will be 3 dB worse
as compare to
Avdd=Verfp=3.3v
INL +/- 4 LSB
DNL +/- 1 LSB
GAIN ERROR
Gain Drift
With Temperature
With A VDD
With Input Common
Mode
+/- 1%
0.01 %/degreeC
0.2 %/V
0.1 %/V
OFFSET
Offset Drift
With Temperature
With A VDD
With Input Common
Mode
+/- 100 LSB
0.25 LSB/degree C
20 LSB/V
10 LSB/V
SNR
Gain=1
Gain=2 and 1/2
Gain=4 and 1/3
Gain=8
Gain=16
Gain=32
100dB
97dB
94dB
88dB
82dB
76dB
THD (in All Gain) 100 dB
TEMPERATURE -40 25 125
AREA 0.65 mm^2
CURRENT CON-
SUMPTION\*\*
A VDD
LPMODE=00
01
10
11
0.9 mA
0.7 mA
0.5 mA
0.4 mA
vdd
LPMODE=00
01
10
11
TBD
TBD
TBD
TBD
A VDD
vdd
(POWER DOWN-
MODE,EN=0)
1uA
TBD
A VDD
vdd
(SLEEP MODE
EN=1,SLEEP=1)
40uA
TBD
Parameters MIN TYP MAX

7/14 Company Confidential
AD19SDMUXLP\_36to24\_M10 Revision 0.1 DATASHEET
\* at AVDD=2.2V Full speed is not acheive-
able.Max speed achievable is 7.5Ksps i.e.
Input Clock frequency should be 4.8MHz
\*\* Power consumption max/min would vary
wrt typ by +/- 30%.
\*\*\* Gain= 4 and above are functional ONLY
when Avdd=3.3v +/- 10% in full speed mode
i.e LPMODE=11.
Gain=4 and above are functional for till
Avdd=2.4V in lower speed Mode i.e.
LPMODE=00/01/10

8/14 Company Confidential
AD19SDMUXLP\_36to24\_M10 Revision 0.1 DATASHEET
4.0 GAIN AND INPUT RANGE
VREFP
VREFN
V
t
AINP
AINM
Differential Mode Gain=1
Digital Output ( min to max )
(AINP+AINM)/2 =(VREFP+VERFM)/2
VREFP
VREFN
V
t
AINP
AINM
Differential Mode Gain=2
Digital Output ( min to max )
(AINP+AINM)/2 =(VREFP+VERFM)/2
0.75\*VREFP
0.25\*VREFP
VREFP
VREFN
V
t
AINP
AINM
Differential Mode Gain=2
Digital Output ( min to max )
(AINP+AINM)/2 =(VREFP+VERFM)/4
0.5\*VREFP
VREFP
VREFN
V
t
AINP
AINM
Differential Mode Gain=2
Digital Output ( min to max )
(AINP+AINM)/2 =3\*(VREFP+VERFM)/4
0.5\*VREFP
min=0000000000000000000
max=1111111111111111111
mid=1000000000000000000

VREFP
VREFN
V
t
AINP
=AINM
SE Mode Gain=1
Digital Output ( mid to max )
VREFP
VREFN
V
t
SE Mode Gain=2
Digital Output ( min to mid )
VREFP
VREFN
V
t
AINP
=AINM
SE Mode Gain=2
Digital Output ( mid to max )
0.5\*VREFP
VREFP
VREFN
V
t
AINP
=AINM
SE Mode Gain=2
Digital Output ( min to mid )
0.5\*VREFP
=AINM
AINM = VREFN
AINM = VREFP
AINM=VREFN AINM=VREFP
9/14 Company Confidential
AD19SDMUXLP\_36to24\_M10 Revision 0.1 DATASHEET

VREFP
VREFN
V
t
AINP
AINM
SE Mode Gain=1
Digital Output ( 0.25\*max to 0.75\*max )
VREFP
VREFN
V
t
SE Mode Gain=2
Digital Output SATURATED
VREFP
VREFN
V
t
AINP
=AINM
SE Mode Gain=4
Digital Output ( mid to max )
0.25\*VREFP
VREFP
VREFN
V
t
AINP
=AINM
SE Mode Gain=4
Digital Output ( min to mid )
0.75\*VREFP
=AINM
AINM = (VREFP+VREFN)/2
AINM=VREFN AINM=VREFP
AINM
AINM = (VREFP+VREFN)/2
10/14 Company Confidential
AD19SDMUXLP\_36to24\_M10 Revision 0.1 DATASHEET

11/14 Company Confidential
AD19SDMUXLP\_36to24\_M10 Revision 0.1 DATASHEET
5.0 INPUT/REFERENCE INTERFACE
Csmp
S2
AINP
CLK
S3
Cfb
CLK
R=200K
VREFP
AIN Interface
VREFP interface
Zin
Constant R=250K also to be considred in Zin Calculation i.e
Zineffective = Zinsw in Parallel with 200K Ohm
S2
CLK
AINM
Zd
AINP
AINM
Zc
INCM
VCM=A VDD/2
=(AINP+AINM)/2
CLK
Equivalent Differential Circuit Equivalent Common Mode Circuit
Iavg(AINP)= (AINP-AINM)/Zd + (INCM-VCM)/Zc
Iavg(AINM)= (AINM-AINP)/Zd + (INCM-VCM)/Zc

12/14 Company Confidential
AD19SDMUXLP\_36to24\_M10 Revision 0.1 DATASHEET
6.0 FUNCTIONAL/TIMNG DESCRIPTION
Functional/Timing description is shown below.
EN and SLEEP inputs to be conﬁgured for
ADC functional mode selection.The ADC
would be in power up condition and ready for
conversion after the delay speciﬁed in section
3.0.
RESETN must be applied (1 to 0 to 1) prior to
application of START. The width of RESETN
must be atleast 2 CLK pulses wide.
EOC remains at ‘0’ initially.
To start a conversion process : START = ‘1’ to
be applied.
START is detected at falling edge of
CLK.Conversion process starts from the sub-
sequent falling edge.At the onset of conversion
process: If EOC was at ‘0’ (for the ﬁrst con-
version after power up) it remains at ‘0’.If
EOC was at ‘1’ (due to end of one conversion
process) it will be pulled to ‘0’.
The mux/gain/lpmode selection bits are cap-
tured in the same falling edge of CLK in which
EOC is pulled to ‘0’.The setting decided by
these bits remains unchanged for that particu-
lar conversion cycle.
Conversion takes total 638 cycles.
During conversion process: START will not be
detected any more.At that time START can go
High or Low any number of times without
impacting the conversion process.
The START pulse should be at least one CLK
pulse wide (from rising edge to rising edge of
CLK) for a safe initiation of a Conversion Pro-
cess.
EOC is pulled High (at falling edge of
CLK)after conversion i.e. 638 cycles.The valid
digital data is available in data output lines
when EOC=1.
EOC remains ‘1’ till a new “START=1” is
detected at CLK falling edge.
It can be clearly seen that maximum sample
rate is achieved when START is constantly
kept at ‘1’.
With this conﬁguration output is available in
every 640 Cycle.
Hence output rate is = CLK/640.
Also EOC remains Low for 638 cycles and
High for 2 cycle.

CLK
SLEEP
RESETN
START
EOC
DATA
638Cycles 638 Cycles 638 Cycles
Mux/Gain setting bits are captured at this edge and remains constant throughout the conversion
EN
13/14 Company Confidential
AD19SDMUXLP\_36to24\_M10 Revision 0.1 DATASHEET
7.0 INTEGRATION GUIDELINE
To be added
8.0 RECOMMENDED IO RING
To be added

14/14 Company Confidential
AD19SDMUXLP\_36to24\_M10 Revision 0.1 DATASHEET
9.0 HISTORY
Date
Document
Version
Applicable
IP Version
Changes wrt previous version Prepared by
30-08-2012 0.1 1.0 First Release
(derived from
AD19SDMUX\_36to24\_M10
v0.7)
Chandrajit
Debnath
12-05-2014 0.2 1.0 - INL/DNL/THD updated Chandrajit
Debnath