



**commodore semiconductor group**  
**NMOS**

## 6560/6561 Video Interface Chip (VIC)

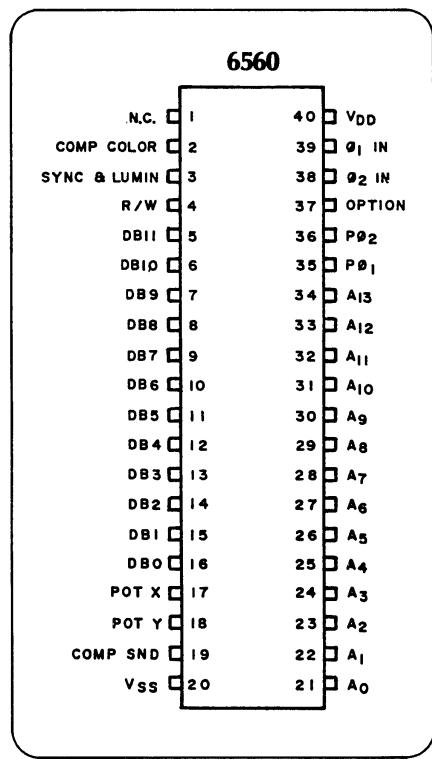
- Fully Expandable System With 16K Byte Address Space
- Mask-Programmable Sync Generation (NTSC-6560 or PAL-6561)
- On-Chip Color Generation
- Up to 600 Independently Programmable And Movable Background Locations
- Screen Grid Size Up to 192 x 200
- Two Selectable Graphic Character Sizes
- On-Chip Sound System
- On-Chip DMA And Address Generation
- 16 Addressable Control Registers
- Light Gun/Pen For Target Games

### DESCRIPTION

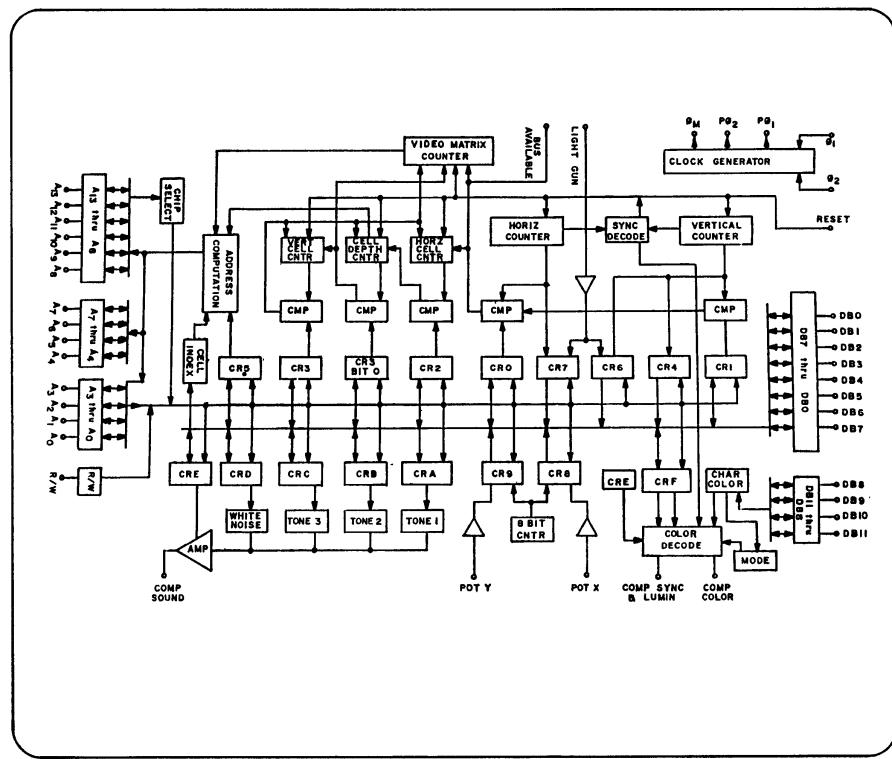
The 6560/6561 Video Interface Chip (VIC) is designed to implement color video graphics applications such as low-cost CRT terminals, biomedical monitors, control system displays and arcade/home video games. It provides all circuitry necessary for generating color programmable character graphics with high-screen resolution. VIC also incorporates sound effects and A/D converters for use in a video game environment.

Its on-chip sound system includes three independent, programmable tone generators, a white-noise generator and an amplitude modulator. It is designed so that no CPU wait states are required during screen refresh and offers the option of interlaced or non-interlaced operation via a switch which is programmable. The 6560/6561 provides two modes of color operation.

### PIN CONFIGURATION



### BLOCK DIAGRAM



#### Note

MCS = Ceramic package

MPS = Plastic package

## 6560 SIGNAL DESCRIPTION

### **Address Bus (A<sub>0</sub>-A<sub>13</sub>)**

The 14-bit address bus (A<sub>0</sub>-A<sub>13</sub>) is bidirectional. During P0<sub>2</sub> = 1, the address pins are in the input mode. In this mode the microprocessor can access any of the sixteen VIC Control Registers. The high order pins of the Address Bus (A<sub>8</sub> thru A<sub>13</sub>) act as Chip Select pins in this input mode. A true chip select condition occurs when A<sub>13</sub> = A<sub>11</sub> = A<sub>10</sub> = A<sub>9</sub> = A<sub>8</sub> = 0 and A<sub>12</sub> = 1, which equates to a VIC chip select address of 1000 in HEX. The lower order 4 bits of the address bus (A<sub>0</sub> thru A<sub>3</sub>) are used as the control register select portion of the input address.

During P0<sub>1</sub> = 1, the VIC address pins will be in the output mode if data (either Character Pointer or Character Cell) is to be fetched. In this mode, VIC will output the address of the memory location to be fetched. The address from VIC will be valid 50ns after the rising edge of P0<sub>1</sub> and remain valid until the rising edge of P0<sub>2</sub>.

### **Read/Write (R/W)**

This signal is an input only and controls the flow of data between VIC and the microprocessor. When the R/W signal is low and the VIC chip select conditions have been satisfied, the microprocessor can write data into the selected VIC Control Register. If the R/W signal is high and the chip select conditions have been met, the microprocessor can read data from the selected VIC Control Register.

It is important to note that all VIC/microprocessor data transfers can only occur when P0<sub>2</sub> = 1. During P0<sub>1</sub>, the VIC will be fetching data from memory for display and the R/W signal must be held high to insure that VIC will not write into any memory location.

### **Data Bus (DB<sub>0</sub>-DB<sub>11</sub>)**

The 12-bit data bus, DB<sub>0</sub> - DB<sub>11</sub>, is divided into two sections. The low-order eight bits, DB<sub>0</sub> thru DB<sub>7</sub>, are used both to interface to the microprocessor and to fetch data needed for display, while the high-order four bits are used exclusively for retrieving color and mode information. The operation of the low-order eight bits (DB<sub>0</sub> thru DB<sub>7</sub>) can also be separated into two categories: microprocessor interface and video data interface. During P0<sub>2</sub> = 1, DB<sub>7</sub> thru DB<sub>0</sub> are used exclusively for data transmission between the microprocessor and VIC. During P0<sub>1</sub> = 1, DB<sub>7</sub> thru DB<sub>0</sub> are used for fetching display data.

## CLOCKS

**Master Oscillator Clock Inputs—(Φ1 and Φ2).** The 6560 requires a 14.31818 MHz (NTSC), Two-Phase Clock. The clock signals must be +5V and non-overlapping. The 6561 requires a 4.436187 MHz clock for PAL standard.

**System Clocks—(P0<sub>1</sub> and P0<sub>2</sub>).** These clocks are the master timing generator for the VIC System. They are +5V, non-overlapping 1.02 MHz clocks capable of driving the capacitance of the 6512 microprocessor.

**Memory Clock—(Optional, ΦM).** This is a single-phase, 2.04 MHz clock used when memories in the VIC System require a strobe after the address bus is valid. It is one of the options available on Pin 37.

### **Analog to Digital Converters (POTX and POTY).**

These input pins are used to convert potentiometer position into a microprocessor-readable 8-bit hex number. This is accomplished by a simple RC time constant integration technique. The potentiometer is used to charge an external capacitor tied to the pot pin.

### **Composite Sound (COMP SND).**

This pin provides the output of the sound synthesizer portion of the 6560 shown in the VIC Block Diagram. It is a high-impedance output (approximately 1KΩ) and must be buffered and amplified externally to drive a speaker.

### **Composite Sync and Luminance (SYNC & LUMIN).**

This pin is an open-drain output which provides all necessary video synchronization and luminance information required by a standard television.

### **Composite Color (COMP COLOR).**

This signal provides the necessary color information required by a standard television to receive a full-color picture. The composite color pin is a high-impedance output buffer which provides the reference burst signal plus the color-encoded phase and amplitude information at the proper 3.579545 MHz frequency.

### **Reset**

This optional Pin 37 input signal is used to synchronize the horizontal and vertical sync counter to an external signal.

### **Bus Available**

This optional Pin 37 output signal indicates the state of the VIC with respect to the video memory fetch. The pin will go low 2 μsec before VIC performs any memory access and will remain low until the entire screen has been refreshed.

### **Light Gun/Pen**

The optional Pin 37 input signal causes the current dot position being scanned onto the screen to be latched onto control registers 6 and 7, upon a negative-going edge. This pin would be used in conjunction with a photo detector for use in a "target shoot" type game or for light pen applications.

**AVAILABLE AUXILIARY/BACKGROUND COLORS**

- 0 BLACK**
- 1 WHITE**
- 2 RED**
- 3 CYAN**
- 4 MAGENTA**
- 5 GREEN**
- 6 BLUE**
- 7 YELLOW**
  
- 8 ORANGE**
- 9 LIGHT ORANGE**
- A PINK**
- B LIGHT CYAN**
- C LIGHT MAGENTA**
- D LIGHT GREEN**
- E LIGHT BLUE**
- F LIGHT YELLOW**

**AVAILABLE BORDER/CHARACTER COLORS**

- 0 BLACK**
- 1 WHITE**
- 2 RED**
- 3 CYAN**
- 4 MAGENTA**
- 5 GREEN**
- 6 BLUE**
- 7 YELLOW**

**THEORY OF OPERATION**

To produce programmable color characters, VIC accesses external memory which can be divided into three areas: character pointers, display characters and color pointers. The character pointer area is a block of bytes in RAM (typically 506 bytes called the Video Matrix) in which each byte points to a particular character to be displayed. The character area consists of a set of 8 or 16 byte blocks (usually called cells) which contain the actual dot patterns to be displayed. These character cells can be located in either RAM or ROM, depending on how the objects are to

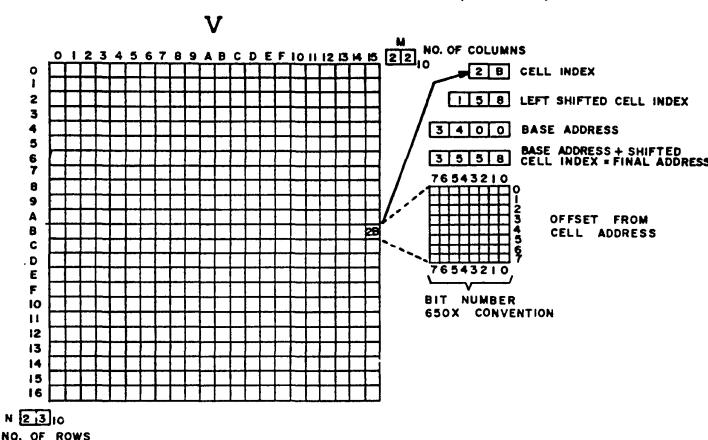
be displayed or moved on the screen. The color pointer area is a block of nibbles in RAM (typically 506 four-bit nibbles called the Color Matrix). The four-bit color pointers are used to define the color of any character to be displayed and to select one of the two color modes.

It is the task of an external microprocessor to organize the Video Matrix, Color Matrix and Character Cells into the proper format to display the data desired on-screen.

To understand the operation of VIC more completely, refer to Figure 1. This is a typical Video Matrix, in which 22 characters horizontally by 23 characters vertically are to be displayed, yielding a total of 506 character display locations, with a screen resolution of 176 horizontal by 184 vertical dots. Each one of these character display locations has a corresponding character pointer, or index, which specifies (points at) a character to be displayed in a particular location.

In the example shown, rectangle (B, 15) has a character index of 2B. This means character number 2B is to be displayed in that rectangle. VIC will fetch the character index value 2B and perform an address computation to locate the character to be displayed. The computation is quite simple. If 8 x 8 character cells are selected, the index is left shifted 3 times (multiply by 8) and the starting address of the character cells, found in VIC Control Register CR5, is added to the left-shifted value. In this case, the character cell starting address is 3400H which is added to the left-shifted value of the character index to yield the actual character location in memory of 3558H.

The number of times that any particular character can be displayed is unlimited. By using the same character index (2B for example) elsewhere on the grid, the character data will be displayed again. Alternately, through the use of a simple software driver, VIC can be used as a bit-mapped display system provided enough RAM (approximately 4K bytes of cell RAM) is available.

**TYPICAL VIDEO MATRIX (23 x 22)****Figure 1**

**1000** ORIGIN

### VIC CONTROL REGISTERS

		7	6	5	4	3	2	1	0	(bit number)
CR <sub>0</sub>	1000	I	S <sub>X</sub> <sup>6</sup>	S <sub>X</sub> <sup>5</sup>	S <sub>X</sub> <sup>4</sup>	S <sub>X</sub> <sup>3</sup>	S <sub>X</sub> <sup>2</sup>	S <sub>X</sub> <sup>1</sup>	S <sub>X</sub> <sup>0</sup>	Screen Origin X-Coordinate
CR <sub>1</sub>	1001	S <sub>Y</sub> <sup>7</sup>	S <sub>Y</sub> <sup>6</sup>	S <sub>Y</sub> <sup>5</sup>	S <sub>Y</sub> <sup>4</sup>	S <sub>Y</sub> <sup>3</sup>	S <sub>Y</sub> <sup>2</sup>	S <sub>Y</sub> <sup>1</sup>	S <sub>Y</sub> <sup>0</sup>	Screen Origin Y-Coordinate
CR <sub>2</sub>	1002	B <sub>V</sub> <sup>9</sup>	M <sub>6</sub>	M <sub>5</sub>	M <sub>4</sub>	M <sub>3</sub>	M <sub>2</sub>	M <sub>1</sub>	M <sub>0</sub>	No. of Video Matrix Columns
CR <sub>3</sub>	1003	R <sub>0</sub>	N <sub>5</sub>	N <sub>4</sub>	N <sub>3</sub>	N <sub>2</sub>	N <sub>1</sub>	N <sub>0</sub>	D	No. of Video Matrix Rows
CR <sub>4</sub>	1004	R <sub>8</sub>	R <sub>7</sub>	R <sub>6</sub>	R <sub>5</sub>	R <sub>4</sub>	R <sub>3</sub>	R <sub>2</sub>	R <sub>1</sub>	Raster Value
CR <sub>5</sub>	1005	B <sub>V</sub> <sup>13</sup>	B <sub>V</sub> <sup>12</sup>	B <sub>V</sub> <sup>11</sup>	B <sub>V</sub> <sup>10</sup>	B <sub>C</sub> <sup>13</sup>	B <sub>C</sub> <sup>12</sup>	B <sub>C</sub> <sup>11</sup>	B <sub>C</sub> <sup>10</sup>	Base Address Control
CR <sub>6</sub>	1006	L <sub>H</sub> <sup>7</sup>	L <sub>H</sub> <sup>6</sup>	L <sub>H</sub> <sup>5</sup>	L <sub>H</sub> <sup>4</sup>	L <sub>H</sub> <sup>3</sup>	L <sub>H</sub> <sup>2</sup>	L <sub>H</sub> <sup>1</sup>	L <sub>H</sub> <sup>0</sup>	Light Pen Horizontal
CR <sub>7</sub>	1007	L <sub>V</sub> <sup>7</sup>	L <sub>V</sub> <sup>6</sup>	L <sub>V</sub> <sup>5</sup>	L <sub>V</sub> <sup>4</sup>	L <sub>V</sub> <sup>3</sup>	L <sub>V</sub> <sup>2</sup>	L <sub>V</sub> <sup>1</sup>	L <sub>V</sub> <sup>0</sup>	Light Pen Vertical
CR <sub>8</sub>	1008	P <sub>X</sub> <sup>7</sup>	P <sub>X</sub> <sup>6</sup>	P <sub>X</sub> <sup>5</sup>	P <sub>X</sub> <sup>4</sup>	P <sub>X</sub> <sup>3</sup>	P <sub>X</sub> <sup>2</sup>	P <sub>X</sub> <sup>1</sup>	P <sub>X</sub> <sup>0</sup>	Pot X
CR <sub>9</sub>	1009	P <sub>Y</sub> <sup>7</sup>	P <sub>Y</sub> <sup>6</sup>	P <sub>Y</sub> <sup>5</sup>	P <sub>Y</sub> <sup>4</sup>	P <sub>Y</sub> <sup>3</sup>	P <sub>Y</sub> <sup>2</sup>	P <sub>Y</sub> <sup>1</sup>	P <sub>Y</sub> <sup>0</sup>	Pot Y
CR <sub>A</sub>	100A	S <sub>1</sub>	F <sub>1</sub> <sup>6</sup>	F <sub>1</sub> <sup>5</sup>	F <sub>1</sub> <sup>4</sup>	F <sub>1</sub> <sup>3</sup>	F <sub>1</sub> <sup>2</sup>	F <sub>1</sub> <sup>1</sup>	F <sub>1</sub> <sup>0</sup>	F <sub>IN</sub> <sup>(1)</sup>
CR <sub>B</sub>	100B	S <sub>2</sub>	F <sub>2</sub> <sup>6</sup>	F <sub>2</sub> <sup>5</sup>	F <sub>2</sub> <sup>4</sup>	F <sub>2</sub> <sup>3</sup>	F <sub>2</sub> <sup>2</sup>	F <sub>2</sub> <sup>1</sup>	F <sub>2</sub> <sup>0</sup>	F <sub>IN</sub> <sup>(2)</sup>
CR <sub>C</sub>	100C	S <sub>3</sub>	F <sub>3</sub> <sup>6</sup>	F <sub>3</sub> <sup>5</sup>	F <sub>3</sub> <sup>4</sup>	F <sub>3</sub> <sup>3</sup>	F <sub>3</sub> <sup>2</sup>	F <sub>3</sub> <sup>1</sup>	F <sub>3</sub> <sup>0</sup>	F <sub>IN</sub> <sup>(3)</sup>
CR <sub>D</sub>	100D	S <sub>4</sub>	F <sub>4</sub> <sup>6</sup>	F <sub>4</sub> <sup>5</sup>	F <sub>4</sub> <sup>4</sup>	F <sub>4</sub> <sup>3</sup>	F <sub>4</sub> <sup>2</sup>	F <sub>4</sub> <sup>1</sup>	F <sub>4</sub> <sup>0</sup>	F <sub>IN</sub> <sup>(4)</sup>
CR <sub>E</sub>	100E	C <sub>A</sub> <sup>3</sup>	C <sub>A</sub> <sup>2</sup>	C <sub>A</sub> <sup>1</sup>	C <sub>A</sub> <sup>0</sup>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Amplitude
CR <sub>F</sub>	100F	C <sub>B</sub> <sup>3</sup>	C <sub>B</sub> <sup>2</sup>	C <sub>B</sub> <sup>1</sup>	C <sub>B</sub> <sup>0</sup>	R	C <sub>E</sub> <sup>2</sup>	C <sub>E</sub> <sup>1</sup>	C <sub>E</sub> <sup>0</sup>	Color Control

**Note**

N. U. = NOT USED.

Figure 2

#### REGISTER DESCRIPTION

There are 16 eight-bit control registers within the 6560 which enable the microprocessor to control all operating modes of VIC. The control registers and their functions are tabulated and explained below, while a diagram of the register locations and contents are shown in Figure 2.

#### CR0

Bits 0-6 determine how far from the left-hand side of the T.V. screen the first column of characters will appear. It is used to horizontally center various sizes of video matrices on-screen. Bit 7 selects interlaced scan mode (I = 1).

#### CR1

Determines how far from the top of the T.V. screen the

first row of characters will appear. It is used to vertically center various sizes of video matrices on-screen.

#### CR2

Bits 0-6 set the number of columns in the Video Matrix. Bit 7 is part of the Video Matrix address found in CR5.

#### CR3

Bits 1-6 set the number of rows in the Video Matrix. Bit 0 is used to select either 8 x 8 character matrices (D = 0) or 16 x 8 character matrices (D = 1). Bit 7 is part of the raster value found in CR4.

#### CR4

Contains the number of the line currently being scanned by the T.V. raster beam.

**CR5**

Bits 0-3 determine the starting address of the character cell space. (Note that these bits form bits A13 through A10 of the actual address.) Bit 4-7 (along with Bit 7 of CR2) determine the starting address of the Video Matrix (these bits form bits A13 through A9 of the actual address).

**CR6**

Contains the latched horizontal position of the light gun/pen.

**CR7**

Contains the latched vertical position of the light gun/pen.

**CR8**

Contains the digitized value of POTX.

**CR9**

Contains the digitized value of POTY.

**CRA**

Bits 0-6 set the frequency of the first audio oscillator. Bit 7 turns the oscillator on (= 1) or off (= 0).

**CRB**

Same as CRA for second audio oscillator.

**CRC**

Same as CRA for third audio oscillator.

**CRD**

Same as CRA but sets frequency of noise source.

**CRE**

Bits 0-3 set the volume of the composite audio signal (Note that at least one sound generator must be turned on for any sound to be produced). Bits 4-7 contain the Auxiliary color code used in conjunction with the "Multicolor" mode of operation.

**CRF**

Bits 4-7 select one of 16 colors for the background common to all characters. (Essentially, they set the color of the background area within the Video Matrix.) Bits 0-2 select 1 of 8 colors for the exterior border area of the screen (all area outside the Video Matrix). Bit 3 determines whether

the Video Matrix will be displayed as different colored characters on a common background color ( $R = 1$ ) or inverted ( $R = 0$ ), that is, all characters will be the same color (the background color in  $CR_F$ ) while each character's background will now be a different color, determined by the code in the Color RAM. Note that the R bit has no effect when Multicolor mode is selected and the CRF also functions differently in this mode. Refer to the section called "Operating Modes" for complete information.

**COLOR OPERATING MODES**

VIC incorporates two modes of color operation – HI-RES (high resolution) mode and Multicolor mode. Basically, the operating mode affects how the Character Cell information will be translated into dots on the T.V. screen. The operating mode is determined by the MSB of the color pointer associated with each character location in the Video Matrix. If the MSB of a character's color pointer is zero, that character will be displayed in HI-RES mode. Alternately, if the MSB is one, the character will be displayed in the Multicolor mode.

With HI-RES mode selected, there is a one-to-one correspondence between Character Cell bits and the dots displayed on-screen. That is, all one bits of a character will be displayed in one color, and all zero bits in another color. The foreground color of the character is specified by the remaining 3 bits of the character's color pointer, while the character's background color is specified by Control Register F.

With Multicolor mode selected, each two bits of a character cell correspond to one dot on-screen and the color of that dot is determined by the two-bit code. Unlike HI-RES mode, in which only two colors can be displayed in a single character, Multicolor mode allows four colors per character; however, since two bits of cell data now correspond to a single dot on-screen, the horizontal resolution is half that of the HI-RES mode. That is, each 8x8 Character Cell in memory maps onto an 8x4 character on-screen (8 lines of 4 dots each). Note that the amount of memory required for these 8x4 Multicolor characters is the same as that for 8x8 HI-RES characters; the data is simply mapped differently on-screen.

In Multicolor mode, the two bits which make up a dot select one of four colors for that dot. The four codes created by these two bits tell VIC where to find the color information for the dot. The color of the dot can be either the Background color (in CRF), the Exterior Border color in (CRF), the Auxiliary color (in CRE) or the Foreground color (bits 0 thru 2 of the character's color pointer).

The Multicolor mode color select codes are:

- 00—Background color (CR<sub>F</sub>)
- 01—Exterior Border color (CR<sub>F</sub>)
- 10—Foreground color (Color RAM)
- 11—Auxiliary color (CR<sub>E</sub>)

Note that the two-bit code is not itself a color code; rather it is a pointer to four different color codes, allowing greater color flexibility, as each code pointed to has either 3 or 4-bit resolution.

#### Example:

Given:

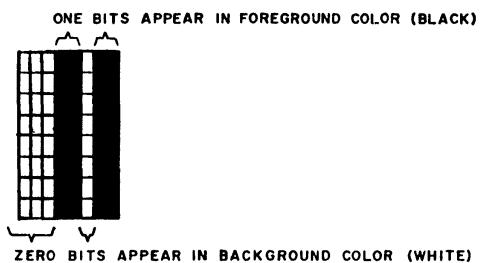
CR<sub>F</sub> = 1F      Character Background color is WHITE (1),  
Exterior Border color is YELLOW (7),  
Invert is not selected (R = 1).

CR<sub>E</sub> = 6X      Auxiliary color is BLUE (6).

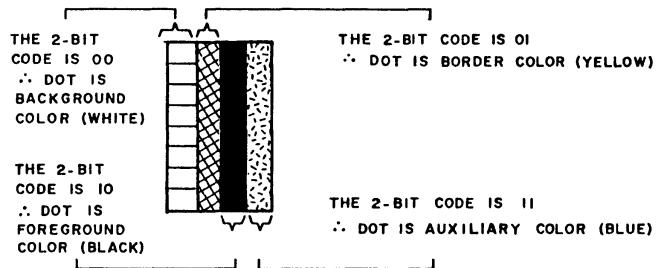
and a character definition of:

	bit	HEX
byte	76543210	
	0 00011011	1B
	1 00011011	1B
	2 00011011	1B
	3 00011011	1B
	4 00011011	1B
	5 00011011	1B
	6 00011011	1B
	7 00011011	1B

If the color pointer nibble for that character is 0 (0000), then the Foreground color is BLACK (0) and HI-RES modes is selected (MSB = 0). The character will then appear on-screen as:



If the color pointed nybble for that character is 8 (1000), then the Foreground color is BLACK (0) and the Multicolor mode is selected (MSB = 1). The character will then appear on-screen as:

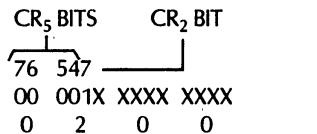
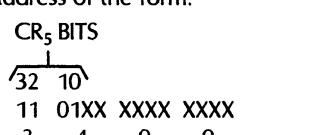


(Note that this is given solely as an example and due to color transition limitations of most TV sets, closely spaced dots of different colors will not appear sharply defined on-screen.)

Since the mode of display for a character is selected by the character's color pointer and each character location on-screen has a unique color pointer, it is possible to freely intermix HI-RES and Multicolor characters. This provides great display flexibility, allowing HI-RES characters for alphanumerics, etc. and Multicolor characters for a wider array of colors available simultaneously.

**EXAMPLE OF VIC CONTROL REGISTER USE:**

For simplicity, assume all characters are in the HI-RES mode and the VIC Registers are loaded with the following values:

Reg	Contents (HEX)	Binary	Results
CR0	03	0/000 0011	Moves Video Matrix over 3(x4) dot widths from the left side of the screen. Interlace is not selected (I = 0).
CR1	19	0001 1001	Moves Video Matrix down HEX 19 (x2) dot heights from top of screen.
CR2	96	1/001 0110	Sets HEX 16 (=22 base 10) columns in Video Matrix. (Bit 7 is used with CR <sub>5</sub> .)
CR3	2E	X/010 111/0	Sets 010111 (=23 base 10) rows in Video Matrix. 8 x 8 character matrices are selected (D = 0).
CR5	Should be set to access the proper memory locations of the specific system. Suppose it is desired to locate the Video Matrix starting at address HEX 0200, and the character matrices starting at address HEX 3400. In order to accomplish this, CR <sub>5</sub> is set:		
CR5	0D	0000 1101	and bit 7 of CR <sub>2</sub> is set to 1.
	This would create a 14-bit address of the form:  for the Video Matrix. It would also create a 14-bit address of the form:  for the character matrices.		
CRA	00	0/000 0000	Oscillator 1 is OFF.
CRB	9A	1/001 1010	Oscillator 2 is ON, with a relative frequency of 1A.
CRC	00	0/000 0000	Oscillator 3 is OFF.
CRD	A5	1/010 0101	Noise generator is ON with a relative frequency of 25.
CRE	XF	XXXX 1111	Sound effects are set for loudest volume.
CRF	OE	0000/1/110	The background color common to all characters is black (0), the border color is dark blue (6) and each character is displayed in its own color on the black background (R = 1).

These register values will produce a screen with a properly centered Video Matrix of 23x22 characters, each character appearing in color on a black background, with a dark blue border surrounding the Video Matrix area. Additionally, the sound effects generator will be producing a pitched oscillation, along with white noise.

All of these registers can be modified to produce different effects.

For example:

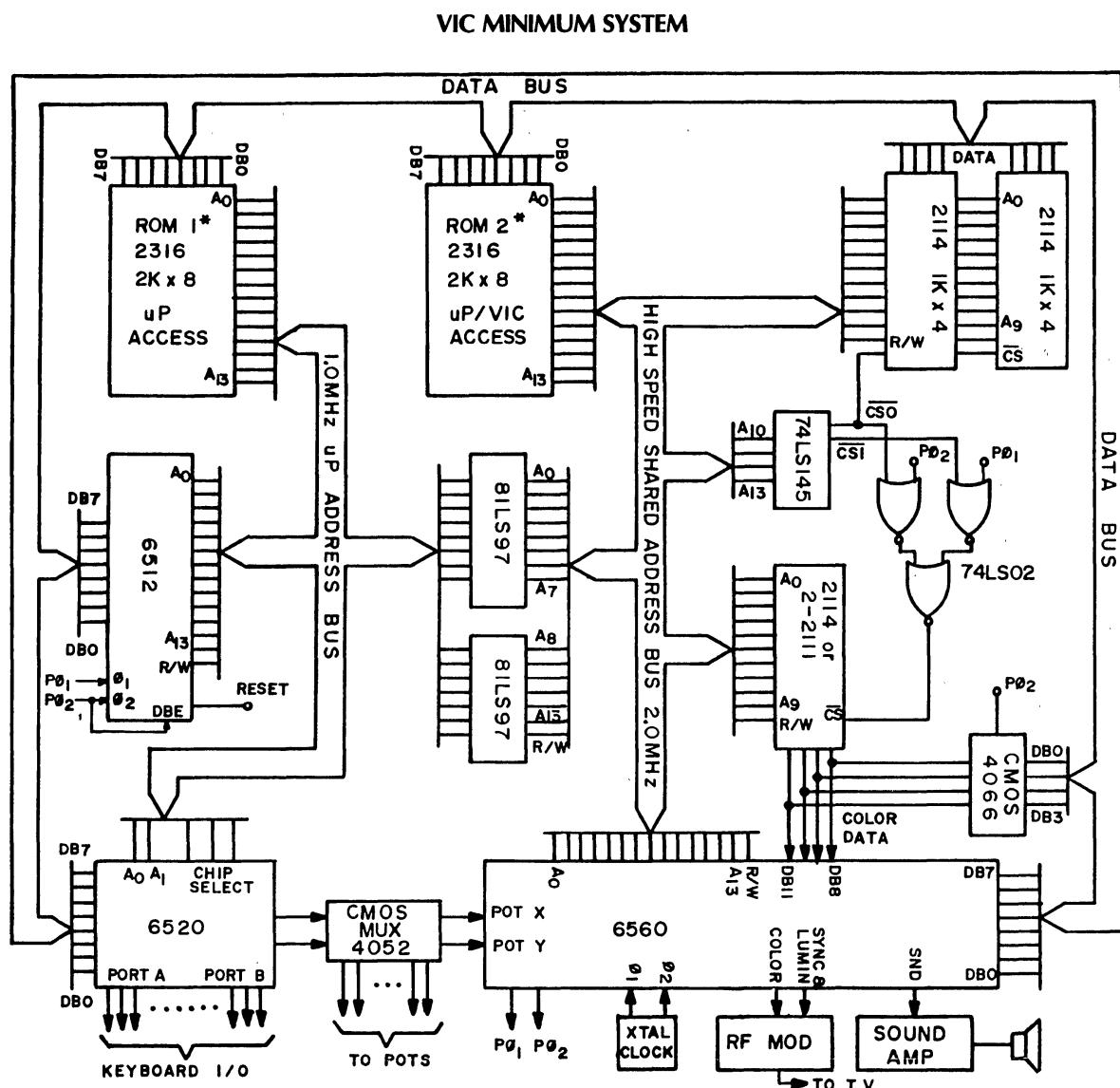
If the number in CR0 is increased, the Video Matrix region will shift farther to the right. If the number in CRB is reduced (leaving bit 7 a one) the frequency of oscillator 2 will go down.

If CRF is changed to 06 (turning R OFF), the border will remain dark blue, but now the Video Matrix will appear as black characters on different colored backgrounds.

For VIC to produce a picture on-screen, the number of rows and columns and appropriate centering values must be loaded into the proper registers.

## MINIMUM SYSTEM DESCRIPTION

A minimum VIC System would consist of a microprocessor, VIC, ROM, RAM and I/O. The basic system includes one  $\mu$ P (6512), one Video Interface Chip (VIC/6560), one PIA (6520), two 1K x 4 static RAMS, two 256 x 4 static RAMS, and one or more program/graphics ROMS (2K x 8 or 4K x 8). See Figure 3.



### \*NOTE

ROM 1 or ROM 2 is optional, since either can be cartridge loaded. ROM 1 is accessed by the processor only. ROM 2 can be accessed by the processor or VIC.

Figure 3

The tasks involved in a complete game are divided between the  $\mu$ P and VIC. The  $\mu$ P controls the game logic and VIC controls the video display as well as the sound generation.

#### 6512 Microprocessor

The 6512 is a member of the 6500 microprocessor family, which has gained wide acceptance in the video game industry. The 6512 architecture and addressing capability are well suited to graphic data manipulation. Alternately, a 6502 processor can be used by feeding VIC P02 OUT into the 6502 00 IN; however, tri-state buffers must then be added to the data bus as well as the address bus.

#### 6560 Video Interface Chip

The 6560 is a video display device which reads data that has been formatted by the  $\mu$ P and supplies the appropriate color graphic signals to the RF modulator. To accomplish this, the 6560 does a transparent DMA of the  $\mu$ P's memory space, accessing ROM and/or RAM.

#### 6520 Peripheral Interface Adapter

This chip is used for keyboard scanning and joystick multiplexing.

#### Resident RAM = 2 (2114) and (2111)

These RAM chips are used as working storage by the  $\mu$ P

and for holding the screen organization and color matrices. They may be modified by the  $\mu$ P at any time. Note that to achieve a full bit-map display, a minimum of 4K bytes of character RAM are necessary.

#### Program/Graphics ROM(s)

These chips normally contain the game logic and/or coded graphic data. There is no need for a resident ROM in a minimum system. A cartridge ROM can contain all the relevant information.

#### ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	-10° to 80°C
Storage Temperature	-65°C to 150°C
Voltage on any Pin*	-0.5V to +7V
Power Dissipation	1.0W

#### NOTE

\*With respect to Ground

#### COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**DC CHARACTERISTICS**  $T_A = 0^\circ\text{C}$  to  $+50^\circ\text{C}$ ,  $V_{DD} = 5\text{V} \pm 5\%$  (unless otherwise specified)

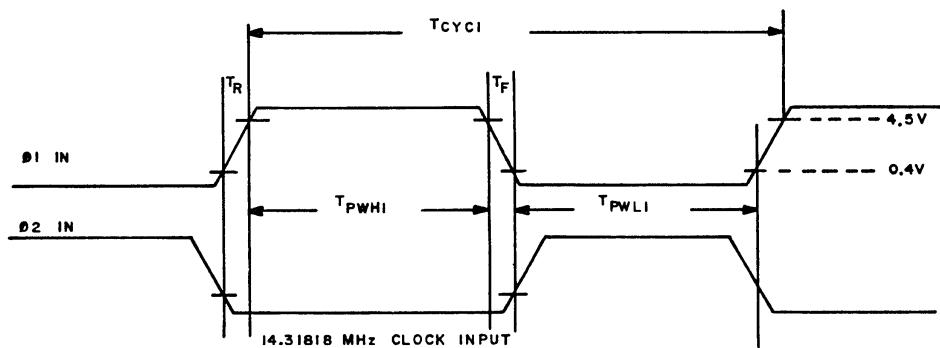
Parameter	Min	Max	Typ	Units
<b>Read/Write, Reset (Option)</b>				
Address and Data-Input State				
$V_{IL}$	-0.2	0.4		Volts
$V_{IH}$	2.4	5.6		Volts
Input Capacitance		8.0	5.0	pF
Input Leakage (all outputs in high impedance state)		10.0	1.0	$\mu\text{A}$
<b>Address and Data-Output State</b>				
$V_{OL}$		0.4		Volts
$V_{OH}$	2.4			Volts
$I_{OL}$ – Sink current $V_{OL} = 0.4$	2.4			mA
$I_{OH}$ – Source current $V_{OH} = 2.4$	200			$\mu\text{A}$
Impedance in Three State Condition		$1 \times 10^6$		Ohms
<b>Clock Input (<math>\phi_1</math> and <math>\phi_2</math> Input)</b>				
Frequency			14.31818	MHz
Capacitance				pF
$V_{IL}$	-0.2	10.0		Volts
$V_{IH}$	4.5	0.3	5.0	Volts
<b>Clock Outputs (<math>P\phi_1</math>, <math>P\phi_2</math>)</b>				
$V_{OL}$		0.3V		Volts
$I_{OL}$ @ 0.3 Volts $V_{OL}$	1.6			mA
$V_{OH}$				Volts
$I_{OH}$ @ 4.7 Volts $V_{OH}$	$V_{DD} - .2$			$\mu\text{A}$
Loading	200			pF
Frequency		120.0	1.02	MHz

# 6560/6561

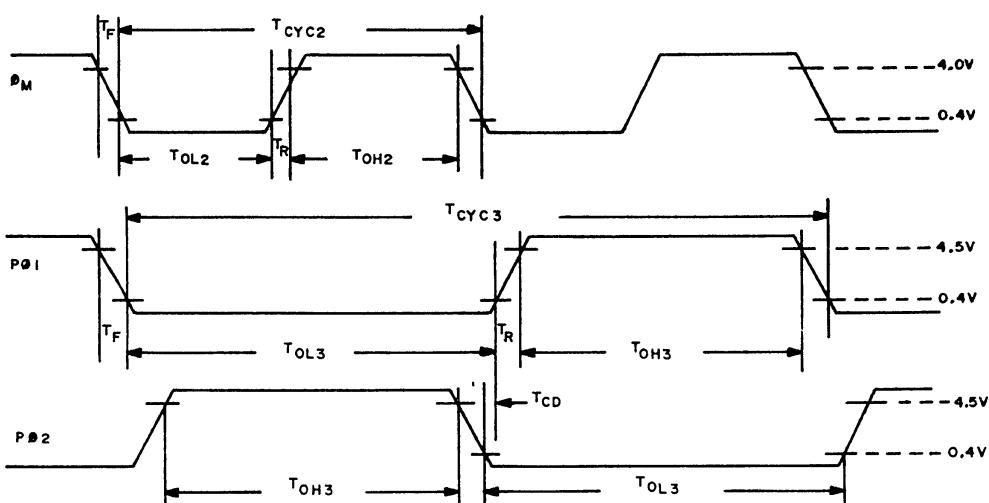
**DC CHARACTERISTICS**  $T_A = 0^\circ\text{C}$  to  $+50^\circ\text{C}$ ,  $V_{DD} = 5\text{V} \pm 5\%$  (unless otherwise specified)

Parameter	Min	Max	Typ	Units
<b>Composite Sound</b>				
Output Impedance		2000	1000	$\Omega$
Max. Current (Sink or Source)		500		$\mu\text{A}$
Output Offset Voltage	2.2	2.8	2.5	Volts
$V_{OH}$ (Max. Amplitude)	3.2		3.5	Volts
$V_{OL}$ (Max. Amplitude)		1.8	1.5	Volts
$V_{OH}$ (Min. Amplitude)	2.55		2.6	Volts
$V_{OL}$ (Min. Amplitude)		2.45	2.4	Volts
<b>Pot Inputs</b>				
$V_{TRIGGER}$ (Rising Edge)	2.2	2.8	2.5	Volts
<b>Pot Reset</b>				
$V_{OL}$		0.2		Volts
$I_{OL} @ V_{OL} = 0.2$	500			$\mu\text{A}$
<b>Light Pen Input (Option)</b>				
$V_{TRIGGER}$ (Falling Edge)	2.8	2.2	2.5	Volts
<b><math>\phi_M</math> (Option)</b>				
$V_{OL}$		0.4		Volts
$I_{OL} @ 0.3 \text{ Volts } V_{OL}$	1.6			$\text{mA}$
$V_{OH}$	$V_{DD} - .7$			Volts
$I_{OH} @ 4.7 \text{ Volts } V_{OH}$	100			$\mu\text{A}$
Loading		60		$\text{pF}$
Frequency			2.04	$\text{MHz}$
<b>Bus Available (Option)</b>				
$V_{OL}$		0.3		Volts
$I_{OL}$	1.6			$\text{mA}$
$V_{OH}$	2.4			Volts
$I_{OH}$	100			$\mu\text{A}$
$V_{DD}$	4.75	5.25	5.00	Volts
$I_{DD}$	150	120		$\text{mA}$

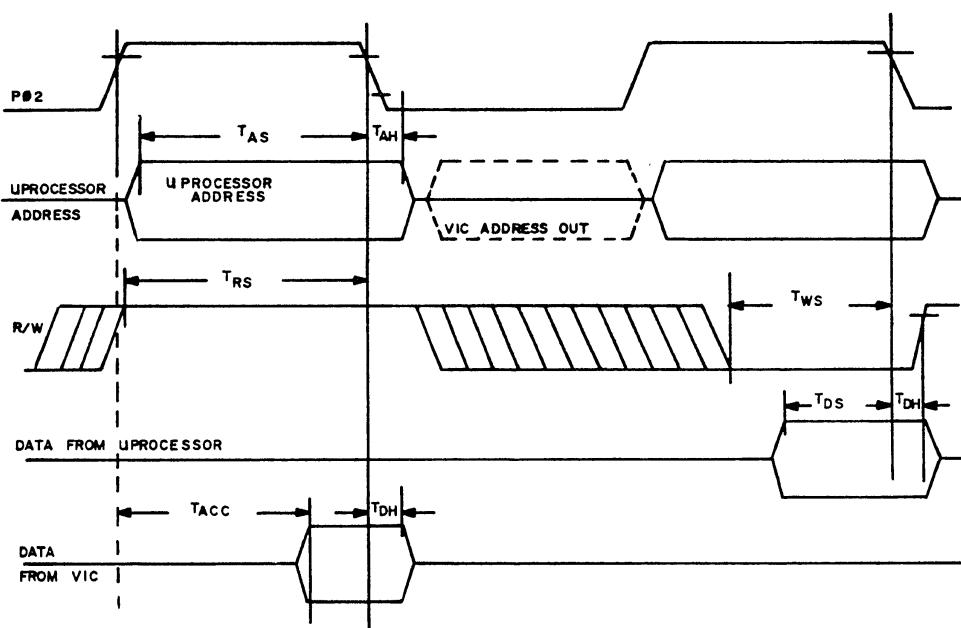
## VIC INPUT CLOCKS



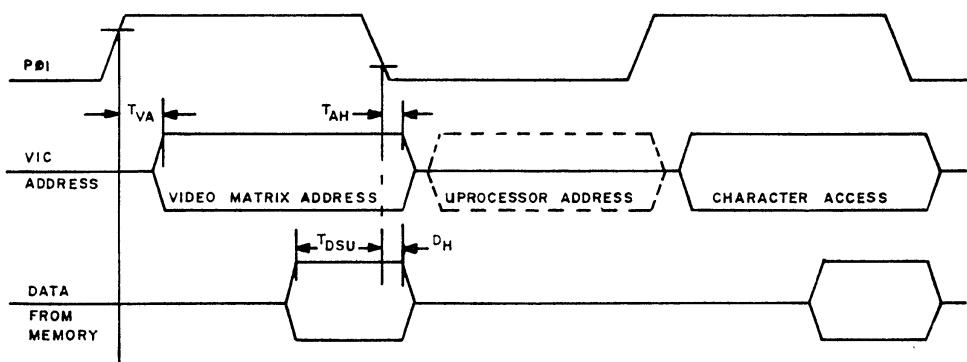
**VIC OUTPUT CLOCKS**



**MICROPROCESSOR READ/WRITE TIMING TO VIC**



**VIC READ TIMING FROM MEMORY**



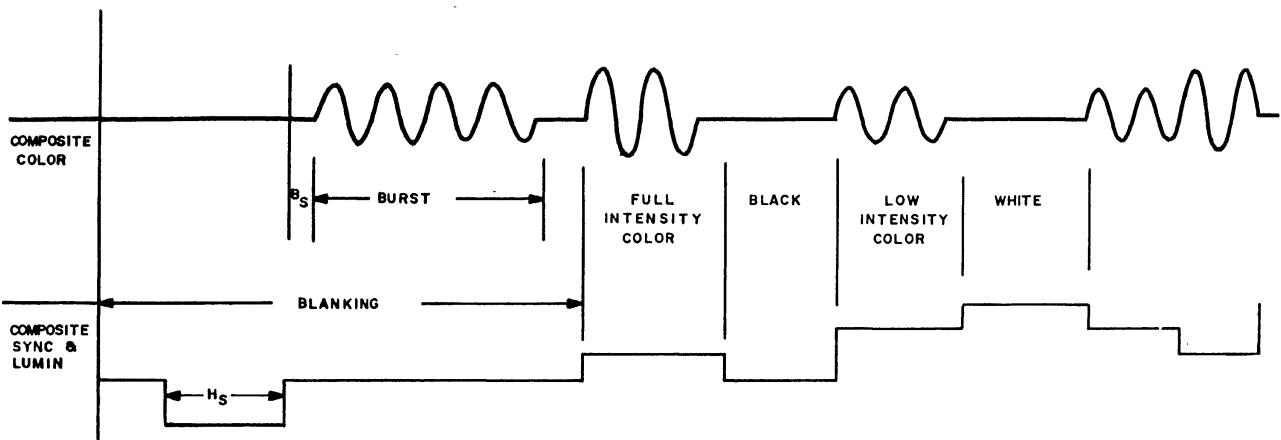
**VIC SYSTEM TIMING**

Symbol	Characteristic	Min	Typ	Max	Units
T <sub>CYC1</sub> T <sub>PWH1</sub> T <sub>PWL1</sub> T <sub>R</sub> , T <sub>F</sub>	<b>VIC Input Clock Timing</b> Input Clock Cycle Time Clock High Clock Low Rise and Fall Time	69.82 20 20		69.84 10	ns ns ns ns
T <sub>CYC2</sub> T <sub>OL2</sub> T <sub>OH2</sub> T <sub>CYC3</sub> T <sub>OL3</sub> T <sub>OH3</sub> T <sub>CD</sub> T <sub>R</sub> T <sub>F</sub>	<b>VIC Output Clock Timing</b> Two MHz Clock Cycle Time $\phi_M$ Clock Output Low $\phi_M$ Clock Output High 1MHz $\mu$ Processor Clocks Cycle Time $P\phi_1$ , $P\phi_2$ Clocks Low $P\phi_1$ , $P\phi_2$ Clocks High Delay Time Between Clocks At .4v Rise Time, Max. C <sub>L</sub> Fall Time, Max. C <sub>L</sub>	480 200 180 960 380 380 5		500 260 250 990 500 500 20 80 40	ns ns ns ns ns ns ns ns ns
T <sub>AS</sub> T <sub>AH</sub> T <sub>RS</sub> T <sub>WS</sub> T <sub>DS</sub> T <sub>ACC</sub> T <sub>DH</sub>	<b>Microprocessor Read/Write Timing to VIC</b> Address Set Up Time Address Hold Time Read Set Up Time Write Set Up Time Data Set Up Time Data Access Time Data Hold Time	375 5 375 275 200 350 30			ns ns ns ns ns ns ns
T <sub>VA</sub> T <sub>AH</sub> T <sub>DSS</sub> D <sub>H</sub>	<b>VIC Read Timing From Memory</b> Time To Valid Address From P $\phi_1$ Address Hold Time Data Set Up Time Data Hold Time	10 60 20			ns ns ns ns
BLANKING B <sub>S</sub> BURST	<b>Composite Sync, Color And Luminance Timing</b> Blanking Period (No Video) Breeze Way Color Burst Reference Signal	10.0 .3 4.0	11.0 .5 5.0	12.0 .7 6.0	$\mu$ s $\mu$ s $\mu$ s
H <sub>S</sub> H <sub>L</sub> H <sub>L/2</sub> E E <sub>L</sub> V <sub>S</sub> V <sub>S</sub> to V <sub>S</sub>	<b>Composite SYNC Output Timing</b> Horizontal Sync Pulse Horizontal Line Period One Half Horizontal Line Period Equalization Pulse Equalization Time Period Vertical Sync Period Vertical Sync to Vertical Sync Time Period	4.0 63.0 30.0 2.0 188.0 188.0	5.0 63.5 31.5 2.5 190.5 190.5	6.0 64.0 32.5 3.0 192.0 192.0	$\mu$ s $\mu$ s $\mu$ s $\mu$ s $\mu$ s ms

**Notes**

1. The color burst signal is the 3.579545 MHz color phase reference from which all other color information is measured.  
For Example: Full intensity blue is a 3.579545 MHz signal which has a relative delay of 135ns from burst if the burst signal was available throughout the entire H<sub>L</sub> period.
2. The number of H<sub>L</sub> periods between V<sub>S</sub> periods is 262.5 in the interlace mode.
3. The number of H<sub>L</sub> periods between V<sub>S</sub> periods in the non-interlace mode is 262 per frame.
4. NTSC only.

**Composite SYNC, Color and Luminance**



**Composite SYNC Output**

