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AN-002: Replacement Notes for Obsolete Versions of 6502 8-bit Microprocessors

APPLE-1 Replacement Notes (Not Validated at WDC)
For those with an Apple-1, WDC recommends the following modifications when replacing the MOS 6502 with a W65C02S6T MPU:

- 1.) VPB (Pin 1) - Carefully bend this pin outward before placing the chip in the socket.
- 2.) MLB (Pin 5) - Carefully bend this pin outward before placing the chip in the socket. The Apple-1 had pin 5 as VMA as part of the 6800 support. The 6502/W65C02 always has Valid Memory Addressing. The Apple-1 has a jumper that should be in place when using the 6502/W65C02S.
- 3.) BE (Pin 36) - Tie this pin to VDD (Pin 8).
- 4.) The Apple-1 has a 3K resistor pulling RDY (Pin 2) high. WDC does not recommend using the SToP or WAIt instruction on the Apple-1.

APPLE IIe Replacment Notes (Validated at WDC):
For those with an Apple IIe, WDC recommends the following modification when replacing the 65C02 with a W65C02S6T MPU:

- 1.) VPB (Pin 1) - Carefully bend this pin outward before placing the chip in the socket.
- 2.) BE can be tied directly to VDD (Pin 8), which has been validated WDC.
- 3.) The Apple IIe has a 1K resistor pulling RDY (Pin 2) high. WDC does not recommend using the SToP or WAIt instruction on the Apple-1.

Comparison of 6502, W65C02S, R65C02, R65102, R65C112 and G65SC02

The 6502, R6502, and G65SC02 all use the exact same instruction set. The W65C02S and R65C02 use the same set of instructions except the W65C02S has WAI and STP. The WAI instruction was added for improved interrupt response time and low power. The STP instruction can help to conserve power in current designs.

The W65C02S8PL (44 pin PLCC) has the same additional pin functions as the DIP version. In addition, pin numbers have changed, i.e. W65C02S (PLCC) pin 9 is VDD, pin 9 on the other PLCC parts in a NC. This package is not pin compatible since almost all pin numbers have changed.

The following parts are pin compatible in a 40 pin DIP package.

- W65C02S (WDC)
- R65C02, R6502 (Rockwell)
- G65SC02 (GTE)

The W65C02S (40 pin DIP) pin differences are as follows:

PIN COMPARISON CHART

Pin	W65C02S	6502	R65C02	R65C102	R65C112	G65SC02
1	VPB *	VSS	VSS	VSS	VSS	VSS
2	RDY **	RDY	RDY	RDY	RDY	RDY
3	PHI1O	Ø1(OUT)	Ø1(OUT)	Ø4(OUT)	NC	Ø1(OUT)
5	MLB ***	NC	NC	MLB	MLB	NC
35	NC	NC	NC	XTLO	NC	NC
36	BE ****	NC	NC	BE	BE	NC
37	PHI2	Ø2(IN)	Ø0(IN)	XTLI	Ø2(IN)	Ø0(IN)
39	PHI2O	Ø2(OUT)	Ø2(OUT)	Ø2(OUT)	NC	Ø2(OUT)

* VPB is Vector Pull (output) pin goes low when an interrupt vector is on the address bus.

** RDY is a bidirectional pin on the W65C02S. Early W65C02S version has a low impedance pull up resistor. The latest W65C02S6T devices (wafers manufactured at TSMC) no longer have the internal pull-up on the RDY pin (pin 2 PDIP, pin 3 PLCC, pin 41 QFP). When not driving RDY, WDC recommends having a pull up resistor (3.3K Ohm) to VDD on this pin. When driving RDY, WDC recommends have a current limiting resistor (3.3K Ohm) in series with the RDY pin.

*** MLB is Memory Lock (output) pin goes low during specific cycles of a read-modify-write instruction to indicate when memory should not be accessed.

**** BE is Bus Enable (input). When Bus Enable goes low this forces the Address Bus, Data Bus and RWB to a high impedance state. BE should be tied directly to VDD (Pin 8).

IN SUMMARY: The W65C02S6T (40 pin PDIP) is mostly pin compatible by making the following modifications:

- 1.) Cut the trace to VPB (Pin 1). Optionally you can pull this pin up.
- 2.) BE (Pin 36) should be tied directly to VDD (Pin 8).
- 3.) Add a 3.3K Ohm pull-up resistor on RDY (Pin 2) if not being driven; Add a 3.3K Ohm series current limiting resistor to RDY (Pin 2) if being driven.
- 4.) WDC does not recommend using the SToP or WAIt instruction on the replacement designs that do not have a current limiting resistor.

SIGNAL DESCRIPTIONS:

Clock Signals (W65C02S)

All internal clock signals for the W65C02S are generated by the input clock signal Ø2 (IN/PHI2I). WDC recommends using a clock oscillator for PHI2I. Also, PHI2I should be used for the system clock.

Clock Signals (R65C02/G65SC02)

The R65C02 requires an external Ø0 clock. Ø0 is a TTL level input that is used to generate the internal clocks of the R65C02. Two full level output clocks are generated by the R65C02. The Ø2 clock is in phase with Ø0. The Ø1 clock output is 180° out of phase with Ø0. When the input clock is stopped, the CPU is in the standby mode. For non-critical timing configurations, a simple RC or crystal network may be strapped between Ø0 (IN) and Ø1 (OUT).
Consult the Rockwell or GTE Datasheet/Databook for clock configuration options.

Clock Signals (R65C102)

The R65C102 internal clocks may be generated by a TTL level single phase input, and RC time base input, or a crystal time base input (÷ 4) using the XTLO and XTLI input pins. Two full level output clocks are generated by the R65C102. The Ø2 clock output provides timing for external R/W operations. Addresses are valid after the address setup time (t_{ADS}) referenced to the falling edge of Ø2 (OUT). The Ø4 output is a quadrature output clock that is delayed from the falling edge of the Ø2 clock by delay time t_{AVS}. Using the Ø4 clock, addresses are valid at the rising edge of Ø4.
Consult the Rockwell Datasheet/Databook for clock configuration options.

Clock Signals (R65C112)

All internal clock signals for the R65C112 and W65C02S are generated by the input clock signal Ø2 (IN). Since this device is intended to be operated in the slave mode it does not have internal clock generation, but rather requires the external clock Ø2 (IN) from a host device.
Consult the Rockwell Datasheet/Databook for clock configuration options.

FAMILY COMPARISON CHART

Feature	R65C02	R65C102	R65C112	W65C02S
Pin compatible with NMOS R65C02	X			
64K addressable bytes of memory	X	X	X	X
IRQ interrupt	X	X	X	X
On-chip clock oscillator	X	X		
External clock only			X	X
TTL level single phase clock input	X	X		
RC time base clock input	X	X		
Crystal time base clock input	X	X		
Single phase clock input			X	X
Two phase output clock				
SYNC and RDY signals	X	X	X	X
Bus Enable (BE) signal		X	X	X
Memory Lock (ML) output signal		X	X	X
Direct Memory Access (DMA) capacity		X	X	X
NMI interrupt signal	X	X	X	X

G65C02PEI vs. W65C02SPL

PIN	G65SC02PEI	W65C02SPL
1	VSS	VSS
2	NC	VPB
3	RDY	RDY
4	PHI1O	PHI1O
5	IRQB	IRQB
6	NC	MLB
7	NMIB	NMIB
8	SYNC	SYNC
9	NC	VDD
10	VDD	A0
11	A0	A1
12	A1	NC
13	A2	A2
14	A3	A3
15	A4	A4
16	A5	A5
17	A6	A6
18	A7	A7
19	A8	A8
20	A9	A9
21	A10	A10
22	A11	A11
23	VSS	VSS
24	NC	VSS
25	A12	A12
26	A13	A13
27	A14	A14
28	A15	A15
29	D7	D7
30	D6	D6
31	D5	D5
32	D4	D4
33	D3	D3
34	D2	D2
35	D1	D1
36	D0	D0
37	RWB	VDD
38	NC	RWB
39	NC	NC
40	NC	BE
41	PHI2	PHI2
42	SOB	SOB
43	PHI2O	PHI2O
44	RESB	RESB

Comments

1. The gray cells are used show differences in the pins.
2. Pin 40 (BE) on the W65C02SPL is an input and must be held high or driven for use in the system. If it is allowed to float it will cause problems because the buffers may get turned off if it goes low.

2166 E. Brown Rd. Mesa, Arizona 85213
phone: 480 962-4545, fax: 480 835-6442

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