Personal amateur radio computer "Radio-86RK"

Already today, humanity is literally drowning in a stream of information. According to experts, in the early 80s, about half of the working population of industrially developed countries was employed in one way or another in the field of information processing, and according to some forecasts, by the 90s this share will increase to 80%! A person is simply not capable of independently coping with such a volume of information, and naturally, he looks for an assistant.

This assistant is the powerful means of computing technology, which, thanks to the creation of microprocessors, are becoming more accessible to a wider range of users every day, and the day is not far off when each of us will have a personal computer on our desk (both at work and at home). Obviously, radio amateurs will be among the first to acquire them.

In 1982-1983, the magazine "Radio" published a description of the personal computer "Micro-80", but for some reasons this design did not become widespread. The complexity of the computer (more than 200 microcircuits), the lack of printed circuit board drawings, and most importantly - the lack of microcircuits necessary for assembling the computer in retail.

The amateur radio computer "Radio-86RK", the description of which we are beginning to publish, is more suitable for mass replication: the number of microcircuits has been reduced to the limit - there are only 29 of them in it, all the parts — are mounted on one printed circuit board, the drawing of which has been checked during experimental assembly in the editorial office.

Unfortunately, it is still difficult to acquire these 29 microcircuits. In the opinion of the editors, the optimal solution to the problem is to produce a set of microcircuits — for self-assembly of a computer in amateur conditions. I would like to hope that our industry and trade will listen to this opinion.

COMPUTER ARCHITECTURE

The block diagram of the personal amateur radio computer (RC) is shown in Fig. 1. The "heart" of the RC is the KR580IK80A microprocessor. A clock generator on the KR580GF24 microcircuit is used to synchronize the operation of the microprocessor and all other units. The memory is formed by a read-only memory device (ROM) with a capacity of 2 KB (K573RF5 microcircuit) and a random access memory device (RAM) with a capacity of 16 or 32 KB (respectively on eight or sixteen K565RUZA microcircuits). The ROM stores the MONITOR control program, and the RAM serves to store the codes of symbols displayed on the display screen, user programs and data. Information is entered into the RK from a household cassette recorder and keyboard, the results of the work are displayed on the TV screen and can be saved on magnetic tape.

The keyboard and tape recorder are connected to the RK via the programmable peripheral adapter (PPA) KR580IK55. Various amateur radio designs with digital control of operating modes can be connected via an additional PPA, for example, an RTTY unit, household radio complex devices, various sensors, actuators, etc.

The video signal is generated by the display controller, built on the KR580VG75 integrated circuit. The contents of the RAM area, in which the codes of the displayed characters are stored, are transferred to the internal registers of the controller using the direct memory access (DMA) method. The KR580IK57 integrated circuit is used to control the DMA process. Simultaneously with the for-

By processing the video signal during the PDP process, the contents of the RAM are regenerated.

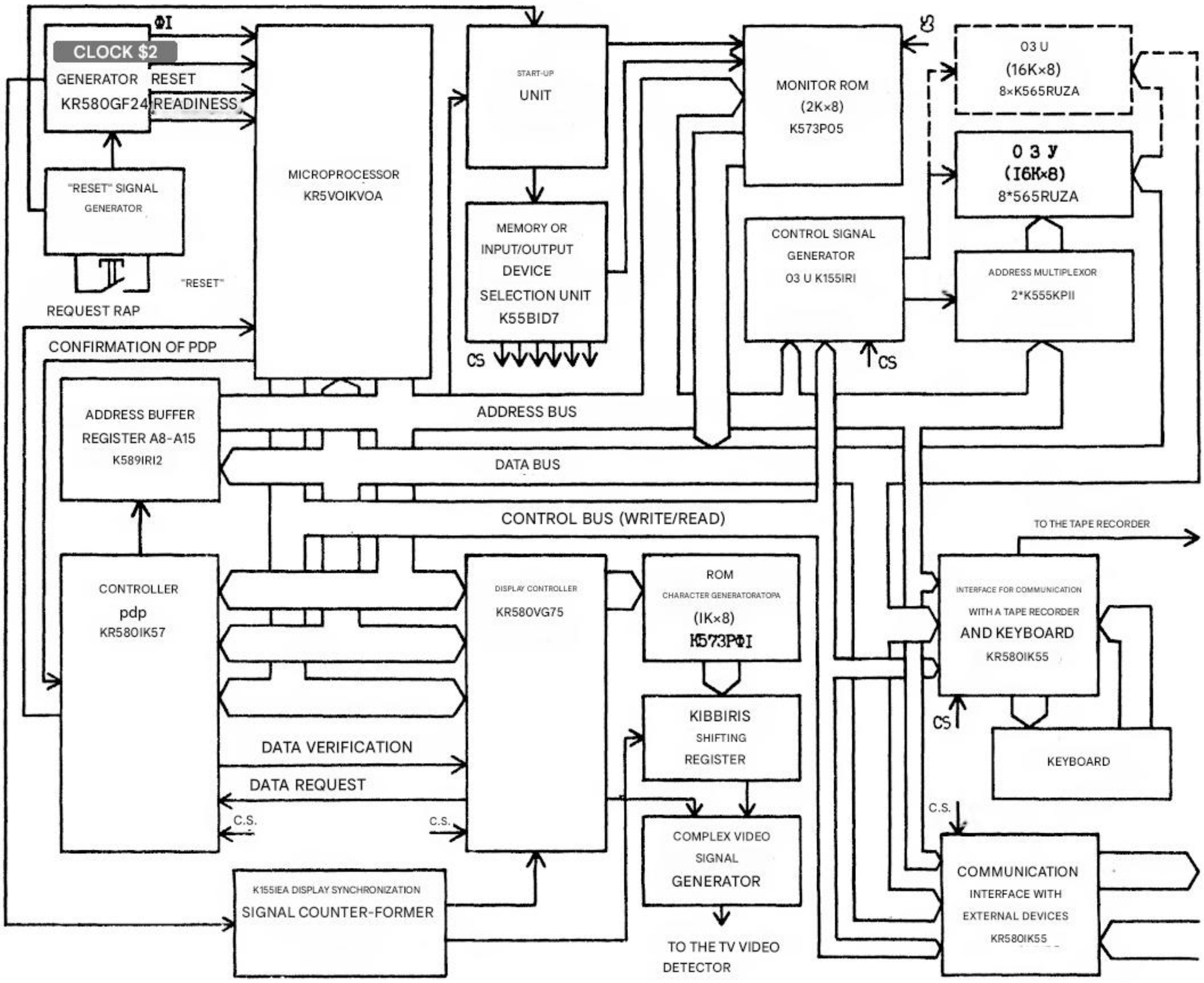
In order to better understand the principle of the RK construction, we will briefly dwell on the considerations that guided the authors during its development. The main thing was the desire to reduce, as much as possible, the number of microcircuits in the RK and to ensure software compatibility with the "Micro-80".

To achieve these goals, it was decided to build a display controller on the KR580VG75 integrated circuit. Using it and the integrated circuit of the PDP controller made it possible to abandon the special controller for regenerating the contents of the dynamic RAM.

As in the "Micro-80", the image on the TV screen is formed in the "Radio-86RK" by illuminating individual dots of the television raster; the same ROM character generator (K573RFI BIS) is used, and for displaying the characters, the same matrix of elements measuring 6x8 is used. The beam is modulated by signals from the output of the shift register, where information about the next character to be displayed is preliminarily entered in parallel form from the ROM character generator.

In the "Radio-86RK" part of the RAM cells is allocated for the so-called screen area (Fig. 2 shows the memory distribution in the RK for RAM with a capacity of 16K and 32K). Each character place on the TV screen corresponds to a specific cell in the screen area of the RAM, therefore, to output a symbol to a specific character place, the microprocessor must write its code into the corresponding cell of this area.

In order for the image to be constantly present on the CRT screen, it is necessary during the scanning of each television



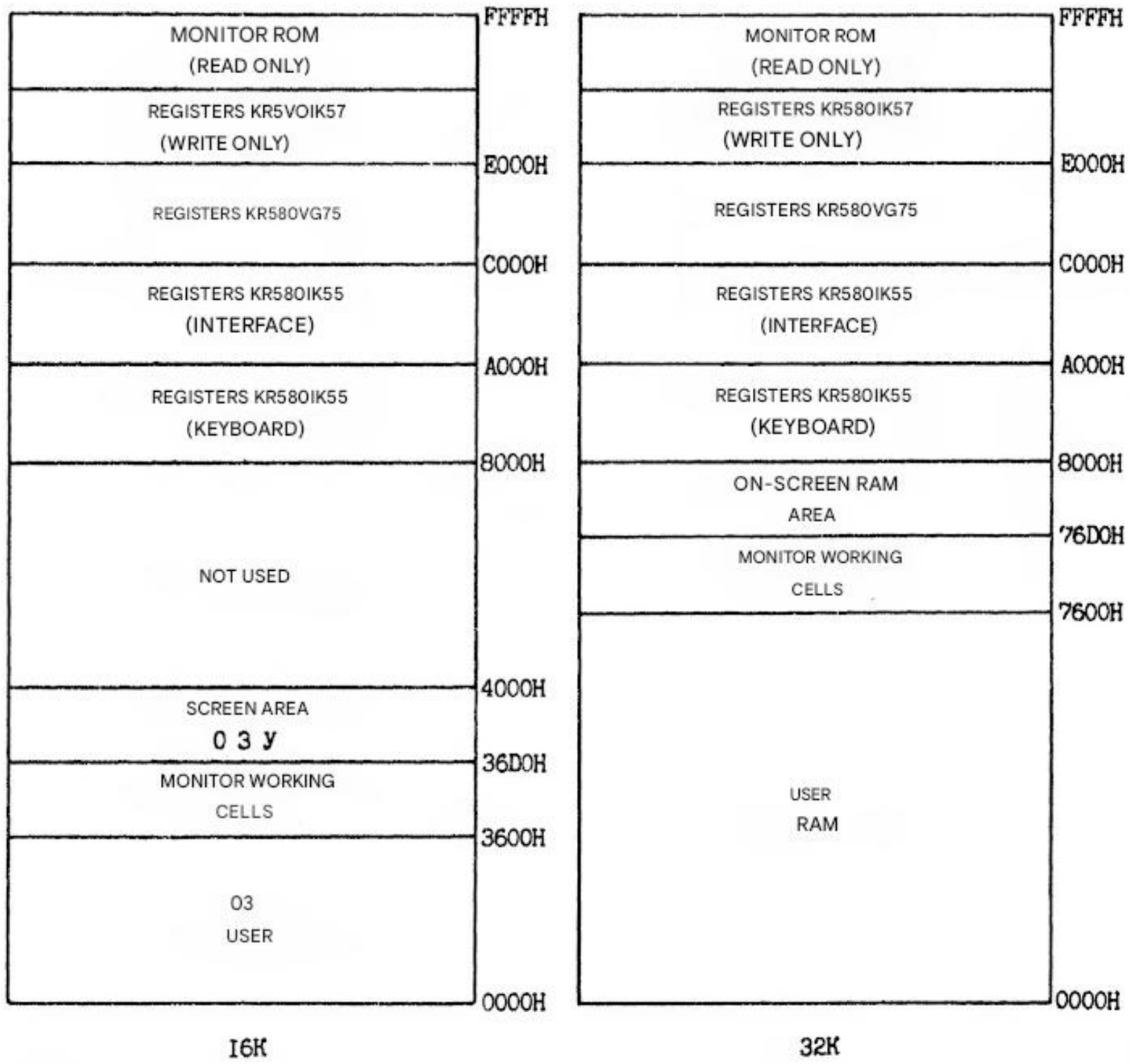
Rice. 1

frame, periodically, synchronously with the movement of the beam, to issue sequentially all codes from the screen area to the address inputs of the ROM of the character generator. This function is performed by the display controller LSI together with the PDP controller.

The KR580VG75 integrated circuit has two internal buffer registers, each of which can store up to 80 eight-bit character codes for subsequent display on the screen. This organization of the integrated circuit allows minimizing the downtime of the microprocessor due to the fact that the memory is busy exchanging with the display controller. During operation,

RK bots, while the symbols stored in one of the buffer registers are sequentially displayed on the TV screen, the codes of the following symbols are rewritten from the screen area of RAM to the other buffer in the DDP mode. Thus, these buffers store the codes of symbols of two adjacent lines. Upon completion of displaying information from one register, the display process from the other begins. An important feature of the KR580VG75 BIS is the ability to programmatically adjust the parameters of the sync pulses, the type and position of the cursor on the screen, the format of displaying information (number of lines, number of in characters in a line, etc.). More details about the operation of the BIS can be found in [1].

As noted earlier, the transfer of characters from the screen area of RAM to the display controller buffers is carried out using the DMA. In the DMA mode, data is directly transferred from RAM to the display controller, bypassing the microprocessor. To organize such transfers, the KR580IK57 LSI is used in the RC. During direct access to memory, it generates signals on the address and control buses instead of the microprocessor. A detailed description



Rice. 2

The description of the operation of this controller is given in [2].

The interaction of the display controllers, the PDP and the microprocessor occurs as follows. To output the next line to the screen, the first of them generates a DATA REQUEST signal on the DRQ pin. Based on this signal, the KR580IK57 controller prepares the microprocessor for operation in the PDP mode, issuing a PDP REQUEST signal to the HOLD input of the microprocessor, which in response to this switches its buses to a high-impedance state and notifies the controller with a PDP ACKNOWLEDGE signal on the HLDA pin. Having received this signal, the PDP controller initiates the output of data from RAM to the data bus, i.e., it sets the address codes of the screen area cells on the address bus, issues a READ signal on the control bus and generates a DATA ACKNOWLEDGE signal on the DACK pin of the display controller. Based on these signals and the appearance of a logical () at the IORD pin, the controller

ra PDP bytes from RAM are rewritten via the data bus into the internal buffer of the display controller.

Since the process of data transfer from the screen area of RAM to the display controller is regular, and the period of access to RAM does not exceed 2 ms, it turned out to be possible to use the PDP cycles to regenerate the contents of RAM and to refuse to use a special memory regeneration controller. However, it is necessary to limit the duration of the RESET signal. If the pulse duration on the RESET pin does not exceed 1...1.5 ms, then the microprocessor, having started to execute the MONITOR control program, will have time to reconfigure the display controller and PDP, thereby resuming the memory regeneration process. Otherwise, the information stored in RAM will be lost.

To simplify the RK circuit, it was decided to use a control bus, consisting only of READ AND WRITE signal transmission lines. In this case, access to the ports of the RK controllers occurs in the same way as to the memory cells, i.e. the addresses of the ports and memory cells are located in a single address space. The maximum permissible volume of directly addressed memory in this case is naturally less than 64 KB. Such a simplified control bus required a non-standard connection of the KR580IK57 LSI controller. In the PDP mode, the WR signal for the KR580VG75 LSI is formed at the IORD controller pin, and the READ signal for the memory LSI is formed at the MEMW pin. When WRITING control words into the PDP controller LSI, a logical 0 signal from the WR output of the microprocessor is sent to the IOW'R pin.

The presence of only two control signals made it impractical to use the KR580VK28 system controller microcircuit, but the developers were faced with the task of reducing the load on the address and data bus lines of the microprocessor, since their maximum load capacity is one TTL input (1.9 mA). For this purpose, the RK uses microcircuits of the series with low input consumption.

The named circuit solutions made it possible to develop the RK on only 29 microcircuits. Many tasks, traditionally implemented circuit design, were solved by software: as in the "MICRO-80", the functions of scanning and eliminating the chatter of keyboard contacts, forming the screen area of RAM, recording signals and reading from the tape recorder were solved by software.

(To be continued)

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in accordance with Fig. 6, a, towards the younger ones in accordance with Fig. 6, b. At level 1 at the "Record" input, pulses are counted; at level 0, the counted information is shifted.

In dynamic indication devices it is necessary to shift information by one decimal place at once, therefore the shift register is closed in a ring, as shown in Fig. 7 (the circuits for supplying pulses and control signals can be implemented according to the circuits in Fig. 4 or 5). The role of the shift enable input in this case is also played by the "Record" input. Obviously, when connecting microcircuits in accordance with Fig. 7, recording parallel information in them is impossible.

The K155IE9 counter can also be used in a divider with a variable division coefficient (Fig. 8). To do this, it is necessary to supply a carry signal of a single-bit or multi-bit (from the most significant digit) counter via an inverter to the write enable input 1, and the code levels determining the conversion coefficient to the inputs D1, D2, D4, D8. When the state 99...9 is reached during the counting process, the counter switches to the parallel recording mode, and when the next clock pulse is applied, instead of switching to the zero state, the parallel code signals supplied in parallel to the inputs D1, D2, D4, D8 of the microcircuits are written. As a result, the overall conversion factor N is reduced by the number K corresponding to the decimal value of this code: N = 10 - K, where n is the number of microcircuits in the divider. The conversion factor at output 2 can be changed within the range from 1 to 10 (the duration of positive output pulses is equal to the duration of input pulses), at output 1 from 2 to 10 (the duration of negative output pulses is equal to the period of input pulses). If the divider is assembled according to the circuit in Fig. 5, the inverter DD3.1 must be replaced by a 2AND-NOT element, the second input of which must be connected to the carry output P of the first microcircuit of the divider.

(To be continued)

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2. Alekseev S. Application of K155 series microcircuits. - Radio, 1978, No. 5, pp. 37, 38. 3. Alekseev S. Application of K155 series microcircuits. - Radio, 1982, No. 2, pp. 30-34.

Personal amateur radio

Computer "Radio-86PK"

CENTRAL

CPU

MICROCOMPUTERS

The basic electric circuit diagram of the microcomputer (hereinafter for brevity RK) is shown in Fig. 3. The clock generator RK is implemented on the chip KR580GF24 (D1), designed specifically for work with the microprocessor KR 580IK80A (D6). The frequency of the clock pulses is determined by the quartz resonator connected to the terminals X1 and X2. Its resonant frequency should be 9 times greater than the selected clock frequency of the microprocessor. Since in the RK the clock generator also serves to synchronize the operation of the display controller, which is an ordinary TV set, the frequency of the quartz resonator is chosen equal to 16 MHz. In this case, the clock frequency of the micropressor is equal to 16/9 = 1.78 MHz, which is slightly lower than the maximum permissible (2 MHz).

The pulses required to synchronize the microprocessor at the terminals Φ1 and Φ2 have an amplitude of 12 V. At the remaining terminals of the microcircuit, signals with a TTL level are formed. Synchronization of the peripheral integrated circuits is carried out by a sequence of pulses received at the terminal Φ2TTI. The sequence of pulses C has the frequency of the quartz resonator and the duty cycle about 2, formed at the OSC pin, is used to synchronize the display controller and the dynamic memory integrated circuit control signal generator. The READY and RESET signals from external devices are fed to the RDY IN A RESIN pins at arbitrary times. These signals are stored in the internal triggers of the clock generator and are transmitted to the RDY and RES pins at the leading edge of the pulse sequence Φ2. In addition, the RES signal can be formed by the Schmitt trigger contained in the clock generator. The signal comes to the RESIN input from the forming device assembled on elements C1, C2, R1, R2, R3, VD1 and the "RESET" button (Fig. 1) and limiting the duration of the signal of the same name.

Since there are no slow-working devices in the RK that would require switching the microprocessor to the standby state when "communicating" with it, the RDYIN pin is constantly fed with a logical 1 level.

At the STSTB output at the moment of action signal Φi ϕo a pulse is formed, strobing the byte of the microprocessor status. Usually this signal is fed to the same-name input of the system controller. In the described computer this signal is not used, however, KO OH is necessary for organizing the cycle mode during debugging of the RK.

Let us consider the formation of the WRITE and READ signals of the control bus. The first of them can be formed only by the D6 microprocessor on its WR output. This signal goes directly to the corresponding inputs of the D2, D14, D17, D20 microcircuits, and to the WE inputs of the D22-D29 memory microcircuits and the RAM control signal generator.

res repeater D5.4, and to the WR output of the display controller D8 and through the element D4.1.

Continued. See the beginning in Radio, 1986, No. 4.

The READ signal is formed not only by the microprocessor D6, but also by the PDP controller D2 when transmitting character codes from the screen area of the RAM to the display controller. Some features of the microprocessor and PDP controller operation are used. The signal at the DBIN pin of the microprocessor is active (logical level 1) only when reading data, and at the MEMW pin of the controller (logical level 0) - at the moment of reading a byte from the screen area of the RAM to the display controller. The READ signal is formed from these signals by the element D5.1. Resistor R5 serves to form the logical level 1 at pin 2 of the element D5.1 at the time when the MEMW output of the controller is in a high-impedance state.

MEMORY OR I/O DEVICE SELECTION UNIT

The address decoder is implemented on microcircuits D11, D5.3, D10.4 and D4.3. Depending on the state of lines A13-A15 of the address bus, a logical 0 level is formed at one of the outputs of microcircuit D11, which makes it possible to determine which group of memory - cells is being accessed. Thus, the entire address space of the microprocessor (64 KB) is divided into 8 blocks of 8 KB each. At the outputs of elements D5.3 and D10.4, when accessing RAM cells with addresses 0000H 3FFFH 4000H 7FFFH, respectively, a logical 1" signal is formed.

The signals from outputs 4-7 of decoder D11 are used to select one of the peripheral integrated circuits: D20, D14, D8 or D2. It should be noted that the signal from output 7 is also used to select the ROM chip D17, i.e. the same signal is used to select both the integrated circuit of the PDP controller and the ROM. This solution was possible due to the fact that information is only read from the ROM, and it is only written to the PDP controller during initialization of the latter.

* See Fig. 2 in Radio, 1986, No. 4.

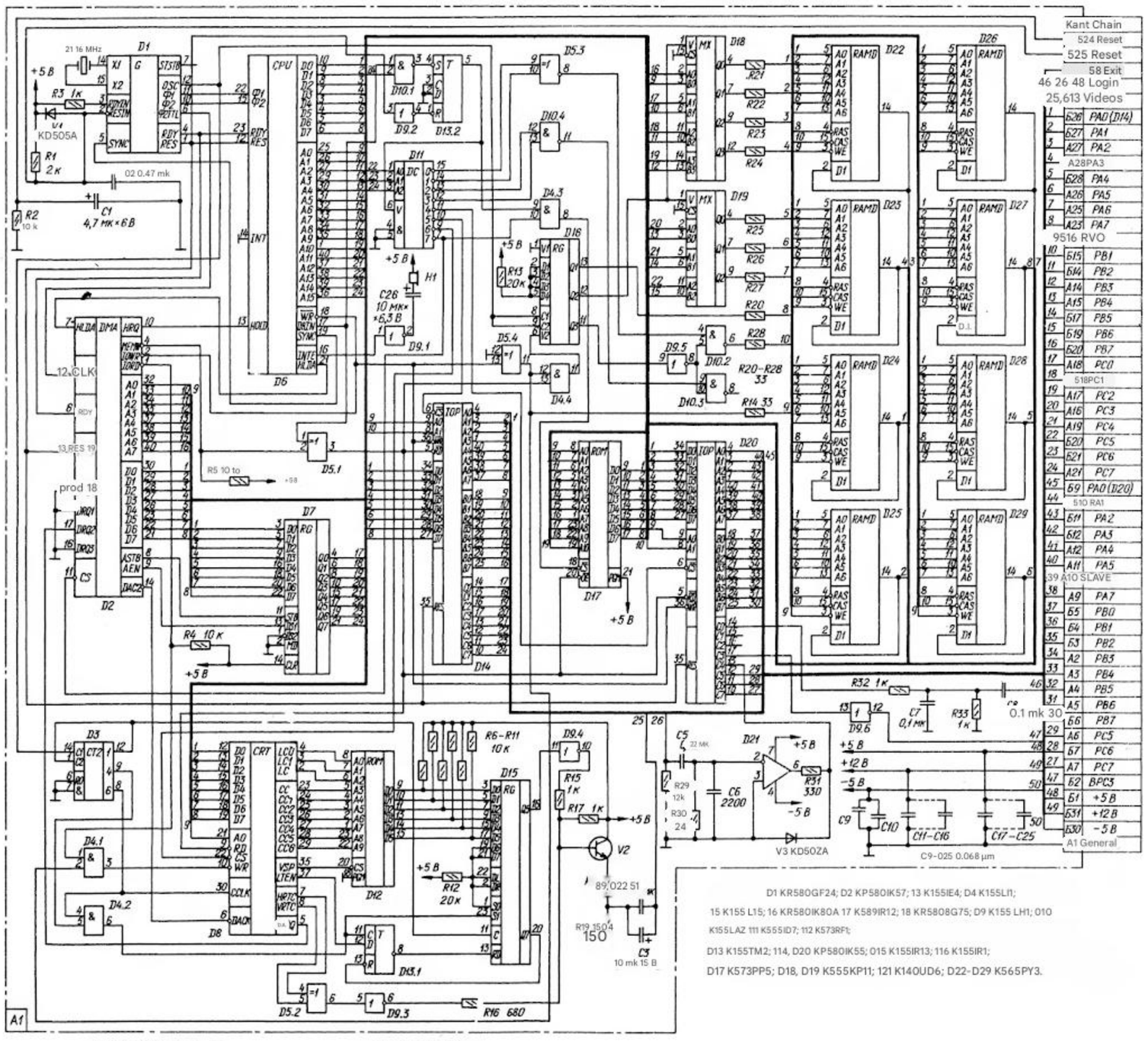
after reset the microprocessor starts executing the program from the command located at address 0000H, and the ROM storing the MONITOR control program is allocated addresses starting with F800H, the computer has entered the initial startup block. At the output of trigger D13.2 at the moment of arrival of the RESET signal, the logical 0 level appears, which prohibits the operation of decoder D11 and through element D4.3 goes to the CS input of ROM microcircuit D17, which ensures reading of the first command from the ROM Since command of unconditional transition to the beginning of MONITOR. After execution of this command, the address code of the next command appears on the address bus, the most significant bit of which is equal to - 1. The appearance of a high level on line A15 transfers trigger D13.2 to the initial state, as a result of which further decoding of addresses occurs in the usual way.

RAM

RAM microcircuits of the RK is implemented on a dynamic The memory microcircuit of the K565RUZ type (D22-D29). The peculiarities of these are temporary multiplexing maximum number of — of addresses and the need for periodic regeneration of the information stored in them. The address code is entered into the address register of the microcircuits through the AO-A6 inputs sequentially: first, the codes of the seven junior and then the seven senior address bits are received, accompanied by the row selection signals (RAS) and column (CAS) respectively. The addresses are multiplexed by the D18 and D19 microcircuits, to the inputs of which the AO-A13 bits of the address code are received from the address bus. Depending on the signal level at the V inputs of these multiplexers, signals from either the AO-A6 lines or the A7-A13 lines of the address bus are received at the AO-A6 inputs of the D22-D29 microcircuits.

To generate signals that control the operation - of the dynamic memory, a unit assembled on the D16 microcircuit and elements D4.4, D9.5, D10.2 and D10.3 is used. The OSC signal of the clock generator is fed to the C1 C2 inputs of the shift register D16. In the absence of READ and WRITE signals on the control bus, a high logic level is fed to the V2 input of the register D16 from element D4.4, causing it to operate in parallel mode.

data reception. If necessary, READING from RAM Fig. 3



or WRITING into it, a low logic level is formed at the output of element D4.4, as a result of which the register goes into the information shift mode, and low logic levels are set at its outputs in turn, with a delay of 62.5 ns. Signals Q1 and Q2 are fed respectively to the RAS inputs of the memory chips and the V inputs of multiplexers D18, D19. The same level, in the presence of a RAM selection signal, is fed through element D10.2 from the Q3 output of register D16 and to the CAS inputs of the memory chips. Resistors R14, R20-R28 are used to improve the shape of the signals fed to the address inputs of the RAM chips.

As already noted, the RAM capacity of the RK can be increased to 32 KB. To do this, 8 additional memory chips are introduced into it, the terminals of which are connected to the terminals of the same name of the D22 - D29 chips. The exception is the CAS inputs: they are combined with each other and connected to the output of the D10.3 element, the purpose of which is similar to the purpose of the D10.2 element. The simplest design solution is to install additional RAM chips on those already on the printed circuit board and solder their terminals to the terminals of the latter.

PDP CONTROLLER

As already noted, the transfer of data from RAM to the display controller is carried out by the method of direct access to the memory of the KR580IK57 (D2). controller

The multimode buffer register D7 operates in conjunction with the D2 PDP controller and is designed to temporarily store eight senior address code digits. This is necessary because the DO-D7 outputs are used in the multiplex-HOM mode of the controller both to receive information from the data bus during its initialization and to output senior address code digits to — the address bus in the PDP mode. In this mode, a high-level signal is sent from the controller to the DS1 input of the D7 microcircuit, switching its outputs from the high-impedance state to the active state. In the first clock cycle of each PDP cycle, eight senior address code digits are sent to the DO-D7 inputs of the register, which are recorded by the STB signal and are sent through the terminals Q0-Q7 to the address bus. After this, the controller outputs Q0-Q7 are transferred to a high-impedance state, freeing the data bus for transmitting character codes from the screen area of the RAM to the display controller.

DISPLAY CONTROLLER

Let us now consider how the RK forms an image on the TV screen. To simplify the video signal formation unit, frame and line sync pulses are formed directly at the HRTC and VRTC outputs of the D8 display controller, thanks to its corresponding adjustment. Since the image at the edges of the TV screen is less sharp and often goes beyond its boundaries, it is darkened in these areas programmatically, i.e. by writing codes of the "space" symbol into the corresponding cells of the RAM screen area, which is equivalent to forming blanking intervals in the video signal. Alphanumeric information is displayed on the screen in 25 lines of 64 character spaces each. A 6×8 matrix of dots is allocated for each character space. The character lines are separated by two darkened lines of the television raster.

Thus, in one raster line, the display time of which is 48 µs, 6×64 = 384 dots can be illuminated. Consequently, the repetition frequency of the pulses fed to the input C of the shift register D15 must be equal to 8 MHz. It is obtained by dividing the frequency of the clock generator D1 by 2. The counter D3 is used as a frequency divider. At the same time, it forms symbol synchronization pulses fed to the CCLK input of the display controller D8 (FCCLK fosc/12). The repetition period of these pulses, equal to the time it takes for the kinescope beam to pass within one character cell, determines the frequency of changing the symbol codes.

at the terminals of the controller CCO - CC6.

After the information about the graphic representation of the current symbol is sequentially output to the output 05 of the shift register D15, the latter, under the action of the output signal of the element D4.2, switches from the shift mode to the mode of receiving information about the next symbol. The same signal is used to form the cursor of a flashing dash located under the displayed symbol. This type of cursor is determined by recording the corresponding

the code word into the internal register of the display controller D8.

When the beam passes the marked character place, a high logic level periodically appears at the LTEN pin of the display controller. It prepares the D13.1 trigger for switching the output signal of the D4.2 element, which occurs at the moment the marked character place begins to be displayed, which ensures the formation of the cursor.

Element D4.1 generates a signal for writing information to the display controller. A low logic level appears at its output at the same level on the WRITE line of the control bus during display controller initialization or a low level at the IOR pin of the PDP controller during the transfer of a byte from the screen area of RAM. Resistor R4 performs the same functions as resistor R5.

The formation of a complex television video signal is carried out by an emitter follower on transistor V2. Signals from the output of shift register D15 and the synchronization mixture formation unit, made on elements D5.2 and D9.3, respectively, are fed to its input via resistors R15 and R16.

FORMATION

SOUND SIGNALS

The INTE output of the microprocessor is used in the RK in an unconventional way — as a single-bit output port: using the EI and DI commands and the time delay subroutines, it is possible to generate audio frequency signals on it. Through the D9.1 element, they are sent to the H1 microphone capsule. Thus, the RK has the ability to programmatically implement various sound effects. A special subroutine is provided for this purpose in the MONITOR.

ma, which can be accessed from other programs, those written in BASIC.

(To be continued)

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