**Amateur Radio Kit**

**Microprocessor УМПК-Р**

**OPERATION MANUAL**

**Introduction**

This operating manual is intended for studying the operation of the microprocessor amateur radio kit.

The operating manual provides general information about the microprocessor amateur radio kit, technical specifications, purpose, operating principle, and procedure.

For operating the microprocessor amateur radio kit, a household television set is used as a display, and a user's mono cassette recorder is used as an external storage device. When using a colour television receiver, there may be a degradation in the image quality of characters due to permissible beam misalignment at the edges of the screen, which is typical for colour televisions.

**ATTENTION!**

Due to the continuous improvement of the УМПК-Р, the electrical circuit and design of the product may undergo minor changes, which are reflected in the operating manual.

**Additional Information for the English Translation**

A fresh Russian language copy of the manual was first generated from the original scanned manual. This was lightly edited to fix obvious errors and some guesses were made when words disappeared into the binding.

Machine translation (Grok & ChatGPT) was then used to generate an initial English-language version of the manual, which you are presently reading. Likely still a work in progress.

This was then further edited and enhanced with additional information to help with troubleshooting.

Why go to this effort?

Well, my machine doesn’t work so I want to fix it, or at least make a decent attempt to. Also, this machine is based upon the home brew/DIY РАДИО-86РК computer. There are actually quite a few industrially produced versions of this design so I hope that by having a general understanding of how this machine works, other machines may also be repaired.

**Conventions Used**

* Soviet part identifiers are shown in the original Cyrillic to avoid confusion.
* Equivalent Western part identifiers are included to aid with finding pinouts & data sheets as well as sourcings.
* Note that Soviet parts use 2.5mm pin pitch and not the Western 2.54mm/0.1” pitch - this doesn’t really matter on smaller parts but will cause issues with fitting 40-pin parts.

**What Does УМПК-Р Mean?**

The machine originated from the Ukrainian SSR so it is tempting to think it might stand for

Украинский МикроПроцессорный Компьютер - Радио

Ukrainian Micro Processor Computer - Radio

However the Soviets were aPPIrently wary about any sort of nationalistic naming so it’s most likely stands for

Универсальный МикроПроцессорный Комплект - Радио

Universal MicroProcessor Kit - Radio

Brett Hallen, March 2025

Port Macquarie, Australia

www.youtube.com/@Brfff

**1. Purpose**

**1.1 Overview**

The microprocessor amateur radio kit УМПК-Р (hereinafter referred to as УМПК-Р) is designed to familiarise the user with the basics of computer technology, study programming methods in the BASIC language and machine code, develop practical skills in working with a microcomputer and external devices connected to it, developed by the user.

Depending on the programs developed or acquired by the user, the УМПК-Р can be used for:

* controlling amateur radio constructions;
* electronic television games;
* various types of calculations, both technical and economic;
* performing graphical work;
* creating home archives or catalogs on cassette tapes;
* programmatic control of household electronic devices, and so on.

**1.2 Terms Of Use**

1. Ambient air temperature from 10 to 35°C;

2. Relative humidity of ambient air up to 80% at 25°C and lower temperatures without moisture condensation;

3. Atmospheric pressure from 84 to 106.7kPa.

1.3 Climatic version - UHL 4.2 according to GOST I5150-69 (ГОСТ I5150-69)

**4. Device And Operation of УМПК-Р**

The УМПК-Р structurally consists of a computer and a power supply unit, connected to each other by a power supply cable, and functioning as complete standalone devices.

The УМПК-Р is built based on the K580 microprocessor series. The functional electrical diagram of the УМПК-Р is shown in Figure 1.

The main component of the circuit is the KR580VM80A (Intel 8080A) microprocessor. For synchronising the operation of the УМПК-Р, a clock generator based on the KR580GF24 (Intel 8224) chip is used.

The memory of the УМПК-Р consists of:

* a read-only memory (ROM) with a capacity of 2KB, implemented on the К573РФ5 or К573РФ2 chip, containing the MONITOR control program;
* a character generator ROM with a capacity of 2KB, implemented on the К573РФ2 or К573РФ5 chip;
* a random-access memory (RAM) with a capacity of16 KB for the УМПК-Р 16 version, implemented on the КР565РУ5Д3 or КР565РУ5Д4 chips, and 32KB for the УМПК-Р 32 version, implemented on the КР565РУ5Д1 or КР565РУ5Д2 chips.

The keyboard and external storage device (the user’s cassette recorder) are connected to the УМПК-Р processor via a programmable parallel interface (PPI) chip, the KR580VV55A (Intel 8255A). An additional programmable parallel interface chip, also the KR580VV55A, is intended for connecting external devices to the УМПК-Р.

The video signal is generated by the display controller КР580БГ75 (Intel 8275). The information displayed on the screen area of the RAM is transmitted to the controller using direct memory access (DMA). To manage this process, a large integrated circuit (IC) КР580ВТ57 (Intel 8257) is used.

The image on the television screen is formed by illuminating individual points of the television raster with a signal from the modulator output УМПК-Р. A 6x8 dot matrix is used to display characters.

The video signal is formed from signals from the display controller КР580БГ75 and the signals of the displayed character from the output of the shift register on the К155ИР13, where the character generator's ROM information is loaded in parallel format.

Figure 2 shows the memory address distribution of the УМПК-Р with a RAM size of 16KB (УМПК-Р I6 version) and 32KB (УМПК-Р 32 version). To display a character at a specific position on the screen, the microprocessor writes the character code to the corresponding cell in the screen area of the RAM.

In order for the image to remain on the television screen, it is necessary to periodically output all the codes from the screen area sequentially to the address inputs of the character generator's ROM. This function is performed by the display controller КР580БГ75.

The display controller has two internal buffer registers, each of which can store up to 30 8-bit character codes.

This organisation of the controller minimises the downtime of the microprocessor because the memory is occupied with exchanging data with the display controller. During operation, while the characters stored in one buffer register are sequentially displayed on the screen, the codes of the next characters are written to the other buffer register in DMA mode from the screen area of the RAM. After the display process from one buffer register is completed, the process of displaying from the other register begins.

Since the transfer of characters from the screen area of the RAM to the display controller’s buffer registers is done using DMA, the data in this mode is transferred directly from the RAM to the display controller, bypassing the microprocessor. The КР580ВТ57 IC is used to organise such transfers. In DMA mode, it independently generates signals on the address and control buses.

The interaction between the display controllers, DMA, and the microprocessor occurs as follows: to display the next line on the screen, the display controller generates a “DATA REQUEST" signal. In response to this signal, the DMA controller outputs a "DMA REQUEST" signal to the microprocessor's input, which then places its buses in a high-impedance state and issues a "DMA ACKNOWLEDGEMENT" signal. In response, the DMA controller sets the address codes for the screen area cells on the address bus, issues a "READ" signal on the control bus to transfer each byte, and sets the “DATA ACKNOWLEDGMENT" signal on the display controller’s output. Using these signals, a byte from the data bus is written to the internal buffer register of the display controller.

Since the process of transferring data to the screen area of the RAM to the display controller is regular, and the RAM access period does not exceed 2µs, DMA cycles are used for regenerating dynamic RAM. With a pulse duration of 1-1.5µs, the microprocessor, upon starting to execute the control program (the MONITOR), manages to reconfigure the display and DMA controllers, thus resuming the memory regeneration process. Otherwise, the information stored in the RAM would be lost.

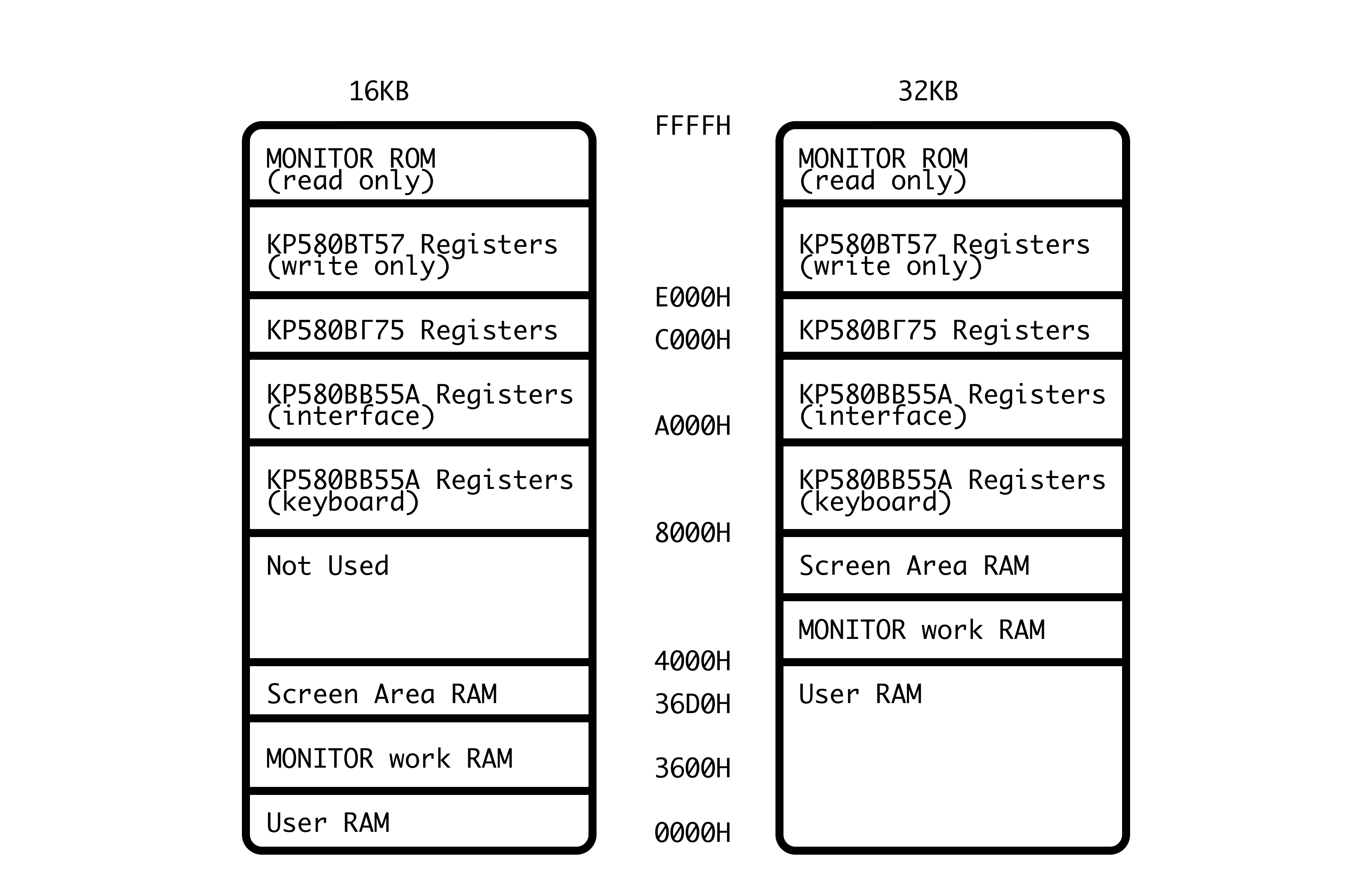
The control bus consists of two data transfer lines: "READ" and "WRITE."

Access to the controller ports is done in the same way as to memory cells, i.e. the addresses of the ports and memory cells are in the same address space.

The computer is powered by a power supply unit providing voltages of -5V, +5V, and +12V, and is implemented as a separate device.

**MEMORY ALLOCATION IN УМПК-Р FOR RAM**

**WITH 16KB AND 32KB**



**5. Structure and Operation of the Component Parts of УМПК-Р**

**5.1 Computer УМПК-Р**

The external appearance and functional purpose of the computer components of the УМПК-Р are shown in Figure 3. The УМПК-Р computer consists of a microprocessor board and a keyboard device board. The electrical connection between them is carried out via connectors, while the mechanical connection is achieved using brackets.

**5.1.1 Microprocessor (KP580BM80A, 8080A)**

The principal electrical schematic of the microprocessor is presented in Figures 4 and 5, with a list of components provided in Table 3. The microprocessor board and the arrangement of its components are shown in Figure 6.

**5.1.1.1 Clock Generator (КР580ГФ24/8224)**

The УМПК-Р clock generator is implemented on the КР580ГФ24 (D1) microcircuit, designed specifically for operation with the KP580BM80A (D5) microprocessor. The frequency of the clock pulses is determined by a quartz resonator connected to inputs XTAL1 (D1 pin 15) and XTAL2 (D1 pin 14).

Since the clock generator synchronises the operation of the display controller, the frequency of the quartz generator is chosen to be 16kHz. As a result, the clock frequency of the microprocessor is 16/9 = 1.78MHz.

The clock generator forms pulses with an amplitude of 12V at outputs Ф1 (D1 pin 11) and Ф2 (D1 pin 10), which are necessary for synchronising the microprocessor. At the remaining outputs, signals are generated with TTL levels. The sequence of pulses from the quartz generator, with a duty cycle of approximately two, is formed at the OSC output (D1 pin 12) and is used to synchronise the display controller and generate control signals for dynamic memory.

Inputs RDYIN (D1 pin 3) and /RESIN (D1 pin 2) receive "RESET" and "READY" signals from external devices at arbitrary moments in time. These signals are stored in the internal triggers of the clock generator and transmitted to the READY (D1 pin 4) and RESET (D1 pin 1) outputs, synchronised with the leading edge of the Ф2 pulse sequence. The /RESIN input signal comes from a "RESET" signal generation circuit, assembled from components C1, C2, R2, R3, VD1, and the [СБР] key of the keyboard device, limited by the strength of a single signal.

The RDYIN input is constantly supplied with a "logical 1", i.e. in this computer there are no slow devices that would require transitioning the microprocessor to a wait state. The   
/STSTB output (D1 pin 7), a control point, is not used for organising a cyclic mode during debugging.

**5.1.1.2 READ & WRITE Signals**

The formation of "WRITE" and "READ" signals in УМПК-Р occurs as follows.

The "WRITE" signal on the control bus is received from the /WR output of the D5 microprocessor (pin 18) and sent to the corresponding inputs of microcircuits D2 (8257,   
/MEMW pin 4), D14 (8255 pin 36), and D24 (8255)

For the WE inputs of memory elements D20 to D23 and D25 to D28, this signal is received through repeater D6.4 and resistor R34, and for the WR input of the display controller D8, it is also received through element D4.1.

The "WRITE" signal from the output of element D6.4 is also output to a connector for connecting external devices XS1. The "Read" signal is formed at the output of element D6.1, where the /MEMW signal from the DMA controller output (D2), which is active during the reading of a byte from the screen RAM area for the display controller, and the DBIN signal (pin 17) from the microprocessor D5 output, which is active during data reading, are supplied.

Resistor R5 is used to form a "logical 1" at the output 2 of D6.1 when the output 4 of element D2 is in a high-impedance state. The "READ" signal, similar to the "WRITE" signal, is output to a connector for external devices XS1 from the output of element D6.1.

**5.1.1.3 Address Decoding**

The address decoder is implemented using microcircuits D9, D4.3, D6.3, and D10.2. Depending on the state of the address bus lines A13 to A15, a "logical 0" level is formed at one of the outputs of the D9 microcircuit, allowing determination of which group of memory cells is being accessed. Thus, the entire address space of the microprocessor (64KB) is divided into eight blocks of 8KB each. At the outputs of elements D6.3 and D10.2, when accessing RAM cells with addresses 0000H to 3FFFH and 4000H to 7FFFH respectively, a "logical 1" level is formed. Depending on the version (УМПК-Р 16 or УМПК-Р 32) and the RAM microcircuits used, three jumpers are installed between contact pads 1 to 9, as shown in Table 1 on Figure 4. Using these jumpers and signals from elements D6.3 and D10.2, the necessary A7 and /CAS signals are formed for the RAM microcircuits.

The signals from outputs 4 to 7 of the D9 decoder (pins 7, 9, 10, 11) are used to select one of the integrated circuits: D24 (8255), D14 (8255), D8 (8275), D2 (8257). The signal from the output, in addition to selecting the DMA controller D2, is also used to select the ROM microcircuit D19. This is possible because only information reading is performed from the ROM, while information is only written to the DMA controller during initial programming. Since, after a reset, the microprocessor begins executing the program from the command located at address 0000H, and the ROM storing the MONITOR control program is assigned addresses starting from F800H, an initial startup block has been introduced into the computer. At the output 5 of the D13.1 trigger, at the moment the "RESET" signal arrives, a "logical 0" appears which disables the operation of the D9 decoder and, through element D4.3, is applied to the CS input of the ROM microcircuit D19. This ensures the reading of the first command from the ROM, a command for an unconditional jump to the start of the MONITOR. After executing this command, the address bus will display the address code of the next MONITOR command, the most significant bit of which is "1". The appearance of a "logical 1" on the A15 line of the address bus switches the D13.1 trigger back to its initial state, as a result of which address decoding subsequently occurs in the usual manner.

**5.1.1.4 RAM**

The RAM of the УМПК-Р is implemented using dynamic-type memory microcircuits of the КР565 series (D20 to D23, D25 to D28).

In the УМПК-Р version with a memory capacity of 16KB, eight microcircuits of type КР565РУ5Д3 or КР565РУ5Д4 are used. In the УМПК-Р 32 version with a memory capacity of 32KB, eight microcircuits of type КР565РУ5Д1 or КР565РУ5Д2 are used. The positions of the three jumpers on contact pads 1 to 9 for the corresponding version and the microcircuits installed on the board are specified in Table 1 of Figure 4.

The specific features of these microcircuits include time-multiplexed addressing and the need for periodic regeneration of the stored information.

The address code is loaded into the address register of the microcircuits through inputs A0 to A7 sequentially: first, the codes of the eight least significant bits are received, which are latched by the row selection signal /RAS, followed by the eight most significant bits, which are latched by the column selection signal /CAS. For address multiplexing, the circuit employs multiplexers К555КП11 (D17, D18). The address bus inputs to these multiplexers receive bits A0 to A13 of the address code, and the address inputs of the memory microcircuits are supplied with either bits A0 to A6 from the address bus or bits A7 to A13, depending on the signal level at the V inputs of the multiplexers.

To generate signals controlling the operation of dynamic memory, a module is used, assembled on the К155ИР1 microcircuit (D15) and elements D4.4, D10.3, D10.4, D11.1, and D11.4. The OSC signal from the clock generator is fed to the C2 input of the shift register D15 (pin 9). In the absence of "READ" and "WRITE" signals on the control bus, a "logical 1" is received at the V2 input of the shift register D15 (pin 6) from element D4.4, enabling its operation in parallel data reception mode. Meanwhile, with some delay, a low level is received at the C1 input (pin 8) from the output of element D11.1, performing a parallel write of "logical 1s” into the D15 register.

When a "READ" or "WRITE" signal appears, a "logical 0" is applied to the V2 input of the D15 microcircuit, causing the shift register to switch to the information shift mode. As a result, low logical levels are sequentially established at its outputs with a delay of 62.5ns. The signals from outputs Q1 and Q2 are fed to the RAS inputs of the memory microcircuits and the control inputs V of the multiplexers D17 and D18, respectively. Element D11.4, using the low level from the Q3 output of the D15 register and the presence of RAM selection signals from the D9 decoder, forms a "logical 0" level on elements D10.3 or D10.4 for the   
/CAS inputs of the memory microcircuits.

Resistors R23 to R32 and R34 are used to improve the shape of the signals applied to the inputs of the memory microcircuits.

**5.1.1.5 DMA Controller (КР580BT57, 8257)**

The Direct Memory Access (DMA) controller, implemented on the КР580BT57 microcircuit (D2), operates in conjunction with the multi-mode buffer register KP589ИР12 (D7).

The buffer register is designed for temporary storage of the eight most significant bits of the address code. This is necessary because, in the DMA controller, the D0 to D7 outputs are used both for receiving information from the data bus and for outputting the eight most significant bits of the address code to the address bus in DMA mode. In this mode, a "logical 1" is applied from the DMA controller to the DS2 input of the D7 microcircuit, switching its outputs from a high-impedance state to an active state.

In the first cycle of each DMA operation, the eight most significant bits of the address code are fed to the D0 to D7 inputs of the D7 register. These are latched by the STB signal and output through the Q0 to Q7 outputs to the address bus. After this, the D0 to D7 outputs of the DMA controller are switched to a high-impedance state, freeing the data bus for transferring character codes from the screen RAM area to the display controller.

**5.1.1.6 CRT Controller (КР580BГ75, 8275)**

The display controller КР580BГ75 (D8), due to its appropriate configuration, generates frame and line sync pulses directly at the HRTC and VRTC outputs. Since the image at the edges of television receiver screen is less sharp and often extends beyond their boundaries, it is darkened in these areas programmatically, i.e., by writing the "Space" character codes into the corresponding cells of the screen RAM area, which is equivalent to forming blanking intervals in the video signal.

Alphanumeric information is displayed on the screen in 25 lines, with 64 characters per line. Each character is formed by a 6x8 dot matrix. The character lines are separated by two darkened television raster lines.

In one raster line, the display time of which is 48µs, 6x64 = 384 dots can be illuminated. Therefore, the frequency of the pulses supplied to the C input of the shift register D16 must be 8MHz. This frequency is obtained by dividing the frequency from the OSC output of the clock generator D1 by two. A counter D3 is used as the frequency divider. It is also used to generate character synchronisation pulses, which are supplied to the CCLK input (pin 30) of the display controller D8, by dividing the clock generator frequency by 12. The period of these pulses, equal to the time it takes for the CRT beam to traverse one character position, determines the rate at which character codes change at the CC0 to CC6 outputs (pins 23-26) of the display controller D8.

When the information about the graphical representation of the currently displayed character has been sequentially output to the Q5 output of the shift register D16, this register will transition from shift mode to the mode of receiving information about the next character under the influence of the output signal from element D4.2. This signal is used to generate a cursor positioned beneath the displayed character. A blinking underscore is used as the cursor. This type of cursor is selected by writing the corresponding code word into the internal register of the controller D8.

During the scanning of a television line beneath a marked character, a "logical 1" periodically appears at the LTEN output (pin 37) of D8. At the moment the display of the marked character begins, the trigger D13.2 is switched by the output signal of element D4.2. This ensures the formation of the cursor.

Element D4.1 generates a signal for writing information to the display controller. A "logical 0" appears at its output when there is a low level on the "Write" line of the control bus during the initialisation of the display controller, or when there is a low level at the /MEMW output of the DMA controller during the transfer of a byte from the screen RAM area.

**5.1.1.7 Video Output**

The formation of the video signal is carried out by an emitter follower on transistor VT2. Signals of the displayed characters from the Q5 output of the shift register D16 are fed to its input through element D11.5 and resistor R18, while frame and line sync pulses are supplied through resistor R19 and a sync mixer shaper on elements D6.2 and D11.3.

The video signal from the adjustable resistor R22 of the emitter follower is applied to the gate of the field-effect transistor VT5 of the modulator.

**5.1.1.8 Audio Output**

The generation of an audio signal accompanying the pressing of any key (except for [СБР], [СС], and [УС]) in the УМПК-Р is carried out through the /INTE output of the microprocessor and transistor VT1 to the speaker BF1, located on the keyboard device board.

In the MONITOR program, a special subroutine is provided for this purpose, which can be accessed from other programs, including those written in BASIC.

The УМПК-Р allows for the programmatic implementation of various sound effects through the /INTE output of the microprocessor using commands E1 and D1, along with time delay subroutines.

**5.1.1.9 RF Modulator**

The modulator, whose principal electrical schematic is shown in Figure 5, generates a television signal for the fifth channel in the meter band of television broadcasting.

The quartz oscillator of the modulator is implemented using transistor VT3 and resonator BQ2 with a frequency of 93.25MHz. The adjustable capacitor C32 is used to set the maximum amplitude of the oscillator’s oscillations. Amplitude modulation of the high-frequency oscillations is performed on transistor VT4 by the field-effect transistor VT5, to whose gate the video signal is applied. The DC operating mode of the modulator is set by the adjustable resistor R45. The necessary amplitude of the modulating video signal is adjusted by the variable resistor R22. The output impedance of the modulator, equal to 75Ω, is provided by the voltage divider R50, R51.

**5.1.1.10 External Storage**

The tape recorder (external storage device) is connected to the microprocessor via lines C0 and C4 of channel C of the programmable peripheral interface (PPI) КР580BB55А (D24). The recording of information onto the tape cassette of the external storage device is carried out through line C0 and an RC filter composed of elements R35, C6, R38, and C8. The input of information from the magnetic tape into the УМПК-Р is performed via line C4 of the PPI (D24) through a hysteresis comparator based on the operational amplifier K553UD2 (D29). The adjustable resistor R39 is used to set the required waveform of the recorded information signal.

**5.1.1.11 Expansion Interface**

The УМПК-Р includes an additional PPI based on the КР580BВ55 integrated circuit (D14), intended for interfacing with external devices developed by the user. According to the MONITOR program, this PPI is not configured. After receiving the "RESET" signal, all three of its channels operate in information input mode.

All eight communication lines of each of the A, B, and C channels of the PPI on D14, as well as the "READ" and "WRITE" signals, are routed to the XS1 connector, which is intended for external devices.

**5.1.1.12 Control Program MONITOR**

The control program, MONITOR, in the УМПК-Р, recorded in a 2KB ultraviolet-erasable ROM К573РФ5 (D19), initialises all programmable integrated circuits and ensures the operation of the keyboard, display, and cassette tape recorder interface. Additionally, MONITOR facilitates interaction with the user, who inputs specific directives via the keyboard and reads messages about the results of their execution on the display screen. The available directives allow viewing and modifying memory contents, manually entering programs or loading them from a tape recorder, executing programs or their parts stored in RAM while monitoring the contents of the microprocessor's internal registers, and outputting programs and data arrays to an external storage device—magnetic tape. An additional function of MONITOR is to support the operation of other programs (such as a BASIC interpreter, text editor, etc.), for which it includes a set of standard input-output subroutines.

The codes of the MONITOR control program for the УМПК-Р 16 in hexadecimal format are provided in Table 4. Table 5 lists the addresses of MONITOR cells and the hexadecimal codes written into them for the УМПК-Р 32 version, which differ from the MONITOR codes for the УМПК-Р 16.

**5.1.2 Keyboard Device**

The principal electrical schematic and the board layout with the arrangement of the keyboard device components are shown in Figures 7 and 8. The list of components of the keyboard device is provided in Table 6. The functional purpose and arrangement of the keys (Figure 3) correspond to those adopted in most industrial displays.

**5.1.2.1 Keyboard Operation**

The operation of the keyboard device is based on the principle of scanning contacts of a matrix keyboard with addressable keys.

Through the channel A lines of the PPI (chains RA0 to RA7), configured for information output, scanning pulses are sequentially supplied to diodes VD3 to VD10. The diodes protect the port lines from damage during simultaneous pressing of multiple keys.

During the contact polling process, the keyboard subroutine sequentially forms a low logical level on each of the channel A lines (on the other seven lines, the levels remain high). Simultaneously, the subroutine reads and analyses the contents of channel B of the PPI (chains RB0 to RB7). If no key is pressed, high logical levels are applied to all channel B lines through resistors R6 to R13. When any key is pressed, a low level from the corresponding channel A line passes through the corresponding open diode to one of the channel B lines. The service subroutine determines the number of the pressed key and forms its corresponding seven-bit code.

When pressing each of the main keys, depending on whether one of the auxiliary modifier keys (СС or УС) was pressed together with or before the main key, three different codes can be formed. In this case, special control or graphic symbols are displayed on the screen. The

РУС/ЛАТ key determines which of the two alphabets (Russian or Latin) will be displayed on the screen (switching between them requires pressing it once). Closing the contacts of these three keys (СС, УС and РУС/ЛАТ) results in the formation of a low logical level on lines S5 to S7 of the PPI channel (chains RS5 to RS7), operating in input mode, and otherwise interpreting the main keys, which reduces their number. Noise from key contacts is eliminated programmatically. The auto-repeat mode and audible signalling of key presses in УМПК-Р are also implemented programmatically, i.e., with a prolonged (more than 1 second) press of a key, an audible signal is issued without interruption.

Indicators VD1 and VD2 are installed on the keyboard device board. Indicator VD1, connected to the configured output line S3 of the PPI through element D11.6 (see Figure 4) and resistor R4 (chain VRS3), signals the display of the Russian alphabet on the screen. Indicator VD2 signals the activation of УМПК-Р. A capsule forming an audible signal is also installed on the keyboard device board.

In Table 7, the symbols (special, control, and graphic) formed by УМПК-Р, their codes, and the addresses of the RAM cells of the generator (D12) with hexadecimal numbers written into them corresponding to these symbols are provided.

**5.1.2.2 Keyboard Construction**

The structurally designed keyboard device is implemented using membrane keyboard technology (see Figure 8).

On the printed circuit board of the keyboard device 1, the closing contacts are made in the form of parallel printed conductors 2 and 3, alternating between each other. The closing element of the keyboard is foiled Lavsan 5 with a set of circular contacts 6, the diameter of which slightly exceeds the distance between the closing printed conductors. The foiled Lavsan 5 is glued to the printed circuit board I on both sides with adhesive tape 4, 0.25 mm thick, with Ø14 mm holes at the key locations.

Film 8 with a key diagram and an image of the corresponding symbols is glued to the foiled Lavsan 5 on both sides with adhesive tape 7, 0.05 mm thick.

When pressing the key diagram, the film 8, adhesive tape 7, and foiled Lavsan 5 bend, and contacts 6 close the printed conductors 2 and 3. To improve the contact properties and prevent oxidation of the printed circuit board in the areas of the closing conductors and contacts of the foiled Lavsan, they are coated with palladium.

"Lavsan" is a Russian trade name for a type of polyester film, chemically known as polyethylene terephthalate (PET). It is similar to materials like Mylar in Western terminology. "Фольгированный" means "foiled" or "coated with foil," indicating that the lavsan film has a thin layer of metal foil (often aluminum) applied to it. In the context of the УМПК-Р keyboard device, this refers to a metallized polyester film used in the membrane keyboard construction, where the foil provides conductive tracks or contacts for key operation.

So, in technical terms, it could be described as "metallized polyester film" or simply "foiled PET film", depending on the context.

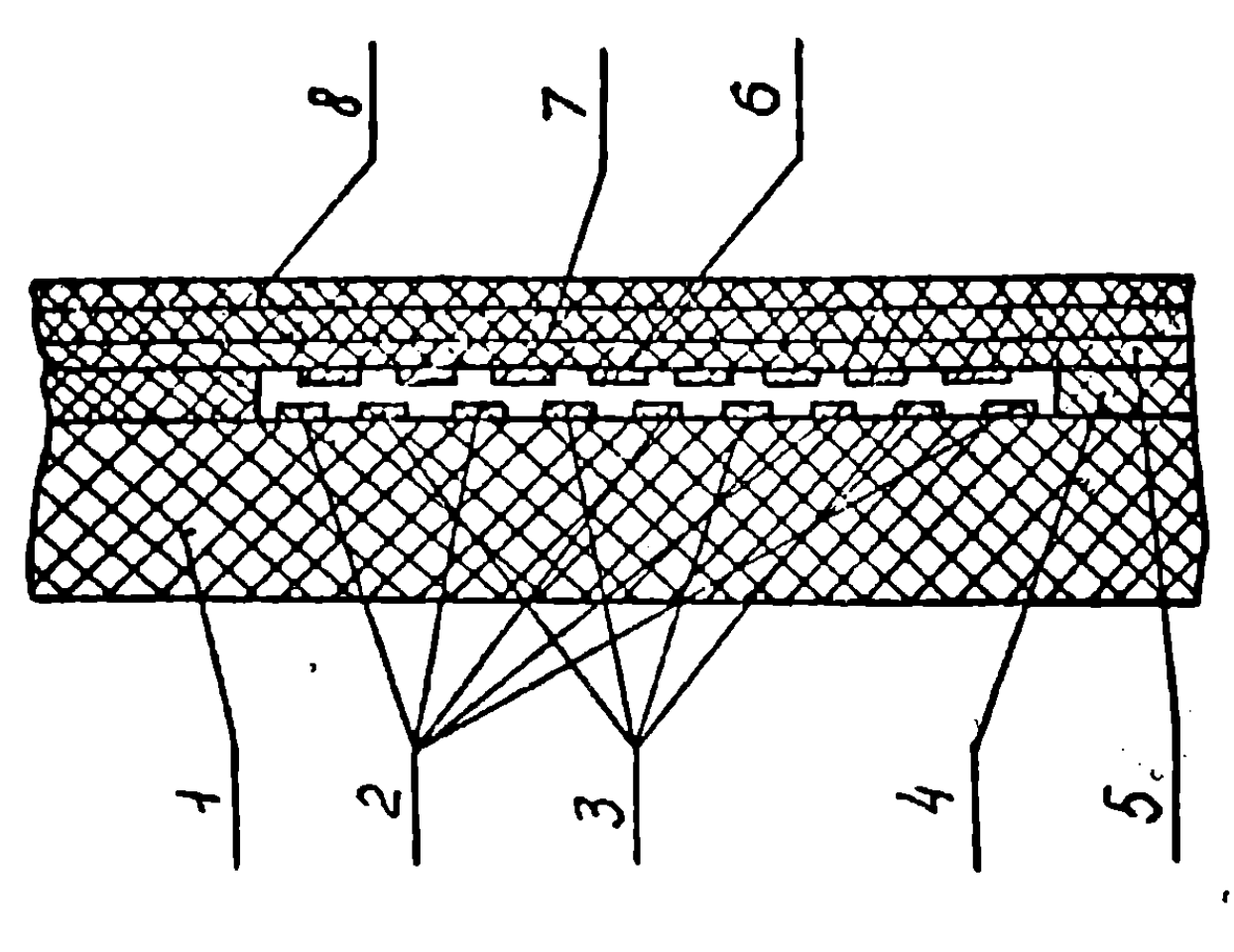


Figure 8

**Keyboard Special Keys**

[ВК] Возврат Каретки (carriage return)

[ЗБ] ЗЗабой (backspace)

[СС] Специальные символы (special characters)

[ПС] Перевод Строки (line feed)

[СБР] Сброс (reset)

[УС] Управляющие символы (control characters)

[АР2] Автоматический Режим 2 (automatic mode), or more recently

Альтернативный Регистр 2 (alternate register)

[СТР] Система Трансформации Реальности, or [CTRL]

ВКЛ Включить (turn ON)

**IC List**

D1 КР580ГФ24 8224 Clock generator

D2 КР580ВТ57 8257 DMA controller

D3 К155ИЕ4 74LS92 Divide-by-12 counter

D4 К155ЛИ1 74LS08 Quad 2IN AND

D5 КР580ВМ80А 8080A CPU

D6 К155ЛП5 74LS86 Quad 2IN XOR

D7 К589ИР12 8212 8-bit I/O port

D8 КР580ВГ75 8275 CRT controller

D9 К555ИД7 74LS138 1-of-8 decoder/demultiplexer

D10 К155ЛА8 74LS01 Quad 2IN NAND

D11 К155ЛН1 74LS04 Hex inverter

D12 К573РФ2 2716 EPROM (for character data)

D13 К155ТМ2 74LS74 Dual D-type flip flop

D14 КР580ВВ55А 8255 Programmable peripheral adaptor

D15 К155ИР1 74LS95 4-bit shift register

D16 К155ИР13 74LS198 8-bit shift register

D17, D18 К555КП11 74LS257 Quad 2IN multiplexer

D19 К573РФ5 2716 EPROM (for MONITOR)

D24 КР580ВВ55А 8255 Programmable peripheral adaptor

D29 К553УД2 LM301 Op. Amp.

**Change History**

9-Mar-2025: initial version

10-Mar-2025: added intro, section 1, section 4, memory layout

Brett Hallen aka The Clueless Engineer

www.youtube.com/@Brfff