2.2. Debugging the RK

A brief description of the RK debugging process will help you identify the cause of a malfunction, either immediately after assembly or during operation.

Despite the simplicity of its design, the computer is a complex object for diagnosing faults. This is due to the close interplay between its software and hardware components.

In research laboratories or production environments, debugging and testing microprocessor devices typically involve specialised technical and software tools, such as logic analysers and simulation programs. In amateur practice, alternative methods and tools must be used to address this task.

A debugging methodology has been developed for the RK, relying solely on a standard oscilloscope and multimeter (ohmmeter). By following this methodology, you can verify the functionality of individual modules and the computer as a whole or identify and localise existing faults.

Let's review the RK debugging sequence.

Step 1

Begin debugging by checking the printed circuit board assembly with an ohmmeter and correcting any detected defects. Pay special attention to verifying electrical connections between the power supply pins of the microchips (especially D22–D29, К565РУ3 RAM) and the corresponding connector contacts. The ohmmeter probes should directly touch the microchip pins to detect poor-quality solder joints. The absence of one of the supply voltages on microchips D6 (КР580ИК80А CPU), D12 (К573РФ1 character ROM), or D22–D29 (К565РУ3 RAM) may cause them to fail.

Next, ensure that the power supply provides the required voltages: +5 V ± 10% at a current of up to 1 A, +12 V ± 10% at a current of up to 200 mA, and -5 V ± 10% at a current of up to 100 mA.

Step 2

Remove microchip D17 (К573РФ5 monitor ROM) from its socket and install a ROM containing a test program. Connect pin 3 of microchip D1 (КР580ГФ24 clock generator) to the ground wire, apply power, and verify the presence of voltages on the corresponding pins of all microchips.

Step 3

Using an oscilloscope, check the presence and parameters of signals generated by microchip D1 (КР580ГФ24 clock generator):
- On pins 10 and 11: pulses with an amplitude of 12 V and a period of 562 ns.
- On pin 6: pulses with an amplitude of 5 V and a period of 562 ns.
- On pin 12: pulses with an amplitude of 5 V and a period of 62.5 ns.

The absence of these signals typically indicates a fault in the microchip or the quartz resonator.

To determine the cause of the absence of the specified signals, proceed as follows: Disconnect the OSC pin of microchip D1 (КР580ГФ24 clock generator) from the circuit board and recheck this signal using an oscilloscope. If the OSC signal appears, it indicates defects in the circuit board assembly or in microchips К155ИЕ4 (D3) or К155ИР1 (D16).

If the OSC signal is still absent, it definitively indicates a fault in the quartz resonator or the clock generator microchip.

To test the clock generator's functionality, connect a ceramic capacitor with a capacitance of 10–15 pF to pins X1 and X2 in place of the quartz resonator. If generation occurs, it confirms that the quartz resonator is faulty.

The RK can use quartz resonators with frequencies of 15–17 MHz. At these frequencies, television receiver synchronisation remains sufficiently stable, and the reliability of reading data from a tape recorder is not compromised. If a suitable quartz resonator is unavailable, it can be replaced with a trimmer capacitor or, better yet, an LC circuit. Connect a circuit consisting of a 5.6 pF capacitor and an inductor in series between pins X1 and X2. A 20 pF capacitor should be connected in parallel with the inductor. The inductor is wound on a standard core from an IF filter of an FM receiver (e.g., M100NN-SS2, 8x15), with 16 turns of PEV-1 0.2 wire.

This substitution does not degrade the computer's performance. The clock pulse frequency should be set using a frequency meter or adjusted for optimal image synchronisation on the television screen.

If any other signals generated by the clock generator are absent, disconnect the corresponding pin of microchip D1 (КР580ГФ24 clock generator) from the circuit board. If the signal appears, the fault lies either in the circuit board assembly or in the microchips receiving this signal. It is also useful to check for a high logic level on the RDY output of the clock generator microchip.

If these checks reveal that the issue is due to circuit board assembly defects, carefully inspect the printed circuit board. Regardless of the manufacturing method, solder at least the vias transitioning from one side to the other, especially those under microchips.

Most microchips used in the RK are manufactured using MOS technology and are sensitive to static electricity. Therefore, use a low-voltage soldering iron with a grounded tip, preferably connected to an operator's wrist strap.

Handle RAM microchips with particular care, as failure to follow proper assembly procedures can damage several memory cells, rendering the microchips unusable.

Experience with operating multiple RK units has shown that the clock generator is not sufficiently reliable. It is advisable to install microchip D1 (КР580ГФ24 clock generator) in a socket. For future expansion of the RK's capabilities, microchip D14 (КР580ИК55 PPI) should also be installed in a socket.

Step 4

Verify the operation of the reset signal generation circuit. Each press of the designated reset button should produce a pulse with an amplitude of 5 V and a duration of approximately 1 ms on pin 1 of microchip D1 (КР580ГФ24 clock generator).

The "single-step program execution circuit" uses SA1 to trigger a pulse via the flip-flops, which asserts RDYIN (pin 3) on the КР580ГФ24, allowing the KP580BM80A to execute one machine cycle up to T2. After T2, RDYIN is deasserted, forcing the CPU into a wait state for static signal monitoring. The STSTB signal (pin 7), referenced in "К А1 ВыВ. 7 D1," likely helps time the RDYIN pulse to align with the T2 cycle.

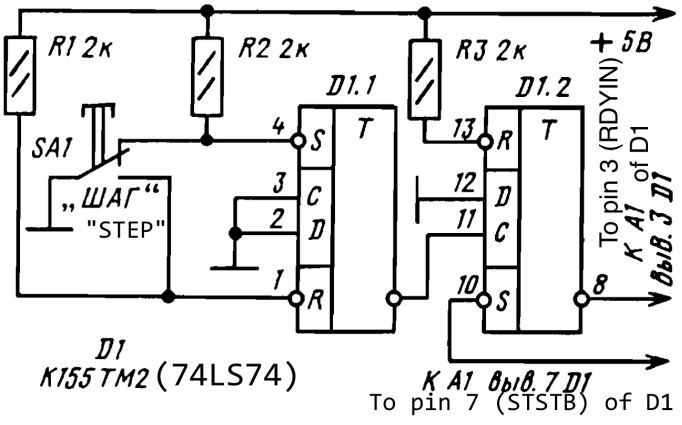
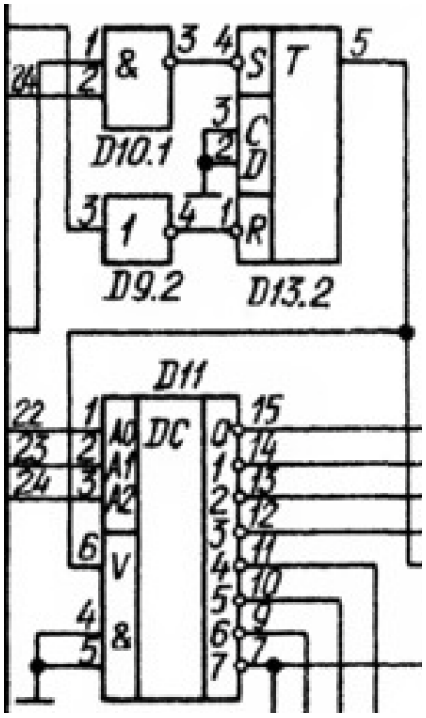


Figure 2.14 Schematic Diagram of the Single-Cycle Command Execution Unit

Step 5

Confirm the presence of a high voltage level on pin 24 of microprocessor D6 (КР580ИК80А CPU), indicating that it is in a wait state triggered by the jumper setting as described in step 2. Check the state of the RK's address and data buses by sequentially probing the corresponding pins of the microchips with an oscilloscope. All address bus lines should show a low voltage level, while the data bus lines should display the binary code 10101010, written to the zero cell of the test program.

If discrepancies are found, check for short circuits between address bus lines and other signal lines or power supply lines. Verify the functionality of ROM D17 (К573РФ5 monitor ROM), the initial reset circuit consisting of microchips D10.1 (К155ЛА3), D9.2 (К155ЛН1) and D13.2 (К155ТМ2), and decoder D11 (К555ИД7). A low voltage level on pin 18 of microchip D17 (К573РФ5 monitor ROM) indicates proper decoder operation. After correcting any identified faults, repeat the debugging steps 4 and 5.



Step 6

Turn off the power supply, remove the previously installed jumper, connect the single-step program execution circuit for the microprocessor, and power on the RK again (see Figure 2.14).

Pressing the "ШАГ" (STEP) button once causes the microprocessor to enter a wait state after executing the T2 cycle of each machine cycle, allowing all signals to be monitored in static mode.

Step 7

Apply the "СБРОС" (RESET) signal and monitor the execution of the first 11 commands to identify any faulty microchips.

With each press of the "ШАГ" (STEP) button, monitor the state of the address, data, and control buses according to Table 2.3. As noted, when fetching the first (single-byte) command from the ROM, the data bus displays the code 10101010. The next ROM cell contains the code 01010101. These two codes are used to test the data bus. The third command (lines 3–5) is an unconditional

jump to address F805H. After pressing the “ШАГ” (STEP) button three times (this command takes three machine cycles), the initial startup circuit should activate, and a high voltage level should appear on pin 5 of flip-flop D13.2 (K155TM2). The next four commands (lines 6–17) configure the programmable peripheral adapters (PPA) D14 and D20 (КР580ИК55). To display the test program’s results, we will use PPA D14.

The code combination 01010101 appears next. Executing the following two commands (lines 24–30) lights up the “РУС/ЛАТ” (RUS/LAT) LED, confirming the functionality of microchip D20 (КР580ИК55 PPI).

Table 2.3

Line	Address	Data	RD	WR	Command	Comment
1	0000	AA	0	1		Data bus check
2	0001	55	0	1		
3	0002	C3	0	1	JMP	Jump to program start
4	0003	05	0	1	05	
5	0004	F8	0	1	F8	
6	F805	3E	0	1	MVI	Configure port
7	F806	84	0	1	A,8AH	
8	F807	32	0	1	STA	Keyboard (D20)
9	F808	03	0	1	03	
10	F809	80	0	1	80	
11	8003	84	0	1		Write to port
12	F80A	3E	0	1	MVI	Configure additional port
13	F80B	80	0	1	A,80H	
14	F80C	32	0	1	STA	
15	F80D	03	0	1	03	(D14)
16	F80E	A0	0	1	A0	
17	A003	80	0	1		Write to port
18	F80F	3E	0	1	MVI	Output test signal
19	F810	55	0	1	A,55H	
20	F811	32	0	1	STA	to channel
21	F812	01	0	1	01	of microchip
22	F813	A0	0	1	A0	D14
23	A001	55	1	1		Write to port
24	F814	3E	0	1	MVI	Light “RUS/LAT” LED
25	F815	08	0	1	A,08H	
26	F816	32	0	1	STA	
27	F817	02	0	1	02	
28	F818	80	0	1	80	
29	8002	08	1	1		Write to port
30	F819	AF	0	1	XRA A	

Turn off the power supply and disconnect the single-cycle operation unit. Further debugging and testing of the keyboard, RAM, and display unit will be conducted with the RK operating automatically under the test program.

Step 8

Turn on the power supply. Press the “СБРОС” (RESET) button, and after the sound signal ends, press the “РУС/ЛАТ” (RUS/LAT) key. These actions initiate the RAM test program. If microchips D22–D29 are functioning correctly, the test program will complete with a sound signal, and the VD2 LED will light up. If there are faulty microchips, the RK will indicate this with two sound signals (the VD2 LED should not light up in this case) and will generate high voltage levels on the

lines of Channel B of the PPA D14, corresponding to the data bus bits connected to the faulty RAM microchips.

The cause of a malfunction may be defects in the microchips or improper operation of the program.

First, verify the functionality of the signal generators for RAS and CAS (D16, К155ИР1) or multiplexers D18 and D19 (К555КП11).

To do this, check the presence and shape of signals at the RAS, CAS, and WE inputs of the memory microchips and at the V inputs of address multiplexers D18 and D19 (see Figure 2.15). Note that the CAS signal becomes active (0) only in the presence of a reset signal from the “РУС/ЛАТ” (RUS/LAT) key.

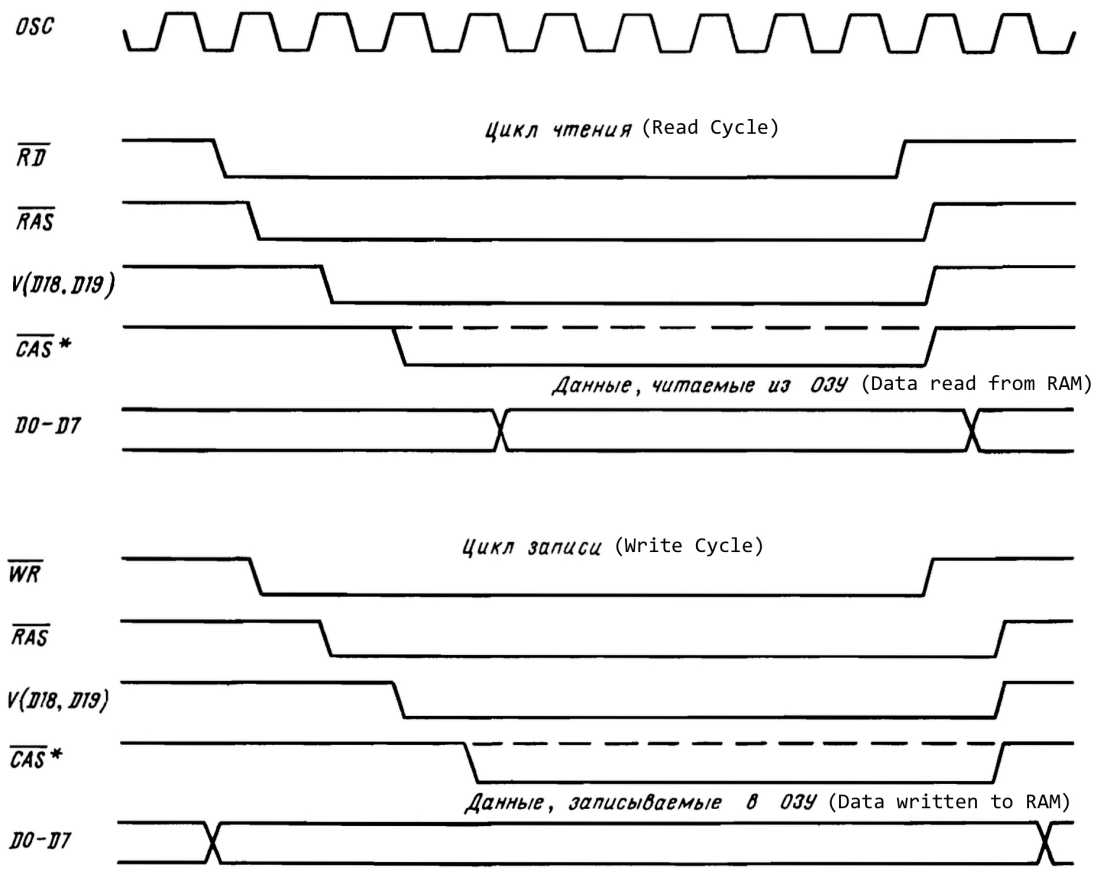
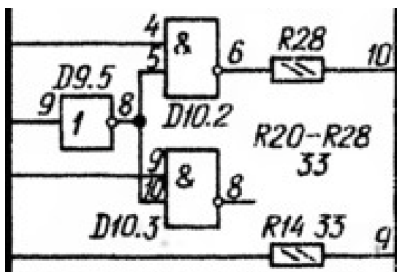


Figure 2.15. Timing Diagram of Signals During RAM Read and Write Operations

Note that the test program only checks the RAM located at addresses 0000H–3FFFH. To test additional RAM, the signal from the output of D10.2 (К155ЛА3) must be applied to the corresponding pins of its microchips. Testing of other RK components is only possible with fully functional RAM.



Step 9

Verify the functionality of the display unit and the DMA controller by pressing the “СБРОС” (RESET) button and, after the sound signal ends, the “УС” (US) key. This command causes the test program to clear the screen area of the RAM, initialise the DMA and display controllers, and place the cursor in the upper-left corner of the screen. If this does not occur, use an oscilloscope to check the display controller’s ability to generate the “DMA Request” signal on pin 17 of integrated circuit D2 (КР580ИК57 DMA controller), as well as the presence of “Request” and “DMA Acknowledge” signals on pins 13 and 21 of microprocessor D6 (КР580ИК80А CPU). Then, ensure that the display controller generates line and frame synchronisation pulses with periods of 64 μs (HRTC) and 20 ms (VRTC), respectively.

If all these signals are generated, the cause of the malfunction may be the absence of the “Display Disable” signal (VSP), which becomes active during frame and line synchronisation pulses and inter-line intervals, or defects in the components of the video signal generation circuit.

In a fully functional display unit, pressing the “УС” (US) key each time initiates the output of alphanumeric characters to the screen. Correct display of these characters confirms the functionality of the character generator ROM and the shift register.

Step 10

Finally, verify the operation of the keyboard. To do this, press the “СБРОС” (RESET) button and the “СС” (SS) key, then press each of the remaining keys in sequence and ensure that the displayed characters correspond to the keys pressed.

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