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**MAINTENANCE MANUAL**





## **COMMUTER MAINTENANCE MANUAL**

**Visual Technology Incorporated  
540 Main Street  
Tewksbury, MA 01876**

### **FCC STATEMENT**

The Commuter Portable Computer has been certified to comply with the FCC limits set for a Class B computing device, pursuant to Subpart J of Part 15 of FCC Rules. Only peripheral devices (computer input/output devices, terminals, printers, etc.) certified to comply with the Class B limits may be attached to this computer. Operation with noncertified peripheral devices is likely to result in interference with radio and television reception.

Part Number: MM1083-001-00A

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## PREFACE

This manual is written for electronic service personnel who have been trained in the maintenance and repair of the Visual Commuter system. Its intention is to provide all of the information required to perform the following maintenance procedures.

- Isolate hardware faults to the subassembly level.
- Replace any of the subassemblies.
- Install any of the available system options.

The Visual Commuter Maintenance Manual contains five chapters.

**Chapter 1, Introduction**, describes the Commuter system and provides a functional overview.

**Chapter 2, Fault Diagnosis**, describes the diagnostics and other tools required for fault diagnosis. Procedures for locating faulty subassemblies are also provided.

**Chapter 3, Subassembly Replacement**, contains detailed illustrations showing subassembly removal and replacement procedures.

**Chapter 4, System Upgrade**, provides information for installing the various options available for the Commuter system.

**Chapter 5, Theory of Operation**, contains circuit descriptions. This information may be used for component level troubleshooting.

## RELATED INFORMATION

Technical information for the Visual Commuter system includes the following elements:

- Visual Commuter Operator's Guide
- Visual Commuter Maintenance Manual
- An Introduction to the Visual Commuter (A video tape)



# CHAPTER 1

## INTRODUCTION

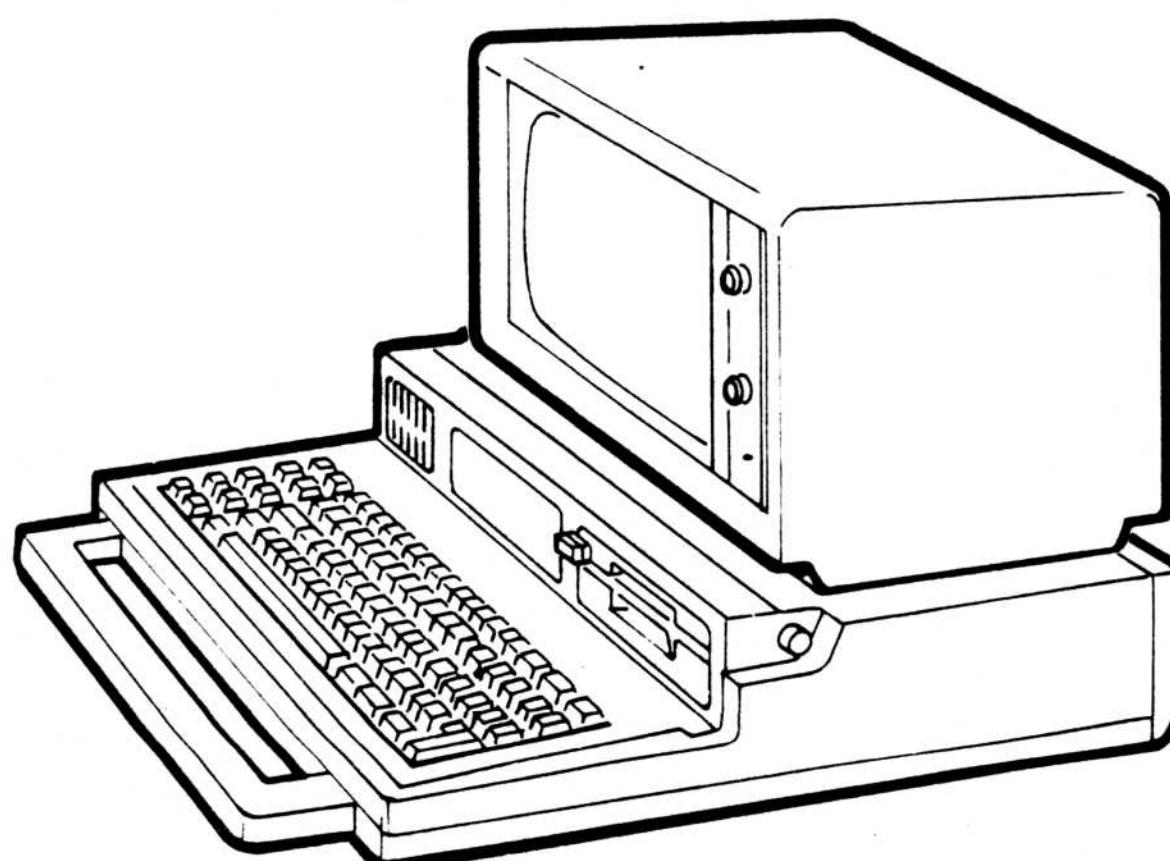
### 1.1 GENERAL DESCRIPTION

The Visual Commuter system is a portable, IBM compatible, personal computer. A typical Commuter system is shown in Figure 1-1. This briefcase size system contains the following major features:

- MS-DOS operating system and GW Basic.
- 16-bit 8088 processor.
- 128K bytes of memory (expandable to 512K bytes).
- Diskette controller that supports two 5 1/4" drives.
- One 5 1/4" diskette drive (double sided, double density).
- ROM-based power-up self-test and BIOS.
- ROM-based and disk-based diagnostics.

In addition, the Commuter system supports the following optional devices:

- An 80 column by 16 line flat panel, LCD display.
- An 80 column by 25 line flat panel, LCD display with graphics capabilities
- A monochrome or color monitor.
- An additional 5 1/4" disk drive.
- An 8087 numerical coprocessor.
- A programmable, synchronous/asynchronous serial port.
- IBM expansion chassis with 10 MB hard disk.



**Figure 1-1. A Typical Commuter System with Optional Monitor**

### 1.1.1 Configurations

The Commuter system may be reconfigured by adding certain options to the base level configuration.

The base level configuration includes the following hardware components:

- An 8088 CPU (central processing unit).
- 128K bytes of RAM (random access memory).
- An integrated keyboard.
- One 5 1/4" disk drive.
- A parallel printer port.
- An asynchronous serial communication port.

Any or all of the following hardware options may be added to the base level configuration:

- A second 5 1/4" disk drive.
- An 80 × 16 flat panel LCD (liquid crystal display).
- Additional RAM (up to 512K bytes).
- An 8087 numerical coprocessor.
- An RS-232-C programmable synchronous/asynchronous serial port.

A switch pack on the system PCB is used to set the system configuration.

### 1.1.2 Controls, Connectors, and Switch Settings

All controls and connectors required for normal operation are accessible from the outside of the Commuter system (see Figure 1-2).

One switch pack with eight switches is located under the disk drive platform on the system PCB. The switch settings are described in Figure 1-3.

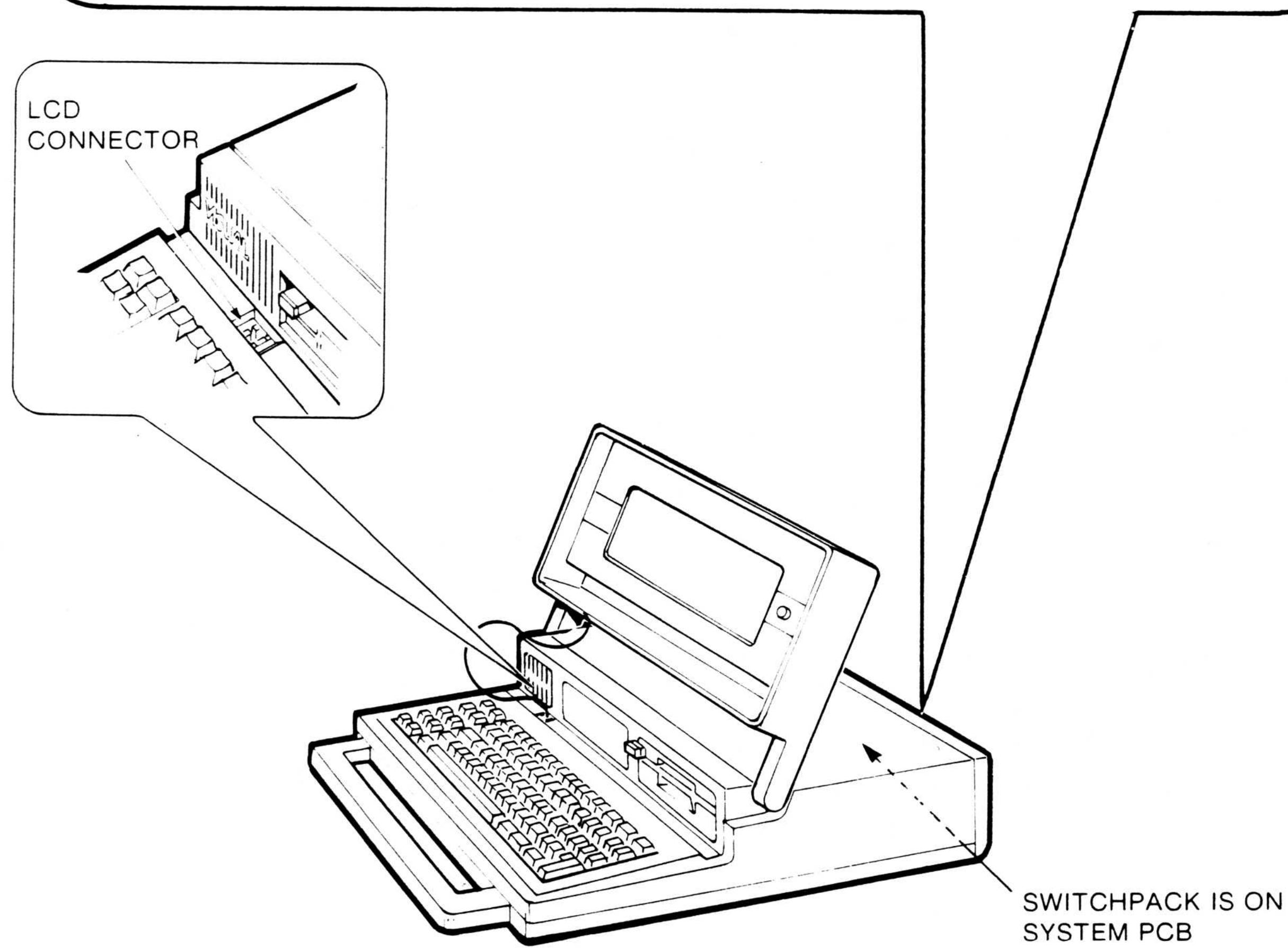
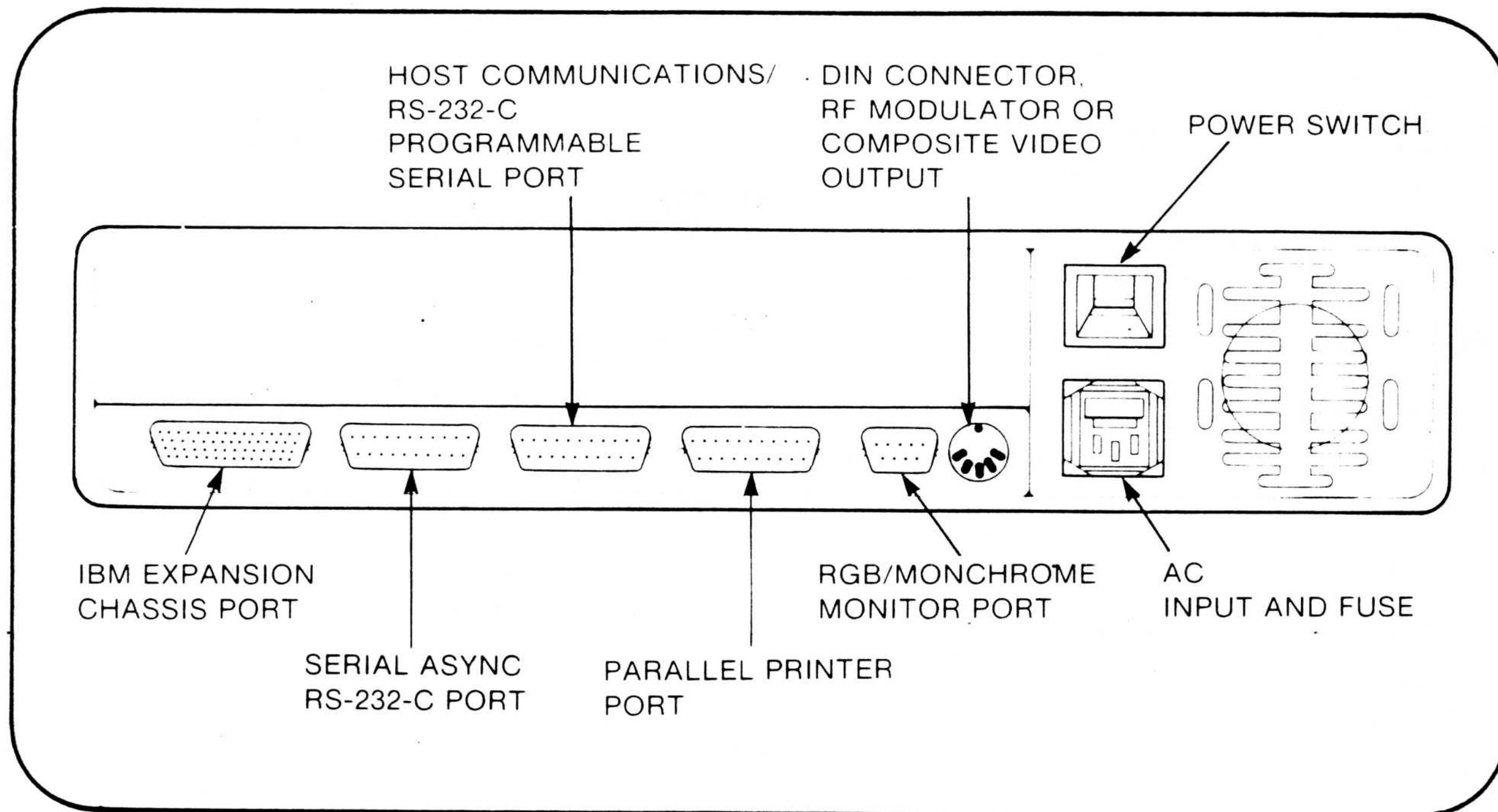
**Keyboard:** the low profile, IBM-type keyboard has 83 keys and is integrated with the system chassis. The following features are provided:

- 10 function keys
- Numeric "calculator" keypad
- Indicator lights for CAPS and Numeric Lock

**Expansion chassis port:** used to connect the IBM expansion chassis to the Commuter system. The expansion chassis allows for the use of expansion cards designed for the IBM Personal Computer. A 10 MB hard disk drive unit may be available with the chassis.

**ASYNC port:** an IBM-type asynchronous serial port for use in communications.

**Host communications port:** inactive with standard equipment. With PCB modification, this fully programmable, RS-232-C port can be activated to support ASYNC, BISYNC, SDLC, and HDLC communications.



**Figure 1-2. Locations of Controls and Connectors**

**Parallel printer port:** equipped with a Centronics parallel interface that supports most parallel printers.

**RGB/Monochrome monitor port:** designed for connection with either colorgraphics or IBM-compatible, high resolution, monochrome monitors.

**Composite video output port:** a 5-pin DIN port designed for connection to either RF modulators; for use with home televisions or composite data input monitors.

**Power switch:** a rocker-type switch used to power-on the Commuter system.

**Power receptacle:** an IEC-type power connector with built-in fuse.

**Switch pack:** the eight switches on the switch pack are set according to the system configuration that is used. Switch settings reflect the following configurations:

- The number of disk drives.
- The type of display used.
- Amount of memory installed.
- Whether a numeric coprocessor is installed.

Specific switch settings are described in Figure 1-3. Note that switches S5 and S6 (these switches set the system default for the display type used) can be temporarily overridden by entering certain key sequences.

#### NOTE

**The temporary override of switches terminates when the Commuter system is turned off or rebooted (Hold CTRL and ALT and press DEL).**

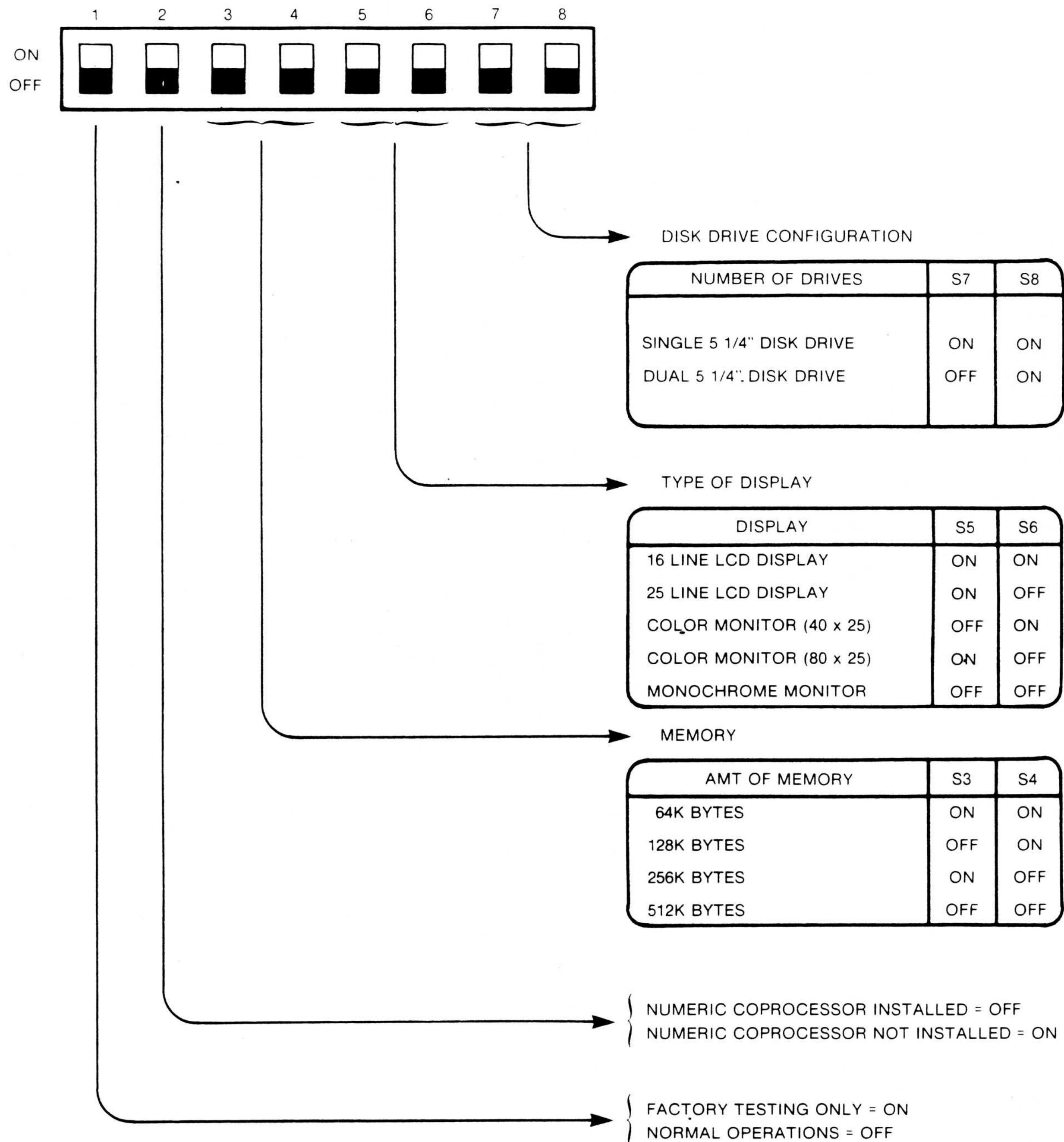
The following display types can be temporarily selected by entering the corresponding keystrokes:

- |                         |  |
|-------------------------|--|
| • 40 by 25 colorgraphic | Hold <b>CTRL</b> and <b>ALT</b> and press <b>4</b> |
| • 80 by 25 colorgraphic | Hold <b>CTRL</b> and <b>ALT</b> and press <b>8</b> |
| • IBM monochrome        | Hold <b>CTRL</b> and <b>ALT</b> and press <b>M</b> |
| • 16 line LCD display   | Hold <b>CTRL</b> and <b>ALT</b> and press <b>L</b> |
| • 25 line LCD display   | Hold <b>CTRL</b> and <b>ALT</b> and press <b>8</b> |

## 1.2 SYSTEM ARCHITECTURE

This section provides a general overview of the system architecture. The Commuter system block diagram in Figure 1-4 highlights functional relationships between various system devices.

A more detailed discussion of the system components is provided in Chapter 5 (Theory of Operation).



**Figure 1-3. Switchpack Switch Settings**

### **1.2.1 The Central Processing Unit (CPU)**

The Commuter system is based on an Intel 8088 microprocessor that is operated in maximum mode. Thus bus control is delegated to an 8288 bus controller. This frees the CPU for controlling extended system features.

System I/O devices are served by an 8259 programmable interrupt controller. The controller provides eight levels of vectored interrupts.

Four prioritized DMA channels are provided by an 8237 DMA controller. Memory refresh, the floppy disk controller and two expansion chassis channels are supported by the controller.

### **1.2.2 System Memory**

The Commuter system supports one megabyte of fully addressable memory space. A memory map (see Figure 1-5) illustrates the allocation of memory space.

Random access memory is made up of DRAM (dynamic random access memory) devices. Three configurations are supported:

- 128k bytes
- 256k bytes
- 512k bytes

Video RAM is implemented in two 64k byte by four-bit devices. 4k bytes are required for monochrome applications; 16k bytes are required for colorgraphics applications.

The BIOS (basic input output system) is stored in ROM (read only memory). The top 64k bytes of system memory space is allocated to the BIOS.

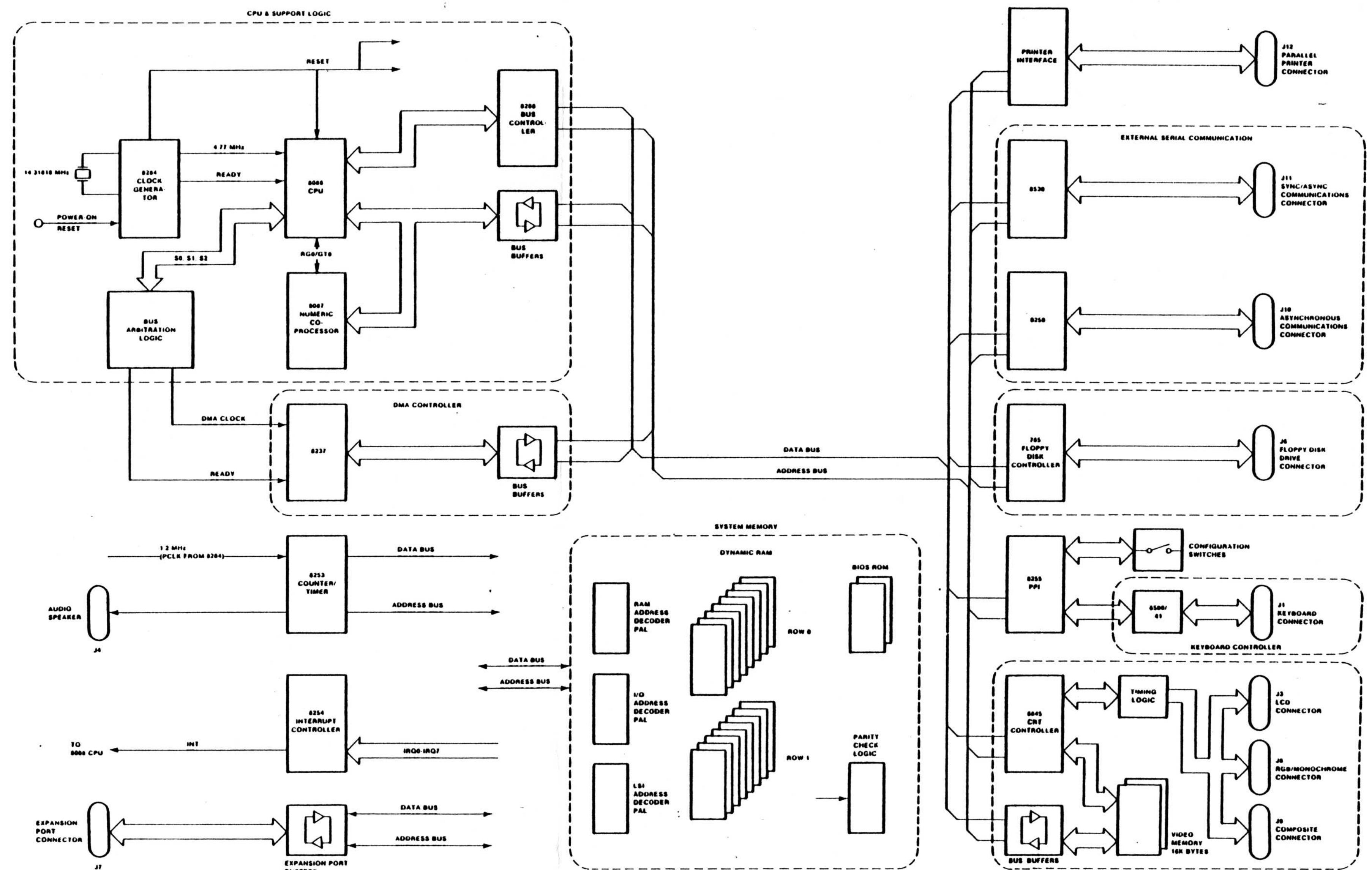
### **1.2.3 System I/O**

Seven I/O channels are supported by the Commuter system:

- Video output ports
- Keyboard
- Floppy disk
- Asynchronous serial communication port
- Synchronous/Asynchronous serial communication port
- Parallel printer port
- Expansion port

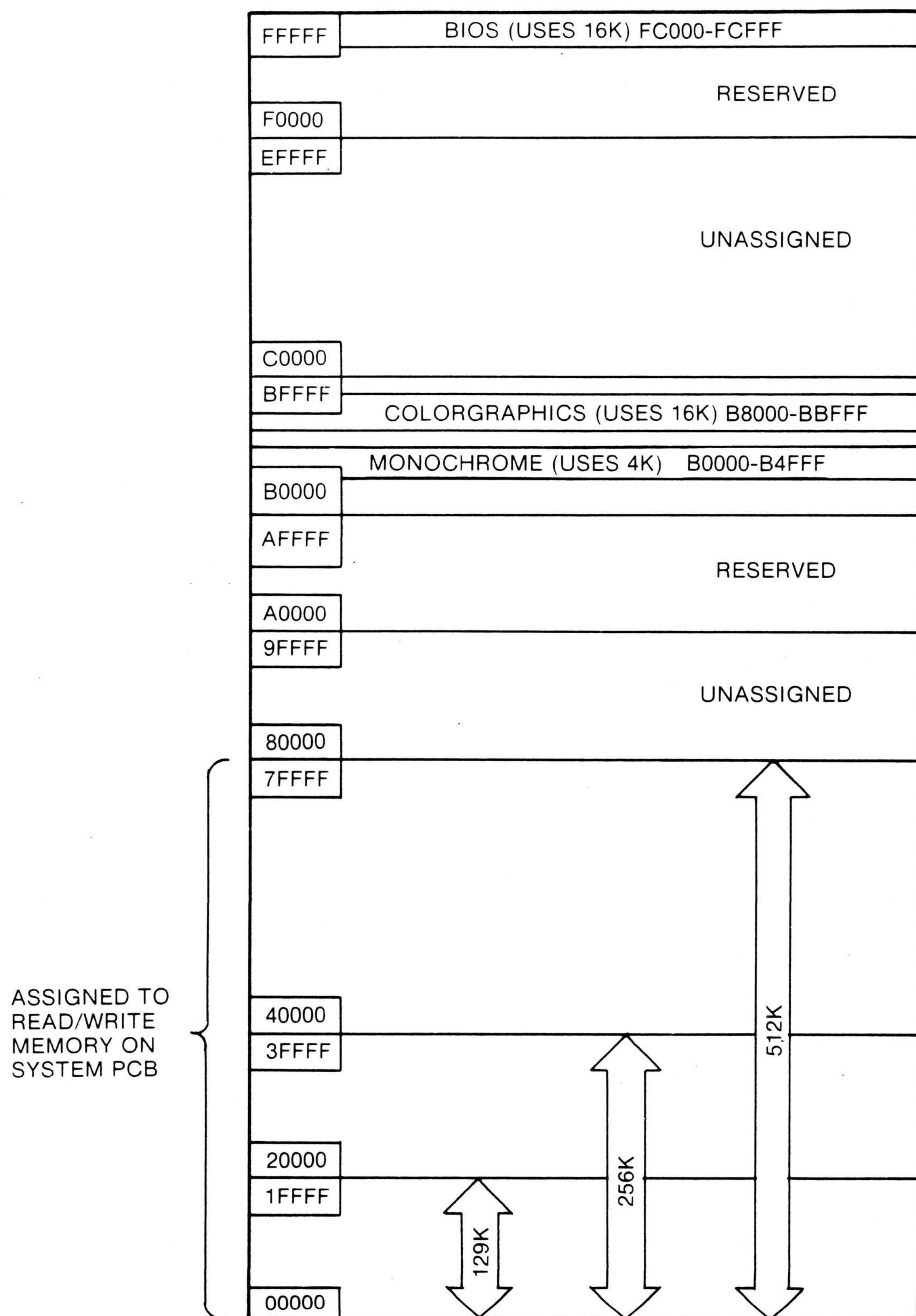
## **1.3 SYSTEM PCB**

The electronic circuitry of the Commuter system is primarily contained on a single system PCB (printed circuit board). Figure 1-6 shows the system PCB, the major devices and connectors.

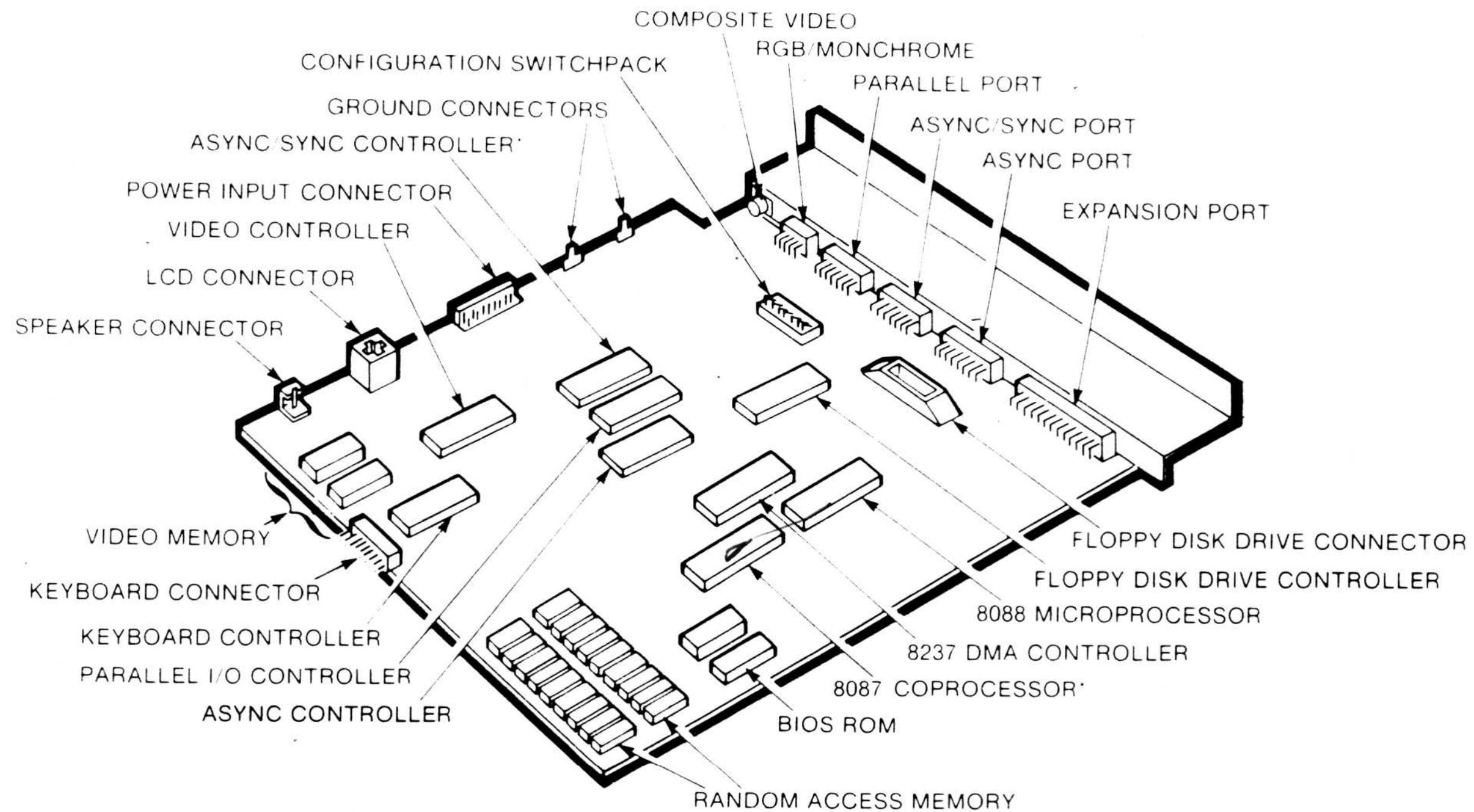


**Figure 1-4. Commuter System Block Diagram**





**Figure 1-5. Commuter Memory Map**



\*OPTIONAL DEVICE

**Figure 1-6. Commuter System PCB Layout**

The system PCB is of multilayer construction. Signals are on the outside layers, voltage and ground are on the two inside layers. All of the d.c. voltages required (+12, +5, -5 and GND) are supplied via connector J5.

## 1.4 EQUIPMENT SPECIFICATIONS

The following specifications identify storage, transport and operational constraints for the Commuter system.

### 1.4.1 Physical Specifications

#### Dimensions

- Height      3.5 in.
- Width      18.0 in.
- Length      15.5 in.

#### Unit Weight

- With one floppy disk drive      15 lbs.
- With two floppy disk drives      18 lbs.
- Addition of LCD display increases unit weight by 2 lbs.

#### **1.4.2 Electrical Specifications**

##### **Input Voltage (Jumper Selectable):**

- 90 V to 130 V (115 V nominal) or
- 180 V to 260 V (230 V nominal).

##### **Input Frequency:**

47 - 63 Hz

##### **Line Fuse Rating:**

2A, 250 V

##### **Power Dissipation:**

35 W

##### **Reliability:**

- MTBF        10,000
- MTTR        30 Minutes
- Data Integrity
  - $10^{-9}$  Soft Error
  - $10^{-12}$  Hard Error
  - $10^{-6}$  Seek Error

##### **Power Cord**

- Length       5 ft. 0 in.
- Gauge        18 AWG

#### **1.4.3 Environmental Specifications**

##### **Temperature:**

- Operating      4 to 40 C
- Storage       -20 to 60 C

##### **Humidity:**

- Operating      20% to 80% (no condensation)
- Storage       90% or less

**Altitude:**

- Operating 87 mm. Hg

**Vibration:**

- Operating 5 to 60 Hz, 0.6 G
- Storage/Transportation 5 to 60 Hz, 3.0 G or less

**Impact (Shock):**

50 G or less, 2 msec. Half sine pulses, once on each of the six surfaces.

## **CHAPTER 2**

## **FAULT DIAGNOSIS**

### **2.1 INTRODUCTION**

This chapter contains the information required to isolate hardware faults to the subassembly level. The following information is provided:

- Identification of replaceable subassemblies.
- Descriptions of the various diagnostic tools available.
- Procedures for using the diagnostic tools.

#### **2.1.1 Philosophy**

The maintenance philosophy for the Commuter system is based on replacement of the faulty subassembly(ies).

#### **2.1.2 Replaceable Subassemblies**

The main subassemblies for the Commuter system are as follows:

- System PCB
- Keyboard assembly
- Power supply
- Disk drive unit(s)\*
- LCD display\*

Part numbers for subassemblies and for other items such as wiring harnesses and interconnecting cables are contained in the SERVICE AND SUPPORT POLICIES AND SPARE PARTS PRICING documentation.

#### **2.1.3 Required Tools and Test Equipment**

The following tools and test equipment are needed to perform the maintenance procedures described in this chapter:

- ROM-based power-up self-test
- ROM-based extended diagnostics
- Disk-based diagnostic exercisers

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\*Certain subassemblies such as a second disk-drive unit and an LCD display are options that may not be present on some Commuter system configurations.

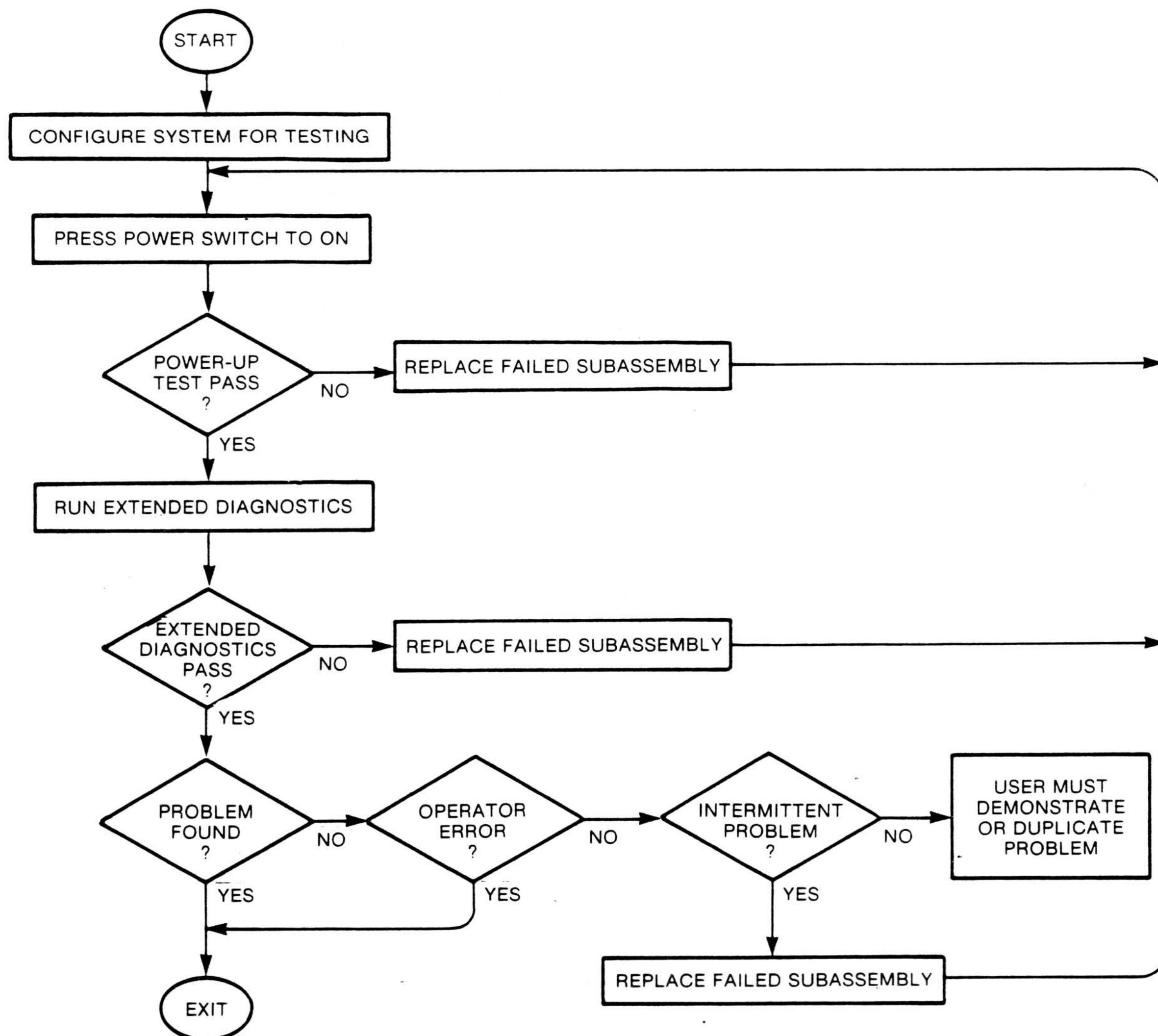
- Communications loopback test connector
- Volt/ohm meter
- RGB or composite color monitor

## 2.2 TROUBLESHOOTING OVERVIEW

The troubleshooting procedures comprise two basic steps.

1. Pass the power-up self-test.
2. Successfully execute ROM-based and disk-based extended diagnostics.

The flow diagram (see Figure 2-1) illustrates the approach used to diagnose and correct system problems.



**Figure 2-1. Flow Diagram for Using Diagnostic Procedures**

## **2.3 TROUBLESHOOTING TIPS**

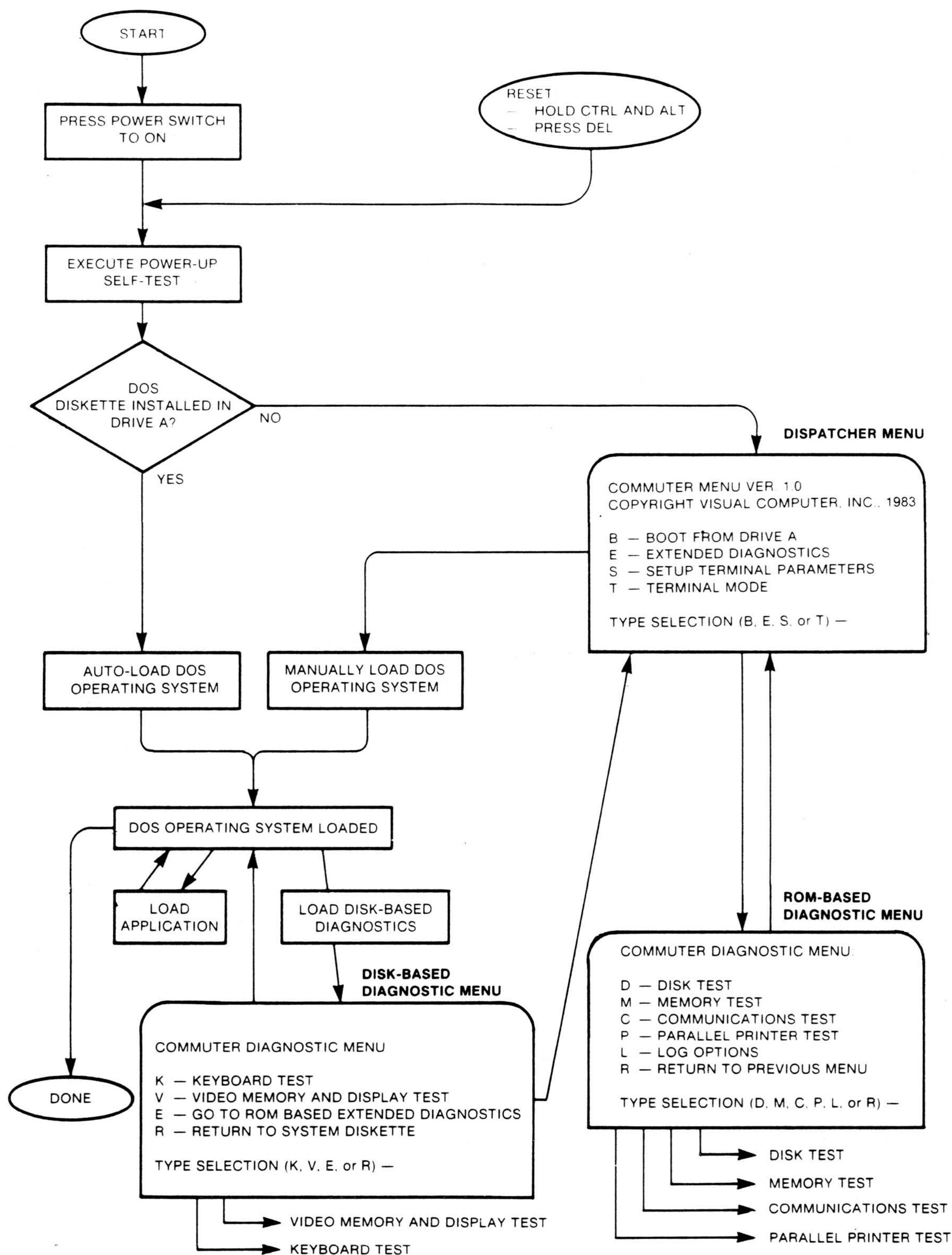
The following tips are provided to help make the troubleshooting process more efficient:

- Make sure the problem(s) can be demonstrated (if possible) before diagnosing the fault. A clear understanding of the symptom(s) is important.
- Always look for the obvious:
  - Power cord
  - Fuses
  - Cable connections
  - Operator error
- Run all extended diagnostics starting with those most likely to identify the particular problem.
- For some symptoms several remedies may be suggested. Try the remedies in the order that they are suggested.
- Redundant components such as disk drive units or cables may be interchanged to isolate faults.
- When video capabilities are limited, audio responses such as fan noise and coded "beep" tones provide important indications on system operation. In some cases, test results may be output to a recording device (see Section 2.8).
- Do not overlook possible problems in the customer's environment such as power fluctuations, interference from other equipment, operating temperature and so on.
- When symptoms can not be duplicated, that is, the fault seems to have disappeared, suspect the following.
  - An intermittent fault exists.
  - The operator has made an error or misinterpreted symptoms.

## **2.4 HOW TO INVOKE DIAGNOSTICS**

Figure 2-2 illustrates the paths available to run the self-test and to invoke the various diagnostic menus. Note the following:

- The power-up self-test is executed each time the system is turned on or reset.
- ROM-based diagnostics may be invoked without the operating system being loaded.
- To invoke the disk-based diagnostics, it is necessary to load the operating system (DOS).



**Figure 2-2. Invoking Diagnostic Menus**

#### **2.4.1 Invoking the ROM-Based Diagnostic Menu**

To invoke the ROM-based diagnostic menu:

1. Boot the system with no DOS disk installed so that the dispatcher menu is displayed (refer to Section 2.6).
2. Select (type) E from the dispatcher menu.

The ROM-based diagnostic menu may also be invoked from the disk-based diagnostic menu.

#### **2.4.2 Invoking the Disk-Based Diagnostic Menu**

To manually invoke the disk-based diagnostic menu:

1. Boot the system with no DOS disk installed so that the dispatcher menu is displayed (refer to Section 2.6).
2. Load the operating system manually.\*
  - Insert the DOS diskette in drive A.
  - Select (type) B from the dispatcher menu.
3. Load the disk-base diagnostics (DIAG.COM) into memory.
  - Type DIAG then press RETURN.
  - Verify the system configuration that is displayed by pressing RETURN. The system configuration display reflects the switch settings of the switchpack on the system PCB.

### **2.5 TEST CONFIGURATION**

To fully test the Commuter system, it is desirable to interconnect the full configuration shown in Figure 2-3. Note, however, that certain types of problems (such as a faulty keyboard) may be effectively diagnosed without the full configuration.

### **2.6 THE POWER-UP SELF TEST**

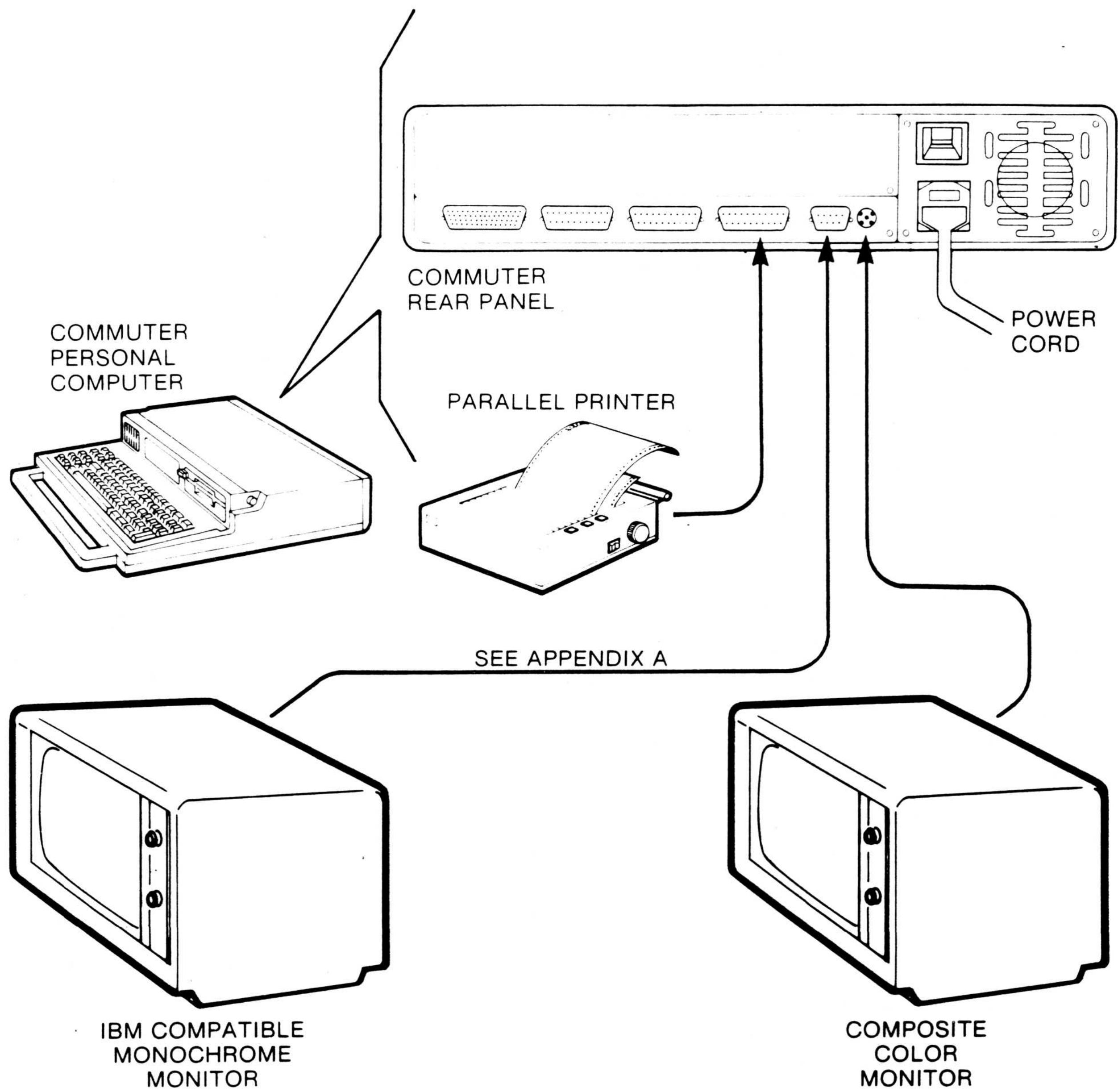
The power-up self-test executes each time the Commuter system is turned on or reset. The self-test takes 5 – 40 seconds depending on the amount of memory installed and exercises approximately 90 percent of the logic.

To execute the power-up self-test and display the dispatcher menu (refer to Figure 2-2):

1. Configure the Commuter system as shown in Figure 2-3 (do not insert any disks at this time).
2. Press the power switch to the ON position. If the system is already on, it may be reset by holding **Ctrl** and **Alt** and pressing **Del**.

---

\*If the DOS diskette is installed in drive A, the DOS operating system may load automatically when the system is powered up or rebooted (Hold **CTRL** and **ALT** and press **DEL**).



**Figure 2-3. Typical Test Configuration**

Expect the following responses:

- The fan turns on.
- One short audio “beep” tone is sounded (5 to 40 seconds after the system is turned on).
- The dispatcher menu is displayed.

If the Commuter system performs as expected, go to section 2.7 and continue the extended diagnostic procedures indicated.

If the Computer system fails to perform as expected, continue with the diagnostic procedures in this section. The following sections are provided:

- 2.6.1 Power Problems
- 2.6.2 Audio Alarm Tones
- 2.6.3 Self-Test Error Messages

#### **NOTE**

**When a self-test error message is displayed, it may be possible to proceed from the error by typing *CTRL P*. Extended diagnostics may then be used to further define the problem.**

##### **2.6.1 Power Problems**

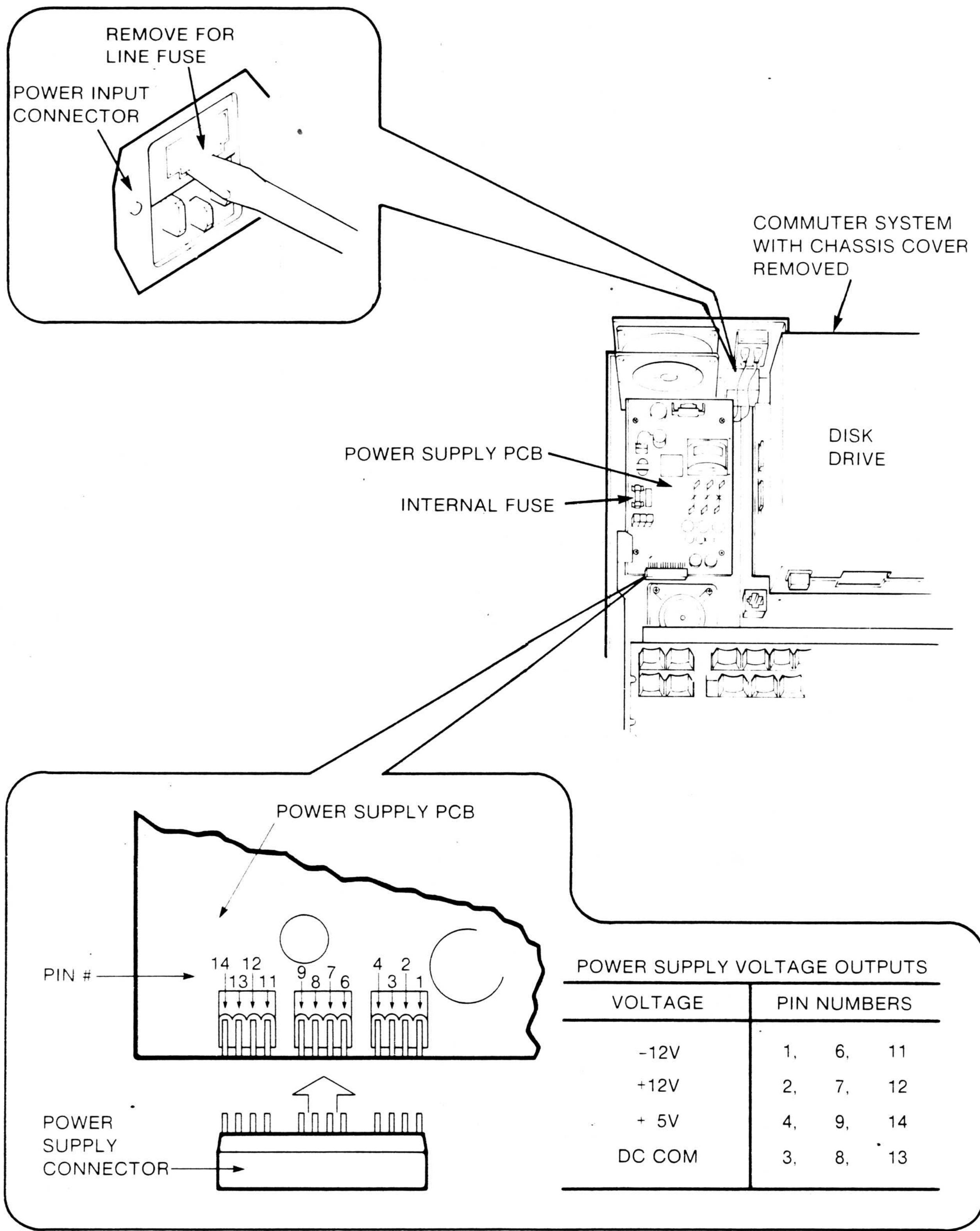
Refer to Table 2-1 when power indications are absent. Power indications include the following:

- The fan turns on
- Audio tone(s) and video are present.

The table describes various symptom(s) and suggests procedures to correct the apparent problem.

**Table 2-1. Power Problems and Suggested Corrective Procedures**

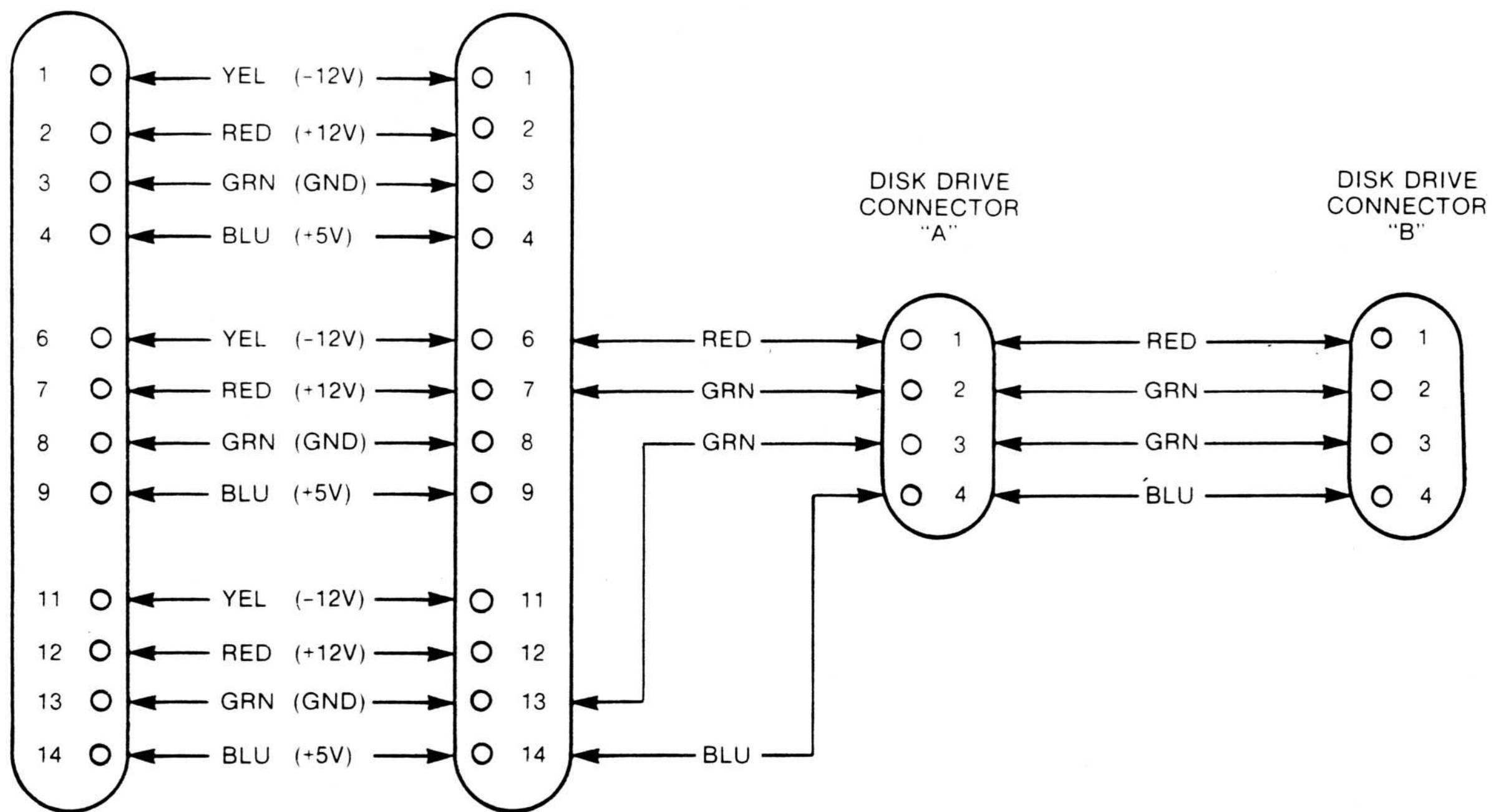
Symptom(s)	Suggested Corrective Procedure(s)
No signs of power: — No fan — No audio tone(s) — No video	<ul style="list-style-type: none"><li>• Check the power switch. Verify that the system is turned on</li><li>• Make sure that both ends of the power cord are properly connected.</li><li>• Check for proper power at the electrical socket by plugging a lamp into it.</li><li>• Check the line fuse (refer to Figure 2-4). Replace if blown.</li><li>• Verify the power cord by measuring the voltage at the device end of the cord.</li></ul>
Fan is on	
No audio	
No video	<ul style="list-style-type: none"><li>• Check the internal fuse (refer to Figure 2-4). Replace if blown. If it blows again, replace the power supply.</li><li>• Check the test points shown in Figure 2-4 for the proper voltage. If any of the voltages are missing, replace the power supply.</li><li>• Check the continuity of the power supply cable (see Figure 2-5). If the cable is damaged or open, replace the cable.</li><li>• Replace the system PCB</li></ul>



**Figure 2-4. Locations of Line Fuse, Internal Fuse and Voltage Test Points**

POWER SUPPLY  
CONNECTOR

SYSTEM PCB  
CONNECTOR



**Figure 2-5. Power Supply Cable Schematic**

### 2.6.2 Audio Alarm Tones

Refer to Table 2-2 when audio alarm tones are sounded after the power-up self-test. The table indicates the probable cause of the alarm tones and suggests procedures to correct the apparent problem.

**Table 2-2. Alarm Tones and Suggested Corrective Procedures**

Alarm Tones Sounded	Probable Cause	Suggested Corrective Procedure(s)
One long one short	8237 (U64) DMA controller read/write test failed.	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>
One long two short	8253 (U113) counter 1 (memory refresh) not counting.	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>
One long three short	Error in 1st 16K bytes of RAM.	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>
One long four short	8259 (U86) interrupt controller test failed.	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>
One long five short	6845 (U95) CRT controller test failed or vertical and horizontal retrace bits in CRT status register (at port address 3DAH) not toggling.	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>
One long six short	Video memory (U144, U145) test failed.	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>

### 2.6.3 Self-Test Error Messages

Refer to Table 2-3 when the video monitor displays an error message after the power-up self-test. The table lists each error message alphabetically, indicates a probable cause of the error message and suggests corrective procedures.

#### NOTE

**It may be possible to proceed from a self-test error by typing *CTRL P*. Extended diagnostics may then be used to further define the problem.**

**Table 2-3. Error Messages and Suggested Corrective Procedures**

Error Message/Probable Cause	Suggested Corrective Procedure(s)
<b>** COM1 ERR</b> 8250 (U72) async controller read/write test or internal loopback test failure.	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>

**Table 2-3. Error Messages and Suggested Corrective Procedures (Cont.)**

Error Message/Probable Cause	Suggested Corrective Procedure(s)
<b>** DISK ERR</b>  Floppy disk controller, drive motor, or seek problem.	<ul style="list-style-type: none"> <li>• Check for obstruction in drive.</li> <li>• Check electrical connections to drive (refer to Figure 2-5). Replace drive power cable if necessary.</li> <li>• Replace disk drive.</li> <li>• Replace (ribbon) cable.</li> <li>• Replace system PCB.</li> </ul>
<b>** I/O PARITY CHECK</b>  I/O channel parity error detected. Possible memory parity chip problem	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>
<b>** KEYBD ERR</b>  Keyboard self-test failure.	<ul style="list-style-type: none"> <li>• Check for stuck keys</li> <li>• Replace keyboard cable.</li> <li>• Replace keyboard.</li> <li>• Replace system PCB.</li> </ul>
<b>** LPT1 ERR</b>  Parallel port register read/write test failure.	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>
<b>** MEM PARITY CHECK - ssss</b>  Detected memory parity error in segment ssss.	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>
<b>** RAM ERROR - ssss:oooo=xx</b>  Memory test (including video memory) detected error at segment ssss, offset oooo. "xx" (hex) is the XOR (exclusive OR) between expected and actual data (the data bits in error are shown as ones).	<ul style="list-style-type: none"> <li>• Check switchpack switch settings.</li> <li>• Replace system PCB.</li> </ul>

**Table 2-3. Error Messages and Suggested Corrective Procedures (Cont.)**

Error Message/Probable Cause	Suggested Corrective Procedure(s)
<b>** ROM ERR - ssss</b> ROM checksum test error at segment ssss.	<ul style="list-style-type: none"> <li>Replace system PCB.</li> </ul>
<b>** SYS TIMER ERR</b> 8253 (U113) (counter 0) is not counting at the correct interval.	<ul style="list-style-type: none"> <li>Replace system PCB.</li> </ul>
<b>** UNEXP INT - nn</b> Received an unexpected interrupt from level nn. Possible device controller problem.	<ul style="list-style-type: none"> <li>Replace system PCB.</li> </ul>

## 2.7 EXTENDED DIAGNOSTICS

This section identifies some general requirements for various extended diagnostic tests. More specific information regarding execution and error messages is located in section 2.9.

Two types of extended diagnostics are provided with the Computer system.

- ROM-based diagnostics execute outside (without) the DOS operating system.  
The ROM-based diagnostic tests have been designed to thoroughly test, over an extended period of time, the specific area chosen by the technician. The tests run continuously until terminated by the technician.
- Disk-based diagnostics are on the DOS diskette and require the operating system in order to execute.  
Disk-based diagnostics are interactive hardware exercisers that require operator input to execute. The operator must verify (usually by pressing RETURN or other keys) various screens that are displayed as the tests proceed.

Table 2-4 lists individual tests, identifies the location of each and specifies additional requirements.

### NOTE

**Extended diagnostic tests may not execute successfully unless the power-up self-test has passed.**

**Table 2-4. Extended Diagnostic Test Locations and Requirements**

Test	Location	Requirements
Disk	ROM	Formatted scratch diskette in the drive to be tested. This test may overwrite the disk.
Memory	ROM	None
Communications	ROM	An external loopback connector may be installed if desired.
Parallel printer	ROM	A parallel printer must be connected.
Keyboard	Disk	Requires DOS diskette in drive A. Requires a monochrome or color monitor or an LCD display panel.
Video memory and display	Disk	Requires DOS diskette in drive A. Requires a monochrome or color monitor or an LCD display panel.

## **2.8 EXTENDED DIAGNOSTIC TEST RESULTS AND ERROR LOGGING**

ROM-based diagnostic test activity and results may be observed on a video monitor or may be logged on a recording device connected to the serial or parallel port.

The results of the disk-based diagnostics are displayed on a video monitor (or the flat-panel LCD display). Color circuit testing requires a composite or RGB color monitor.

### **2.8.1 Test Results Observed on a Video Monitor**

A typical ROM-based diagnostic test display is shown in Figure 2-6. The status line located at the bottom of the screen typically indicates what the test is doing, and displays the number of test passes and accumulated errors. Other error messages may be displayed above the status line.

```
TYPE SELECTION (D,M,C,P,L,R) - c
Select serial comm test port (1 or 2) 1
Are you using external loop-back (Y/N)?y
Testing serial comm port 1
With external loop-back
Type any key to abort
Comm test, Pass 1, error count = 0
```

**Figure 2-6. Typical Video Display During Diagnostic Test**

### **2.8.2 Logging Errors on a Recording Device**

ROM-based diagnostic errors may be logged (recorded) on a device connected to the serial or parallel port of the system.

To establish a logical link to the recording device, perform the following steps:

1. Select "L — LOG OPTIONS" from the ROM-based diagnostic menu.
2. Enter information requested for enabling selected port.
3. Connect the logging device (typically a printer) to the enabled port.

## **2.9 DIAGNOSTIC TESTS, INDICATIONS, SUGGESTED SOLUTIONS**

This section provides the following information on each of the extended diagnostics:

- How to execute the test
- How to observe the test results
- How to diagnose faults using the test results

ROM-based tests are presented first since the DOS operating system is not required for execution. The following diagnostic tests are described (tests are ROM-based unless otherwise noted):

- Disk
- Memory
- Communications
- Parallel printer
- Keyboard (disk-based)
- Video memory and display (disk-based)

### **2.9.1 Disk Test**

The disk test is a ROM-based write/read or read only diagnostic that is used to test the performance of a selected disk drive.

The write/read test writes data onto a selected (and formatted) disk and then reads the data to verify disk drive unit operation.

#### **CAUTION**

**A formatted scratch diskette should be used for the write/read test. This test overwrites the entire diskette and any data is destroyed.**

The read only test verifies disk drive unit operation by reading the data from a (formatted) disk in the selected drive unit.

### **Executing the Disk Test**

1. Select "D" (DISK TEST) from the ROM-based diagnostic menu (to invoke the ROM-based diagnostic menu, refer to section 2.4.1).
2. Configure and start the test by responding to the prompts displayed.

### **Observing Test Results**

The status line displays the following information:

- The number of the track, sector and side under test
- The cumulative number of test passes and hard errors
- The cumulative number of soft errors may be displayed by holding Ctrl and Alt and pressing F1.

When an error is detected, the following information is displayed in an error message above the status line\*:

- Type of error (hard or soft)
- Retry count
- Side, track, and sector number of error
- Error status (a hexadecimal byte)

### **Fault Diagnosis**

Refer to Table 2-5 when an error message indicates problems during a disk test. The table provides the definition of the error status byte (from the error message) and suggests procedures to correct the fault indicated.

### **NOTES**

- **Disk errors frequently result from faulty media (disks) or dirty write/read heads. Eliminate these possible causes of errors before continuing with the diagnostic procedures.**
- **If two drives are available, try interchanging drives and cables to isolate faults before changing the system PCB.**

---

\*Error messages may be logged on a recording device. Refer to section 2.8.2.

**Table 2-5. Disk Errors and Suggested Corrective Procedures**

Error Status and Definition	Possible Cause(s)	Suggested Corrective Procedure(s)
02 Address mask not found.	Unformatted or bad disk. Disk controller or data separator logic problem.	<ul style="list-style-type: none"> <li>• Use known good disk.</li> <li>• Replace system PCB.</li> </ul>
03 Write attempted on write-protected disk.	Disk is write-protected.	<ul style="list-style-type: none"> <li>• Use a disk that is not write-protected.</li> </ul>
04 Requested sector not found.	Unformatted or bad disk. Disk controller problem.	<ul style="list-style-type: none"> <li>• Use known good disk.</li> <li>• Replace system PCB.</li> </ul>
08 DMA overrun on operation.	DMA controller or disk controller problem.	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>
09 Attempt to DMA across 64K boundary.	Disk controller or support logic problem.	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>
10 CRC error on disk read.	Bad disk. Data separator logic problem.	<ul style="list-style-type: none"> <li>• Use known good disk.</li> <li>• Replace system PCB.</li> </ul>
20 Disk controller failed.	Disk controller problem.	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>

**Table 2-5. Disk Errors and Suggested Corrective Procedures (Cont.)**

Error Status and Definition	Possible Cause(s)	Suggested Corrective Procedure(s)
<b>40</b> Seek operation failed.	Power to disk drive.  Disk drive motor problem.  Disk controller problem.	<ul style="list-style-type: none"> <li>• Check for obstruction in drive.</li> <li>• Check drive power harness for correct power (refer to Figure 2-5). Replace harness or power supply if necessary.</li> <li>• Replace disk drive ribbon cable.</li> <li>• Replace disk drive unit.</li> <li>• Replace system PCB.</li> </ul>
<b>80</b> Time out error.	Drive head(s) not loaded or drive(s) not running.	<ul style="list-style-type: none"> <li>• Make sure drive button is pushed in.</li> <li>• Check drive power harness for correct power (refer to Figure 2-5). Replace harness or power supply if necessary.</li> <li>• Replace ribbon cable.</li> <li>• Replace disk drive unit.</li> <li>• Replace system PCB.</li> </ul>

### 2.9.2 Memory Test

The memory test is a ROM-based diagnostic that is used to test the performance of system memory.

The memory test displays the system memory size and then performs a write/read check of each location in memory.

## **Executing the Memory Test**

- Select “M” (MEMORY TEST) from the ROM-based diagnostic menu (to invoke the ROM-based diagnostic menu, refer to Section 2.4.1).

## **Observing Test Results**

The status line displays the following information:

- The name of the test (“Memory test”).
- The cumulative number of test passes and errors.

When an error is detected, the following error message is displayed above the status line (ssss:oooo is the address of the failing location, nn and xx are hex bytes):\*

**DRAM ERROR at: ssss:oooo expected = nn read = xx**

## **Fault Diagnosis**

Memory errors may result from any of the following:

- Faulty locations in memory.
- Faulty PAL (programmable array logic).
- Improperly installed memory upgrades.
- Incorrectly set switchpack.

Table 2-6 indicates the types of memory errors, possible cause(s) of the errors and suggests corrective procedures.

**Table 2-6. Memory Errors and Suggested Corrective Procedures**

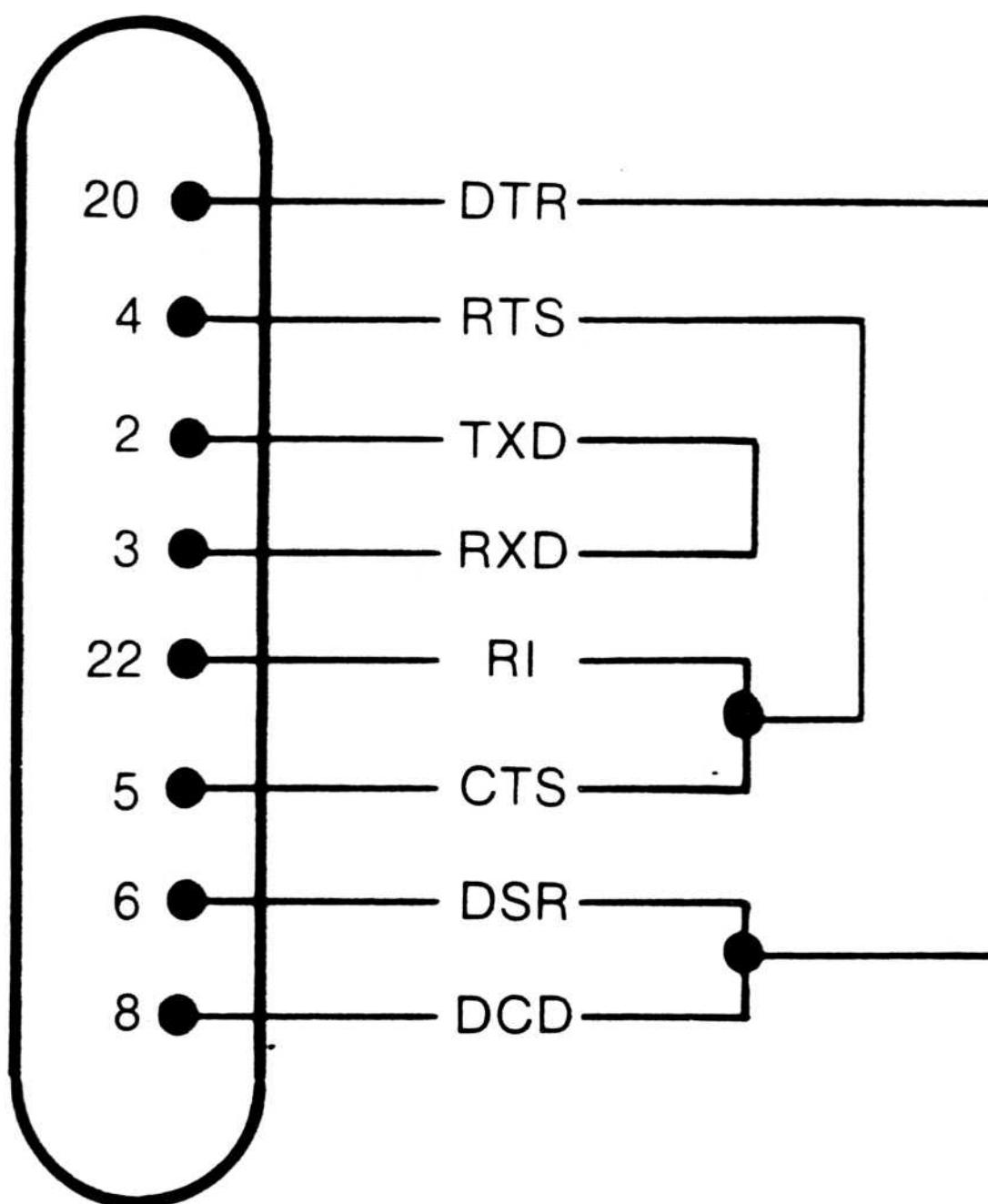
Error Type	Possible Cause(s)	Suggested Corrective Procedures
Many errors in contiguous locations.	Switchpack or memory incorrectly configured.  Faulty RAM chip, PAL, or address decoder.	<ul style="list-style-type: none"><li>• Check switchpack switch settings.</li><li>• Verify proper memory configuration.</li><li>• Replace system PCB.</li></ul>
Error(s) in one location or in random locations.	Faulty RAM chip or PAL.	<ul style="list-style-type: none"><li>• Replace system PCB.</li></ul>

\*Error messages may be logged on a recording device. Refer to Section 2.8.2.

### 2.9.3 Communications Test

The communications test is a ROM-based diagnostic that is used to test the performance of the ASYNC port (port 1) or the ASYNC/SYNC port (port 2).

The test may be configured for internal or external loopback. A loopback connector (refer to Figure 2-7) is required for external loopback testing.



**Figure 2-7. External Loopback Connector Schematic Diagram**

#### Executing the Communications Test

1. Select "C" (COMMUNICATIONS TEST) from the ROM-based diagnostic menu (to invoke the ROM-based diagnostic menu, refer to Section 2.4.1).
2. Configure and start the test by responding to the prompts displayed.

#### Observing Test Results

The status line displays the following information:

- The name of the test (Comm test).
- The cumulative number of test passes and errors.

Each time an error is detected, an error message is displayed above the status line. Error messages are described below.

## **Fault Diagnosis for Port 1**

Communications test error messages for port 1 (ASYNC PORT) are described below (error messages are boldface and in alphabetical order). Possible causes of the error messages and suggested corrective procedures are also listed.

### **Data error: expected = xx read = yy**

Received data did not match transmitted data.

#### **Possible Causes:**

- Loop-back connector.
- Rear panel connector.
- EIA drivers (U6, U9 and U10).
- 8250 controller (U72).

#### **Suggested Corrective Procedures:**

- Verify loop-back connector (refer to Figure 2-7).
- Replace system PCB.

### **Intrpt error**

8250 failed to generate interrupt on IRQ4 line.

#### **Possible Causes:**

- 8250 controller (U72).
- IRQ4 line shorted.
- 8259 interrupt controller (U86).

#### **Suggested Corrective Procedures:**

- Replace system PCB.

### **Modem status error: expected = xx read = yy**

Status of modem signals looped back through the external loopback plug is not as expected.

#### **Possible Causes:**

- Loop-back connector.
- EIA drivers (U6, U9 and U10).
- Rear panel connector.

#### **Suggested Corrective Procedures:**

- Verify loop-back connector (refer to Figure 2-7).
- Replace system PCB.

## **Modem Status Bit Descriptions**

Bit	Signal
0	Clear To Send has changed (DCTS)
1	Data Set Ready has changed (DDSR)
2	Trailing Edge of Ring Indicator (TERI)
3	Receive Line Signal Detect has changed (DRLSD)
4	Clear To Send (CTS)
5	Data Set Ready (DSR)
6	Ring Indicator (RI)
7	Receive Line Signal Detect (RLSD)

## **Receiver error, line status = xx**

Receiver error was detected.

### **Status Bit Descriptions:**

Bit	Meaning
0	Data ready (receiver)
1	Overrun error
2	Parity error
3	Framing error
4	Break detected
5	Transmit holding register empty
6	Transmit shift register empty
7	Time out

### **Possible Causes:**

- Loop-back connector
- EIA drivers (U6, U9 and U10)
- Rear panel connector

### **Suggested Corrective Procedures:**

- Verify loop-back connector (refer to Figure 2-7).
- Replace system PCB.

## **R/W register error: zzzz expected = xx read = yy**

8250 (U72) read/write test failed at port address zzzz, data written is xx, data read back is yy.

### **Possible Causes:**

- 8250 Controller (U72)

### **Suggested Corrective Procedures:**

- Replace system PCB.

### **Transmitter time out, line status = xx**

Time out occurred while waiting for transmitter buffer to be empty. Line status bits (xx) are described below.

#### **Status Bit Descriptions:**

Bit	Meaning
0	Data ready (receiver)
1	Overrun error
2	Parity error
3	Framing error
4	Break detected
5	Transmit holding register empty
6	Transmit shift register empty
7	Time out

#### **Possible Causes:**

- Missing baud rate clock,
- 8250 controller (U72)

#### **Suggested Corrective Procedures:**

- Replace system PCB.

### **Fault Diagnosis for Port 2**

Communications test error messages for port 2 (ASYNC/SYNC PORT) are described below (error messages are boldface and in alphabetical order). Possible causes of the error messages and suggested corrective procedures are also listed.

#### **Data error: **expected = xx** **read = yy****

Received data did not match transmitted data.

#### **Possible Causes:**

- Loopback connector
- Rear panel connector
- Line drivers (U6, U7, U8)
- 8530 controller (U59)

#### **Suggested Corrective Procedures:**

- Verify loopback connector.
- Replace system PCB.

### **Intrpt error**

8530 failed to generate interrupt on IRQ3 line.

#### **Possible Causes:**

- 8530 controller (U59)
- IRQ3 line shorted
- 8259 interrupt controller (U86).

#### **Suggested Corrective Procedures:**

- Replace system PCB

### **Hardware not installed**

#### **Fatal error**

Indicates that the optional ASYNC/SYNC port hardware is not installed or that it is not installed correctly.

#### **Possible Causes:**

- 8530 controller (U59) and/or associated hardware not installed or not installed properly.

#### **Suggested Corrective Procedures:**

- Verify correct installation of the 8530 option
- Replace system PCB.

### **Modem status error: RI DSR DCD CTS**

**expected = x x x x**

**read = y y y y**

"x" and "y" are either 0 or 1. Modem control lines did not change as expected through the loopback plug on comm port 2.

#### **Possible Causes:**

- Loopback connector
- Rear panel connector
- Line drivers (U6, U7, U8)
- 8530 controller (U59)

#### **Suggested Corrective Procedures:**

- Verify loopback connector (refer to Figure 2-7).
- Replace system PCB.

### **Receiver error, line status = xx**

Receiver error detected. xx is the 8530 read register 1 that has the following bit assignments.

#### **Status Bit Descriptions:**

Bit	Meaning
0	All sent
1-3	Not applicable
4	Parity error
5	Overrun error
6	Framing error
7	Not applicable

#### **Possible Causes:**

- Loopback connector
- Rear panel connector
- Line drivers (U6, U7, U8)
- 8530 controller (U59)

#### **Suggested Corrective Procedures:**

- Verify loopback connector (refer to Figure 2-7).
- Replace system PCB.

### **Receiver time out**

Time out occurred before Receive Character Available bit (bit 0) of 8530 controller read register 0 did not become valid

#### **Possible Causes:**

- Loopback connector
- Rear panel connector
- Line drivers (U6, U7, U8)
- 8530 controller (U59)

#### **Suggested Corrective Procedures:**

- Verify loopback connector (refer to Figure 2-7).
- Replace system PCB.

### **Transmitter time out, line status = xx**

Transmitter time out occurred while waiting for transmitter buffer to be empty. xx is the 8530 read register 0 that has the following bit assignments.

#### **Status Bit Descriptions:**

Bit	Meaning
0	Receive character available
1	Not applicable
2	Transmitter buffer empty
3	Data Carrier Detect (DCD)
4	Not applicable
5	Clear To Send (CTS)
6	Transmit underrun
7	Break detected

#### **Possible Causes:**

- Missing baud rate clock,
- 8530 controller (U59)

#### **Suggested Corrective Procedures:**

- Replace system PCB.

### **2.9.4 Parallel Printer Test**

The parallel printer test is a ROM-based diagnostic that sends a barber-pole test pattern (see Figure 2-8) to the parallel printer. This test verifies operation of the entire printer circuit including the printer.

A functioning parallel printer is required to perform this test.

```
!"#$%&" ()*+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmno
!"#$%&" ()*+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnop
!"#$%&" ()*+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopq
#$%&" ()*+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqr
$%&" ()*+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqrs
%&" ()*+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqrst
&" ()*+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqrst
&" ()*+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqrstuv
? ()*+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqrstuv
()*+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqrstuvw
) *+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqrstuvw
*+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqrstuvwxy
+, -./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqrstuvwxyz
,-./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqrstuvwxyz(
-/0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqrstuvwxyz(
./0123456789: ; <=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefgijklmnopqrstuvwxyz(1)
```

**Figure 2-8. Typical Barber-Pole Printer Test Pattern**

## **Executing the Parallel Printer Test**

- Select “P” (PARALLEL PRINTER TEST) from the ROM-based diagnostic menu (to invoke the ROM-based diagnostic menu, refer to section 2.4.1).

## **Observing Test Results**

The barber pole test pattern prints continuously on the parallel printer. **PRINTER NOT READY** may be displayed on the monitor if the printer is not connected or not turned on.

## **Fault Diagnosis**

If the printer does nothing or prints erratically, the following corrective procedures are suggested.

- Verify that the printer is properly connected and turned on.
- Verify that the correct cable is being used.
- If a known good cable and printer fails to operate properly, replace the system PCB.

## **2.9.5 Keyboard Test**

The Keyboard test is an interactive disk-based test that allows the technician to verify operation of each of the 83 keys on the keyboard. A self-test of the keyboard controller is also executed each time the keyboard test is invoked.

## **Executing the Keyboard Test**

1. Select “K” (KEYBOARD TEST) from the disk-based diagnostic menu (to invoke the disk-based diagnostic menu, refer to section 2.4.2).
2. Run the test by responding to the prompts displayed.

## **Observing Test Results**

The results from the keyboard self-test are displayed on the screen by one of the following messages.

- **KEYBOARD SELF TEST PASSED**
- **KEYBOARD SELF TEST FAILED**

A phantom keyboard may then be displayed on the monitor. As each key on the keyboard is pressed, the corresponding key is highlighted on the screen.

## **Fault Diagnosis**

If the keyboard self-test fails, then one or more of the following components may be at fault.

- 6500/41 keyboard controller.
- Scan line problems on the keyboard PCB.

If the keyboard self-test passes but the phantom keyboard test does not execute properly, then one or more of the following components may be at fault.

- Keyboard
- Keyboard interface cable
- System PCB

#### **2.9.6 Video Memory and Display Test**

The video memory and display test is a disk-based diagnostic that is used to exercise various video capabilities. The full test is made up of three separate tests:

- A video memory test (executes each time the video test is invoked).
- A monochrome test (requires a monochrome monitor).
- A color test (requires an RGB and/or a composite color monitor).

#### **NOTE**

**The test procedures assume that the video monitors are adjusted and functioning properly and that the proper cables are used. Schematic diagrams of cables are included in Appendix A.**

Fault diagnosis for the monochrome and color tests is provided at the end of this section.

#### **Executing the Monochrome Video Test**

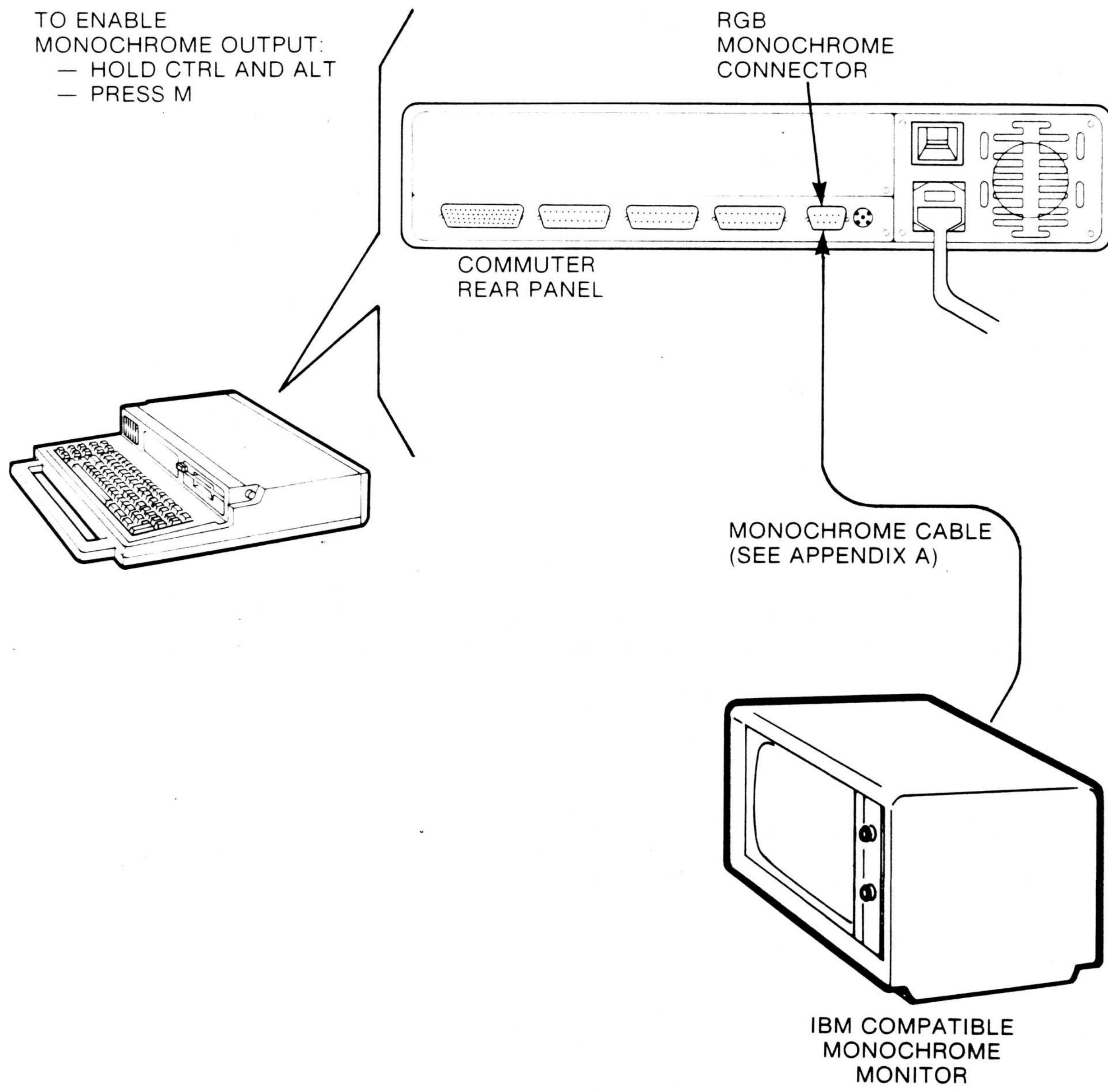
1. Configure the Commuter system as shown in Figure 2-9.
2. Enable monochrome output (if necessary).
  - Hold **Ctrl** and **Alt**
  - Press **M**
3. Select "V" (VIDEO MEMORY AND DISPLAY TEST) from the disk-based diagnostic menu (to invoke the disk-based diagnostic menu, refer to section 2.4.2).
4. Execute the test by responding to the prompts displayed.

#### **Observing Monochrome Test Results**

The video memory self-test results are displayed on the monitor(s) by one of the following messages.

**VIDEO MEMORY TEST PASSED**

**VIDEO MEMORY TEST FAILED, ssss:oooo=xx**



**Figure 2-9. Typical Monochrome Video Test Configuration**

Then the following video capabilities may be sequentially displayed on the monochrome monitor:

- Display attributes (blinking, reverse video, and so on).
- Character set
- 80 column × 25 row display of characters

### **Executing the Color Video Test**

1. Configure the Commuter system as shown in Figure 2-10.
2. Enable RGB and Composite outputs if necessary.
  - Hold **Ctrl** and **Alt**
  - Press **8**
3. Select “V” (VIDEO MEMORY AND DISPLAY TEST) from the disk-based diagnostic menu (to invoke the disk-based diagnostic menu, refer to section 2.4.2).
4. Execute the test by responding to the prompts displayed.

### **Observing Color Video Test Results**

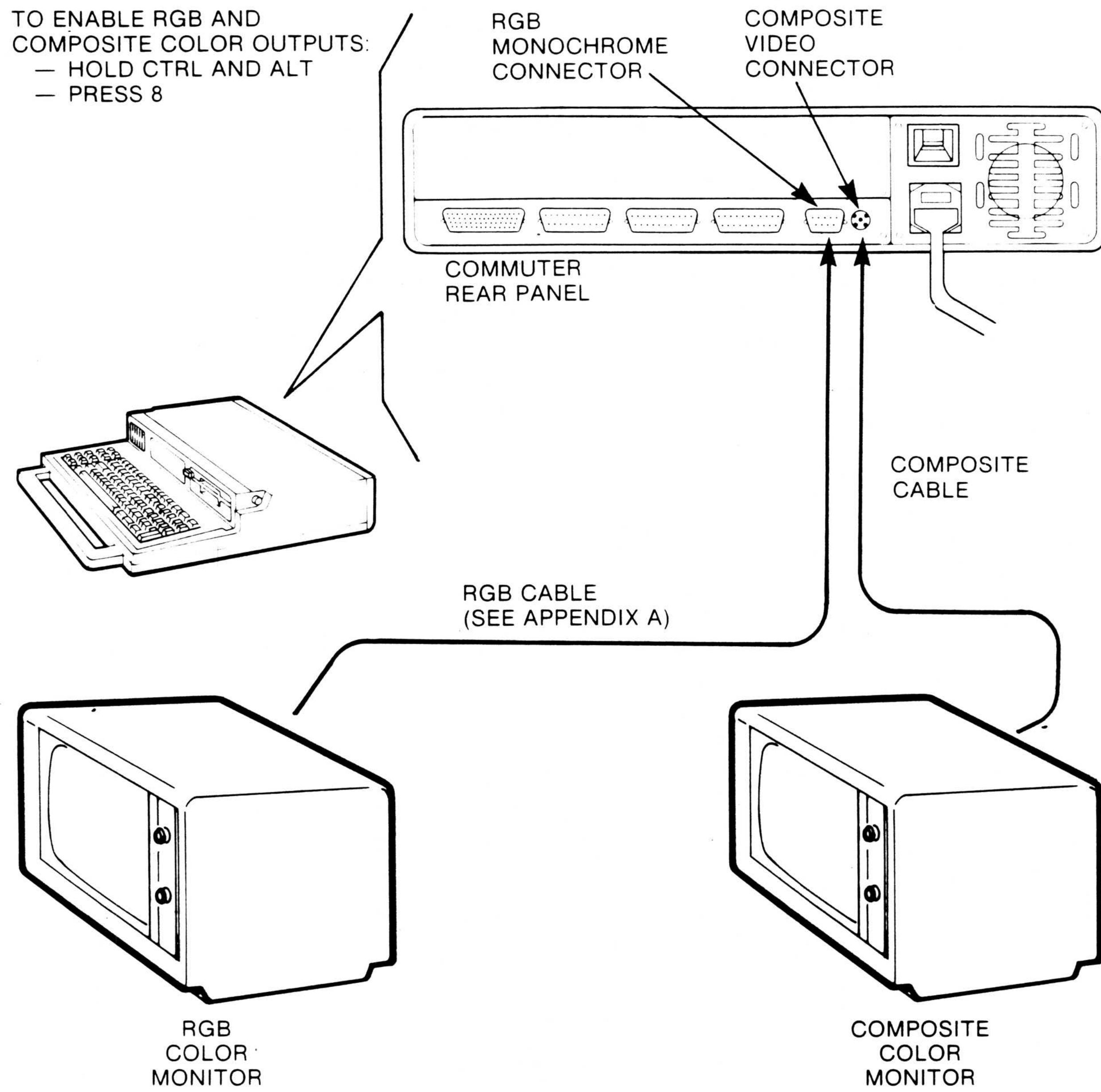
The video memory self-test results are displayed on both monitors (the self-test message is described under **Fault Diagnosis** for the monochrome video test). Then the following video capabilities may be sequentially displayed on both monitors.

- Display attributes (blinking, reverse video, and so on).
- Color bar display
- Character set
- 80 column × 25 row display of characters
- 40 column × 25 row display of characters
- 320 × 200 graphic display
- 640 × 200 graphic display
- Display pages of “0”s through “7”s

### **Fault Diagnosis for Monochrome or Color Video**

The diagnostic procedures in this section pertain to both the monochrome and the color video tests.

If **VIDEO MEMORY TEST FAILED ssss:oooo=xx** is displayed, the system PCB may be at fault and should be replaced. This message indicates that the video memory test detected an error at segment **ssss**, offset **oooo**. The value **xx** (hex) is the XOR (exclusive OR) of expected and actual data (the data bits in error are shown as ones).



**Figure 2-10. Typical Color Video Test Configuration**

Refer to Table 2-7 when the monochrome or color video test fails to execute properly. The table describes typical symptoms, indicates a possible cause of the symptom and suggests corrective procedures.

**Table 2-7. Video Test Symptoms and Suggested Corrective Procedures**

Symptom	Possible Cause	Suggested Corrective Procedure(s)
No video present on one (or both) monitors	Video oscillator or timing logic	<ul style="list-style-type: none"> <li>• Verify that monitor(s) are plugged in and functional.</li> <li>• Verify proper cabling (Refer to Figures 2-9, 2-10 and Appendix A).</li> <li>• Replace system PCB.</li> </ul>
Synchronization (Horizontal or Vertical) or alignment problems	6845 Video controller or support logic, or timing logic	<ul style="list-style-type: none"> <li>• Verify that monitor(s) are properly adjusted.</li> <li>• Replace system PCB.</li> </ul>
Character set pixel (dot) problems	Character generator (U142)	<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>
Attribute problems		<ul style="list-style-type: none"> <li>• Replace system PCB.</li> </ul>
Color problems	Color generation or color control logic	<ul style="list-style-type: none"> <li>• Verify that monitor(s) are properly adjusted.</li> <li>• Replace system PCB.</li> </ul>

## **CHAPTER 3**

### **SUBASSEMBLY REMOVAL AND REPLACEMENT**

#### **3.1 INTRODUCTION**

This chapter describes the procedures for removing subassemblies from the Commuter system.

To replace any subassembly, reverse the steps used in the removal procedure.

#### **WARNING**

**Always turn the power off and disconnect the power cord before servicing the Commuter system.**

When it is necessary to remove a subassembly, follow the procedures in the section indicated below.

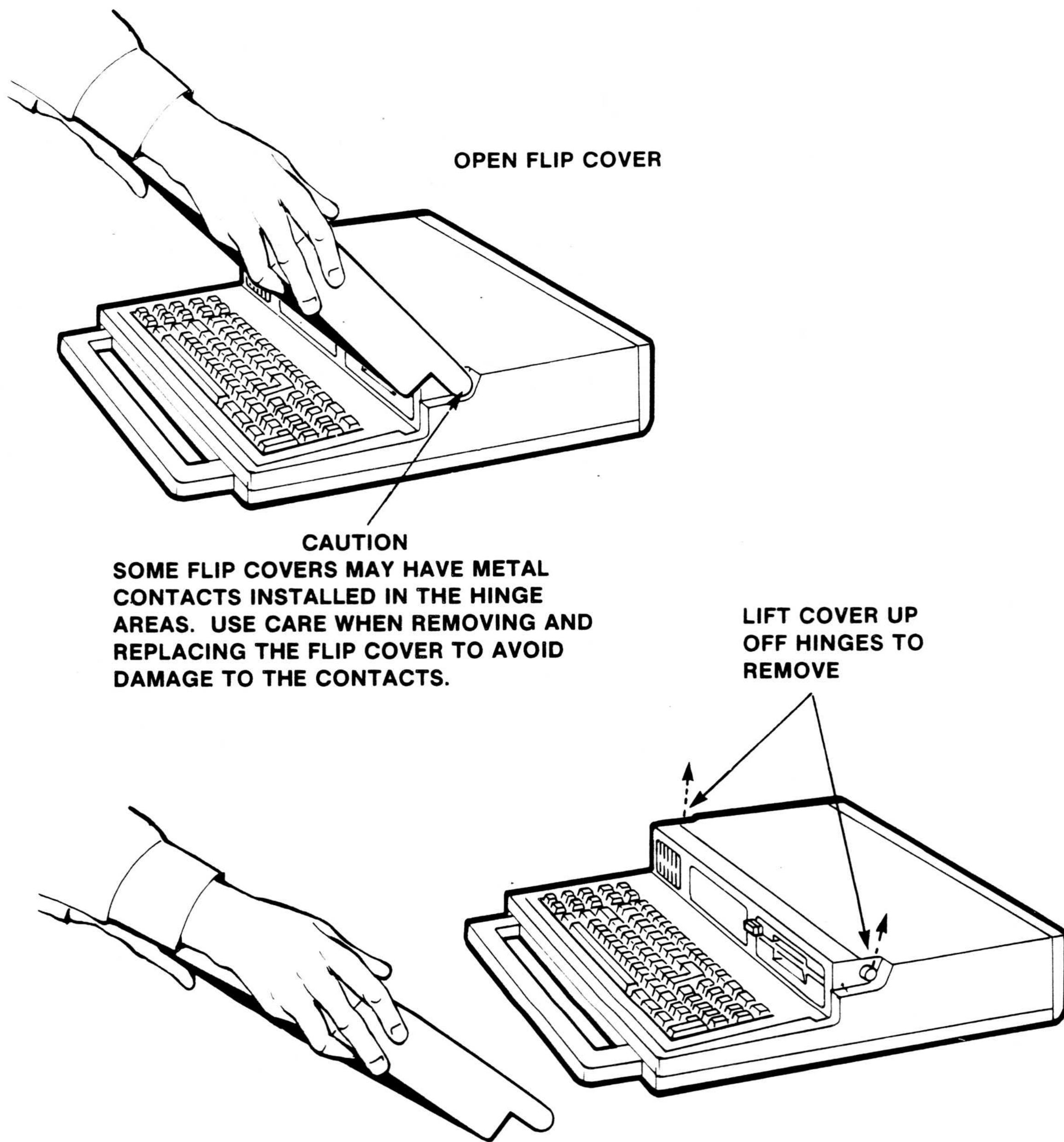
- |                         |                 |
|-------------------------|-----------------|
| • Flip Cover Removal    | See Section 3.2 |
| • LCD Panel Removal     | See Section 3.3 |
| • Chassis Cover Removal | See Section 3.4 |
| • Power Supply Removal  | See Section 3.5 |
| • Disk Drive(s) Removal | See Section 3.6 |
| • Keyboard Removal      | See Section 3.7 |
| • System PCB Removal    | See Section 3.8 |

### 3.2 FLIP COVER REMOVAL

This section describes the procedures for removing the flip cover.

#### To remove the flip cover:

1. Pull the slide locks on both sides of the flip cover forward and open the cover to about a 60° angle (see Figure 3-1).
2. Disconnect the LCD display connecting cable (if applicable).
3. Remove the cover by lifting it straight up off of the hinges as shown in Figure 3-1.



**Figure 3-1. Flip Cover Removal**

### 3.3 LCD ASSEMBLY REMOVAL

This section describes the procedures for removing the LCD display assembly from the flip cover.

#### CAUTION

An LCD display contains CMOS devices that may be damaged by static electricity. When handling an LCD display, both the workstation and the technician must be properly grounded.

To remove the LCD display assembly:

1. Remove the flip cover (refer to section 3.2).
2. Remove the two screws that hold the LCD assembly in the flip cover and lift the assembly out of the flip cover (see Figure 3-2.).

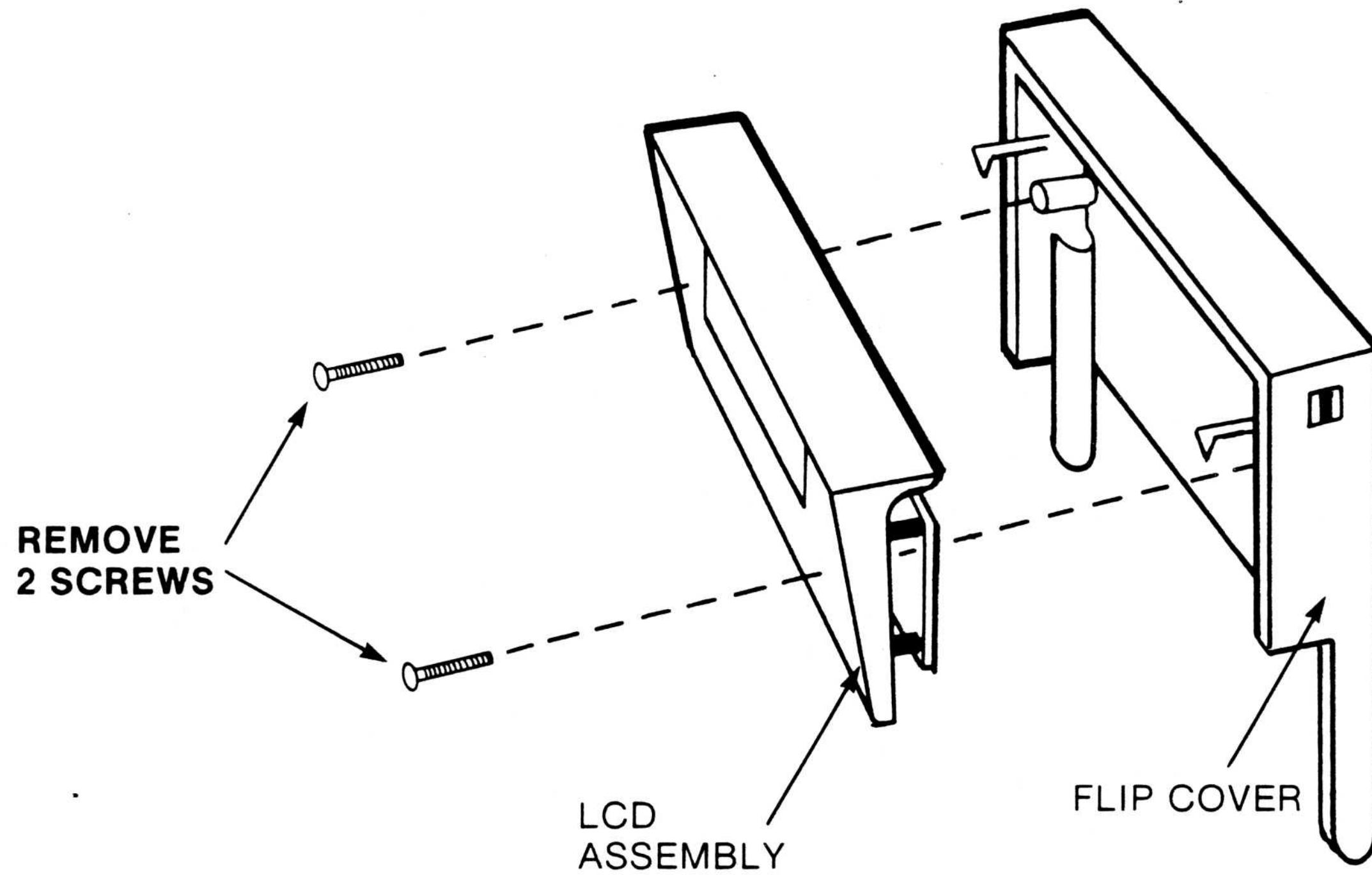


Figure 3-2. LCD Assembly Removal

### **3.4 CHASSIS COVER REMOVAL**

This section describes the procedures for removing the chassis cover.

#### **WARNING**

**Always unplug both ends of the power cord before removing the chassis cover.**

#### **To remove the chassis cover:**

1. Remove the flip cover (refer to Section 3.2).
2. Remove the nine screws shown in Figure 3-3.
3. Release the front catches as shown in Figure 3-3.
4. Carefully pull up on both of the rear corners and ease the chassis cover off.

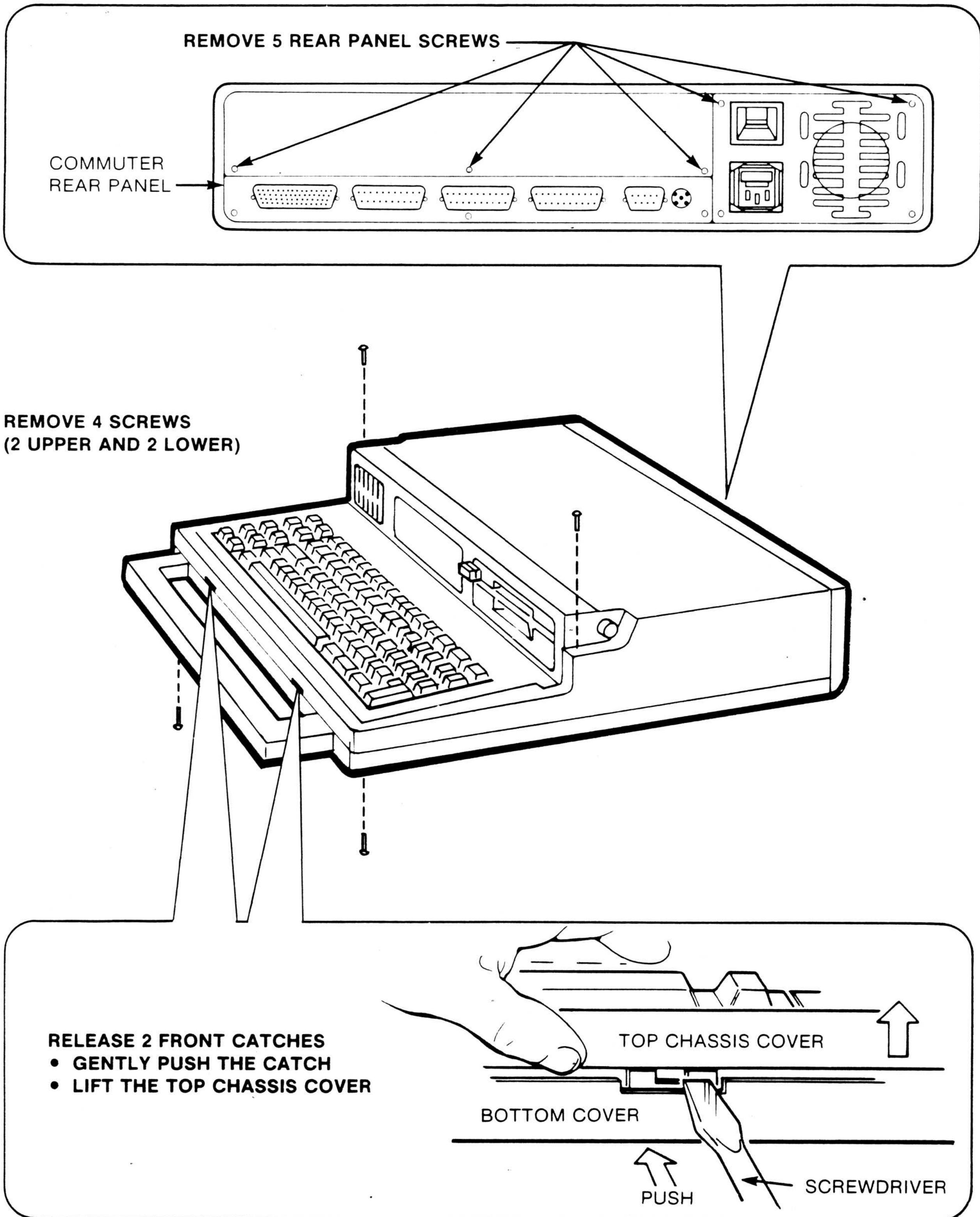


Figure 3-3. Chassis Cover Removal

### **3.5 POWER SUPPLY REMOVAL**

This section describes the removal procedures for the power supply module.

#### **To remove the power supply module:**

1. Remove the chassis cover (refer to Section 3.4).
2. Unplug the three connectors shown in Figure 3-4.
3. Remove the four screws shown in Figure 3-4.
4. Lift the module out of the chassis.

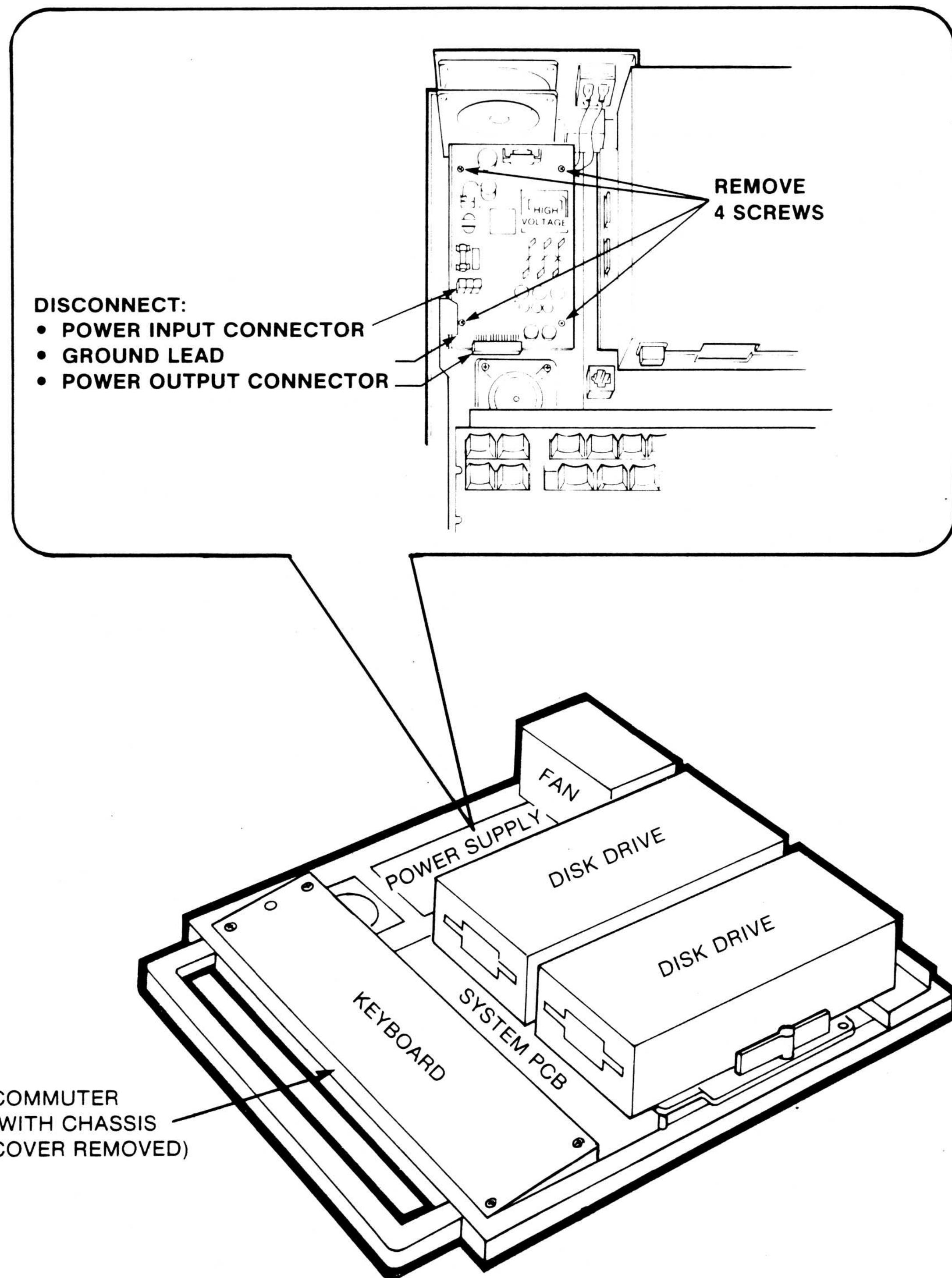


Figure 3-4. Power Supply Removal

### **3.6 DISK DRIVE REMOVAL**

This section describes the removal procedures for the disk drive unit(s).

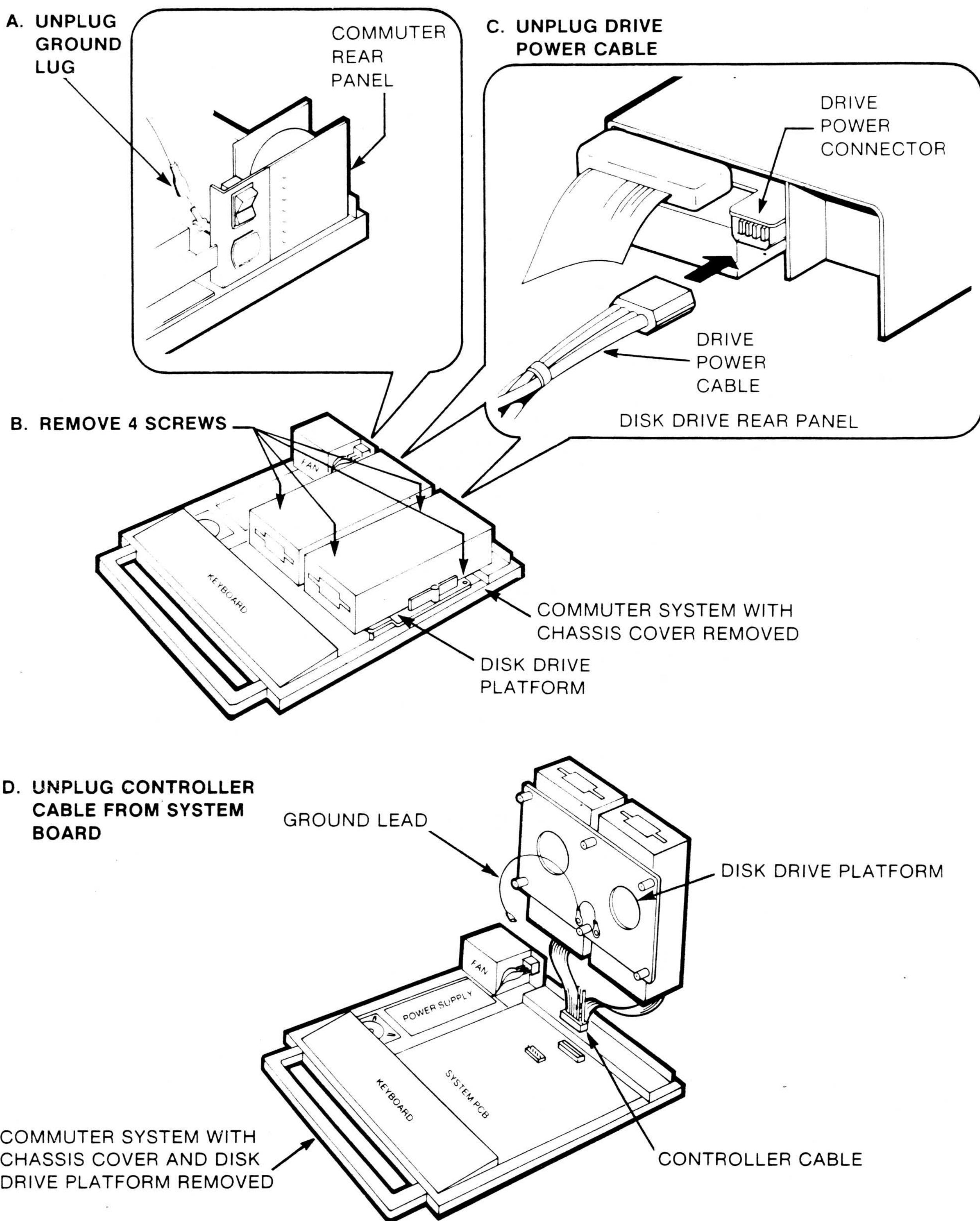
#### **To remove the disk drive(s):**

1. Remove the chassis cover (refer to Section 3.4).
2. Remove the drive platform (see Figure 3-5).
  - a. Unplug the ground lead from the ground lug.

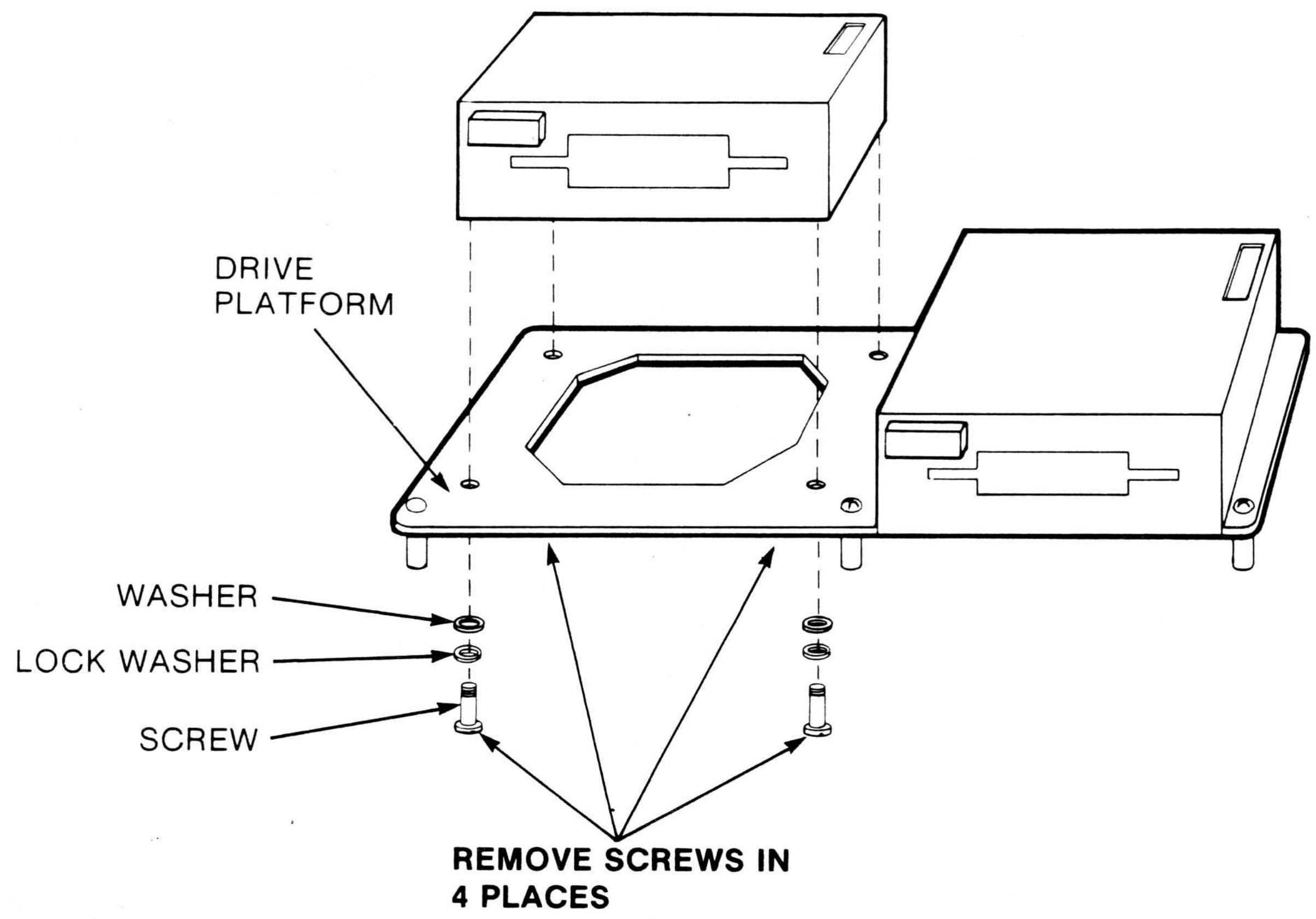
#### **CAUTION**

**When a single drive unit is installed, the spare cables may be secured to the drive platform. Release these cables before removing the platform.**

- b. Remove the four screws that secure the drive platform to the system PCB.
- c. Unplug the power cable(s) from the rear of the drive(s) as shown in Figure 3-5.
- d. Unplug the controller cable from the system PCB while lifting the platform out of the chassis.
3. Remove the individual drive unit from the platform by removing the four screws that secure the drive unit to the platform as shown in Figure 3-6.



**Figure 3-5. Disk Drive Platform Removal**



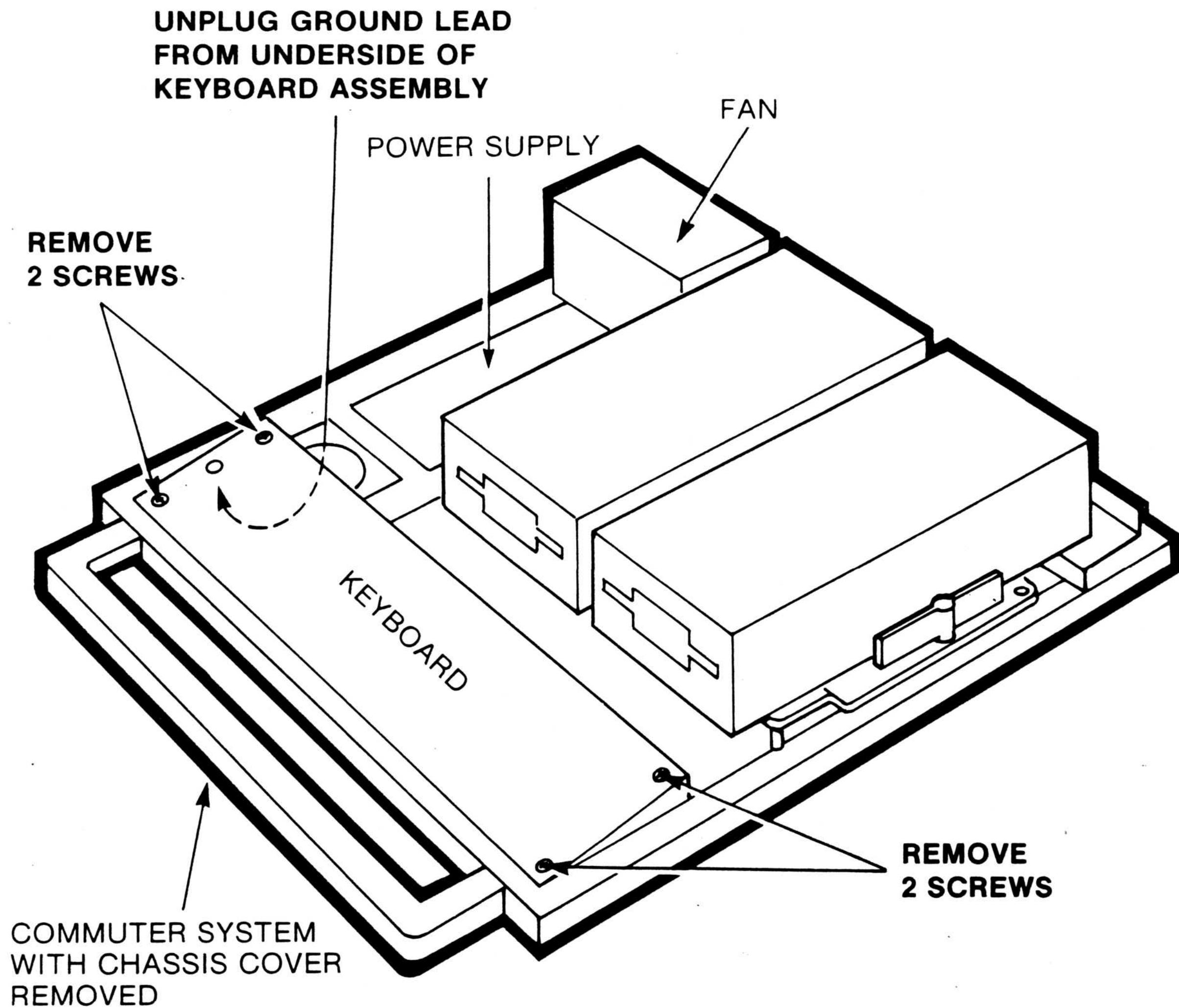
**Figure 3-6. Disk Drive Removal**

### 3.7 KEYBOARD REMOVAL

This section describes the removal procedures for the keyboard assembly.

#### To remove the keyboard assembly:

1. Remove the chassis cover (refer to Section 3.4).
2. Remove the four screws that secure the keyboard assembly to the chassis as shown in Figure 3-7.
3. Disconnect the controller cable from the keyboard.
4. Disconnect the ground lead while lifting the keyboard assembly out of the chassis (see Figure 3-7).



**Figure 3-7. Keyboard Removal**

### **3.8 SYSTEM PCB REMOVAL**

This section describes the removal procedures for the system PCB.

**To remove the system PCB:**

1. Remove the following subassemblies.
  - Chassis cover (refer to Section 3.4).
  - Disk drive platform (refer to Section 3.6)
  - Keyboard assembly (refer to Section 3.7).
2. Unplug the three cables shown in Figure 3-8.
3. Remove the three screws that secure the rear of the system PCB to the lower chassis and carefully lift out the PCB.

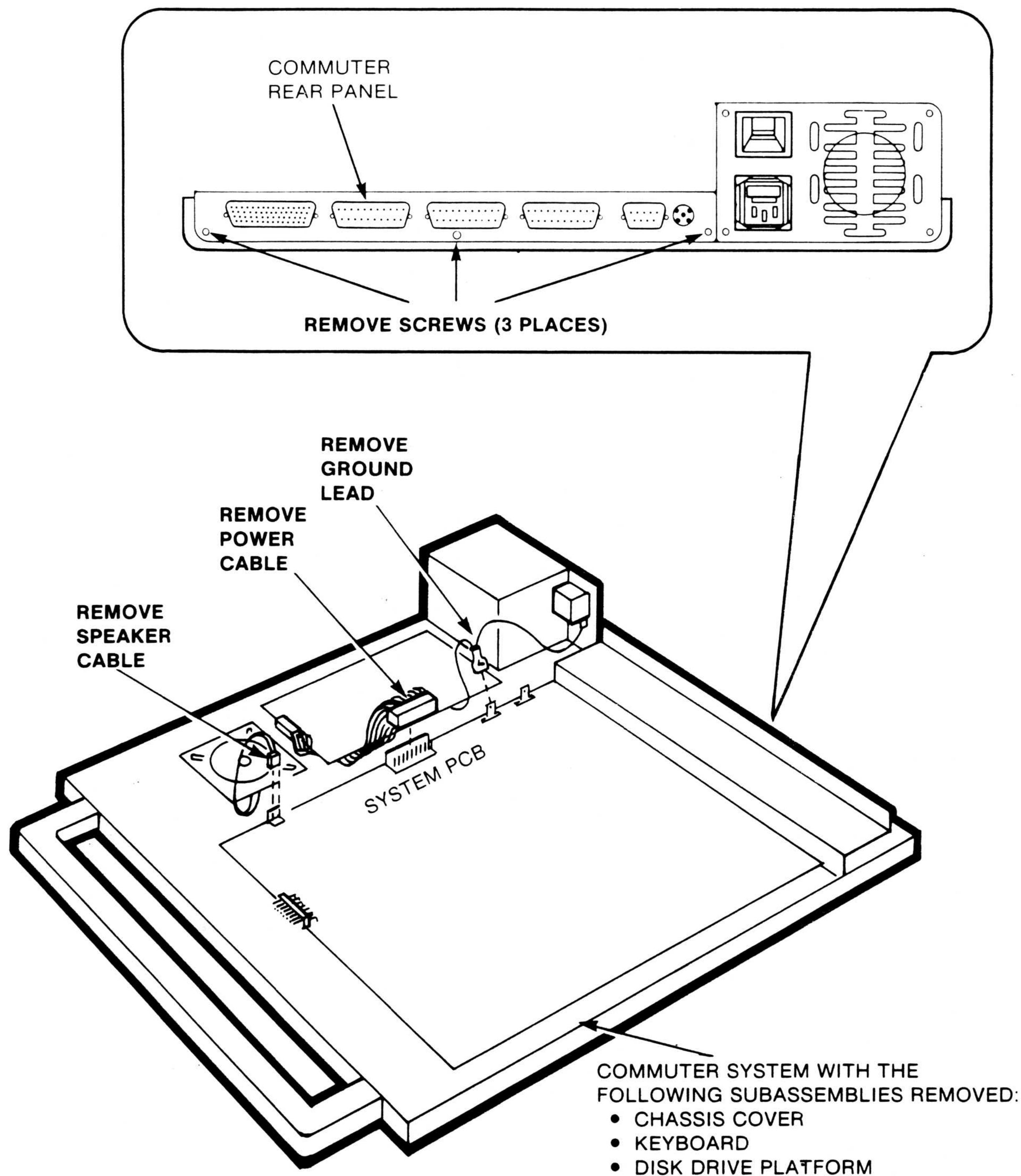


Figure 3-8. System PCB Removal



## **CHAPTER 4**

### **INSTALLING SYSTEM OPTIONS**

#### **4.1 INTRODUCTION**

This chapter provides information required for installing the following system options.

- Additional memory
- 8087 numeric coprocessor
- Second 5 1/4" disk drive
- Flat panel LCD display.
- RS-232-C programmable serial port

All of the system options are available from Visual Technology Incorporated. Option order numbers are contained in the SERVICE AND SUPPORT SPARE PARTS PRICING documentation.

#### **4.2 OPTION INSTALLATION GUIDELINES**

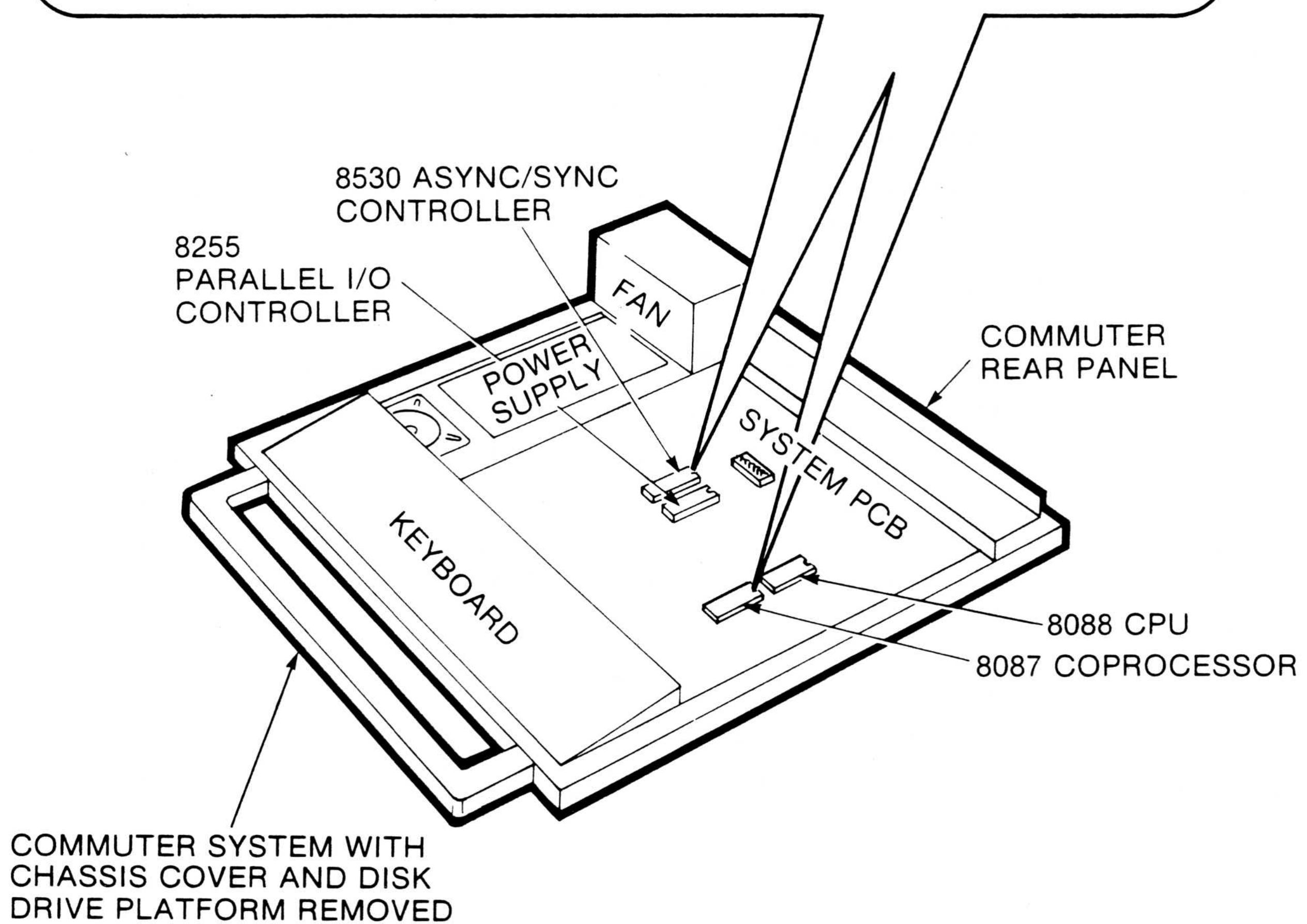
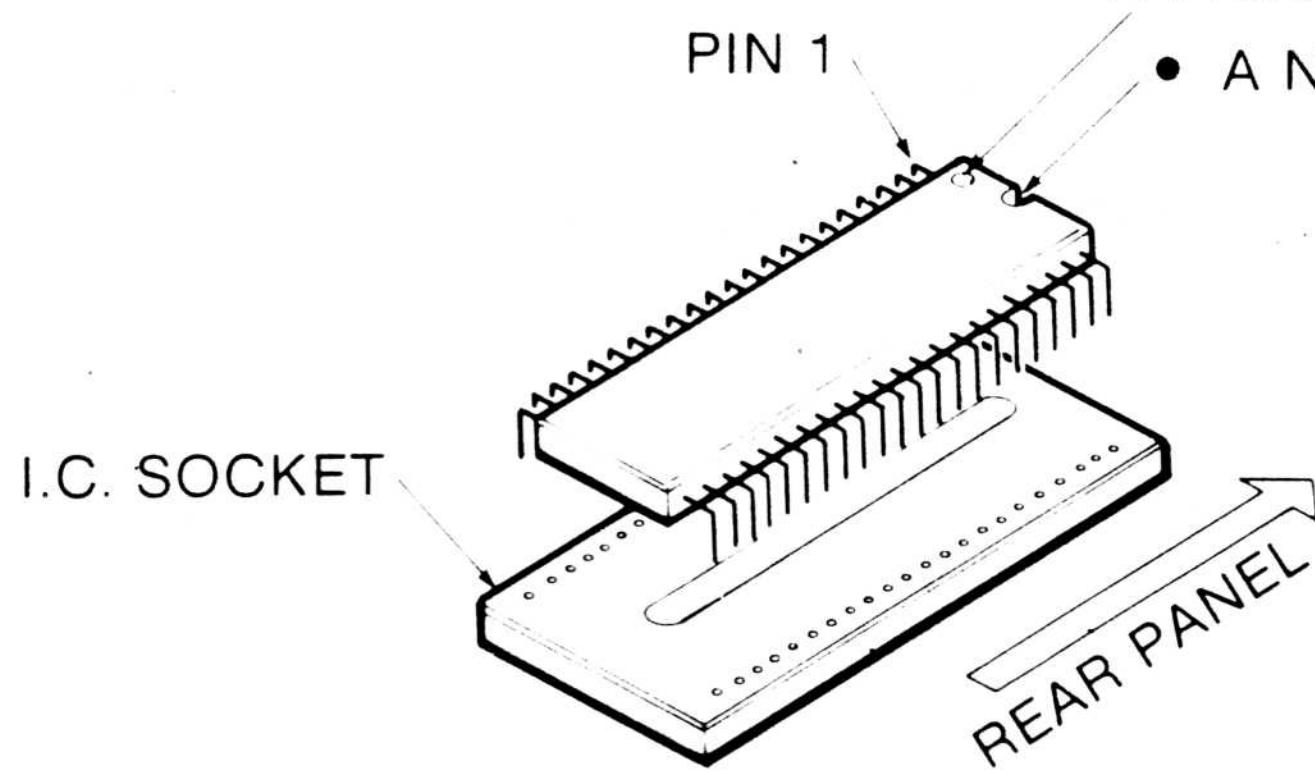
Some system options require the installation of integrated circuits (IC) components that may become damaged if handled or installed improperly.

Avoid damage to the option or to the Commuter system by adhering to the following guidelines.

1. Place the IC into the correct socket. The socket locations are provided with the specific option installation instructions.
2. Make sure that pin 1 in the IC is toward the rear of the Commuter system (see Figure 4-1).
3. Make sure the IC pins are uniformly bent to a 90° angle (see Figure 4-2) for insertion. Otherwise the IC must be prepared for insertion as described in Figure 4-2.
4. When inserting the IC into the socket:
  - Partially insert one side and then the other.
  - Make sure every pin is properly inserted.
  - Carefully push on each side until the IC is fully inserted.

PIN 1 MAY TYPICALLY BE IDENTIFIED BY:

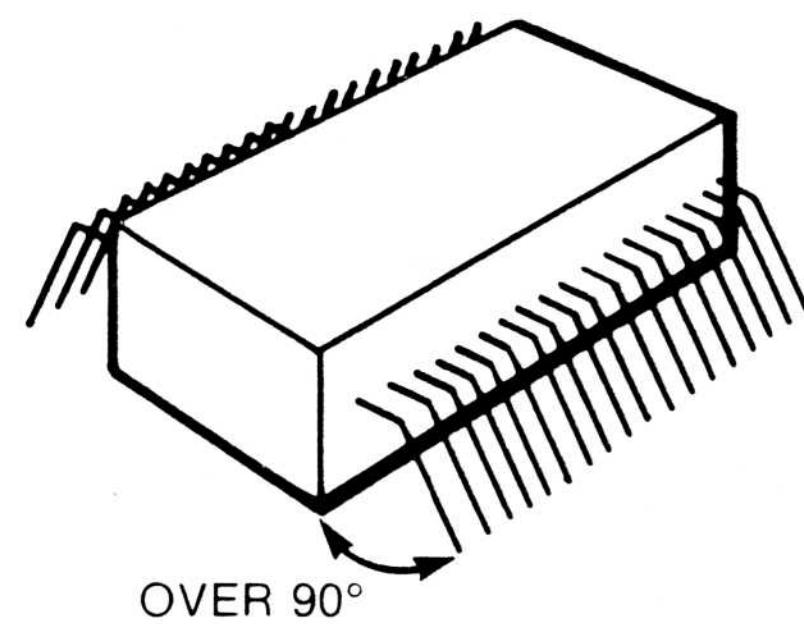
- A PRINTED OR INDENTED DOT.
- A NOTCH CUT IN THE I.C.



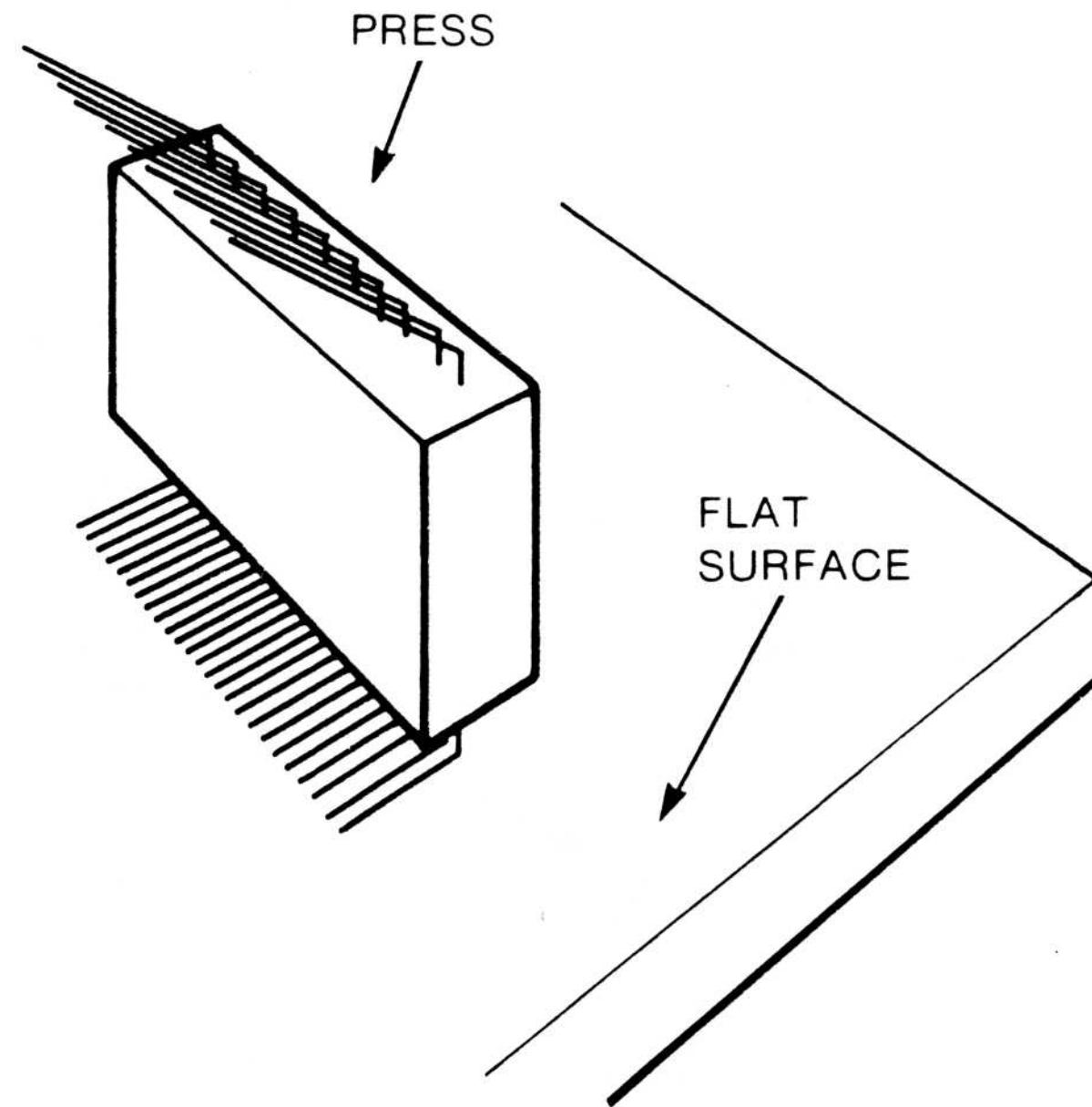
**Figure 4-1. Orienting ICs with Pin 1 Towards the Rear Panel**

The following figure illustrates how to prepare an IC for insertion into an IC socket.

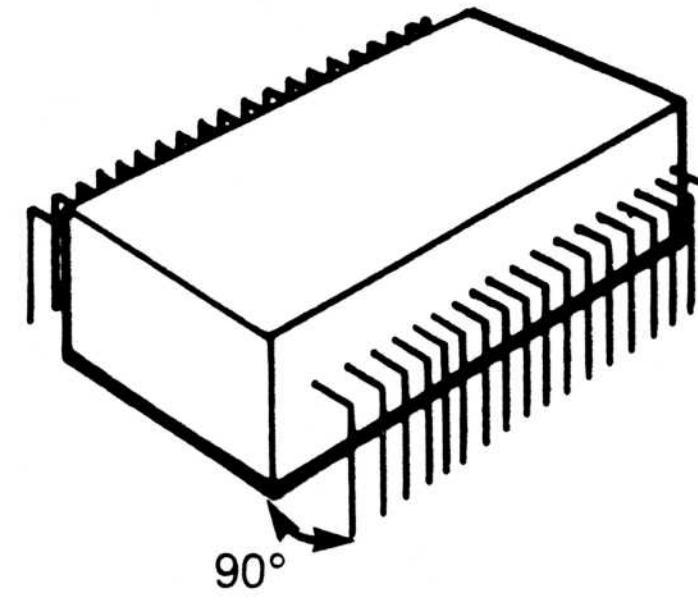
IC NOT READY FOR INSERTION  
(THE PINS ARE NOT AT A UNIFORM  
90° ANGLE).



2. PRESS THE IC PINS AGAINST A FLAT SURFACE.



3. IC READY FOR INSERTION. THE PINS ARE AT THE DESIRED ANGLE.



**Figure 4-2. Preparing an IC for Insertion**

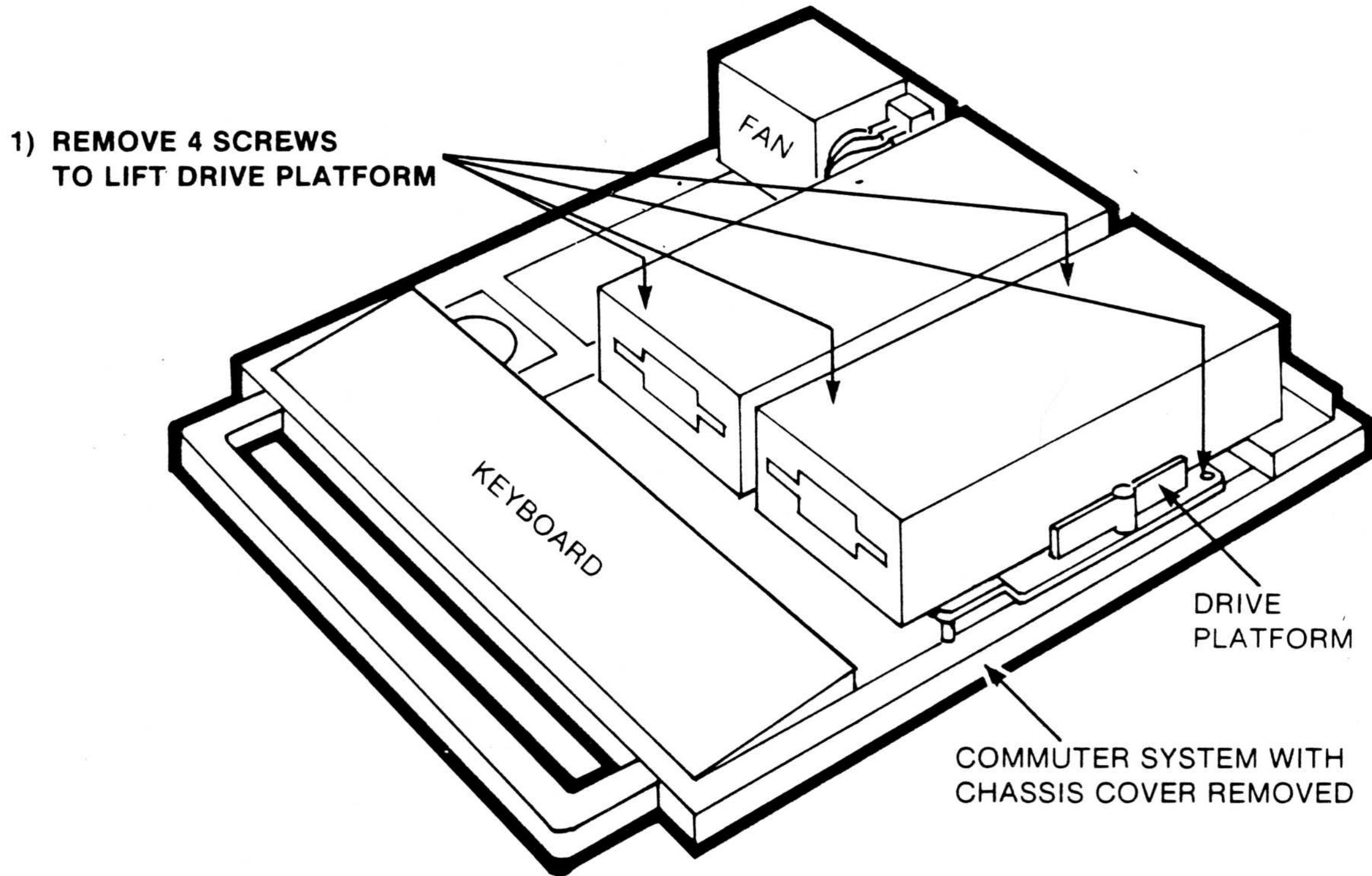
#### 4.3 SETTING THE SWITCHPACK SWITCHES

A switchpack is located on the system PCB under the disk drive platform. The following option installations may require setting one or more switches on the switchpack.

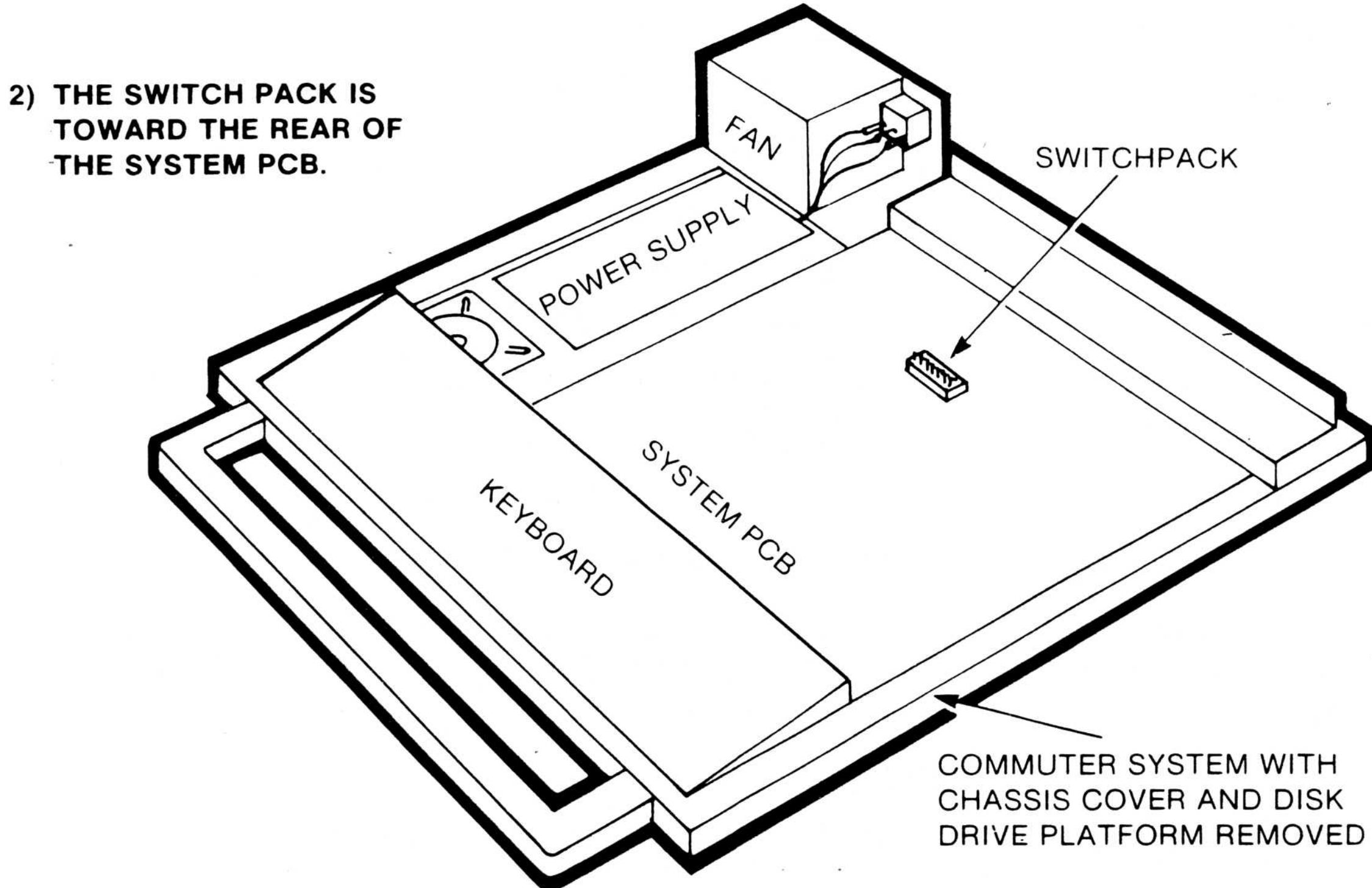
- Additional memory
- 8087 numeric coprocessor
- Second disk drive
- Flat panel LCD display

##### To gain access to the switchpack:

1. Open the chassis cover (refer to section 3.4).
2. Remove the 4 screws that hold the disk drive platform in place (refer to Figure 4-3).
3. Carefully lift the drive platform. It is not necessary to disconnect drive cables unless the platform is to be completely removed.



**Figure 4-3. Gaining Access to the Switchpack (Sheet 1 of 2)**



**Figure 4-3. Gaining Access to the Switchpack (Sheet 2 of 2)**

#### 4.4 INSTALLING ADDITIONAL MEMORY

The Commuter system may be configured to support any of the following amounts of DRAM (dynamic random access memory).

- 128k bytes (standard configuration)
- 256k bytes
- 512k bytes

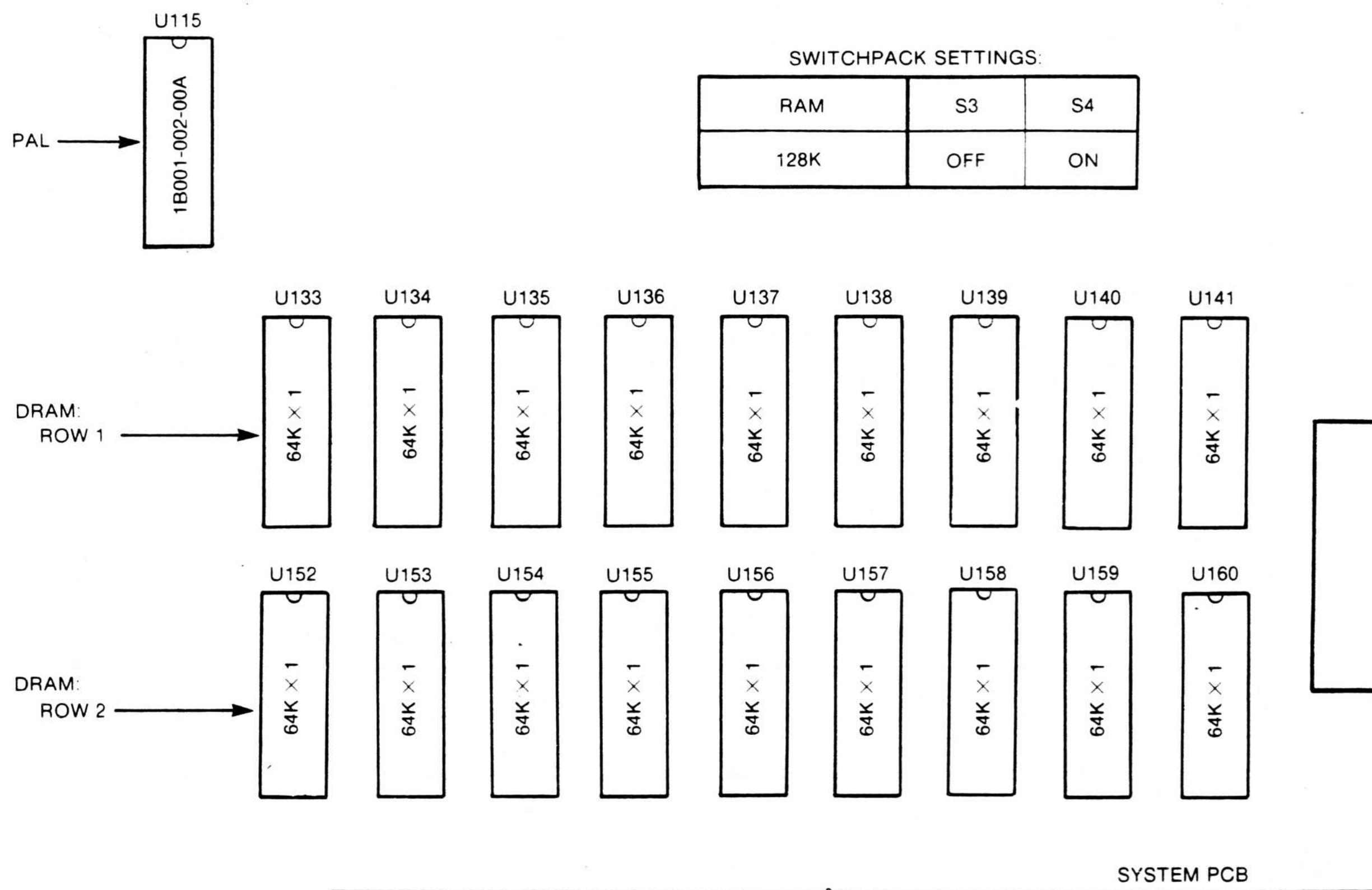
Table 4-1 shows the requirements for each memory configuration.

**Table 4-1. Memory Configuration Requirements**

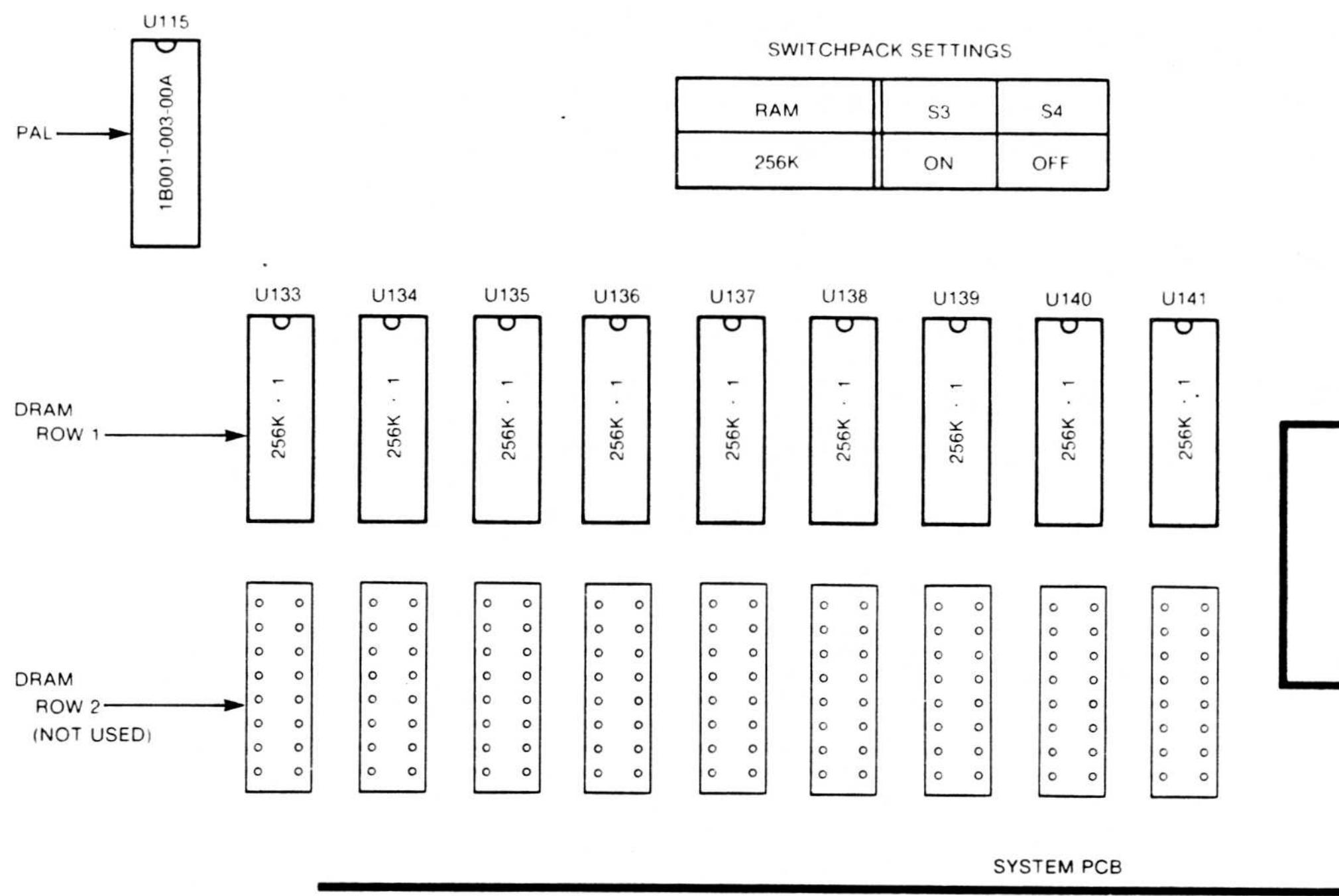
Memory Size	DRAM ICs	PAL Number (U115)	Switchpack S3	S4
128k	64k (two rows)	1B001-002-00A	Off	On
256k	256k (one row)	1B001-003-00A	On	Off
512k	256k (two rows)	1B001-004-00A	Off	Off

**To install any of the memory configurations:**

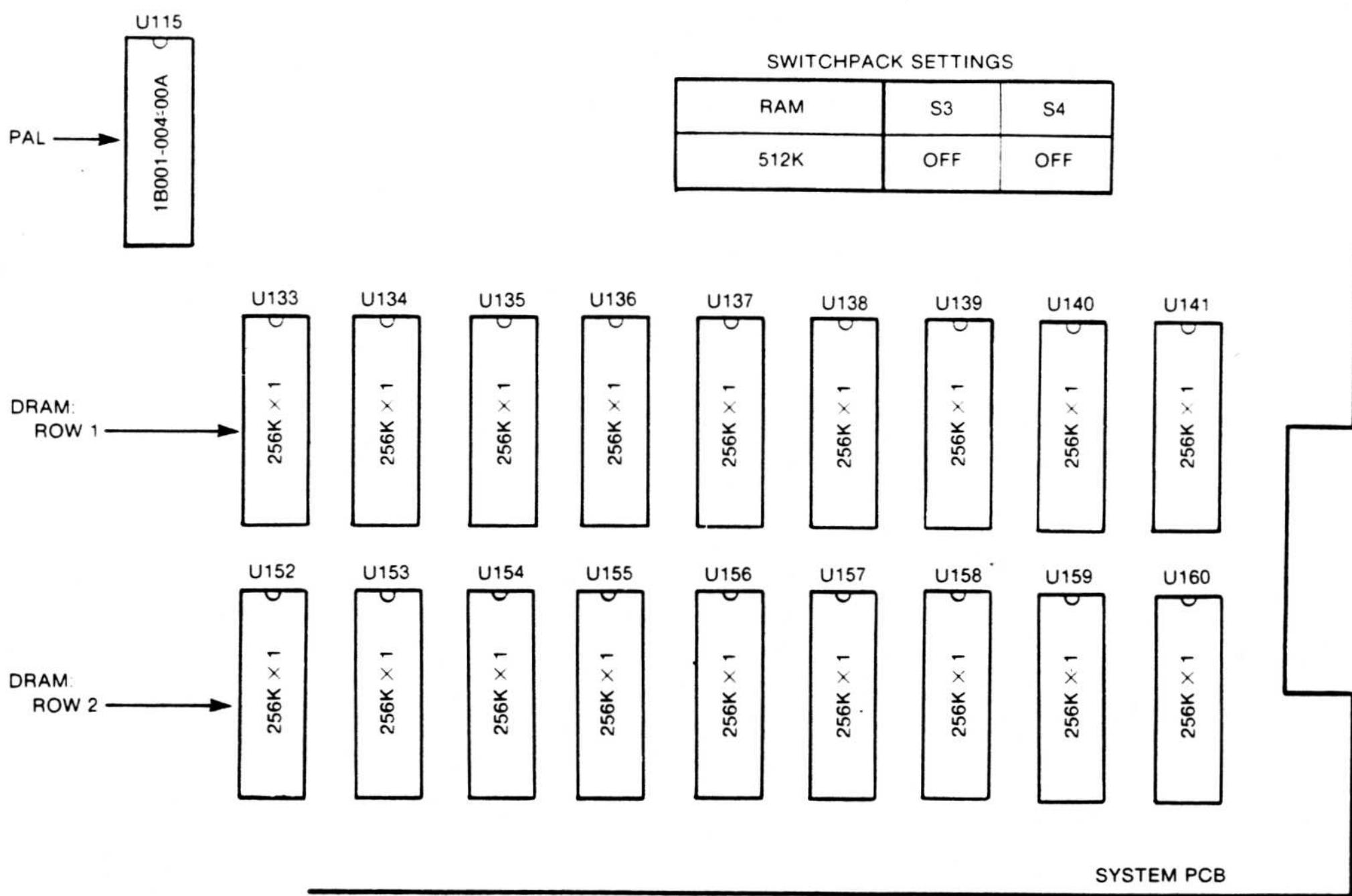
1. Gain access to the DRAM chip sockets (U133-U141 and U152-U160).
  - a. Open the chassis cover (refer to section 3.4).
  - b. Remove the keyboard assembly (refer to section 3.7).
2. Remove the existing ICs from sockets U133-U141 and U152-U160 (sockets U152-U160 may be vacant depending on the configuration installed).
3. Install the DRAM chips and the PAL as shown in the appropriate illustration below.
  - A typical 128k DRAM configuration is shown in Figure 4-4.
  - A typical 256k DRAM configuration is shown in Figure 4-5.
  - A typical 512k DRAM configuration is shown in Figure 4-6.
4. Set the switchpack switches as shown in the appropriate illustration. The switchpack is located under the disk drive platform (refer to section 4.3 to gain access to the switches).
5. Reassemble the Commuter system.
6. Test the installation by running the ROM-based memory diagnostic (refer to section 2.9).



**Figure 4-4. 128k Byte Memory Hardware Configuration**



**Figure 4-5. 256k Byte Memory Hardware Configuration**



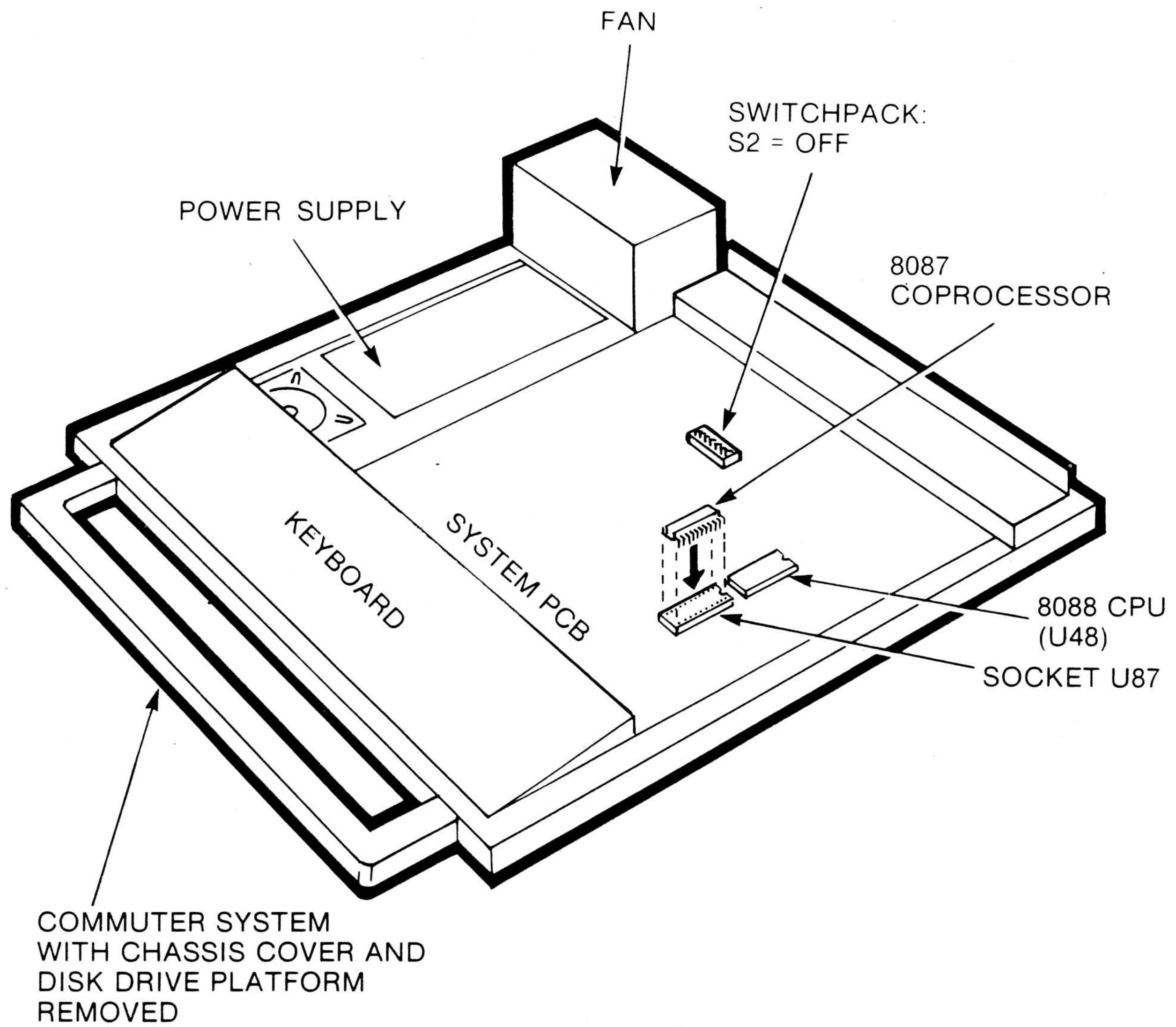
**Figure 4-6. 512k Byte Memory Hardware Configuration**

#### **4.5 INSTALLING AN 8087 NUMERIC COPROCESSOR**

An 8087 numeric coprocessor may be installed in a Commuter system. A coprocessor option consists of one 8087 numeric processor.

##### **To install the 8087 coprocessor:**

1. Locate the 8087 socket (U87) and to the switchpack.
  - a. Open the chassis cover (refer to section 3.4).
  - b. Lift up the disk drive platform (refer to section 4.3).
2. Install the 8087 numeric processor chip in socket U87 as shown in Figure 4-7.
3. Set switchpack switch S2 to OFF.
4. Reassemble the Commuter system.



**Figure 4-7. 8087 Coprocessor Installation**

#### **4.6 INSTALLING A SECOND DISK DRIVE**

A second 5 1/4" disk drive unit may be installed in a Commuter system. The disk drive option consists of a single 5 1/4" disk drive unit.

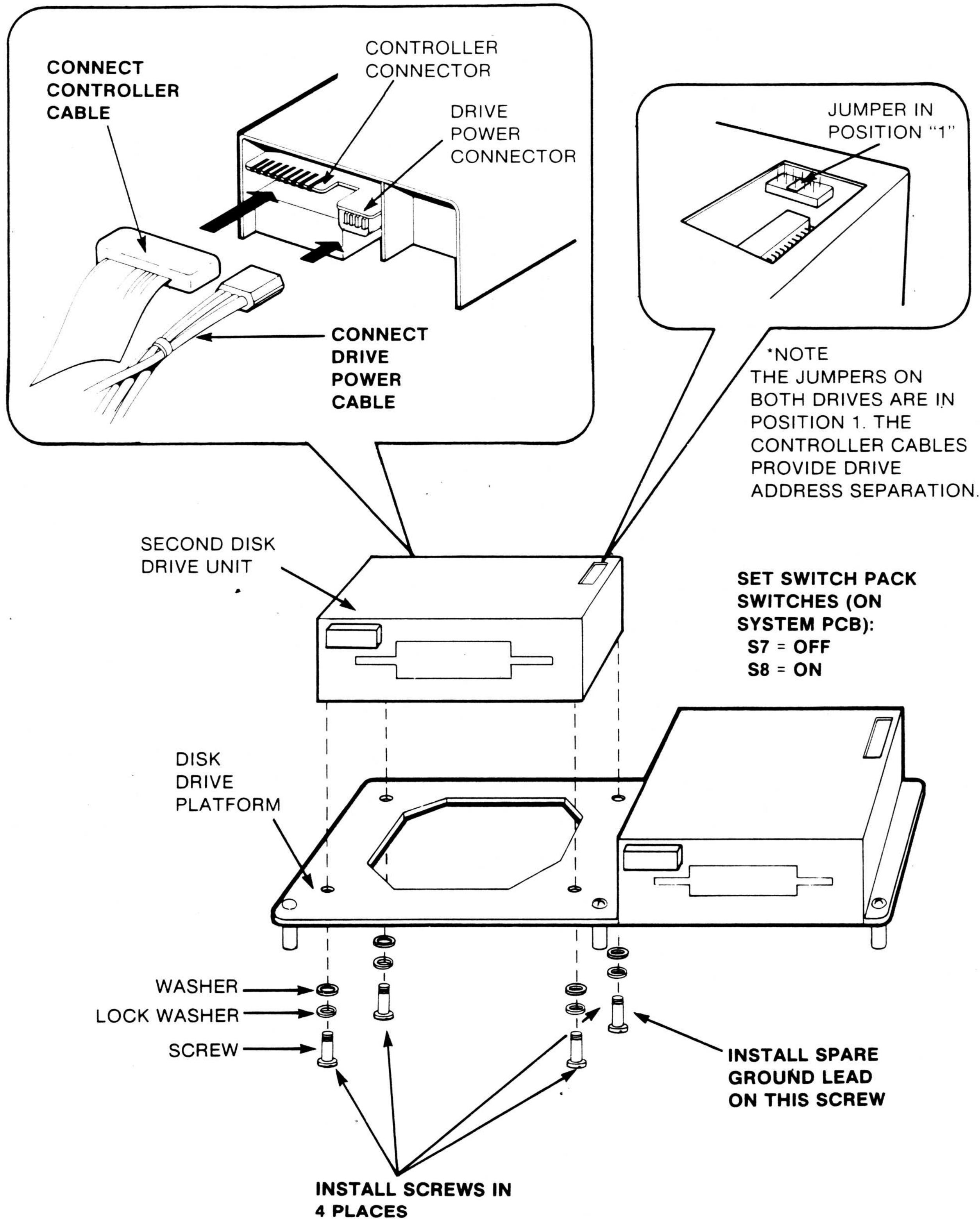
##### **To install a second disk drive unit:**

1. Remove the disk drive platform (refer to section 3.6).
2. Remove the cable ties that secure the unused portion of the drive harness to the drive platform.
3. Set switchpack switches on the system PCB as follows.
  - S7 = Off
  - S8 = On
4. Verify that the jumper on the new drive (refer to Figure 4-8) is in position 1.
5. Mount the second disk drive unit onto the platform as shown in Figure 4-8.

##### **NOTE**

**Be sure to connect the spare ground lead to the new drive unit (the spare lead is secured to the rear left screw of the existing drive as shown in Figure 4-8).**

6. Reassemble the Commuter system.
7. Test the installation by running the ROM-based disk diagnostic (refer to section 2.9).



**Figure 4-8. Second Disk Drive Installation**

#### **4.7 INSTALLING AN LCD FLAT-PANEL DISPLAY**

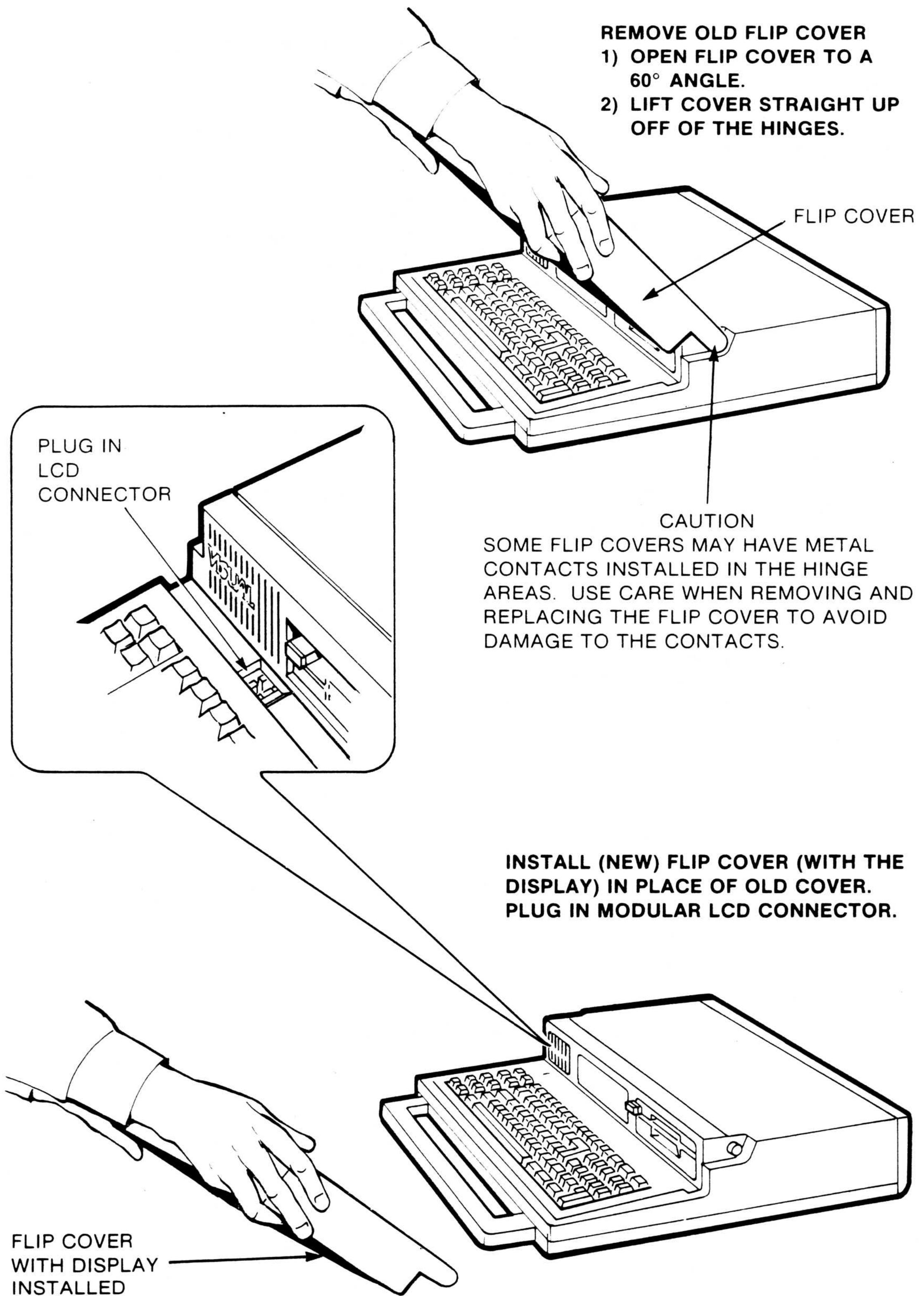
An optional 16 line or 25 line LCD flat-panel display may be installed on a Commuter system. An LCD display option contains one flip cover with a complete LCD display assembly pre-installed.

##### **To install either LCD display:**

1. Remove the old flip cover from the Commuter system (refer to Figure 4-9).
2. Install the flip cover with the LCD display.
3. Plug in the modular connector until it clicks into place.
4. To temporarily enable the LCD display:
  - a. Turn the system power on.
  - b. Wait for the beep. Then:
    - Hold **Ctrl** and **Alt**.
    - Press **L** for 16 line LCD or
    - Press **8** for 25 line LCD.
5. To set the system default to the LCD display:
  - a. Set the switchpack switches as follows:

for 16 line LCD	for 25 line LCD
S5 = On	S5 = On
S6 = On	S6 = Off

The switchpack is located under the disk drive platform. The platform must be lifted up (refer to section 4.3) to gain access to the switches.
  - b. Reassemble the Commuter system.
6. Verify the installation by observing the display during system operation.



**Figure 4-9. LCD Display Installation**

## **4.8 INSTALLING A PROGRAMMABLE RS-232-C SERIAL PORT**

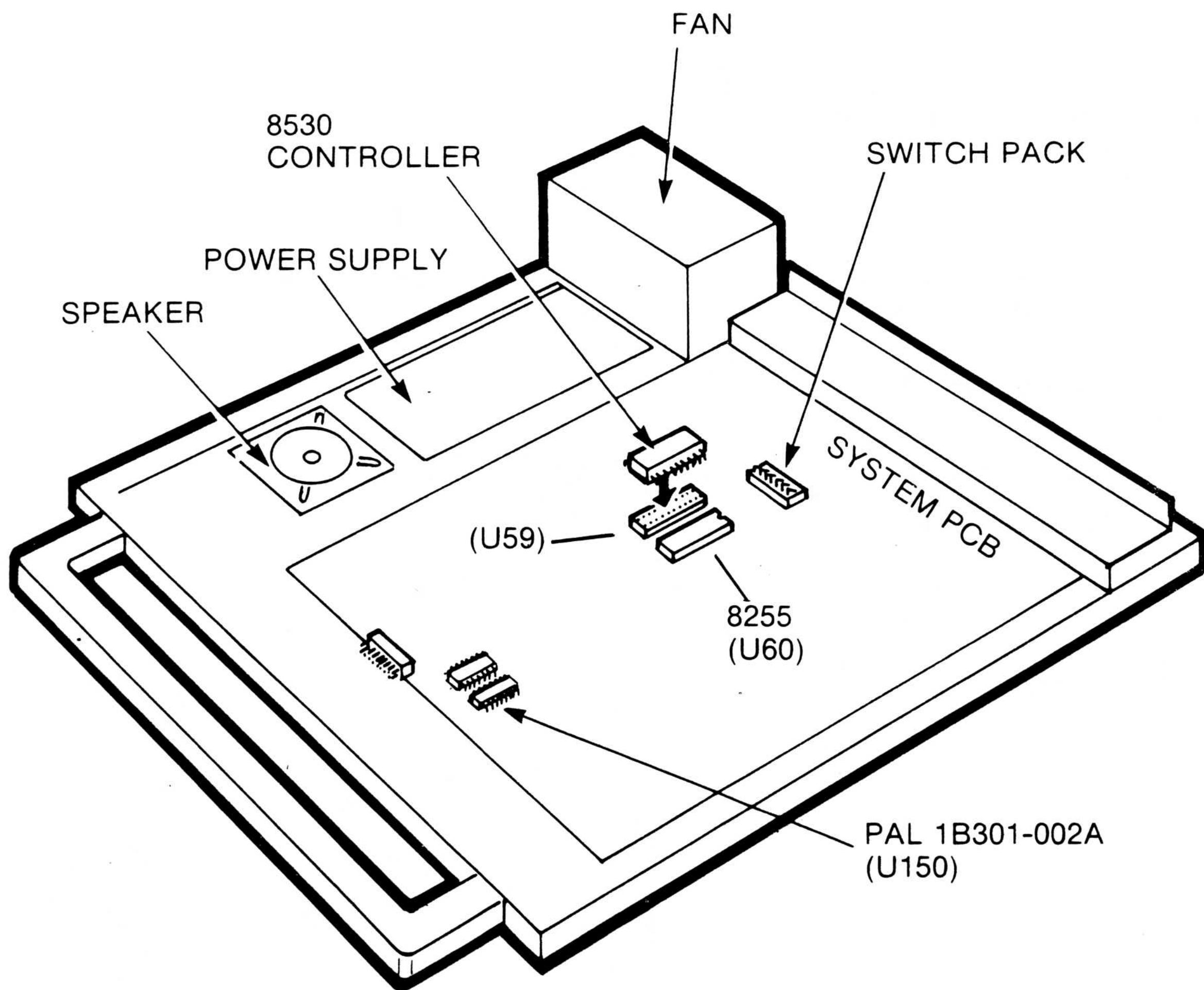
A fully programmable, synchronous/asynchronous serial communications port may be installed in a Commuter system.

The programmable serial port option includes the following hardware.

- Zilog™ 8530 serial I/O communications controller
- Programmable array logic (PAL) IC, Visual Technology Incorporated part number 1B301-002A

### **To install the serial port option:**

1. Gain access to the system PCB.
  - a. Open the chassis cover (refer to section 3.4).
  - b. Remove the keyboard (refer to section 3.7).
  - c. Remove the disk drive platform (refer to section 3.6).
2. Remove existing PAL (1B301-001A) from socket U150.
3. Install new PAL (1B301-002A) in socket U150 (refer to Figure 4-10).
4. Install 8530 controller in socket U59.
5. Reassemble the Commuter system.
6. Test the installation by running the ROM-based communications diagnostic (refer to section 2.9).



**Figure 4-10. Programmable Port Installation**

## 4.9 CHANGING THE COMMUTER OPERATING VOLTAGE

The Commuter system is set at the factory to operate from one of the following input voltages.

- 115 vac; 50-60 Hz
- 230 vac; 50-60 Hz

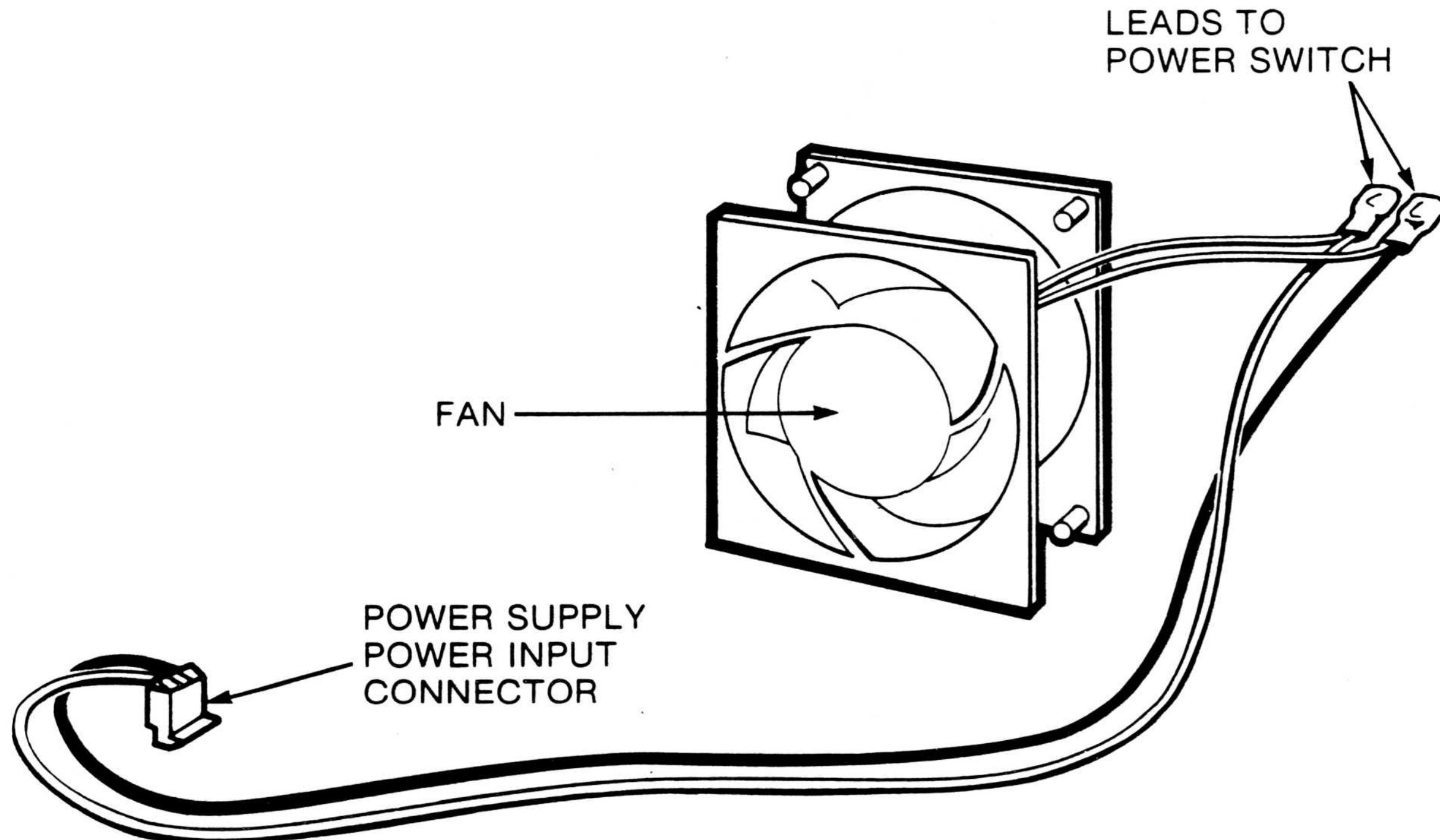
### To change the Commuter system operating voltage:

1. Replace the fan or fan assembly (refer to Figure 4-11) with a unit that operates from the desired input voltage.

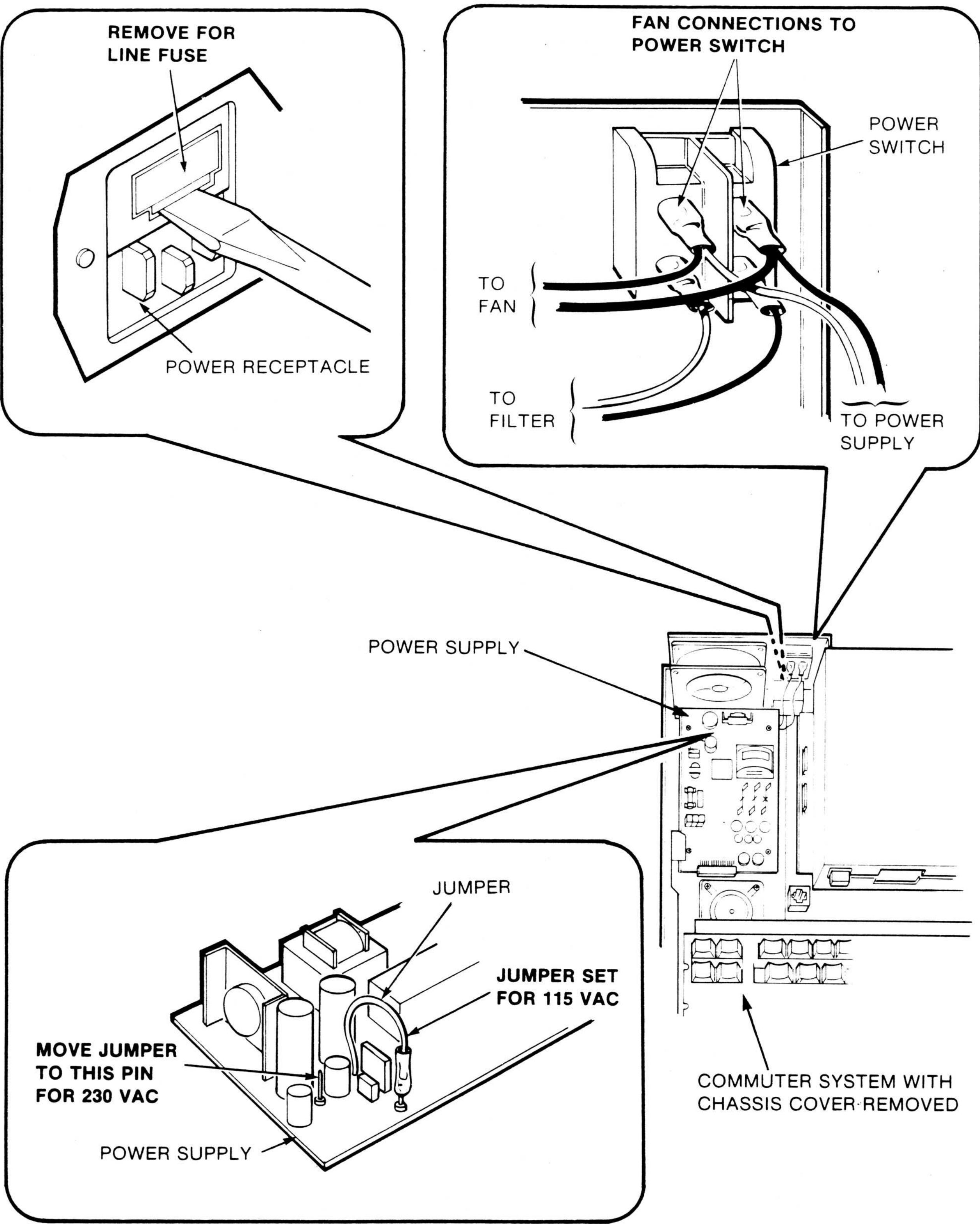
#### NOTE

**If replacing the entire fan assembly, the power supply must be removed (refer to section 3.5).**

2. Move the jumper on the power supply to the pin that selects the desired input voltage (refer to Figure 4-12).
3. Replace the line fuse with one of the following fuses.
  - For 115 vac - 2.0 Amp
  - For 230 vac - 1.0 Amp



**Figure 4-11. Commuter Fan Assembly**



**Figure 4-12. Commuter Voltage Selection Wiring**



## **CHAPTER 5**

### **THEORY OF OPERATION**

#### **5.1 OVERVIEW**

This chapter provides information that may be used to isolate component failures on the system PCB. Knowledge of logic and VLSI theory as well as specialized equipment may be required to troubleshoot to the component level.

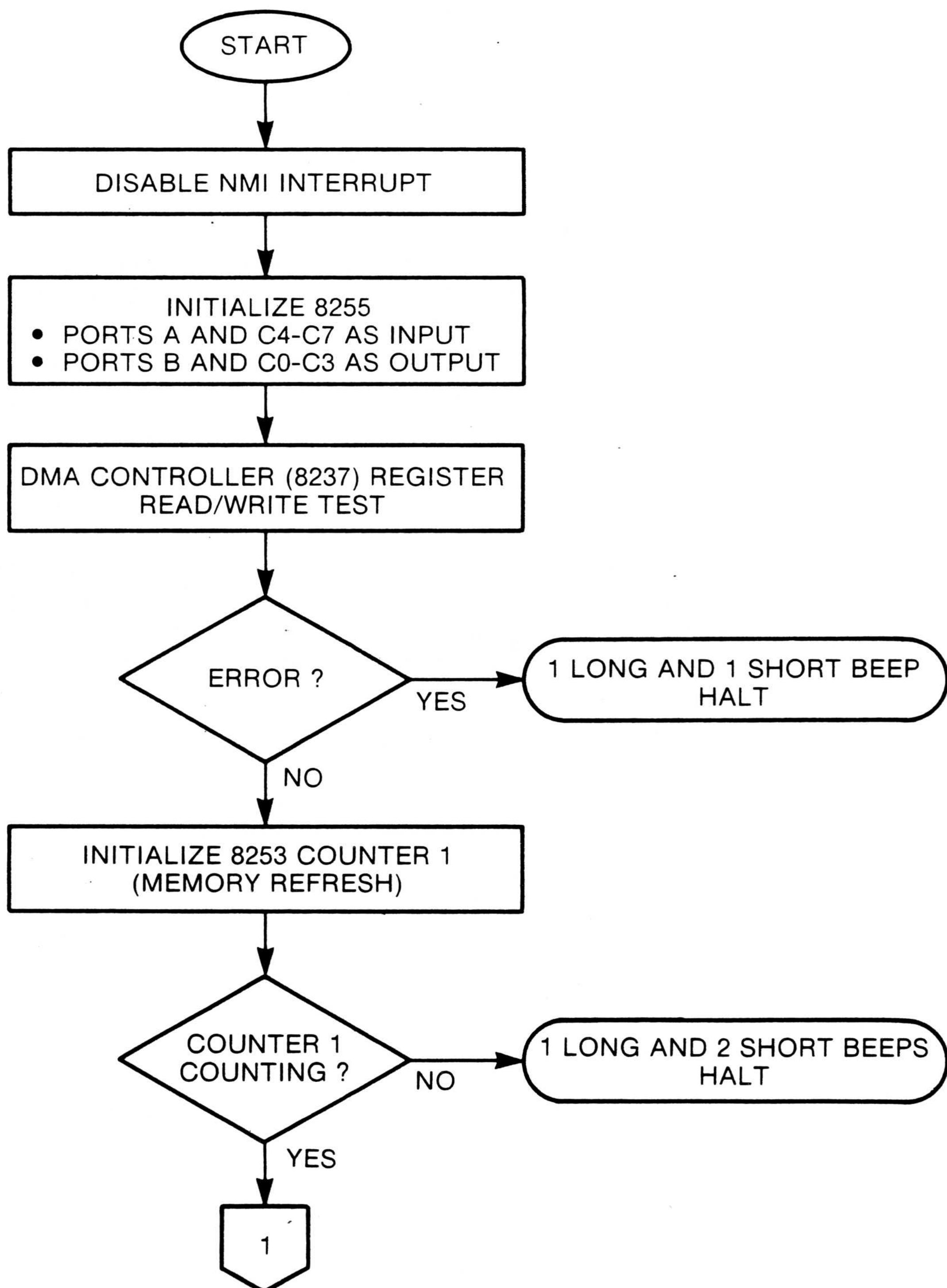
The following topics are discussed:

- System power-up sequence
- Circuit descriptions

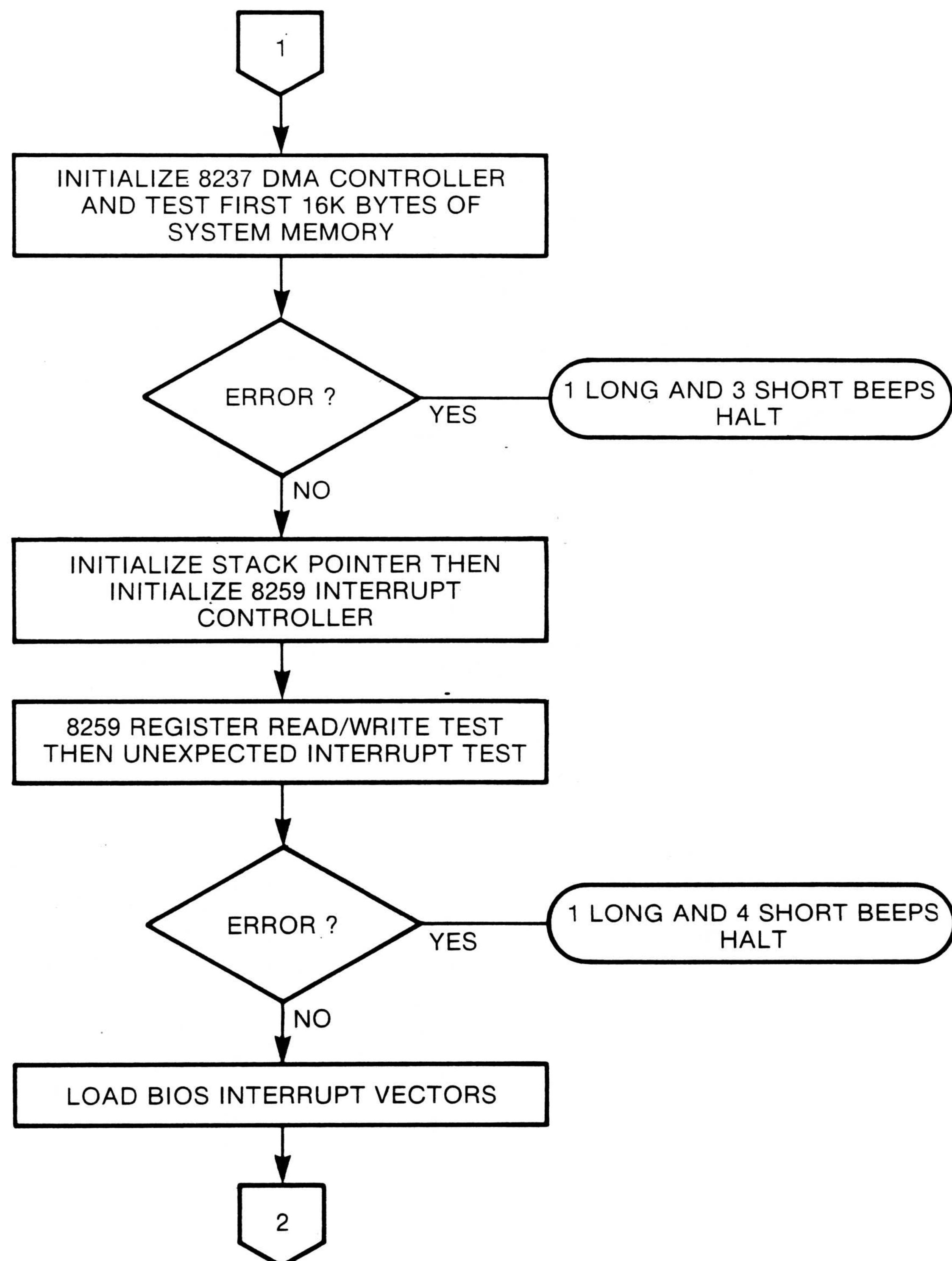
#### **5.2 POWER-UP SEQUENCE**

When the system is turned on, the 8284 clock controls the system power-up reset. The RESET pulse sets all of the registers to a known state and initiates a ROM-controlled system startup and self-test. The RESET signal must be active (high) for at least four clock cycles. Program execution begins at location FFFF0 (hex) after the RESET signal returns low.

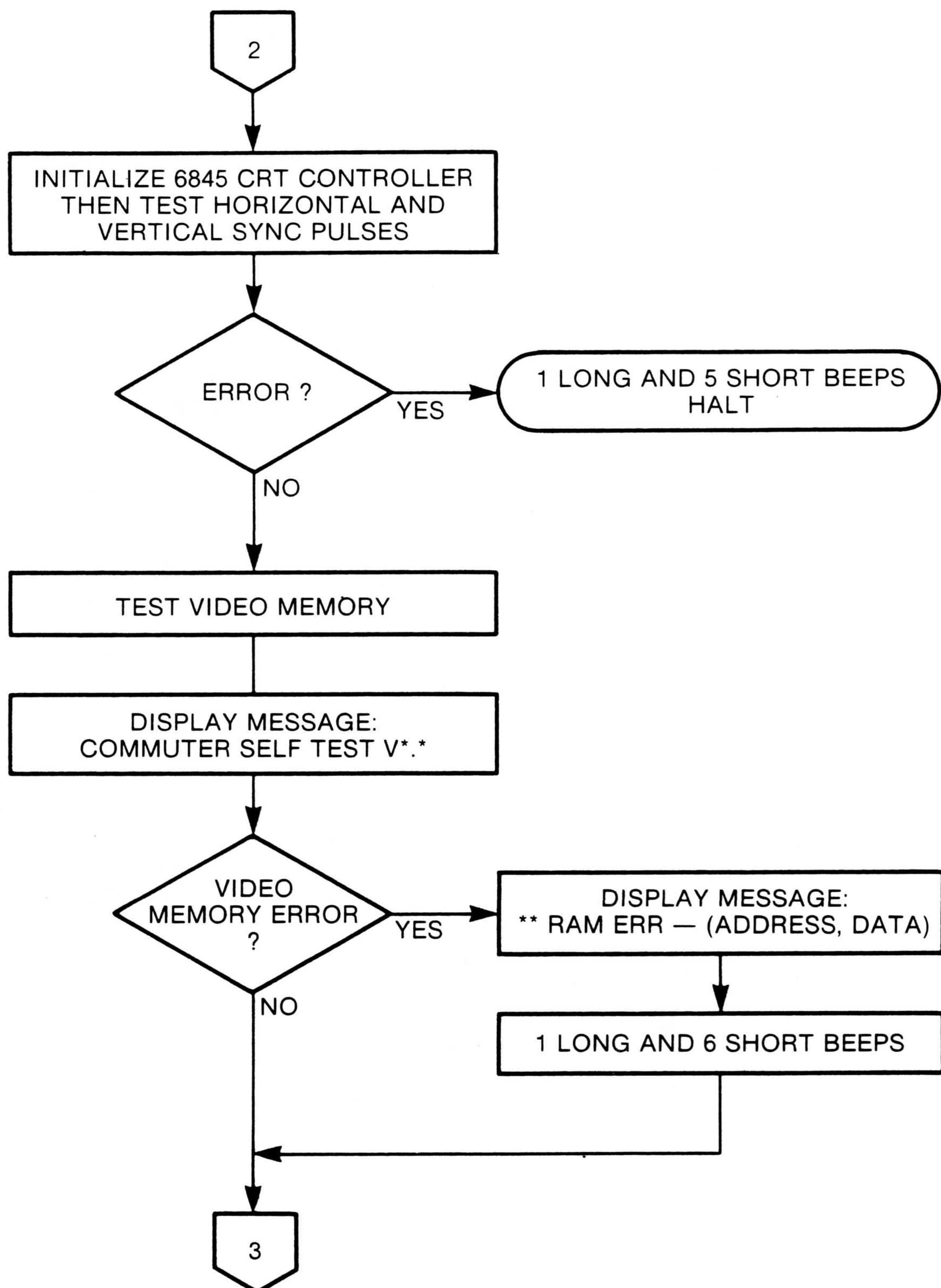
The flow diagram in Figure 5-1 indicates the program control sequence that occurs after the RESET pulse.



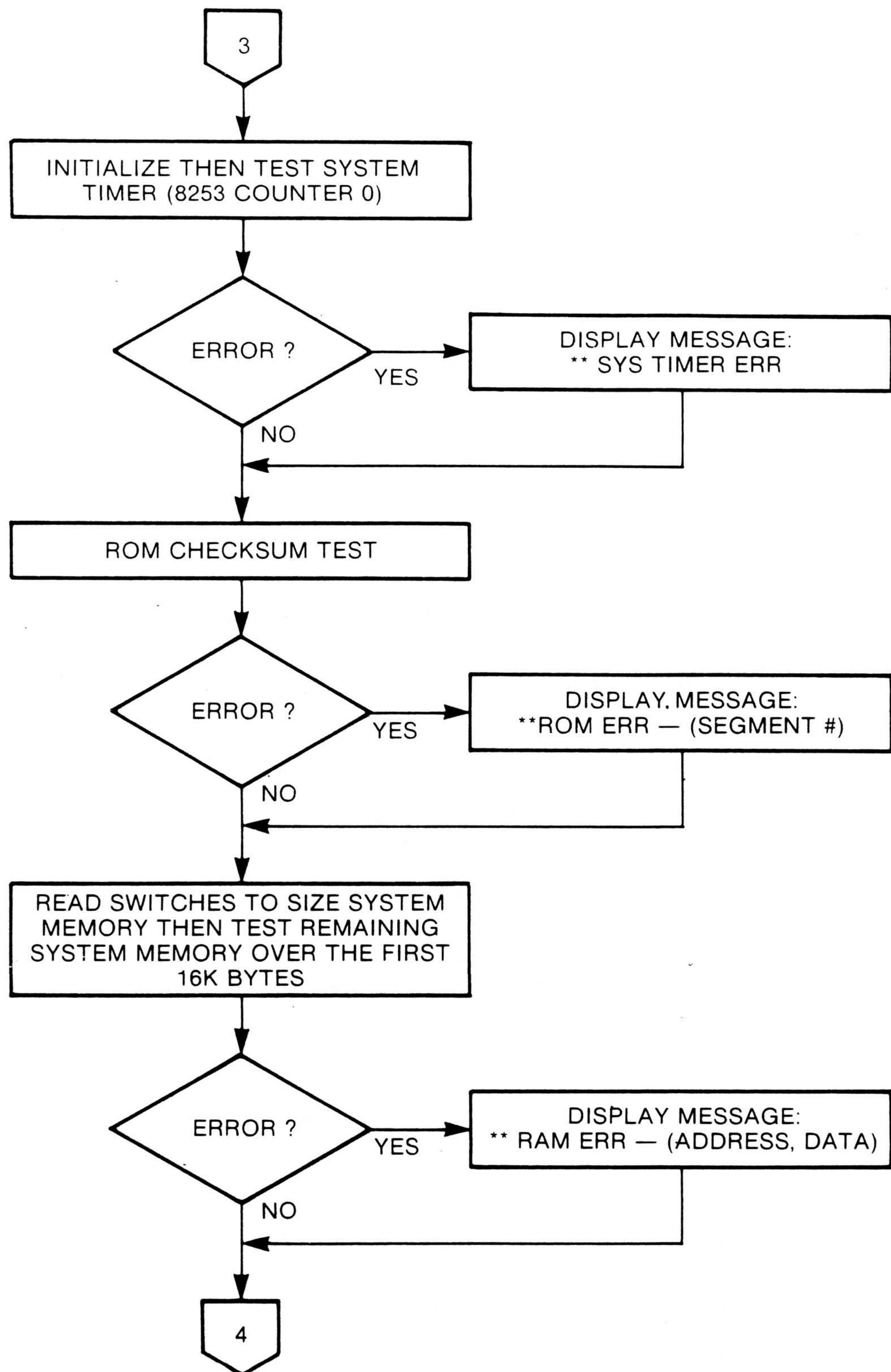
**Figure 5-1. Power-Up Sequence Flow Diagram (Sheet 1 of 7)**



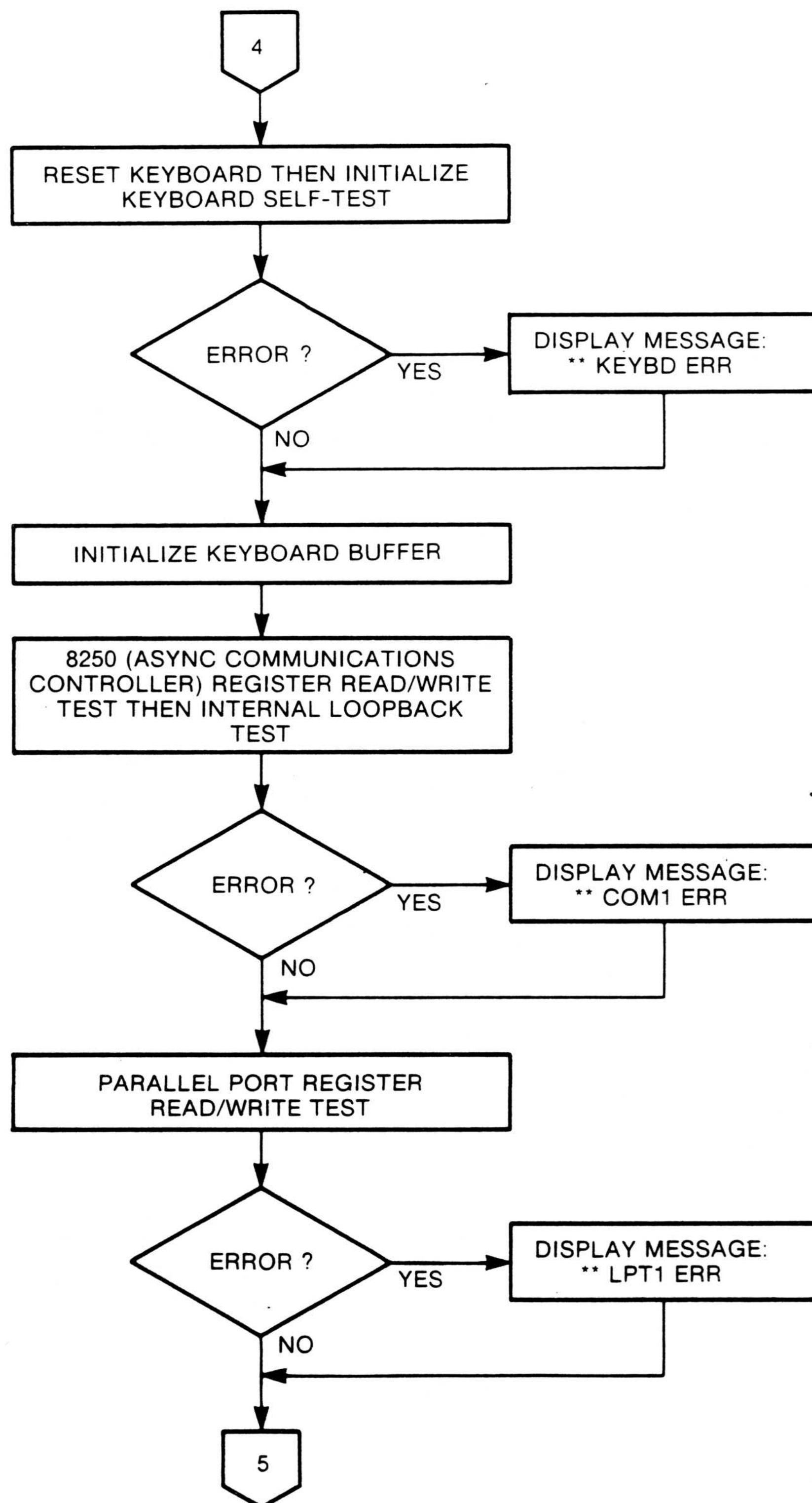
**Figure 5-1. Power-Up Sequence Flow Diagram (Sheet 2 of 7)**



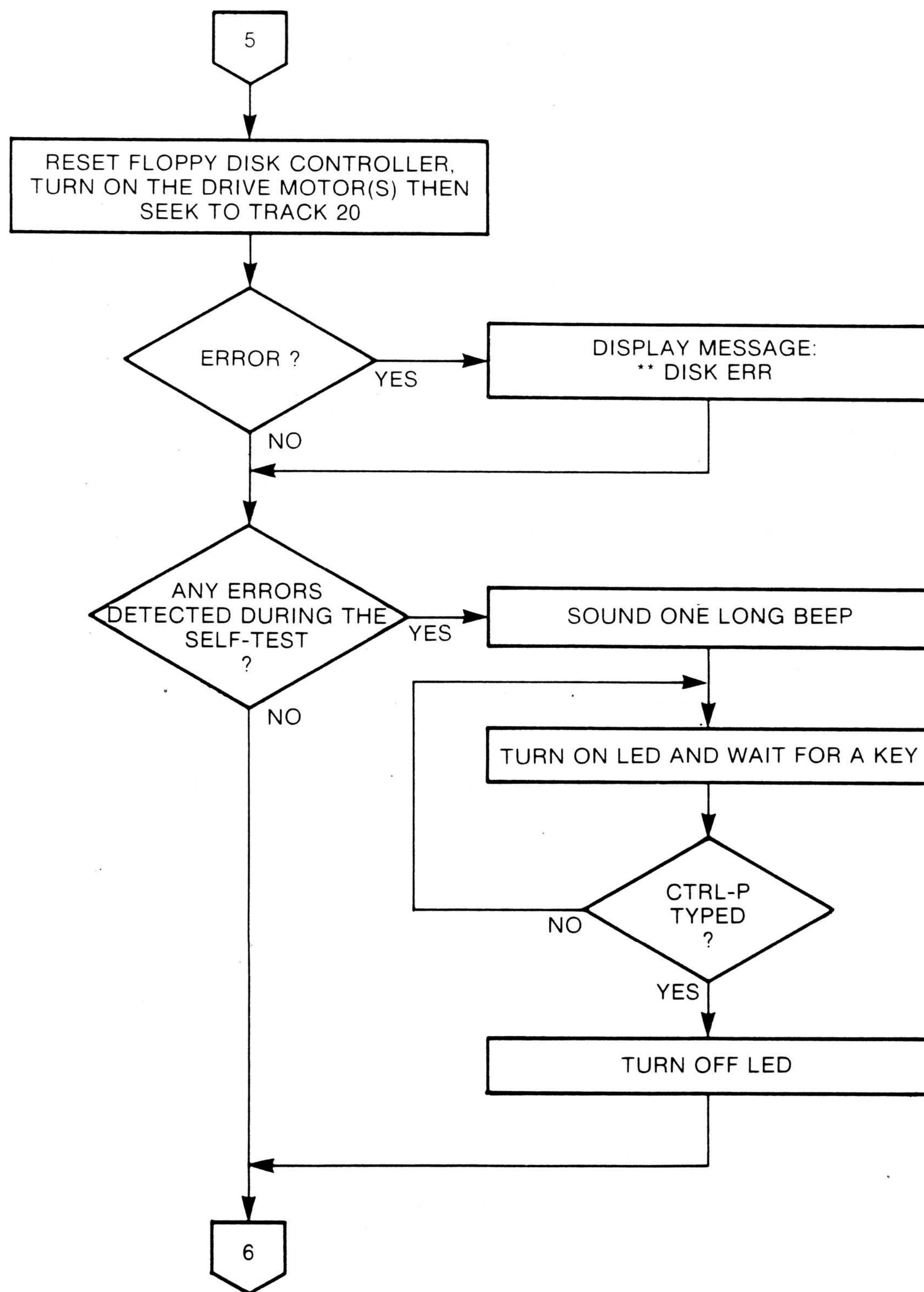
**Figure 5-1. Power-Up Sequence Flow Diagram (Sheet 3 of 7)**



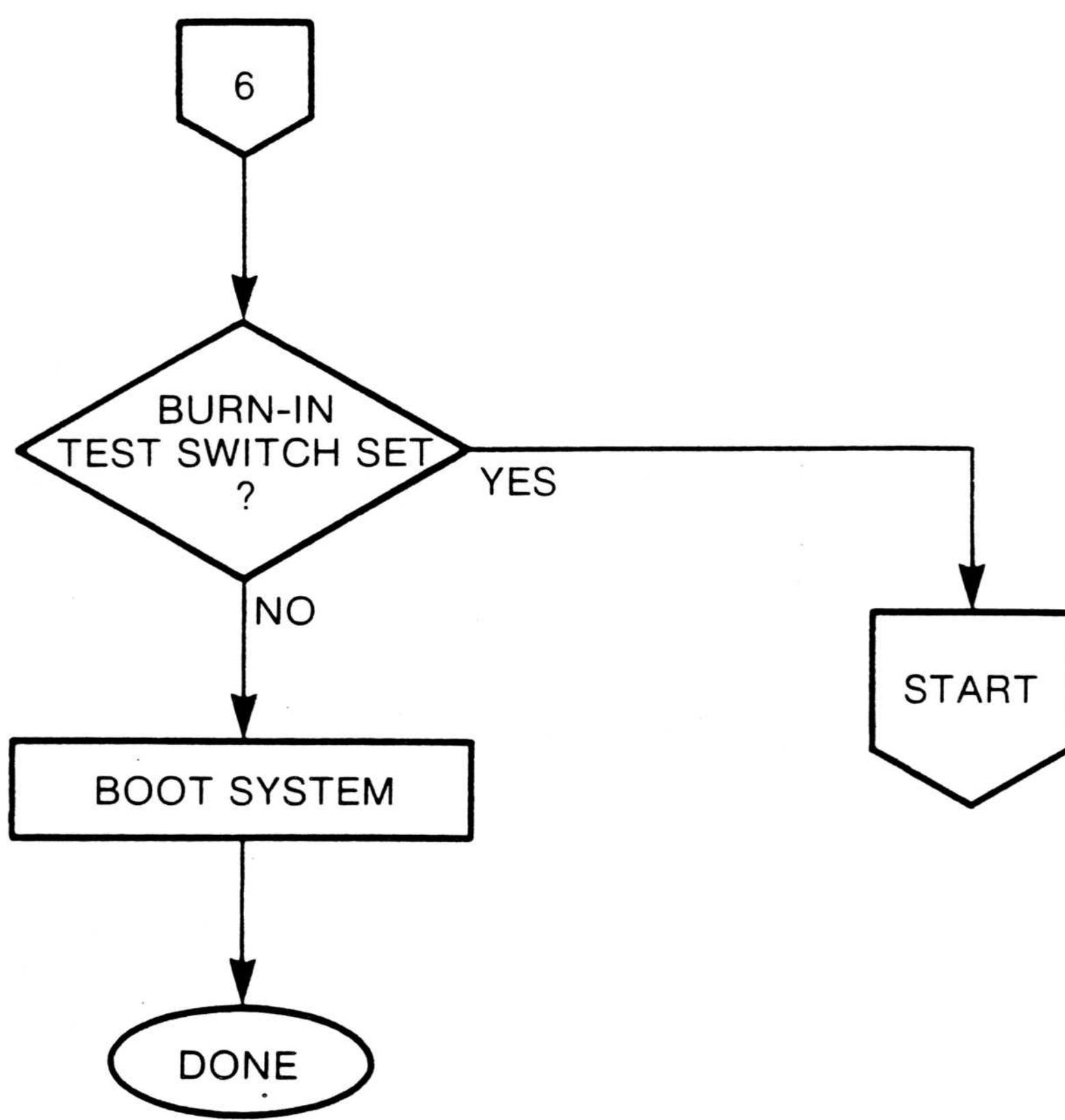
**Figure 5-1. Power-Up Sequence Flow Diagram (Sheet 4 of 7)**



**Figure 5-1. Power-Up Sequence Flow Diagram (Sheet 5 of 7)**



**Figure 5-1. Power-Up Sequence Flow Diagram (Sheet 6 of 7)**



**Figure 5-1. Power-Up Sequence Flow Diagram (Sheet 7 of 7)**

### **5.3 CIRCUIT DESCRIPTIONS**

The electronic circuitry of the Commuter system is made up of the following functional blocks:

- CPU and support logic
- Interrupt controller
- DMA (direct memory access) controller
- DMA page register
- Numeric data coprocessor (optional)
- System timers
- System memory
- Programmable peripheral interface
- Keyboard controller
- Floppy disk controller and support logic
- Asynchronous serial communication
- Synchronous/asynchronous serial communication
- Parallel printer interface
- Video controller and support logic
- Expansion port interface

The block diagram shown in Figure 5-2 illustrates relationships between functional blocks of the Commuter system.

#### **5.3.1 CPU and Support Logic**

The CPU and support logic includes the following components.

- 8088 microprocessor (operated in maximum mode)
- Bus arbitration logic
- 8284 clock generator
- 8288 bus controller
- 8259 interrupt controller

#### **8088 MICROPROCESSOR**

The 8088 microprocessor is operated in maximum mode at 4.77 MHz. The maximum mode extends system architecture to support multiprocessor configurations (8237 DMA controller) and local instruction set extension processors such as an 8087 numeric co-

processor. A bus controller (8288), rather than the CPU, provides all bus control and command outputs. This allows the CPU pins previously delegated to these functions to be redefined to support multiprocessing functions.

### **Bus Arbitration Logic**

Normally, the 8088 CPU is the bus master and initiates all data transfers within the system. However, two other devices may become bus master. They are:

- The 8237 DMA controller and
- The 8087 numeric coprocessor.

The bus arbitration logic controls transfer of the system bus back and forth between the 8088 CPU and the 8237 DMA controller. The 8088 CPU is the default bus master. When the DMA controller is not requesting control, bus control is always given to the 8088 CPU.

The 8087 numeric coprocessor gains control of the bus via a bus arbiter that is built into the 8087 and 8088 devices. This bus arbiter includes a request and grant control line (RG0/GT0) that runs between both devices.

### **Hardware Interrupts**

Two types of hardware interrupts are used in the Commuter system.

- Non-maskable interrupt (NMI)
- Interrupt request levels IRQ0 through IRQ7

An NMI (non-maskable interrupt) is a non-maskable interrupt level and is handled directly by the 8088 CPU. The 8259 interrupt controller (U86) provides eight additional (prioritized) interrupt request levels (IRQ0 through IRQ7 with IRQ0 having the highest priority). These levels can be masked through the 8259 registers.

Since the NMI cannot be masked inside the CPU, an external hardware mechanism is provided to mask off NMI during system power-up. System software may also be used to set and reset the mask bit as follows.

- Set mask (enable NMI): write hex 80 to I/O address 00A0.
- Clear mask (disable NMI): write hex 00 to I/O address 00A0.

An NMI (if enabled) may come from any of three sources.

- On-board system memory issues an NMI whenever a parity error is detected during a read operation. Once a parity error has occurred, the error condition is latched until the EN PAR ERR (enable parity error) line goes inactive (low).
- The 8087 coprocessor (if one is installed) issues an NMI whenever an illegal operation (such as divide by 0) is attempted.
- The expansion chassis port provides a signal called I/O channel error (IOCHK). This signal corresponds to a line that connects to the expansion chassis port. Options installed in the expansion chassis may initiate an NMI by driving the error line active (low).

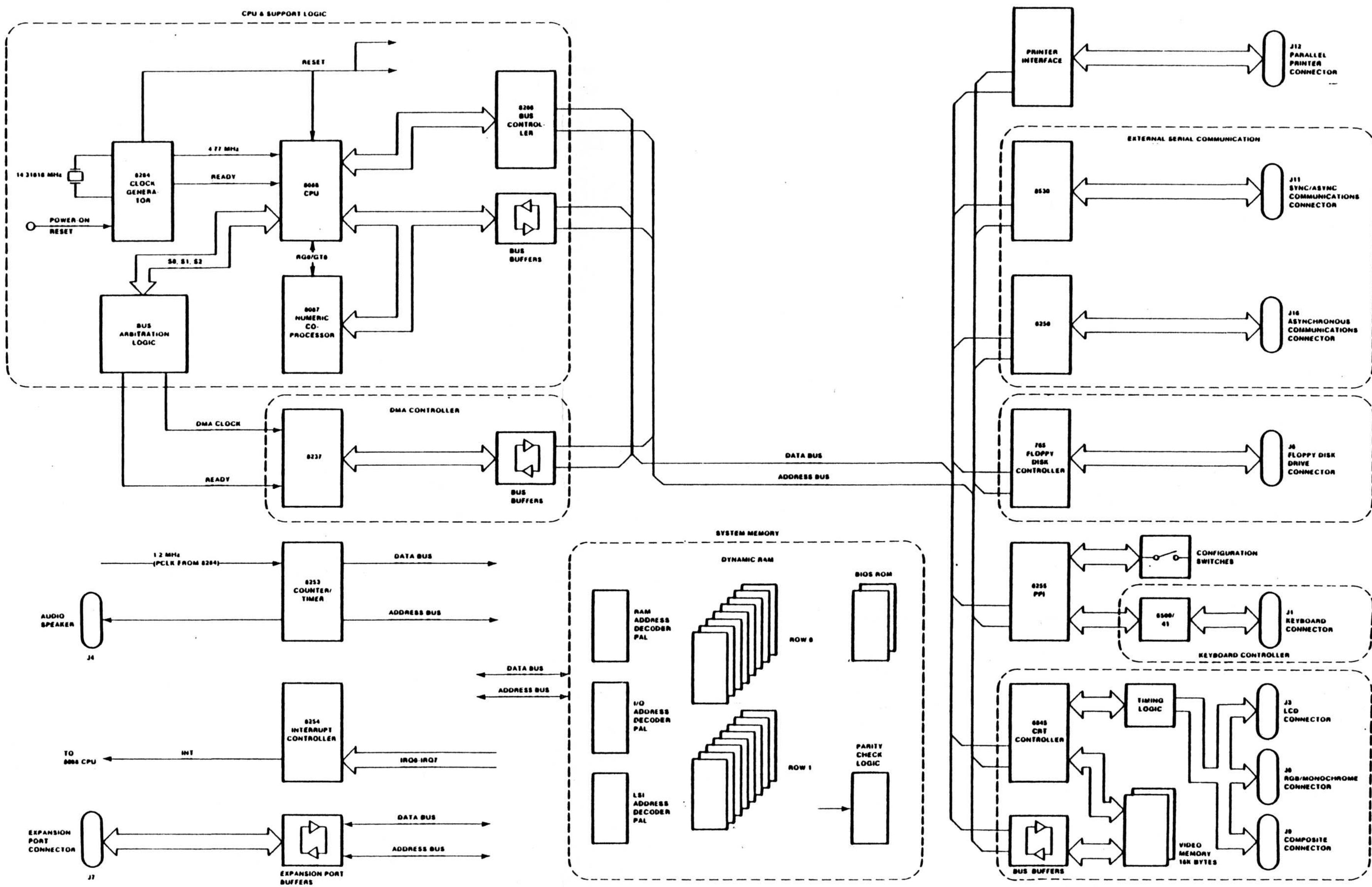


Figure 5-2. Commuter System Block Diagram



The source of an NMI is determined by PC6 and PC7 of the 8255 (U60) parallel I/O controller (refer to Section 5.3.8).

## 8284 CLOCK GENERATOR

The 8284 clock generator provides a 4.77 MHz clock to the 8088 CPU (the crystal frequency of 14.31818 MHz is divided by three). Thus each cycle is approximately 210 nanoseconds in duration.

Most bus cycles require four clock cycles to complete. However, some bus cycles requires an additional clock cycle. Table 5-1 shows the number of clock cycles required to complete various bus cycles.

**Table 5-1. Bus Cycle Duration**

Bus Cycle	Number of Clock Cycles
Memory read of system ROM or RAM	4
Memory write to system RAM	4
Read/write to I/O	5
Read/write to expansion port	5

## 8288 BUS CONTROLLER

The 8288 bus controller commands I/O devices or the memory system to read data from or write data to the data bus. The controller is enabled by the arbitration support logic (88ENB) and is steered by inputs S0, S1 and S2 from the 8088 CPU when the 8088 is the intended bus master.

### 5.3.2 8259 Interrupt Controller

The 8259 interrupt controller (U86) supports interrupt request levels IRQ0 through IRQ7. Table 5-2 indicates the source(s) of each level of interrupt.

**Table 5-2. Interrupt Sources**

Interrupt Level	Source
IRQ0	8253 timer (U113) channel 0
IRQ1	6500 keyboard controller
IRQ2	Expansion port
IRQ3	8530 communication controller (U59), Expansion port
IRQ4	8250 Asynchronous controller (U72)
IRQ5	Expansion port (hard disk option)
IRQ6	765 floppy disk controller (U27)
IRQ7	Parallel printer

Two I/O registers are used to program and monitor the 8259 interrupt controller. The I/O register addresses and their functions are described in Table 5-3.

**Table 5-3. 8259 Interrupt Controller Register Descriptions**

I/O Address	Read/ Write*	Register Function
0020	R	Interrupt request register Bits 0-7 for IRQ0 to IRQ7 Bit = 1 indicates interrupt request on
0020	R	In service register Bits 0-7 for IRQ0 to IRQ7
0020	W	Initialization command word 1
0021	W	Initialization command word 2
0021	W	Initialization command word 3
0021	W	Initialization command word 4
0021	R/W	Interrupt mask register
0021	R	Operation control word 2
0021	R	Operation control word 3

\*R = read only; W = write only; R/W = read and write.

### 5.3.3 DMA (Direct Memory Access) Controller

The 8237 DMA controller (U64) permits high speed data transfers between I/O devices and memory. The controller supports four prioritized channels, 0, 1, 2 and 3, with channel 0 having the highest priority. Each channel includes a request (DREQ) and acknowledge (DACK) control line. The channels have the following functions:

- Channel 0 enables a Dynamic RAM refresh by forcing a read from memory. DREQ0 is invoked from the 8253 system timer (U113).
- Channel 1 connects to the expansion port (J7) and may be used by options installed in an expansion chassis if one is being used.
- Channel 2 connects to the 765 floppy disk controller (U27).
- Channel 3 connects to the expansion port (J7) and may be used by options installed in an expansion chassis if one is being used.

When a DREQ is received, the 8327 controller sends an HRQ (hold request) to the bus arbitration logic. The HRQ and the status of the CPU (LOCK\*, S1 and S2) is used by the arbitration logic to give bus control to the DMA controller.

Sixteen I/O registers are used to program and monitor the DMA controller. These registers are described in Table 5-4.

**Table 5-4. DMA Controller Register Descriptions**

I/O Address	Read/ Write*	Register Function
0000	R/W	DMA channel 0 address (memory refresh)
0001	R/W	DMA channel 0 count
0002	R/W	DMA Channel 1 address (expansion port)
0003	R/W	DMA Channel 1 count
0004	R/W	DMA Channel 2 address (floppy disk controller)
0005	R/W	DMA Channel 2 count
0006	R/W	DMA Channel 3 address (expansion port)
0007	R/W	DMA Channel 3 count
0008	R	DMA status
0008	W	DMA command
0009	W	DMA request
000A	W	Write single mask bit
000B	W	DMA mode
000C	W	Clear byte point flip flop
000D	R	Read temporary register
000D	W	Master clear for all registers
000E	W	Clear mask register
000F	W	Write all mask register bits

\*R = read only; W = write only; R/W = read and write.

#### 5.3.4 DMA Page Register

An LS670 (U75) is used as a DMA page register that expands DMA addressing to 20 bits. The page register contains four four-bit memory locations that are written into by the CPU. Thus each of the four DMA channels has its own page register. DACK control lines and DMAENB (DMA enable) enable the chip to read the contents of the appropriate register onto address bus lines A16 - A19.

The I/O register addresses and their functions are described in Table 5-5.

**Table 5-5. DMA Page Register Descriptions**

I/O Address	Read/ Write*	Register Function
0080	W	DMA Channel 0 page register
0081	W	DMA Channel 1 page register
0082	W	DMA Channel 2 page register
0083	W	DMA Channel 3 page register

\*R = read only; W = write only; R/W = read and write.

### 5.3.5 8087 Numeric Data Coprocessor

The optional 8087 coprocessor resides on the local bus with the 8088 CPU and maintains synchronization by monitoring the CPU status and queue status lines (S0-S2 and QS0-QS1). When errors are detected, the 8087 coprocessor sends an NMI (non-maskable interrupt) to the CPU.

The 8087 numeric coprocessor gains control of the bus via a bus arbiter that is built into the 8087 and 8088 devices. The bus arbiter includes a request and grant control line (RG0/GT0) that runs between both devices.

The 8087 coprocessor is dedicated to performing arithmetic and logical operations on a variety of numeric data types.

### 5.3.6 8253 System Timer

The 8253 timer (U113) provides three programmable intervals used to time various system events. All three counters derive their timing from a 1.2 MHz clock (PCLK divided by two). The counters have the following functions:

- Counter 0 is used as a system timer. The counter issues an interrupt request (IRQ0) every 55 microseconds. This interrupt causes the CPU to increment a software count that may be used by the operating system (MS-DOS) to increment the time of day.
- Counter 1 is used as the time base for Dynamic RAM refresh. The counter issues a DMA request (DREQ0) to the DMA controller approximately every 16 microseconds on DMA channel 0. The DMA controller then forces a memory refresh (refer to Section 5.3.3).
- Counter 2 is used as the frequency source for the audio speaker. Different count down values programmed into the 8253 timer via the data bus permit generation of various tones.

Four I/O registers are used to program and monitor the 8253 timer. The I/O register addresses and their functions are described in Table 5-6.

**Table 5-6. 8253 System Timer Register Descriptions**

I/O Address	Read/Write*	Register Function
0040	R/W	Timer/counter 0
0041	R/W	Timer/counter 1
0042	R/W	Timer/counter 3
0043	W	Mode register

\*R = read only; W = write only; R/W = read and write.

### 5.3.7 System Memory

This section describes the system memory. Two topics are discussed.

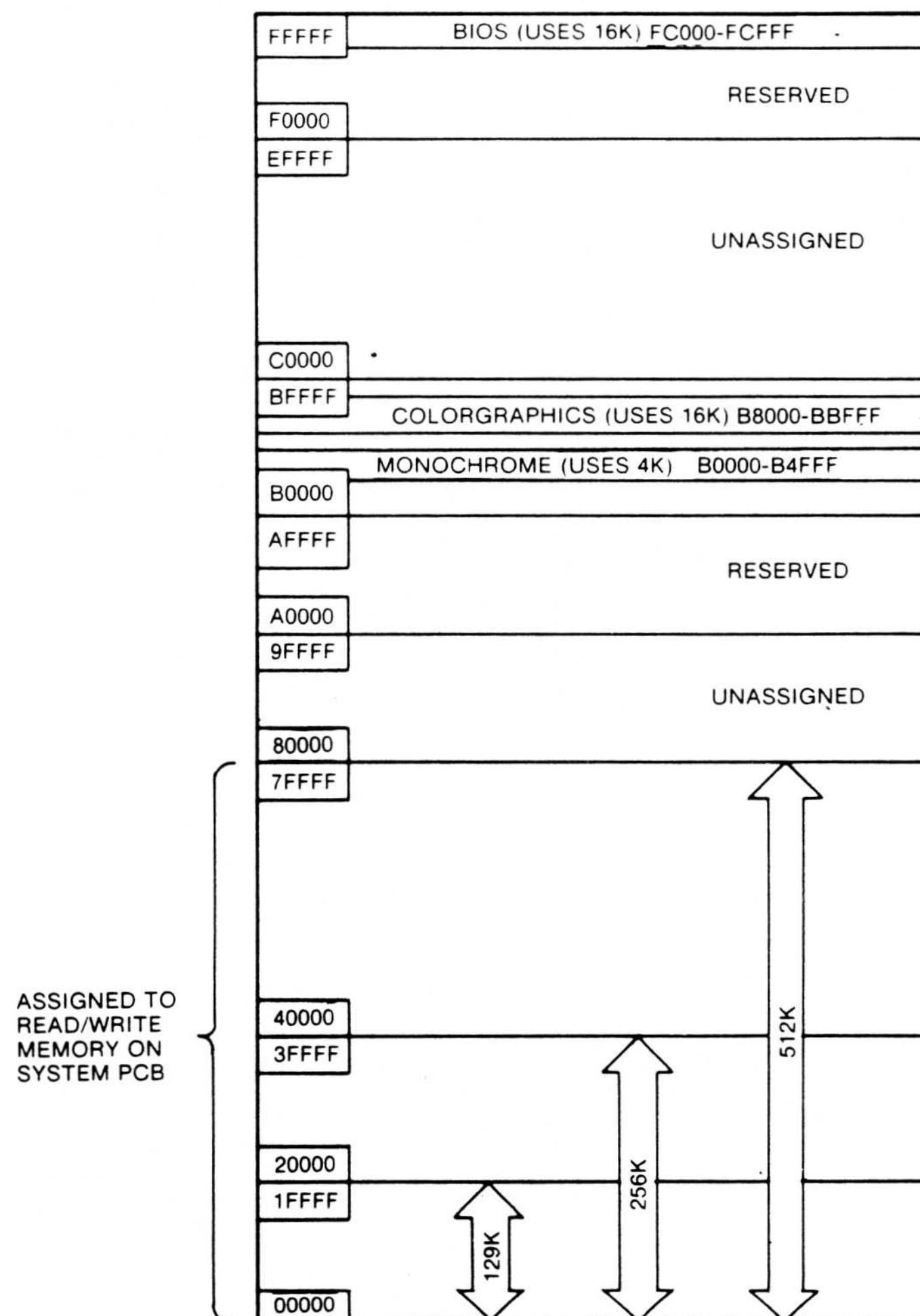
- Memory allocation
- Hardware configurations

### MEMORY ALLOCATION

System memory is made up of the following components.

- Up to 512k bytes of on-board DRAM (Dynamic RAM)
- 16k bytes of video memory
- 64k bytes of ROM (BIOS)

A memory map is shown in Figure 5-3. The map illustrates the boundaries for each allocated area in the system memory.

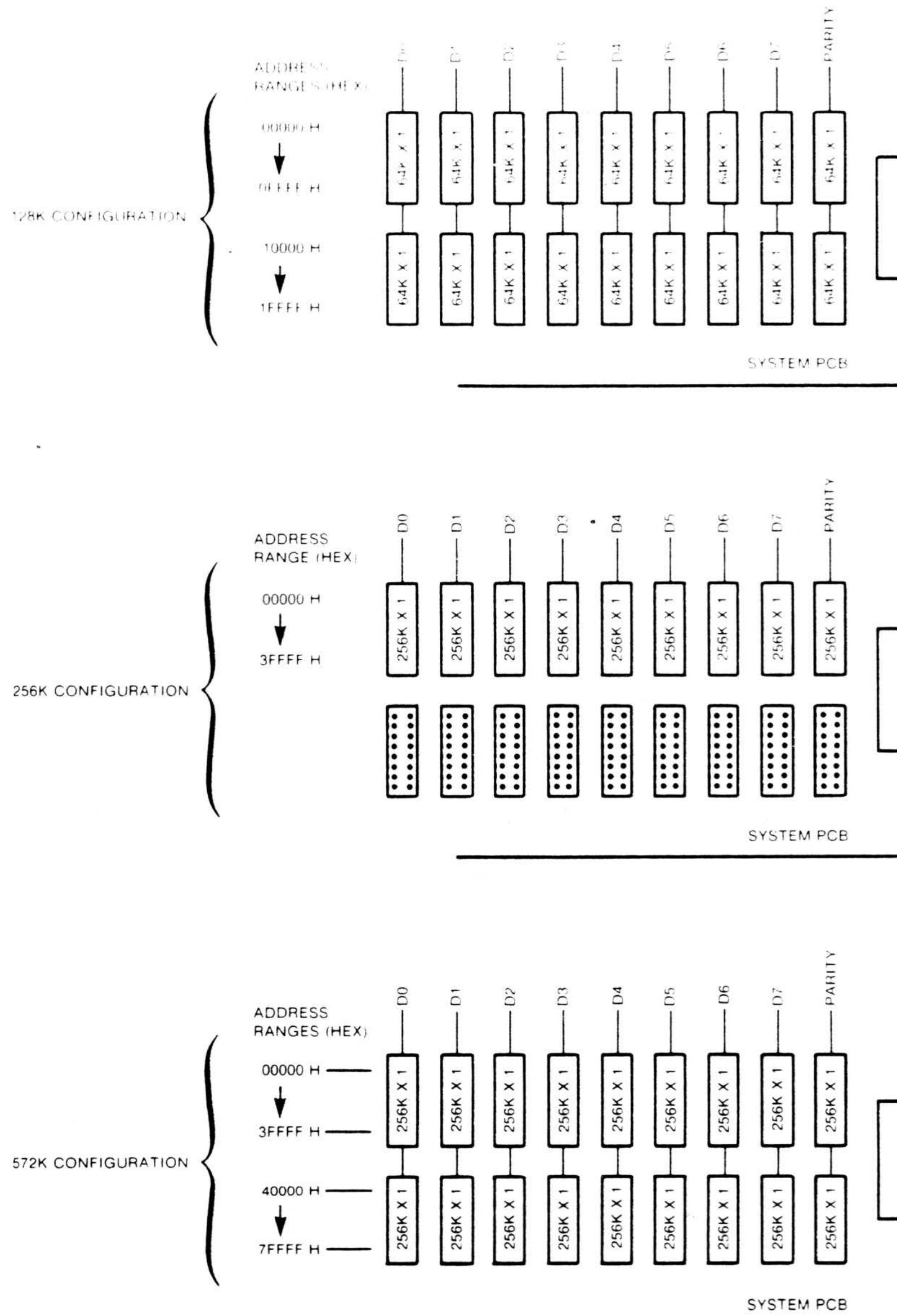


**Figure 5-3. Commuter System Memory Map**

## DRAM HARDWARE CONFIGURATIONS

DRAM must be refreshed on a periodic basis. Counter 1 of the 8253 system timer (U113) initiates this process by sending a DMA request (DREQ0) to the DMA controller approximately every 16 microseconds. The DMA controller then issues an HRQ (Hold Request) to the arbitration logic to gain bus control. Upon gaining control of the bus the DMA controller then performs a dummy read to the next sequential location in memory. The DACK0 signal issued as a result of HLDA (Hold Acknowledge) resets the refresh request flipflop.

The DRAM hardware comprises the majority of system memory. Three configurations are possible and are illustrated in Figure 5-4 .



**Figure 5-4. DRAM Hardware Configurations**

Each illustration provides the following information.

- the hardware layout on the system PCB
- the function associated with each device
- the size of each device
- the address range of each row

## BIOS ROM CONFIGURATIONS

Two ROMS (U103 and U104) are typically used to store the BIOS. Though 64k bytes of system memory are allocated to BIOS, only 16k bytes are used.

ROM may be configured in one of three ways. Each configuration requires certain jumper changes that are described in Table 5-7.

**Table 5-7. ROM Configurations and Jumper Requirements**

ROM	Jumpers *			
	W4	W5	W6	W7
64 K			IN	IN
128 K	IN		IN	
256 K	IN	IN		

\* Jumpers are OUT unless otherwise indicated.

### 5.3.8 Peripheral Interface Device

The 8255 programmable peripheral interface provides a variety of control and interfacing signals to other functional blocks within the Computer system.

The interface (U60) supports 24 control or interfacing lines. Each line is described in Table 5-8.

**Table 5-8. 8255 Interface Port Addresses and Functions**

I/O Address	Port Name	Port Type	Function
0060	PA0	Input	Keyboard scan code 0 or SW #1
0060	PA1	Input	Keyboard scan code 1 or SW #2
0060	PA2	Input	Keyboard scan code 2 or SW #3
0060	PA3	Input	Keyboard scan code 3 or SW #4
0060	PA4	Input	Keyboard scan code 4 or SW #5
0060	PA5	Input	Keyboard scan code 5 or SW #6
0060	PA6	Input	Keyboard scan code 6 or SW #7
0060	PA7	Input	Keyboard scan code 7 or SW #8

**Table 5-8. 8255 Interface Port Addresses and Functions (Cont.)**

I/O Address	Port Name	Port Type	Function
0061	PB0	Output	Enables (1) audio speaker
	PB1	Output	Audio speaker data
	PB2	Output	Not used
	PB3	Output	Not used
	PB4	Output	Enables (0) parity error
	PB5	Output	Enables (0) I/O channel error
	PB6	Output	Reset keyboard (0)
	PB7	Output	Read switches on port A and reset keyboard interrupt (1) OR enable keyboard scan code (0) on port A
0062	PC0	Output	Enable 16 line LCD display mode timing (0)
	PC1	Output	Enable high resolution monochrome display mode timing (0)
	PC2	Output	Reset video control logic (0)
	PC3	Output	Not used
	PC4	Input	Not used
	PC5	Input	Timer channel 2 output
	PC6	Input	I/O channel error (1)
0062	PC7	Input	Memory parity error (1)

#### NOTES

- (0) indicates active low, (1) indicates active high
- PC6 and PC7 are used to determine the source of NMI.
- PB0 and PB1 may be used to separately disable the speaker or modify its output.

#### 5.3.9 Keyboard Controller

The 6500/41 keyboard controller (U126) is used to interface the keyboard to the data bus via the 8255 peripheral interface (U60). The keyboard controller is initialized and tested at power-up.

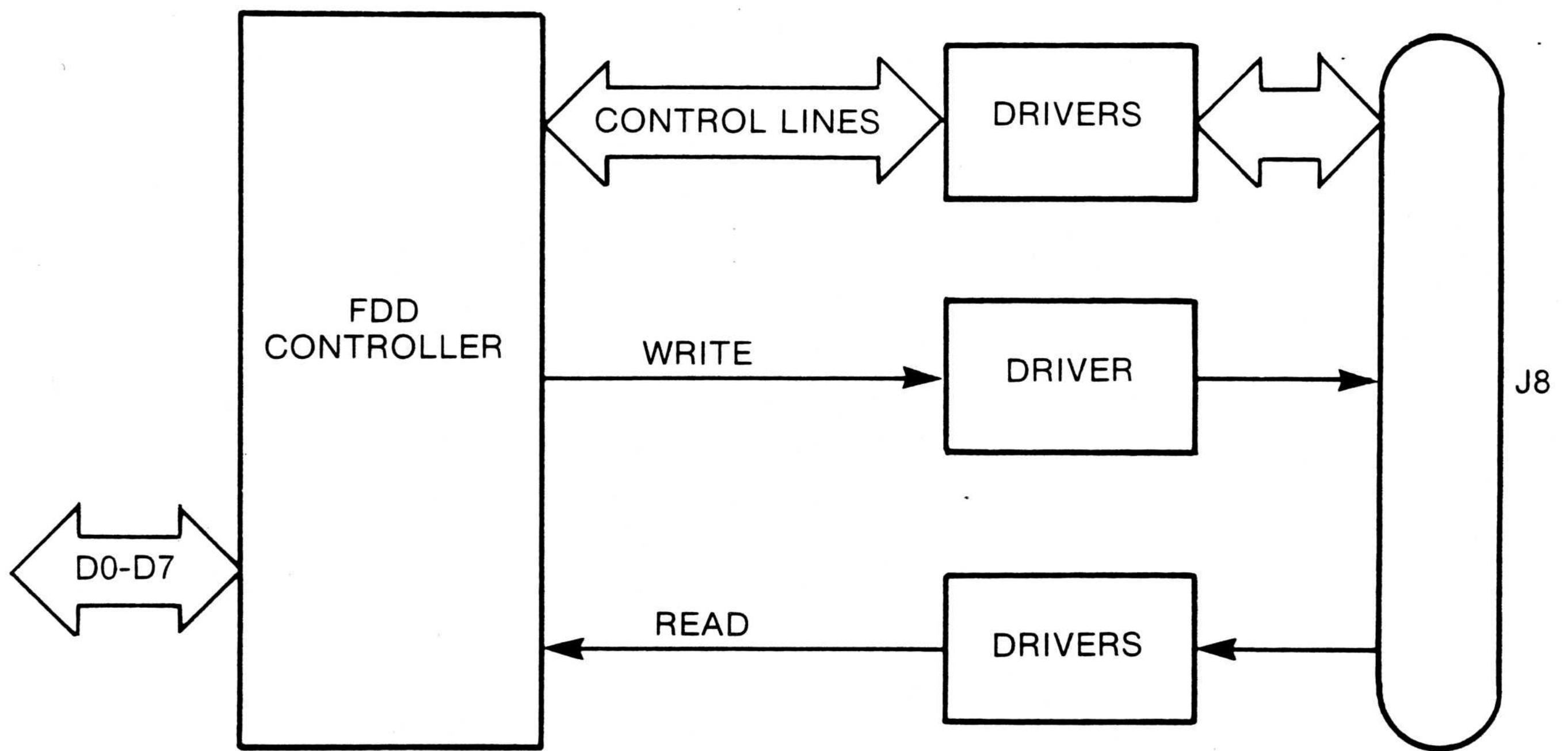
#### 5.3.10 Floppy Disk Controller and Support Logic

The 765 FDD (floppy disk drive) controller (U27) and support logic interfaces up to two FDD units that may be installed in a Commuter system. The 765 controller also provides the following functions.

- FDD unit selection
- Seek control
- Parallel to serial data conversion for writing to an FDD
- Serial to parallel data conversion for reading from an FDD
- Interrupt generation (IRQ6)
- DMA request/acknowledge (DREQ2/DACK2)

The floppy disk controller support logic is made up of the following elements:

- Open collector drivers drive data and control signals along the interface cable.
- Precompensation logic implemented via a 4046 compensator device (U165) allows for shifting of write data bits.
- Data separator logic separates clock and data from the incoming data stream using PLL.



**Figure 5-5. Floppy Disk Drive Interface Block Diagram**

Three I/O registers are used to program and control the 765 floppy disk controller. The I/O register addresses and their functions are described in Table 5-9.

**Table 5-9. Floppy Disk Controller Register Descriptions**

I/O Address	Read/Write *	Register Function												
03F2	W	<p>Digital output register with the following bit descriptions.</p> <p>Bit 0-1; Drive select. The hardware decodes these bits to select one drive if its motor is on.</p> <table> <thead> <tr> <th>Bit #</th> <th>Drive Selected</th> </tr> <tr> <th>1 0</th> <th></th> </tr> </thead> <tbody> <tr> <td>0 0</td> <td>0 (A)</td> </tr> <tr> <td>0 1</td> <td>1 (B)</td> </tr> <tr> <td>1 0</td> <td>2 (C)</td> </tr> <tr> <td>1 1</td> <td>3 (D)</td> </tr> </tbody> </table> <p>Bit 2; FDC reset.</p> <ul style="list-style-type: none"> <li>• When clear (bit 2=0) the FDC is held in reset.</li> <li>• When set by the program (Bit 2=1) the FDC is enabled.</li> </ul> <p>Bit 3; Enable INT and DMA requests.</p> <ul style="list-style-type: none"> <li>• When clear (bit 3=0) the FDC interrupt and DMA request functions are disabled.</li> <li>• When set (bit 3=1) the FDC interrupt and DMA request functions are enabled.</li> </ul> <p>Bit 4-7; Drive motor enable. Bit 4 controls drive 0, bit 5 controls drive 1 and so on. If a bit=0, the motor is off and the drive cannot be selected.</p>	Bit #	Drive Selected	1 0		0 0	0 (A)	0 1	1 (B)	1 0	2 (C)	1 1	3 (D)
Bit #	Drive Selected													
1 0														
0 0	0 (A)													
0 1	1 (B)													
1 0	2 (C)													
1 1	3 (D)													
03F4	R	Status register												
03F5	R/W	Data register												

\* R = read only; W = write only; R/W = read and write.

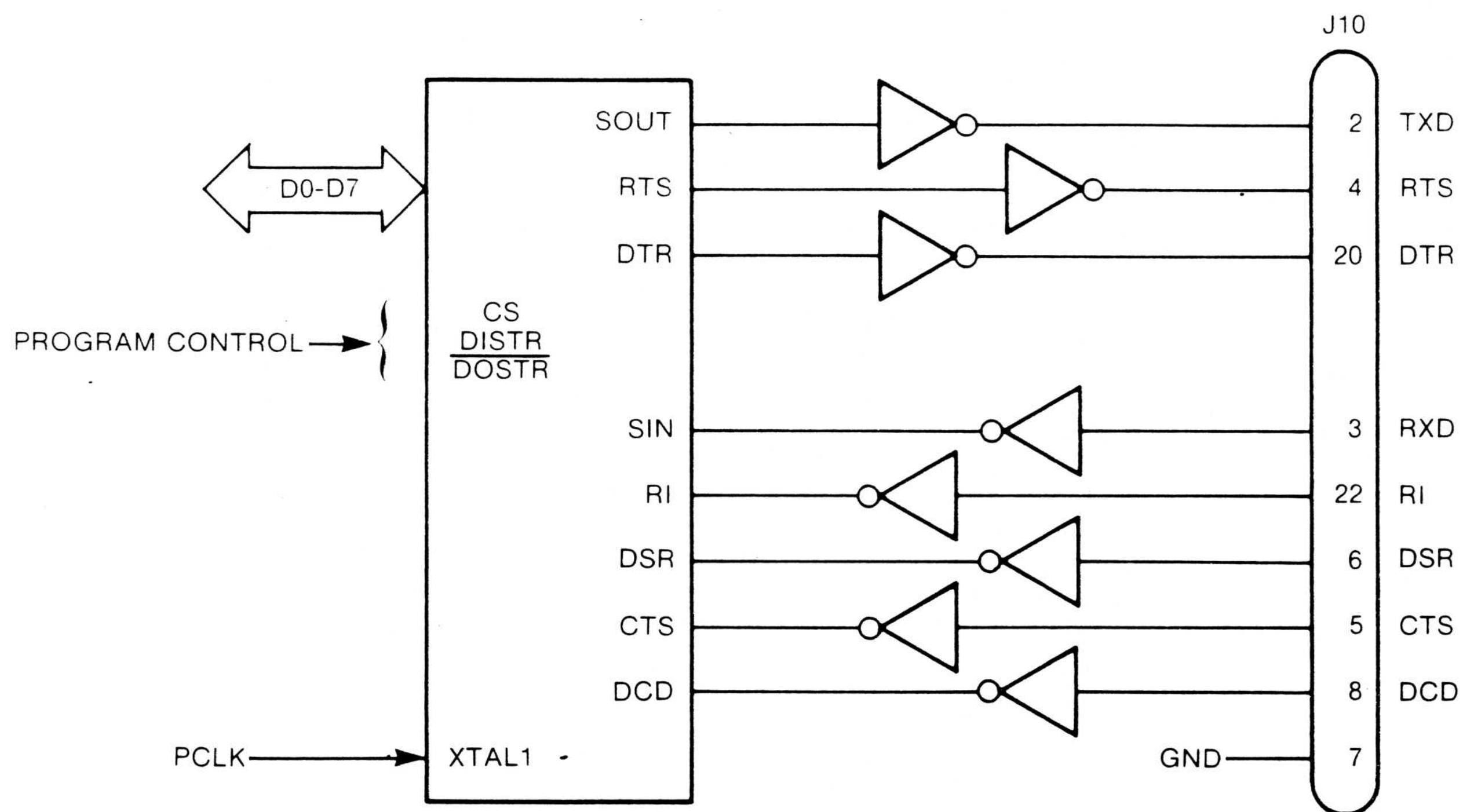
### 5.3.11 8250 Asynchronous Communication Interface

The 8250 asynchronous communication interface (U72) is fully programmable and supports the following capabilities.

- EIA RS-232-C standard for serial communication
- Asynchronous communication
- Baud rate generator allows operation from 50 to 9600 baud
- Adds and removes start bits, stop bits and parity bits
- Diagnostic functions provide an internal data loopback

The controller interfaces via drivers and receivers to J10 (a 25-pin, female, D connector) on the rear of the Commuter system. All pin designations follow standard EIA RS-232-C conventions.

Figure 5-6 shows a block diagram for the 8250 controller circuitry.



**Figure 5-6. 8250 Interface Block Diagram**

Seven I/O registers are used to program and control the 8250 controller. Note that the register with address 03F9 serves a dual function. The I/O register addresses and their functions are described in Table 5-10.

**Table 5-10. 8250 Communications Controller Register Descriptions**

I/O Address	Read/Write*	Register Function
03F8	R/W	Divisor latch lsb
03F9	R/W	Divisor latch msb
03F9	R/W	Interrupt enable
03FA	R	Interrupt ID
03FB	R/W	Line control
03FC	R/W	Modem control
03FD	R	Line status
03FE	R	Modem status

\*R = read only; W = write only; R/W = read and write.

### 5.3.12 8530 Synchronous/Asynchronous Communication Interface

The optional 8530 synchronous/asynchronous communication interface (U59) is fully programmable and supports the following capabilities.

- EIA RS-232-C standard for serial communication
- Asynchronous communication
- Synchronous (BSC, SDLC and HDLC) communication
- Baud rate generator allows operation from 50 to 9600 baud
- Adds and removes start bits, stop bits and parity bits
- Diagnostic functions provide an internal data loopback

The controller interfaces via EIA drivers and receivers to J11 (a 25 pin, female, D connector) on the rear of the Computer system. All pin designations follow standard EIA RS-232-C.

Figure 5-7 shows a block diagram for the 8530 controller circuitry.

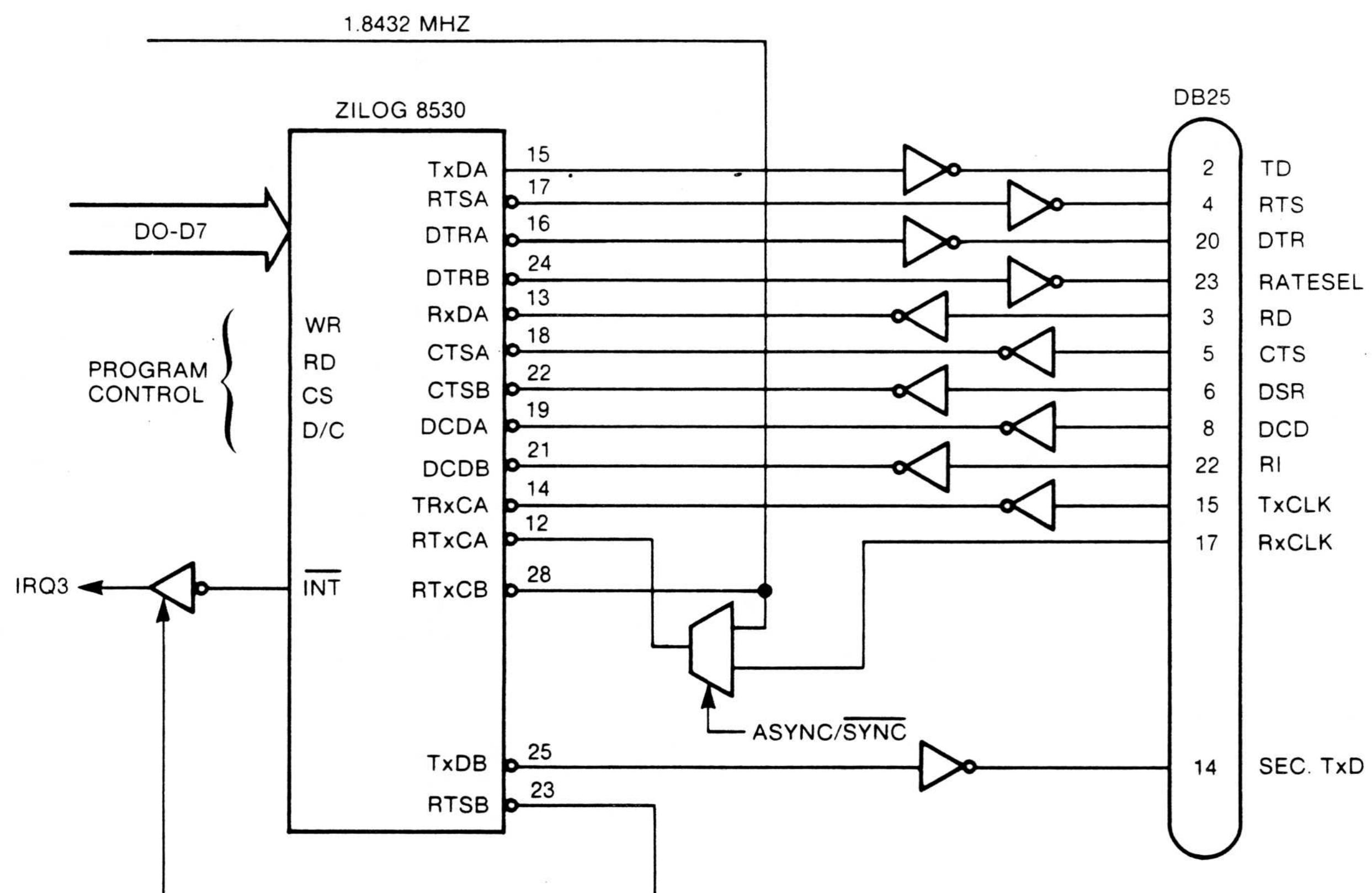


Figure 5-7. 8530 Interface Block Diagram

Four I/O registers are used to program and control the 8530 controller. The I/O register addresses and their functions are described in Table 5-11.

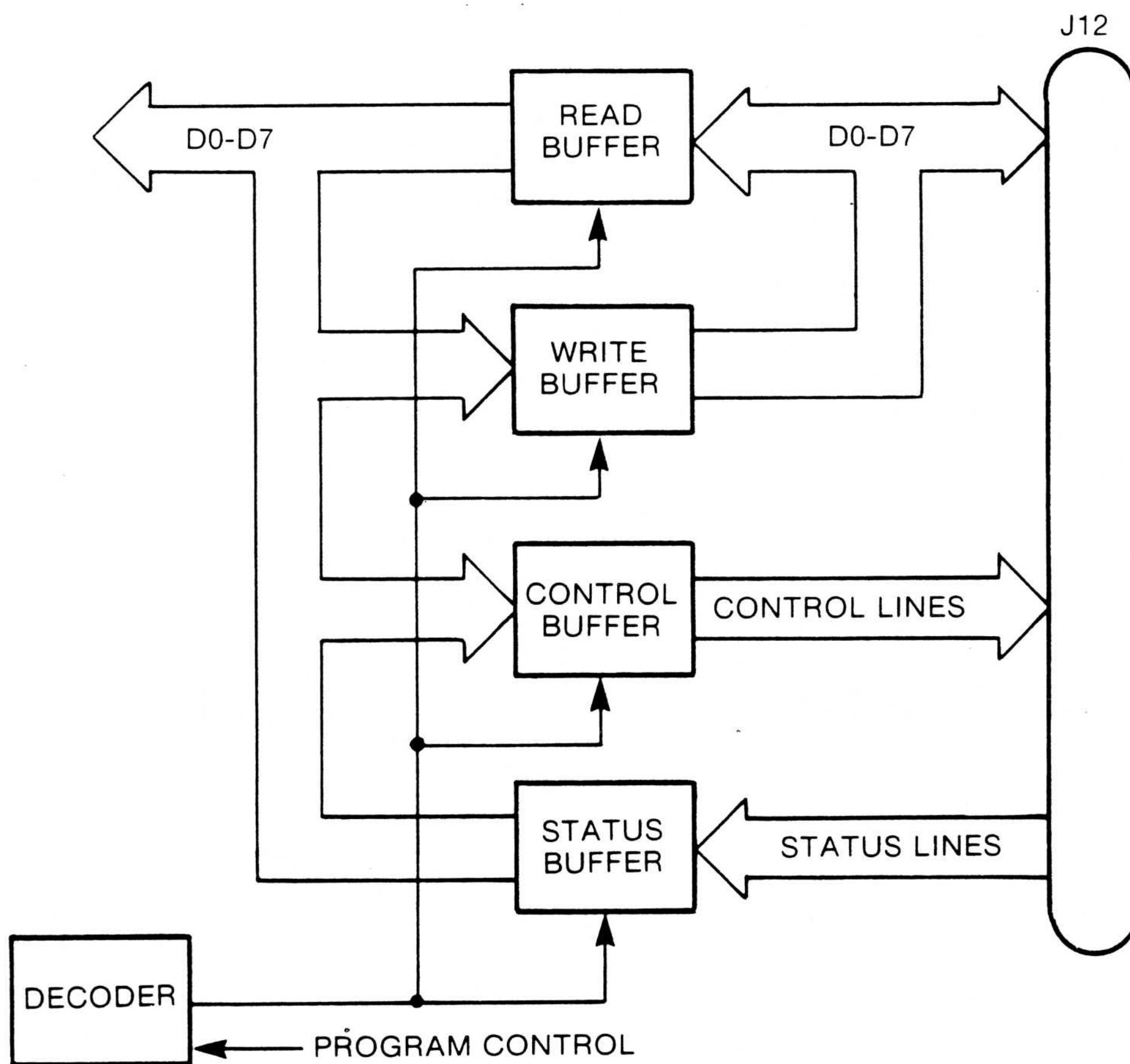
**Table 5-11. 8530 Communications Controller Register Descriptions**

I/O Address	Read/ Write*	Register Function
0380	W	Channel B control register
0381	R/W	Channel B data register
0388	W	Channel A control register
0389	R/W	Channel A data register

\*R = read only; W = write only; R/W = read and write.

### 5.3.13 Printer Interface

The printer interface supports a single parallel printer that may be connected to J12 on the rear panel of the Computer system. The functional blocks that make up the printer interface are shown in Figure 5-8.



**Figure 5-8. Printer Interface Block Diagram**

Four I/O registers are used to control and drive the printer interface. These registers are described in Table 5-12. The bit names for the control and status registers are described after the table.

**Table 5-12. Printer Interface Register Descriptions**

I/O Address	Read/ Write*	Register Function
0378	W	Data to printer
0378	R	Data echo
0379	W	Control register that has the following bit names.  Bit 0 - STROBE (Strobe) Bit 1 - AUTOFDXT (Autofeed) Bit 2 - INTI (Initialize printer) Bit 3 - SLCTIN (Select printer)
037A	R	Status register that has the following bit names.  Bit 0 - BUSY Bit 1 - ACK Bit 2 - PE Bit 3 - SLCT

\*R = read only; W = write only; R/W = read and write.

### CONTROL REGISTER BIT DEFINITIONS

The control register bits have the following definitions:

**STROBE (Strobe)** — When this bit is cleared (set to 0) data can be read into the parallel printer.

**AUTOFDXT (Autofeed)** — When this bit is cleared (set to 0) one linefeed is automatically performed after printing.

**INTI (Initialize printer)** — This bit is cleared (set to 0) to reset the printer controller to its initial state and to clear the printer buffer.

**SLCTIN (Select printer)** — This bit is cleared (set to 0) to select the printer.

### STATUS REGISTER BIT DEFINITIONS

The status register bits have the following definitions:

**BUSY** — This bit is set to 1 to indicate that the printer cannot receive data. This bit is set to 1 under the following conditions:

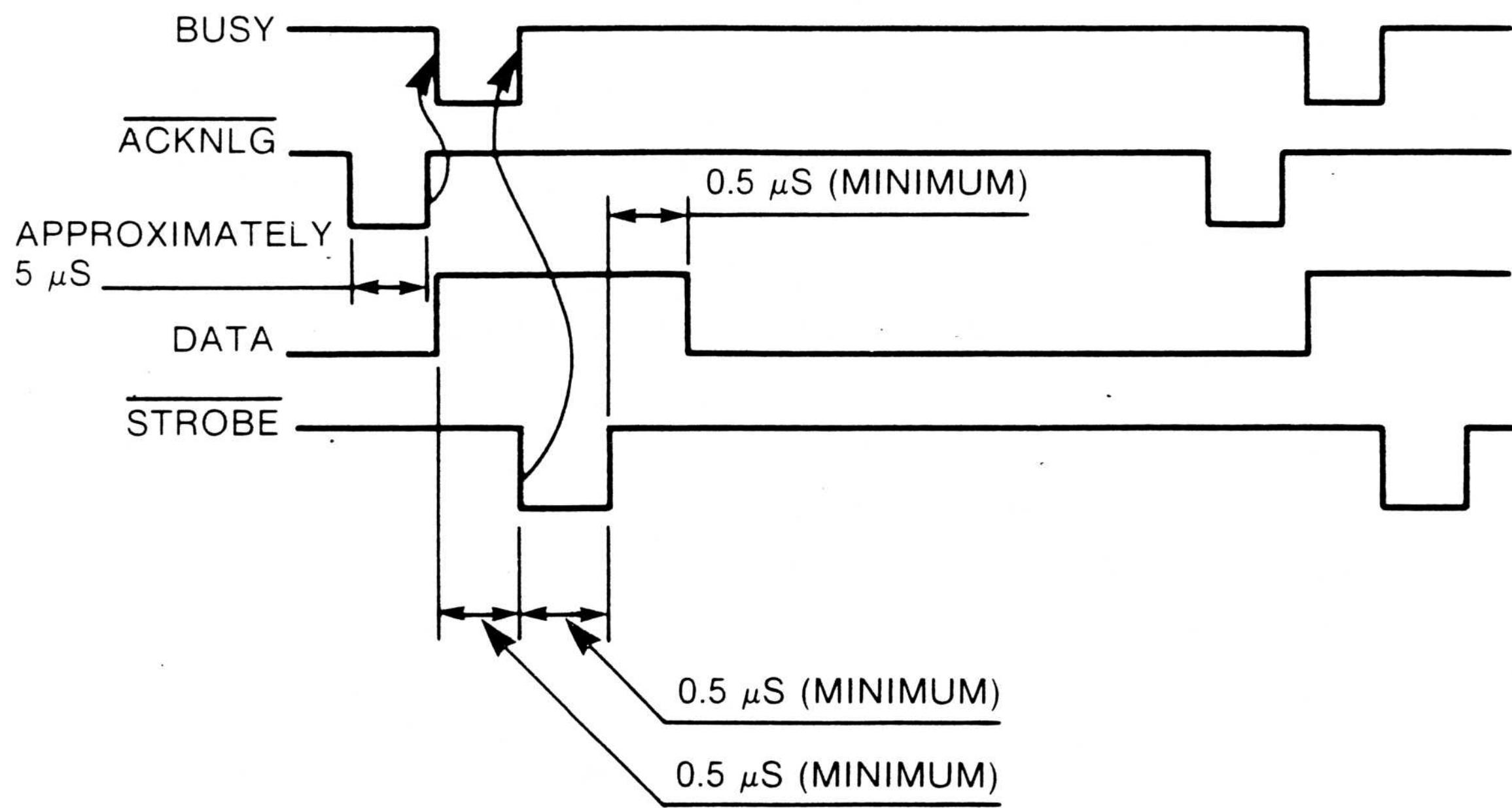
- While data is being entered.
- When the printer is in an “offline” state.
- While the printer is printing.
- During printer error status.

**ACK** — When this bit is set to 0 it indicates that the printer has received data and is ready to accept other data.

**PE** — When this bit is set to 1, it indicates that the printer is out of paper.

**SLCT** — When this bit is set to 1 it indicates that the printer is in the selected state.

Figure 5-9 illustrates the timing requirements for the parallel printer interface.



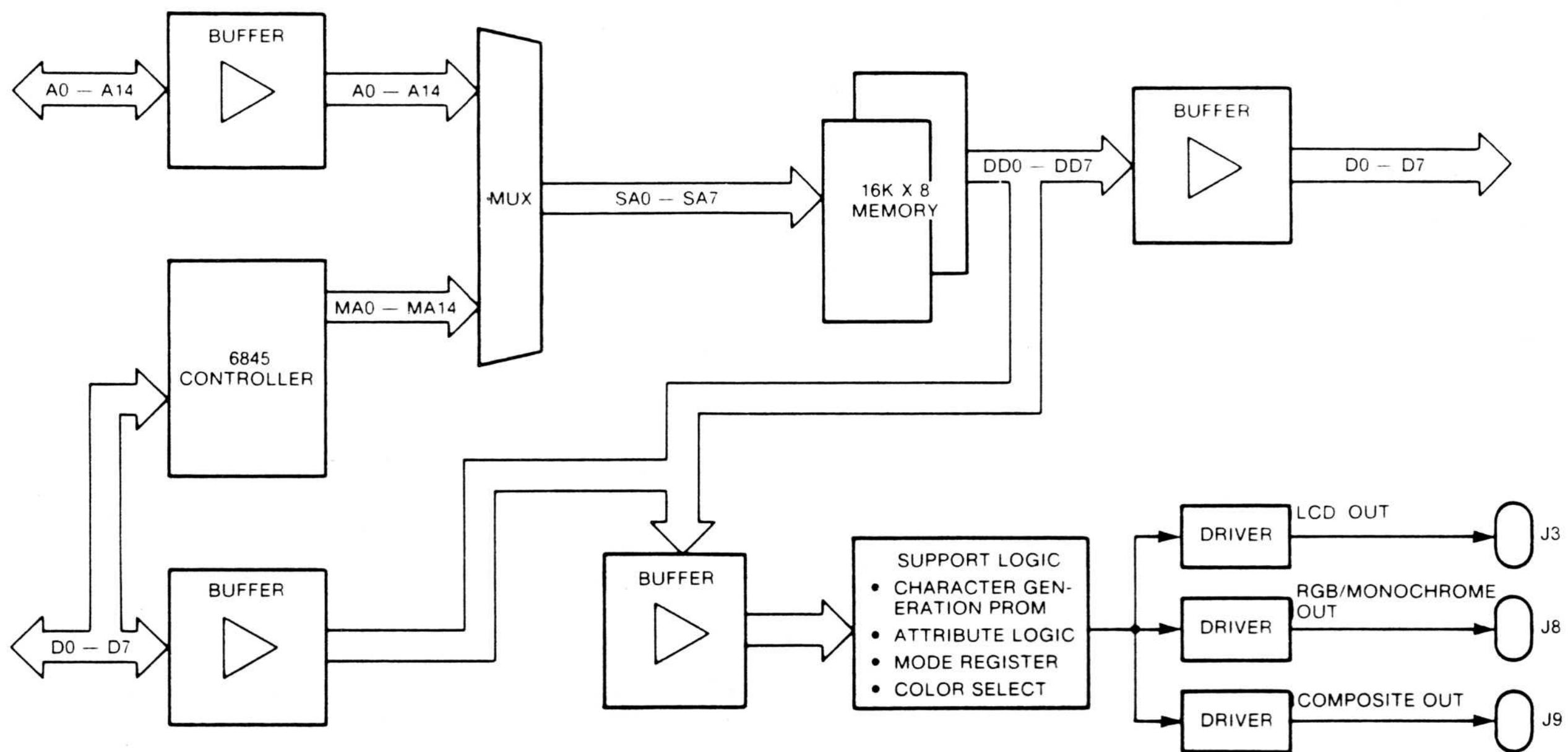
**Figure 5-9. Parallel Printer Interface Timing Diagram**

### 5.3.14 Video Controller and Support Logic

The video interface is made up of the following functional blocks.

- 6845 CRT controller
- 16k × 8 bits video memory (RAM)
- Video support logic

The block diagram in Figure 5-10 illustrates the relationships between the functional blocks.



**Figure 5-10. Video Interface Block Diagram**

### 6845 CRT CONTROLLER (U95)

The CRT controller provides control for a wide variety of raster scanned monitors. Four I/O registers are used to monitor and drive the controller. These registers and their functions are described in Table 5-13.

The address register (I/O address 03D0) is used as a pointer to select any one of 18 internal registers. A data register (I/O address 03D1) is used as a buffer for writing data to or reading data from the selected internal register. Table 5-14 identifies the functions of the internal registers.

**Table 5-13. CRT Controller I/O Register Descriptions**

I/O Address	Read/ Write*	Register Function
03D0	W	Internal register address
03D1	R/W	Internal data register
03D8	W	Mode select register with the following bit descriptions.  Bit 0 - select $80 \times 25$ mode Bit 1 - Select graphic mode Bit 2 - Select B & W mode Bit 3 - Enable video signal Bit 4 - Select $640 \times 200$ B & W mode Bit 5 - Enable blink attribute
03D9	R	Color select register with the following bit descriptions.  Bit 0 - B (blue) border color select Bit 1 - G (green) border color select Bit 2 - R (red) border color select Bit 3 - I (intensify) border color Bit 4 - Select alt bkgnd color for alpha Bit 5 - $320 \times 200$ color set select
03DA	R	Controller status register with the following bit descriptions.  Bit 0 - Display enable Bit 3 - Delayed vertical sync

\*R = read only; W = write only; R/W = read and write.

**Table 5-14. 6845 Controller Internal Register Descriptions**

Register Address	Register Number	Register Function
0	R0	Horizontal total
1	R1	Horizontal displayed
2	R2	Horizontal sync position
3	R3	Horizontal sync width
4	R4	Vertical total
5	R5	Vertical total adjust
6	R6	Vertical displayed
7	R7	Vertical sync position
8	R8	Interlace mode
9	R9	Maximum scan line address
10	R10	Cursor start
11	R11	Cursor end
12	R12	Start address (high)
13	R13	Start address (low)
14	R14	Cursor address (high)
15	R15	Cursor address (low)
16	R16	Not used
17	R17	Not used

## VIDEO MEMORY

The video memory (RAM) comprises 16k bytes of RAM that is used as the display buffer. The memory is configured from two 16k × 4 RAM ICs (U145 and U144). U145 contains the low order bits (D0 - D3) and U144 contains the high order bits (D4 - D7).

## VIDEO SUPPORT LOGIC

The video support logic is driven by the 6845 CRT controller and provides the following functions:

- Video synchronization
- Graphics data generation
- Alphanumeric character generation
- Composite video data generation

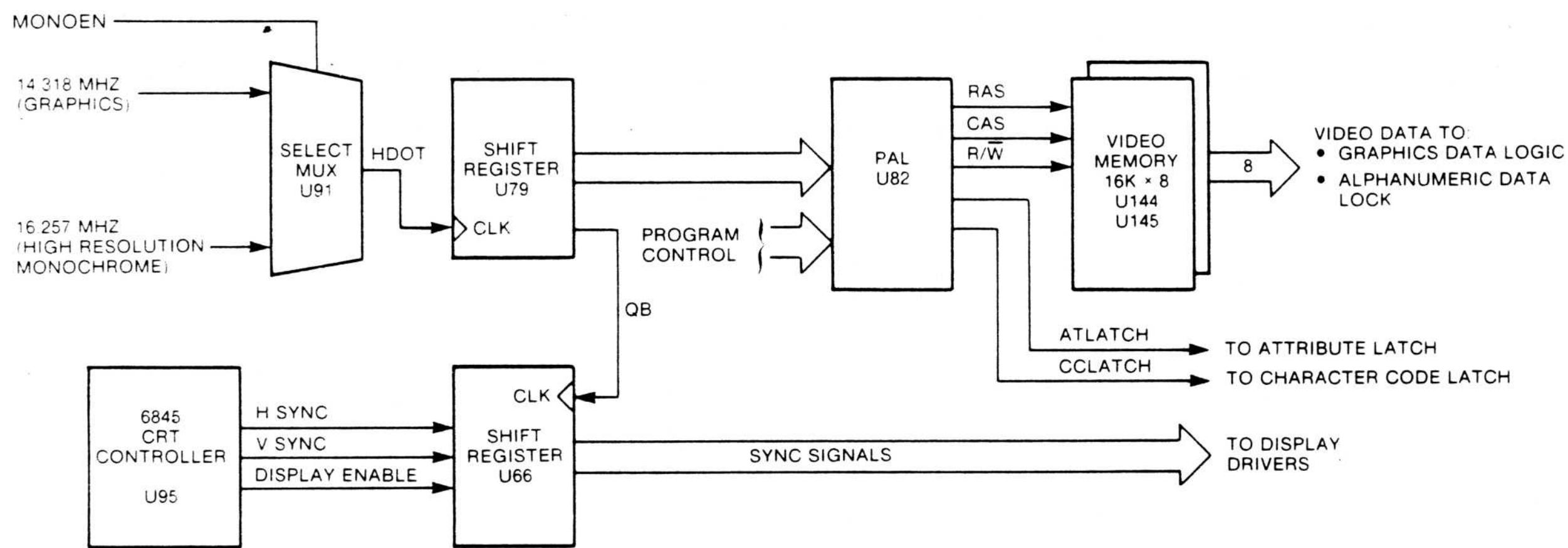
## Video Synchronization

This section describes the video synchronization logic that is illustrated in the block diagram in Figure 5-11. This diagram shows the functional design used in the video synchronization logic.

HDOT is produced in either of two frequencies and is used to synchronize the video memory and the horizontal and vertical sync signals. 14.318 MHz is used to time graphics applications, and 16.257 MHz is used to time high resolution monochrome applications.

HDOT clocks a shift register (U79). Outputs of U79 control two major functions.

1. Provide control signals that are used by PAL (U82) to:
  - a. Scan the video memory.
  - b. Clock video memory data through the character code and attribute latches.
2. Clock horizontal and vertical sync signals through flip-flop (U66). The resulting synchronized sync signals are then routed to the output drivers.



**Figure 5-11. Video Synchronization Logic Block Diagram**

## **Graphics Data Generation**

When the Commuter system is in **graphics mode**, the data is mapped onto a monitor screen that is defined as 640 pixels wide by 200 pixels long. In the graphics mode each bit in video memory (128,000 bits) has a corresponding pixel on the screen.

Data from the video memory is used as an input to parallel to serial shift registers U106 and U121 (refer to Figure 5-12). The shift registers (U106 and U121) separate video data into even and odd numbered bits called C0 DOTS and C1 DOTS.\*

C0 DOTS, C1 DOTS, and program control lines are provided to a PAL (U58). The outputs of the PAL drive multiplexers U56 and U69 to inject remaining attributes such as color and intensity. The completed data is then provided to the port drivers along with horizontal and vertical synchronization signals.

## **Alphanumeric Character Generation**

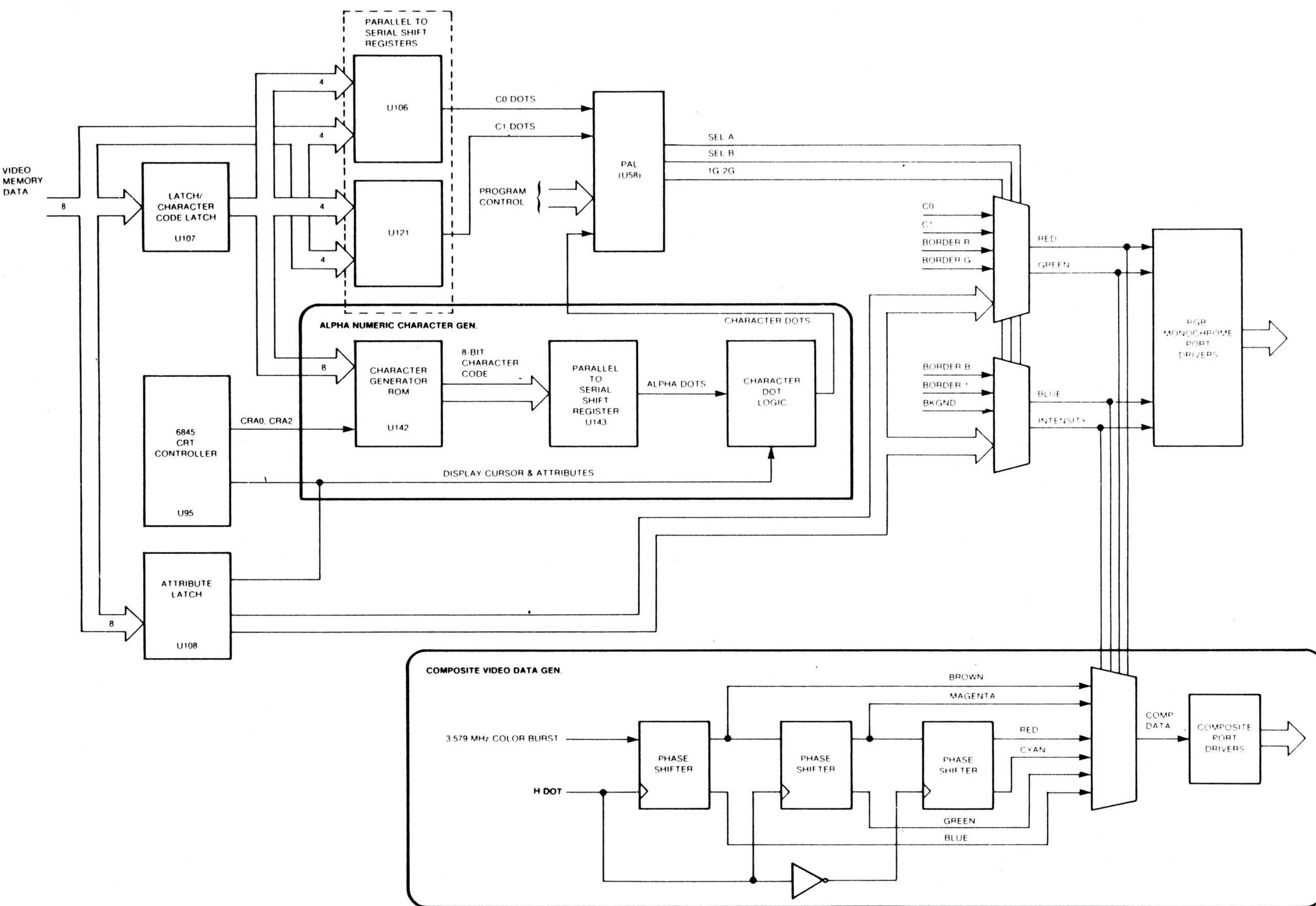
When the Commuter system is in **alphanumeric mode**, data from the video memory is latched (refer to Figure 5-12) in an eight-bit Character Code Latch (U107) and then used as an input to the character generator ROM (U142). The ROM generates predefined alphanumeric characters that correspond to the character code received.

The dots that make up the characters are used as a serial input to character dot logic. Blinking, underlining and cursor blinking is established at this stage. The output, called ALPHA DOTS, is used as an input to PAL (U58) along with other program control lines.

The outputs of the PAL drive multiplexers U56 and U69 to inject remaining attributes such as color and intensity. The completed data is then provided to the port drivers along with horizontal and vertical synchronization signals.

---

\*Signal separation provides control for medium resolution (320 by 200) graphics and high resolution (640 by 200) graphics. In medium resolution, C0 dots and C1 dots define single pixels. When both dots are off (0), the background color is displayed. The remaining three combinations determine the color of a foreground pixel. In high resolution, C0 and C1 dots define alternating pixels. The foreground may be colored. The background is always black.



**Figure 5-12. Colorgraphics, Alphanumeric, and Composite Video Logic**

## **Composite Video Data Generation**

Composite video data is derived from graphic or alphanumeric data at the stage just before it is sent to the port drivers.

The method for generating composite video data uses phase shifters that are shown in the block diagram (Figure 5-12). A color burst frequency (3.579 MHz) is phase shifted to provide six separate phases that are used to produce specific colors. The six phases are provided as inputs to multiplexer U20. U20 is an eight-line to one-line multiplexer that is steered by the RED, GREEN, and BLUE outputs of multiplexers U56 and U69.

The composite data is then sent to the composite port drivers.

### **5.3.15 Expansion Port Interface**

The expansion port (J7) is designed to interface to the IBM expansion chassis. The expansion chassis contains its own power supply and a backplane that accepts a variety of IBM expansion cards such as a hard disk controller or graphics adaptor.

The expansion port is supported by the following address, data and control lines.

- A0 - A19.
- D0 - D7.
- Three interrupt request lines.
- Three DMA request and acknowledge lines.
- One I/O channel error line (EIOCHCK).
- Miscellaneous signal and control lines.

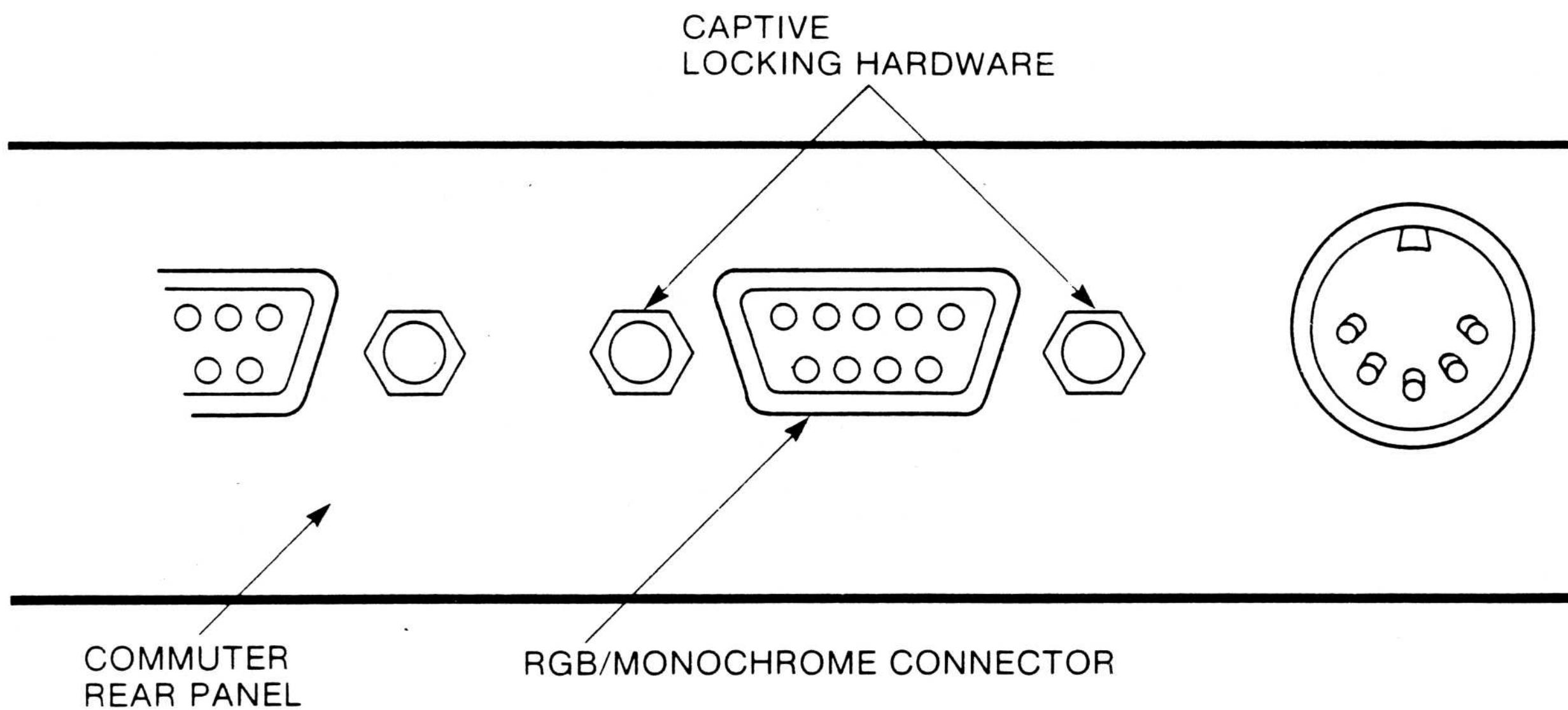
## APPENDIX A RGB/MONOCHROME MONITOR INTERFACING REQUIREMENTS

### A.1 INTRODUCTION

This Appendix provides information required to interface RGB and monochrome monitors to the Computer system. The mechanical and electrical characteristics of the RGB/Monochrome connector are described.

#### A.1.1 Mechanical Characteristics

The RGB/Monochrome connector (see Figure A-1) is a nine-pin, female, "D" type connector. Captive hardware allows a mating connector to be held in place with locking screws.



**Figure A-1. RGB/Monochrome Connector**

#### A.1.2 Electrical Characteristics

Table A-1 lists each pin and signal name for the RGB/Monochrome connector. An asterisk (\*) then identifies those signals that are typically used to drive RGB and/or monochrome monitors.

**Table A-1. RGB/Monochrome Signal Usage**

Pin Number	Signal Name	Typically used for:	
		RGB	Monochrome
1	Ground	*	*
2	Ground	*	*
3	Red	*	
4	Green	*	
5	Blue	*	
6	Intensity		*
7	Black/White Video		*
8	Horizontal Drive	*	*
9	Vertical Drive	*	*

## APPENDIX B PIN ASSIGNMENTS

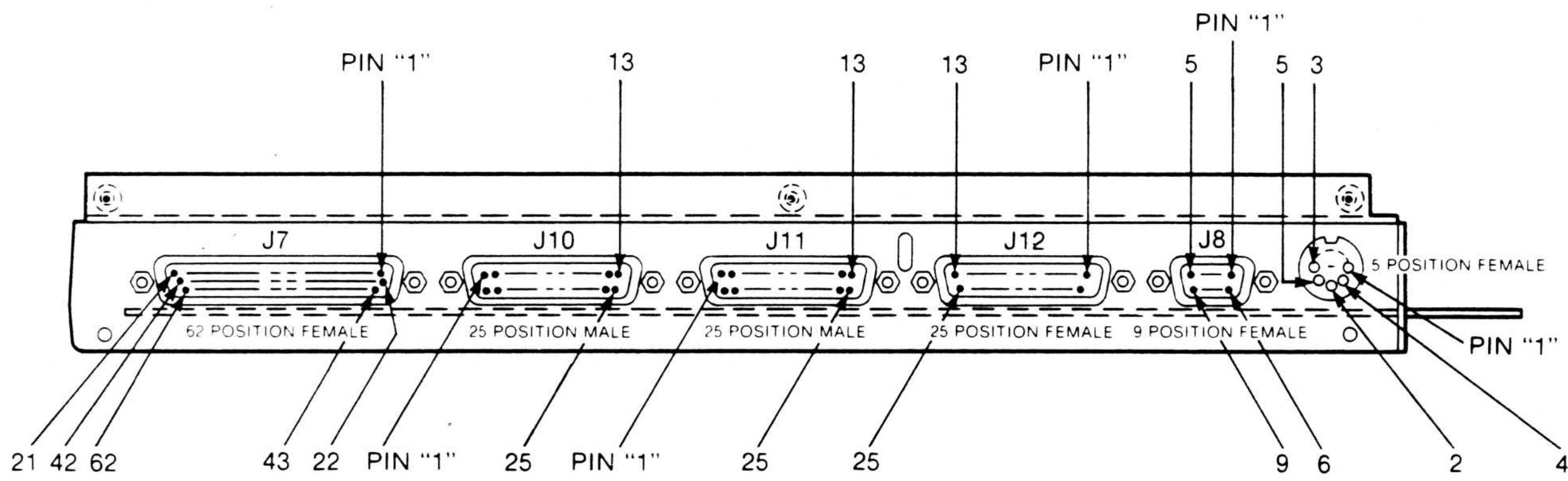
### B.1 INTRODUCTION

This Appendix provides pin assignment information that may be used for interfacing the Commuter system to various peripheral devices.

Figure B-1 illustrates the mechanical aspects of each port on the rear of the Commuter system. Corresponding tables show the pin assignments for each port.

The following port pin assignments are provided.

- Composite video
- RGB/monochrome
- Parallel port
- Async/Sync port
- Async port
- Expansion port



**Figure B-1. Rear Panel Connector and Pin Locations**

### B.2 COMPOSITE VIDEO CONNECTOR (J9)

The composite video connector is a five-pin female, DIN type connector. Table B-1 shows the pin assignments for each pin.

**Table B-1. Composite Video Connector Pin Assignment**

Pin Number	Pin Assignment
1	+12V
2	Chassis ground
3	No connection
4	Composite video output
5	Signal ground

### **B.3 RGB/MONOCHROME CONNECTOR (J8)**

The RGB/monochrome connector is a nine-pin, female, "D" type connector. Table B-2 shows the pin assignments for each pin.

**Table B-2. RGB/Monochrome Connector Pin Assignment**

Pin Number	Pin Assignment
1	Ground
2	Ground
3	Red
4	Green
5	Blue
6	Intensity
7	Black/White Video
8	Horizontal Drive
9	Vertical Drive

### **B.4 PARALLEL PORT (J12)**

The parallel port connector is a 25-pin, female, "D" type connector. Table B-3 shows the pin assignments for each pin.

**Table B-3. Parallel Port Connector Pin Assignment**

Pin Number	Pin Assignment*	Pin Number	Pin Assignment*
1	STROBE	10	ACK
2	DATA 0	11	BUSY
3	DATA 1	12	PE
4	DATA 2	13	SLCT
5	DATA 3	14	AUTOFDXT
6	DATA 4	15	ERROR
7	DATA 5	16	INTI
8	DATA 6	17	SLCTIN
9	DATA 7	18 – 25	GROUND

#### **B.5 ASYNC/SYNC PORT (J11)**

The asynchronous/synchronous port connector is a 25-pin, male, "D" type connector. Table B-4 shows the pin assignments for each pin.

**Table B-4. Asynchronous/Synchronous Port Connector Pin Assignment**

Pin Number	Pin Assignment*	Pin Number	Pin Assignment*
1	No connection	14	SEC TxD
2	TxD	15	TxCLK
3	RxD	16	SEC RxD
4	RTS	17	RxCLK
5	CTS	18 – 19	No connection
6	DSR	20	DTR
7	Ground	21	No connection
8	DCD	22	RI
9 – 13	No connection	23	RATE SEL
		24 – 25	No connection

#### **B.6 ASYNC PORT (J10)**

The asynchronous port connector is a 25-pin, male, "D" type connector. Table B-5 shows the pin assignments for each pin.

---

\*A line over a signal name such as STROBE indicates an active low signal.

**Table B-5. Asynchronous Port Connector Pin Assignment**

Pin Number	Pin Assignment*
2	<u>TxD</u>
3	<u>RxD</u>
4	RTS
5	CTS
6	DSR
7	Ground
8	DCD
9 – 19	No connection
20	DTR
22	RI
23 – 25	No connection

### B.7 EXPANSION PORT (J7)

The expansion port connector is a 62-pin, female, "D" type connector. Table B-6 shows the pin assignments for each pin.

**Table B-6. Expansion Port Connector Pin Assignment**

Pin Number	Pin Assignment*
1 – 2	No connection
3	<u>EDIR</u>
4	EENB
5	<u>E88CLK</u>
6	EEXMEM
7	EA17
8	EA16
9	EA5
10	EDACK0
11	EA15
12	EA11
13	EA10
14	EA9
15	EA1
16	EA3
17	EDACK1
18	EA4
19	No connection

---

\*A line over a signal name such as **STROBE** indicates an active low signal.

**Table B-6. Expansion Port Connector Pin Assignment (Cont)**

Pin Number	Pin Assignment*
20	EIOWC
21	EA13
22	ED5
23	EDREQ1
24	EDREQ3
25	No connection
26	EALE
27	EEOP
28	EREST
29	EAN
30	EA19
31	EA14
32	EA12
33	EA18
34	EMRD
35	EMWC
36	EA0
37	EDACK3
38	EA6
39	EIORD
40	EA8
41	EA2
42	EA7
43	EIRQ7
44	ED6
45	EWAIT
46	EIRQ3
47	ED7
48	ED1
49	EIOCHCK

---

\*A line over a signal name such as **STROBE** indicates an active low signal.

**Table B-6. Expansion Port Connector Pin Assignment (Cont)**

Pin Number	Pin Assignment*
50	EIRQ2
51	ED0
52	ED2
53	ED4
54	EIRQ5
55	No connection
56	ED3
57	Ground
58	Ground
59	Ground
60	Ground
61	Ground
62	<u>ENB</u>

---

\*A line over a signal name such as **STROBE** indicates an active low signal.

## APPENDIX C MNEMONIC TRANSLATIONS

This Appendix may be used to locate the sources of many of the signals contained in the schematic diagrams in Appendix D. Table C-1 lists mnemonics in alphanumeric order. The signal source is identified by the schematic sheet and IC number. A definition of the listed mnemonics is contained in the last column.

**Table C-1. Mnemonic Listing**

Mnemonic*	Sheet	IC #	Definition
1G/2G	8	U58	Enable Channel 1 Gate or Channel 2 Gate
80/25 ALPHA	8	U39	80 by 25 Alphanumeric Mode
3.579 MHZ	7	U61	3.579 MHz
4MHZ	5	U28	4 MHz
8530 ASYNC/SYNC	2	U72	8530 Async/Sync
88CLK	1	U30	8088 Clock (4.77 MHz)
88ENB	1	U100	8288 Chip Enable
A0-A19	1	Several	Address Bus (Bits 0-19)
AA5-AA12	6	Several	Adder Address (Bits 5-12)
<u>ACIACS</u>	4	U150	Async Controller Chip Select
ADJC/GVSYNC	7	U67	Adjusted Color/Graphics Vert. Sync
ADJC/GHSYNC	7	U68	Adjusted Color/Graphics Horiz. Sync
ALE	1	8288	Address Latch Enable
ALPHA DOTS	6	U143	Alpha Dots
AT0-AT7	6	U108	Attribute (Bits 0-7)
ATLATCH	6	U82	Attribute Latch Enable
BACKGRND I	8	U38	Background Intensity
<u>BDATAEN</u>	4	U149	Buffered Data Enable
BD0-BD7	4	Several	Buffered Data (Bits 0-7)
<u>BI/BLINK</u>	8	U39	Background Intensity or Blink
BLUE	7	U56	Blue
BLUE SELECT	8	U163	Blue Select
BOFF	8	U118	Bottom Offset (for LCD Screen Refresh)
BORDER B	8	U38	Border Blue
BORDER G	8	U38	Border Green
BORDER I	8	U38	Border Intensity
BORDER R	8	U38	Border Red
B/W SEL	8	U39	Black and White Select

\*A line over a signal name such as **ACIACS** indicates an active low signal.

**Table C-1. Mnemonic Listing (Contd.)**

Mnemonic*	Sheet	IC #	Definition
C0	8	U106	C0 Dots
C1	8	U121	C1 Dots
<u>CADD</u>	6	U82	Column Address Data
<u>CASEL</u>	3	U132	Column Address Select
<u>CASEN</u>	3	U115	Column Address Enable
CC0-CU7	6	U107	Character Code (Bits 0-7)
<u>CCLATCH</u>	6	U82	Character Code Latch Enable
C/GHSYNC	7	U66	Color/Graphics Horizontal Sync
CHAR BLINK	7	U18	Character Blink
CHAR DOTS	8	U35	Character Dots
<u>CHCLK</u>	8	U55	Character Clock
<u>CLOCK HOLD</u>	2	U60	Clock Hold
<u>CLR/EN</u>	2	U60	Clear/Enable
<u>CLRSHIFT</u>	7	U80	Clear/Shift
<u>COLOR SEL</u>	8	U38	Color Select
<u>COMP DATA</u>	7	U20	Composite Data
<u>CPUCOL</u>	6	U92	CPU Column
CPU/CRT	7	U71	CPU Timing or CRT Timing
<u>CPUCYCLE</u>	8	U83	CPU Cycle
CPU ROW	6	U92	CPU Row
<u>CRA0-CRA3</u>	6	U95	Character Row Address (Bits 0-3)
<u>CRT COL</u>	6	U92	CRT Column
<u>CRTCOLOR</u>	4	U130	CRT Color
<u>CRTCS</u>	4	U150	CRT Controller Chip Select
<u>CRT/PRT SEL</u>	4	U149	Select CRT or Printer
<u>CRTMODE</u>	4	U130	CRT Mode
<u>CRT ROW</u>	6	U92	CRT Row
<u>CRTSEL</u>	4	U149	Crt Select
<u>CRTSTAT</u>	4	U130	CRT Status
CURSOR	6	U95	Cursor
CURSOR BLINK	7	U18	Cursor Blink
<u>DACK0-DACK3</u>	1	U64	DMA Acknowledge (Lines 0-3)
<u>DCAS</u>	6	U82	Dot Column Address Strobe
<u>DD0-DD7</u>	6	Several	Display Data (Bits 0-7)
<u>DISEN</u>	6	U95	Display Enable
<u>DLYCPUCYCLE</u>	6	U111	Delayed CPU Cycle
<u>DLYCURSOR</u>	7	U66	Delayed Cursor
<u>DLYDISEN</u>	7	U66	Delayed Display Enable
<u>DLYVSYNC</u>	7	U66	Delayed Vertical Sync
<u>DMACLK</u>	1	U84	DMA Clock
<u>DMACS</u>	4	U150	DMA Controller Chip Select

\*A line over a signal name such as ACIACS indicates an active low signal.

**Table C-1. Mnemonic Listing (Contd.)**

Mnemonic*	Sheet	IC #	Definition
DMAPG	4	U149	DMA Page Register Enable
DMARDY	1	U74	DMA Ready
DOTCLK	8	U55	Dot Clock
DOT DATA LATCH	6	U82	Dot Data Latch
DRAS	6	U82	Dot Row Address Strobe
DREQ0	4	U114	DMA Request 0
DREQ1	9	U31	DMA Request Level 1
DREQ2	5	U14	DMA Request Level 2
DREQ3	9	R25	DMA Request Level 3
DRR/W	6	U82	Display RAM Read/Write
EN PAR ERR	2	U60	Enable Parity Error
EXMEM	3	U115	External Memory
FDCCS	4	U150	Floppy Disk Controller Chip Select
FDMOT	4	U149	Floppy Drive Motor Enable
GRAPHIC SEL	8	U39	Graphic Mode Select
GREEN	7	U69	Green
HDOT	7	U91	High Frequency Dot Clock
HSYNC	6	U95	Horizontal Synchronization
INT	7	U56	Intensity
INTCS	4	U150	Interrupt Controller Chip Select
IOCHERR	2	U41	I/O Channel Error
IOCHK	9	U31	I/O Channel Check
IORD	1	U63	I/O Read
IOWC	1	U63	I/O Write Command
IRQ0	4	U113	Interrupt Request Level 0
IRQ1	2	U127	Interrupt Request Level 1
IRQ2	9	R31	Interrupt Request Level 2
IRQ3	10	U42	Interrupt Request Level 3
IRQ3	9	U31	Interrupt Request Level 3
IRQ4	2	U72	Interrupt Request Level 4
IRQ5	9	R29	Interrupt Request Level 5
IRQ6	5	U27	Interrupt Request Level 6
IQR7	4	U52	Interrupt Request Level 7
IRQ7	9	R27	Interrupt Request Level 7

\*A line over a signal name such as **ACIACS** indicates an active low signal.

**Table C-1. Mnemonic Listing (Contd.)**

Mnemonic*	Sheet	IC #	Definition
LA0-LA19	1	Several	Local Address Bus (Bits 0-19)
LCCLK	7	U66	Low Frequency Character Clock
LCDEN	2	U60	Liquid Crystal Display Enable
LDOT	7	U79	Low Frequency Dot Clock
LOCK	1	U48	Lock
MA0-MA12	6	U95	Memory Address (Bits 0-12)
MONO BACKOFF	8	U35	Monochrome Backoff
<u>MONOEN</u>	8	U58	Monochrome Enable
<u>MONOEN</u>	2	U60	High Resolution Monochrome Enable
MRD	1	U63	Memory Read
MRD	3	U102	Memory Read
MRW	8	U93	Memory Read/Write
MWC	1	U63	Memory Write Command
NMI	3	U118	Non Maskable Interrupt
<u>NMIMK</u>	4	U149	Non Maskable Interrupt Mask
PA0-PA7	2	Several	Peripheral Interface Ports 0-7
PARITY ERR	3	U117	Parity Error
PCLK	1	U30	Peripheral Clock (1.2 MHz)
<u>PIACS</u>	4	U150	Peripheral Interface Chip Select
<u>PRTCTRL</u>	4	U130	Printer Control
<u>PRTDATA</u>	4	U130	Printer Data
<u>PRTSTAT</u>	4	U130	Printer Status
QS0-QS1	1	U48	Queue Status
RAD0-RAD3	3	U131	Row Address (Bits 0-3)
RAD4-RAD7	3	U151	Row Address (Bits 4-7)
RAD8	3	U132	Row Address (Bit 8)
<u>RADD</u>	6	U82	Row Address Data
<u>RAS0-RAS1</u>	3	U115	Row Address Strobes 0 and 1
RDY	1	U30	Ready
RED	7	U69	Red
<u>RESET</u>	1	U30	Reset
<u>RG1</u>	1	Several	Request/Grant Control
<u>ROM0-ROM1</u>	3	U115	Rom Chip Select
S0-S2	1	U48	Status
<u>SA0-SA7</u>	6	Several	Screen Address (Bits 0-7)
SCCCS	4	U150	Sync/Async Controller Chip Select
SEL A	8	U58	Select A
SEL B	8	U58	Select B
SPKRDATA	2	U60	Speaker Data

\*A line over a signal name such as ACIACS indicates an active low signal.

**Table C-1. Mnemonic Listing (Contd.)**

Mnemonic*	Sheet	IC #	Definition
TIMRCS	4	U150	Timer Chip Select
TMRSPKRGATE	2	U60	Timer Speaker Gate
TOFF	8	U52	Top Offset (for LCD Screen Refresh)
UNDLNE	6	U168	Underline
VIDEO EN	8	U39	Video Enable
VSYNC	6	U95	Vertical Synchronization
<u>WAIT</u>	8	U120	Wait
WE	5	U27	Write Enable

\*A line over a signal name such as **ACIACS** indicates an active low signal.



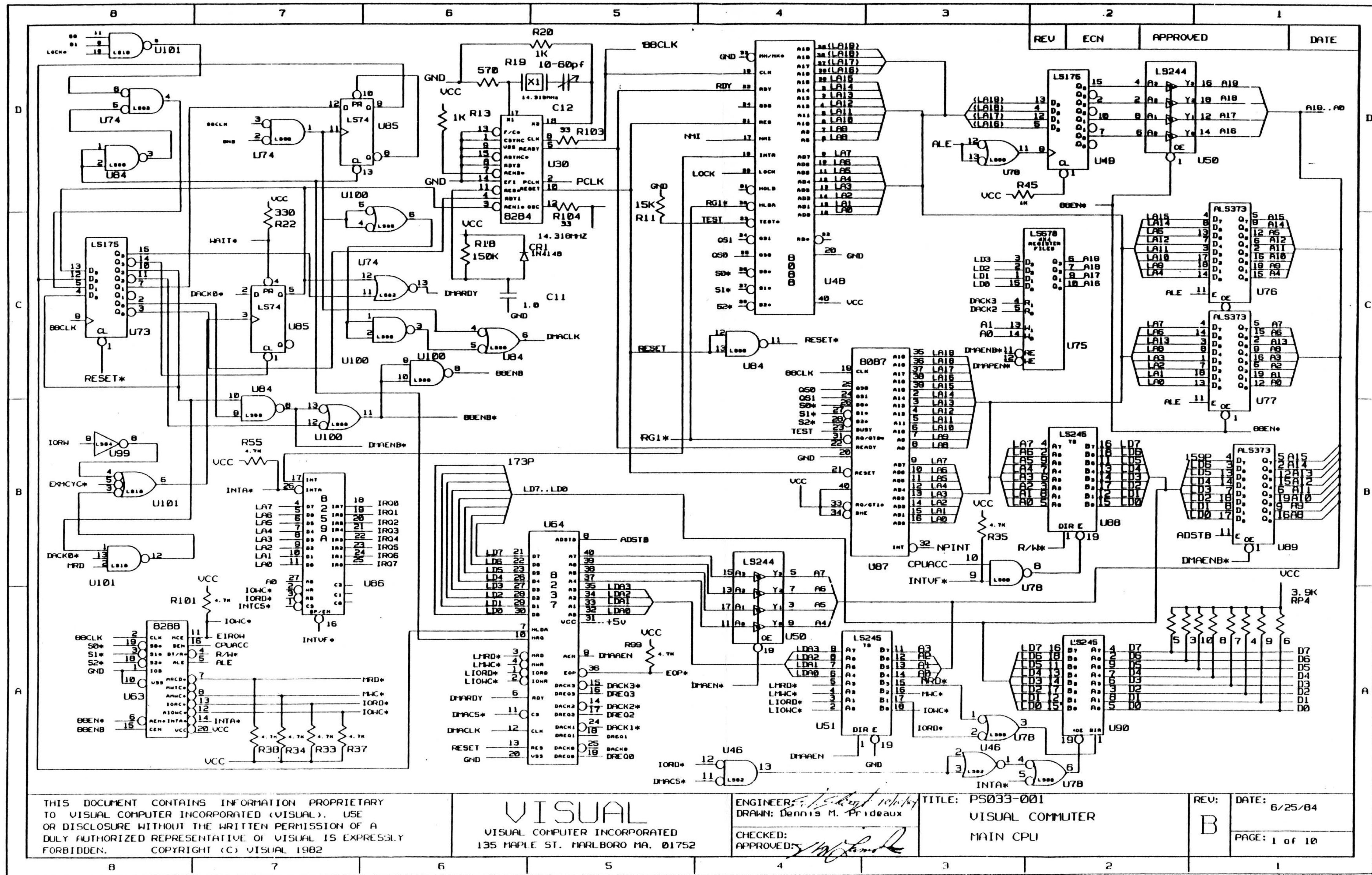
## **APPENDIX D**

### **SCHEMATIC DIAGRAMS**

This appendix contains schematic diagrams for the Commuter system. The following diagrams are included:

- Main CPU
- I/O Keyboard
- System RAM
- Address Decoder and Printer Interface
- Floppy Disk Controller
- CRT Memory
- CRT Timing
- CRT Color Control
- Expansion Port
- Host Communications Interface (Sync/Async Serial Port)
- Switching Power Supply





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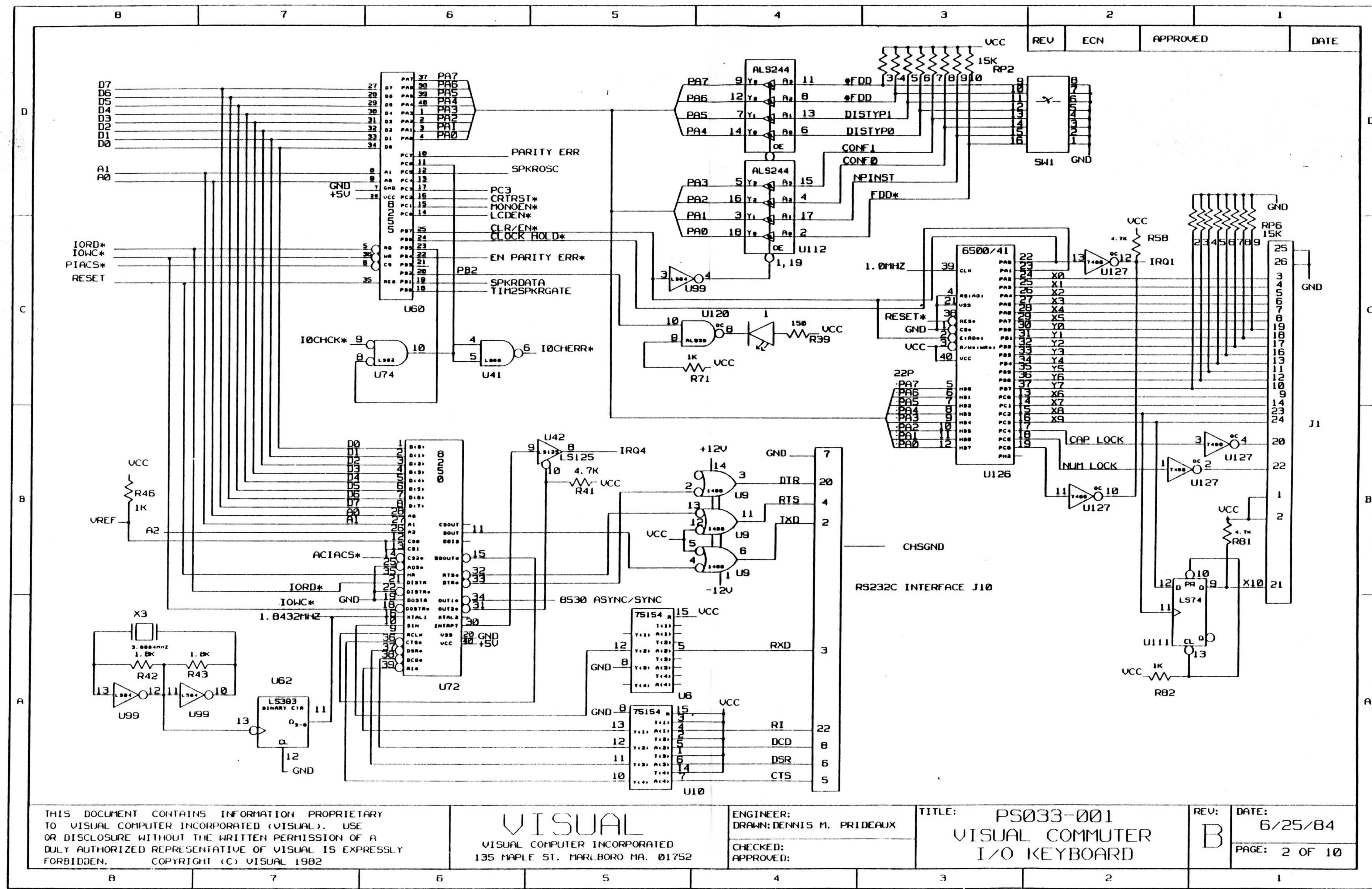
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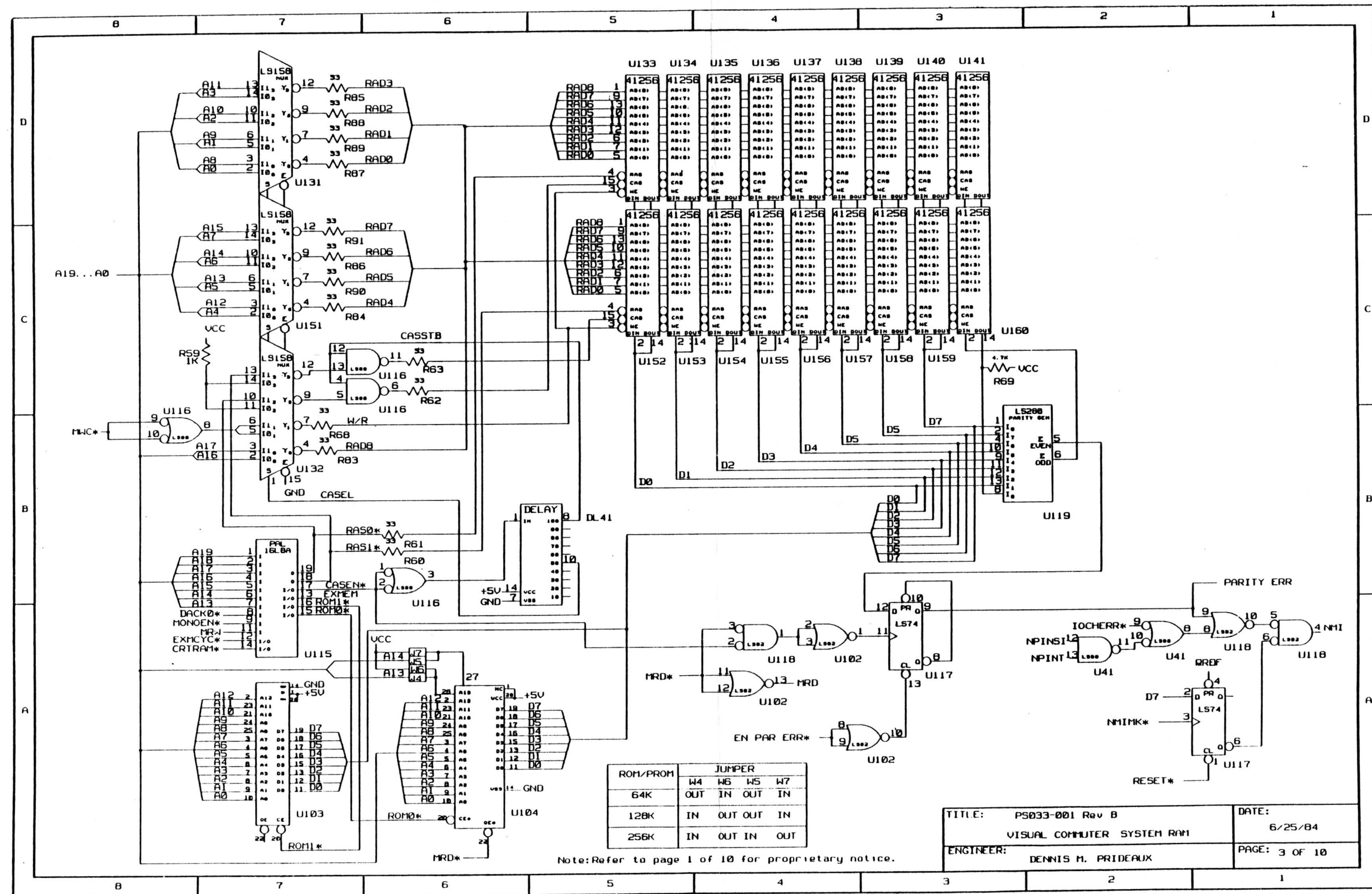
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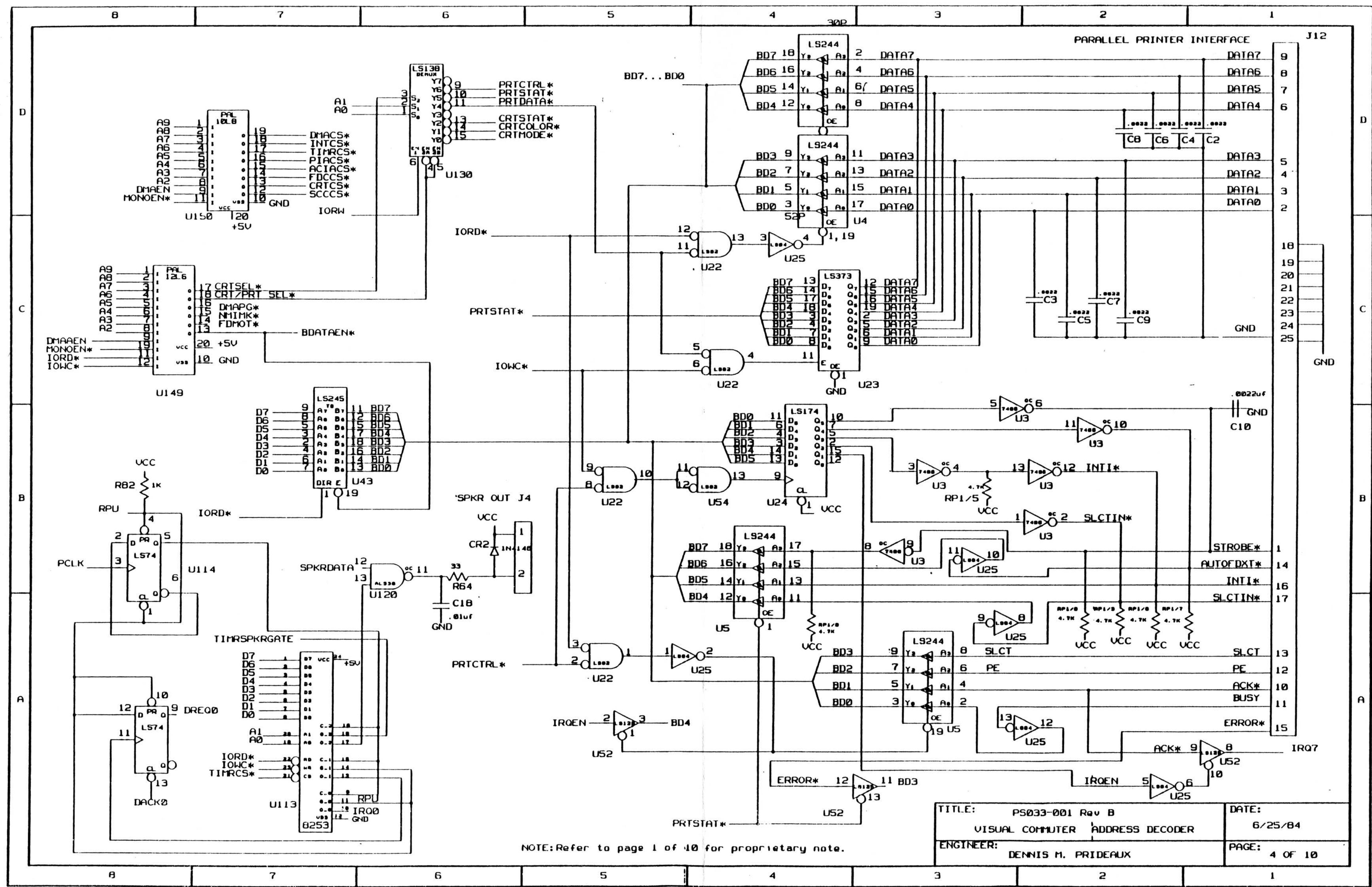




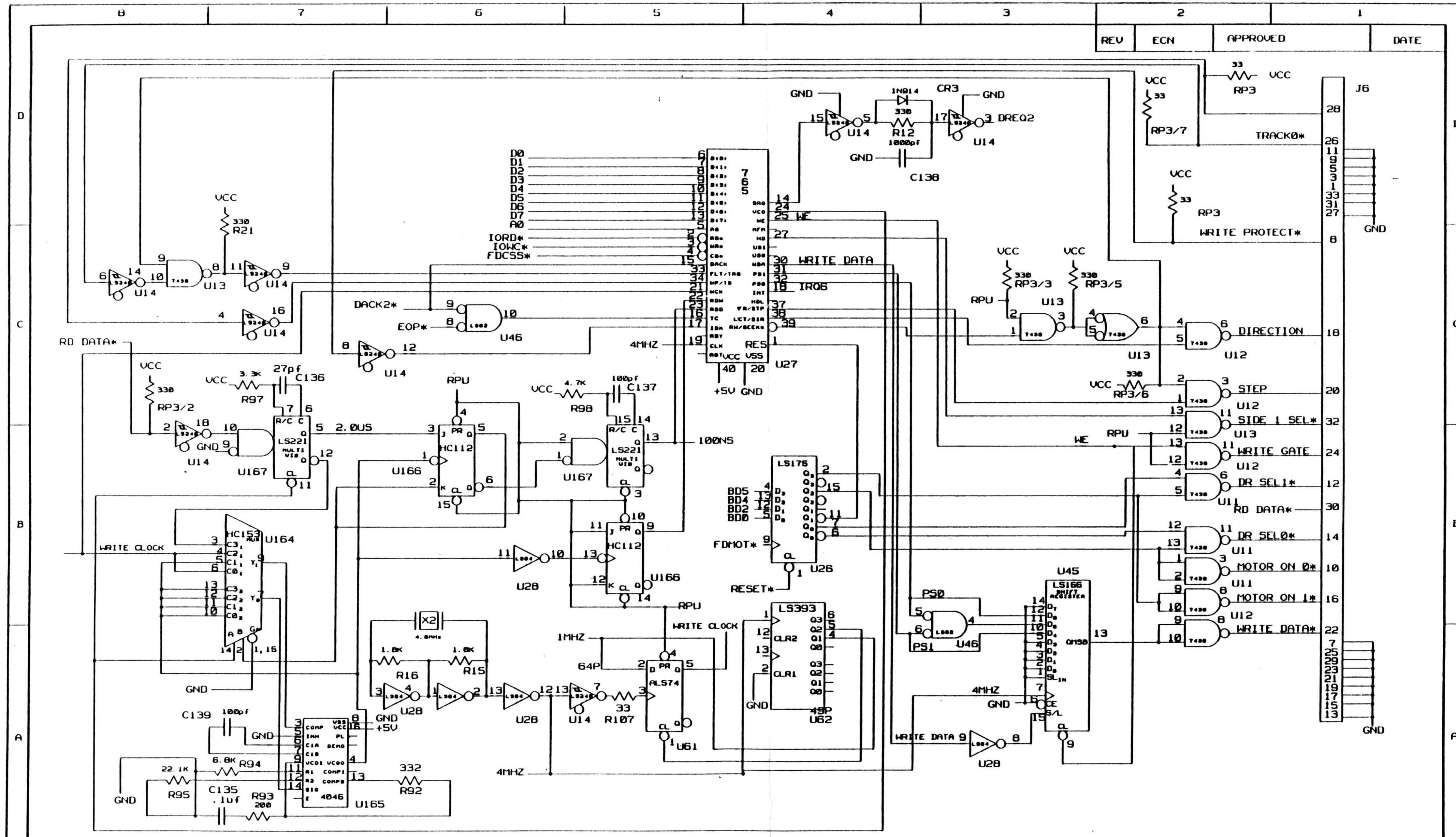












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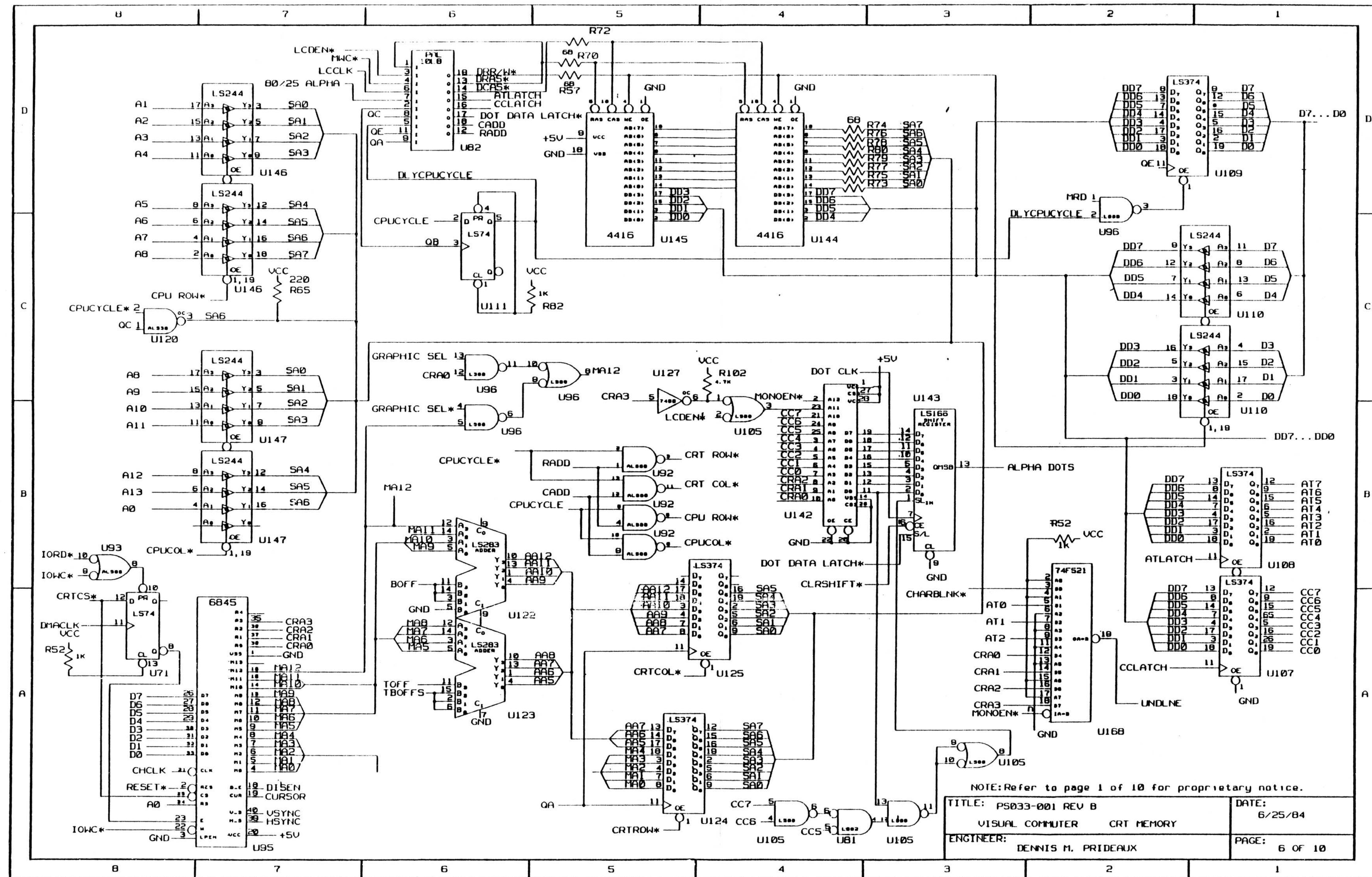
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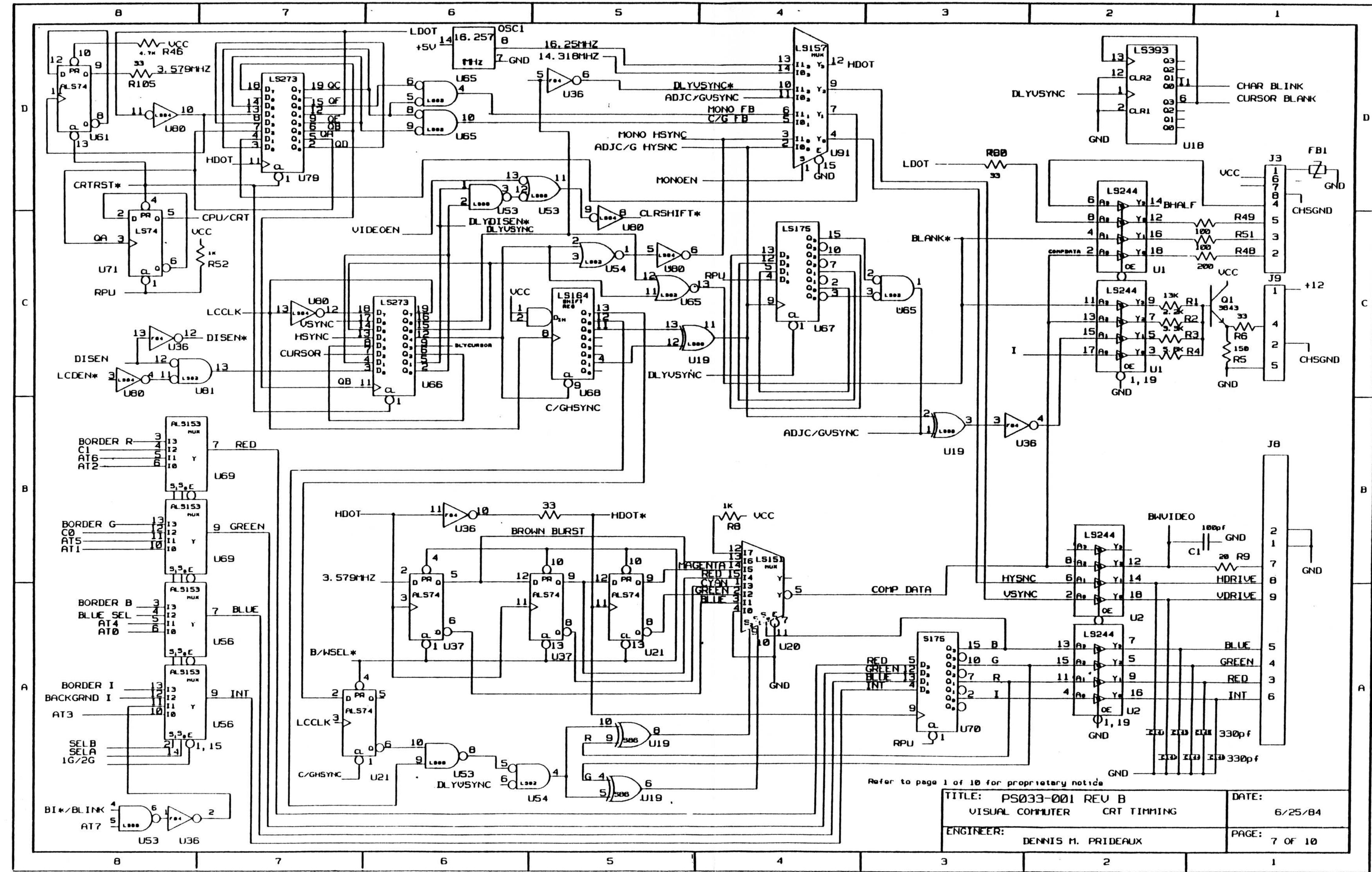
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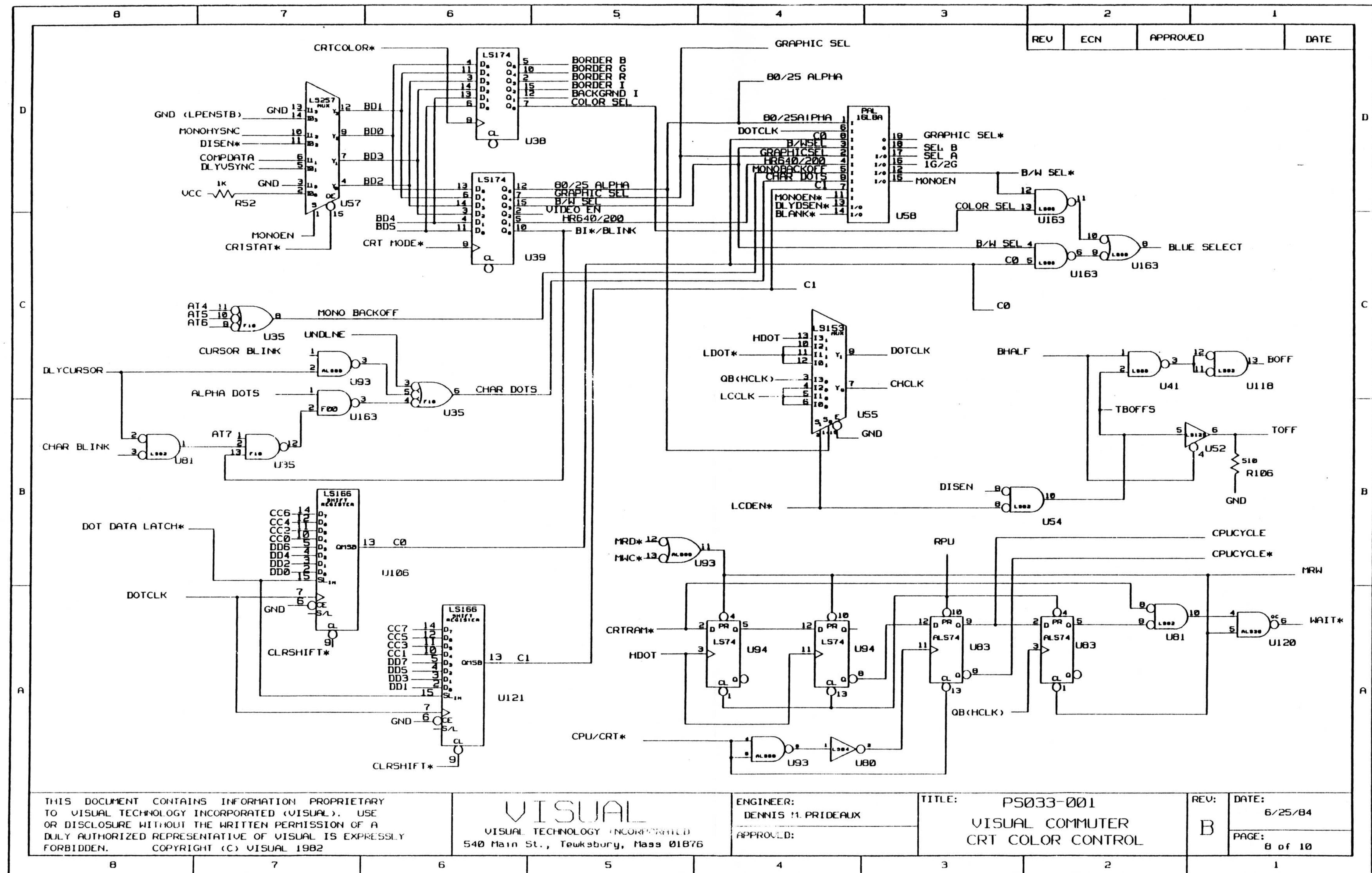
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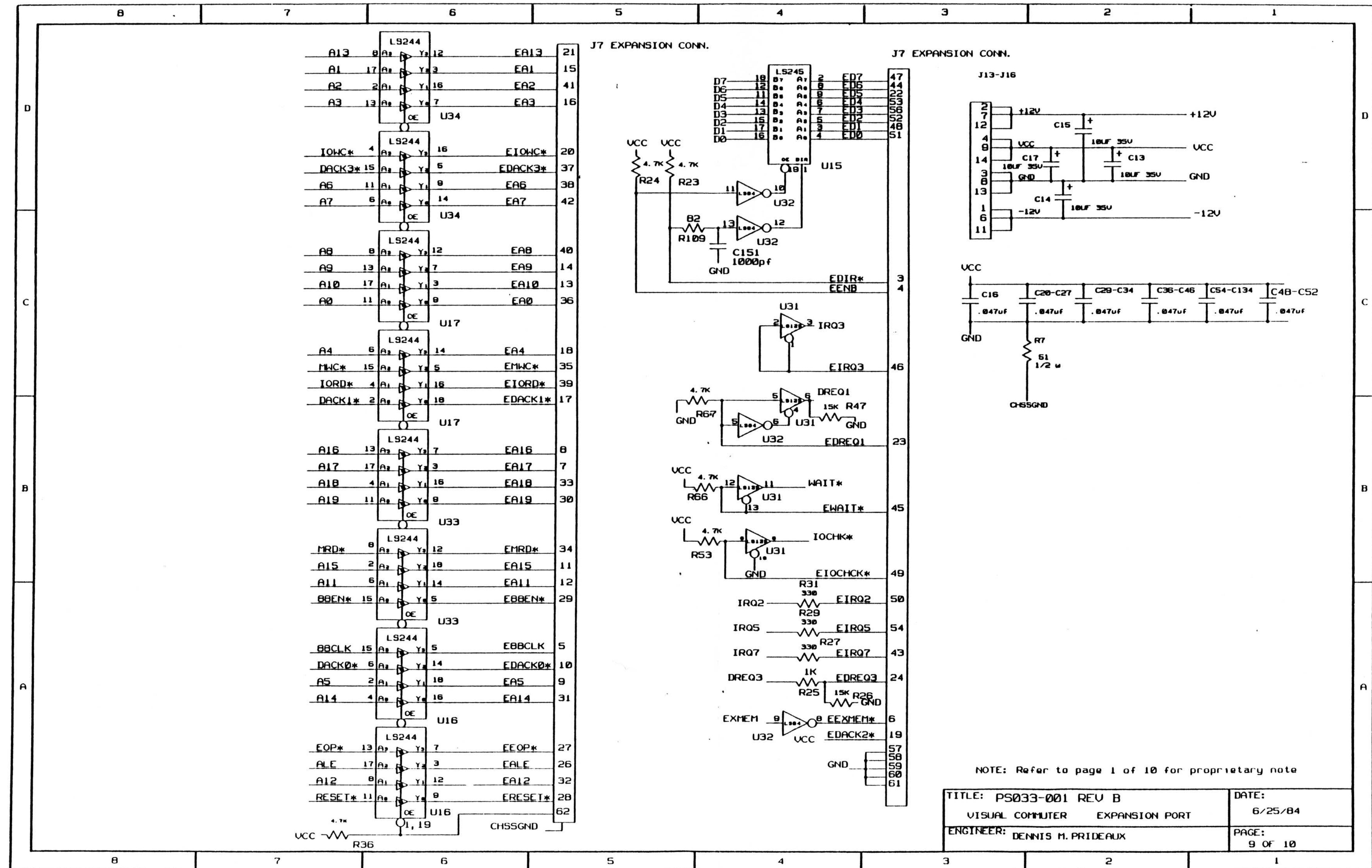




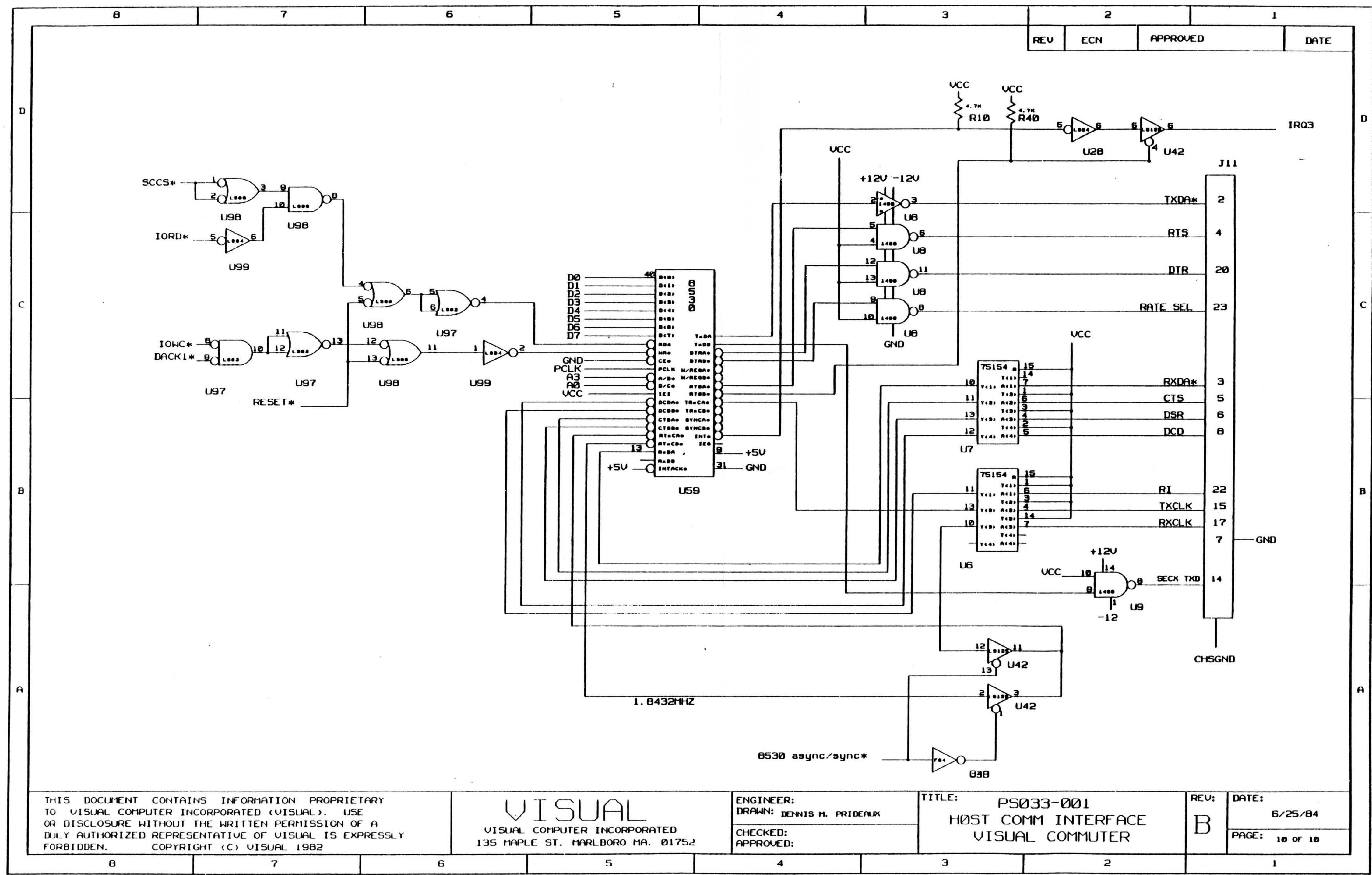












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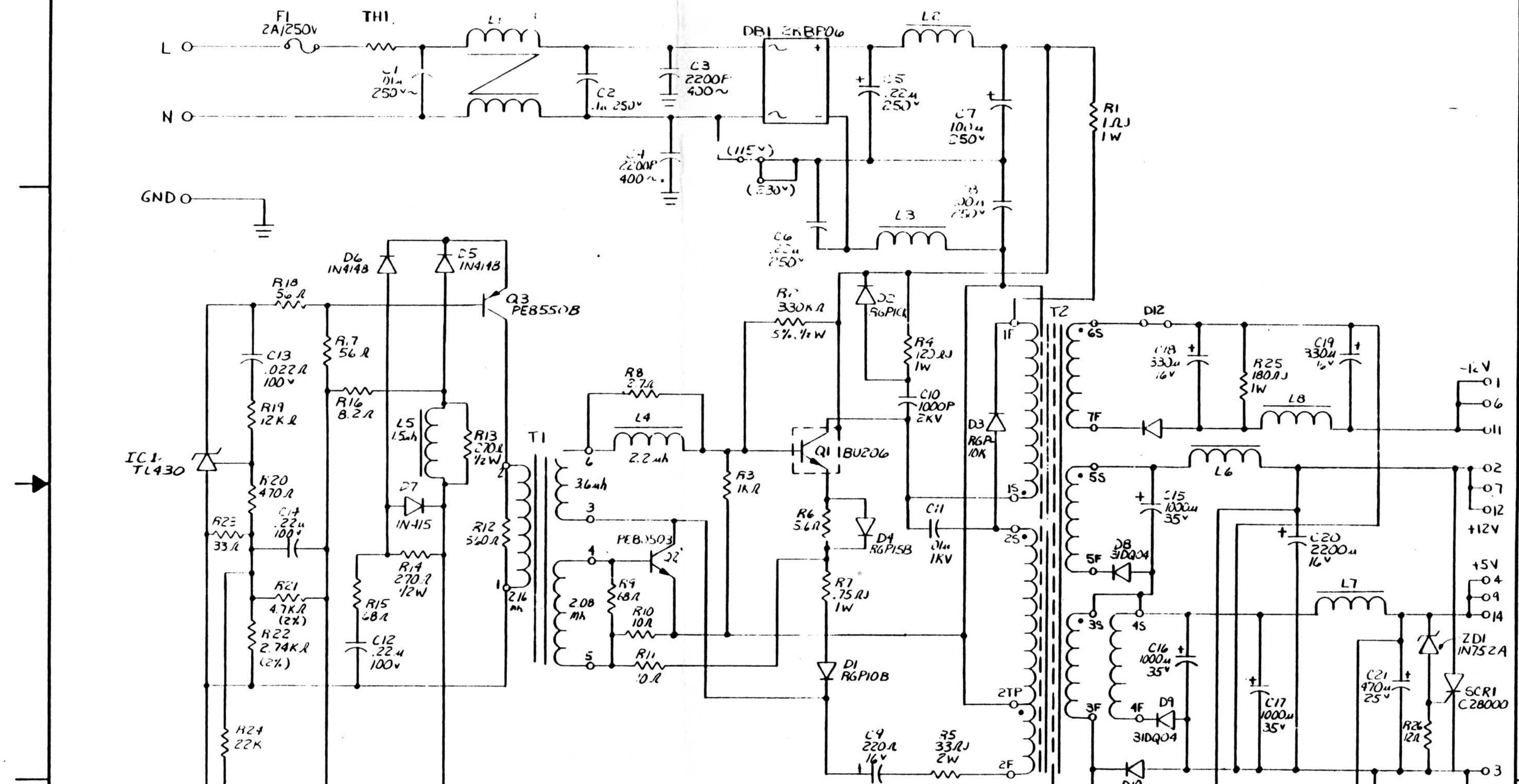
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				Next Assy	UNIT NO PH022-A01
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