Preferred Networks Intern Screening 2017 Coding Task for Chip Development

Changelog

- 2017-05-12 : Initial version

Things to submit

- Please submit the code or the circuit diagram for the tasks you solve. Either is enough. Please submit the report as well.
- If you select the code, use VHDL or Verilog to write it.
- If you select the circuit diagram, please draw it with PowerPoint or drawing tools or manually and submit image files.
- Please write your code so that it will be easy to read for other people. Also, please make sure that it is easy to re-run your program. As for the report, please make sure that it is concise and easy to understand.

How to submit

Submit files should be uploaded to Google drive. After uploading them, please fill in the share URL on the submission form. See the following URL for how to upload files to Google drive:

- Submission form: https://docs.google.com/a/preferred.jp/forms/d/e/1FAIpQLSd_zC_XT2dHM-yRO9WQ-YuRU0sx2HeQIep-NBoqMWpN_j8KNw/viewform
- How to upload files : https://www.preferred-networks.jp/wp-content/uploads/2017/04/intern2017_GoogleUpload_3.pdf

Inquiry

If you have any questions about the problems, please also send these to intern2017@preferred.jp (the same address as used for applying to the internship)

Task description

Please choose and solve two from the following tasks.

1. 4-bit Gray code counter.

Implement a 4-bit Gray code counter.

2. 16-bit adder-subtractor

Implement a 16-bit integer adder-subtractor with logical operations (AND, OR, XOR, NOT). Please design the circuit so that the total number of stages from input signals to output signals is as small as possible. Use two's complement to represent negative values.

3. Implement an arbiter circuit for bus arbitration

Describe it with a state machine diagram or timing chart.

There are three client circuits (A, B, C) that requests to use the bus. Each client requests to use the bus, accepts the request, and finishes (releases) using the bus with the following signals:

- client A
- BUS_REQ - Input signal from client A to the arbiter circuit. It is set to 1 when the bus is requested to be used. It is set to 0 when the request is accepted (A.BUS_GNT is set to 1).
- BUS_GNT - Output signal from the arbiter circuit to client A. It is set to 1 for a 1 clock cycle when the right of use is given to client A.
- BUS_FREE - Input signal from client A to the arbiter circuit. It is set to 1 for a 1 clock cycle at the end (release) of the use of the bus.

Client B and client C have the same signals. Priority of signals is A > B > C when there are multiple requests simultaneously.

4. FIFO

Implement a FIFO whose data width is 32 bit and whose depth is 8.