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1.1 Main Features

1.1.1 Basic Features

Computing Capability

The Hi3660 has the following computing specifications:

- 8-core CPU, including the ARM Cortex-A73 MPCore high-performance heavy cores (four 2.4 GHz cores) and ARM Cortex-A53 MPCore energy-efficient light cores (four 1.8 GHz cores)
- High-performance 3D acceleration technologies, including OpenGL ES 3.2, OpenCL 1.2, OpenCL 2.0, DirectX 11, and Renderscript
- Memory management unit (MMU) management for all the chip channels, reducing the overhead of reserved memories
- 1866 MHz 4-channel low-power double data rate 4 (LPDDR4) and maximum 8 GB space for the double data rate (DDR)

Multimedia Features

The Hi3660 has the following multimedia features:

- Built-in video hardware decoder (H.265/H.264 4096 x 2160@60 fps)
- Built-in video hardware encoder (H.265/H.264 4096 x 2160@30 fps)
- Built-in independent graphics processing unit (GPU), Mali G71 MP8@1 GHz
- 960 megapixel/s throughput rate, up to 23 megapixels@30 fps, and 16 megapixels@30 fps for each of the two pipes
- Independent JPEG encoder and face detection acceleration module
- Dual Mobile Industry Processor Interface (MIPI) Display Serial Interfaces (DSIs), supporting the maximum resolution of 3840 x 2400@60 Hz and multiple IFBCs
- External display interface extended by using the MIPI DSI and Sony/Philips Digital Interface Format (S/PDIF) interface
- TypeC interface supported when the Hi3660 connects to another chip

Table 1-1 Multimedia features of the Hi3660

Media Feature	Description
GPU	
3D acceleration	• OpenGL 3.2/Open VG1.1 • OpenGL ES 1.1/2.0/OpenGL ES 3.0/ OpenGL ES 3.1/ OpenGL ES 3.2 • OpenCL 1.1/1.2/2.0 • DirectX 11.1 Specification • Renderscript
Display pixel depth	RGB888, RGB565
LCD resolution	Maximum resolution of 3840 x 2400, 60 Hz refresh rate
LCD interface	Two MIPI-DSI LCD interfaces. The display data can be compressed to 1/3 or 1/2 of the original data. The 3840 x 2400 display is supported.
TV interface	• External display interface extended by using the MIPI DSI and S/PDIF interface • TypeC interface supported when the Hi3660 connects to another chip
Wi-Fi Display (WFD)	1080p@60 fps
Video encoding	• H.265 or H.264 encoding format • 3840 x 2400@30 fps HD photographing • 4 x 1080p@30 fps simultaneous HD encoding • 720p 240 fps video, supporting fast recording and slow playing
Video decoding	• Decoding formats: H.265, High Efficiency Video Coding (HEVC) MP/High Tier, Main 10/High Tier, H.264 BP/MP/HP, MPEG1/2/4, VC-1, VP6/8, RV8/9/10, Scalable Video Coding (SVC), DIVX, and multiview video coding (MVC) • Up to H.265 4K@60 fps and H.264 4K@30 fps
Audio interface	• SLIMbus, I^2S, and PCM interfaces, supporting the master and slave modes • DSD interface
Audio sampling rate	• 8 kHz • 16 kHz • 32 kHz • 48 kHz • 96 kHz
ADC/DAC	• Five independent DAC channels and four digital DAC channels supported by the analog codec (two channels supporting ultrasonic wave transmission and the other two channels supporting HD playing) • 100 dB signal-to-noise ratio (SNR) ADC (A-weighted) with –80 dB THD and 48 kHz sampling rate
Data precision	24-bit data precision, SNR supported by audio channels
Audio digital signal processor (DSP)	• Hi-Fi 3.0 DSP served as an independent DSP on the Hi3660 and Hi6403 sides • Up to 533 MHz frequency

Media Feature	Description
Audio	MP3 playing
Microphone (MIC) input	Four MIC inputs
Audio effect	Various audio effect processing methods
Audio recording	Dual-track recording
Communication voice	High-performance voice features such as AVS and voice over Long Term Evolution (VoLTE)

1.1.2 Interface Features

Table 1-2 Peripheral interfaces of the Hi3660

Interface	Description
USB port	• USB 3.0 and USB 2.0 On-The-Go (OTG) protocols • BC1.2 charging
PCIe interface	PCIe 1.1/2.0 protocol
Micro SD card interface	• SD 3.0 or SD 2.0 card • High-speed SD card • Hot plug
BT/Wi-Fi air interface	• Wi-Fi: WLAN, portable hotspot, Wi-Fi-DIRECT, compliance with the IEEE802.11 b/g/n/ac protocol • BT: BT 4.1/BT 4.0/BT Class 1.5/ BT Profile (call, A2DP, FTP)
FM air interface	• FM radio over the headphone • FM radio over the FM speaker • FM recording
Mobile TV interface	Integrated Service Digital Broadcasting-Terrestrial (ISDB-T)
Human-machine interface	• Multiple keys. If the keyboard matrix is supported, keys can be extended over the I^2C interface. • Touchscreen • Multi-point touch
MIC interface	The MIC interface supports the following voice inputs: • MIC input • MIC input of the headphone • MIC input of the Bluetooth headphone
I^2C interface	Seven groups of high-speed I^2C interfaces, up to 3 Mbit/s rate
SPI	Five groups of SPIs (master), up to 30 Mbit/s rate

Interface	Description
UART interface	Nine groups of high-speed UART interfaces, up to 9 MBauds frequency
GPIO interface	Multiple GPIO interfaces supported by the Hi3660 and Hi6403
Headset interface	• 3.5 mm headphone output • MIC input of the headphone • MIC with controller (four keys)
Speaker interface	• Extended power amplifier of the stereo speaker • Two line-out interfaces
Receiver interface	One receiver
Keyboard	Keyboard backlight

Table 1-3 Memory interfaces of the Hi3660

Interface	Description
eMMC flash	• eMMC 5.1 and non-volatile memory for storing information such as boot code and data • Bus rate in HS400 mode
Universal Flash Storage (UFS) flash	UFS 2.1 and non-volatile memory for storing information such as boot code and data, supporting in-line encryption
LPDDR4 SDRAM	• Dynamic memory for system running and four channels (each channel supporting at most two chip selects) • 366 balls • 1866 MHz frequency • Maximum capacity of 8 GB
Micro SD card	• Compliance with the SD 3.0 protocol • Support for user data storage, user software installation, and user space extension as the main memory

Table 1-4 Debugging interfaces of the Hi3660

Interface	Description
CoreSight interface	CoreSight debugging interface, supporting the SWD debugging mode
JTAG interface	JTAG debugging interface, which is compliant with *IEEE Std 1149.1*

1.1.3 Low-Power Features

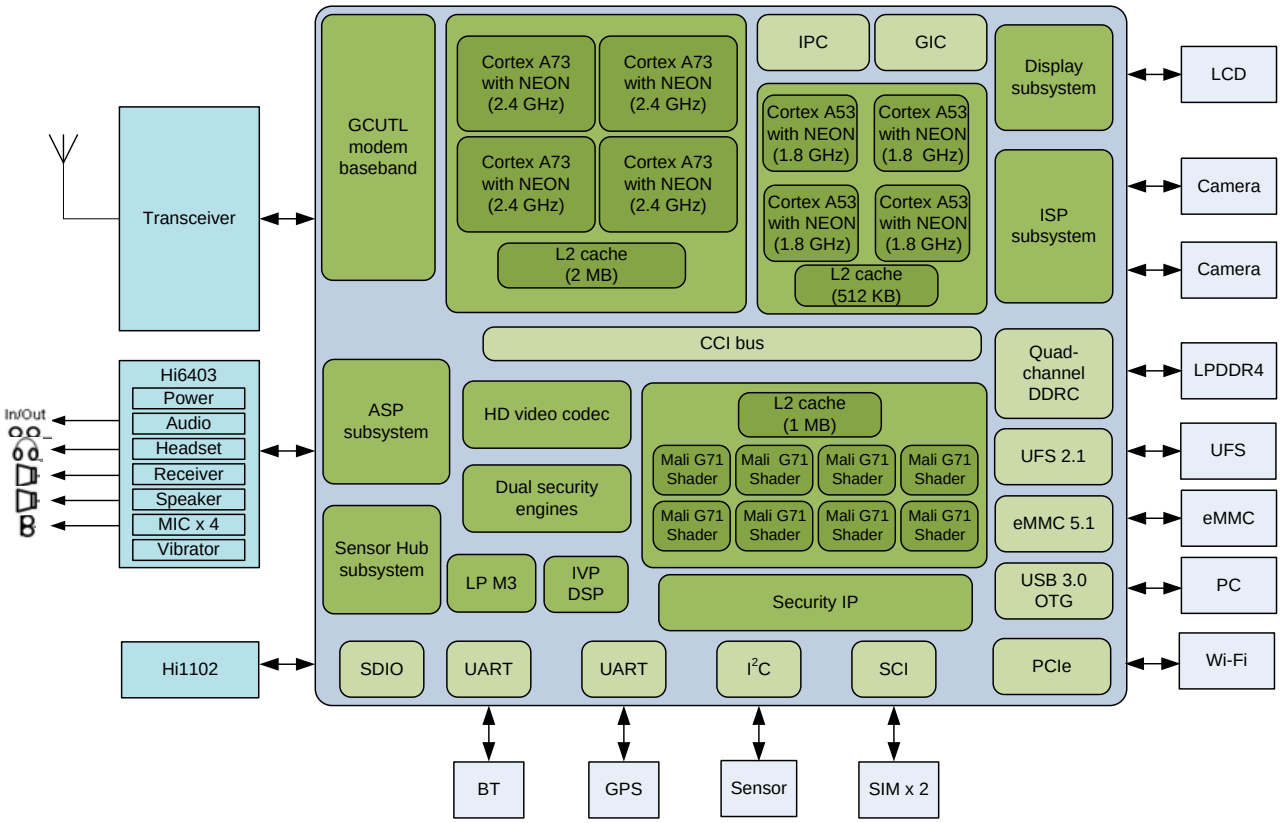
Table 1-5 Low-power features of the Hi3660

Power Consumption Control	Description
Dynamic voltage and frequency scaling (DVFS)	Independent DVFS function for the four Cortex A73 heavy cores, four Cortex A53 light cores, and the GPU
Power management in the idle state	Ultra-low-power design in the idle state to minimize system power consumption

1.2 Chip Architecture

The Hi3660 uses the 16 nm fin field-effect transistor (FinFET) technology of TSMC, and features multiple cores, multiple modes, high performance, and high integration. As the core system on chip (SoC) in the Kirin960 high-end smartphone solution, the Hi3660 provides high-speed mobile computing, integrates various multimedia processing functions and high-specification communication processing functions, and uses the industry-leading low-power technology.

Figure 1-1 Architecture of the Hi3660



The Hi3660 consists of the following functional modules and subsystems:

- Big.LITTLE 8-core CPU subsystem, which contains the ARM Cortex-A73 MPCore high-performance heavy cores (four cores) and ARM Cortex-A53 MPCore energy-efficient light cores (four cores)
- ARM Mali G71 MP8 3D GPU
- Independent image signal processor (ISP)
- 3840 x 2400 HD video hardware decoder and encoder
- Display and graphics acceleration subsystem
- Audio subsystem with one Tensilica Hi-Fi 3.0 DSP
- Peripheral subsystem for the I/O device controllers such as the direction memory access (DMA), PCIe, USB 3.0, and SD card controllers
- DDR and UFS controllers

1.3 Typical Application

The Hi3660 is applied to the smartphone and tablet.

Figure 1-2 Typical (smartphone) application of the Hi3660