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3 Mobile Processing Module

3.1 CPU

3.1.1 Overview

The main processor is a big.LITTLE heterogeneous CPU subsystem that consists of the Cortex-A73 MP and Cortex-A53 MP processors. The Cortex-A73 MP and Cortex-A53 MP processors are based on the ARMv8-A architecture.

The Cortex-A73 MP processor has the following features:

- Processing performance of 3.66 Dhrystone Millions Of Instructions Per Second (DMIPS)/MHz
- Superscaler, variable-length, and out-or-order pipeline
- Dynamic branch prediction with the branch target buffer (BTB), global history buffer (GHB), return address stack, and indirect predictor
- Fully-associative L1 instruction translation lookaside buffer (TLB) with 32 entries, supporting the page entry size of 4 KB, 16 KB, 64 KB, or 1 MB
- Fully-associative L1 data TLB with 48 entries, supporting the page entry size of 4 KB, 16 KB, 64 KB, or 1 MB
- 4-way set-associative L2 TLB with 1024 entries
- Fixed size of 64 KB for the L1 instruction cache and 64 KB for the L1 data cache
- 2 MB L2 cache shared by the data and instruction
- ACE bus interface
- Embedded Trace Macrocell (ETM) trace debugging
- CTI multi-core debugging
- Performance statistics unit with the PMUv3 architecture
- Vector floating point (VFP) and NEON units
- ARMv8-based Cryptography extended instruction
- External generic interrupt controller (GIC)
- Internal 64-bit universal counter for each CPU
- Independent power-off for the CPU core

The Cortex-A53 MP processor has the following features:

- Processing performance of 2.3 DMIPS/MHz

- In-order pipeline, supporting dual-instruction execution
- Direct and indirect branch prediction
- Two independent fully-associative L1 TLBs for instructions and data loads/stores, respectively.10 entries for each TLB
- 2-way set-associative L2 TLB with 256 entries
- 32 KB L1 data cache and 32 KB L1 instruction cache
- 512 KB L2 cache shared by the data and instruction
- ACE bus interface
- ETM trace debugging
- CTI multi-core debugging
- Performance statistics unit with the PMUv3 architecture
- VFP and NEON units
- ARMv8-based Cryptography extended instruction
- External GIC
- Internal 64-bit universal counter for each CPU
- Independent power-off for the CPU core

The Cortex-A73 MP and Cortex-A53 MP processors implement the following functions:

- Cache data coherency by using the CCI-550
- Interrupt virtualization by using the GIC-400
- Timer virtualization by using the system counter
- Event interaction by using the event interface

3.1.2 Operating Mode

3.1.2.1 Operating State

The Cortex-A73 MP and Cortex-A53 MP processors have the following four working states determined by the ARMv8-A architecture:

- Architecture state: AArch32 or AArch64
- Instruction set state, determined by the supported instruction set. The instruction set states include A32, T32, and A64.
- Exception level state. There are four exception level states, as described in Table 3-1.
- Security state: non-secure state or secure state

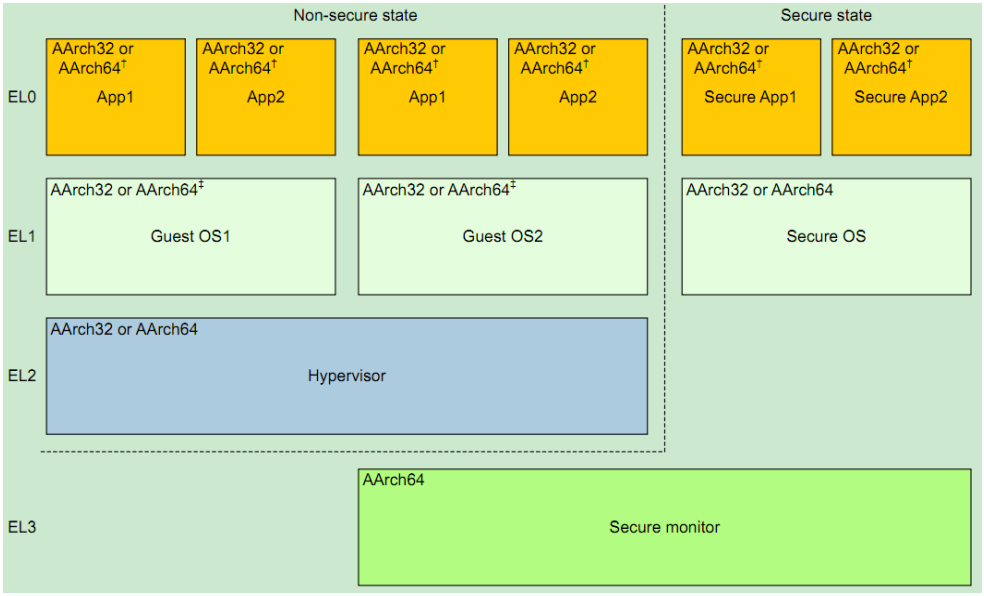
3.1.2.2 Exception Level

Table 3-1 Exception levels of ARMv8-A

Exception Level of the Processor	Description
EL0	Execution mode of the user program, non-privileged, one mode for the Secure World and one mode for the Non-Secure World

Exception Level of the Processor	Description
EL1	Running mode of the operating system, privileged, one mode for the Secure World and one mode for the Non-Secure World
EL2	Mode used for virtualization extension, used only in the Non-Secure World
EL3	Mode used to switch between the Secure World and Non-Secure World

Figure 3-1 Relationship between the running modes



3.1.3 Coherency Bus

The data coherency between the big and LITTLE cores in the big.LITTLE architecture is implemented by using the ARM coherency bus CCI-550. The CCI-550 has the following features:

- Supports the AMBA FULL-ACE and AMBA ACE-Lite protocols and implements data coherency between the big and LITTLE cores as well as other coherency masters.
- Supports the crossbar bus interconnection structure, allowing the upstream master to access the memory and configuration space.
- Implements the snoop filter to improve the snoop performance between coherency masters.
- Supports Distributed Virtual Memory (DVM) message broadcasting between the big and LITTLE cores.
- Supports the bandwidth-based quality of service (QoS) traffic management mechanism.
- Configures the granularity and mode of static interleaving.

- Uses the PMU counter to collect performance statistics of the master, slave, and global events.
- Implements the CCI automatic gating mechanism using the Q-channel handshake.
- Implements the dynamic retention function of the RAM in the CCI using the P-channel handshake.
- Controls the coherency and bus functions using the advanced peripheral bus (APB) slave configuration interface.