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# 7 Storage Control

## 7.1 Overview

The Hi3660 provides the following storage control modules:

- Universal Flash Storage (UFS) controller

  The UFS controller connects to UFS components.

  The protocol version has the following features:

  - Compliance with the UFS 2.1, UniPro 1.6, and M-PHY 3.1 protocols
  - 2-lane transmit (TX) and receive (RX) channels
  - PWM G1–4 and HS G1–3 Rate A/B mode
  - Booting from the UFS and using UFS to meet the major non-volatile storage need

- Embedded multimedia card (eMMC) controller

  The eMMC controller supports the eMMC 5.1 protocol and controls the 8-bit eMMC 5.1 component. The SoC and external eMMC components support system startup and meet the major non-volatile storage need of the system.

- SD card controller

  The SD card controller supports the SD 3.0 protocol, and is backward compatible with the SD 2.0 protocol. The controller connects to external SD cards that comply with the Default-Speed, High-Speed, and UHS-I specifications. The SD card is used to extend the non-volatile storage capacity of the system.

- DDRC

  The double data rate controller (DDRC) supports the 4-channel low-power double data rate 4 (LPDDR4) synchronous dynamic random access memory (SDRAM). Each channel supports at most two ranks. As the major dynamic memory of the system, the LPDDR4 SDRAM provides at most 4-GB dynamic storage space and up to 21.3 GB/s theoretical access bandwidth.

## 7.2 Storage Solution

The Hi3660 supports only two storage solutions, as described in Table 7-1.

**Table 7-1** Storage solution

| No. | Solution Description |
|---|---|
| 1 | 4-channel LPDDR4 + UFS + SD card |
| 2 | 4-channel LPDDR4 + eMMC + SD card |

- The symmetric 4-channel LPDDR4 SDRAM is supported. The data width of each channel is 16 bits. Each channel supports at most 2 chip selects. The maximum operating frequency of the LPDDR4 interface is 1866 MHz.
- The UFS supports the 2-lane TX and RX channels, and the PWM G1–4 and HS G1–3 Rate A/B mode.
- The eMMC supports the 8-bit width and the maximum operating frequency of 200 MHz. The eMMC is backward compatible with various single data rate (SDR) and DDR frequencies.
- The SD card supports the 4-bit width and the maximum operating frequency of 200 MHz. The SD card is backward compatible with various frequencies in SDR mode.

# 7.3 eMMC

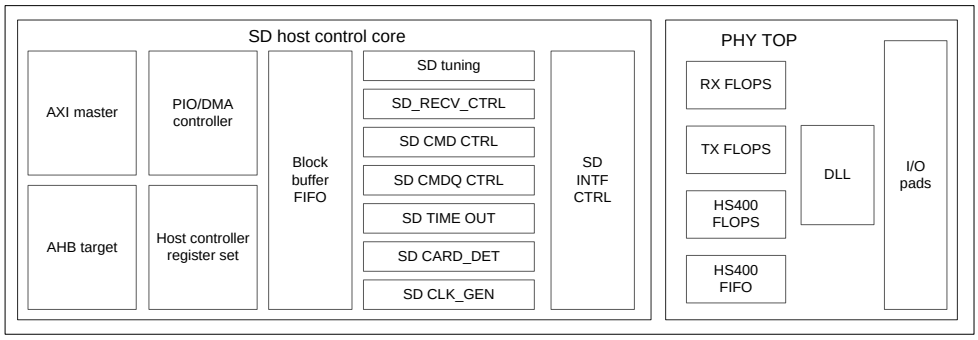
## 7.3.1 Function Description

The eMMC controller is used to receive and transmit commands targeted for the eMMCs and process the data read and write operations on the eMMCs.

The eMMC controller supports the following features:

- Compliance with the JEDEC eMMC 5.1 protocol
- Enhanced strobe
- Command queue (CQ)
- Auto-tuning
- Direct memory access (DMA) transfer in Single Operation DMA (SDMA) or Advanced DMA (ADMA) mode
- Cyclic redundancy check (CRC) on the commands and data

**Figure 7-1** Functional block diagram of the eMMC controller



The eMMC controller consists of the following units:

- Host interface

  The host interface contains the advanced high-performance bus (AHB) target and advanced eXtensible interface (AXI) master. The AHB target is used to configure controller registers and directly read data from or write data to the FIFO. The AXI master is used to read and write data in DMA mode.

- Host controller register set

  The Host controller register set is used to configure registers and read/write FIFO data in Programming Input/Output Model (PIO) mode. The register set supports access to byte operations.

- PIO/DMA controller

  The DMA controller implements the ADMA and SDMA functions. To reduce CPU interference during the read/write process, the DMA controller also transfers data in DMA mode when the eMMC is being read or written. The DMA controller can also directly read data from or write data to the FIFO in PIO mode.

- CQ controller

  The CQ controller implements the CQ function and manages the transmission, query, and execution of tasks.

- Block buffer

  The block buffer is a dual-port data read/write interface and implements data transfer and relay for the bus clock domain and card clock domain.

- Clock generator

  The clock generator is used to divide the clock frequency.

- SD tuning control

  The SD tuning control implements the automatic tuning of the eMMC, transmits tuning commands, checks data, and selects the phase.

- PHY TOP

  The PHY TOP contains the digital circuits of the interface, analog delay-locked loop (DLL), and I/O. The analog DLL contains the TX_DLL, RX_DLL, and STROBE_DLL, which implement the output clock tx_clk, sampling clock rx_clk, and strobe_90 clock, respectively.

## 7.3.2 Register Description

For details about the eMMC IP manual, see https://arasan.com/products/emmc51.html.

# 7.4 SD/SDIO

## 7.4.1 Function Description

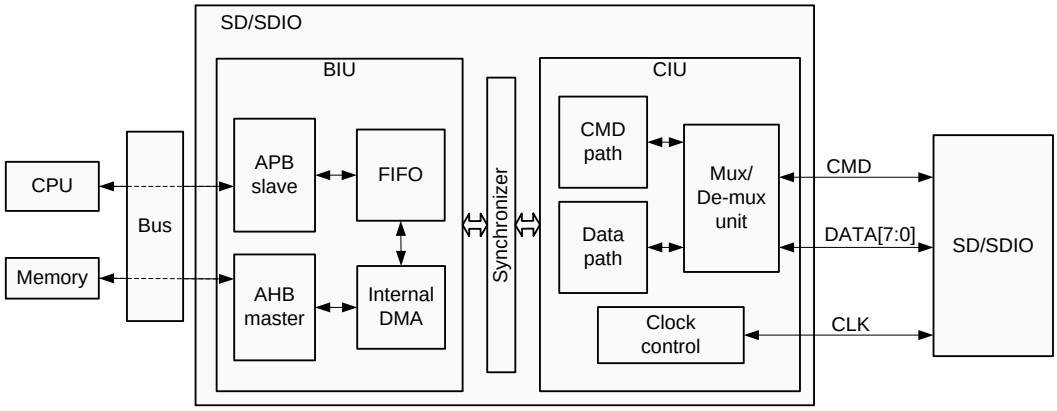
### Functional Block Diagram

The SD/SDIO controller processes the read/write operations on the SD card, and supports extended peripherals such as Wi-Fi devices based on the secure digital input/output (SDIO) protocol. The Hi3660 provides two SD/SDIO controllers (SD and SDIO0), which are used to control the SD card and the Wi-Fi device that uses the SDIO interface, respectively.

The SD/SDIO controller controls the devices that comply with the following protocols:

- Secure Digital memory (SD mem-version 3.0, compatible with 2.0 and 1.1)
- Secure Digital I/O (SDIO-version 3.0, compatible with 2.0)

**Figure 7-2** Functional block diagram of the SD/SDIO controller




The SD/SDIO controller connects to the system through the internal bus. It consists of the following units:

- Bus interface module: Provides the advanced microcontroller bus architecture (AMBA) AHB master and advanced peripheral bus (APB) slave interfaces. The registers are configured and the FIFO is read and written through the APB slave interface. The internal DMA can control the read and write operations on the FIFO data through the AHB master interface.
- Card interface module: Processes protocol-related contents and clocks.
  - Command path: Transmits commands and receives responses.
  - Data path: Reads and writes data by working with the command path.
  - Codec unit: Encodes and decodes the input and output data based on protocols, respectively.
  - Control unit of the interface clock: Determines whether to enable or disable the interface clock, or divides the frequency of the cclk_in clock and uses the output clock as the operating clock of the SD card as required.

The SD/SDIO controller has the following features:

- Internal DMA data transfer
- 256-bit FIFO depth and 32-bit width, configurable FIFO threshold and burst size during DMA transfer
- FIFO overflow and underflow interrupts used to avoid errors during data transfer
- CRC code generation and check for data and commands
- Configurable interface clock frequency
- Disabling of the SD/SDIO controller clock and interface clock in low-power mode
- 1-bit and 4-bit data transfer and SDIO interrupt detection
- Read/Write operations on data blocks with the size ranging from 1 byte to 512 bytes
- Suspend, resume, and read wait operations on the SDIO card

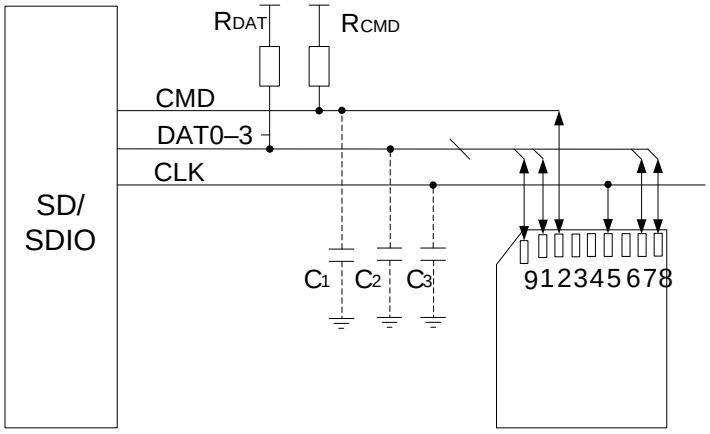
- DDR50 mode not supported

### Typical Application

Figure 7-3 shows the typical application circuit of the SD/SDIO controller by taking the SD card as an example.

The SD/SDIO controller exchanges commands and data with the connected SD card over a clock signal line, a bidirectional command signal line, and four bidirectional data signal lines. The command signal and data signal work in pull-up mode.

**Figure 7-3** Typical application circuit of the SD/SDIO controller




**CAUTION**

Besides the signal lines in Figure 7-3, the card slot also provides the mechanical write protection signal and card detection signal. The system can detect the level on the two signal lines using the GPIO and implement card detection during mechanical write protection and hot plug.

## 7.4.2 Register Description

For details about the SD/SDIO IP manual, see https://www.synopsys.com/dw/ipdir.php?ds=dwc_sd_emmc_host_controller.

# 7.5 UFS

## 7.5.1 Function Description

The UFS controller is used to receive and transmit commands targeted for the UFS mass storage devices and process the data read and write operations on these devices. The UFS is a simple and high-performance serial interface that supports mass storage media. It is used for the mobile phone system.

The UFS controller supports the following features:

- Compliance with the JEDEC UFS 2.0 protocol
  - Higher speed up to HS-G3 (High-Speed Gear 3)
  - Symmetric 2RX-2TX lanes, supporting two lanes
  - Auto-hibernate entry and exit sequences
- Compliance with the JEDEC UFSHCI 2.1 protocol
  - Up to 32 task requests
  - Up to eight task management requests
  - Pre-fetching more than one PRD entry (up to 16 PRD entries)
  - Clock gating ready design
  - Inline encryption (IE)
- Compliance with the MIPI UniPro 1.6 and MIPI UniPro 1.6 protocols
  - SKIP symbol insertion
  - Scrambling for EMI mitigation
  - HS-Gear3 adaption
  - Advanced granularity support

## 7.5.2 Register Description

For details about the UFS IP manual, see https://www.synopsys.com/dw/ipdir.php?ds=ufs.