Contents

6 Media Processing

6.1 Overview

The Hi3660 integrates a powerful multimedia processing subsystem. This subsystem is used for applications such as picture capturing and processing, LCD control, video encoding/decoding acceleration, 2D/3D graphics acceleration, and audio capturing/output processing.

6.2 VENC

The Hi3660 integrates the H.264/H265/JPEG hardware video encoder (VENC), which supports the H.264/H265/JPEG encoding standard, respectively.

The VENC has the following features:

- One JPEG encoder
  - ITU-T T.81 Baseline (sequential) discrete cosine transform (DCT)-based coding
  - Input data formats: 420PL111YCbCr8, 420PL12YCbCr8, 420PL12YCrCb8, 422PL111YCbCr8, 422PL12YCbCr8, 422PL12YCrCb8, 422IL3YCbYCr8, 422IL3YCrYCb8, 422IL3CbYCrY8, and 422IL3CrYCbY8
  - Output data formats: JFIF 1.02 and non-progressive JPEG
  - Maximum 16K x 16K pixels, 16-pixel horizontal/vertical step
- One H.264 encoder
  - Features supported by H.264 Baseline Profile

    I slice and P slice

    The 4 x 4 and 16 x 16 intra-frame division methods support the DC/V/H prediction mode.

    The 8 x 8 and 16 x 16 inter-frame division methods are supported.

    The MB-level bit rate control is supported.

    The inter-frame prediction is supported for the 1/2 and 1/4 pixels.

    The cosine transform supports Hadamard transform.

    De-blocking is supported.
  - New feature supported by H.265 Main Profile on the basis of H.264 Baseline Profile

    The context-adaptive binary arithmetic coding (CABAC) is supported.

  - New features supported by H.265 High Profile on the basis of H.264 Baseline Profile
    Apart from the 4 x 4 conversion, the 8 x 8 conversion is also supported.
    The 8 x 8 intra-frame prediction is supported.
  - Input data formats
    Planar YUV 4:2:0
    Planar YUV 4:2:2
    Semi-planar YUV 4:2:0
    Semi-planar YVU 4:2:0
    Package UYVY4:2:2, VYUY4:2:2
    Package YUYV4:2:2, YVYU4:2:2
    ARGB/BGRA8888
    ABGR/RGBA8888
  - Output data formats: raw streams in the preceding formats
  - Maximum 4K x 2K pixels, 2-pixel horizontal/vertical step
  - Maximum frame rate of 720p@240 fps
  - Maximum bit rate of 80 Mbit/s
  - 4K x 2K@30 fps performance for a single pipe
  - Frame storage format: linear
  - Minimum size of 176 x 144
  - Maximum 1/4x horizontal/vertical scaling
  - Region of interest (ROI) encoding
  - Multi-channel encoding: 4-channel H.264 encoding
- One H.265 encoder
  - Features supported by H.265 Main Profile
    I slice and P slice
    The 4 x 4, 8x 8, 16 x 16, and 32 x 32 intra-frame division methods are supported. The 4 x 4, 8x 8, and 16 x 16 division methods support 35 prediction modes. The 32 x 32 division supports the DC/Planar prediction mode.
    The 8x 8, 16 x 16, 32 x 32, and 64 x 64 inter-frame division methods are supported.
    The CU-level bit rate control is supported.
    The ±512 horizontal integer search and ±144 vertical integer search are supported.
    The inter-frame prediction is supported for the 1/2 and 1/4 pixels.
    DCT4/8/16/32 and DST4 are supported.
    Merge and MergeSkip are supported.
    TMV is supported.
    De-blocking and sample adaptive offset (SAO) are supported.
  - Input data formats
    Planar YUV 4:2:0
    Planar YUV 4:2:2
    Semi-planar YUV 4:2:0
    Semi-planar YVU 4:2:0
    Package UYVY4:2:2, VYUY4:2:2

Package YUYV4:2:2, YVYU4:2:2

ARGB/BGRA8888

ABGR/RGBA8888

- Output data formats: raw streams in the preceding formats
- Maximum 4K x 2K pixels, 2-pixel horizontal/vertical step
- Maximum frame rate of 720p@240 fps
- Maximum bit rate of 60 Mbit/s
- 4K x 2K@30 fps performance for a single pipe
- Frame storage format: linear
- Minimum size of 176 x 144
- Maximum 1/4x horizontal/vertical scaling
- ROI encoding
- Multi-channel encoding: 4-channel H.265 encoding

6.3 VDEC

The Hi3660 integrates a video decoder (VDEC), which supports the H.265, H.264, MPEG1, MPEG2, MPEG4, VC1 (including WMV9), VP6, and VP8 protocols.

The VDEC consists of the video firmware (VFMW) running on the ARM processor and an embedded hardware video decoding engine. The VFMW obtains streams from the upper-layer software, parses the streams, and calls the video decoding engine to generate the image decoding sequences. Under the control of the upper-layer software, the downstream module outputs the sequences to a monitor or other devices.

6.4 DSS

The display subsystem (DSS) implements overlaying and 3D synthesis for multiple graphics layers such as the Base, Video, and Graphic, and sends the overlaid or synthesized pixels to the Display Serial Interface (DSI) or HDMI for displaying.

6.5 ASP

The audio signal processor (ASP) is a subsystem used to manage and process various audio and voice data applications. The ASP supports the following application scenarios:

- Audio playing
- Audio recording
- Digital FM playing
- Bluetooth voice dialing (audio recording)
- Uplink and downlink calling
- Audio mixing
- Voice wakeup

6.5.1 DSP

The audio digital signal processor (DSP) uses the Tensilica Hi-Fi 3.0 processor, and implements HD video sound decoding (such as DTS) and post-processing as well as common audio decoding (such as MP3) of the dedicated player.

6.5.2 SIO

The Sonic Input/Output (SIO) interface connects to the off-chip audio codec to play and record music (voice). The SIO transfers the digital data that complies with the I^2S/PCM protocol. The ASP integrates two SIOs: SIO0 and SIO2. SIO0 is SIO_AUDIO, which plays and records music, and supports the inputs and outputs in the I^2S and PCM formats. SIO2 is SIO_BT, which is used for Bluetooth calling.

- The SIO module supports the master and slave modes as well as playing transmit (TX) and recording receive (RX).
- The SIO module supports the I^2S and PCM interface timings. The interface signal lines in two modes are multiplexed.
- The SIO module supports only the inputs of the clock and synchronization signals. In I^2S master mode, the SIO module needs to work with the CRG module and the CRC module sends the clock and synchronization signals to the outside.

The SIO module has the following features in I^2S mode:

- The I^2S interface supports the 16-bit, 18-bit, 20-bit, 24-bit, and32-bit transfer modes.
- The 8–192 ksps sampling rate is supported.
- The extended module supports 2-/4-/8-/16-channel RX and 8-/16-bit transfer mode.
- The I^2S RX and TX channels have independent FIFOs. The audio-left and audio-right channels each has an independent FIFO. The FIFO depth is 16 and the width is 32 bits.
- The I^2S interface supports the function of disabling the FIFO. When a FIFO is disabled, the RX and TX data is stored in a buffer rather than the FIFO.
- The I^2S interface allows the TX and RX channels to be separately enabled. If a channel is disabled, the control unit and data storage unit of this channel are not reversed. In this way, power consumption is saved.
- For the I^2S interface in 16-bit transfer mode, the RX/TX data of the audio-left and audio-right channels can be combined into one 32-bit data segment and then stored/written into the RX/TX FIFO. In this way, the buffering capacity of the FIFO is improved. The extended module does not support this combination function.
- The RX channel supports upper-bit sign extension.
- The TX and RX audio channel selection signals can be the same, facilitating connection with the 4-wire codec.

The SIO module has the following features in PCM mode:

- The 8-bit and 16-bit transfer modes are supported.
- The extended module supports 2-/4-/8-/16-channel RX and 8-/16-bit transfer mode.
- Only the short frame synchronization mode is supported. Both the standard and customized timing modes are supported.
- The RX and TX channels have independent FIFOs. The FIFO depth is 16 and the width is 32 bits.
- The FIFO can be disabled. When a FIFO is disabled, the RX and TX data is stored in a buffer rather than the FIFO.

- The TX and RX channels can be separately enabled. If a channel is disabled, the control unit and data storage unit of this channel are not reversed. In this way, power consumption is saved.
- The RX channel supports upper-bit sign extension.

The SIO module also provides the CPU/DSP access interface, which has the following features:

- The CPU/DSP can access the SIO using the advanced high-performance bus (AHB) Slave (AMBA 2.0) interface provided by the SIO module.
- The SIO AHB interface supports only 32-bit operations.
- The SIO AHB interface supports only the OK response, and does not support the ERROR, Retry, and Split responses.
- The SIO AHB interface supports various burst operations.
- The SIO supports direct memory access (DMA) operations in burst mode.
- The SIO allows the audio-left and audio-right channels to use the same TX address for the TX data and the same RX address for the RX data.

NOTE

- The master and slave modes of the SIO module differ in the sources of the clock (BCLK) and sampling rate (ADWS). In master mode, the AP side of Hi3660 generates the clock and sampling rate. In slave mode, the AUDIO_CODEC side generates the clock and sampling rate. The master and slave modes are not related to the TX and RX.
- If the data width is 24 bits or 32 bits in PCM mode, only the upper-16-bit data is transferred because the maximum bit width of the SIO is 16.