BLG212E – MIDTERM EXAM ANSWERS

QUESTION 1) [15 points]

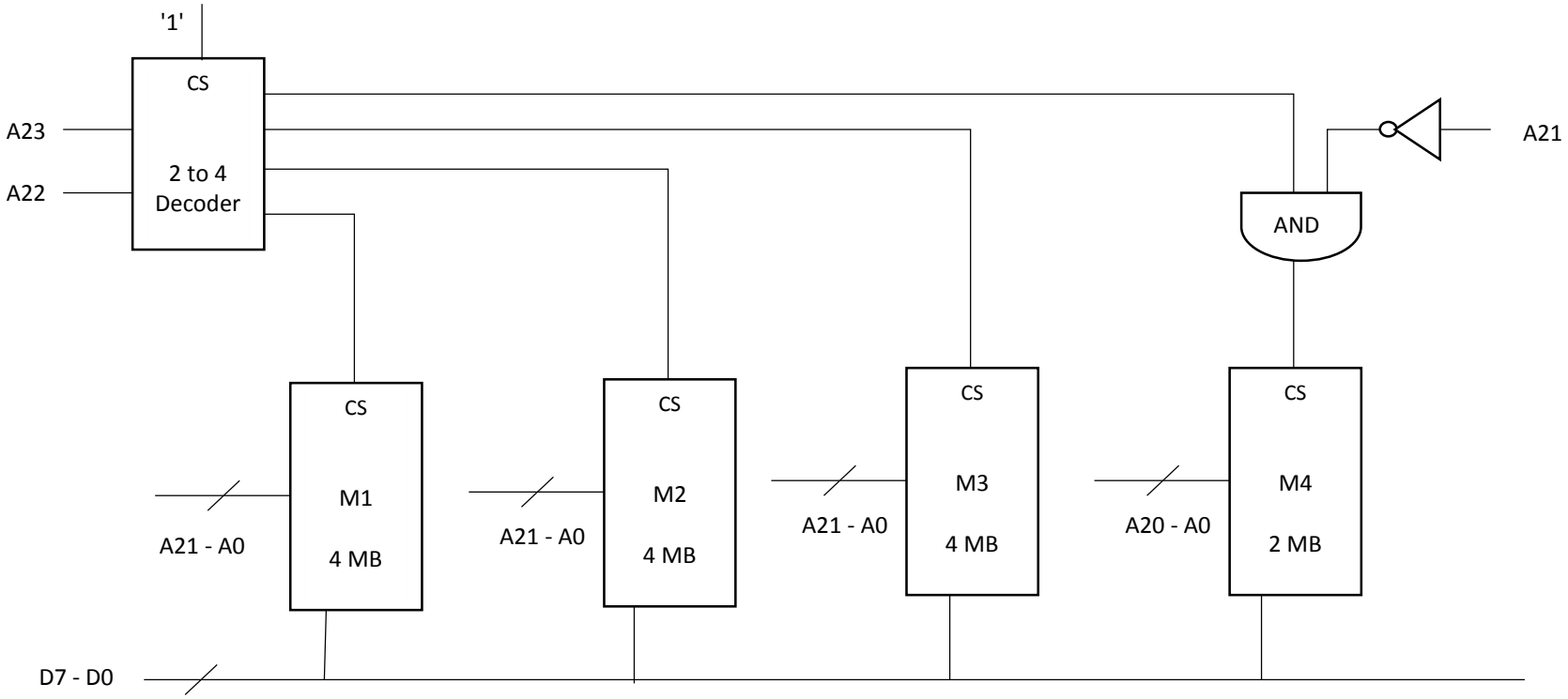
a) [5 points]	b) [5 points]	c) [5 points]
Both are unsigned. X = 1000 0100 (132 decimal) Y = 1011 1010 (186 decimal) +---------- 1 0011 1110 (318 decimal, but with 9 bits) 0011 1110 (Actual = 62 decimal, carry discarded) FLAGS: Carry: Carry out of Result MSB (Most Significant) bit. Overflow : X MSB (1) + Y MSB (1) --> Result MSB (0)	Both are signed. X = 0111 1000 (+120 decimal) Y = 0100 0110 (+70 decimal) +---------- 1011 1110 (190 decimal, but max signed is +127) 1011 1110 (or -66 decimal, same as 190) FLAGS: Negative : Result MSB is 1 (sign bit). Overflow : X MSB (0) + Y MSB (0) --> Result MSB (1)	Both are signed (two's complement). X = 1111 1011 (-5 decimal) Y = 1111 1101 (-3 decimal) +---------- 1 1111 1000 (+504 decimal, but with 9 bits) 1111 1000 (Actual = -8 decimal, carry discarded) FLAGS: Carry: Carry out of Result MSB bit. Half Carry: Carry out of Result 3rd to 4th bit. Negative : Result MSB bit is 1 (sign bit).

QUESTION 2) [35 points]

a) [15 points] Addressable range is from 00 0000 to FF FFFF, which contains 6 hexadecimal digits.
Since each hexadecimal digit is 4 bits, 6 * 4 = 24 bits are required as minimum number of address lines.
Total addressable capacity of memory = $2^{24} = 2^4 * 2^{20}$ = 16 MB

Memory Chip	Smallest Address	Biggest Address	Calculating Number of Locations = (Biggest - Smallest) + 1	Number of Locations (2^{20} = 1 MB)	Capacity (Mega Bytes)
M1	00 0000	3F FFFF	3F FFFF - 00 0000 --> 3F FFFF 3F FFFF + 1 --> $(40\ 0000)_{16}$ locations	4.2^{20}	4 MB
M2	40 0000	7F FFFF	7F FFFF - 40 0000 --> 3F FFFF $(40\ 0000)_{16}$ locations	4.2^{20}	4 MB
M3	80 0000	BF FFFF	BF FFFF - 80 0000 --> 3F FFFF $(40\ 0000)_{16}$ locations	4.2^{20}	4 MB
M4	C0 0000	DF FFFF	DF FFFF - C0 0000 --> 1F FFFF 1F FFFF + 1 --> $(20\ 0000)_{16}$ locations	2.2^{20}	2 MB
EMPTY	E0 0000	FF FFFF	FF FFFF - E0 0000 --> 1F FFFF $(20\ 0000)_{16}$ locations	2.2^{20}	2 MB

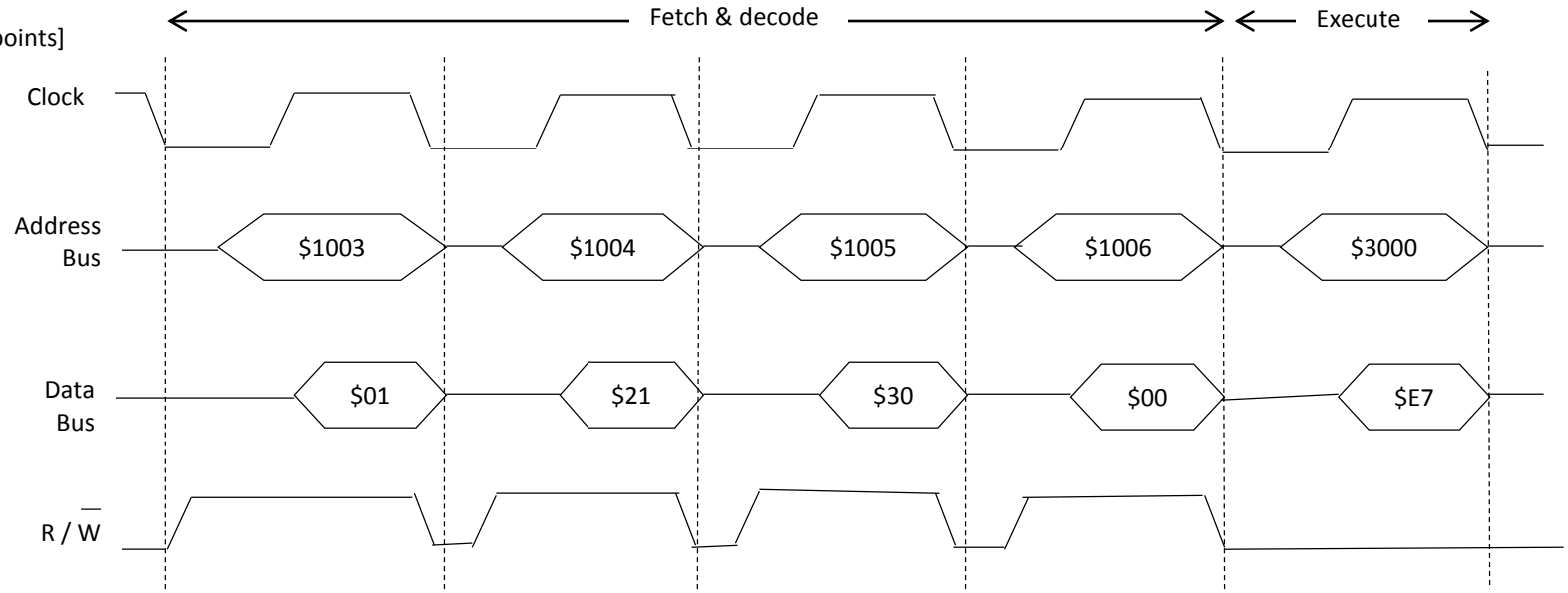
b) [20 points] The following is the shortest answer, other correct answers are also accepted.



To distinguish M4 from Empty addresses, A21 should be 0 (inverted A21) for M4's chip select, and should be 1 for Empty addresses.
If A21 is not used in design (for M4 chip selection), empty addresses can select the M4 chip.

QUESTION 3) [20 points]

a) [15 points]



b) [5 points]

Frequency = 10 MHz

$$Clock\ period\ (seconds) = \frac{1}{Frequency\ (Hertz)}$$

$= 1/(10 * 10^6) = 10^{-7}\ seconds$

$= 10^{-7} * 10^9\ \ nanoseconds$ = 100 nanoseconds

The STA instruction takes 5 clock periods to complete.
Therefore it takes 5 * 100 = 500 nanoseconds.

QUESTION 4) [30 points]

```
COUNT  EQU  5    ; Number of elements in arrays

ARRAY1   RMB  1
   ORG  ARRAY1
   DAT  10,20,30,40,50

ARRAY2   RMB  1
   ORG  ARRAY2
   DAT  60,70,80,90,100

TOTAL_ARRAY  RMB  COUNT
AVG_ARRAY    RMB  COUNT

START
   LDA  CD, 0      ; Loop counter

CONTINUE
   LDA  SK, ARRAY1
   LDA  A, <SK+CD+0>

   LDA  SK, ARRAY2
   ADD  A, <SK+CD+0>

   LDA  SK, TOTAL_ARRAY
   STA  A, <SK+CD+0>

   LDA  SK, AVG_ARRAY
   LSR  A            ; Logical Shift Right (means divide by 2)
   STA  A, <SK+CD+0>

   INC  CD
   CMP  CD, COUNT
   BLT  CONTINUE
   INT
```

Totals and Averages of corresponding elements.

ARRAY1	ARRAY2	TOTAL_ARRAY	AVG_ARRAY
10	60	70	35
20	70	90	45
30	80	110	55
40	90	130	65
50	100	150	75