

# Rock and a Hard Place

## How Hard It Is To Be a CPU Idle Time Governor

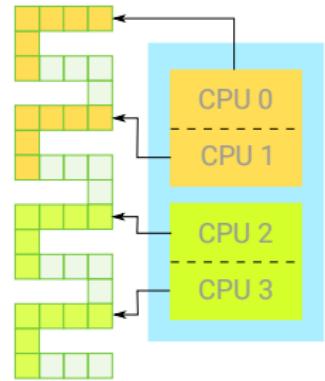
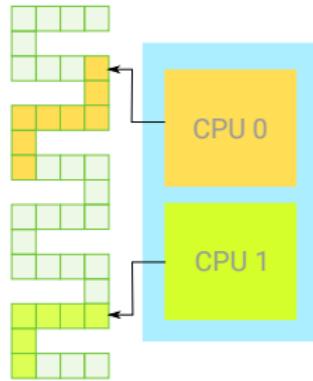
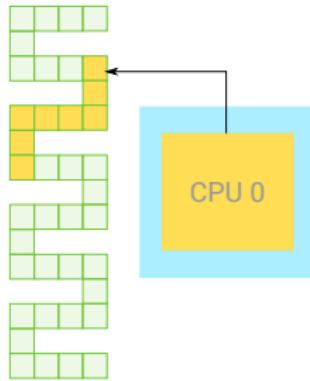
Rafael J. Wysocki

Intel Linux Systems Engineering

May 20, 2019



# Terminology: CPUs = Logical CPUs



# CPUs: Busy Vs Idle

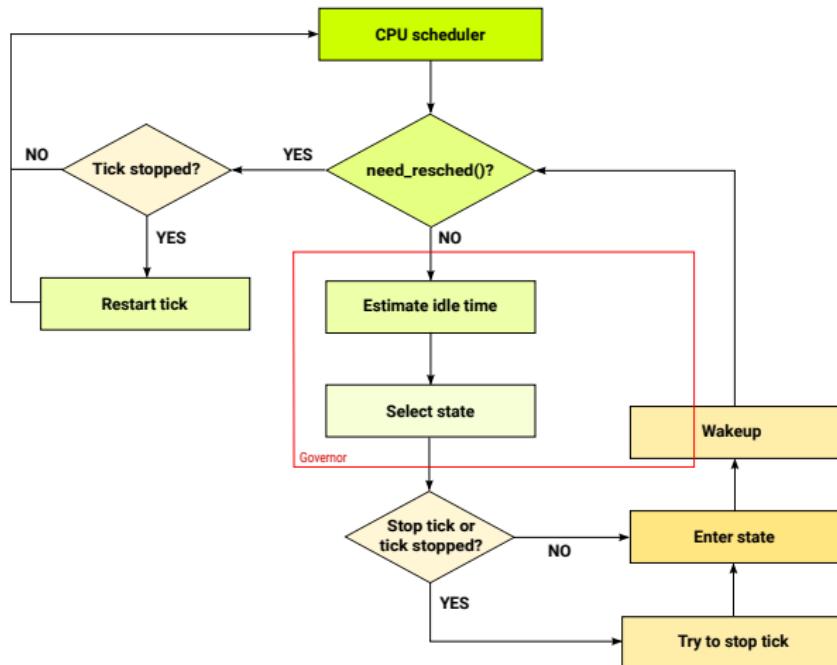


# Idleness Is an Opportunity to Save Energy



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# The Idle Loop in Linux\* (4.17 and Later)

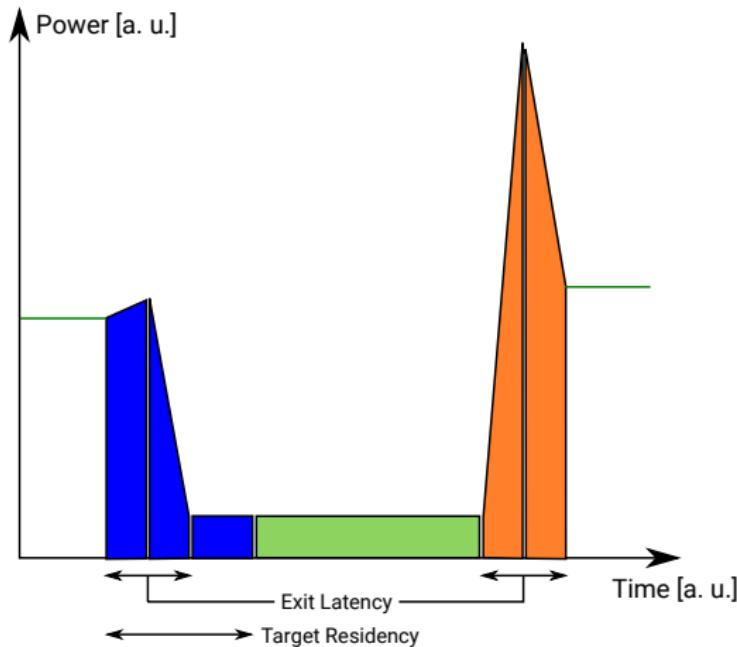


# Idle Governor and Idle Driver Need To Communicate



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# CPU Idle State Parameters



# Worst-case Numbers Are Difficult To Come By

## Worst case measurement Catch 22

In order to measure the worst case you must experience it, but you cannot know whether or not you have experienced it unless you know beforehand what it is.



# Governor Perspective



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# The Rock and The Hard Place

## The Rock

Selecting idle states that are too shallow hurts energy-efficiency.

## The Hard Place

Selecting idle states that are too deep hurts energy-efficiency and performance (through excessive latency).



# Two Categories of Wakeup Events



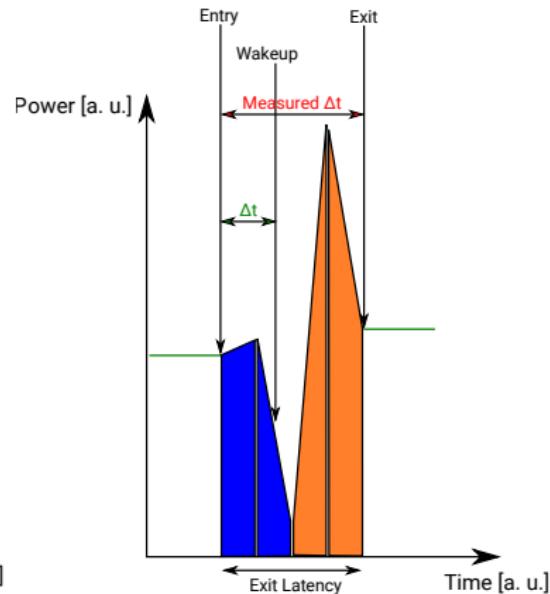
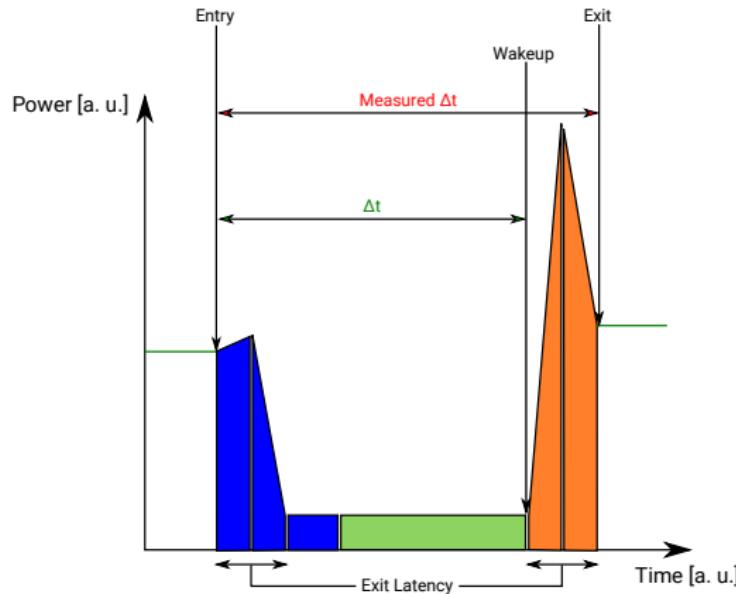
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# Measurement Issues

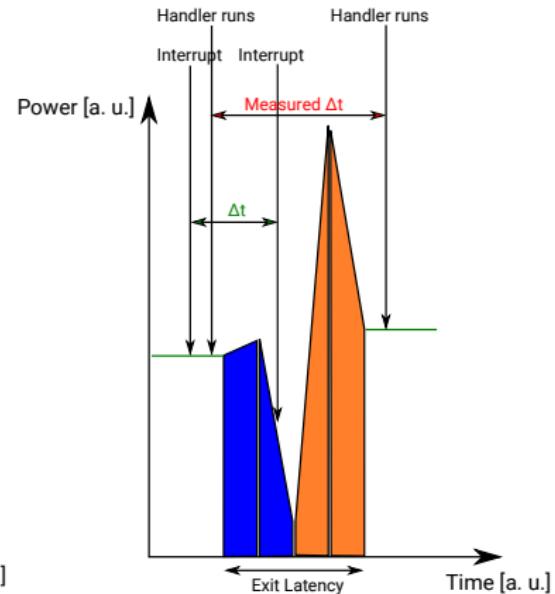
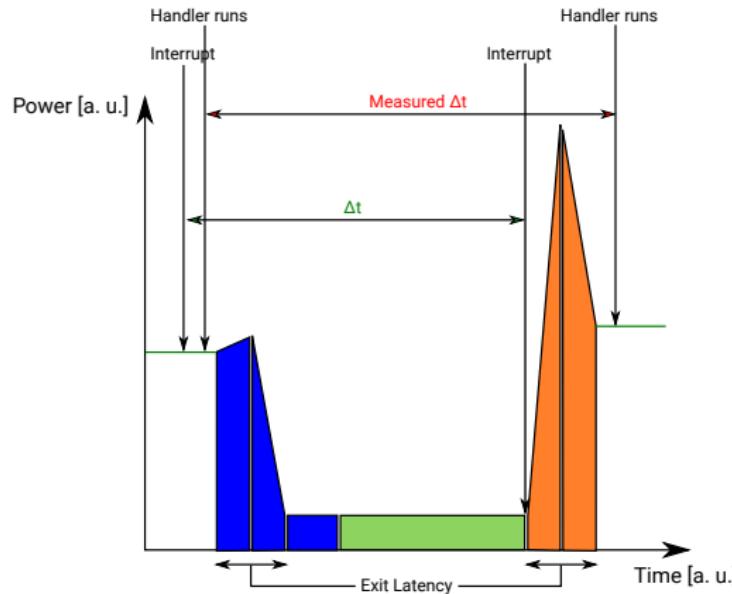


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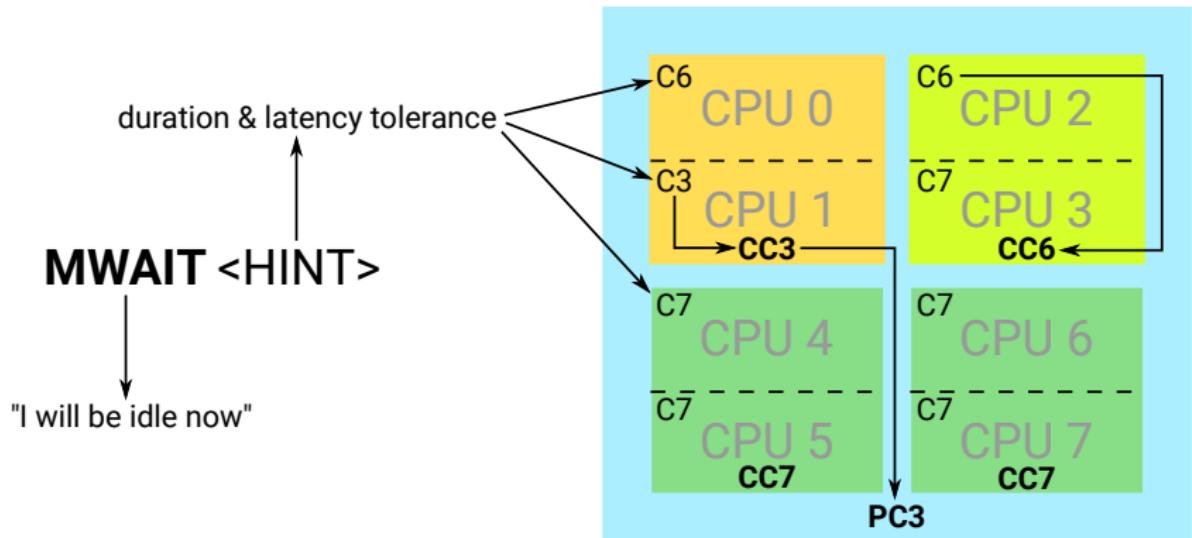
# Idle Duration Is Difficult To Measure Precisely



# Interrupt Timing Measurements May Be Affected Too



## Example: Core and Package C-states

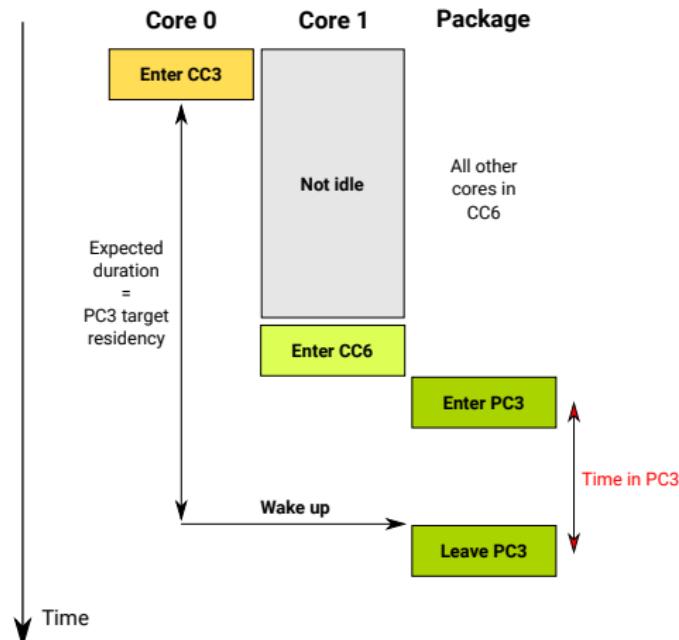


# What Target Residency To Use for a “Combo” State?

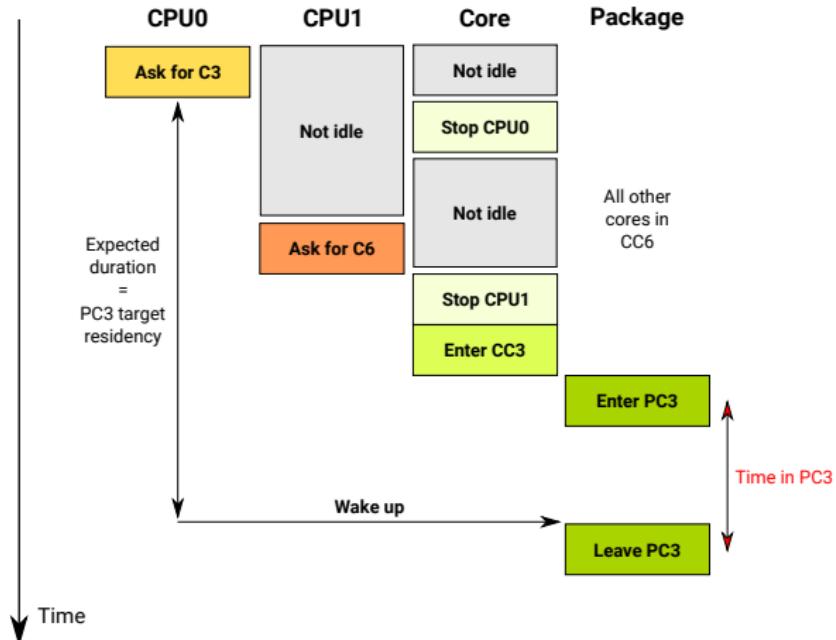


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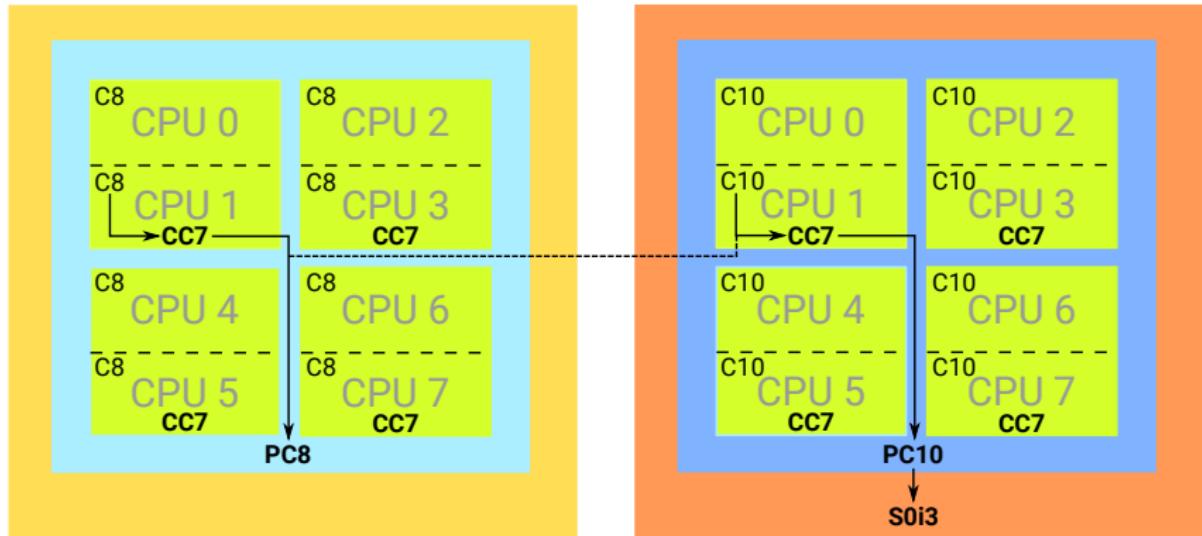
# Target Residencies May Be Missed Due to Interactions (1)



# Target Residencies May Be Missed Due to Interactions (2)



# Overlapping Hints and Missed Opportunities



# Fall-through Idle States Idea

Assume target residency (TR) of the next idle state

Selected for latency reasons only.

Results (12 runs on Dell XPS13 9360, TEO governor)

Metric	Baseline	C6 – C10: TR of C6	Δ	%
BaseMark	$301.0 \pm 6.5$	$305.9 \pm 5.6$	4.9	1.7
JetStream2 (1)	$54.5 \pm 1.7$	$55.1 \pm 1.6$	0.6	1.1
speedometer	$44.9 \pm 0.4$	$45.2 \pm 0.3$	0.3	0.7
JetStream2 (2)	$53.5 \pm 1.4$	$54.4 \pm 1.6$	0.9	1.6
Active Watt (pkg)	$13.1 \pm 0.1$	$13.1 \pm 0.2$	0.0	0.0
Idle Watt (pkg)	$0.93 \pm 0.08$	$0.88 \pm 0.07$	-0.05	-5.8

# Questions?



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# References

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