* **Test Bench Description:**

We used a generic testbench to generate random instruction with random sources, destinations, and types, in order to fully test our multi cycled MIPS.

Testbench uses randomization techniques in system Verilog , but the generated randomized function is constrained to our OP Codes and saved registers location of our MIPS Processor, in order to avoid making any undefined instructions that our processor donot support.

We also made a monitor function to give us a complete description of each randomized instruction in order to tell which instruction passes or fails within our design.

And we output both of results in two separate files, one containing the randomized instructions which are generated from random function, and the other contains the complete description of each generated instruction.

* Randomize Function:

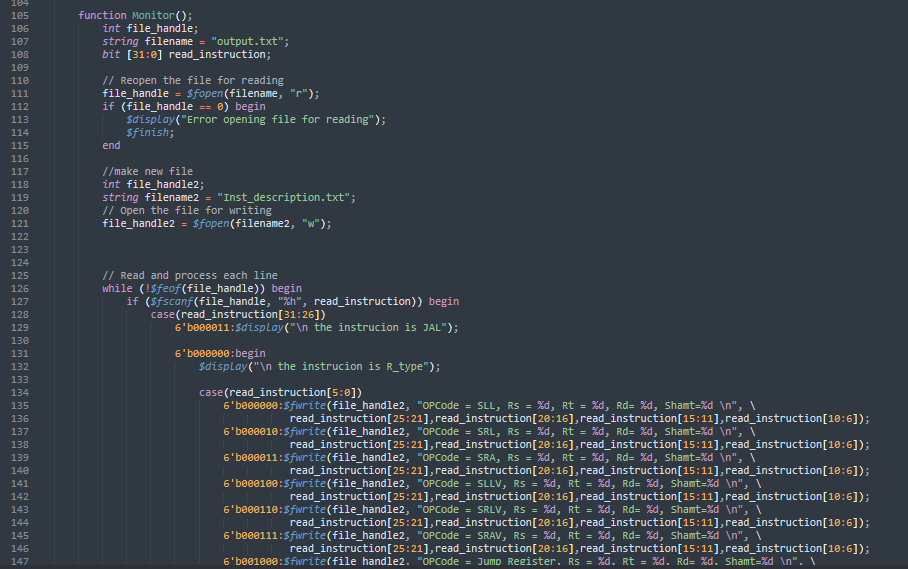
A screenshot of a computer program

Description automatically generated

A screen shot of a computer program

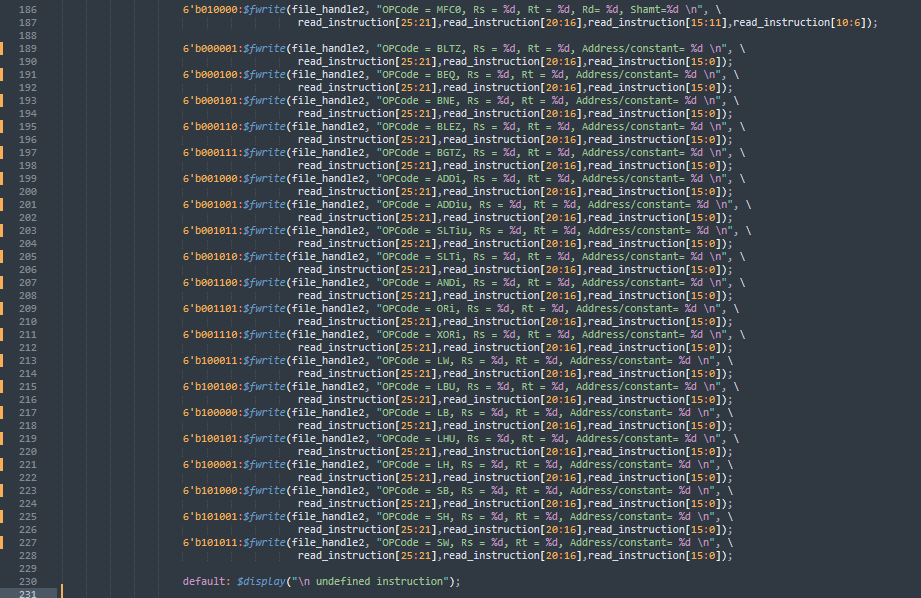
Description automatically generated

* Monitor Function:



A screen shot of a computer screen

Description automatically generated

 A blue rectangle with white text

Description automatically generated

* Testbench Function:

A screen shot of a computer code

Description automatically generated

* Sample of Random Instruction File Produced:

A screenshot of a computer

Description automatically generated

* Sample of Detailed Instruction Description File Produced:

A screen shot of a computer

Description automatically generated