Signal tap and Simulation screenshots:

1)DDS signal outputs and modulation/signal select signals

A screenshot of a computer

Description automatically generated

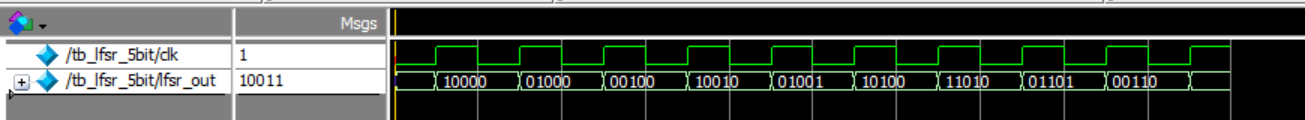
2) LSFR , signal selector , modulation selector and post synchronization outputs (SIG data\_out and MOD data\_out)

A screenshot of a computer

Description automatically generated



3)LSFR simulation



Lsfr\_out changing with each clock cycle

4)Signal selector simulation

A screenshot of a computer

Description automatically generated

Combinational logic where for each select value (“signal\_selector “ signal), we see the corresponding signal being fed to “signal\_out”, and for default value of “signal\_selector” we get sin wave as output ( 000010100000 in binary).

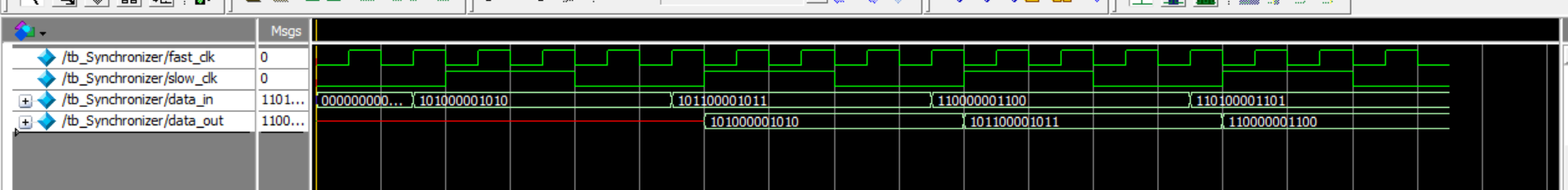
5) Modulator select simulation

A screen shot of a computer

Description automatically generated

“qpsk” signal at the top is used to trigger qpsk modulation for the combinational block, when it is set to 0 , we move to other modulations which are selected based on the “modulation\_selector” signal, in which we use “lfsr” signal to actually modulate using “sin” and “cos” signals.

6)Synchronizer simulation



The simulation quite clearly shows the data\_out being correctly synchronized with the posedge of the slower clock