Digital System Design: Complex Engineering Activity

Osama Anees Mirza, Rayyan Munir, Zafir Asad

Department of Electrical and Computer Engineering, Air University Islamabad

26 May 2024

Objective

The aim of this project is to design and implement a datapath using Verilog, a hardware description language. This includes:

- Understanding the principles behind datapath design.
- Practical implementation of a datapath.
- Exploring the interaction and flow of data within the datapath.

Introduction

We designed a 16-bit single-cycle RISC core that supports MIPS-like instructions. Our design is extendable and currently executes R-type instructions.

Instruction Formats

We implemented three types of instructions:

- **R-Type:** Register operations (e.g., add, sub, and, or).
- **I-Type:** Immediate operations (e.g., lw, sw).
- **J-Type:** Jump operations.

R-Type Instructions

Instruction	op	rs	rt	rd	function
add	000	3 bit	3 bit	3 bit	0000
sub	000	3 bit	3 bit	3 bit	0001
and	000	3 bit	3 bit	3 bit	0010
or	000	3 bit	3 bit	3 bit	0011

I-Type Instructions

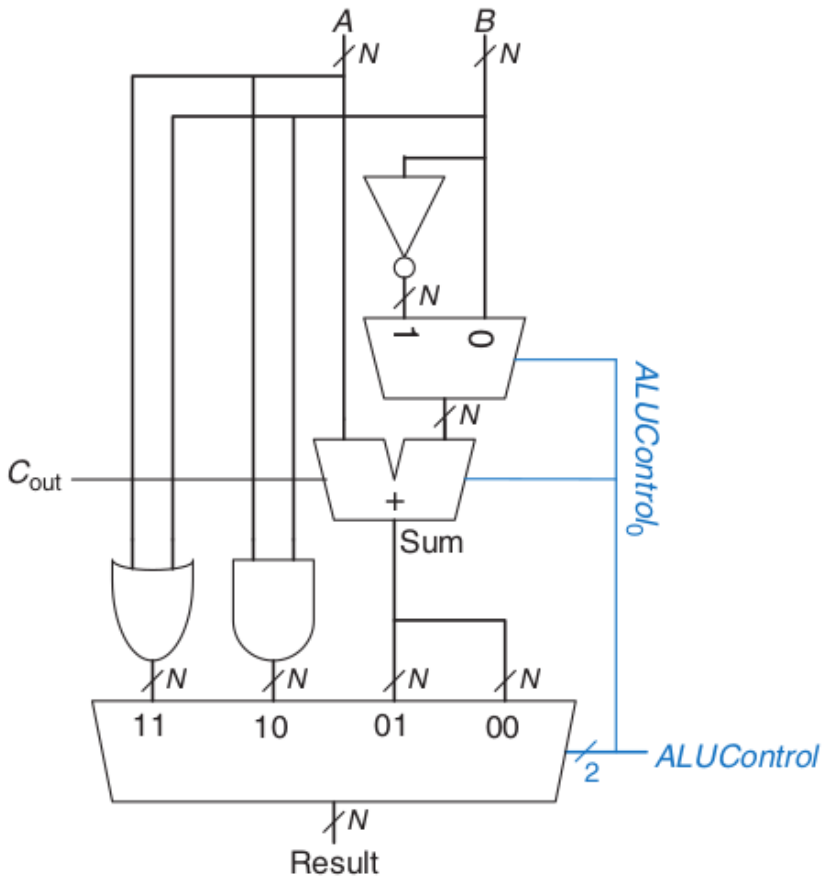
Instruction	op	rs	rt	Shift Amount/Function
lw	001	3 bit	3 bit	0000000
sw	010	3 bit	3 bit	0000000
addi	100	3 bit	3 bit	0000000

J-Type Instructions

Instruction	op	Instruction Memory Address
j	011	13 bit

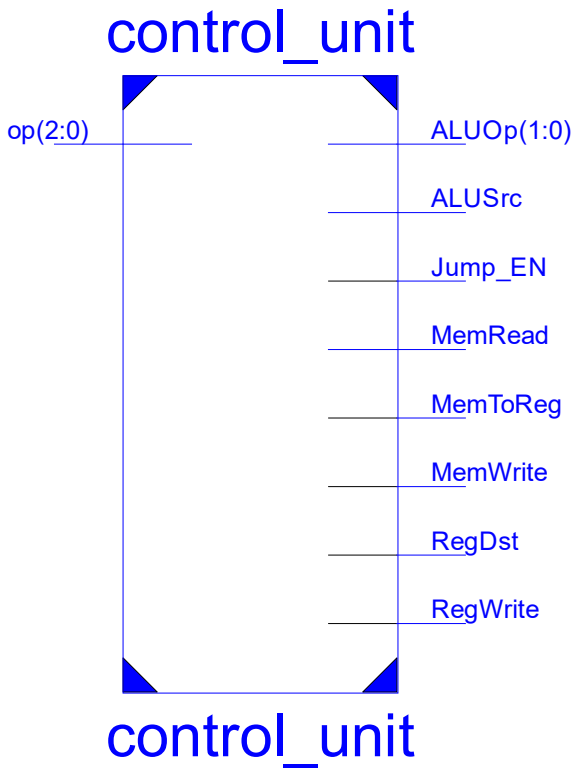
Arithmetic Logic Unit (ALU)

- Performs arithmetic and logical operations.
- Outputs a result and a zero flag.



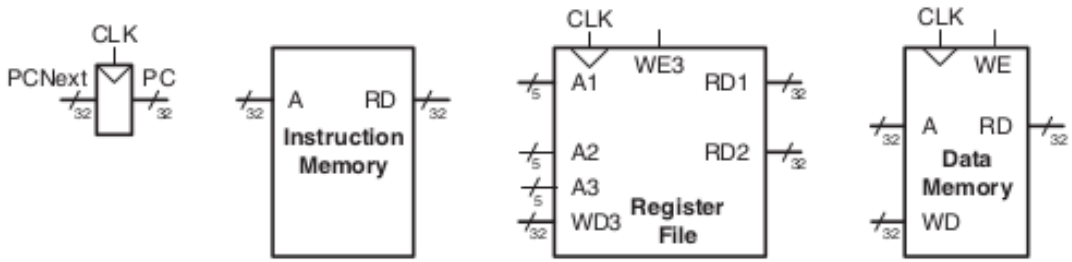
Control Unit

- Coordinates the operation of the datapath.
- Generates control signals based on instruction type.



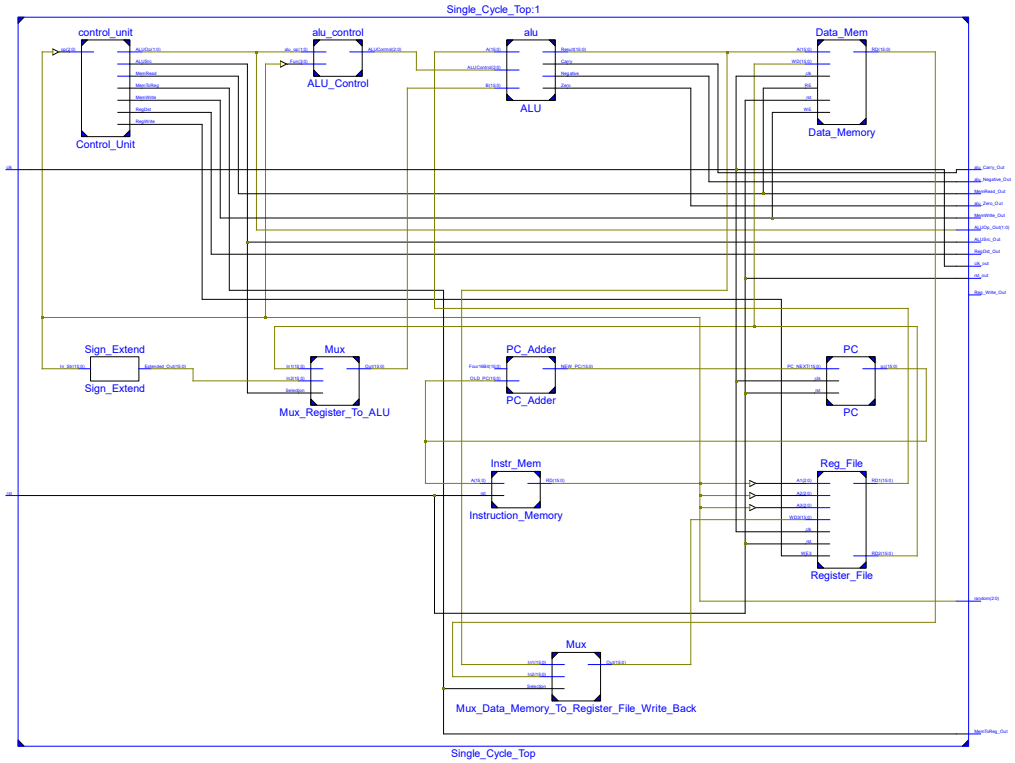
Memory Elements

- **Program Counter:** Holds the address of the next instruction.
- **Instruction Memory:** Stores program instructions.
- **Register File:** Stores general-purpose registers.
- **Data Memory:** Stores data during program execution.



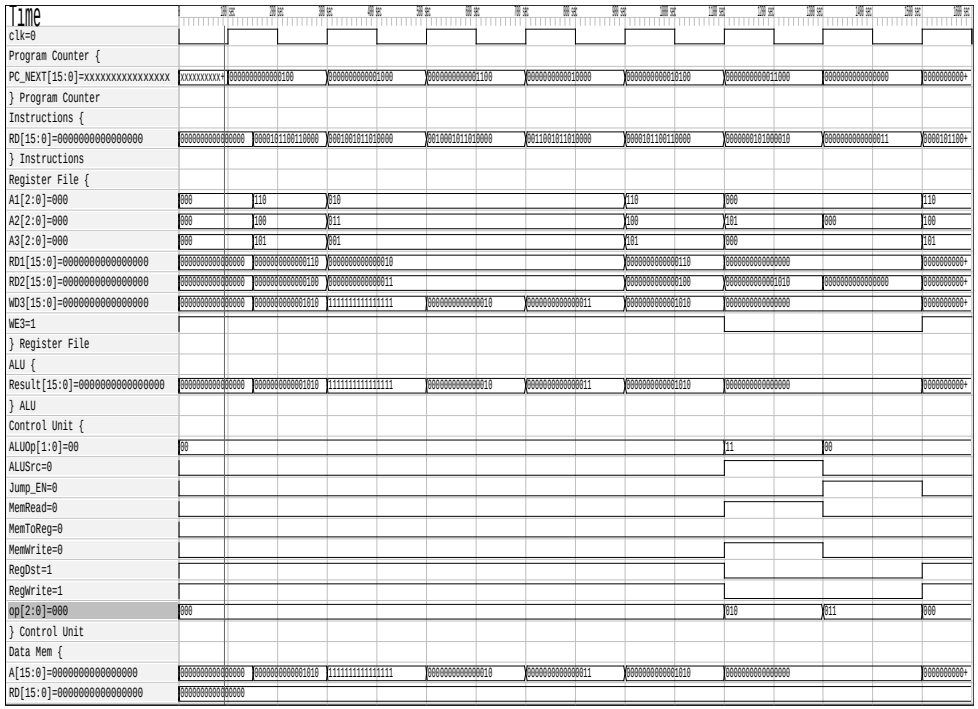
Datapath Implementation

- Combination of ALU, Control Unit, and Memory Elements.
- Single-cycle MIPS implementation.

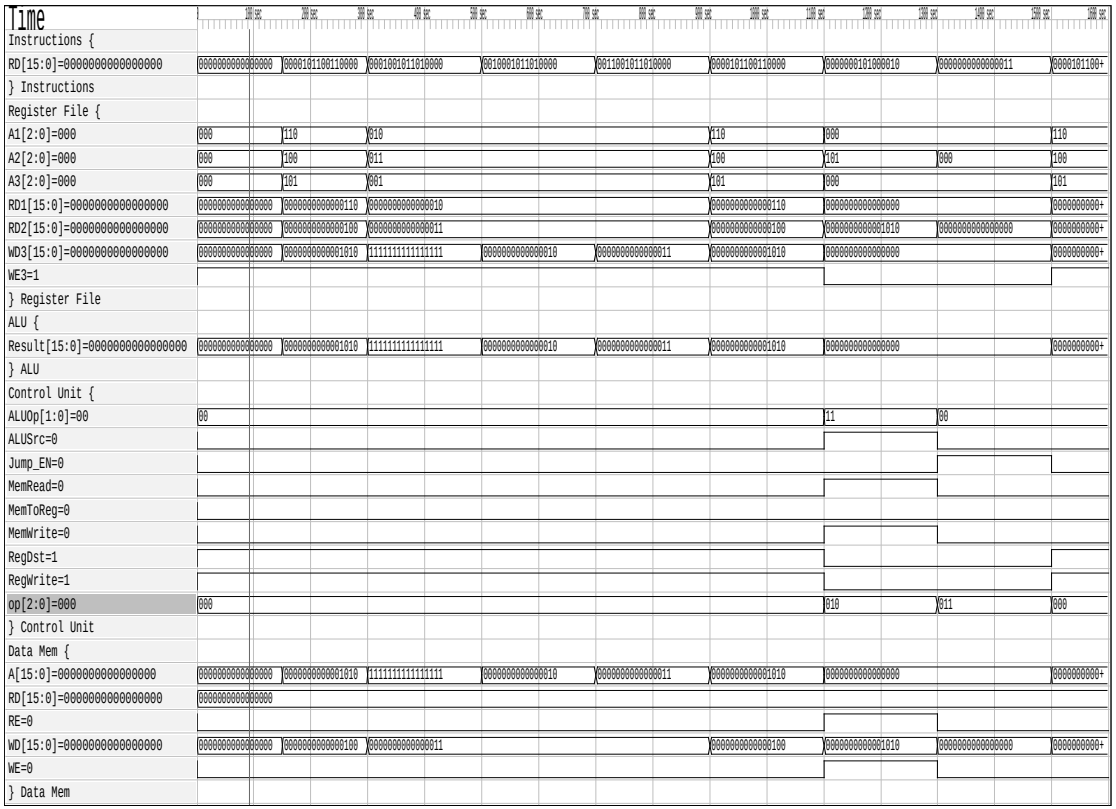


Testing and Results

- Verified functionality using Verilog test benches.
- Observed output waveforms confirm correct operation.



Testing and Results



Advantages of RISC-V

RISC-V offers several advantages:

- **Open Standard:** RISC-V is an open standard, allowing for widespread adoption and innovation.
- **Modularity:** The instruction set architecture is modular, enabling customized extensions.
- **Simplicity:** The design is simple and efficient, which can lead to better performance and lower power consumption.
- **Scalability:** RISC-V can be scaled for various applications, from small embedded systems to large supercomputers.
- **Community Support:** Strong community support and extensive documentation facilitate development and troubleshooting.

Disadvantages of RISC-V

RISC-V also has some disadvantages:

- **Maturity:** Compared to established architectures like x86 and ARM, RISC-V is relatively new and less mature.
- **Ecosystem:** The ecosystem, including tools and libraries, is still growing and may not be as extensive as more established architectures.
- **Adoption:** Industry adoption is still in progress, which may limit immediate opportunities for some applications.

Conclusion

This project provided practical experience in designing and implementing a CPU datapath using Verilog. The understanding gained from this project is essential for tackling more advanced topics in computer engineering.