Digital System Design: Complex Engineering Activity

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Objective

The aim of this project is to design and implement a datapath using Verilog, a hardware description language. This includes:

- Understanding the principles behind datapath design.
- Practical implementation of a datapath.
- Exploring the interaction and flow of data within the datapath.

Introduction

We designed a 16-bit single-cycle RISC core that supports MIPS-like instructions. Our design is extendable and currently executes R-type instructions.

Instruction Formats

We implemented three types of instructions:

- **R-Type:** Register operations (e.g., add, sub, and, or).
- I-Type: Immediate operations (e.g., lw, sw).
- **J-Type:** Jump operations.

R-Type Instructions

Instruction	ор	rs	rt	rd	function			
add	000	3 bit	3 bit	3 bit	0000			
sub	000	3 bit	3 bit	3 bit	0001			
and	000	3 bit	3 bit	3 bit	0010			
or	000	3 bit	3 bit	3 bit	0011			

I-Type Instructions

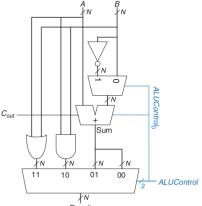
Instruction	ор	rs	rt	Shift Amount/Function
lw	001	3 bit	3 bit	0000000
SW	010	3 bit	3 bit	0000000
addi	100	3 bit	3 bit	0000000

J-Type Instructions

Instruc	tion	ор	Instruction Memory Address
j		011	13 bit

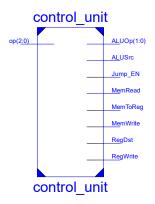
Arithmetic Logic Unit (ALU)

- Performs arithmetic and logical operations.
- Outputs a result and a zero flag.



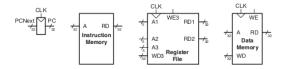
Control Unit

- Coordinates the operation of the datapath.
- Generates control signals based on instruction type.



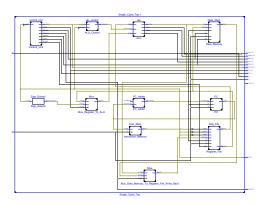
Memory Elements

- **Program Counter:** Holds the address of the next instruction.
- Instruction Memory: Stores program instructions.
- Register File: Stores general-purpose registers.
- **Data Memory:** Stores data during program execution.

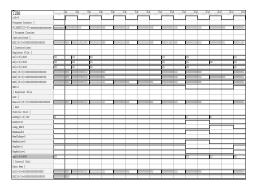


Datapath Implementation

- Combination of ALU, Control Unit, and Memory Elements.
- Single-cycle MIPS implementation.



- Verified functionality using Verilog test benches.
- Observed output waveforms confirm correct operation.



Testing and Results

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A2(2:0)+000	800		200								200		311		30		200
A3(2:0)+000	800		200		100						ŽIII.		000				311
RD1[15:0]+000000000000000000	30000000000	00000	000000	000000130	00000000000	dicco					20000000000	0130	000000000000000000000000000000000000000	(D000			0000000000
RD2[15:0]+00000000000000000		500		00000100		\$00					1	000		(111)		0000	
MD3[15:0]+000000000000000000		8000	nana pa	0000000	1111111111	\$111		BILLI		0011	1	E00		000			
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Register File																	
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ALU																	
Control Unit (
ALUUp(1:0]+00	8												11		0		
ALUSze=0															i		
Jump_ESI=0															_		
NenRead=0															i		
NesSchag=0																	
ManWrite-D															1		
RegDat=1			\neg														
RegWrite=1	ì		-			_			_			_					
op(2:0)+000	300		\neg						_				111		111		000
Control Unit																	
Data Men (
A[15:0]+00000000000000000	3000000000	0000	00000000	00000000	2111111111	\$111	0000000000	0000	10000000000	0011	2000000000	E010	00000000000	0000			0000000000
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0-29		П	\neg												1		
MD(15:0]+00000000000000000	200000000	0000	00000	00000000		800						0000		0001	200000000	0000	000000000
WE-0															1		
Data Men																	

Advantages of RISC-V

RISC-V offers several advantages:

- Open Standard: RISC-V is an open standard, allowing for widespread adoption and innovation.
- Modularity: The instruction set architecture is modular, enabling customized extensions.
- **Simplicity:** The design is simple and efficient, which can lead to better performance and lower power consumption.
- Scalability: RISC-V can be scaled for various applications, from small embedded systems to large supercomputers.
- Community Support: Strong community support and extensive documentation facilitate development and troubleshooting.

Disadvantages of RISC-V

RISC-V also has some disadvantages:

- Maturity: Compared to established architectures like x86 and ARM, RISC-V is relatively new and less mature.
- **Ecosystem:** The ecosystem, including tools and libraries, is still growing and may not be as extensive as more established architectures.
- Adoption: Industry adoption is still in progress, which may limit immediate opportunities for some applications.

Conclusion

This project provided practical experience in designing and implementing a CPU datapath using Verilog. The understanding gained from this project is essential for tackling more advanced topics in computer engineering.