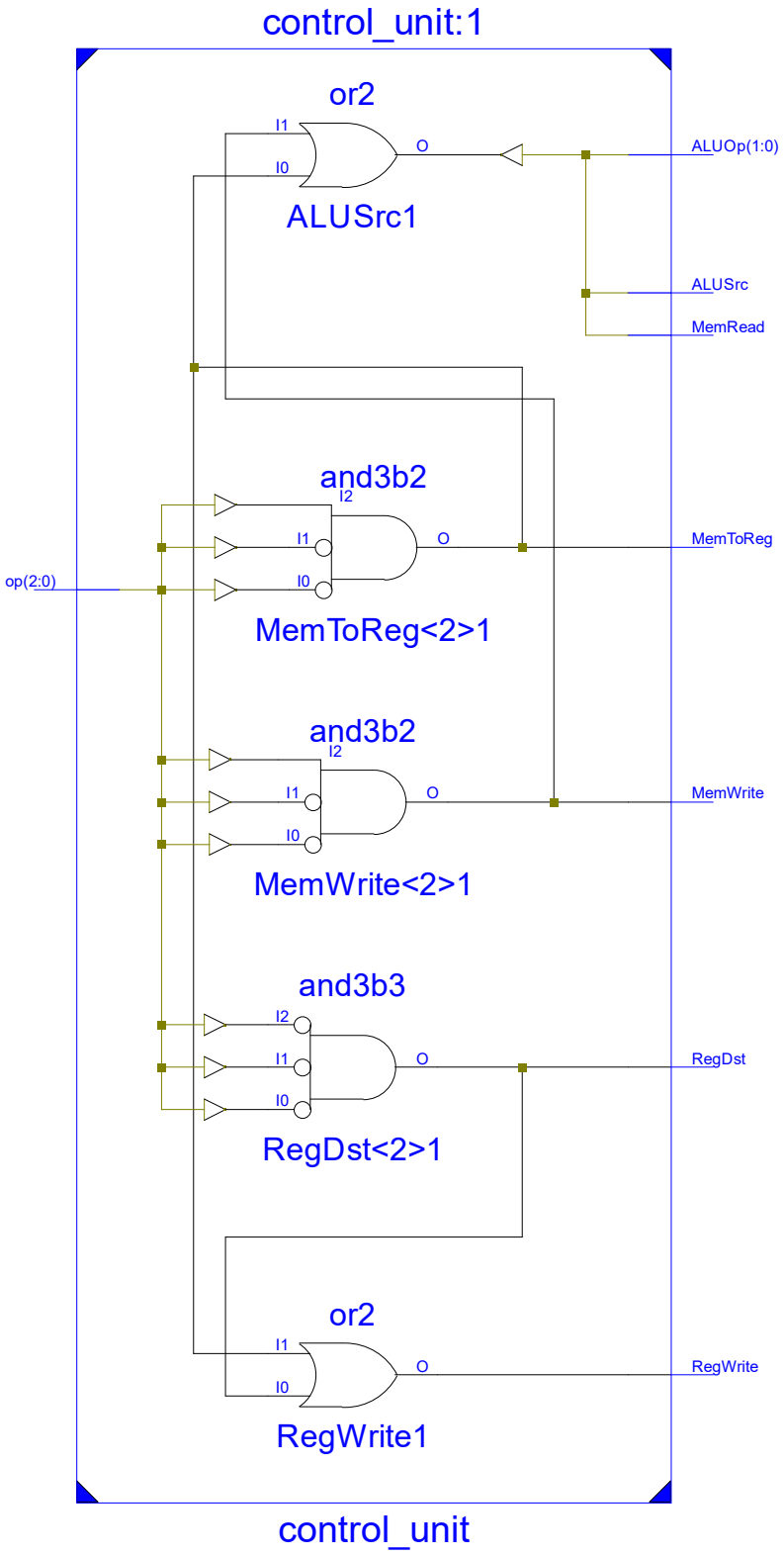
control_unit:1
or2
I1
I0
O
ALUSrc1
ALUOp(1:0)
ALUSrc
MemRead
and3b2
I2
I1
I0
O
op(2:0)
MemToReg
MemToReg<2>1
and3b2
I2
I1
I0
O
MemWrite
MemWrite<2>1
and3b3
I2
I1
I0
O
RegDst
RegDst<2>1
or2
I1
I0
O
RegWrite1
RegWrite
control_unit