Design of a General Purpose Microprocessor

(Schematic and layout diagrams of main units -Perl)

University of Southern California

Aakash Barbhaya

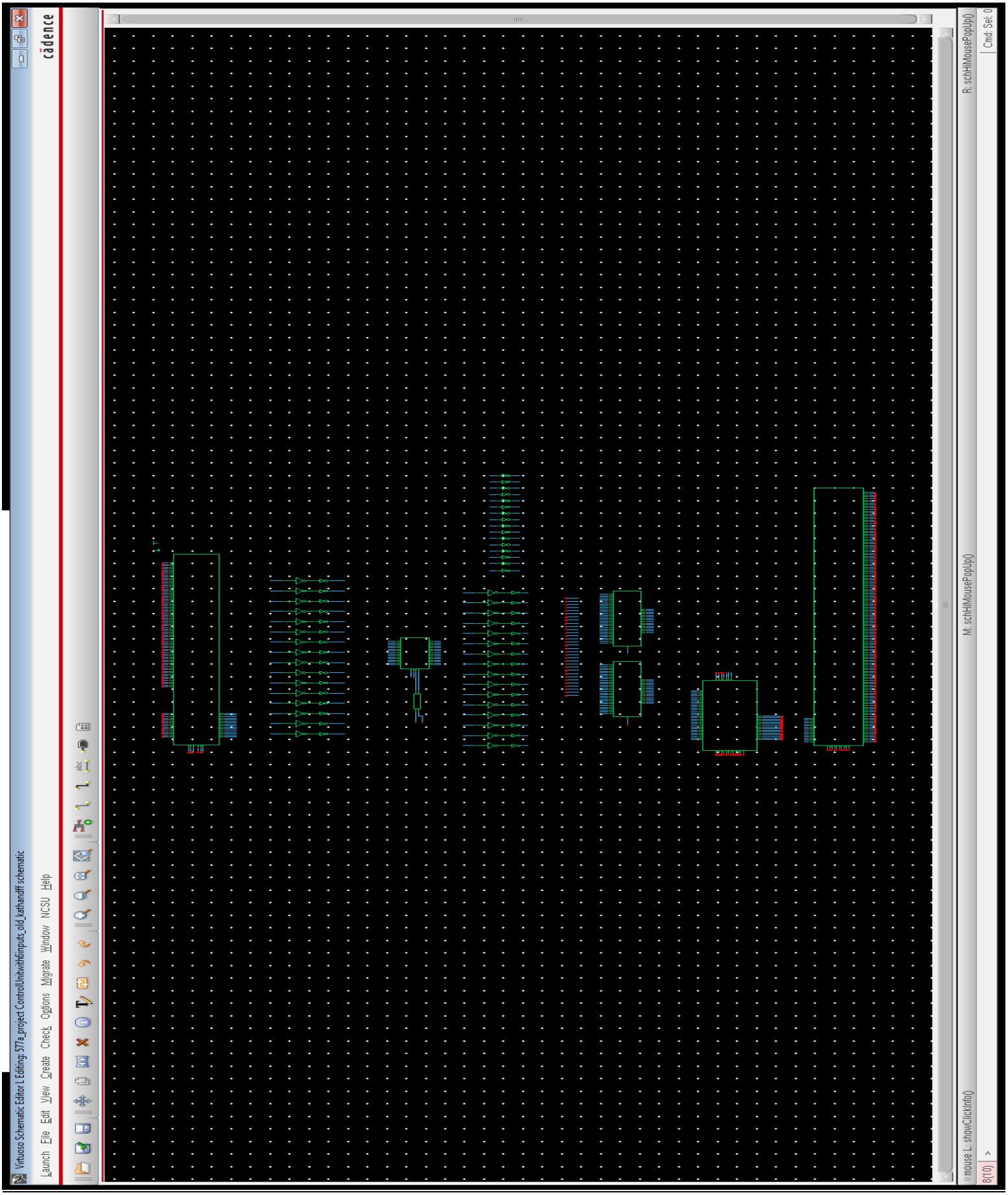
Abhishanga Upadhyay

Amruta Gadre

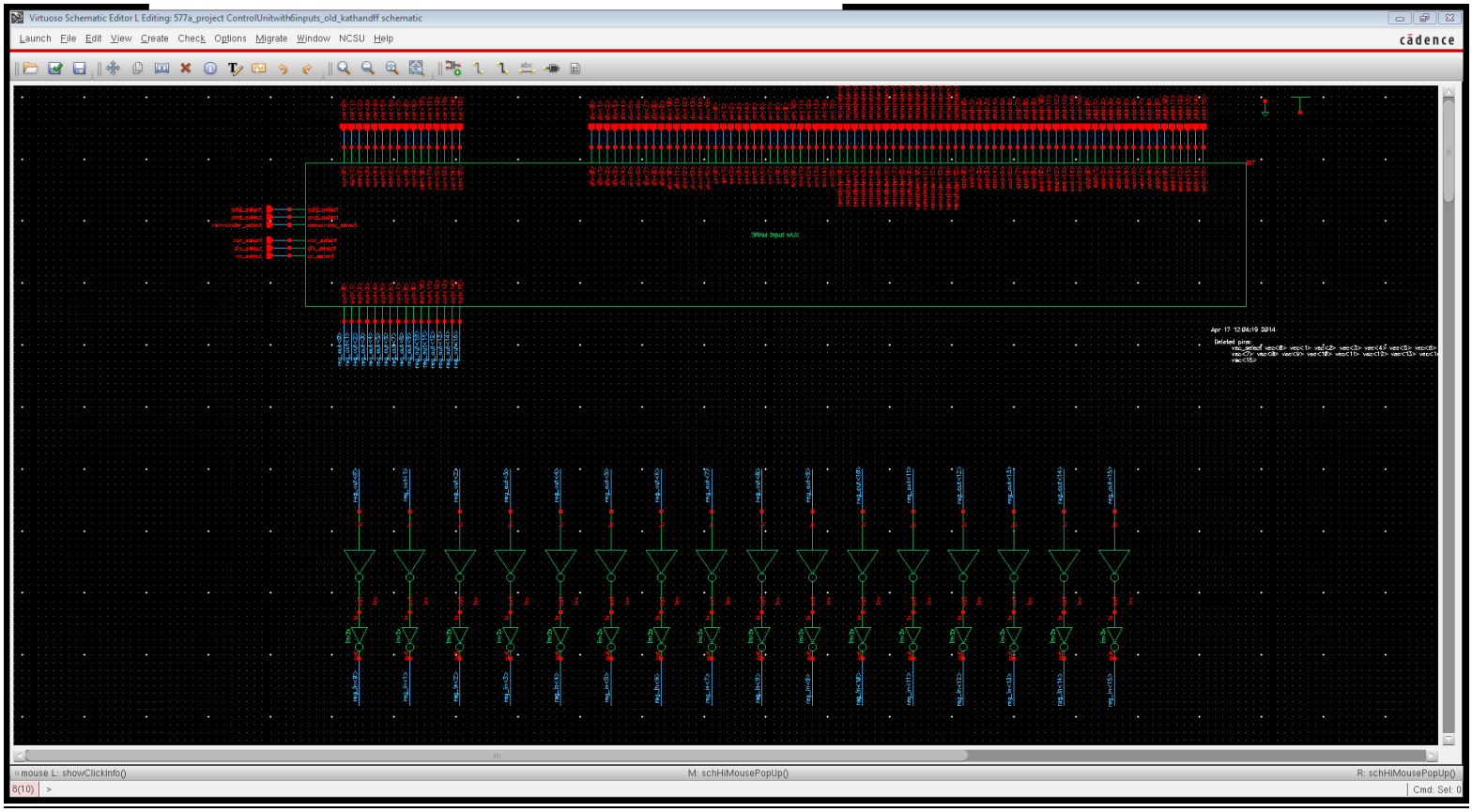
Kathan Shah

Malvika Goda Krishna

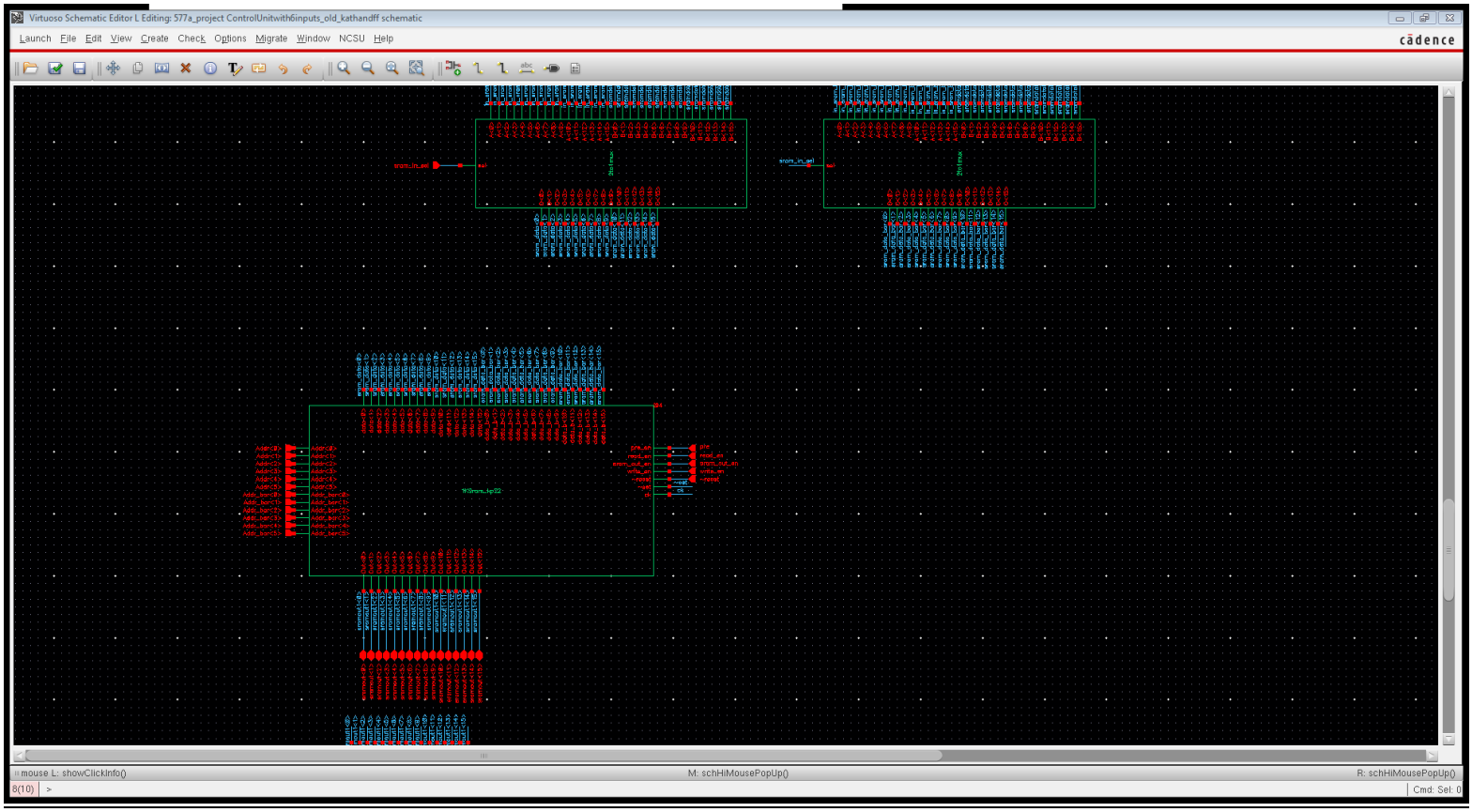
Schematic of design



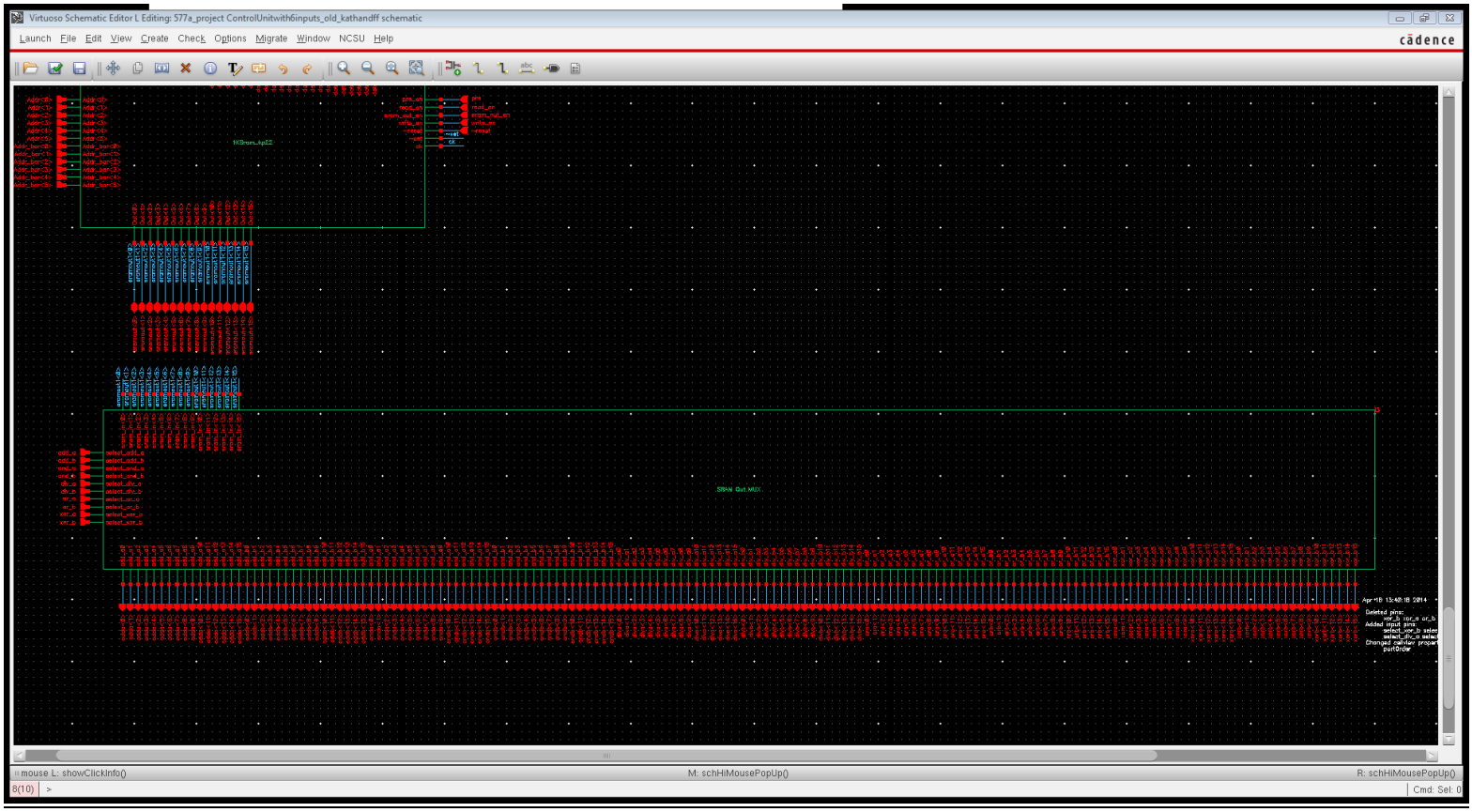
SRAM input mux



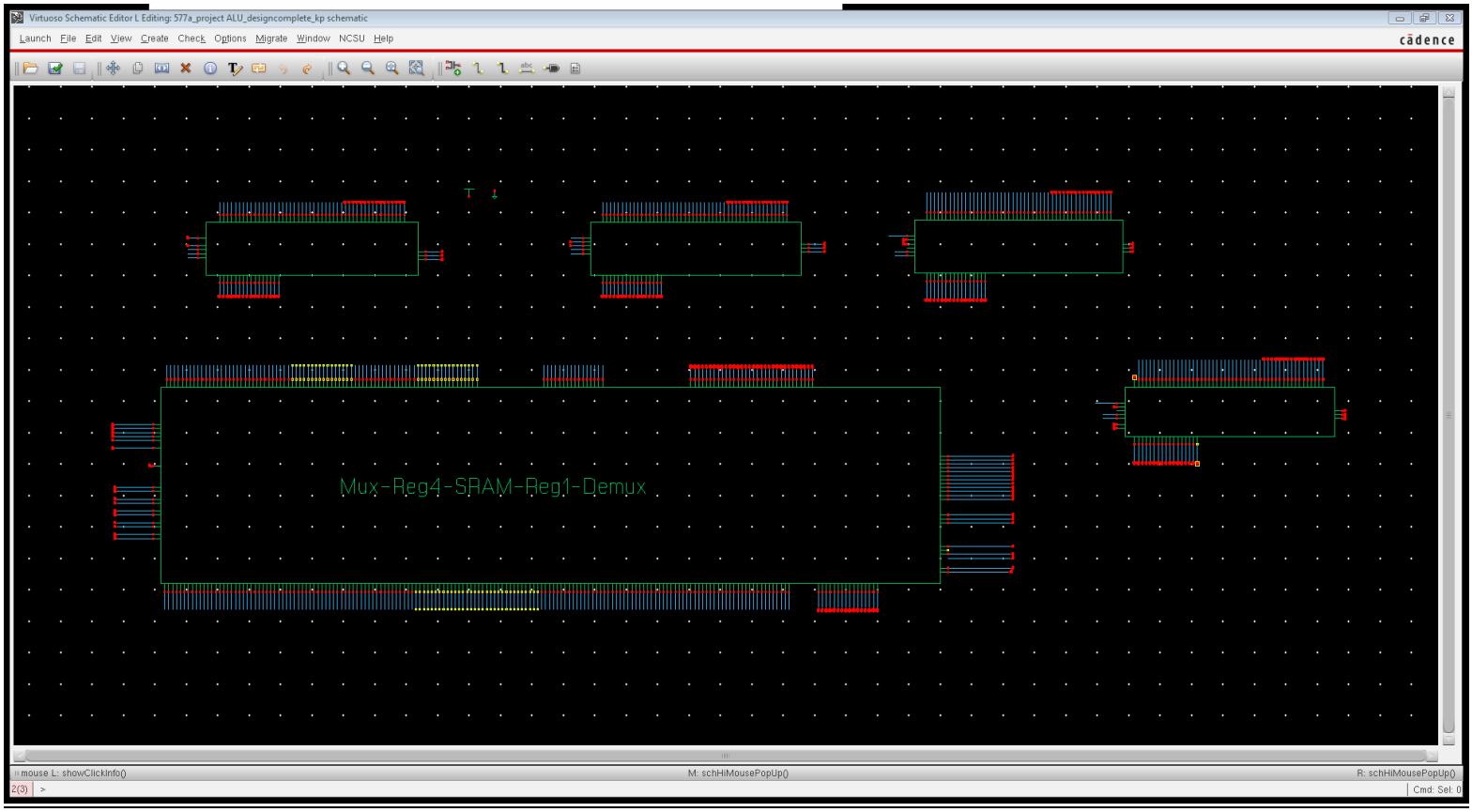
1kb SRAM with registers



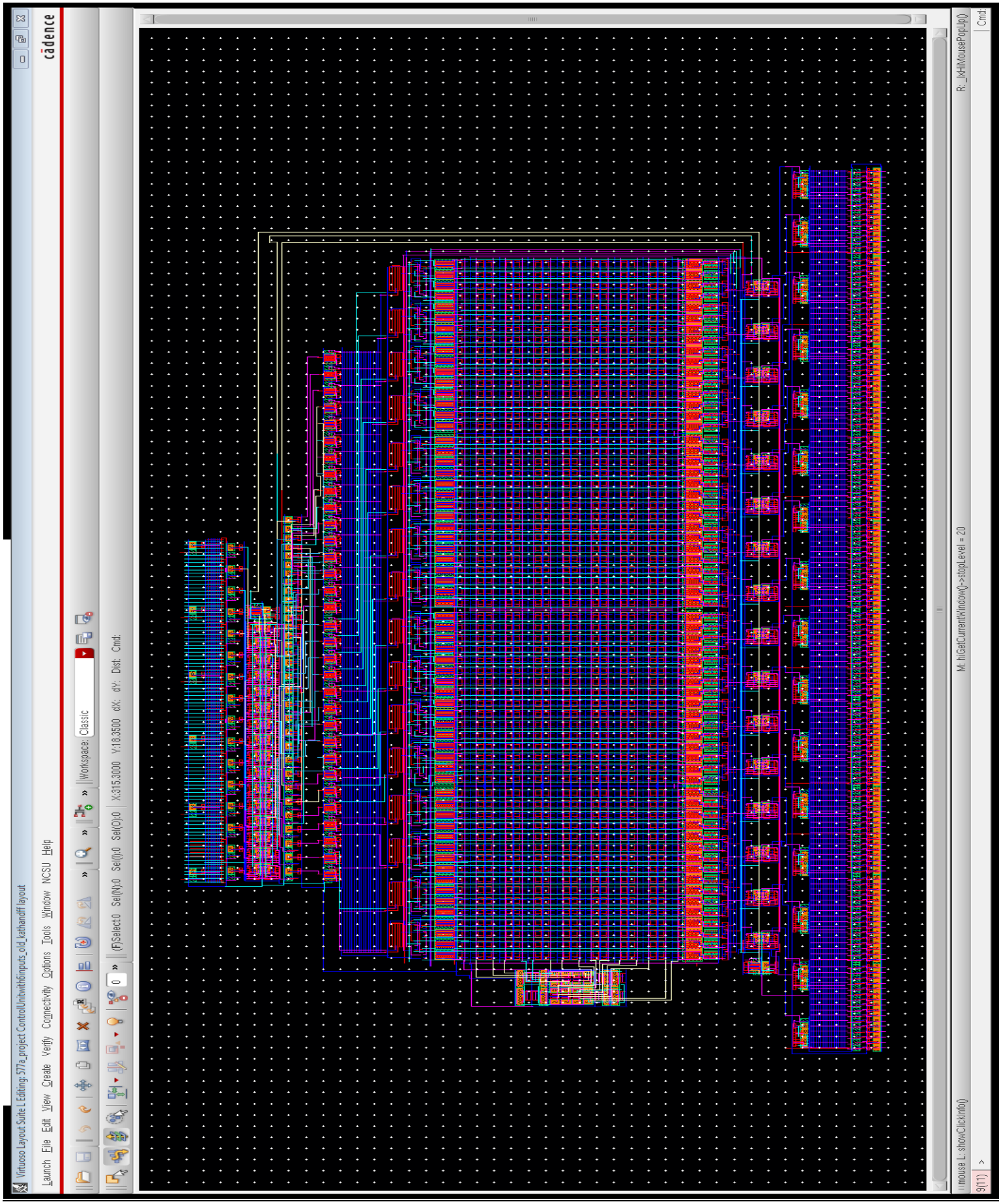
SRAM output mux



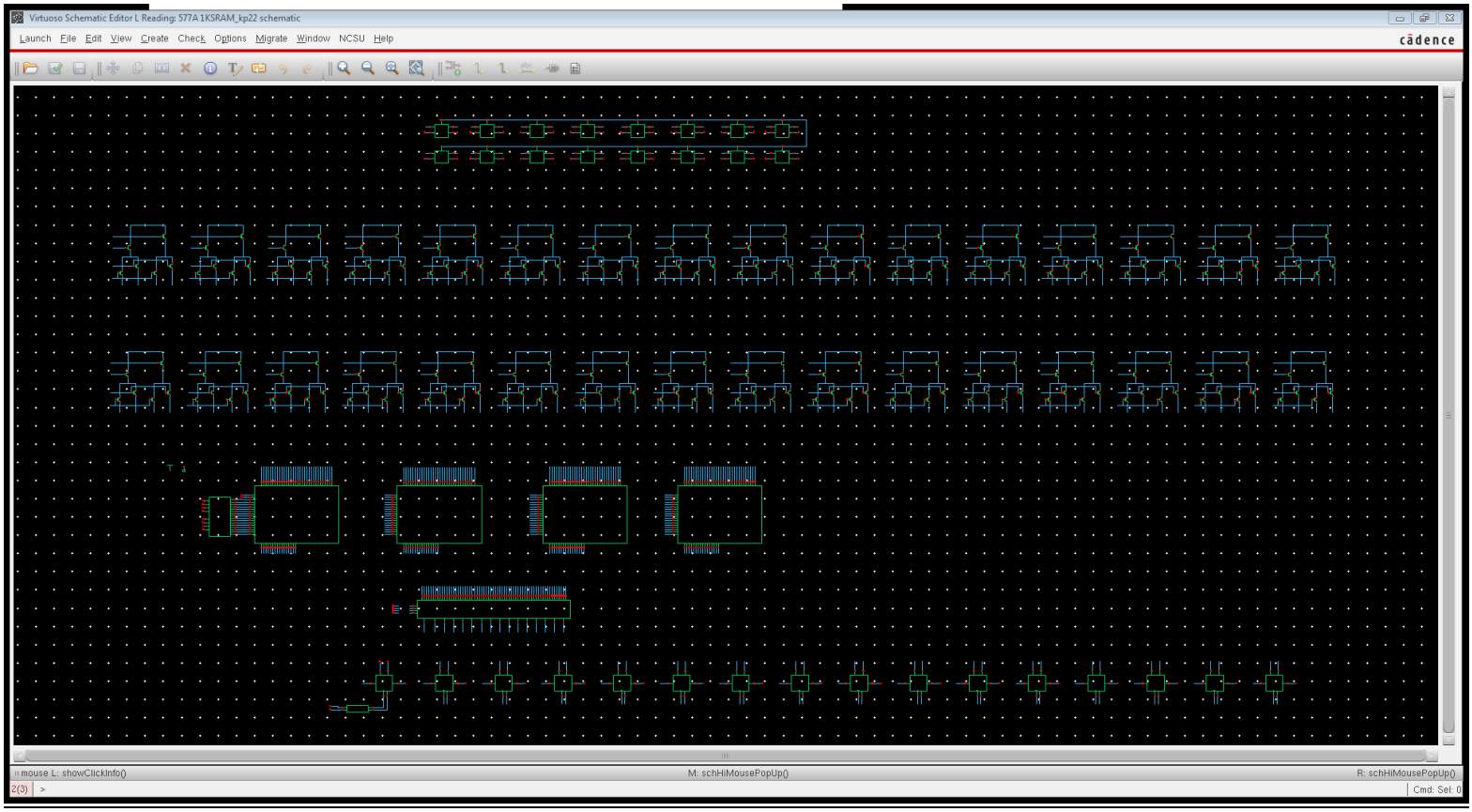
ALU

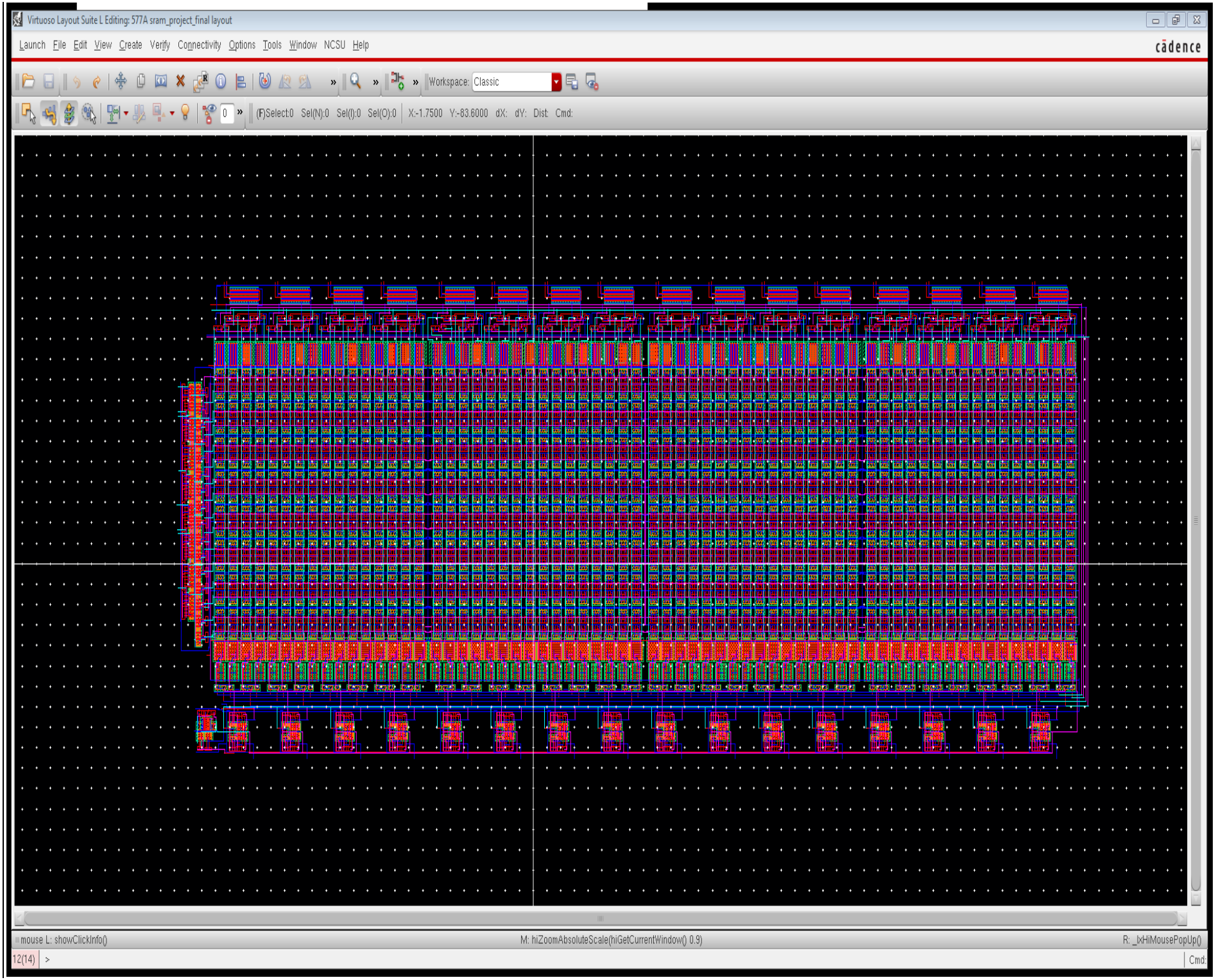

Virtuoso Schematic Editor L Editing: 577a_project ALU_designcomplete_kp schematic
Launch File Edit View Create Check Options Migrate Window NCSU Help
cadence
Mux-Reg4-SRAM-Reg1-Demux
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()
2(3)
Cmd: Sel: 0

Layout of design



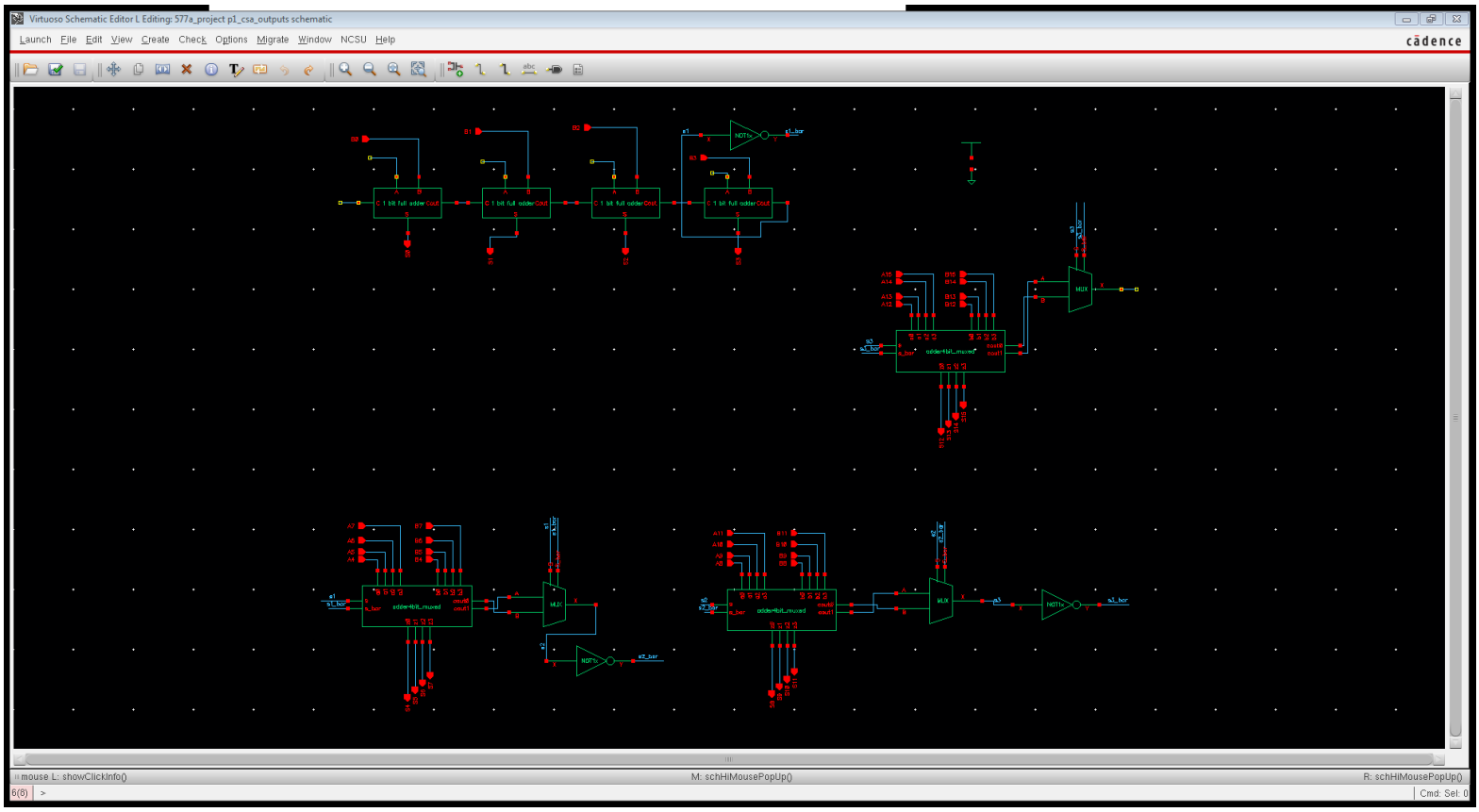
SRAM

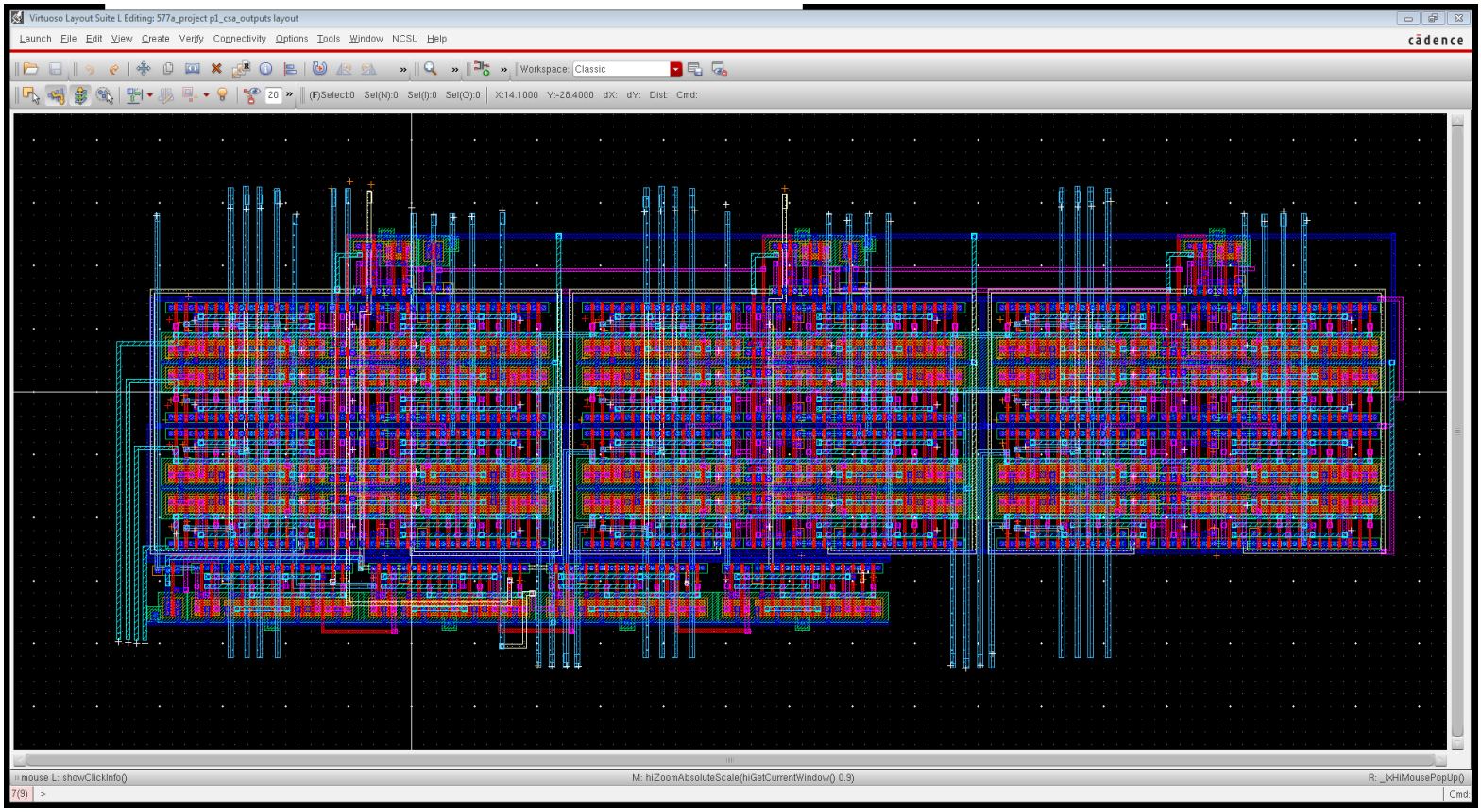

Virtuoso Schematic Editor L Reading: 577A 1KSRAM_kp22 schematic
Launch File Edit View Create Check Options Migrate Window NCSU Help
cadence
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()
2(3)
Cmd: Sel: 0


Virtuoso Layout Suite L Editing: 577A sram_project_final layout
Launch File Edit View Create Verify Connectivity Options Tools Window NCSU Help
cadence
Workspace: Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X:-1.7500 Y:-83.6000 dX: dY: Dist: Cmd:
mouse L: showClickInfo()
M: hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9)
R: _lxHiMousePopUp()
12(14)
Cmd:

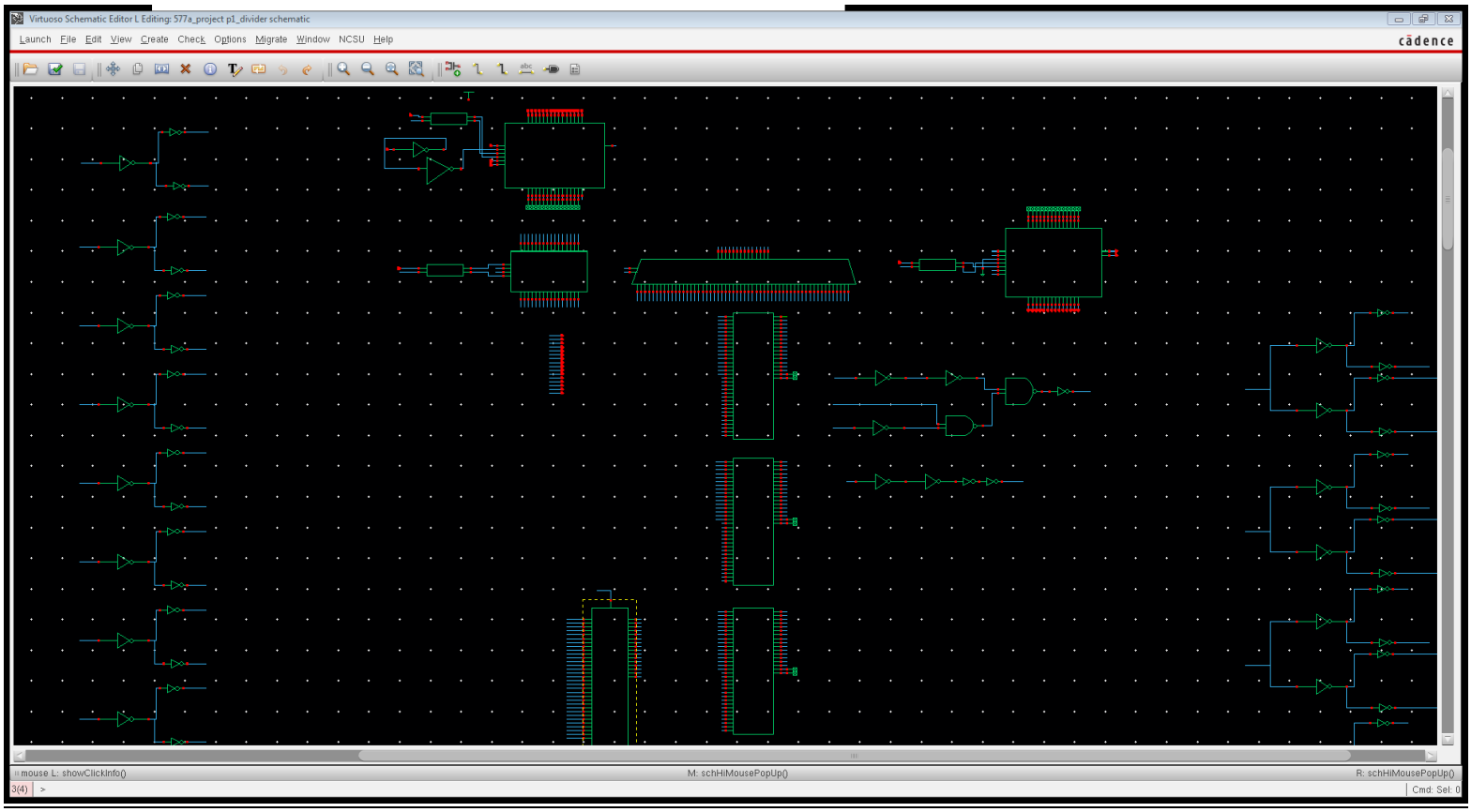
Execution units (ALU)

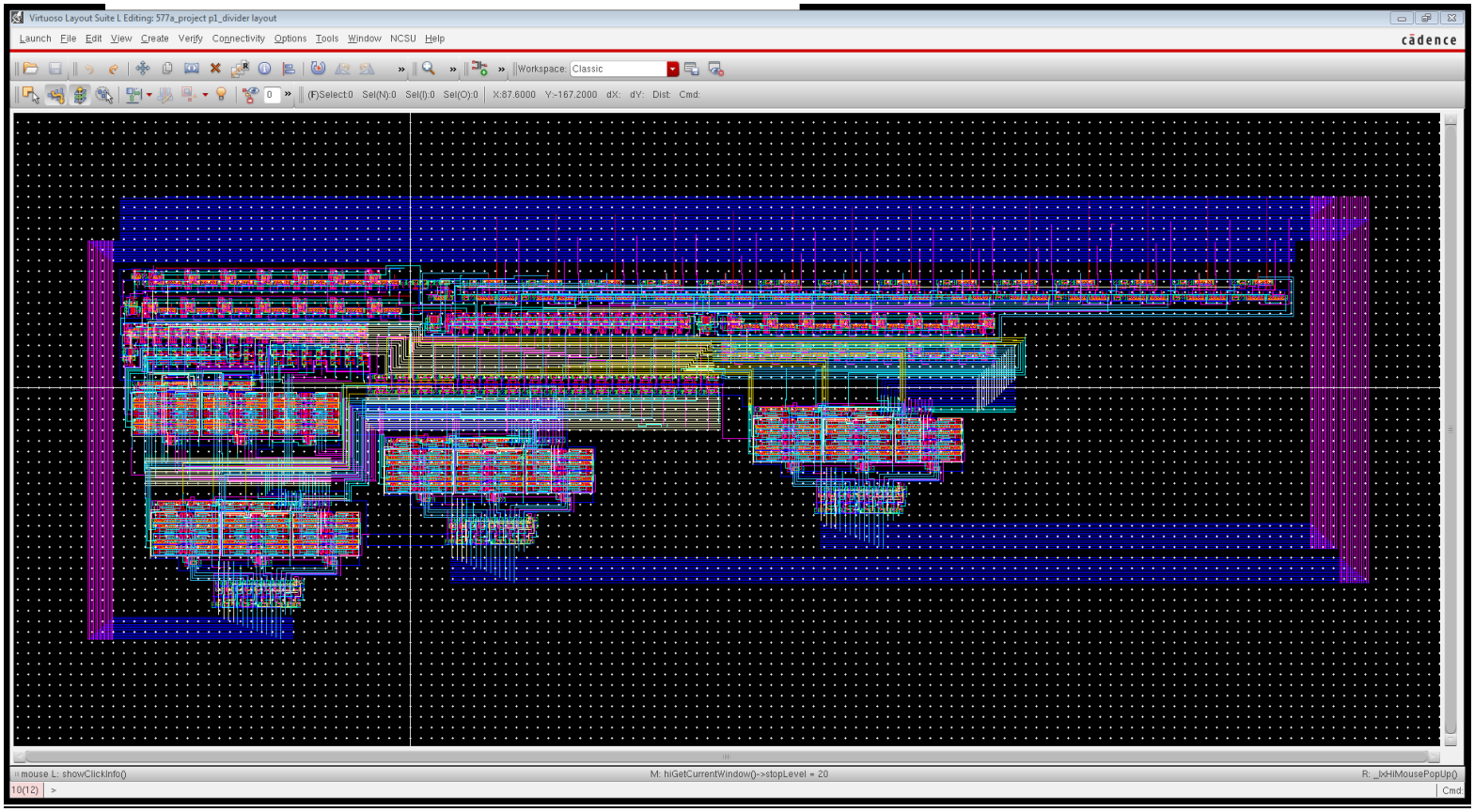
Adder



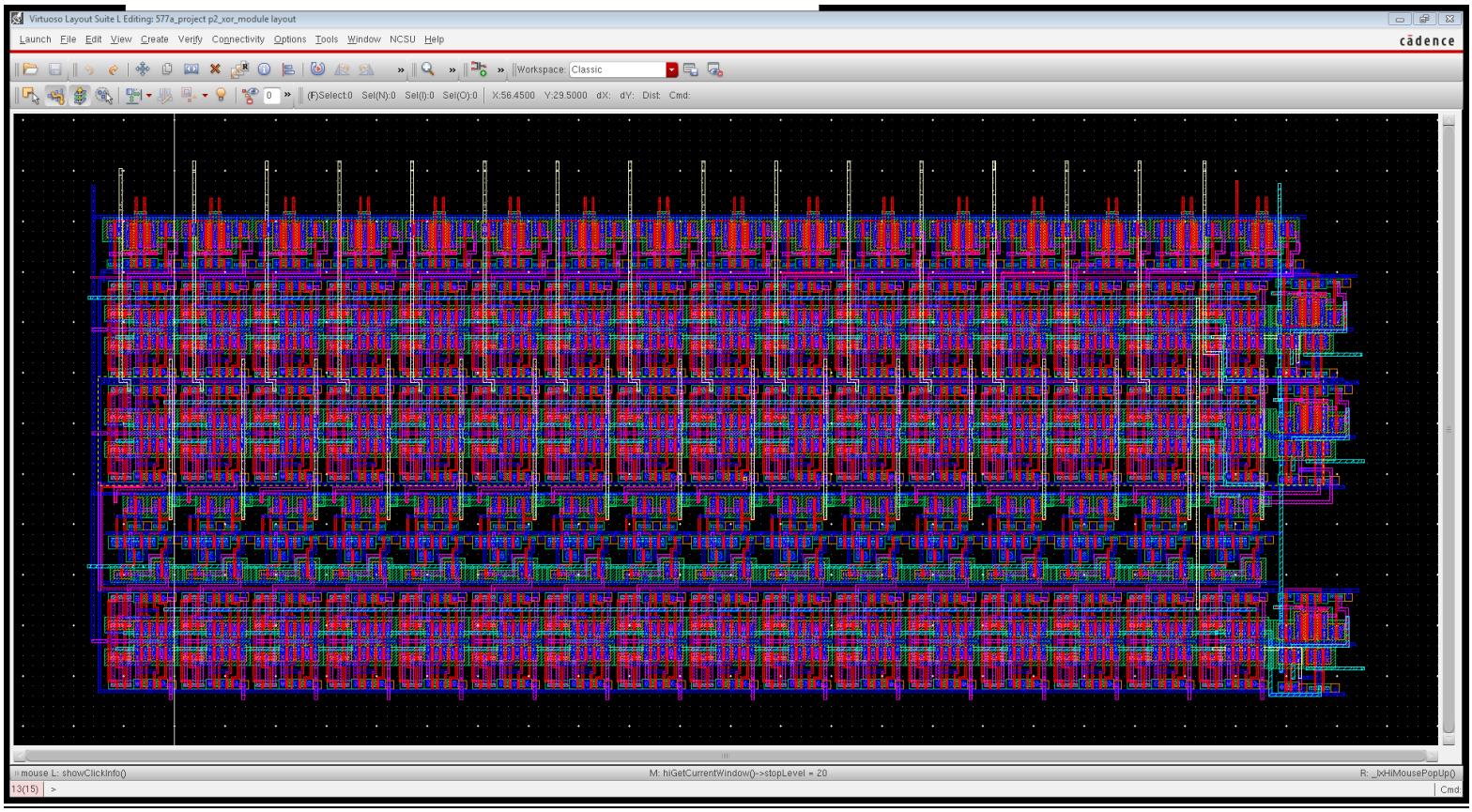


Divider (not integrated into design/separate module)

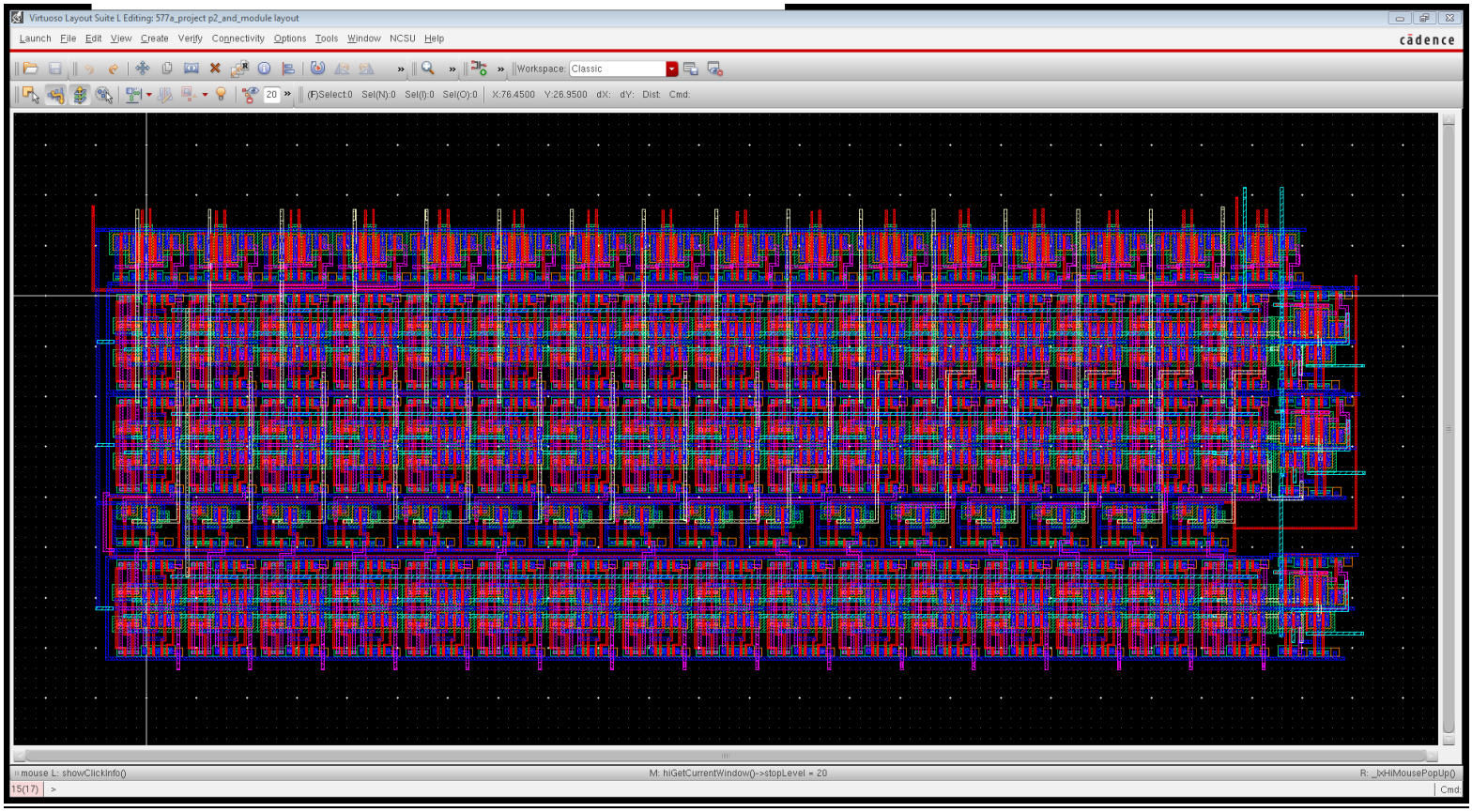



Virtuoso Layout Suite L Editing: 577a_project p1_divider layout
Launch File Edit View Create Verify Connectivity Options Tools Window NCSU Help
cadence
Workspace: Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X:87.6000 Y:-167.2000 dX: dY: Dist: Cmd:
mouse L: showClickInfo()
M: hiGetCurrentWindow()->stopLevel = 20
R: _lxHiMousePopUp()
10(12) >
Cmd:

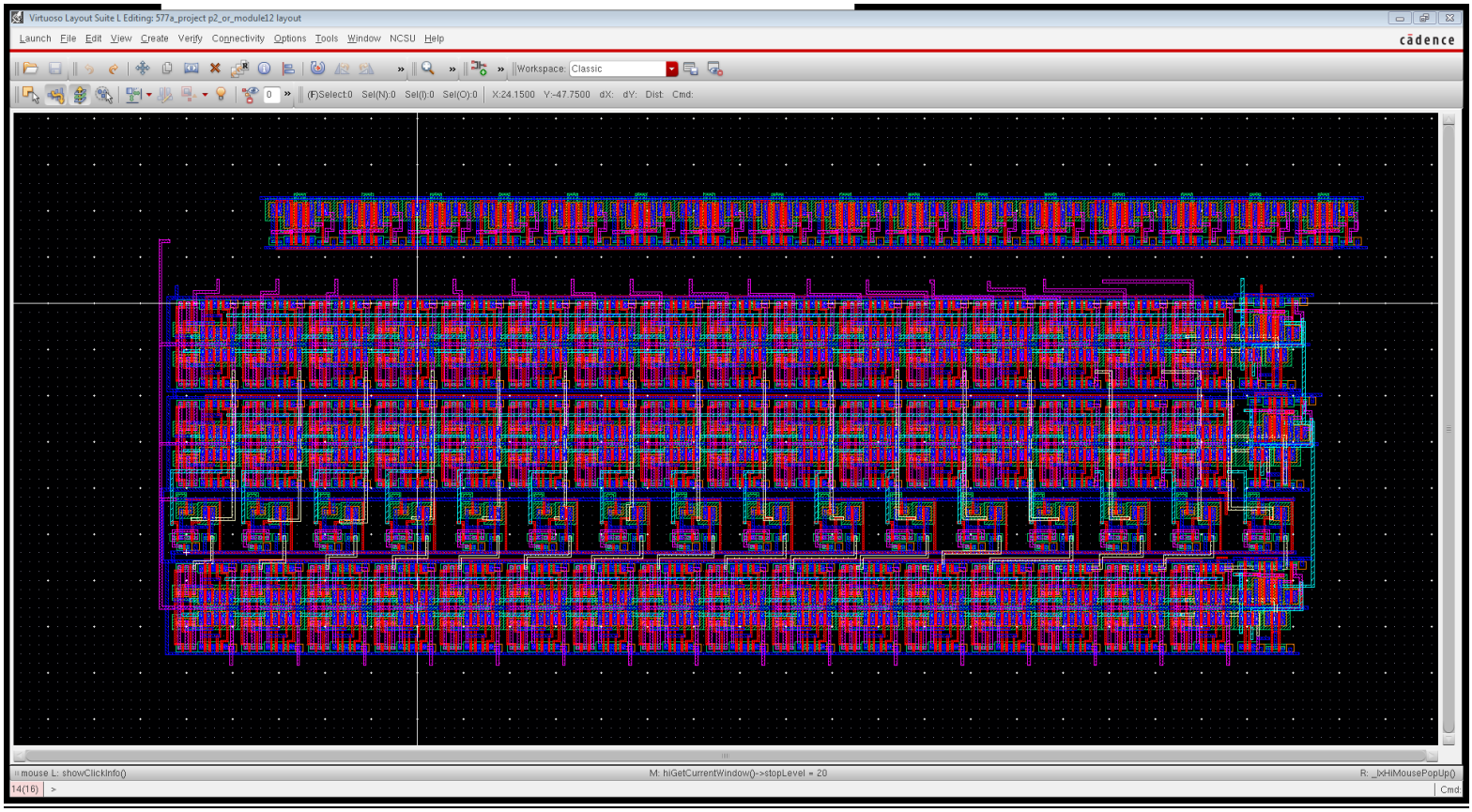
XOR dynamic


Virtuoso Layout Suite L Editing: 577a_project p2_xor_module layout
Launch File Edit View Create Verify Connectivity Options Tools Window NCSU Help
cadence
Workspace: Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X:56.4500 Y:29.5000 dX: dY: Dist: Cmd:
mouse L: showClickInfo()
M: hiGetCurrentWindow()->stopLevel = 20
R: _lxHiMousePopUp()
13(15)
Cmd:

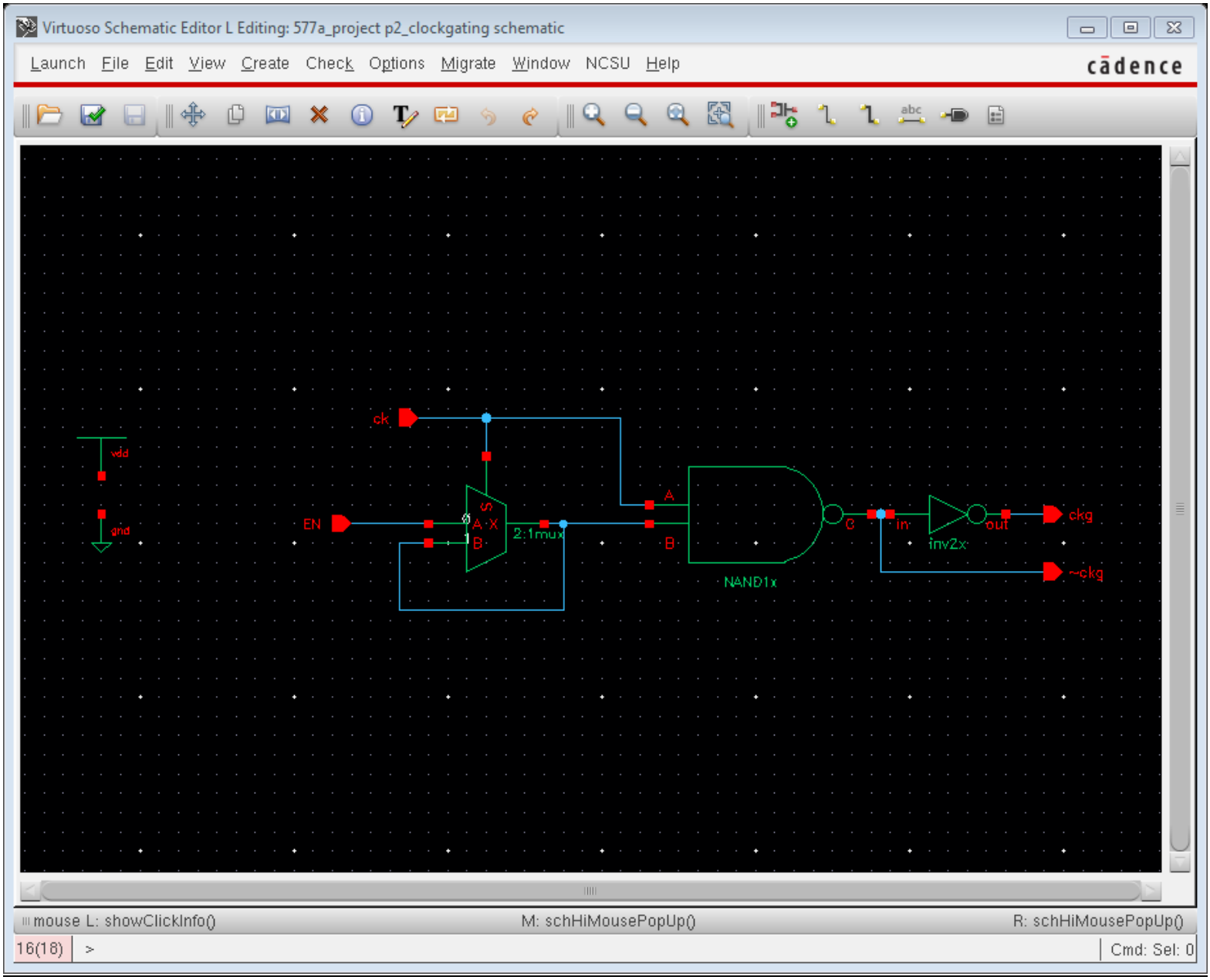
AND dynamic


Virtuoso Layout Suite L Editing: 577a_project p2_and_module layout
Launch File Edit View Create Verify Connectivity Options Tools Window NCSU Help
cadence
Workspace: Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X:76.4500 Y:26.9500 dX: dY: Dist: Cmd:
mouse L: showClickInfo()
M: hiGetCurrentWindow()->stopLevel = 20
R: _lxHiMousePopUp()
15(17)
Cmd

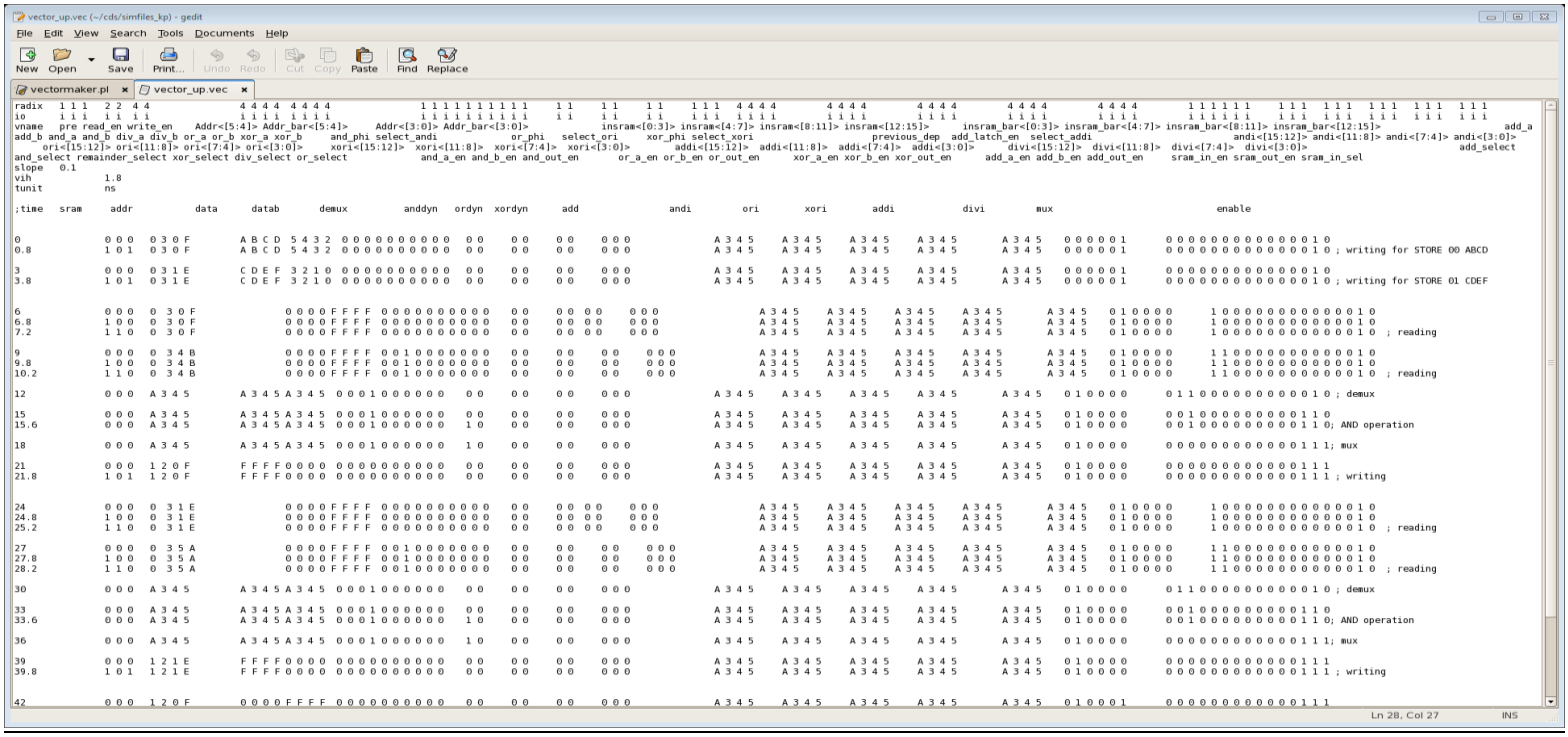
OR dynamic


Virtuoso Layout Suite L Editing: 577a_project p2_or_module12 layout
Launch File Edit View Create Verify Connectivity Options Tools Window NCSU Help
cadence
Workspace: Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X:24.1500 Y:-47.7500 dX: dY: Dist: Cmd:
mouse L: showClickInfo()
M: hiGetCurrentWindow()->stopLevel = 20
R: _lxHiMousePopUp()
14(16)
Cmd

Clock gating for power minimization



Vector file generated by perl (Snapshot)



Perl program snippet (Snapshot)