Product Brief

MM32F0140

ARM® Cortex®-M0 based 32-bit Microcontrollers

Revision: 1.0

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1 Introduction

1.1 Overview

The MM32F0140 microcontrollers are based on ARM Cortex-M0 core. These devices have a maximum clocked frequency of 72MHz, built-in 64KB Flash storage, and contain an extensive range of peripherals and I/O ports. These devices contain one 12-bit ADC, one analog comparator, one 16-bit advanced timer, one 16-bit and one 32-bit general purpose timers and three 16-bit basic timers, as well as communication interfaces including one I2C, two SPI or I2S, three UART and one FlexCAN interface.

The operating voltage of this product series is 2.0V to 5.5V, and the operating temperature range (ambient temperature) includes the industrial tier -40°C to 85°C and the extended industrial tier -40°C to 105°C. Multiple sets of power-saving modes make possible the design of low-power applications.

The target applications of this product series include:

- Industrial IoT devices
- PC accessories
- Electronic door lock
- Medical and healthcare devices
- Handheld devices
- Motor drive
- Elevator calling board
- Gaming and entertainment

This product series is available in LQFP48, LQFP32, QFN32 and TSSOP20 packages.

1.2 Key features

- Core and system
  - 32-bit ARM Cortex-M0.
  - Frequency up to 72MHz.
- Memory
  - Up to 64KB embedded Flash storage.
  - Up to 8KB SRAM.
  - Embedded Bootloader to support In-System-Programming (ISP).
- Clock, reset and power management
  - Power supply ranges from 2.0 to 5.5V.
  - Power-on and Power-down reset (POR/PDR), Brown-out reset (BOR), Programmable voltage detector (PVD).
  - 4 to 24MHz high speed crystal oscillator.
  - 8MHz factory-trimmed high speed RC oscillator.
  - Integrated PLL to generate up to 72MHz system clock and support multiple

prescaler rate to provide clock sources to bus matrix and peripherals.
  - 40KHz low speed oscillator.
  - 32.768KHz low speed crystal oscillator with bypass support.
- Low power
  - Multiple low power modes including sleep mode, stop mode, deep stop mode and standby mode.
  - Ten 16-bit backup registers that keep the value in standby mode.
- One DMA controller with 5 channels to support peripherals including timers, ADC, UART, I2C, SPI, and FlexCAN.
- Total 9 timers:
  - One 16-bit 4-channel advanced timer (TIM1), each channel providing two PWM output including one complementary output, supports hardware dead-time insertion and emergency brake when fault detected.
  - One 16-bit general purpose timer (TIM3) and one 32-bit general purpose timer (TIM2), with up to four input capture or output compare channels and can be used for infrared decode.
  - Three 16-bit basic timers (TIM14 / TIM16 / TIM17), with one input capture or output compare channel and one complementary output, support hardware dead-time insertion, emergency brake when fault detected, and integrated modulator circuit for infrared control.
  - Two watchdog timers, including one independent watchdog (IWDG) and one window watchdog (WWDG).
  - One 24-bit Systick timer.
- Up to 40 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts.
  - All I/O ports can accept input or generate output signal voltage level lower than V_{DD}.
- Up to 7 communication interfaces:
  - Three UART.
  - One I2C.
  - Two SPI (support I2S mode).
  - One FlexCAN module supports CAN 2.0B interface.
- One 12-bit Analog-to-Digital converter (ADC), support 1μs conversion duration, with up to 13 external inputs and 2 internal inputs
  - Conversion range: 0 to V_{DDA}.
  - Configurable sampling cycles and resolution.
  - On-chip temperature sensor.
  - On-chip voltage sensor.
- One high speed analog comparator
- 32-bit hardware divider
- Embedded CRC engine

- 96bit unique chip ID (UID)
- Debug mode
  - Serial-debug-interface (SWD).
- Available in LQFP48, LQFP32, QFN32 and TSSOP20 packages

2 Ordering information

2.1 Ordering table

Table 2-1 Ordering table

Part numbers		MM32F0141				MM32F0144			
Features		B1T(V)	B4Q(V)	B4P(V)	B6P(V)	C1T(V)	C4Q(V)	C4P(V)	C6P(V)
CPU frequency		72 MHz							
Flash - KB		32				64			
SRAM - KB		8				8			
Timers	16-bit GP	1				1			
	32-bit GP	1				1			
	Basic	3				3			
	Advanced	1				1			
Interfaces	UART	3				3			
	I2C	1				1			
	SPI / I2S	1 (SPI1)	2			1 (SPI1)	2		
	FlexCAN	-				1			
GPIO		16	28	26	40	16	28	26	40
12-bit ADC	Modules	1				1			
	Channels	9	13			9	13		
Comparator		1							
Supply voltage		2.0V to 5.5V							
Temperature range		-40◦C to +85◦C / -40◦C to +105◦C (V part)							
Package		TSSOP20	QFN32	LQFP32	LQFP48	TSSOP20	QFN32	LQFP32	LQFP48

2.2 Marking information

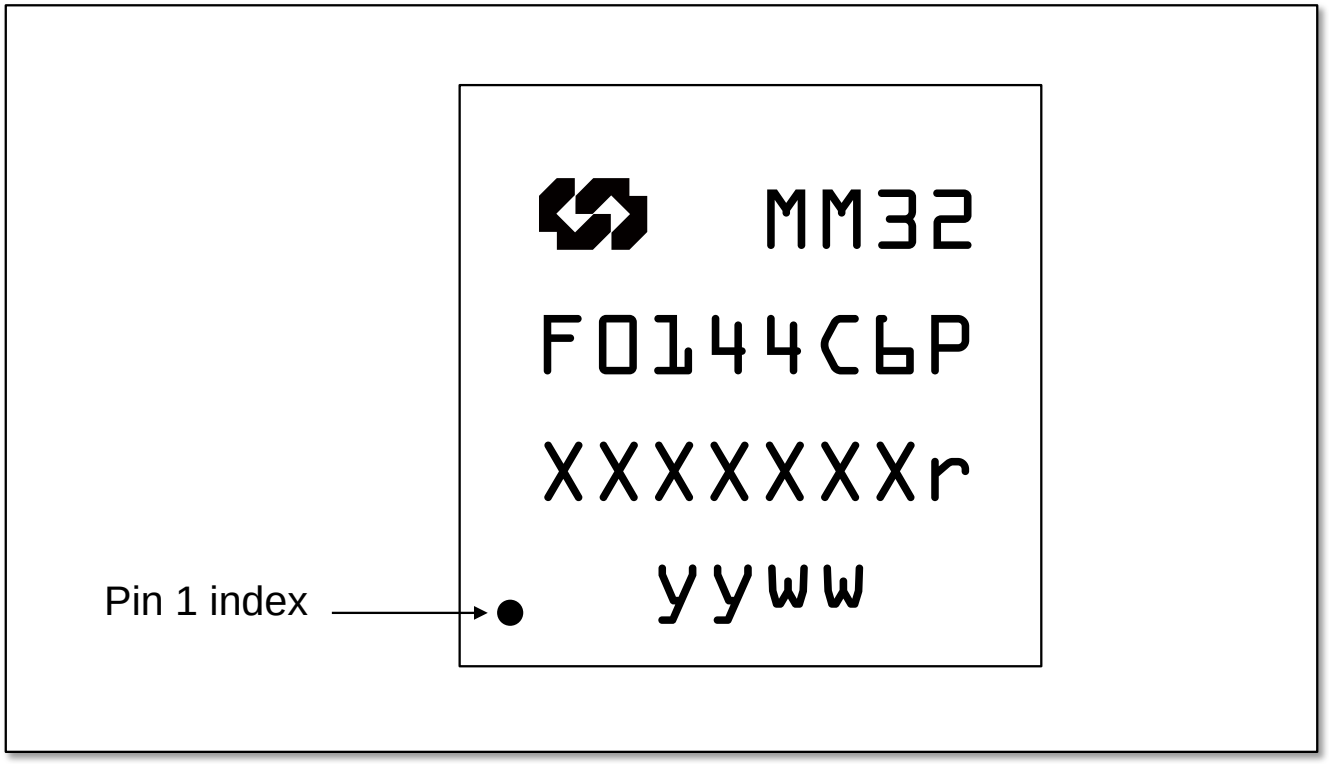

Figure 2-1 LQFP or QFN package marking

LQFP or QFN package has the following topside marking:

- 1st line: MM32
  - Company logo + first part of product name.
- 2nd line: F014xxxx
  - Second part of product name.
- 3rd line: xxxxxxxr
  - Trace code + revision code, the “r” means chip revision.
- 4th line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

Ordering information

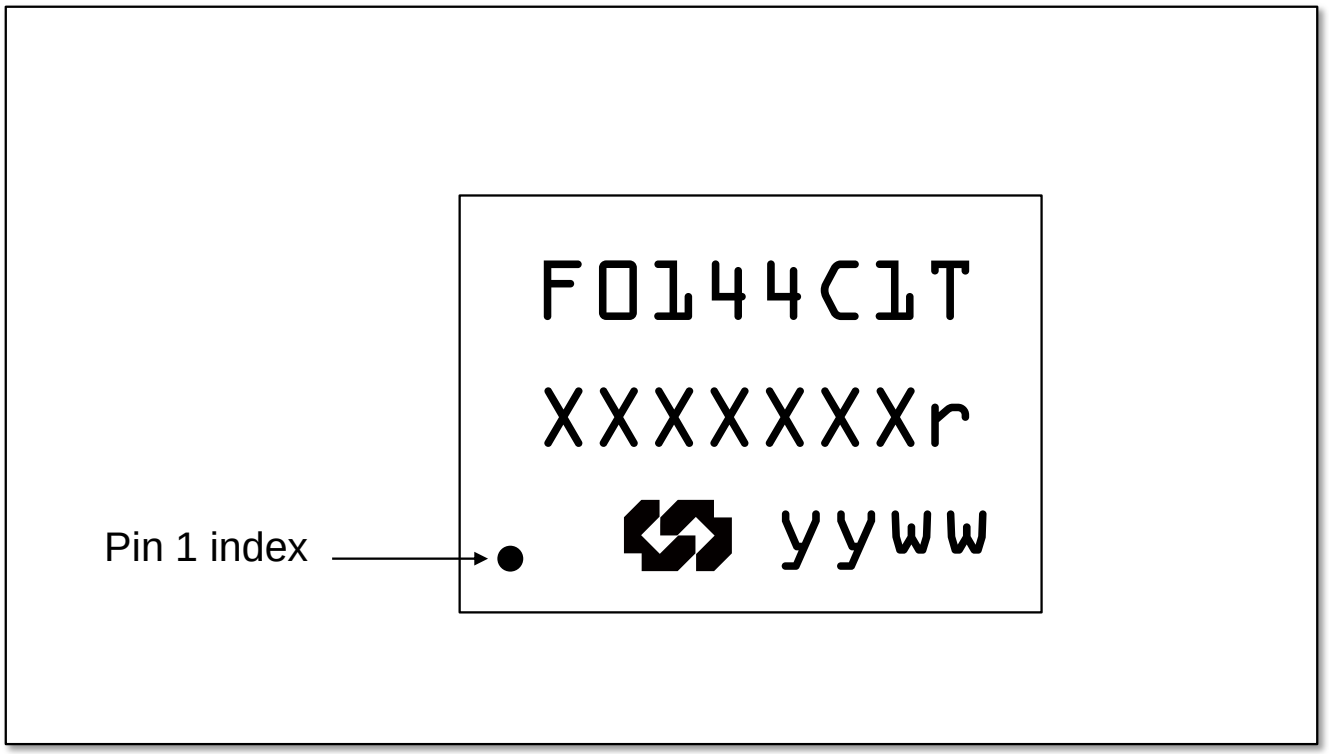

Figure 2-2 TSSOP20 package marking

TSSOP20 package has the following topside marking:

- 1st line: F014xxxx
  - Part of product name.
- 2nd line: xxxxxxxr
  - Trace code + revision code, the “r” means chip revision.
- 3rd line: Company logo + yyww
  - Date code, “yy” means year and “ww” means week in date code.

3 Functional description

3.1 Block diagram

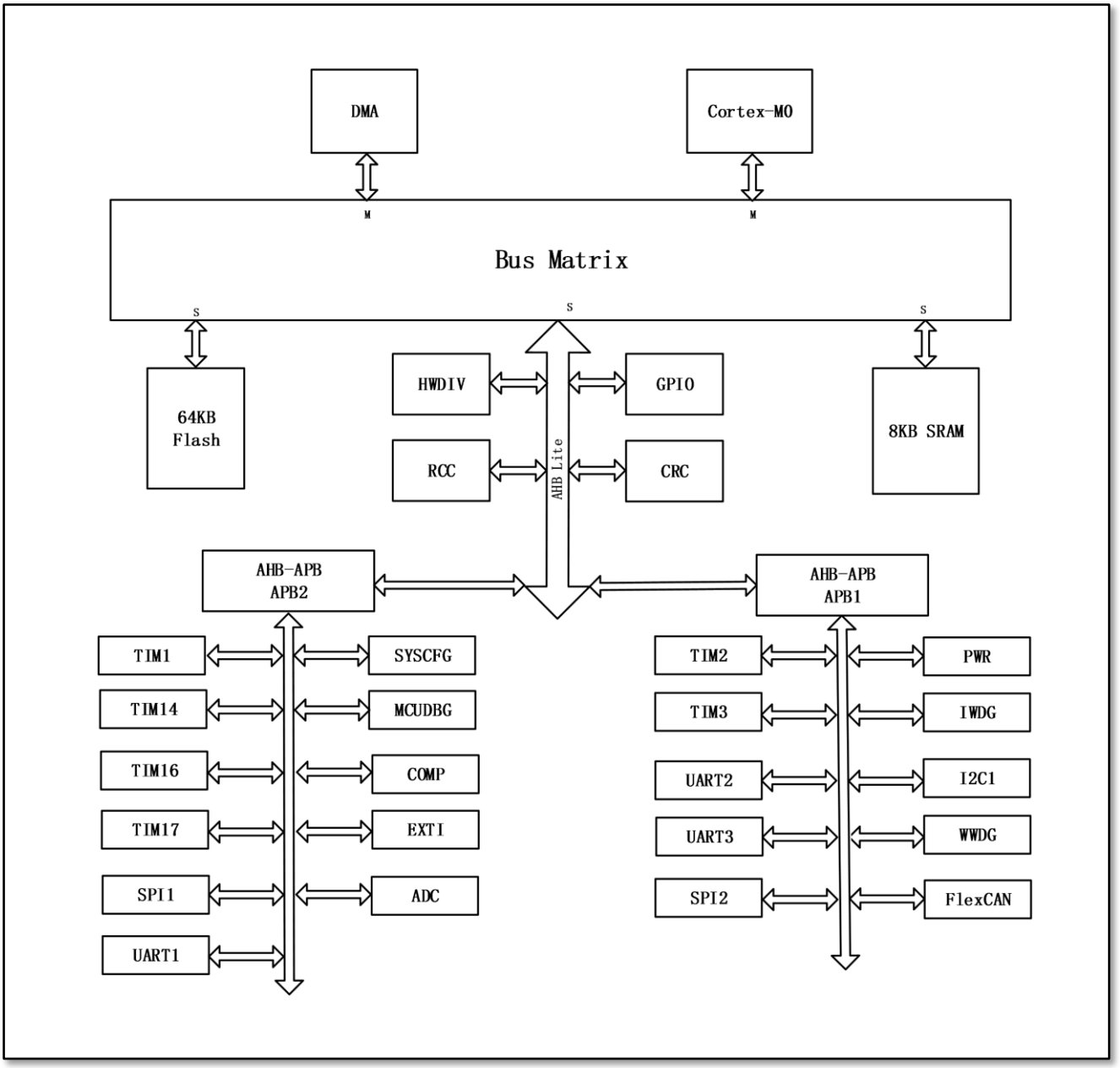

Figure 3-1 System block diagram

3.2 Core introduction

The ARM® Cortex®-M0 processor provides real-time processing and advanced interrupt handling system, which is perfect for cost-effective and low-pin-count microcontrollers targeting real-time control and low power applications.

The ARM® Cortex®-M0 is a 32-bit RISC processor, provides state-of-the-art code efficiency, which is extremely suitable for small memory size microcontrollers and small code size applications.

With its embedded ARM core, this product is compatible with all the tools and software for ARM-based products.

3.3 Bus introduction

The bus matrix includes one AHB inter-connection bus matrix, one AHB bus and two AHB-to-APB bridges. The bus matrix has arbitration capability for scenarios when both CPU and DMA send access simultaneously. The peripherals on the AHB bus (e.g., RCC, HWDIV, GPIO, CRC) are connected to the system bus through the inter-connection matrix. The data are transferred between AHB and APB bus using an AHB-to-APB bridge. When there's 8-bit or 16-bit access to APB registers, the APB bus will extend the access to 32-bit automatically.

3.4 Memory map

Table 3-1 Memory map

Bus	Address range	Size	Peripheral
Flash	0x0000 0000-0x0000 FFFF	64 KB	Map to main Flash, system memory or SRAM according to boot configuration
	0x0000 0000-0x07FF FFFF	~128 MB	Reserved
	0x0800 0000-0x0800 FFFF	64 KB	Main Flash
	0x0801 0000-0x1FFD FFFF	~383 MB	Reserved
	0x1FFE 0000-0x1FFE 01FF	0.5 KB	Reserved
	0x1FFE 0200-0x1FFE 0FFF	3 KB	Reserved
	0x1FFE 1000-0x1FFE 11FF	0.5 KB	Encrypted area
	0x1FFE 1200-0x1FFE 1BFF	2.5 KB	Encrypted area
	0x1FFE 1C00-0x1FFF F3FF	~256 MB	Reserved
	0x1FFF F400-0x1FFF F7FF	1 KB	System memory
	0x1FFF F800-0x1FFF F9FF	0.5KB	Option bytes
	0x1FFF FA00-0x1FFF FFFF	1.5KB	Reserved
SRAM	0x2000 0000-0x2000 1FFF	8 KB	SRAM
	0x2000 2000-0x2FFF FFFF	~255 MB	Reserved
APB1	0x4000 0000-0x4000 03FF	1 KB	TIM2
	0x4000 0400-0x4000 07FF	1 KB	TIM3
	0x4000 0800-0x4000 2BFF	9 KB	Reserved
	0x4000 2C00-0x4000 2FFF	1 KB	WWDG
	0x4000 3000-0x4000 33FF	1 KB	IWDG
	0x4000 3400-0x4000 37FF	1 KB	Reserved
	0x4000 3800-0x4000 3BFF	1 KB	SPI2

Bus	Address range	Size	Peripheral
	0x4000 3C00-0x4000 43FF	2 KB	Reserved
	0x4000 4400-0x4000 47FF	1 KB	UART2
	0x4000 4800-0x4000 4BFF	1 KB	UART3
	0x4000 4C00-0x4000 53FF	2 KB	Reserved
	0x4000 5400-0x4000 57FF	1 KB	I2C1
	0x4000 5800-0x4000 6FFF	6 KB	Reserved
	0x4000 7000-0x4000 73FF	1 KB	PWR
	0x4000 7400-0x4000 83FF	4 KB	Reserved
	0x4000 8400-0x4000 87FF	1 KB	Reserved
	0x4000 8800-0x4000 BFFF	14 KB	Reserved
	0x4000 C000-0x4000 FFFF	16 KB	FlexCAN
APB2	0x4001 0000-0x4001 03FF	1 KB	SYSCFG
	0x4001 0400-0x4001 07FF	1 KB	EXTI
	0x4001 0800-0x4001 23FF	7 KB	Reserved
	0x4001 2400-0x4001 27FF	1 KB	ADC
	0x4001 2800-0x4001 2BFF	1 KB	Reserved
	0x4001 2C00-0x4001 2FFF	1 KB	TIM1
	0x4001 3000-0x4001 33FF	1 KB	SPI1
	0x4001 3400-0x4001 37FF	1 KB	DBGMCU
	0x4001 3800-0x4001 3BFF	1 KB	UART1
	0x4001 3C00-0x4001 3FFF	1 KB	COMP
	0x4001 4000-0x4001 43FF	1 KB	TIM14
	0x4001 4400-0x4001 47FF	1 KB	TIM16
	0x4001 4800-0x4001 4BFF	1 KB	TIM17
	0x4001 4C00-0x4001 7FFF	13 KB	Reserved
AHB	0x4002 0000-0x4002 03FF	1 KB	DMA
	0x4002 0400-0x4002 0FFF	3 KB	Reserved
	0x4002 1000-0x4002 13FF	1 KB	RCC
	0x4002 1400-0x4002 1FFF	3 KB	Reserved
	0x4002 2000-0x4002 23FF	1 KB	Flash Interface
	0x4002 2400-0x4002 2FFF	3 KB	Reserved
	0x4002 3000-0x4002 33FF	1 KB	CRC
	0x4002 3400-0x4002 FFFF	47 KB	Reserved
	0x4003 0000-0x4003 03FF	1 KB	HWDIV
	0x4003 0400-0x47FF FFFF	~127 MB	Reserved
	0x4800 0000-0x4800 03FF	1 KB	GPIOA
	0x4800 0400-0x4800 07FF	1 KB	GPIOB
	0x4800 0800-0x4800 0BFF	1 KB	GPIOC
	0x4800 0C00-0x4800 0FFF	1 KB	GPIOD

3.5 Flash

This product provides up to 64KB embedded Flash memory available for storing code and data.

3.6 SRAM

This product provides up to 8KB embedded SRAM.

3.7 NVIC

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Cortex-M0) and manage 16 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Tightly coupled NVIC interfaces.
- Allow early processing of interrupts.
- Support high priority interrupt preemption.
- Support interrupt tail-chaining.
- Automatically save processor status.
- Automatic restoration when the interrupt returns with no instruction overhead.

This module provides flexible interrupt management with minimal interrupt latency.

3.8 EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

The EXTI can detect the level fluctuation of an external line with a pulse width shorter than the internal APB2 clock period.

3.9 Clock and boot

The system clock can be configured after chip power-on. After the power-on reset, the default clock is the internal 8MHz high speed oscillator (HSI). User can configure to use the external 4 to 24MHz crystal oscillator (HSE) as the system clock. The system will automatically block the external clock source, turn off the PLL and use the internal oscillator when the external clock is detected to be invalid. Meanwhile, if the clock monitor interrupt is enabled, an interrupt request will be generated.

The clock system uses multiple pre-dividers to generate the clock for the AHB and APB (APB1 and APB2) bus. The maximum frequency of the AHB and APB bus clock can reach up to 72MHz.

3.10 Boot modes

During boot, BOOT0 pins and BOOT bit are used to select one of three boot options:

- Boot from embedded Flash
- Boot from system memory
- Boot from embedded SRAM

The Bootloader code locates in the system memory. Once the chip boots from the system memory, it will run the bootloader code and user can program the embedded Flash through UART1 port by using the bootloader.

3.11 Power supply schemes

- V_{DD} = 2.0V ~ 5.5V: I/O ports and internal voltage regulator are powered by the V_{DD} Pins.
- V_{DDA} = 2.0V ~ 5.5V: ADC, reset logic, oscillators, PLL are powered by the V_{DDA} pin. V_{DDA} and V_{SSA} can either be connected to V_{DD} and V_{SS} respectively or be powered individually. When powered individually, the power supply should be at the same voltage level as the V_{DD} and V_{SS}.

3.12 Power supply supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status, without need of an external reset circuit.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enable through user program.

3.13 Voltage regulator

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that can be served by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

3.14 Low power mode

This product supports multiple low power modes, user can select the low power modes according to their end application to achieve a balance between power consumption, wakeup time and wakeup source.

Sleep mode

In sleep mode, only the CPU clock is gated off. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

In stop mode, low power consumption can be achieved with all RAM and registers content in retention. In stop mode, HSI and HSE are powered off. The microcontroller can be woken up by the EXTI signals. EXTI signals can come from the 16 external I/O ports or PVD output.

Deep stop mode

Similar as stop mode, but with lower power consumption.

Standby mode

In standby mode, the lowest power consumption can be achieved. In this mode, the voltage regulator is powered off, and all the 1.5V domain are shut down. PLL, HSI and HSE are also powered off. Wakeup sources include rising edge on WKUP pin, active reset on NRST pin, IWDG reset or RTC timer. SRAM and registers content are lost in this mode. Only backup register and standby circuit are powered.

3.15 Hardware divider

This product has a hardware divider unit (HWDIV). It can automatically run the 32-bit signed or unsigned integer division operation. The HWDIV is especially useful in some high-performance applications.

3.16 DMA

This product has a 5-channel direct memory access (DMA) controller. The DMA controller can be used to move data from memory to memory, peripherals to memory or memory to peripherals without CPU intervention. The DMA controller support ring buffer mode, when data reaches end of the buffer, the ring buffer mode can avoid generating an interrupt.

Each DMA channel has independent DMA request handling logic. All channels can be triggered by software. For each channel, the data length, source address and destination address can be independently configured by software.

DMA can be used for peripherals include UART, I2C, SPI, ADC, and general purpose, advanced, or basic timers.

3.17 Timers and watchdogs

This product has one advanced timer, two general purpose timers, three basic timers, two watchdog timers and one Systick timer. The table below compares the features of advanced, general purpose and basic timers.

Table 3-2 Feature summary of advanced, general purpose and basic timers

Type	Instance	Resolution	Counter direction	pre-divider	DMA request	Capture/compare channels	Complementary output
Advanced	TIM1	16-bit	up, down, up/down	1 to 65536	Yes	4	Yes
General purpose	TIM2	32-bit	up, down, up/down	1 to 65536	Yes	4	No
	TIM3	16-bit	up, down, up/down	1 to 65536	Yes	4	No
Basic	TIM14 / TIM16 / TIM17	16-bit	up	1 to 65536	Yes	-	Yes

Advanced timer (TIM1)

The advanced timer includes a 16-bit counter, four capture/compare channels and three phases complementary PWM generator. This timer supports hardware dead-time insertion when using as complementary PWM generator. This timer can also be used as a full-function general purpose timer. This timer has four independent channels, each channel can be used for:

- Input capture
- Output compare
- PWM generator (center- or edge-aligned)
- Single pulse output

When this timer is used as a general-purpose timer, it has the same function as the TIM2. When this timer is used as a 16-bit PWM generator, it can be configured to a broad duty cycle range from 0% to 100%.

The advanced timer has lots of identical features and internal structures as the general-purpose timer, in this way the advanced timer can work together with the general-purpose timer through the link function, to provide synchronization and event trigger function.

In debug mode, the counter stops counting, and PWM output will be disabled.

General-purpose timer (TIMx)

This product has two general-purpose timers (TIM2, TIM3). The timer has a 16- or 32-bit counter, support both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output.

32-bit general-purpose timer

This timer has a 32-bit up and down counter, a 16-bit prescaler and four independent channels, each channel can be used as input capture, output compare, PWM or single pulse output.

16-bit general-purpose timer

This timer has a 16-bit up and down counter, a 16-bit prescaler and four independent channels, each channel can be used for input capture, output compare, PWM or single pulse output.

These general-purpose timers can also work together through the timer link function, to provide synchronization between timers and event trigger function.

Any general-purpose timer can be used to generate PWM output or work as basic timer. Each timer has independent DMA request.

These timers can also be used to decode incremental encoder signals and can also be used to decode one to four Hall sensors' digital output.

In debug mode, the counter stops counting, and PWM output will be disabled.

Basic timer (TIM14 / TIM16 / TIM17)

The basic timer is based on a 16-bit up counter and a 16-bit prescaler. In debug mode, the counter stops counting.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 40KHz oscillator. As it is independent of the main clock, it can run in shutdown and standby modes. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter stops counting.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the entire system when an system error occurs. It is clocked by the main clock and has an early warning interrupt function; in debug mode, the counter stops counting.

System tick timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a general down counter. It has the following features:

- 24-bit down counter
- Auto-reload capability
- A maskable interrupt can be generated when counter value is 0
- Programmable clock source

3.18 Backup registers

This product has twenty 16-bit backup registers that can be used to store user application data. They are in the backup domain. When the V_{DD} power supply is cut off, they are still powered by V_{BAT}. They will not be reset when the system is woken up from standby mode, or when there is a system reset or power reset.

3.19 GPIO

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripherals function port. Most GPIO pins are shared with digital or analog functions. If necessary, the peripheral functions of the I/O pins can be locked by specific operation to avoid accidental writing to the I/O register.

3.20 UART

This product has up to three UART interfaces. The UART interface supports configurable data length of 5-, 6-, 7-, 8-, and 9-bits. The UART interface also supports LIN master and slave function and ISO7816 smart card mode. All UART interfaces support DMA operation.

3.21 I2C

This product has up to one I2C interface. The I2C bus interface can work in multi-master mode or slave mode and supports standard and fast mode. The I2C interface supports 7-bit or 10-bit addressing.

3.22 SPI

This product has up to two SPI interfaces. The SPI interface can be configured as 1 to 32 bits per frame in master or slave mode, allowing up to 24 Mbps in master mode and 12 Mbps in slave mode. All SPI interfaces support DMA operation.

3.23 I2S

This product has up to two I2S interfaces shared with the SPI module. The I2S module shares three pins with SPI, supports half-duplex communication (transmitter or receiver only), master or slave operation, underflow flag in transmit mode (only slave), and overflow flag in receive mode (master and slave mode) and frame error flag in receive and transmit mode (only slave). 8-bit programmable linear prescaler is used to achieve precise audio sampling frequency from 8KHz to 192KHz. The data format can be 16-bit, 24-bit or 32-bit, and the data packet frame is fixed at 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit or 32-bit data frame).

3.24 FlexCAN

This product has up to one FlexCAN interface. The FlexCAN interface is compatible with CAN 2.0A and 2.0B (active) standard, with bit rate up to 1Mbps. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.

3.25 ADC

This product has a 12-bit analog/digital converter (ADC), with up to 13 external channels available, supports single-shot single-cycle and continuous scan conversion. In the scan mode, the conversion of the sampling value on the selected group of analog inputs is automatically performed. The ADC supports DMA operation.

The analog watchdog function allows the application to monitor one or all selected channels. When the monitored signal exceeds a preset threshold, an interrupt will be generated. The triggers generated by the general-purpose timers (TIMx) and the advanced timers can be selected to trigger the ADC sampling, in this way the ADC sampling can be synchronized with the timer.

Temperature sensor

The temperature sensor can generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel of the ADC to covert the output of the sensor to a digital value.

3.26 COMP

This product has one build-in analog comparators (COMP), which can be used independently (applicable to all I/O ports that have comparator function) or combined with timers. The COMP module can be used for a variety of functions including low-power mode wake-up event triggered by analog input, fast PWM output brake when over-current detected, events capture and OCref-clr events used for cycle-by-cycle current control. The COMP module supports programmable hysteresis voltage, programmable rate and power consumption, rail-to-rail comparator. Each comparator can select the voltage reference from the I/O ports or the internal voltage reference (CRV) which is a divided voltage value of the V_{DDA} or internal bandgap voltage.

3.27 CRC

The cyclic redundancy check (CRC) module uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. Among many applications, CRC is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a method to detect flash memory errors. The CRC module can be used to calculate the signature of the software package in real time and compare it with the signature generated when the software is linked and generated.

3.28 SWD

This product equips ARM standard two-wire serial debug interface (SWD).

4 Pinout and assignment

4.1 Pinout diagram

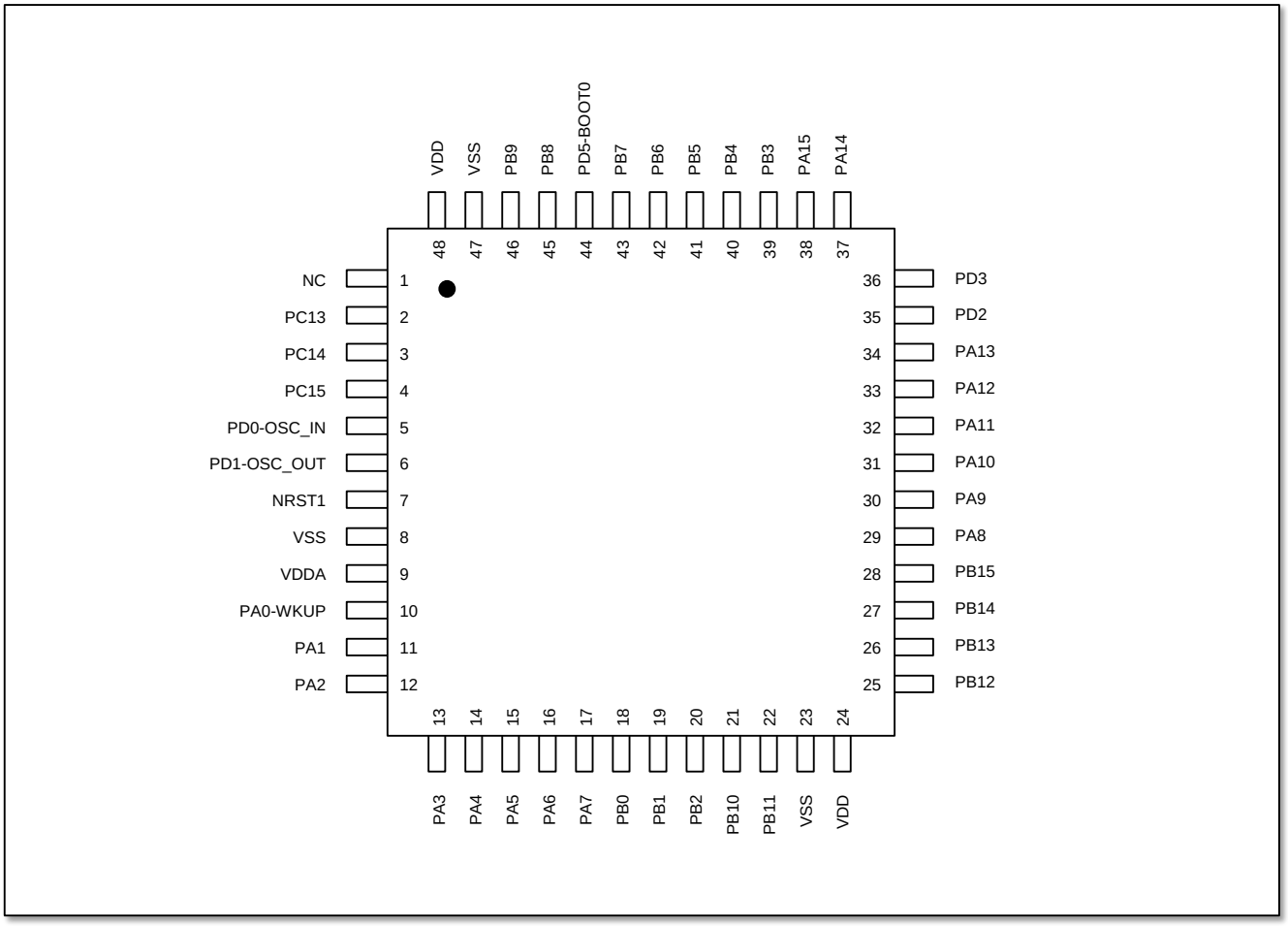

Figure 4-1 LQFP48 pinout diagram

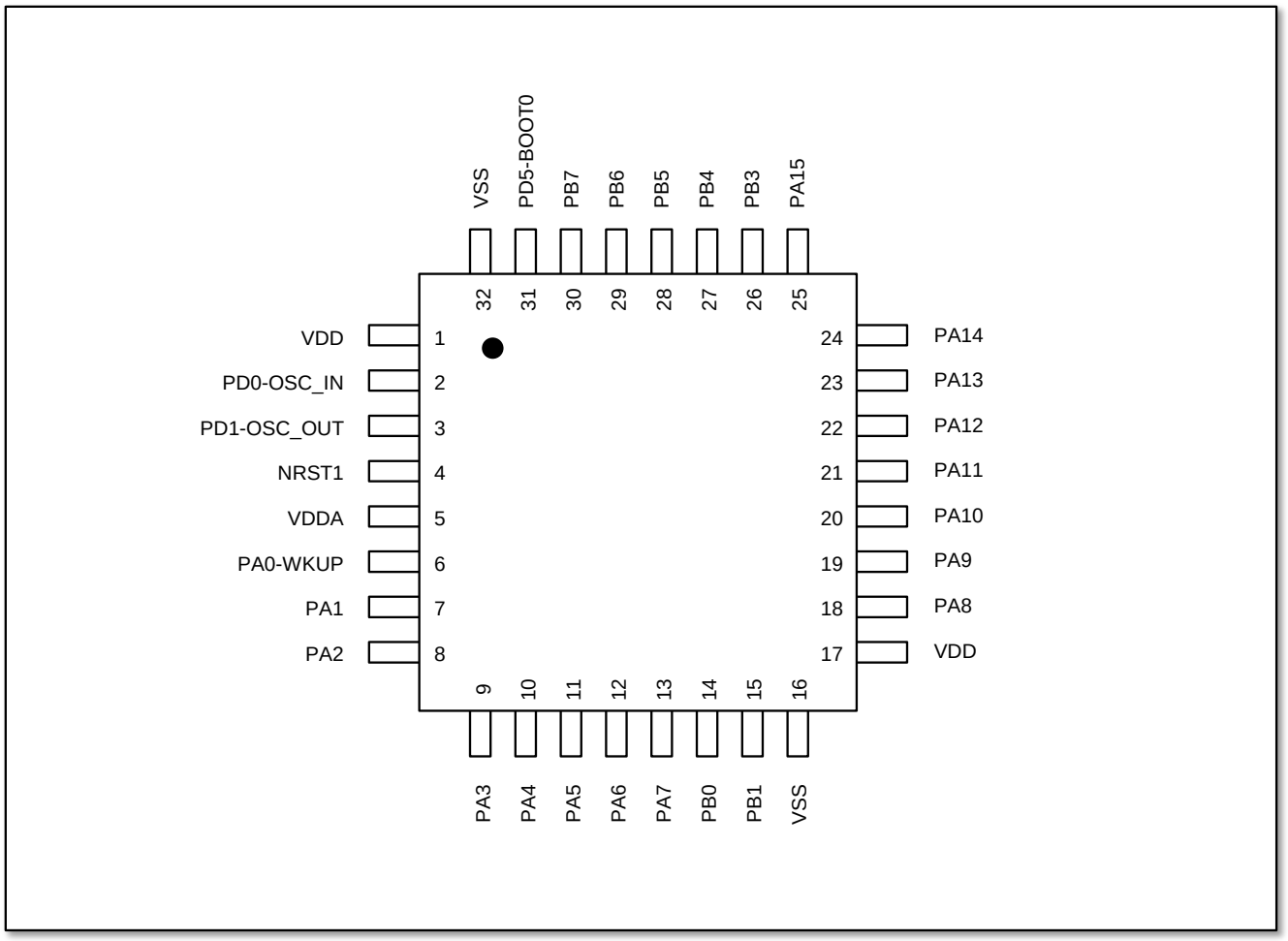

Figure 4-2 LQFP32 pinout diagram

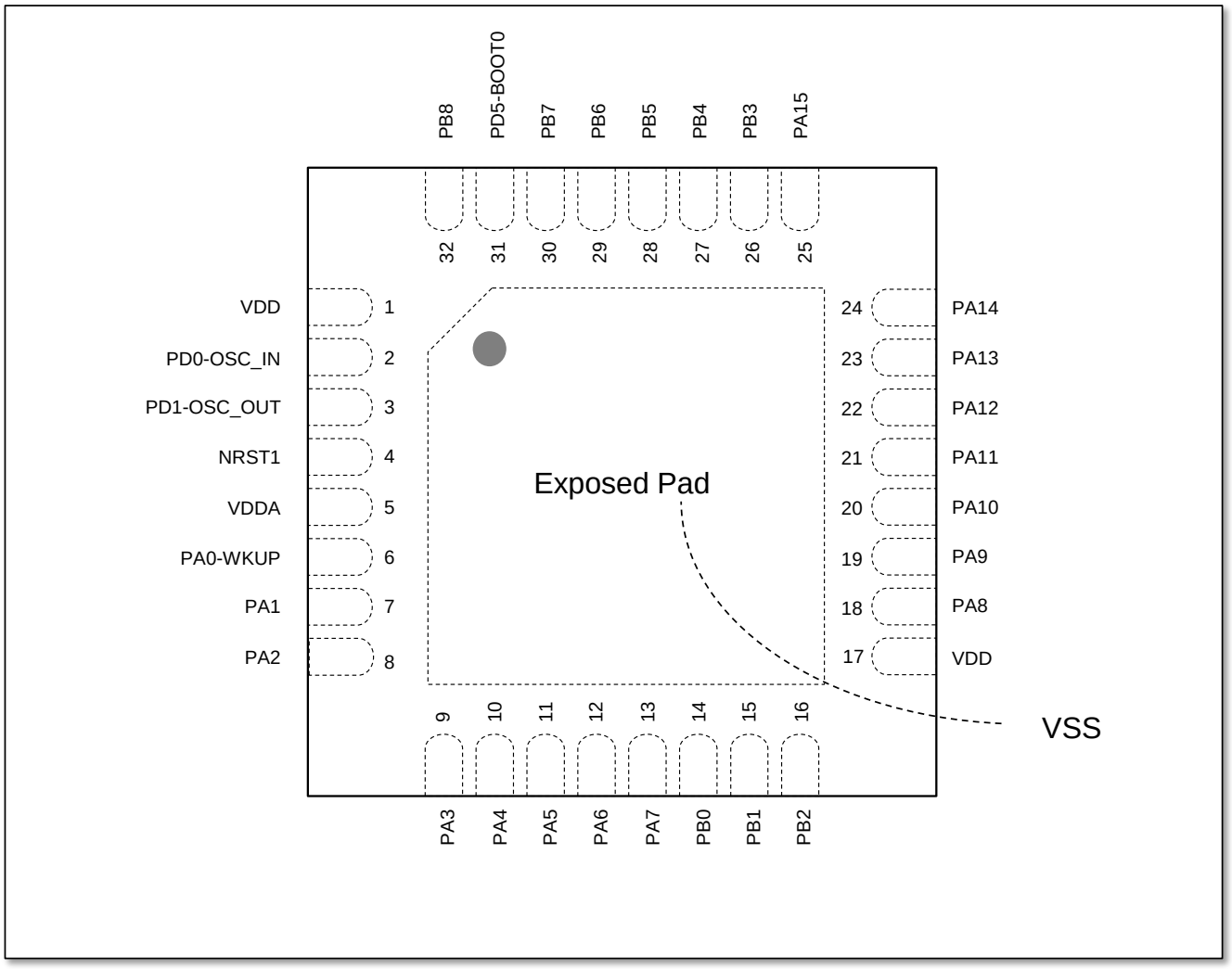

Figure 4-3 QFN32 pinout diagram

Pinout and assignment

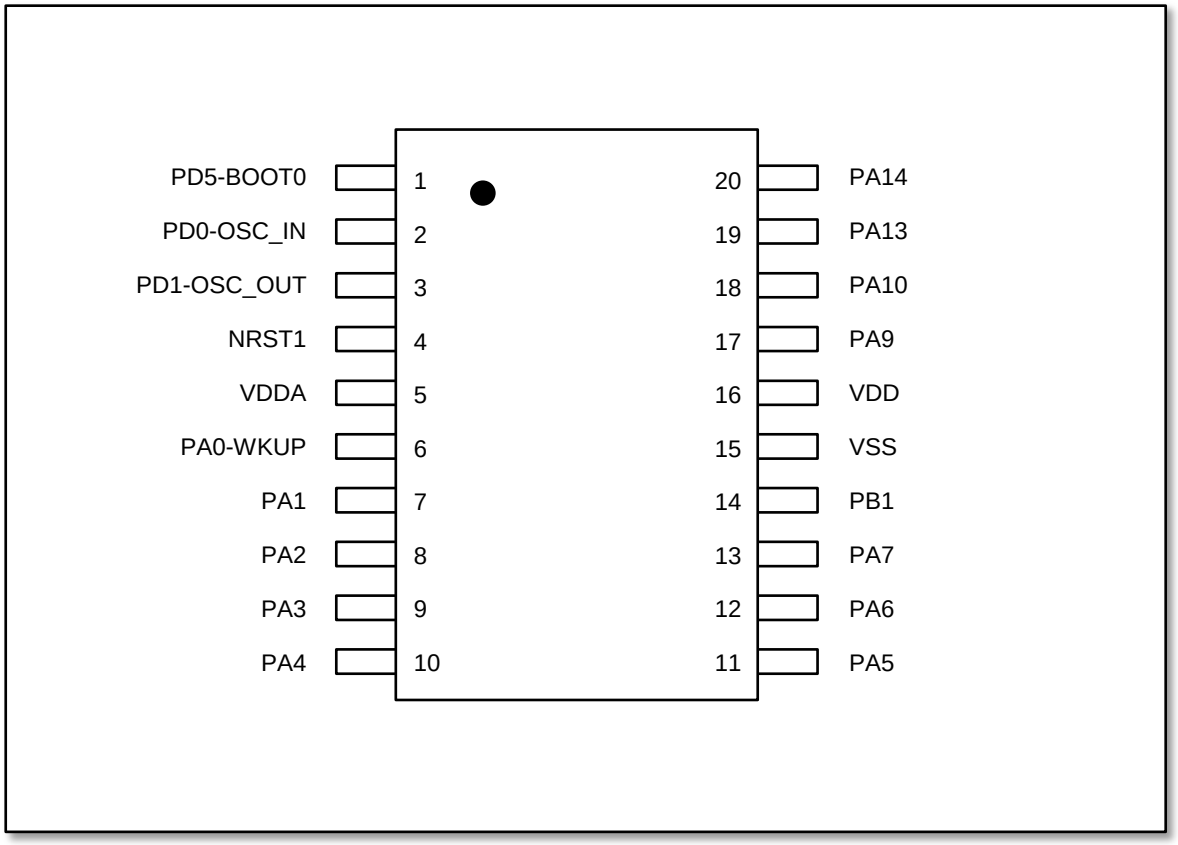

Figure 4-4 TSSOP20 pinout diagram

4.2 Pin assignment

Table 4-1 Pin assignment table

Pin ID[3]				Name	Type[1]	I/O level[2]	Main function	Multiplex function	Additional function
LQFP48	LQFP32	QFN32	TSSOP20						
1	-	-	-	NC	-	-	-	-	-
2	-	-	-	PC13	I/O	TC	PC13	TIM2_CH1	-
3	-	-	-	PC14	I/O	TC	PC14	TIM2_CH2	-
4	-	-	-	PC15	I/O	TC	PC15	TIM2_CH3	-
5	2	2	2	PD0 OSC_IN	I/O	TC	PD0	UART3_TX I2C_SDA	-
6	3	3	3	PD1 OSC_OUT	I/O	TC	PD1	UART3_RX I2C_SCL	-
7	4	4	4	NRST1	I/O	-	NRST1	-	-
8	-	D	-	VSS	S	-	VSS	-	-
9	5	5	5	VDDA	S	-	VDDA	-	-
10	6	6	6	PA0 WKUP	I/O	TC	PA0	UART2_CTS TIM2_CH1/TIM2_ETR SPI2_NSS/I2S2_WS TIM2_CH3 COMP1_OUT	ADC1_VIN[0]
11	7	7	7	PA1	I/O	TC	PA1	UART2_RTS TIM2_CH2	ADC1_VIN[1] COMP_SIN[0]
12	8	8	8	PA2	I/O	TC	PA2	UART2_TX TIM2_CH3 SPI2_NSS/I2S2_WS	ADC1_VIN[2] COMP_SIN[1]
13	9	9	9	PA3	I/O	TC	PA3	UART2_RX TIM2_CH4	ADC1_VIN[3] COMP_SIN[2]
14	10	10	10	PA4	I/O	TC	PA4	SPI1_NSS/I2S1_WS TIM1_BKIN TIM14_CH1 I2C_SDA	ADC1_VIN[4] COMP_SIN[3]
15	11	11	11	PA5	I/O	TC	PA5	SPI1_SCK/I2S1_CK TIM2_CH1/TIM2_ETR TIM1_ETR I2C_SCL TIM1_CH3N	ADC1_VIN[5] COMP_VREF[0]
16	12	12	12	PA6	I/O	TC	PA6	SPI1_MISO/I2S1_MCK TIM3_CH1 TIM1_BKIN UART2_RX TIM1_ETR TIM16_CH1 TIM1_CH3 COMP1_OUT	ADC1_VIN[6] COMP_VREF[1]
17	13	13	13	PA7	I/O	TC	PA7	SPI1_MOSI/I2S1_SD TIM3_CH2 TIM1_CH1N TIM14_CH1 TIM17_CH1 TIM1_CH2N TIM1_CH3N	ADC1_VIN[7] COMP_VREF[2]
18	14	14	-	PB0	I/O	TC	PB0	TIM3_CH3 TIM1_CH2N TIM1_CH1N TIM1_CH3 MIPI_DP	ADC1_VIN[8]
19	15	15	14	PB1	I/O	TC	PB1	TIM14_CH1 TIM3_CH4 TIM1_CH3N TIM1_CH4	ADC1_VIN[9]

Pin ID[3]				Name	Type[1]	I/O level[2]	Main function	Multiplex function	Additional function
LQFP48	LQFP32	QFN32	TSSOP20						
								TIM1_CH2N MCO TIM1_CH2 TIM1_CH1N MIPI_DN	
20	-	16	-	PB2	I/O	TC	PB2	-	-
21	-	-	-	PB10	I/O	TC	PB10	I2C_SCL TIM2_CH3 UART3_TX SPI2_SCK/I2S2_CK	-
22	-	-	-	PB11	I/O	TC	PB11	I2C_SDA TIM2_CH4 UART3_RX	-
23	16	D	15	VSS	S	-	VSS	-	-
24	17	17	16	VDD	S	-	VDD	-	-
25	-	-	-	PB12	I/O	TC	PB12	SPI2_NSS/I2S2_WS SPI2_SCK/I2S2_CK TIM1_BKIN SPI2_MOSI/I2S2_SD SPI2_MISO/I2S2_MCK	-
26	-	-	-	PB13	I/O	TC	PB13	SPI2_SCK/I2S2_CK SPI2_MISO/I2S2_MCK TIM1_CH1N SPI2_NSS/I2S2_WS SPI2_MOSI/I2S2_SD I2C_SCL TIM1_CH3N TIM2_CH1 UART3_CTS	-
27	-	-	-	PB14	I/O	TC	PB14	SPI2_MISO/I2S2_MCK SPI2_MOSI/I2S2_SD TIM1_CH2N SPI2_SCK/I2S2_CK SPI2_NSS/I2S2_WS I2C_SDA TIM1_CH3 TIM1_CH1 UART3_RTS	-
28	-	-	-	PB15	I/O	TC	PB15	SPI2_MOSI/I2S2_SD SPI2_NSS/I2S2_WS TIM1_CH3N SPI2_MISO/I2S2_MCK SPI2_SCK/I2S2_CK TIM1_CH2N TIM1_CH2	-
29	18	18	-	PA8	I/O	TC	PA8	MCO TIM1_CH1 TIM1_CH2 TIM1_CH3	-
30	19	19	17	PA9	I/O	TC	PA9	UART1_TX TIM1_CH2 UART1_RX I2C_SCL MCO TIM1_CH1N TIM1_CH4 CAN_RX	-
31	20	20	18	PA10	I/O	TC	PA10	TIM17_BKIN UART1_RX TIM1_CH3 UART1_TX I2C_SDA	-

Pin ID[3]				Name	Type[1]	I/O level[2]	Main function	Multiplex function	Additional function
LQFP48	LQFP32	QFN32	TSSOP20						
								TIM1_CH1 SPI2_SCK/I2S2_CK CAN_TX	
32	21	21	-	PA11	I/O	TC	PA11	UART3_TX UART1_CTS TIM1_CH4 CAN_RX SPI2_MOSI/I2S2_SD I2C_SCL COMP1_OUT	-
33	22	22	-	PA12	I/O	TC	PA12	UART3_RX UART1_RTS TIM1_ETR CAN_TX SPI2_MISO/I2S2_MCK I2C_SDA TIM1_CH2	-
34	23	23	19	PA13	I/O	TC	PA13	SWDIO UART1_TX SPI2_MISO/I2S2_MCK MCO TIM1_CH2 TIM1_BKIN	-
35	-	-	-	PD2	I/O	TC	PD2	-	-
36	-	-	-	PD3	I/O	TC	PD3	-	-
37	24	24	20	PA14	I/O	TC	PA14	SWDCLK UART2_TX UART1_RX SPI1_NSS/I2S1_WS	-
38	25	25	-	PA15	I/O	TC	PA15	SPI1_NSS/I2S1_WS UART2_RX TIM2_CH1/TIM2_ETR	-
39	26	26	-	PB3	I/O	TC	PB3	SPI1_SCK/I2S1_CK TIM2_CH2 UART1_TX TIM2_CH3 TIM1_CH1 TIM2_CH1	ADC1_VIN[10]
40	27	27	-	PB4	I/O	TC	PB4	SPI1_MISO/I2S1_MCK TIM3_CH1 UART1_RX TIM17_BKIN TIM1_CH2 TIM2_CH2	ADC1_VIN[11]
41	28	28	-	PB5	I/O	TC	PB5	SPI1_MOSI/I2S1_SD TIM3_CH2 TIM16_BKIN MCO TIM1_CH3 TIM2_CH3	-
42	29	29	-	PB6	I/O	TC	PB6	UART1_TX I2C_SCL TIM16_CH1N TIM2_CH1	-
43	30	30	-	PB7	I/O	TC	PB7	UART1_RX I2C_SDA TIM17_CH1N UART2_TX	ADC1_VIN[12]
44	31	31	1	PD5 BOOT0	I/O	TC	PD5	-	-
45	-	32	-	PB8	I/O	TC	PB8	I2C_SCL TIM16_CH1	-

Pin ID[3]				Name	Type[1]	I/O level[2]	Main function	Multiplex function	Additional function
LQFP48	LQFP32	QFN32	TSSOP20						
								CAN_RX UART2_RX	
46	-	-	-	PB9	I/O	TC	PB9	I2C_SDA TIM17_CH1 CAN_TX TIM1_CH4 SPI2_NSS/I2S2_WS	-
47	32	D	-	VSS	S	-	VSS	-	-
48	1	1	-	VDD	S	-	VDD	-	-

1. I = input, O = output, S = power pins, HiZ = high resistance state.
2. TC: standard IO. Input signal level should not exceed VDD.
3. D = downbond

4.3 Pin multiplexing

Table 4-2 PA port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM2_CH1/TIM2_ETR	SPI2_NSS/I2S2_WS	TIM2_CH3	-	-	COMP1_OUT
PA1	-	UART2_RTS	TIM2_CH2	-	-	-	-	-
PA2	-	UART2_TX	TIM2_CH3	SPI2_NSS/I2S2_WS	-	-	-	-
PA3	-	UART2_RX	TIM2_CH4	-	-	-	-	-
PA4	SPI1_NSS/I2S1_WS	-	-	TIM1_BKIN	TIM14_CH1	I2C_SDA	-	-
PA5	SPI1_SCK/I2S1_CK	-	TIM2_CH1/TIM2_ETR	TIM1_ETR	-	I2C_SCL	TIM1_CH3N	-
PA6	SPI1_MISO/I2S1_MCK	TIM3_CH1	TIM1_BKIN	UART2_RX	TIM1_ETR	TIM16_CH1	TIM1_CH3	COMP1_OUT
PA7	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	TIM1_CH2N	TIM1_CH3N
PA8	MCO	-	TIM1_CH1	-	-	-	TIM1_CH2	TIM1_CH3
PA9	-	UART1_TX	TIM1_CH2	UART1_RX	I2C_SCL	MCO	TIM1_CH1N	TIM1_CH4
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C_SDA	-	TIM1_CH1	SPI2_SCK/I2S2_CK
PA11	UART3_TX	UART1_CTS	TIM1_CH4	CAN_RX	SPI2_MOSI/I2S2_SD	I2C_SCL	-	COMP1_OUT
PA12	UART3_RX	UART1_RTS	TIM1_ETR	CAN_TX	SPI2_MISO/I2S2_MCK	I2C_SDA	-	TIM1_CH2
PA13	SWDIO	-	UART1_TX	-	SPI2_MISO/I2S2_MCK	MCO	TIM1_CH2	TIM1_BKIN
PA14	SWDCLK	UART2_TX	UART1_RX	SPI1_NSS/I2S1_WS	-	-	-	-
PA15	SPI1_NSS/I2S1_WS	UART2_RX	TIM2_CH1/TIM2_ETR	-	-	-	-	-

Table 4-3 PB port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	TIM1_CH2N	TIM1_CH1N	TIM1_CH3	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM1_CH4	TIM1_CH2N	MCO	TIM1_CH2	TIM1_CH1N
PB2	-	-	-	-	-	-	-	-
PB3	SPI1_SCK/I2S1_CK	-	TIM2_CH2	UART1_TX	TIM2_CH3	-	TIM1_CH1	TIM2_CH1
PB4	SPI1_MISO/I2S1_MCK	TIM3_CH1	-	UART1_RX	-	TIM17_BKIN	TIM1_CH2	TIM2_CH2
PB5	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM16_BKIN	MCO	-	-	TIM1_CH3	TIM2_CH3
PB6	UART1_TX	I2C_SCL	TIM16_CH1N	-	TIM2_CH1	-	-	-
PB7	UART1_RX	I2C_SDA	TIM17_CH1N	-	UART2_TX	-	-	-
PB8	-	I2C_SCL	TIM16_CH1	CAN_RX	UART2_RX	-	-	-
PB9	-	I2C_SDA	TIM17_CH1	CAN_TX	TIM1_CH4	SPI2_NSS/I2S2_WS	-	-
PB10	-	I2C_SCL	TIM2_CH3	-	UART3_TX	SPI2_SCK/I2S2_CK	-	-
PB11	-	I2C_SDA	TIM2_CH4	-	UART3_RX	-	-	-
PB12	SPI2_NSS/I2S2_WS	SPI2_SCK/I2S2_CK	TIM1_BKIN	SPI2_MOSI/I2S2_SD	SPI2_MISO/I2S2_MCK	-	-	-
PB13	SPI2_SCK/I2S2_CK	SPI2_MISO/I2S2_MCK	TIM1_CH1N	SPI2_NSS/I2S2_WS	SPI2_MOSI/I2S2_SD	I2C_SCL	TIM1_CH3N	TIM2_CH1
PB14	SPI2_MISO/I2S2_MCK	SPI2_MOSI/I2S2_SD	TIM1_CH2N	SPI2_SCK/I2S2_CK	SPI2_NSS/I2S2_WS	I2C_SDA	TIM1_CH3	TIM1_CH1
PB15	SPI2_MOSI/I2S2_SD	SPI2_NSS/I2S2_WS	TIM1_CH3N	SPI2_MISO/I2S2_MCK	SPI2_SCK/I2S2_CK	-	TIM1_CH2N	TIM1_CH2

Table 4-4 PC port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC13	-	-	-	-	-	-	TIM2_CH1	-
PC14	-	-	-	-	-	-	TIM2_CH2	-
PC15	-	-	-	-	-	-	TIM2_CH3	-

Table 4-5 PD port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	UART3_TX	I2C_SDA	-	-	-	-	-	-
PD1	UART3_RX	I2C_SCL	-	-	-	-	-	-
PD2	-	-	-	-	-	-	-	-
PD3	-	-	-	-	-	-	-	-
PD4	-	UART2_TX	TIM2_CH3	SPI2_NSS/I2S2_WS	-	-	-	-
PD5	-	-	-	-	-	-	-	-
PD6	SPI1_MISO/I2S1_MCK	TIM3_CH1	TIM1_BKIN	UART2_RX	TIM1_ETR	TIM16_CH1	TIM1_CH3	COMP1_OUT

5 Package dimensions

5.1 LQFP48

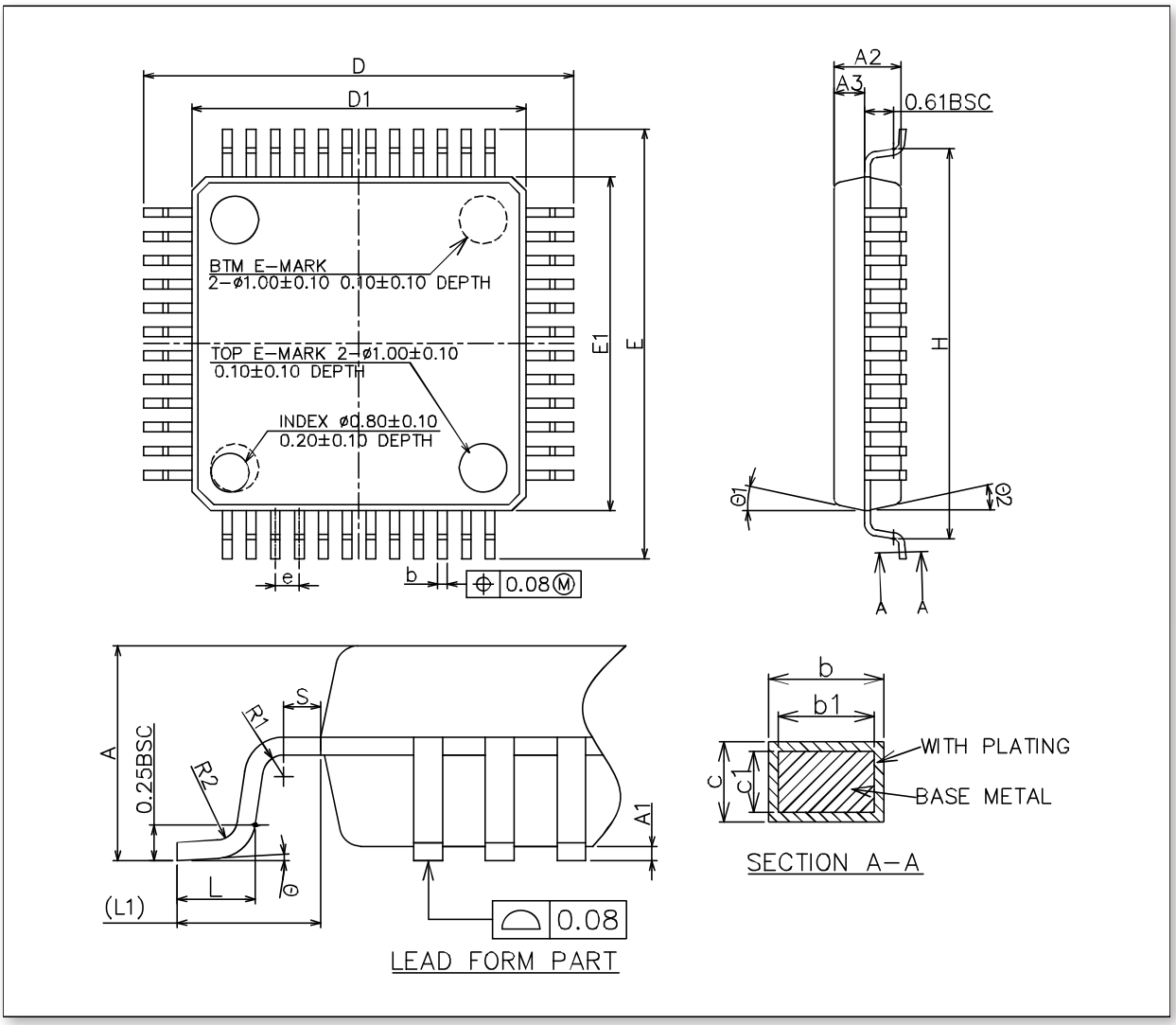

Figure 5-1 LQFP48 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Package dimensions

Table 5-1 LQFP48 package dimension details

ID	Millimeters		
	Minimum	Typical	Minimum
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.4	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
Θ3	11°	12°	13°

5.2 LQFP32

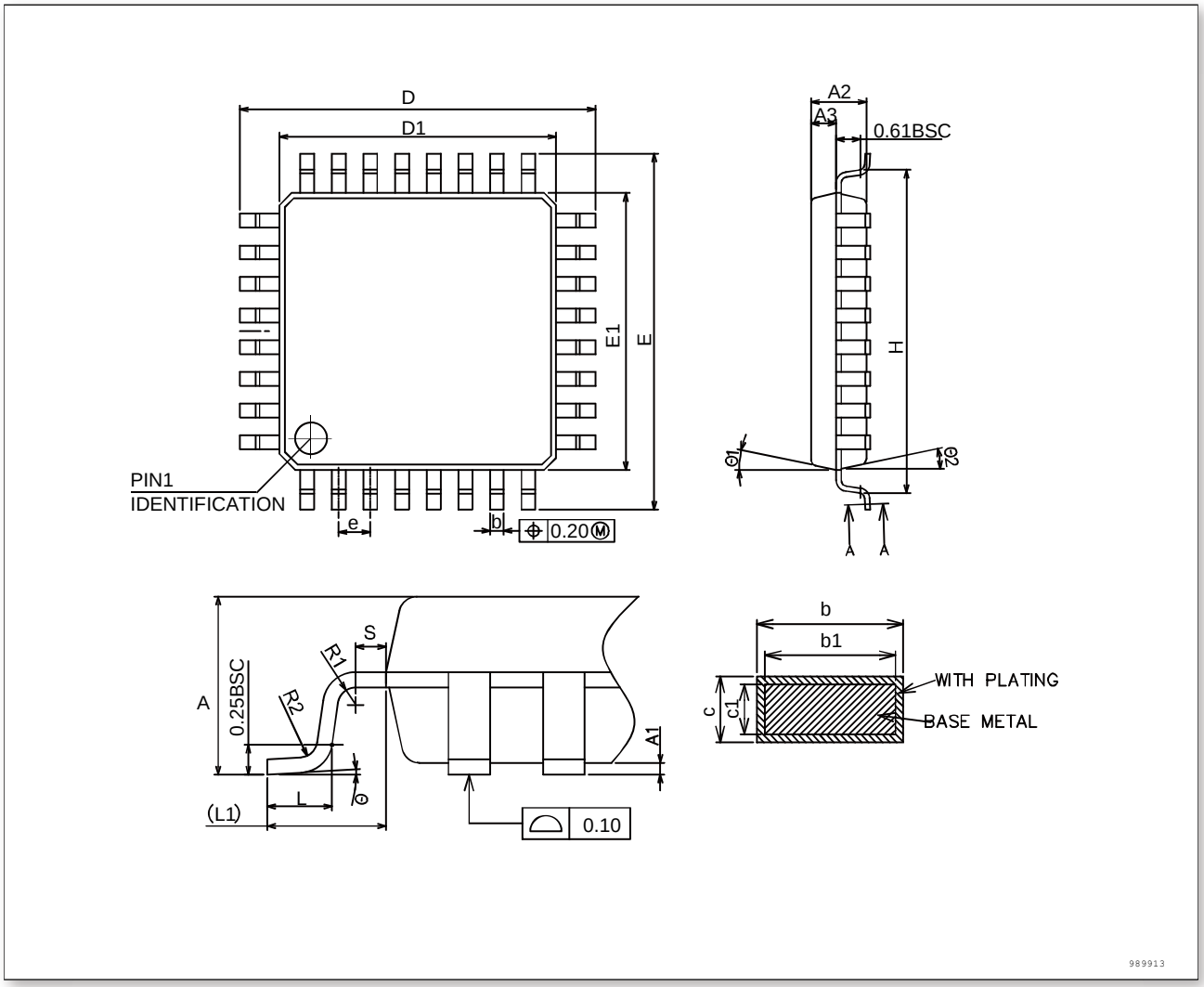

Figure 5-2 LQFP32 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Package dimensions

Table 5-2 LQFP32 package dimension details

ID	Millimeters		
	Minimum	Typical	Minimum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.42
b1	0.32	0.35	0.38
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
H	8.14	8.17	8.20
L	0.50	-	0.70
L1	1.00REF		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0 ◦	3.5 ◦	7 ◦
θ1	11 ◦	12 ◦	13 ◦
θ2	11 ◦	12 ◦	13 ◦

5.3 QFN32

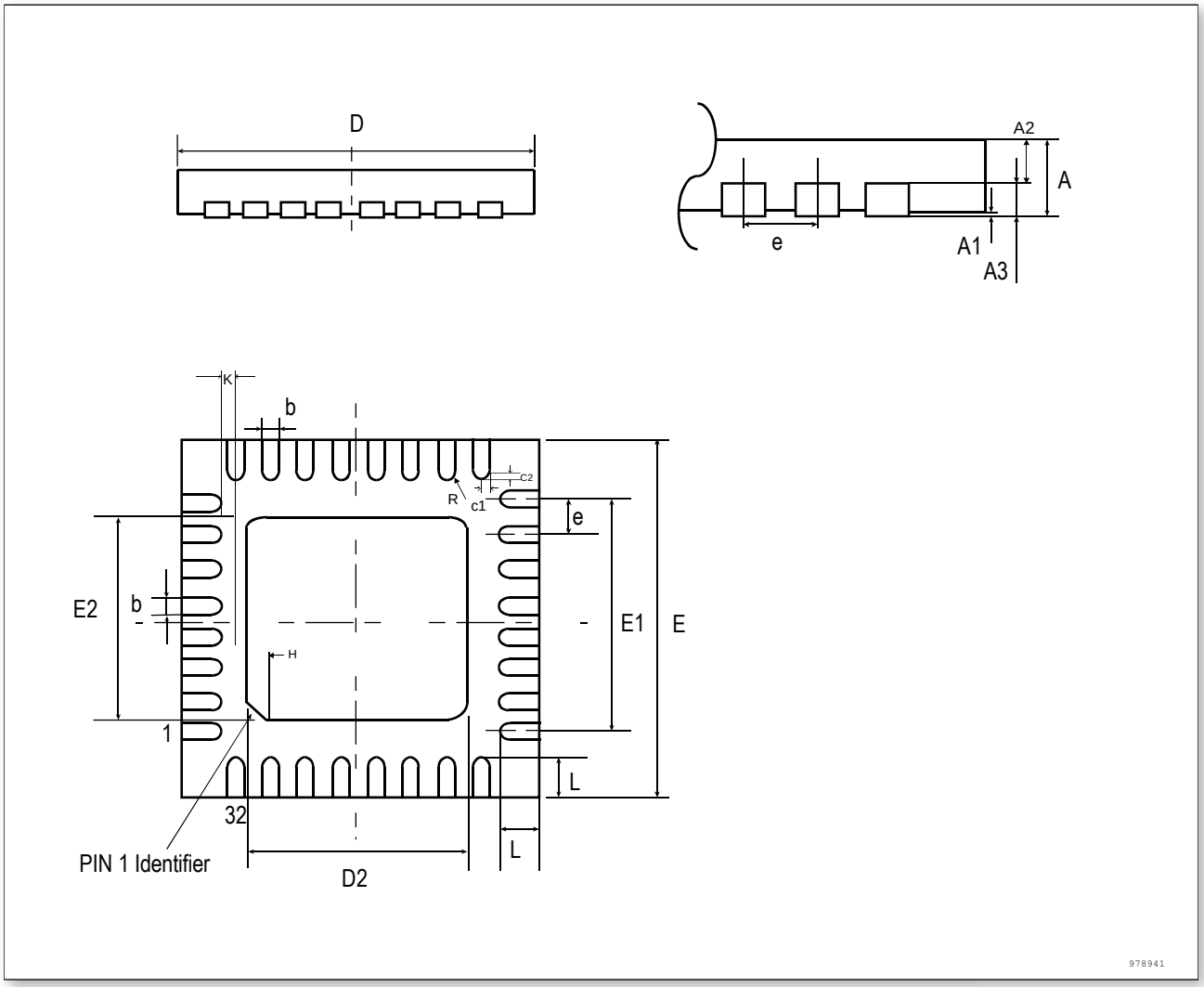

Figure 5-3 QFN32 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Package dimensions

Table 5-3 QFN32 package dimension details

ID	Millimeters		
	Minimum	**Typical**	**Minimum**
A	0.7	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
e		0.5	
H		0.30REF	
K		0.35REF	
L	0.35	0.40	0.45
R	0.09	-	-
c1	-	0.08	-
c2	-	0.08	-
N		Pin count = 32	

5.4 TSSOP20

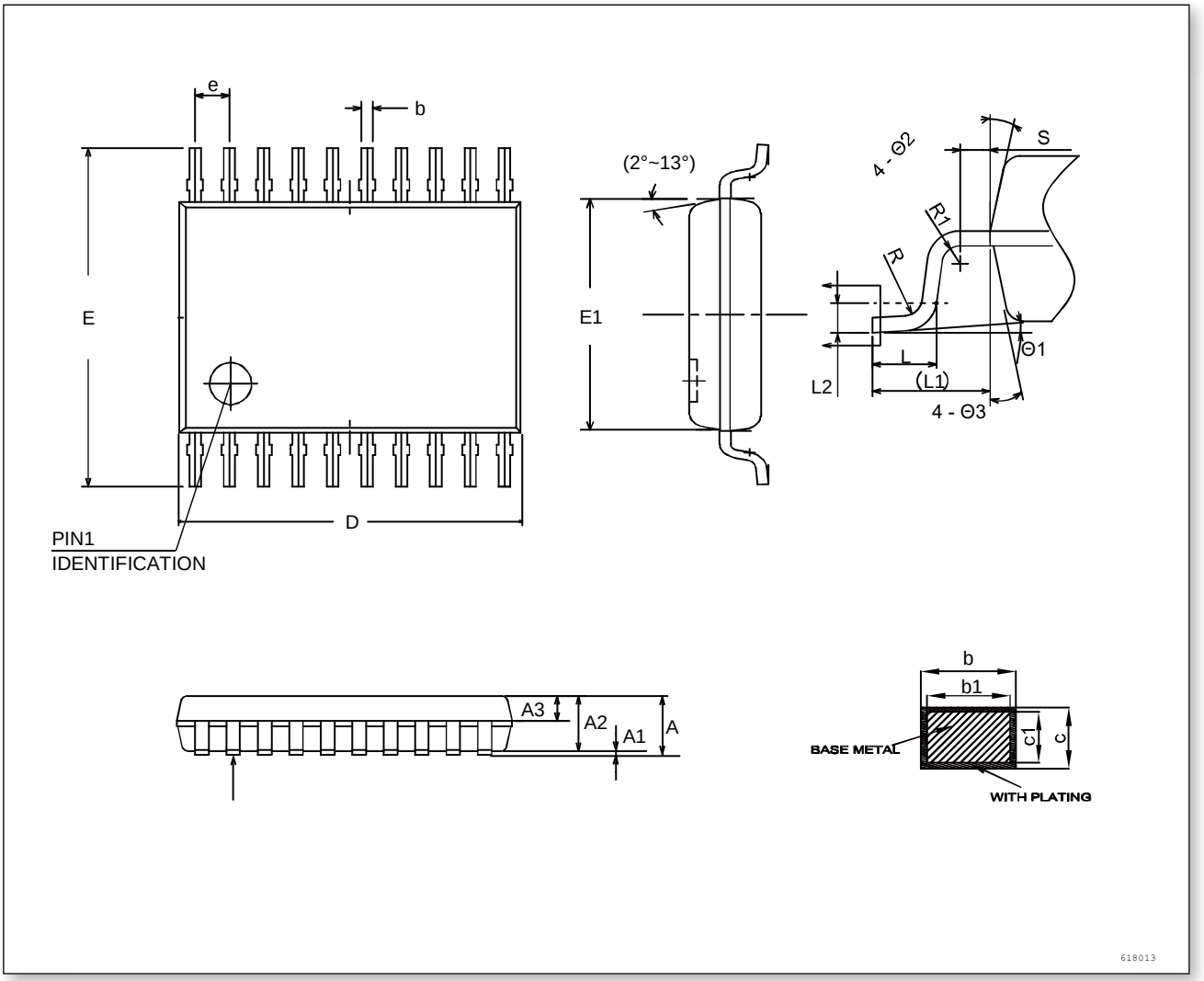

Figure 5-4 TSSOP20 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Package dimensions

Table 5-4 TSSOP20 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	-	-	1.20
A1	0.05	-	0.15
A2	-	-	1.05
A3	0.34	-	0.54
b	0.20	-	0.28
c	0.10	-	0.19
c1	0.10	-	0.15
D	6.40	6.45	6.60
E	6.20	6.40	6.60
E1	-	4.35	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L2	0.25BSC		
L1	1.0REF		
R	0.09	-	-
θ1	0°	-	8°

6 Part identification

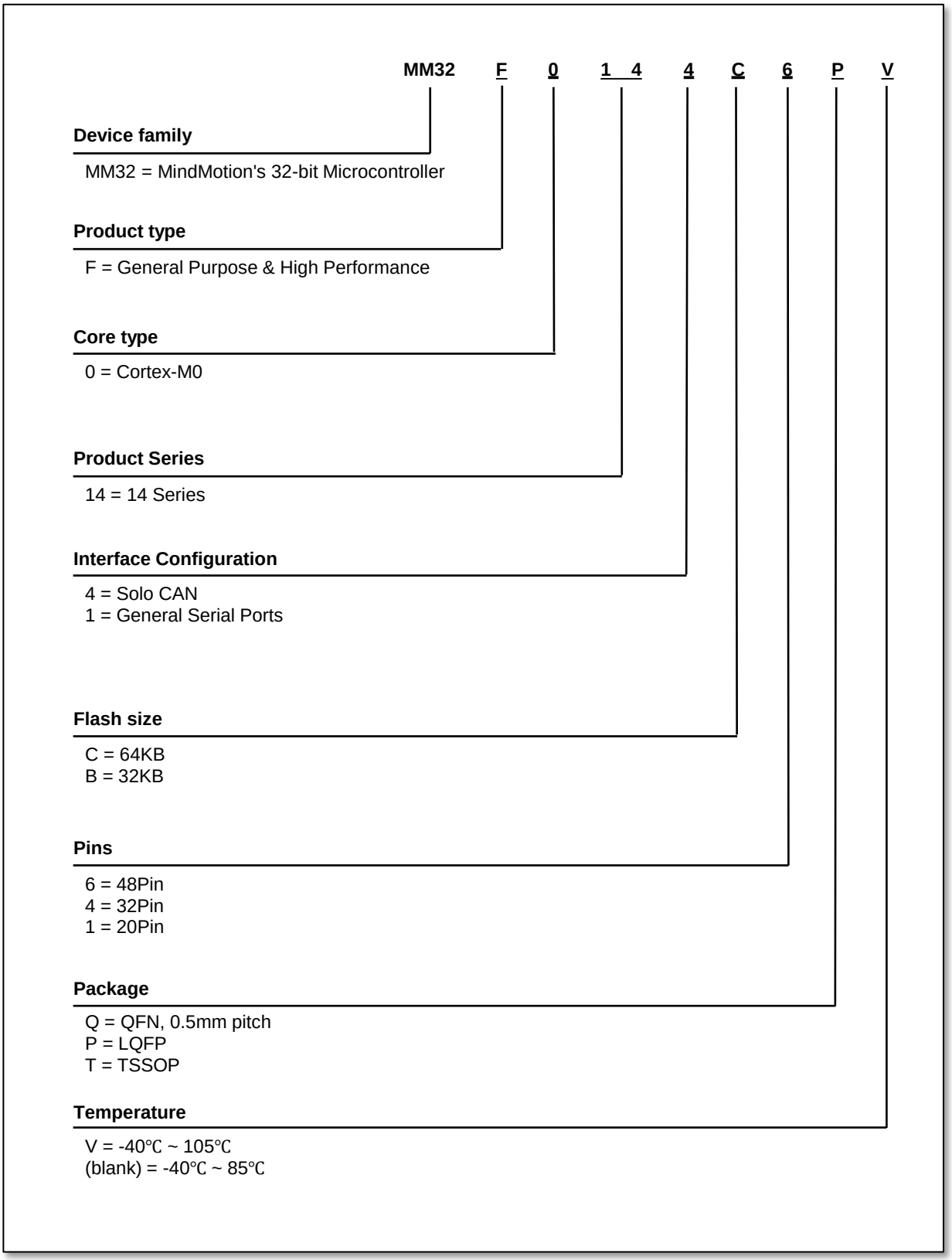

Figure 6-1 Part number naming rule

7 Revision history

Date	Revision	Description
2021/10/01	Rev1.0	Initial release