# An FPGA-Accelerated Platform for Post-FEC BER Analysis of 200 Gb/s Wireline Systems

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***Abstract*—As wireline communication links transition from 100 Gb/s to 200 Gb/s per lane, new and complex forward error correction (FEC) architectures have been proposed to achieve acceptably low bit error rates (BERs). It is essential to understand how these architectures impact link performance under various channel conditions. However, existing methods of post-FEC BER analysis are unsuitable for this application. To address this, we present a flexible platform for FPGA-accelerated post-FEC BER analysis of 200 Gb/s wireline systems. This platform can accurately demonstrate post-FEC BERs at the $10^{-12}$ level within a day of simulation time, a speed improvement of 10,000X over software-based simulation platforms.**

***Keywords*—Concatenated FEC, FPGA, BER, 200Gb/s, Wireline Transceiver, Interleaving, Ethernet**

## I. Introduction

The demand for wireline interconnectivity between data centers is rapidly growing, driven by AI applications, video streaming, and cloud services. Multi-part links are typically employed for communication between data centers, consisting of a short electrical link from a server to an optical module, followed by a long optical link to reach another module at the receiving data center, with another short electrical link connecting to the receiving server. All three links along the data path can introduce errors in the transmitted data. The electrical links have significant inter-symbol interference (ISI), so equalization techniques such as decision feedback equalization (DFE) or maximum-likelihood sequence estimation (MLSE) are used to recover the signal. Both DFE and MLSE suffer from error propagation, which causes the errors from electrical links to be predominantly bursts of correlated errors [1, 2]. In optical links, correlated errors may also be present, but the errors are predominantly random [3]. For modern high-speed wireline applications, forward error correction (FEC) is necessary to achieve acceptable bit error rates (BERs).

For 100 Gb/s communication, a typical end-to-end FEC architecture uses the Reed-Solomon KP4 FEC code [4], shown in Figure 1(a). The KP4 code is a strong, linear block code that operates on 10-bit-long FEC symbols. It can correct up to 15 FEC symbols in a 544-FEC-symbol-long codeword. Any codewords with more than 15 FEC-symbol errors are uncorrectable and contribute to the BER after FEC decoding (post-FEC BER). For 100 Gb/s links, the IEEE 802.3ck 100GBASE-KR1 standard specifies a BER allocation of $2.4\times10^{-4}$ before FEC decoding (pre-FEC BER) to enable a post-FEC BER lower than around $10^{-12}$ to $10^{-13}$ [4].

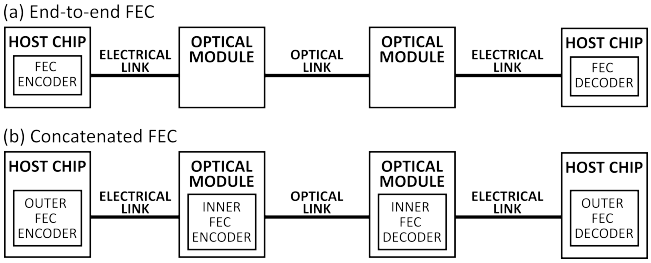


Fig. 1. System-level FEC architectures for multi-part links. (a) End-to-end FEC. (b) Concatenated FEC

The next generation of wireline links will operate at 200 Gb/s. Doubling the data rate degrades signal integrity, necessitating a stronger FEC architecture to achieve acceptable post-FEC BERs. To address this, the IEEE 802.3dj task force has adopted a concatenated FEC architecture [5] that includes an additional inner code protecting the optical link, shown in Figure 1(b). The inner code is a binary Hamming code that can correct one bit error per 128-bit codeword. Although this code can only correct one bit error per codeword, it is effective against the random errors produced by optical links and has low complexity. The outer code is the same KP4 code used in 100 Gb/s links. Because it is strong and non-binary, this code is well-suited to correct the bursts of errors that arise in electrical links. Details on the specific concatenated FEC architecture for 200 Gb/s wireline systems, including interleaving and multiplexing schemes, are still under consideration by the IEEE 802.3dj task force. It is necessary to understand precisely how these architectures affect a system's post-FEC BER to make informed decisions on which to adopt in the upcoming 200 Gb/s standard and to set pre-FEC BER allocations for the electrical and optical links in a way that maintains an acceptable post-FEC BER while minimizing latency and power consumption.

To address the need for a method of analyzing 200 Gb/s link performance, we present a field-programmable gate array (FPGA) platform for accelerated time-domain simulations. It can run simulations of a multi-part link with concatenated FEC at $1.8\times10^{9}$ bits per second on a Xilinx UltraSCALE FPGA, allowing accurate BER estimation down to $10^{-12}$ within a day of simulation time. In Section 2, we discuss existing methods for BER analysis and explain why they are unsuitable for demonstrating targeted BERs for 200 Gb/s architectural explorations. Then, in Section 3, we present our FPGA simulation platform. In Section 4, we show simulation results that verify the accuracy of our platform. Finally, in Section 5, we present a case study that demonstrates the utility of our

platform by solving an open problem in architecting 200 Gb/s wireline systems.

## II. Existing Post-FEC BER Estimation Methods

There are two main approaches for estimating the post-FEC BER of a wireline system. One approach is to use a time-domain simulation, where real data is transmitted through a model of the system, and the BER is estimated by dividing the number of bit errors by the total number of transmitted bits. The other approach is to build a statistical model to analytically determine the post-FEC BER.

Time-domain simulations are typically software-based. Unfortunately, software simulations demonstrating BERs below $10^{-12}$ are prohibitively time-consuming. For example, the software model reported in [6] can simulate $1.47\times10^5$ bits per second when running on 16 parallel CPU cores. At this speed, it would take about two months to observe just one bit error at a BER of $10^{-12}$! Although it is possible to speed this up using more parallel processing, our FPGA platform, which runs over 10,000 times faster, is also parallelizable. For stringent compliance tests that may even require BER verification down to $10^{-15}$ levels, it is far more cost-effective to scale up an FPGA-based simulation platform.

Because software-based time-domain simulations are too slow, various extrapolation methods are used in industry to estimate the post-FEC BER from a simulation that is not long enough to observe post-FEC bit errors. However, in many cases, this approach is inaccurate because the correlation between signal-to-noise ratio (SNR) and BER may change significantly at lower BERs [6].

Another approach is to use a statistical model to determine post-FEC BER analytically [6,7]. While statistical models can determine arbitrarily low BERs in a reasonable amount of time, they are limited in the type of architectures they can model. For example, a statistical model for concatenated FEC codes is proposed by [7], but it cannot capture the interleaving and symbol multiplexing schemes proposed for 200 Gb/s systems. Another drawback of statistical models is that it is difficult to verify their accuracy at very low BERs. Typically, this is done by comparing results with a time-domain simulation. If the results match, designers can be confident in both the statistical and time-domain models. Hence, a fast time-domain simulation platform is still required to develop and verify new statistical models.

## III. FPGA Simulation Platform

Figure 2 shows the system-level architecture of our FPGA simulation platform. To run a simulation, a user models the system of interest by building the *BER simulation IP* block using our library of custom modules. The platform supports parallel processing, where the *BER simulation IP* contains multiple parallel cores to increase simulation speed.

The user configures simulation settings (e.g. SNR of each link, inner FEC on/off, simulation termination condition) via the user interface on a PC. Software running on the MicroBlaze processor configures the *BER simulation IP* with these settings and starts the simulation. Then, binary data is

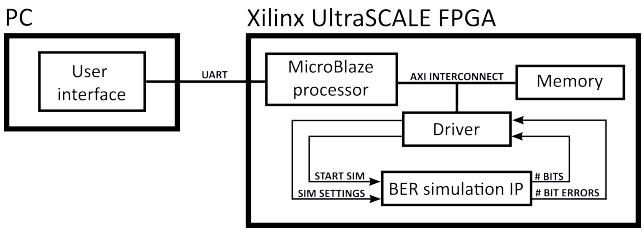


Fig. 2. Proposed FPGA-accelerated simulation platform.

generated and sent through the wireline system model. A count of the total number of bits transmitted is maintained, as well as the number of bit errors before and after outer-FEC decoding. After 1,000 post-FEC bit errors are observed, the results are automatically written to the memory and can be viewed on the user interface. 1,000 observed post-FEC bit errors allow us to be 90% confident that the simulated BER is within 30% of the true BER. The following subsections describe the architecture of 200 Gb/s wireline systems and how they are modelled with our *BER simulation IP*.

### A. Input Data, Modulaton, and Signal Precoding

For the simulations shown in this paper, we use a PRBS sequence as input data for BER testing. Grey-coded PAM-4 modulation is applied to the input binary sequence before transmission through electrical and optical channels. Our platform also has modules to implement 1/(1+D) precoding, a DSP algorithm used to reduce the impact of bursts of consecutive PAM-symbol errors that arise in electrical links due to DFE or MLSE error propagation.

### B. Channel Model

Our platform supports two approaches for modelling the errors introduced by the electrical and optical channels. The first approach is to do a convolution of the PAM-4 signal with a channel pulse response and add a time-domain noise signal. Then, digital equalization such as DFE or MLSE is applied to this noisy received signal. The other approach is to use a Markov model to inject errors in the transmitted PAM-4 signal. While this approach can be less accurate when colored noise is present, it is commonly used in industry to model the errors introduced by electrical and optical channels under a wide range of impairments such as additive white Gaussian noise (AWGN), ISI, and jitter [2]. For the simulation results shown in this paper, we use a Markov model of a 1-tap DFE-based receiver for electrical links [6], and a simple AWGN channel with no ISI for optical links.

### C. KP4 FEC Model

Using a deterministic PRBS sequence as input data provides a convenient way of checking the post-FEC BER without the need for a complex and resource-intensive KP4 encoder and decoder on the FPGA. Our platform includes a simple KP4 checker module that compares the data stream at the output of the simulation to the input PRBS sequence. The module tracks the number of bit errors and FEC-symbol errors for each transmitted codeword, allowing it to determine the pre-FEC and post-FEC BER.

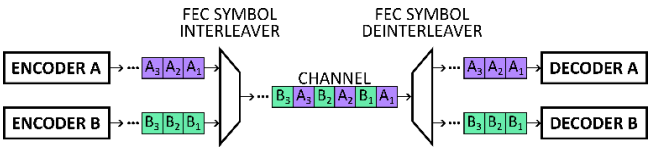


Fig. 3. 2-way FEC-symbol interleaving.

### D. FEC-Symbol Interleaving

FEC-symbol interleaving is another technique used to mitigate bursts of consecutive errors. With *N*-way FEC-symbol interleaving, *N* different codewords are transmitted through the channel simultaneously, with their FEC symbols interleaved in a round-robin fashion. This architecture distributes consecutive FEC-symbol errors over multiple codewords, giving them a greater chance of being corrected. Both 2-way and 4-way FEC-symbol interleaving schemes are considered for 200 Gb/s applications [5]. An example of 2-way FEC-symbol interleaving is shown in Figure 3. Our FPGA platform supports *N*-way interleaving by making a simple modification to the KP4 checker module described earlier: the module keeps track of which of the *N* codewords the current FEC-symbol belongs to and maintains bit errors and FEC-symbol error counts for each of the *N* codewords individually.

### E. Inner Code and Convolutional Interleaving

Due to its small minimum distance, the inner Hamming decoder may exhibit miscorrections, significantly impacting its performance [7]. To properly consider this, we use a real inner-FEC encoder and decoder in our FPGA platform rather than the simplified checker used for the outer code.

Although the errors introduced in optical links may be predominantly random, the inner-FEC decoder changes the error distribution by correcting the inner-FEC codewords with only one error and not correcting codewords with multiple errors. To give the outer code the best chance of correcting errors from an uncorrected 120-bit-long inner-FEC codeword, each of its twelve 10-bit-long outer-FEC symbols should originate from different outer-FEC codewords that get decoded separately. This is achieved with sufficient FEC-symbol interleaving and convolutional interleaving. Convolutional interleaving is a technique that permutes the order of input symbols at the cost of added latency [8]. A recent IEEE standard proposal defines the specific convolutional interleaver architecture to achieve an inner-FEC codeword with outer FEC symbols from 12 distinct KP4 codewords [5]. Our platform includes convolutional interleavers that are customizable to support all the architecture proposals for 200 Gb/s signaling.

## IV. Simulation Results

In this section, we show simulation results from our FPGA platform, demonstrating our platform's ability to accurately determine post-FEC BERs below $10^{-12}$. The systems considered in this section are simple one-link systems so that we can superimpose results obtained using the statistical models presented in [6] and [7]. By showing that the results obtained with our FPGA platform match the statistical model down to low BERs, we verify the accuracy of both models when subject to the same FEC architecture and noise assumptions.

Figure 4 shows post-FEC BER on a logarithmic scale on the *y*-axis and link SNR in decibels (dB) on the *x*-axis. Two different channels in the presence of AWGN are considered: a memoryless channel modelling an optical link, and an ISI channel having pulse response $h = 1 + 0.8z^{-1}$, modelling a long-reach electrical link with around 38dB insertion loss at the Nyquist frequency. A zero-forcing DFE fully cancels the post-cursor ISI. The two channels have the same random error probability for a given SNR, but for the channel with 0.8 DFE tap weight, each random bit error may cause a burst of consecutive errors due to DFE error propagation. These two channels with only the outer KP4 FEC are shown with blue and grey lines, respectively. Figure 4 also shows time-domain software simulation results for the memoryless channel with a red line. Both software and FPGA simulations were performed with one day of simulation time. However, the software simulation could only demonstrate BERs down to around $10^{-8}$, while our FPGA platform demonstrated BERs below $10^{-12}$. Other works on BER analysis including the software simulation presented in [6] and another FPGA platform presented in [9] do not present time-domain-simulated post-FEC BERs lower than $10^{-8}$. This significant speed improvement over existing simulation platforms allows us to explore new and complex FEC architectures with high accuracy, which is the key novelty of our platform.

The green and orange lines show the ISI channel with (1/1+*D*) signal precoding and 4-way interleaving, respectively. Both techniques mitigate the effect of the burst errors. The purple line shows the performance of the AWGN channel with the concatenated Hamming + KP4 FEC architecture. The inner code provides a significant increase in performance across all SNR levels. At high SNR, the concatenated FEC's coding gain diminishes slightly compared to the KP4 FEC due to inner-FEC miscorrections. All FPGA-simulated data points match closely to the statistical model. This allows us to be confident in the accuracy of our

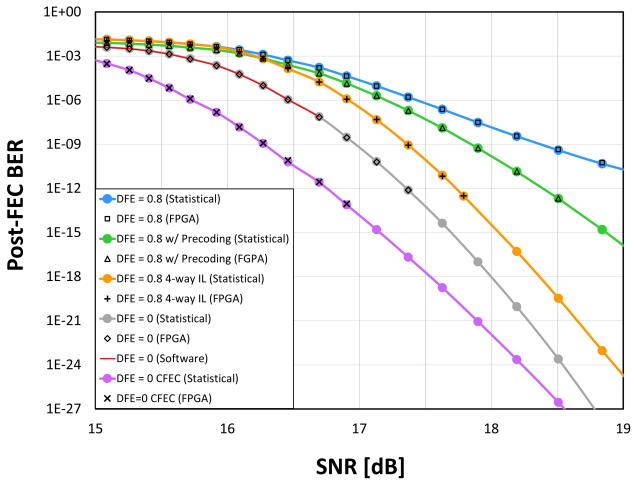


Fig. 4. SNR vs. post-FEC BER for different channels with precoding, interleaving, and concatenated FEC (CFEC).

FPGA platform in Section 5, where we apply it to new FEC architectures for multi-part links that are too complex for any existing statistical models.

## V. Case Study: BER Allocation For multi-Part Links

In Section 4, we verified the accuracy of several components of our FPGA platform individually on a simple single-part link. In this section, we put together all the pieces and show a practical application that demonstrates how our FPGA platform can be used as a tool for architecting 200 Gb/s multi-part links.

A topic of ongoing discussion for 200 Gb/s multi-part links is the BER allocation between optical and electrical links, i.e., how high of a BER can be allowed in each of the three links while maintaining a sufficiently low post-FEC BER for the entire system. Setting the BER allocation is essential to maintain interoperability for hosts and modules from different vendors. Recent IEEE standard contributions have proposed target BERs [10], but until now, there has been no reliable method to validate the proposals rigorously.

Figure 5 shows simulation results for a multi-part link with the concatenated FEC and convolutional interleaving architecture presented in Section 3. We show three cases of optical links producing random errors at different module-to-module BERs: 0, $1.34\times10^{-3}$, and $2\times10^{-3}$. We also consider three electrical (host-to-module and module-to-host) links: a memoryless channel and ISI channels having pulse responses $h = 1+0.5z^{-1}$ and $h = 1+0.8z^{-1}$ in the presence of AWGN with zero-forcing DFE. The electrical channel is protected by precoding and 2-way FEC-symbol interleaving. The host channel SNR is shown on the $x$-axis. Both electrical links have the same pulse response and SNR for each simulation. Post-FEC BER for the entire multi-part link is shown on the $y$-axis.

Figure 5 shows an 'error floor' region at high electrical SNR for systems with errors present in the optical channel. In this region, errors are predominantly from the optical link, so increasing electrical SNR has a smaller effect on the system's overall performance. The channel with 0.5 DFE tap weight shows a slight decrease in performance compared to the memoryless electrical channel, whereas the channel with 0.8 DFE tap weight shows a much larger performance gap.

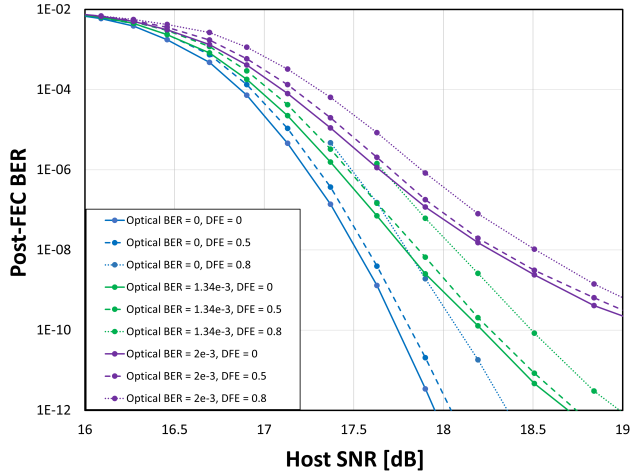


Fig. 5. Host SNR vs. post-FEC BER for multi-part links with different module-to-module BER levels and different electrical channels.

This analysis allows us to determine the required host SNR to achieve an acceptably low post-FEC BER for each system considered. Without our platform, these results could not possibly have been produced in a reasonable amount of time. This platform is also useful for system designers to compare candidate architectures for 200Gb/s systems. For example, the simulations shown in Figure 5 can easily be rerun with the convolutional interleaver turned off, and the resulting decrease in performance can be weighed against the improvement in latency and power consumption.

## VI. Conclusion

We present an FPGA-accelerated platform for post-FEC BER analysis of 200 Gb/s wireline systems. Our platform provides a significant speed increase over time-domain software simulations, allowing for demonstration of BERs down to the $10^{-12}$ level with reasonable computation time. It also allows for precise modelling of complex 200 Gb/s architectural choices, which existing statistical models cannot provide. This platform can serve as a tool for wireline system designers and the IEEE standard working group to quantify the performance of different architectural choices under various channel conditions. The platform can easily be scaled up with more FPGA resources to achieve BER validation down to $10^{-15}$ levels at a much lower cost than parallel software simulations.

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