448G/Lane Modulation & FEC

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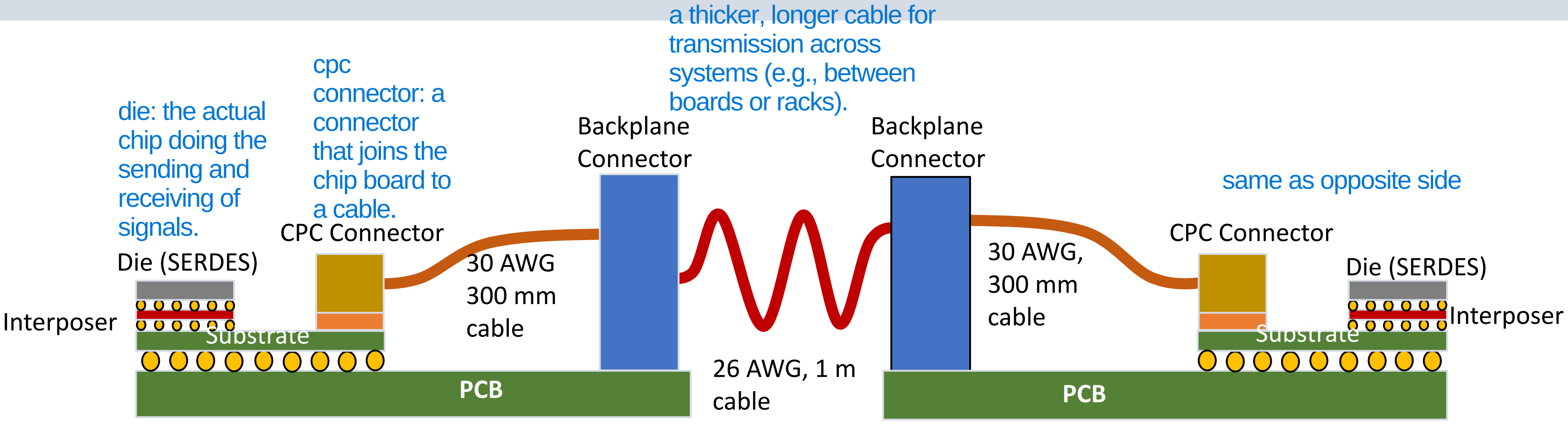
OUTLINE

- 448G/Lane Simulations
  - Channel Models
  - Simulation Results with PAM
  - Bidirectional Signaling
- New FEC Proposal
  - 2D RS FEC Results (Under Burst Error)
  - Complexity and Latency Analysis
- Conclusion (Summary and Future Work)

448G/Lane Channel Model



MTIA Package Substrate + Interposer

meta package for mounting the chip

IEEE Channels standardized test channels

- shah_e4ai_02_250430_25dB_RO_85G_XT_50dB
- shah_e4ai_02_250430_25dB_RO_85G_XT_55dB
- shah_e4ai_02_250430_25dB_RO_85G_XT_60dB
- shah_e4ai_02_250430_30dB_RO_85G_XT_50dB
- shah_e4ai_02_250430_30dB_RO_85G_XT_55dB
- shah_e4ai_02_250430_30dB_RO_85G_XT_60dB
- shah_e4ai_02_250430_35dB_RO_85G_XT_50dB
- shah_e4ai_02_250430_35dB_RO_85G_XT_55dB
- shah_e4ai_02_250430_35dB_RO_85G_XT_60dB
- tracy_efai_250430_DAC

green: acceptable | red: lossy

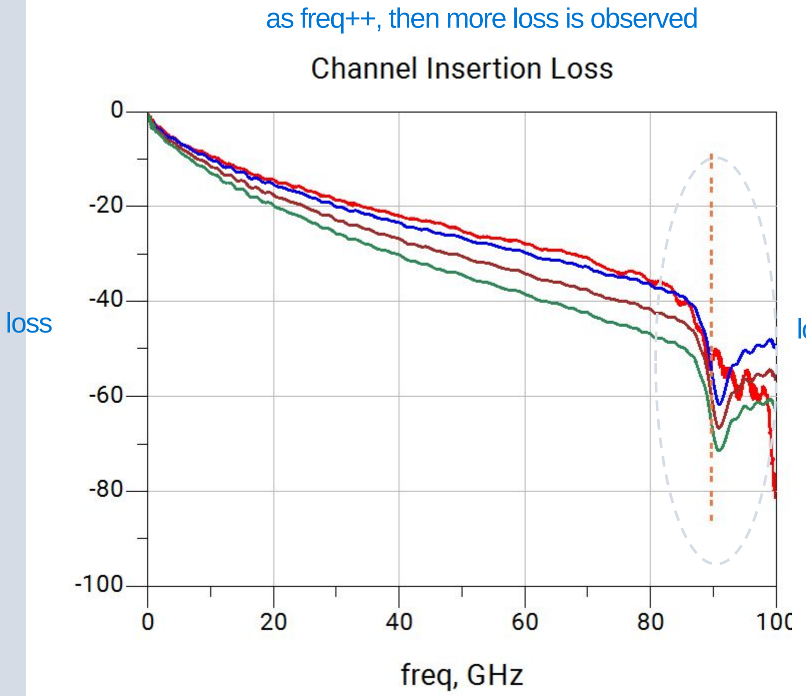
Package Substrate (~35 mm) + Interposer

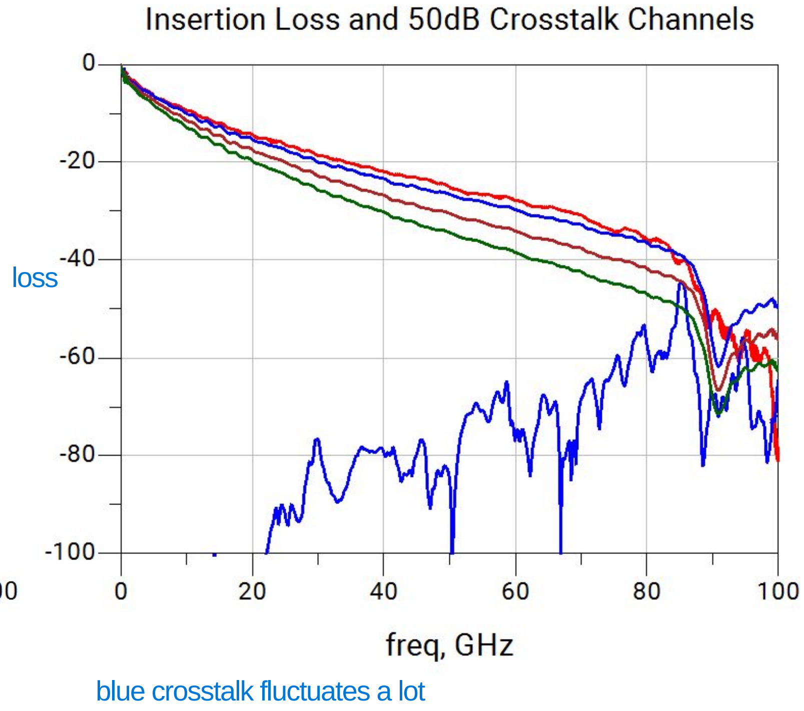
Limiting Factors:

- Channel Insertion loss
  Signal gets weaker as it travels through cables and connectors.
- Resonance/Roll-off within pass band
  Certain frequencies get distorted or attenuated inside the passband (where signals are supposed to travel clearly).
- High crosstalk (NEXT and FEXT)
  Signals from nearby wires interfere (like noise in a crowded room).

We acknowledge IEEE and connector vendor for kindly providing the channel models: https://www.ieee802.org/3/ad_hoc/E4AI/public/channel/index.html

S-Parameter Plots



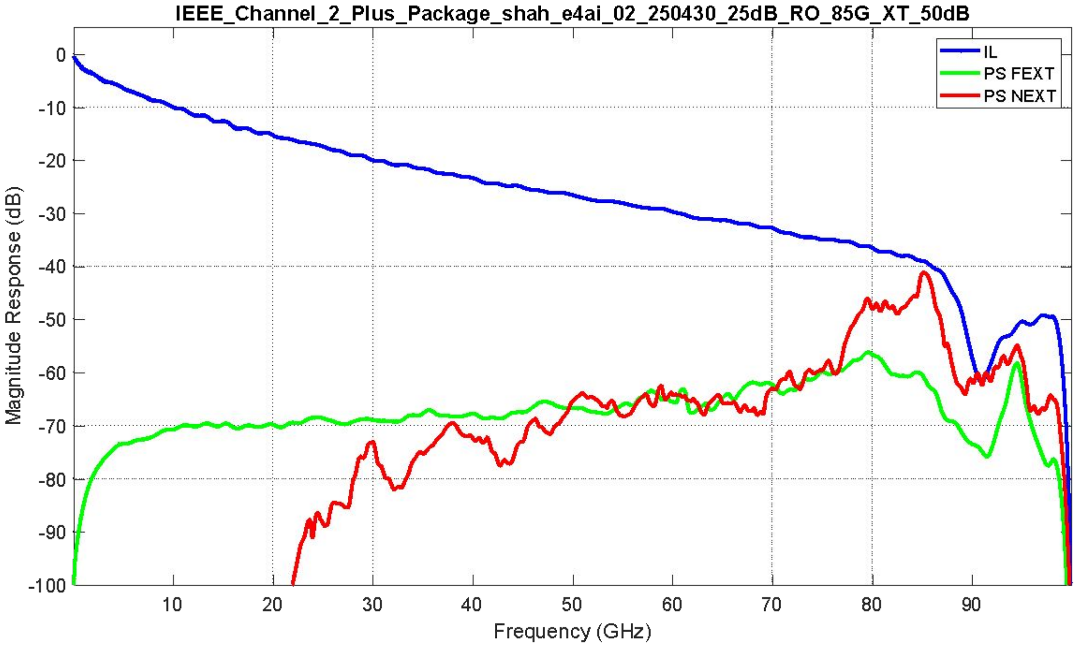


Ask from Industry:

- Provide SERDES Interposer + Package models
- Find ways to reduce crosstalk and eliminate resonance around Nyquist frequency

shah_e4ai_02_250430_25dB_RO_85G_XT_50dB + Package + Interposer

Channel Model Response



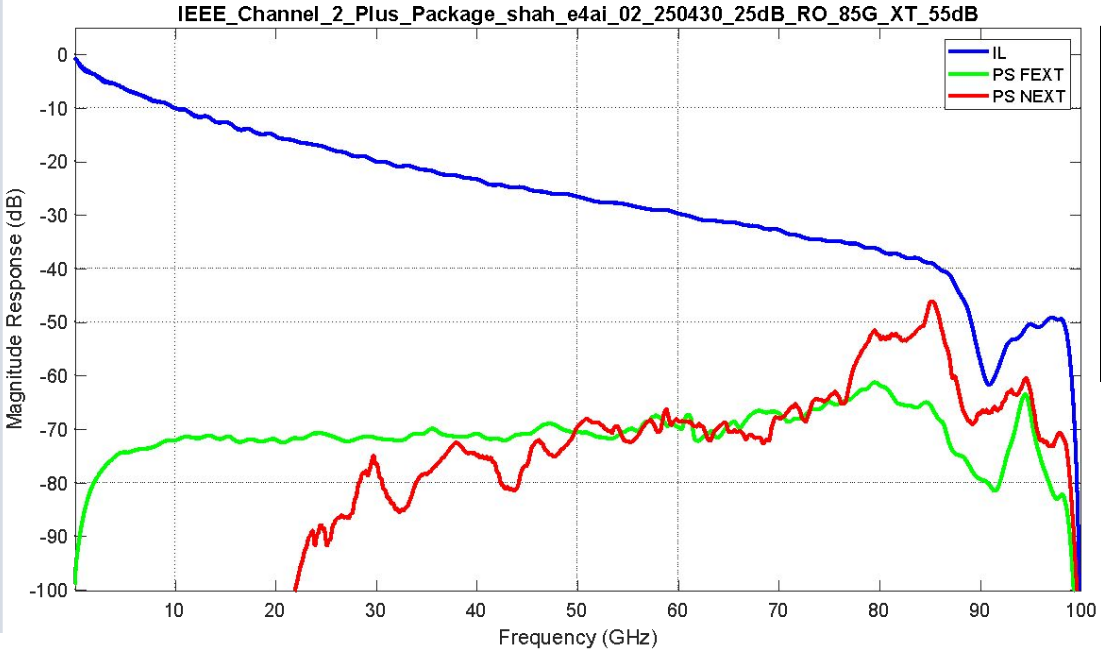
Performance Matrix

BWs (bandwidth)	PAM-6	PAM-6	PAM-8	PAM-8
Component BWs (GHz)	**90**	**100**	**75**	**100**
DAC SNR (dB)	41	41	41	41
Transmit SNR (dB)	31	31	31.8	31.7
ADC/DAC Jitter(fs)	50	50	50	50
CTLE Gain(dB) @ 0.8*BW	18	18	18	18
ADC SNR (dB)	43	43	43	43
Equivalent AFE SNR (dB)	33.2	33.3	33.6	34.1
Slicer SNR	23.1	23.4	25.9	26.4
SNR Margin (@1e-3)	3.0	3.3	3.4	3.9
DFE SER	3.1e-4	2.0e-4	6.4e-5	2.1e-5
MLSE SER	5.9e-6	5.9e-6	5.2e-6	4.3e-6

Metric Type	Indicates...	Importance
SNRs (DAC, TX, ADC)	Signal clarity	Fundamental to quality
Jitter	Timing accuracy	Can cause eye closure
CTLE Gain	High-frequency compensation	Fights channel loss
AFE/Slicer SNR	RX chain effectiveness	Determines bit reliability
SNR Margin	Link robustness	Indicates how "safe" you are
DFE/MLSE SER	Error performance after RX	Key for meeting spec targets

shah_e4ai_02_250430_25dB_RO_85G_XT_55dB + Package + Interposer

Channel Model Response

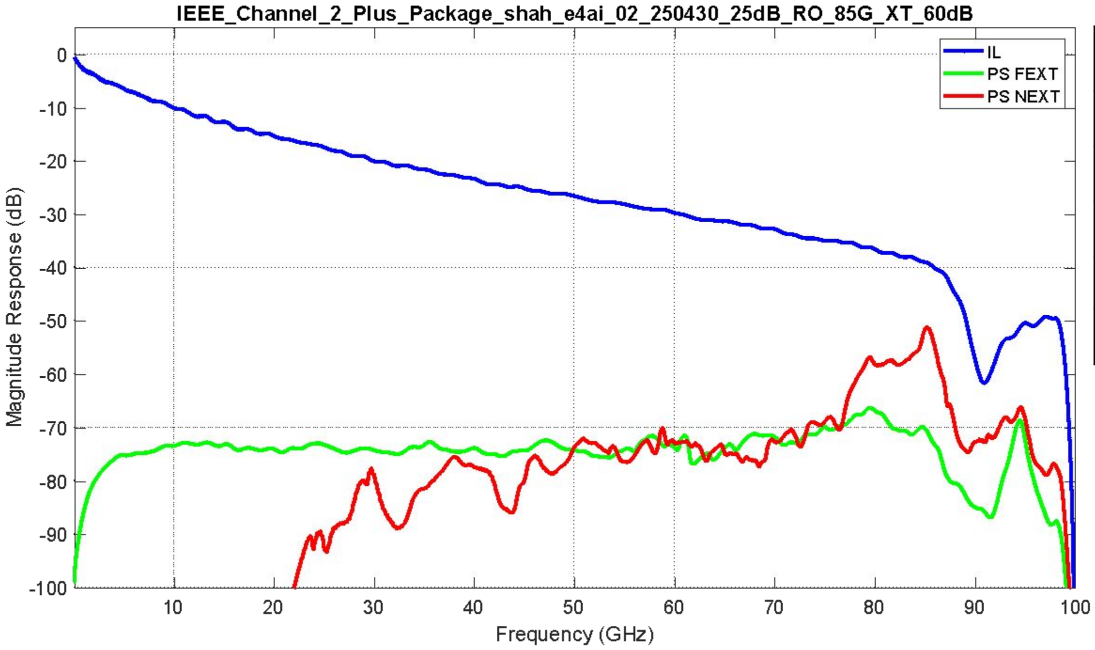


Performance Matrix

	PAM-6	**PAM-6**	**PAM-8**	**PAM-8**
Component BWs (GHz)	**90**	**100**	**75**	**100**
Slicer SNR	23.7	23.9	26.3	27.0
SNR Margin (@1e-3)	3.6	3.8	3.8	4.5
DFE SER	1.3e-4	8.1e-5	1.5e-5	3.3e-6
MLSE SER	3.0e-6	1.8e-6	3.6e-6	1.3e-6

shah_e4ai_02_250430_25dB_RO_85G_XT_60dB + Package + Interposer

Channel Model Response

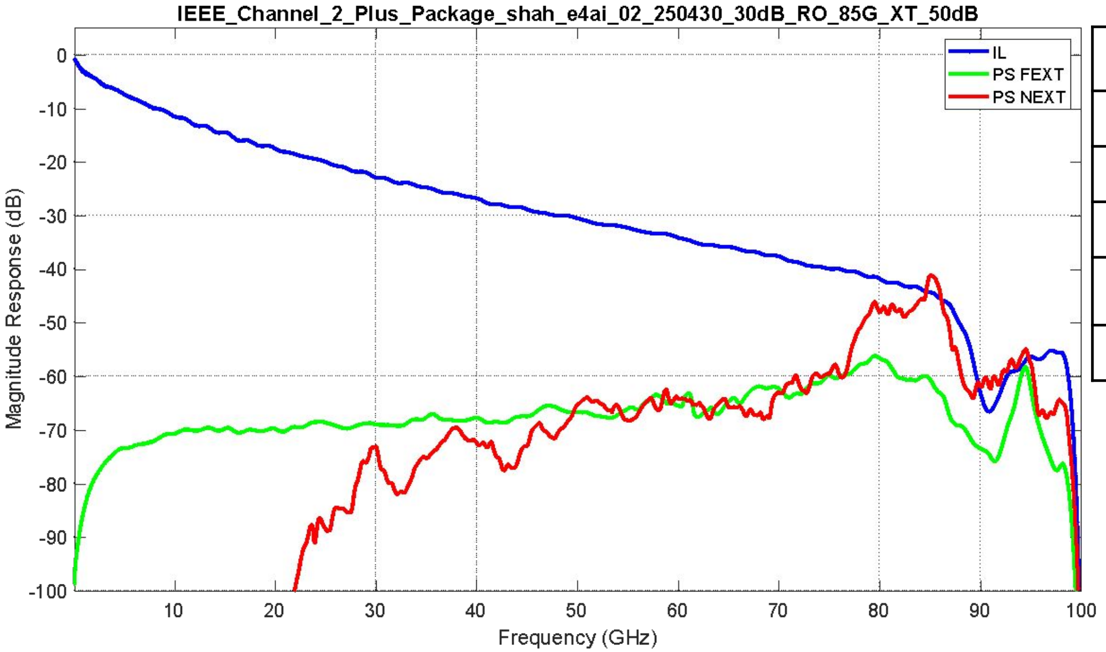


Performance Matrix

	PAM-6	PAM-6	PAM-8	PAM-8
Component BWs (GHz)	**90**	**100**	**75**	**100**
Slicer SNR	23.9	24.1	26.5	27.4
SNR Margin (@1e-3)	3.8	4.0	4.0	4.9
DFE SER	1.1e-4	7.1e-5	1.08e-5	< 1.0e-6
MLSE SER	1.8e-6	2.3e-6	2.20e-6	< 1.0e-6

shah_e4ai_02_250430_30dB_RO_85G_XT_50dB + Package + Interposer

Channel Model Response

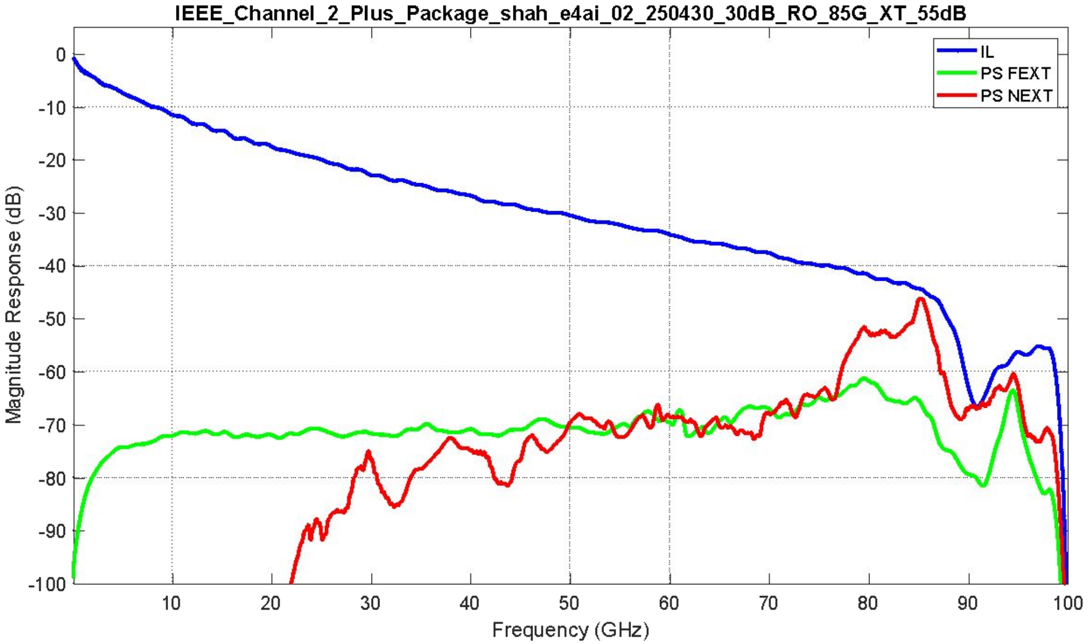


Performance Matrix

	PAM-6	PAM-6	PAM-8	PAM-8
Component BWs (GHz)	**90**	**100**	**75**	**100**
Slicer SNR	20.0	20.2	24.3	24.4
SNR Margin (@1e-3)	-0.1	0.1	1.8	1.9
DFE SER	6.9e-3	5.9e-3	1.6e-3	1.2e-3
MLSE SER	6.7e-4	4.8e-4	4.7e-5	3.4e-5

shah_e4ai_02_250430_30dB_RO_85G_XT_55dB + Package + Interposer

Channel Model Response

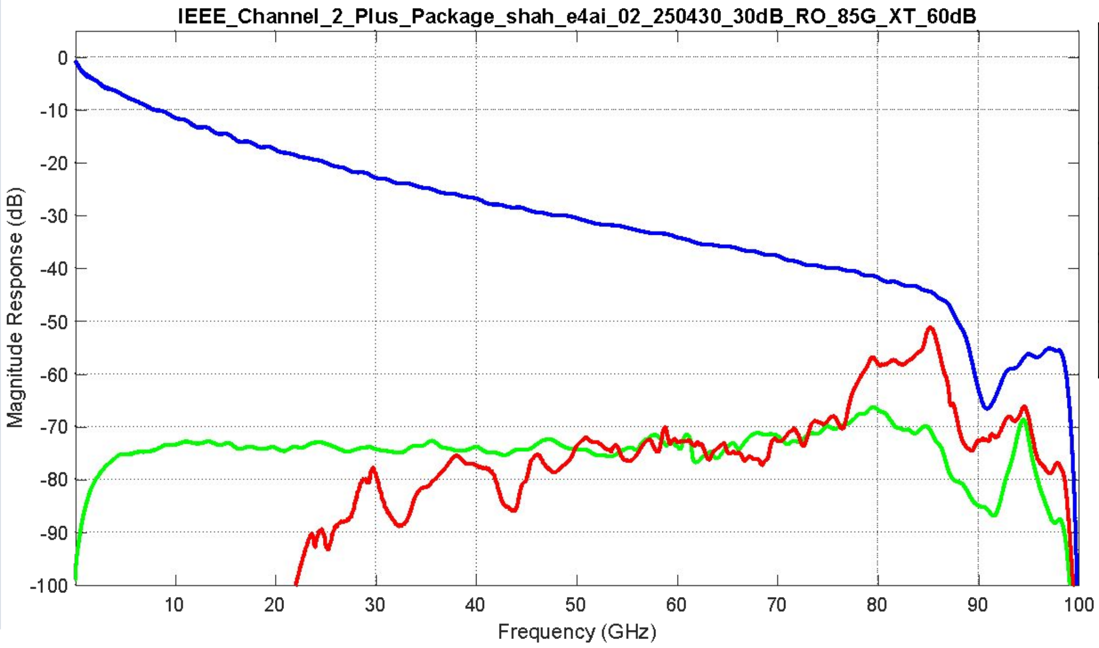


Performance Matrix

	PAM-6	**PAM-6**	**PAM-8**	**PAM-8**
Component BWs (GHz)	**90**	**100**	**75**	**100**
Slicer SNR	21.4	21.7	24.9	25.3
SNR Margin (@1e-3)	1.3	1.6	2.4	2.8
DFE SER	2.2e-3	1.7e-3	4.7e-4	1.8e-4
MLSE SER	9.6e-5	9.0e-5	1.6e-5	1.1e-5

shah_e4ai_02_250430_30dB_RO_85G_XT_60dB + Package + Interposer

Channel Model Response

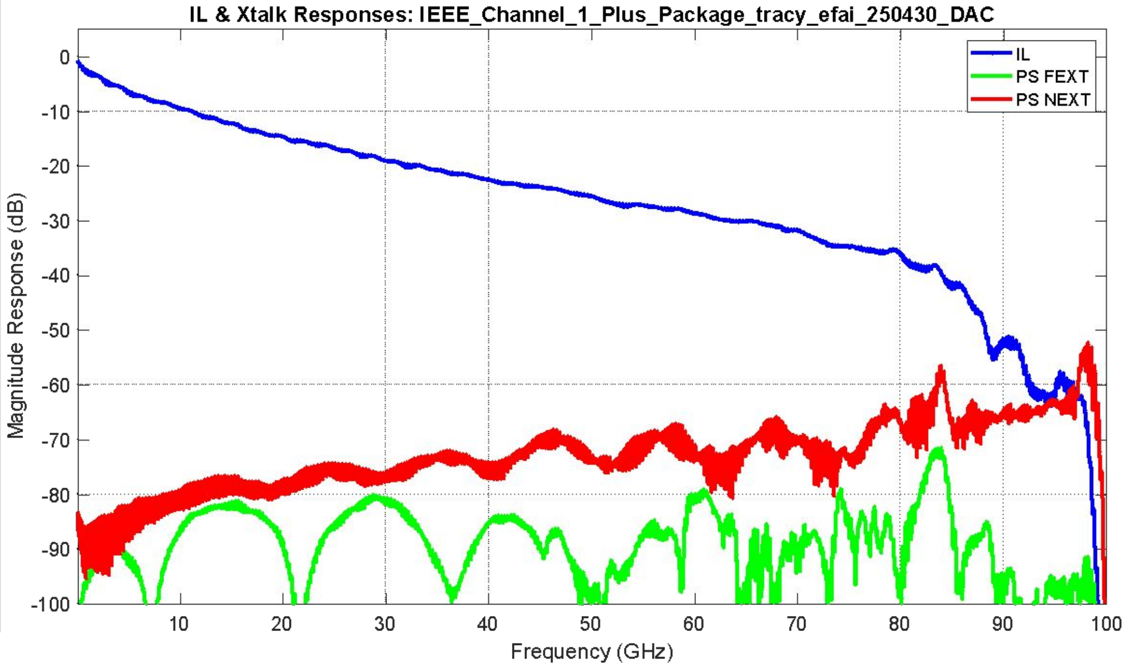


Performance Matrix

	PAM-6	PAM-6	PAM-8	PAM-8
Component BWs (GHz)	**90**	**100**	**75**	**100**
Slicer SNR	21.9	22.3	25.1	25.7
SNR Margin (@1e-3)	1.8	2.2	2.6	3.2
DFE SER	1.5e-3	8.6e-4	3.3e-4	4.8e-5
MLSE SER	5.7e-5	3.0e-5	1.4e-5	7.6e-6

Channel: tracy_efai_250430_DAC + Package + Interposer

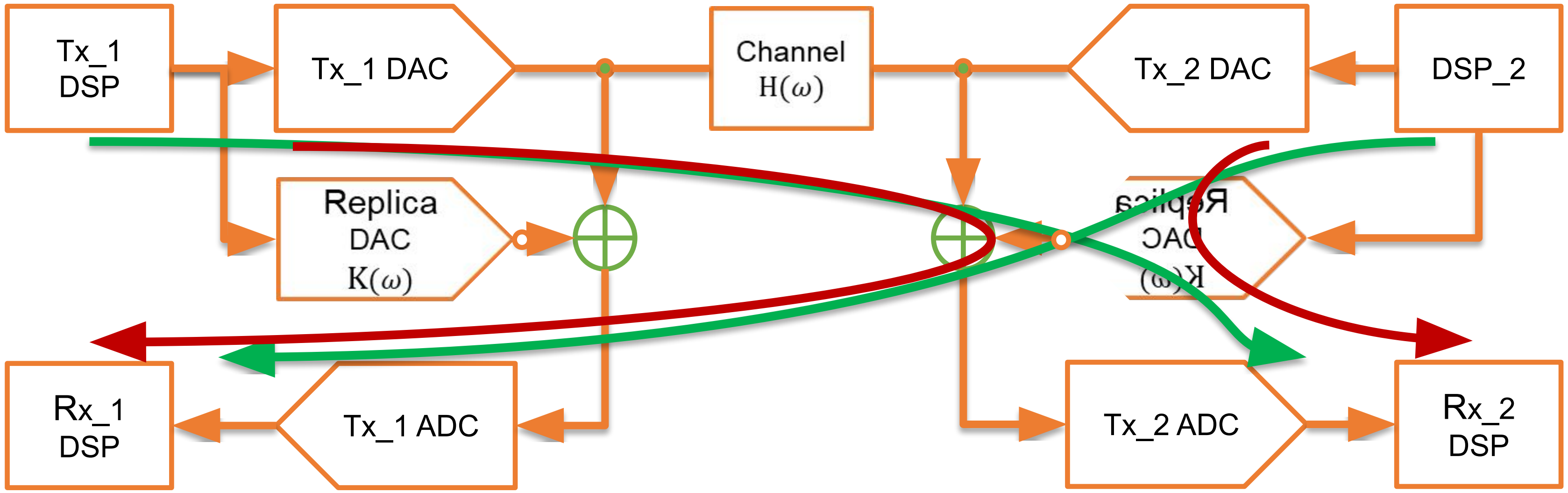
Channel Model Response



Performance Matrix

	PAM-6	PAM-6	PAM-8	PAM-8
Component BWs (GHz)	**90**	**100**	**75**	**100**
Slicer SNR	22.1	22.2	25.1	25.8
SNR Margin (@1e-3)	2.0	2.1	2.6	3.3
DFE SER	1.1e-3	9.6e-4	2.8e-4	3.1e-5
MLSE SER	2.7e-5	2.3e-5	1.4e-5	8.7e-6

Bidirectional Signaling (2x224G PAM-4)



- Received Signal:

$$rx_1(t) = tx_1(t) * \left(1 - k(t)\right) + tx_2(t) * h_{21}(t)$$

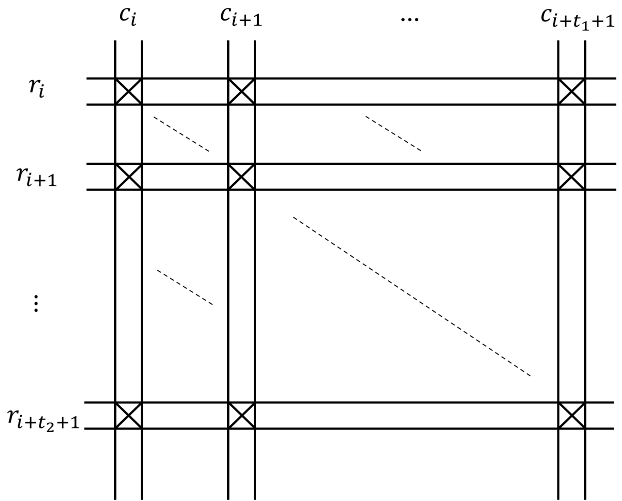
- Ideal Hybrid → Only Tx_2 signal remains as if unidirectional transmission
- Not be the case in practice :
- Non-ideal Hybrid
- Additional Reflections from the channel (S_{11}) and other side

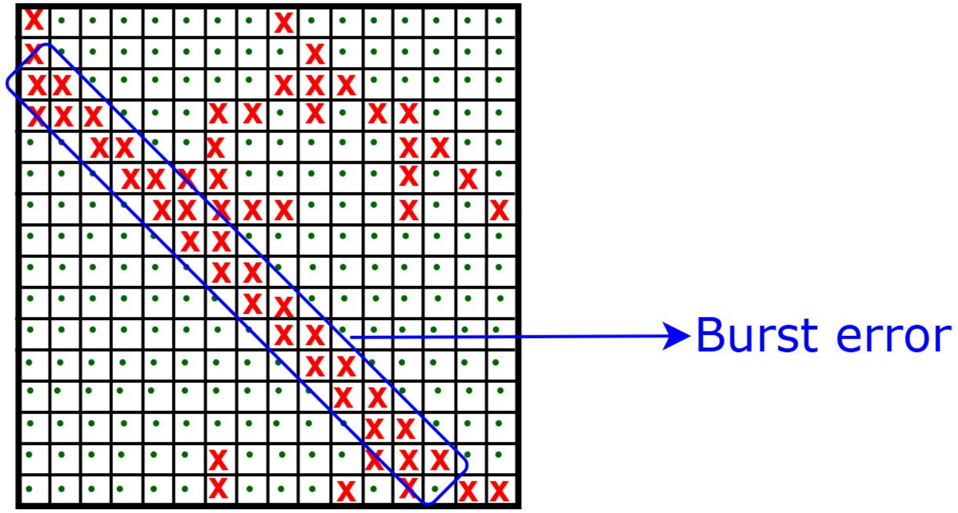
- Due to high insertion loss, TX noises limits the performance, unlike RX-limited unidirectional systems

		Pessimistic	Expected	Optimistic
	Cancellation Level (dB)	10	20	30
	Bandwidth Mismatch (GHz)	10	5	3
	SNR Correlation Coeff	0.5	0.7	0.9
	Jitter Correlation Coeff	0.5	0.7	0.9
224G Channel →	~ Slicer SNR Margin (dB)	-6.4	-3.3	2.1
tracy_efai_250430_DAC + Package →	~ Slicer SNR Margin (dB)	-0.5	1.6	5.0
shah_e4ai_02_250430_25dB_RO_85G_XT_60dB+ Package →	~ Slicer SNR Margin (dB)	-1.2	1.0	4.6

New FEC Proposal

- 2D Codes are both simple and powerful, especially for constructing very long block codes from smaller, more manageable components
- Iterative Decoding
  - Each bit/symbol is encoded by two component codewords
  - Decode rows and columns alternatingly
- Example:
  - Assume a two-error correcting component code
  - A lot more than 2 errors in a row/ column can be corrected by iterative decoding
- Minimum undecodable pattern $(t_1+1)x(t_2+1)$





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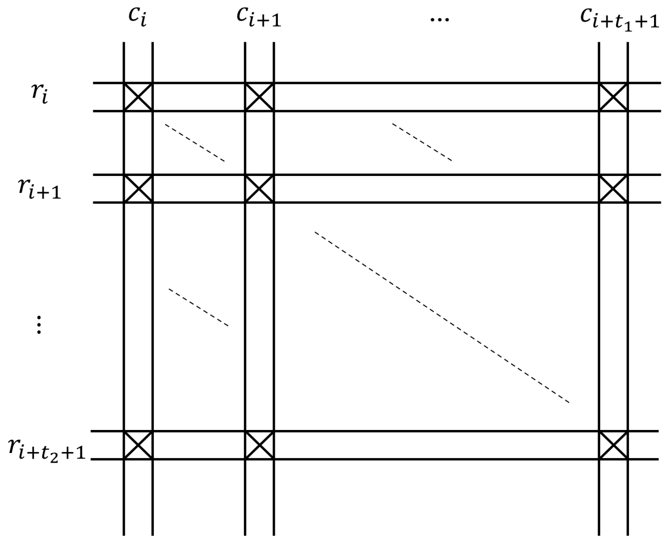
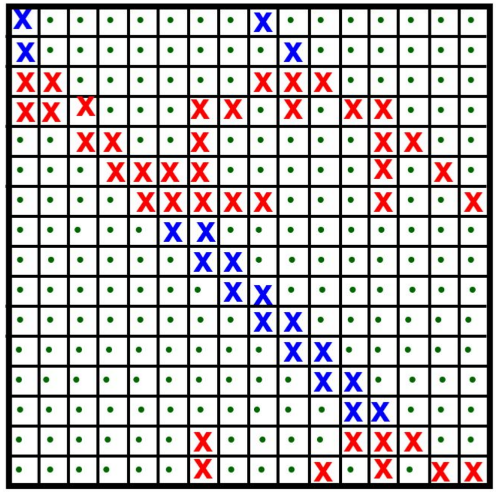


1st iteration →



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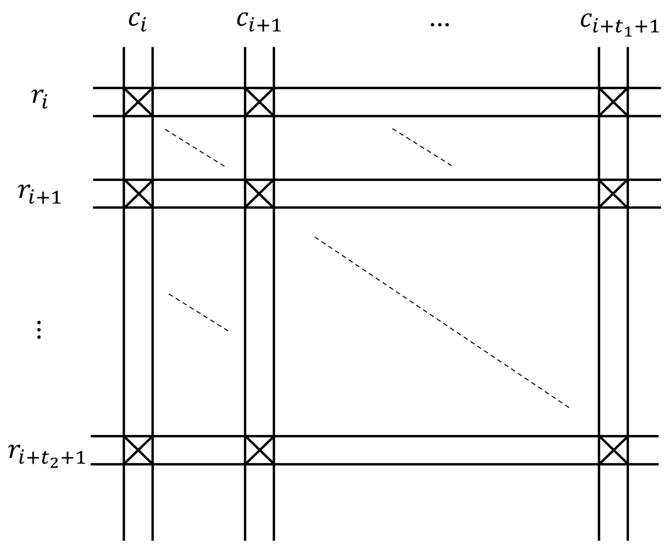
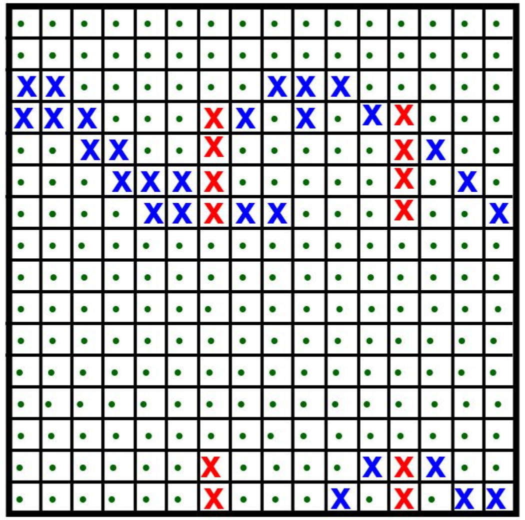


2nd iteration



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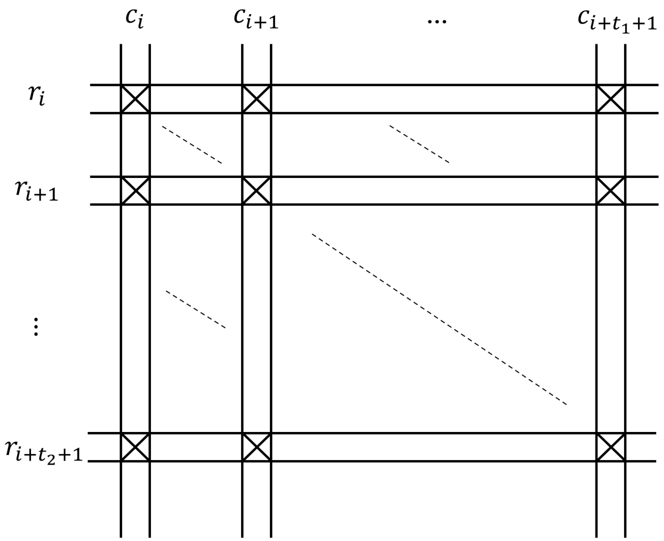
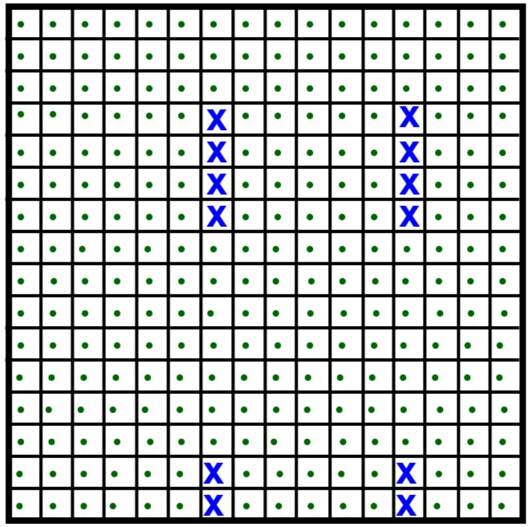
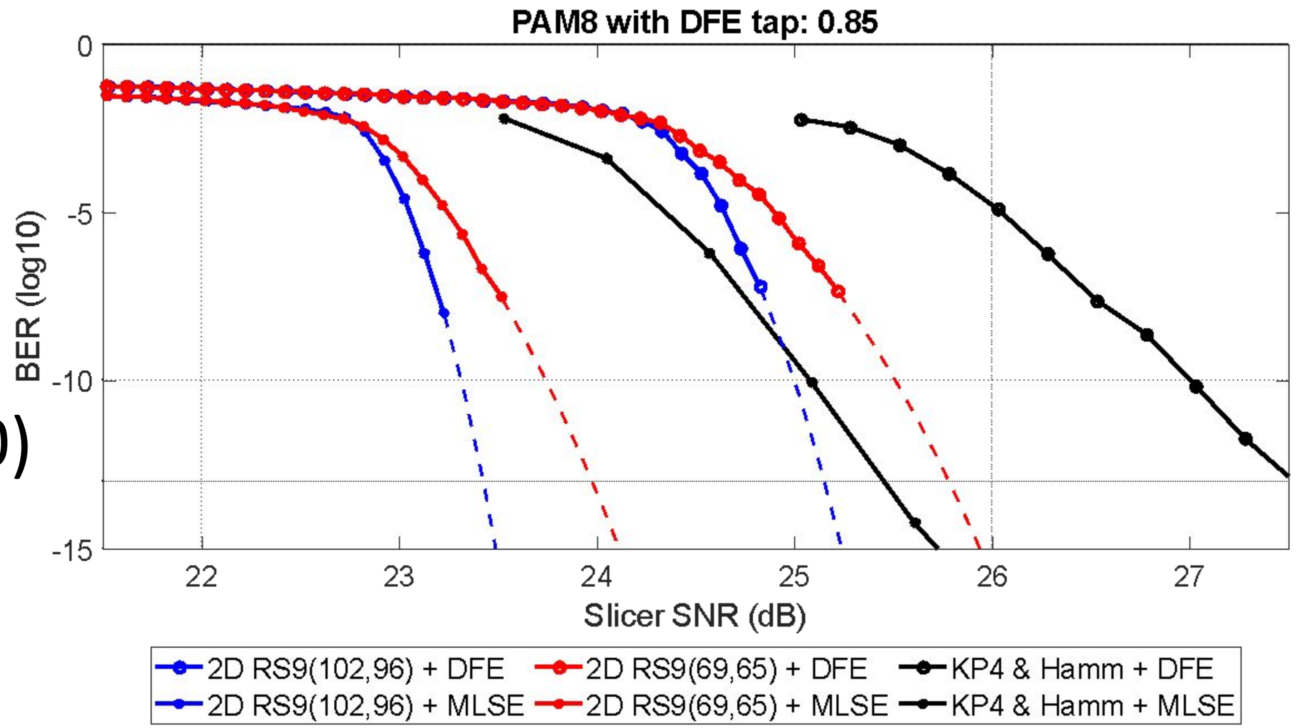


3rd iteration →



New FEC Proposal

- 2D RS FEC : RS Component Codes with t=2 or t=3
- >1.5 dB gain with RS9(69,65) >2 dB gain with RS9(102,96) with respect to RS10(544,514)+Ham.(128,120) (KP4+Hamming)



Complexity and Latency Analysis

- Total Complexity and Latency of some 2D-RS codes at 1.6T PCS wrt KP4

	RS9(69,65)		**RS9(102,96)**	**RS10(544,514) – KP4 (+Hamming)**
	Lower Complexity (8 iterations)	Lower Latency (6 iterations)		
Overhead (OH)	%12.68		%12.89	%5.84 (%12.89)
Total LUT Utilization(FPGA)	100 K	181K	171K	171K(*)
Total Latency(ns)	339.8	201	673.3	83.2(*)
SNR Gain wrt (KP4+Hamming) @10^{-15} BER	1.8	1.7	2.3	0

(*)Additional complexity & latency due to Hamming Code

- High latency due to iterations can be decreased with further optimizations such as:
  - Increase the complexity to a level equivalent to current KP4 for 2D-RS codes
  - Incremental computation of syndromes for subsequent iterations
  - Number of iterations can be decreased with marginal performance penalty

Conclusion

- With the current package and channel models PAM6, PAM8 or bidirectional are feasible options
  - Bidirectional need more analog models for hybrid subtractor
- Need more improvement on channel and xtalks
  - Need more package models
- FEC with more coding gain than KP4(+Hamming) => 2D RS Codes
  - Minimal additional latency: > 1.5 dB coding gain
  - Same complexity: >2 dB coding gain
- Working on alternative decoding strategies for 2D RS codes to lower complexity

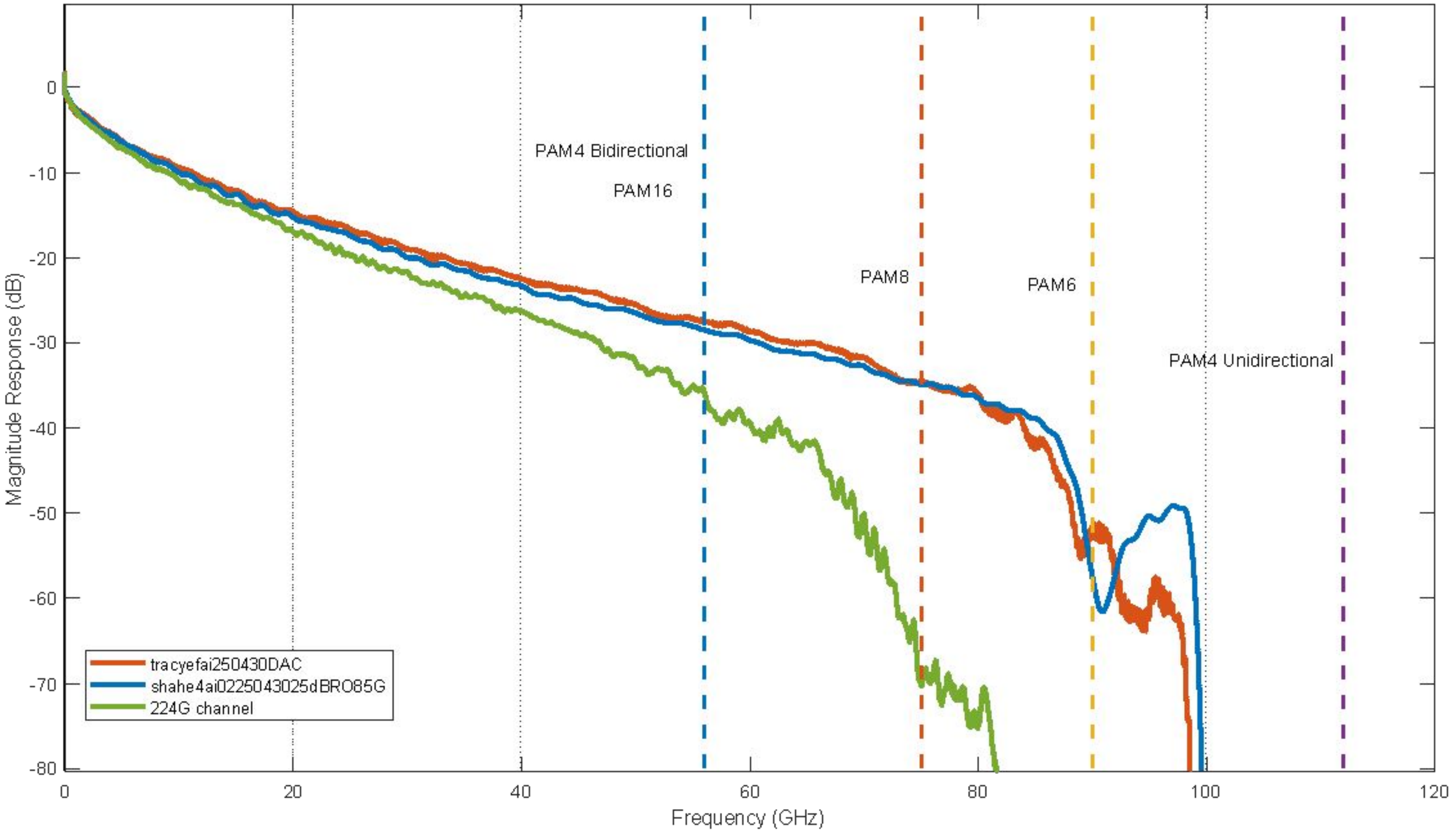
Thank You!

Meta

Back-up Slides

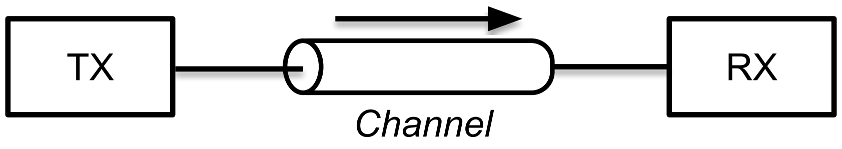
Meta

Channels



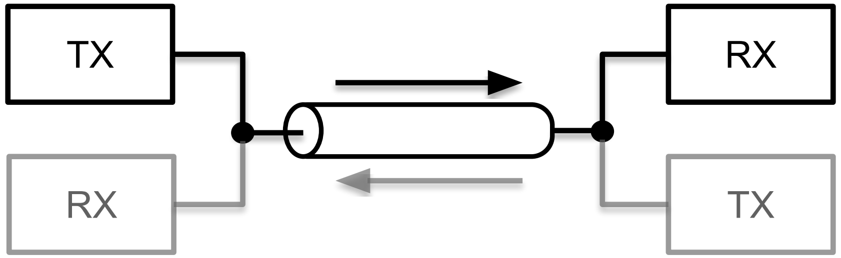
PAM4 Bidirectional
PAM16
PAM8
PAM6
PAM4 Unidirectional
Magnitude Response (dB)
Frequency (GHz)
0
-10
-20
-30
-40
-50
-60
-70
-80
0
20
40
60
80
100
120
tracyefai250430DAC
shahe4ai0225043025dBRO85G
224G channel

Communication Topologies



Uni-Directional Transmission

- Higher Bandwidth
  - Higher Insertion Loss
  - Increased Crosstalk Interference
- Higher Modulation Order
  - Increased SNR Penalty
- One-Way Communication
  - Simple RX Design
  - More Signal Power



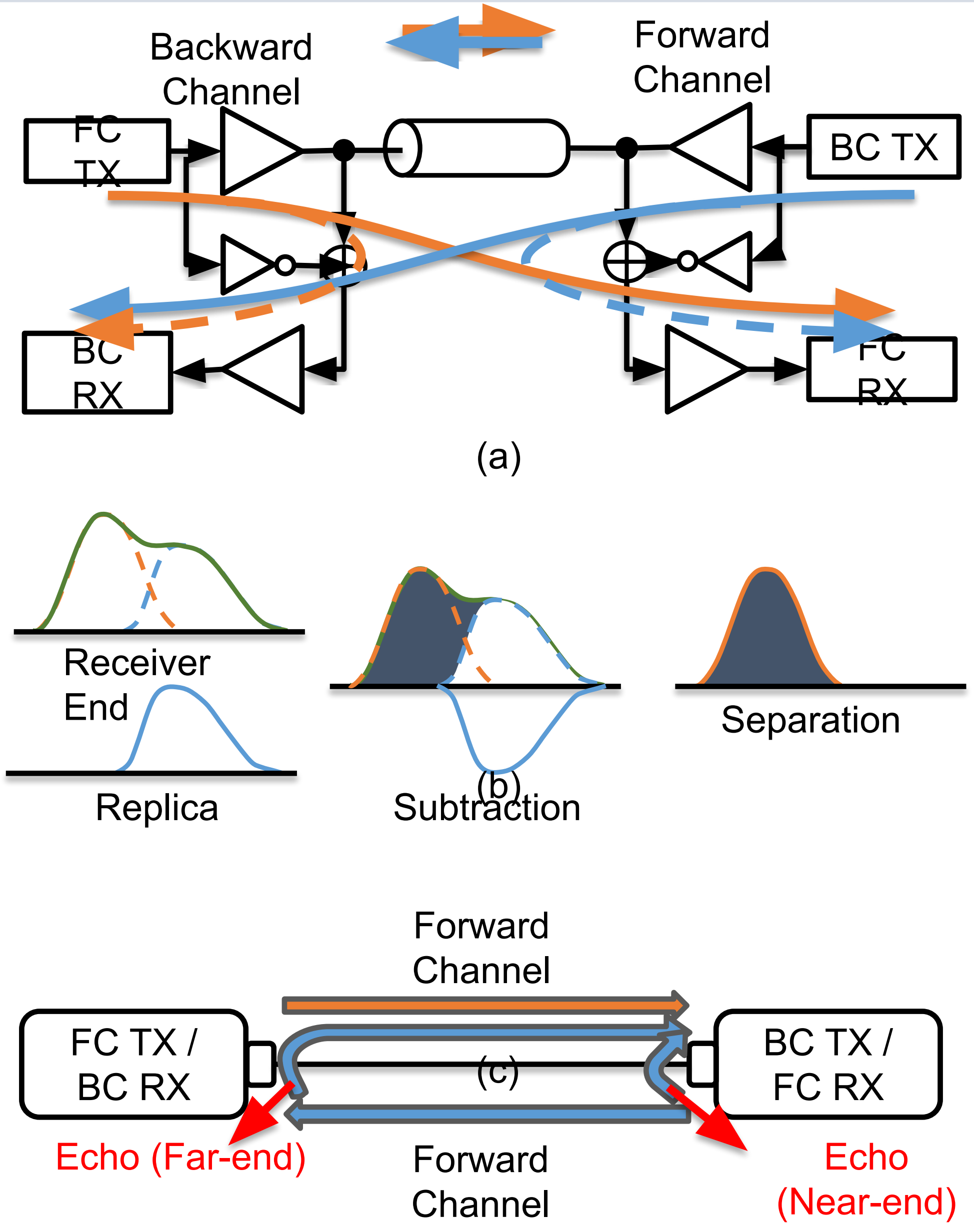
Simultaneous Bi-Directional Transmission

- Same Bandwidth
  - No Extra Loss
  - No Extra Crosstalk Interference
- Same Modulation Order
  - Same SNR Requirements
- Two-Way Communication
  - Complex RX Design with additional components
  - Very high interference

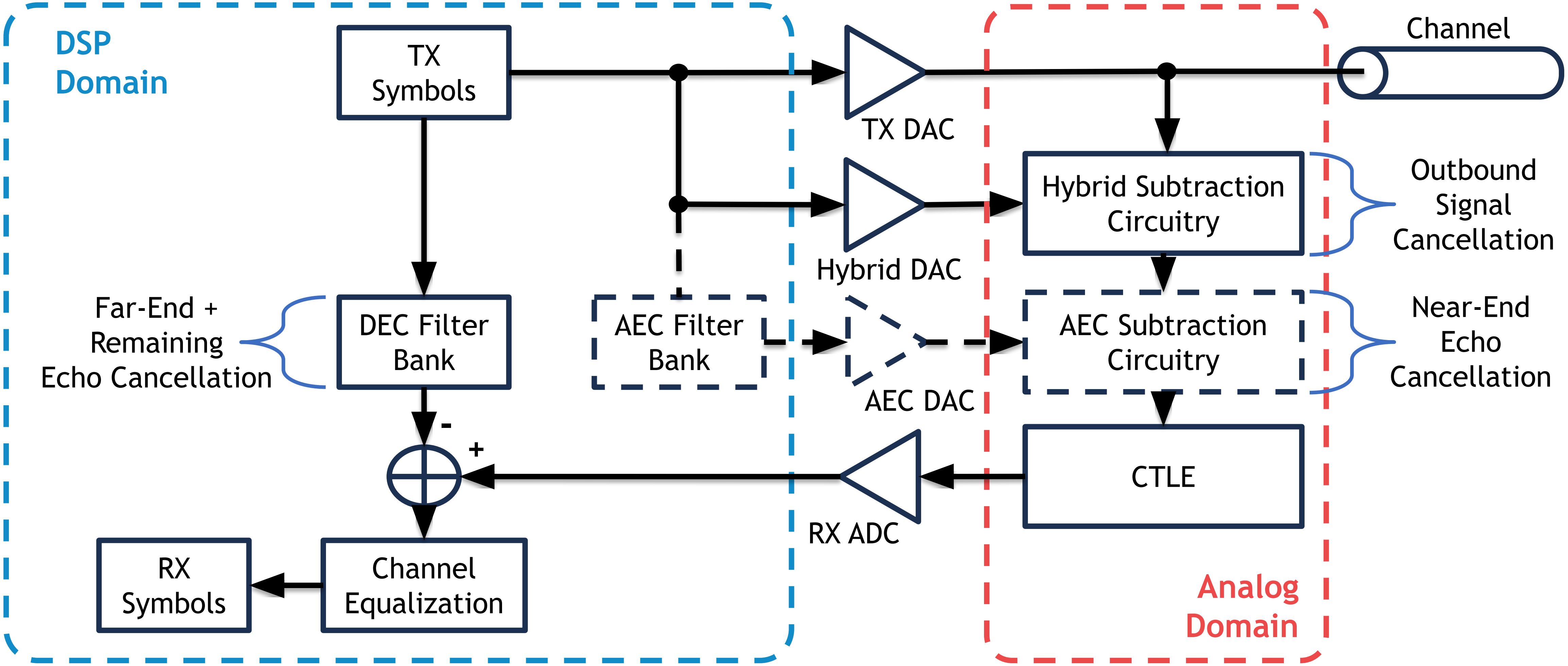
Channel Model and Additional Components

Major Differences over Uni-Directional Channel

- Overlap of Desired Inbound Signal and Very Strong Outbound Signal: Figure (a)
  - Solution: Hybrid Circuitry for cancellation by subtraction of overlapped signal: Figure (b)
  - To utilize dynamic range of ADC better
  - Requires a Replica Driver
- Echoes of Outbound Signal: Figure (c)
  - Analog Echo Cancellation (AEC)
    - Strong Near-End Echo ($\propto S_{11}$ of Channel)
  - Digital Echo Cancellation (DEC)
    - Weak Far-End Echo ($\propto S_{12}$ & S_{21} of Channel)

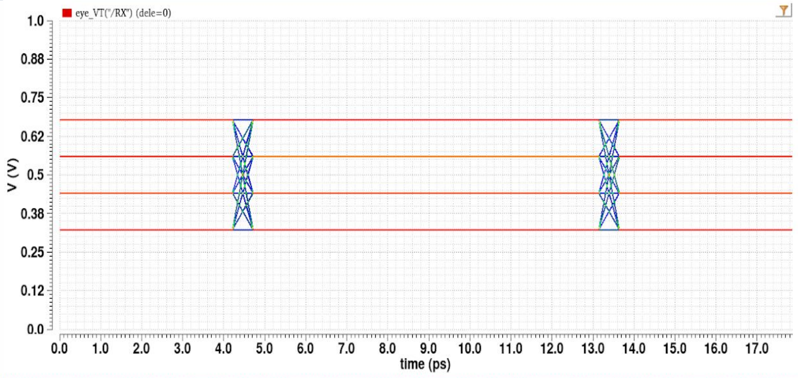


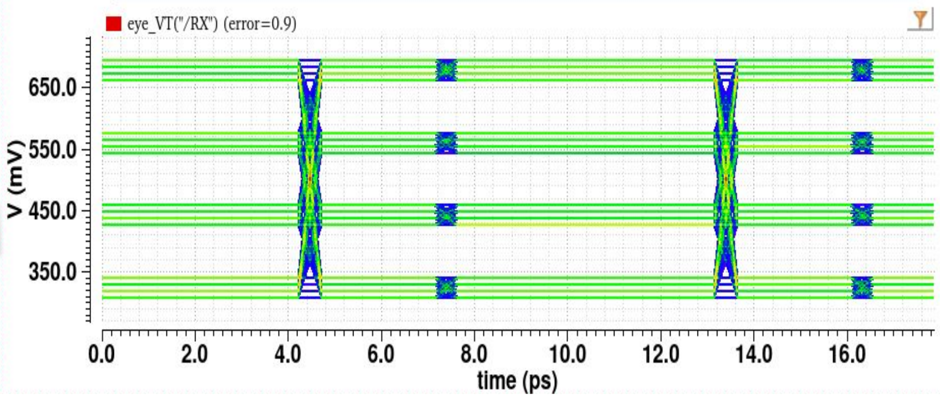
Simple Block Diagram of SBT (Single Side)



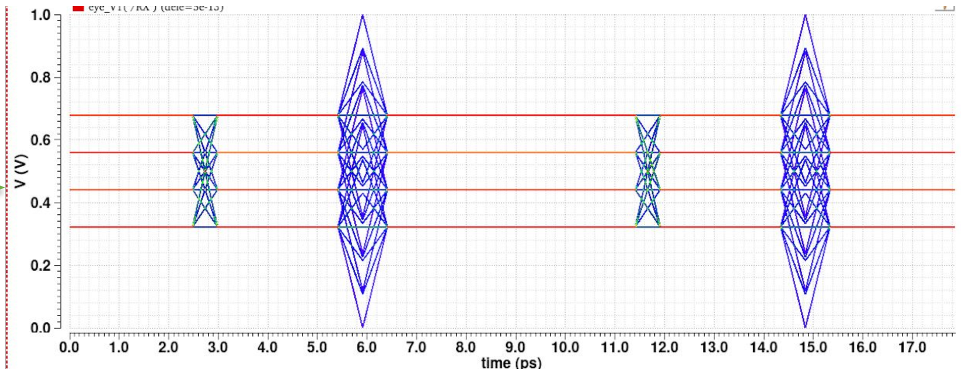
TX - Replica Imperfections

Eye Diagram of Perfectly Matched Replica and Tx DAC

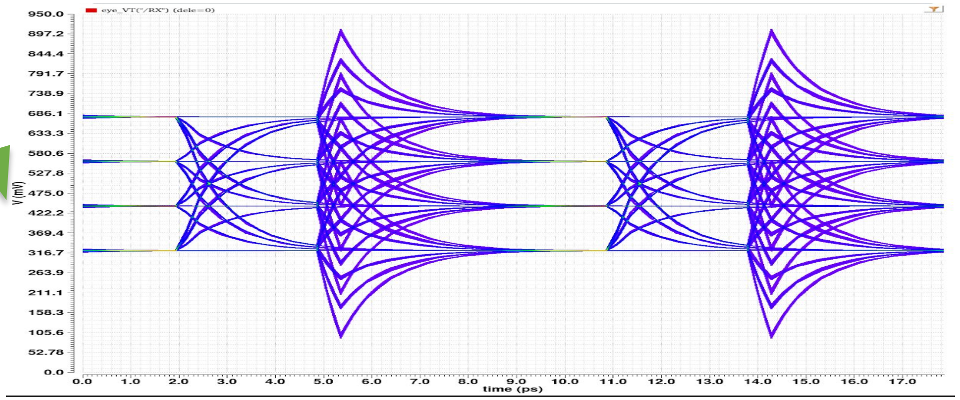




1. Gain Mismatch
   - Commonmode Changes
   - Can be easily calibrated



2. Phase Mismatch
   - Degrades eye performance
   - Calibration required



3. Bandwidth Mismatch
   - Same effect on eye as phase mismatch
   - Broadband calibration required

There will be additional insertion loss depending on the Hybrid design!