An FPGA-Accelerated Platform for Post-FEC BER Analysis of 200 Gb/s Wireline Systems

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***Abstract*—As wireline communication links transition from 100 Gb/s to 200 Gb/s per lane, new and complex forward error correction (FEC) architectures have been adopted to achieve acceptably low bit error rates (BERs). Understanding how these architectures impact link performance under various channel conditions is essential. This brief presents a flexible platform for field-programmable-gate-array (FPGA)-accelerated time-domain simulations. The platform is capable of modeling wireline systems relevant to the upcoming 200 Gb/s Ethernet standard including multi-part links, concatenated FEC codes with convolutional interleaving and soft-decision inner-FEC decoding. This FPGA platform can accurately demonstrate post-FEC BERs at the 10^{-11} level within a day of simulation time, a speed improvement by a factor of 10,000 over software-based simulation platforms.**

***Index Terms*—BER, concatenated FEC, convolutional interleaving, ethernet, FPGA, multi-part link, pulse amplitude modulation (PAM), soft decision, 200Gb/s, wireline transceiver.**

I. Introduction

The demands for wireline interconnectivity in data centers are rapidly growing, driven by artificial-intelligence applications, video streaming, and cloud services. Multi-part links are typically employed for communication between and within data centers, consisting of a short electrical link from a transmitting host chip on a server to an optical module, followed by a long optical link to reach another module, with another short electrical link connecting to the receiving host chip. All three links along the data path can introduce bit errors. Electrical links have large amounts of inter-symbol interference (ISI), requiring equalization techniques such as decision feedback equalization (DFE) or maximum-likelihood sequence detection (MLSD) to recover the signal. Both DFE and MLSD suffer from error propagation, which causes the errors from electrical links to be predominantly bursts of correlated errors [1, 2]. In optical links, correlated errors may also be present, but the errors are predominantly random [3]. For high-speed wireline systems, FEC is necessary to achieve acceptably low BERs. However, understanding and optimizing FEC performance in the presence of complex error dynamics across electrical and optical links remains an open challenge.

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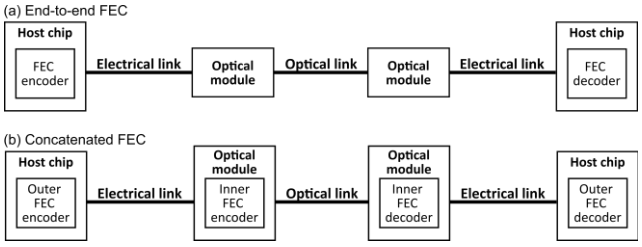

Fig. 1. System-level FEC architectures for multi-part links [5]: (a) End-to-end FEC (b) Concatenated FEC.

For 100 Gb/s communication, a typical end-to-end FEC architecture uses the Reed-Solomon KP4 FEC code [4], shown in Fig. 1(a). The KP4 FEC code is a strong, non-binary linear block code that operates on 10-bit-long FEC symbols. Any 544-FEC-symbol-long codewords with more than 15 FEC-symbol errors are uncorrectable and contribute to the BER after FEC decoding (post-FEC BER).

The next generation of wireline links will operate at 200 Gb/s. Doubling the data rate degrades signal integrity, necessitating a stronger FEC architecture to achieve acceptable post-FEC BERs. To address this, the IEEE 802.3dj task force has adopted a concatenated FEC (CFEC) architecture [6] that includes an additional inner code protecting the optical link, shown in Fig. 1(b). The inner code, a binary Hamming code, can correct one bit error per 128-bit codeword and is effective against the random errors produced by optical links due to its low implementation complexity. Convolutional interleaving (CI) [7] and soft-decision decoding [8] can further improve the inner FEC's performance, making it more robust to correlated errors. The outer code is the same KP4 code used in 100 Gb/s links. Understanding how these architectures affect a system's post-FEC BER is essential for the IEEE 200 Gb/s standard to set pre-FEC BER allocations that balance latency and power consumption.

Two main approaches exist for estimating the post-FEC BER of a wireline system. One approach is to use a software-based time-domain simulation. Unfortunately, software simulations demonstrating BERs below 10^{-12} are prohibitively time-consuming [9]. Various extrapolation methods are also used in industry to estimate the post-FEC BER from a short time-domain simulation. However, the extrapolation can be inaccurate as the correlation between SNR and post-FEC BER may change at lower BERs [9]. A second approach is to use a statistical model to analytically determine post-FEC BERs [9-11]. While statistical models can quickly determine arbitrarily low BERs, they are limited by architectural complexity. For example, a statistical model for concatenated FEC codes is proposed in [11], but it cannot capture the complex interleaving and symbol multiplexing schemes in

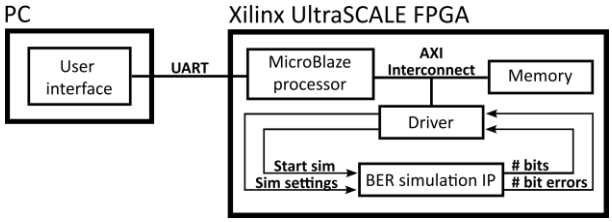

Fig. 2. Proposed FPGA-accelerated simulation platform [5].

200 Gb/s systems. A time-domain FPGA platform presented in [12] did not report BERs lower than 10^{-7}.

The work demonstrated in this brief is an extension of the previous work we reported in [5], where a parallelizable FPGA platform shown in Fig.2 was proposed for 200 Gb/s wireline systems. Each key building block in this FPGA model such as channel model, equalizers, concatenated FEC, block interleaver and 1/(1+D) precoding have been validated with the statistical model proposed in [9-11]. In this work, we discuss the modeling of CI and soft-decision inner-FEC decoding extensively. These two techniques are in the 200 Gb/s wireline standards to minimize the miscorrection caused by the inner-FEC decoding.

In this brief, Section II presents the high-level architecture of the proposed wireline transceiver model. In Section III, the inner-FEC code and convolutional interleaver are introduced. Section IV presents the Chase algorithm for soft-decision inner FEC decoding and the generation of soft channel outputs. Section V presents a case study where a multi-part 200 Gb/s wireline system is modeled. Section VI concludes this brief.

II. Wireline Transceiver Model

This section presents the transceiver model on the FPGA platform. Fig. 3(a) shows the block diagram of an ideal PAM-4 transceiver model with an additive-white-Gaussian-noise (AWGN) channel, and Fig. 3(b) shows its hardware implementation on the FPGA. The PAM-4 symbols b_k are mapped to the transmitted signal levels t_k^{bin} in an m-bit signed decimal representation. The superscript "bin" denotes that is the FPGA platform's binary representation of the analog signal level t_k. The Gaussian noise samples n_k^{bin} are then added to t_k^{bin}. The signal is clipped to maintain the m-bit resolution for the received noisy samples r_k^{bin}. With an appropriate choice of signal resolution, this signal clipping does affect the PAM-4 symbol error rate or the post-FEC BER. An ideal slicer at the receiver outputs the most likely transmitted data sequence, d_k.

The programmable parameter m controls the number of bits representing the analog signal. Increasing m produces a finer resolution that may match better to a statistical or software model that assumes a floating-point representation of analog signals. However, increasing m comes at the cost of additional hardware complexity. A difference between this model and a real 200 Gb/s receiver is that the FPGA platform has no analog-to-digital converter (ADC). Instead, the resolution m is assumed to be the same as the ADC resolution of interest. In this way, the same signal resolution can be used throughout the model, minimizing hardware complexity. An 8-bit signal resolution is chosen for a realistic ADC resolution in a 200 Gb/s receiver [13], hence $m = 8$ for all simulations in this work.

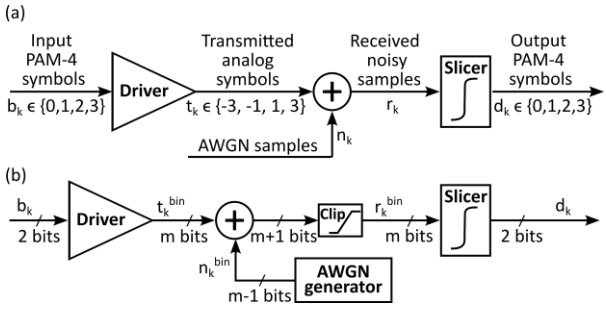

Fig. 3. (a) PAM-4 transceiver system model with AWGN (b) Its FPGA implementation.

There are multiple approaches for generating AWGN samples on an FPGA; for example, the Box-Muller method is commonly used [14]. However, this method is not well-suited for in-runtime programming of the noise variance, which is essential for the platform to efficiently sweep over a range of SNR levels. Instead, the AWGN generator on this FPGA platform uses a pre-computed, programmable look-up table containing the probability of each noise sample, and a 64-bit Tausworthe uniform random number generator (URNG) to randomly choose noise samples with the correct frequency [15]. By re-programming the look-up table, one can change noise variance, or even specify an arbitrary non-Gaussian distribution. Noise coloring can also be introduced by passing the noise samples through a desired filter response.

III. Inner FEC Code and Convolutional Interleaver

A. Shortened Hamming (68,60) Code

Since each Gray-coded PAM-4 symbol contains only up to one erred bit [9], the Hamming decoder can correct errors based on PAM symbols instead of bits. A new shortened (68,60) Hamming code has been adopted by the Ethernet standard for use with a soft-decision decoder that protects PAM-4 symbols rather than individual bits [16]. The (68,60) code is achieved by puncturing the extended Hamming (128,120) code in 60 places.

Fig. 4 shows the encoding and decoding of a shortened Hamming (68,60) codeword. In Fig.4 (a) the encoder takes sequences of 120 bits, denoted $u \in \mathbb{F}_2^{1\times 120}$, and computes codewords $c \in \mathbb{F}_2^{1\times 128}$. The notation $\mathbb{F}_2^{i\times j}$ refers to an i by j vector with entries from $\mathbb{F}_2$ (binary entries). To encode a message, two bits of each pair that form a PAM-4 symbol in the

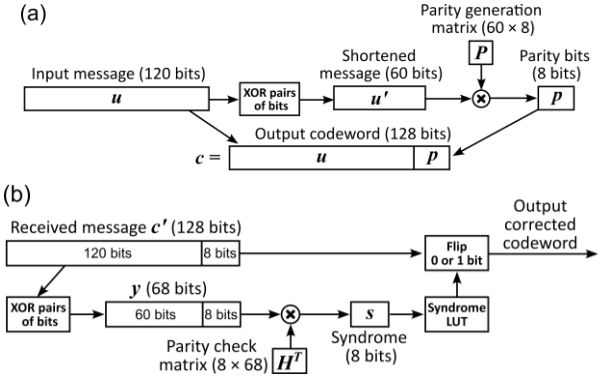

Fig. 4. (a) Encoding 120 information bits using the shortened Hamming (68,60) code (b) Decoding the Hamming code at receiver.

message u are XORed to create a new 60-bit long message u'. A sequence of eight parity bits that protects u' is generated with

$$p = u'P, \tag{1}$$

where $P \in \mathbb{F}_2^{60\times 8}$ is a new punctured parity generation matrix taken from a recent Ethernet standard contribution [16]. This binary matrix multiplication is a Verilog module that uses XOR gates to perform the binary multiply-accumulate operations between u and the columns of P.

In Fig.4 (b), the decoder forms a 68-bit-long received message y based on the received message c'. The first 60 bits in y are produced by XORing the first 60 PAM-4 symbols in c', and the last 8 bits of y are copied from the remaining 8 bits in c'. To decode y, first the syndrome $s \in \mathrm{F}_2^{1\times 8}$ is calculated using the parity-check matrix $H \in \mathrm{F}_2^{8\times 68}$

$$s = yH^T. \tag{2}$$

Because the shortened Hamming code is systematic, define I_8 as the 8×8 binary identity matrix, the parity-check matrix H is

$$H = [P^T\ I_8], \tag{3}$$

The 8-bit syndrome s can now be uniquely mapped to the location of either a PAM-symbol error in the first 60 PAM-4 symbols in c' or the location of a bit error in the 8 parity bits. The syndrome can take $2^8 = 256$ possible values and the corresponding error patterns are stored in a lookup table. With the shortened code, only 68 of the 256 possible syndrome values point to a valid error location in the lookup table. In addition, $s = 0$ indicates no error, and the remaining 187 non-zero syndrome values indicate decoding failure.

B. Convolutional Interleaver

Although the errors in optical links may be predominantly random, the inner-FEC decoder changes the error distribution after decoding the inner-FEC codewords with only one error. As a result, most of the 120-bit long inner FEC messages will be error-free. However, if a codeword has two or more errors, the decoder may miscorrect to a wrong codeword and introduce another bit error. To give the outer KP4 FEC decoder the best chance of correcting errors from an erroneous 120-bit-long inner-FEC codeword, each of its twelve 10-bit-long outer-FEC symbols should be distributed to different outer-FEC codewords, which can be achieved by block interleaving [10]. However, this approach is too resource-intensive for 200 Gb/s systems as it requires multiple KP4 FEC encoders and decoders working in parallel on the same chip.

The distribution of outer-FEC symbols can be realistically achieved using a combination of block interleaving and CI. CI is a technique that permutes the order of input symbols at the cost of added latency [17]. An example of the full convolutional interleaving/de-interleaving flow is shown in Fig. 5. The interleaver delays transmitted symbols by differing amounts, resulting in a shuffled transmission order. This shuffling is reversed on the receiving side by a convolutional de-interleaver. The CI model implemented in our FPGA is described in a recent IEEE standard proposal [16], where an inner-FEC codeword consists of outer FEC symbols from 12 distinct KP4 codewords.

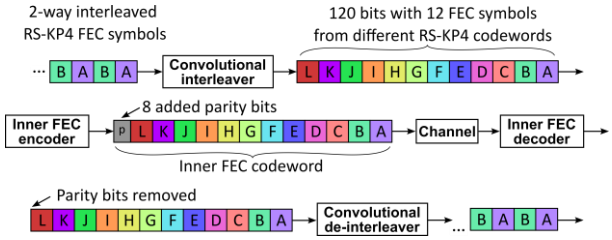

Fig. 5. An example of convolutional interleaving and de-interleaving.

IV. Soft-Decision Decoding

A. Soft-Output Receiver Model

Soft-decision decoding can improve the inner FEC code's performance by using channel reliability information as well as the hard-decision PAM-4 symbols. This boost in performance comes at the cost of added complexity: a soft-output receiver is required to produce this reliability information; in addition, a more complex soft-decision inner-FEC decoder is needed.

Fig. 6 shows the transceiver architecture for soft-decision inner-FEC decoding used on the FPGA platform. The receiver not only produces a sequence of hard-decision PAM-4 symbols $d_k \in \{0,1,2,3\}$, but also a series of reliability values α_k. The reliability values should have the property that if $\alpha_k < \alpha_j$, then the probability $\Pr(d_k = b_k) < \Pr(d_j = b_j)$. In other words, symbols with higher α are more likely to be correct.

Each of the four possible output PAM-4 symbols can be rank-ordered from most to least likely. Typically, the third and fourth most likely PAM-4 symbols are negligible. In this case, the log-likelihood ratio of the first and second most likely symbols can be defined as the α that satisfies the inequality stated above. For example, if at timestep k the most likely symbol is 0 and the second most likely symbol is 1, then

$$\alpha_k = \log\left(\frac{\Pr(b_k=0)}{\Pr(b_k=1)}\right). \tag{4}$$

By definition $\alpha \geq 0$, and $\alpha = 0$ only when the first and second most likely symbols are equally likely. With Gray-coded PAM-4 symbols, the second and first most likely symbols only differ by one bit, the location of this lower-reliability bit could be either in the most-significant bit (MSB) or least-significant bit (LSB) of the PAM-4 symbol. The location of the lower-reliability bit in each PAM-4 symbol is crucial for the soft-decision decoder to correct the bit error. The receiver passes on this information with an additional sign bit β_k. If $\beta_k = 0$, the low-reliability bit is in the LSB of the PAM-4 symbol at time k, and if $\beta_k = 1$, the low-reliability bit is in the MSB.

B. Chase Algorithm

Chase presented an algorithm for soft-decision decoding of binary linear block codes in [18]. This algorithm is a popular choice for practical implementations of the inner-FEC decoder in 200 Gb/s system.

A hard-decision decoder for a binary (n, k) code takes in a received sequence $y \in \mathbb{F}_2^{1\times n} = \{y_1, y_2, ..., y_n\}$, and finds the error sequence z_m of minimum binary weight such that $y+z_m = \{y_1+z_{m1}, y_2+z_{m1}, ...y_n+z_{m1}\}$ is a valid codeword (here operator '+' represents the modulo-2 addition). Hard-decision binary

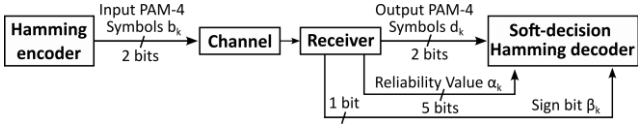

Fig. 6. Transceiver architecture for soft-decision inner-FEC decoding.

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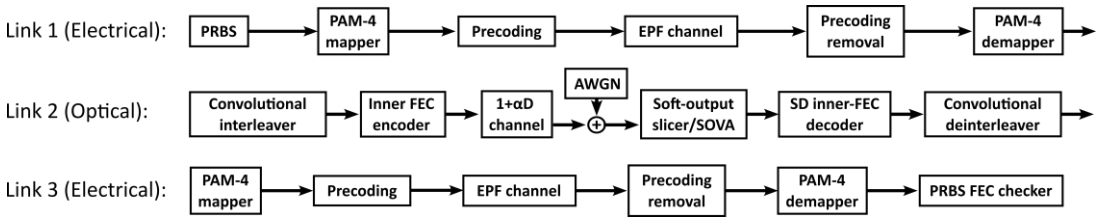

Fig. 7. Case study: system-level architecture of a multi-part link with an AWGN optical link.

decoders can only find error patterns of maximum weight t. For example, the decoder for the shortened Hamming code with $t = 1$ presented in Section III.A can only determine an error pattern of binary weight one. If a valid error pattern of weight one cannot be found, it experiences a decoding failure.

Similarly, a soft-decision decoder finds an error pattern z_m of minimum analog weight such that $y+z_m$ is a valid codeword. The analog weight of an error pattern is defined as $\sum_{i=1}^{N} \alpha_i Z_{mi}$, and it corresponds to the likelihood of an error pattern. An error pattern with a lower analog weight is more likely than one with a higher analog weight. Given a received sequence, an ideal soft-decision decoder finds the most likely codeword by enumerating all possible error patterns. Chase's algorithm approaches the performance of an ideal soft-decision decoder.

Chase's algorithm finds a limited set of possible error patterns and picks the one with the lowest analog weight. An error pattern z_T is found by perturbing y by a test pattern T, and then applying hard-decision decoding on the codeword $y + T$. If the decoding is successful, the decoded codeword gives a new error pattern z' with respect to $y + T$, hence $z_T = z' + T$.

Let q and w be integer parameters. The test patterns are generated by taking all combinations of w or fewer 1s in the least reliable q positions of the Y, including the all-0s test pattern. This gives a total of $\binom{q}{0}+\binom{q}{1}+\ldots+\binom{q}{w}$ test patterns. The Chase algorithm with parameters q and w can potentially extend the decoder's error-correcting capability from t to $t + w$. By increasing q and/or w, a larger number of test patterns are considered in the algorithm, giving a better chance of finding the error pattern with the lowest analog weight.

V. Case Study

This section presents modelling and analysis of a realistic multi-part link on the FPGA platform. The topic of ongoing discussion for 200 Gb/s multi-part links is the BER allocation for optical and electrical links. In general, the electrical links have better signal integrity, and most of the error budget is allocated for the optical link. The overall system's codeword error rate (CER) is primarily determined by the optical link's CER and the FEC architecture. Setting a performance target for the optical link is essential to maintain interoperability for hosts and modules from different vendors. Recent IEEE standard contributions have proposed target BERs [19], but until now, there has been no reliable method to validate the proposals.

Fig. 7 shows the system-level model of a multi-part wireline system on the FPGA platform. This model represents the system detailed in Fig. 1, which communicates data over a three-part link at 200 Gb/s per lane using the Ethernet protocol. In this study, the BER in the electrical links is assumed to be at a known level. The electrical links in Fig.7 are modelled with the error propagation factor (EPF) model [2]. The EPF model is a first-order Markov chain fully characterized by two transition probabilities: the initial error probability (IEP) and the EPF. The electrical links in this model are taken from a recent IEEE contribution [20] with IEP = 2.67×10^{-5} and EPF = 0.75. 1/(1+D) precoding is used, introducing a BER of 4×10^{-5} by each of the electrical links. The optical link is modelled using the AWGN channel presented in Section II with a soft-output slicer or a soft-output Viterbi algorithm (SOVA).

The optical link's SNR is swept to find the level at which the overall system's CER is sufficiently low. This target CER level would ideally be 1.45×10^{-11} by the Ethernet standard's specification (or post-FEC BER at $1x10^{-12}$). However, the available FPGA hardware (Xilinx XCVU095-2FFVA2104E) can only simulate this link at 1.2 Gb/s, which takes around 20 days to demonstrate CER at 1.45×10^{-11}. Since only one FPGA is available, this case study assumes a target CER level at 10^{-9} so that simulations are performed in one day.

Three FEC architectures are compared in this analysis:

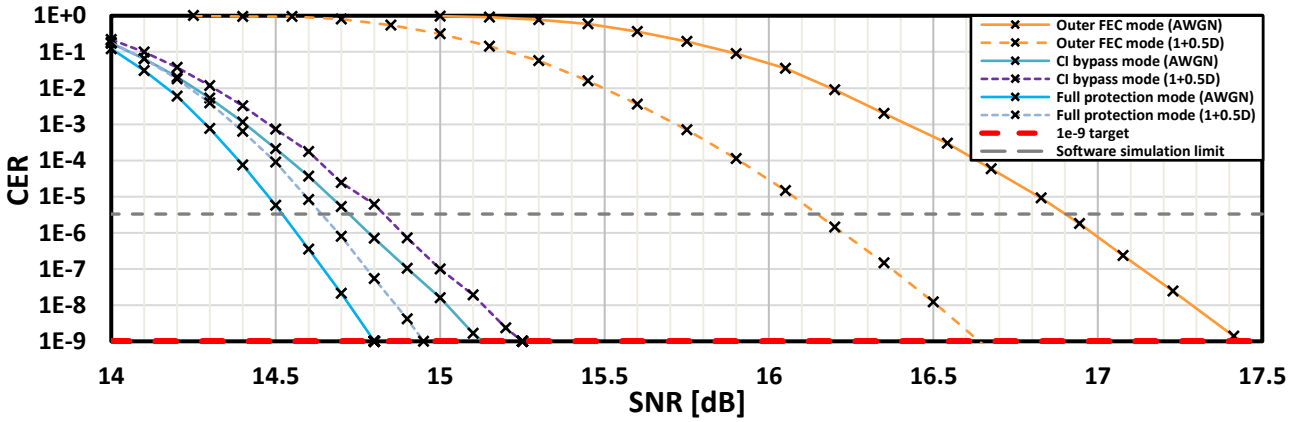

Fig. 8. Overall link CER vs. Optical module's SNR of the multi-part link system in Fig. 7.

(1) Full protection mode enabling the soft-decision Hamming (68,60) code and KP4 FEC codes. 4-way block interleaving and CI are used to maximize the overall coding gain.
(2) CI bypass mode disabling the CI to minimize latency. This mode uses the soft-decision Hamming (68,60) code + KP4 FEC code with 4-way block interleaving.
(3) Outer-FEC mode bypassing the inner FEC code completely. In this mode the channel is equalized with MLSD, equivalent to SOVA without the soft reliability values.

Fig. 8 shows the optical module's SNR on the x-axis and the corresponding overall KP4 CER for the entire system on the y-axis for the three different FEC architectures. Two channel responses 1+0D and 1+0.5D are used in this case study. For the 1+0D channel, outer-FEC mode shows >2 dB degradation at the target CER level. Because of this, bypassing the inner FEC is only practical for a high-SNR optical link. Of the other two candidates, the CI bypass mode shows around 0.3 dB degradation compared to the architecture with full protection. For the 1+0.5D channel, the outer-FEC mode shows a better performance compared to the 1+0D channel. This is because MLSD benefits from a signal power that is amplified from the 1+0.5D response. Despite this increased signal power, the optical channel now suffers from correlated PAM-4 symbol errors, reducing the effectiveness of the inner FEC code. As such, the other two modes show an overall degradation in performance by about 0.1 dB compared to 1+0D channel. This study demonstrates how the FPGA platform may be used to develop BER allocations for the 200 Gb/s Ethernet standard.

VI. Conclusion

In this brief we presented an FPGA-accelerated platform for architecting 200 Gb/s wireline systems. The platform allows the modelling of complex wireline systems, including multi-part links with concatenated FEC, soft-decision decoding, block interleaving, convolutional interleaving, and 1/(1+D) precoding, with the flexibility to explore different channel models and FEC architectures. It provides a speed increase of more than 10,000 times over comparable time-domain software simulations [9-11], allowing for demonstration of the Ethernet standard's target CER of 10^{-9} (~10^{-11} post-FEC BER) for a realistic multi-part-link within one day. In contrast, the time-domain software CFEC model reported in [11] can only simulate down to 10^{-8} post-FEC BER level using 16 parallel CPU cores in one day, which corresponds to the software-simulation limit at CER = 3.3×10^{-6} in Fig.8. The prior FPGA work in [12] uses over-sampled time-domain signals, increasing channel-model accuracy but lowering simulation speed and it does not report BERs lower than 10^{-7} (~10^{-5} CER). Our proposed platform can easily be scaled up using a cluster of 18 or more FPGAs to validate CER levels $\leq 1.45\times10^{-11}$ within 24 hours. This significant speed improvement over existing simulation methods allows us to explore new and complex FEC architectures with high accuracy, which is the key novelty of our platform. The FPGA platform presented in this brief is open sourced and available in [21].

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