

- hit time = block access time + hit data return time

hit time  $\ll$  miss penalty.

~ memory hierarchy : locality 원리 활용.

locality { time : 최근에 접근한 곳 모으기  
spatial : 최근에 접근한 곳 근처에서 접근

~ 예제 Cache block : 4 word

주소 간격 1

DRAM 접근 15

word x245기 1

① one word wide 1블럭 읽기

CPU

1 1

cache

1 + 4 + 60 = 65 bus cycle

1 15x4, 1x4

memory 

② wide memory bank (2 word wide

CPU

| |

cache

| | 15x2, 1x2

memory □ □

$$1 + 2 + 30 = 33 \text{ bus cycle}$$

### ③ Interleave

CPU

| |

cache

| 15, 1x4

memory □ □ □ □

$$1 + 4 + 15 = 20 \text{ bus cycle}$$

### - Direct mapped

tag      ??      xx

↓

index

$$2^2 = 4 \text{ words, } 4 \times 8 = 32 \text{ bits}$$

- Address 0 1 2 3 4 3 4 15

(0) 0000

(1) 0001 (00)

(2) 0010 (01)

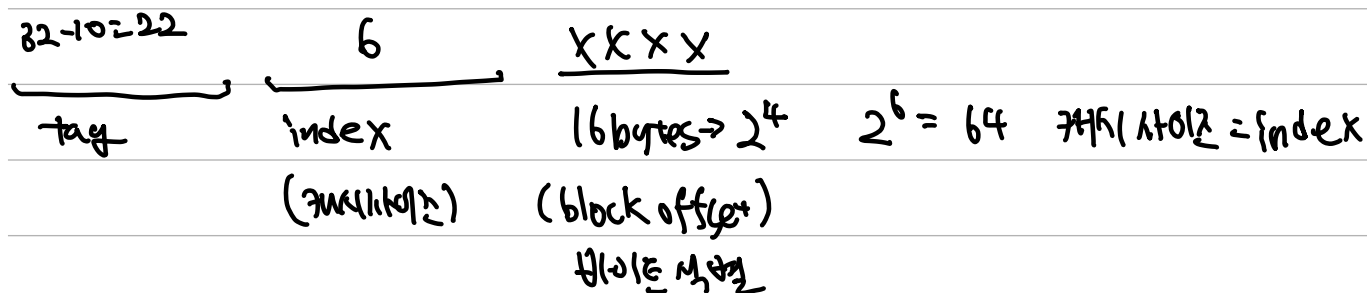
(3) 0011 (10)

(4) 0100 (11)

(15) 1111

- wrong large block size

direct mapped cache , 64 block , 16 bytes per block , 32bit  $\frac{32}{4}$  (4byte)



$$\lfloor 1200/16 \rfloor = 75, \quad 75 \cdot 64 = 11$$

~ 캐시 필터 쓰기

$2^n$ 개 블록  $\rightarrow$  n 비트 인덱스

$2^m$  word ( $2^{m+2}$  byte)  $\rightarrow m+2$  bit offset.

10. 10월 24일 바이트 지정

- Virtual memory

가장 오래된 디스크 (101기)의 21492104 블록 명칭) = page fault

- page table (main memory 에 위치)

valid bit, virtual page num을 physical page num을 찾아 변환

001은 X, 101은 1021044.

reference bit, dirty bit  
 ↓                      ↓  
 (읽기/쓰기), access    write back

page table 은 3 개씩 → TLB  
 (main memory에 있음)

### events

TLB	page table	cache	
hit	hit	hit	yes.
hit	hit	miss	yes.    캐시에만 있음.
miss	hit	hit	yes.    TLB miss
miss	hit	miss	yes.    메모리에만 있음.
miss	miss	miss	yes.    page fault.

hit	(miss) (miss) (miss)	miss	hit/miss. page가 메모리에 있음 → TLB나 cache hit 가 됨.
hit		hit	
miss		hit	

### Virtual address 는 cache까지 안감.

aliasing: 2개 virtual address로 같은 physical에 접근할 수 있음.

- 17년 2011

(cache index는 page offset 번호를 맞추기. (overlap)

- DV는 조지

compulsory (cold)

capacity

conflict (collision)

7H4 H4(2)↑

(capacity miss)↓

accesstime↑  
coldmiss↑

associativity↑

conflict miss↓

access time↑

block size↑

cold miss↓

miss penalty↑

(H4H4H4) miss rate↑

- 17년

1 block = 4word      1 word = 4byte = 32bit  
= 16 byte

data 371 16KB  $\Rightarrow 16 \times 2^{10}$  byte

block 개수 :  $2^{10}$  개

		4	
		┌───────────┐	
32-14=18	10	2	2
└────────┘	└────────┘	└────────┘	└────────┘
tag	block	block	byte
	index	offset	offset

$$\text{cache size} = \underbrace{2^{10}}_{\text{bit}} \times \left( \underbrace{16 \times 8}_{\text{block size}} + \underbrace{18}_{\text{tag bit}} + \underbrace{1}_{\text{valid bit}} \right)$$

Q11 64 block, 1 block = 16 byte

Address 1200

$\begin{array}{ccc} 6 & 2 & 2 \\ \hline & & \end{array}$   
block 4 byte

$$\frac{1200}{2^4} = 75$$

$$75 \% 64 = \underline{\underline{11}}$$