# AC7903A Datasheet

## Zhuhai Jieli Technology Co.,LTD

**Version：V1.2**

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# AC7903A Features

### High performance 32-bit RISC CPU

- Double core RISC 32-bit CPU(Support FPU)
- 24KB D-Cache 6 way, 32KB I-Cache 8way
- DC-280MHz operation
- 128 Vectored interrupts
- Four Levels interrupt priority

### Flexible I/O

- 15 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level Schmitt triggered input
- External wake up/interrupt on all GPIOs

### Peripheral Feature

- USB 1.1 OTG controller
- Audio interface supports IIS, left adjusted, right adjusted and DSP mode
- Multi-function 32-bit timers, support capture and PWM mode
- 16-bit PWM generator for motor driving
- Three full-duplex advanced UART
- Two SPI interface supports host and device mode
- Two SD Card Host controller
- One IIC interface supports host and device mode
- One SPDIF receiving interface without analog amplify
- One Quadrate decoder
- Watchdog
- One Crystal Oscillator
- Two channel 16-bit DAC with headphone amplifier
- Two channels Audio 16-bit ADC
- Two channels MIC amplifie
- Two channels analog MUX
- Seven channels 10-bit ADC
- Power-on reset
- Embedded PMU support low power mode

### Bluetooth Feature

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth V5.0+BR+EDR+ BLE specification
- Bluetooth Piconet and Scatternet support
- Meet class2 and class3 transmitting power requirement
- Support GFSK and π/4 DQPSK all paket types
- Provides +15dbm transmitting power
- Receiver with -93dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp \att\gap\gatt\rfcomm\sdp\l2cap profile

### WIFI Feature

- Support all mandatory IEEE 802.11b data rates of 1, 2, 5.5 and 11 Mbps, all 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11n MCS0~ MCS7, 20MHz, 800ns and 400ns guard interval.
- Support advanced 1x1 802.11n features:
  Full / Half Guard Interval
  Frame Aggregation
  Reduced Inter-frame Space (RIFS)
  Space Time Block Coding (STBC)
  Greenfield mode
- Support
  WEP/WPA-PSK(TKIP/CCMP)/WPA2-PSCK
  AES256/AES128/SHA256/SHA128
- Support apply to AP/STA
- Transmitter power:

| | | |
|---|---|---|
| DSSS 1M/S | 17 | dBm |
| MCS0 | 15 | dBm |
| MCS7 | 12 | dBm |

- Receiver sensitivity:

| | | |
|---|---|---|
| DSSS 1M/S | -95 | dBm |
| MCS0 | -93 | dBm |
| MCS7 | -72 | dBm |

## Power Supply

- VBAT is 2.2V to 5.5V
- VDDIO is 2.1V to 3.6V
- AVDDHP is 2.1V to 3.6V

## Packages

- QFN40(5mm*5mm)

## Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

# 1. Pin Definition

## 1.1 Pin Assignment

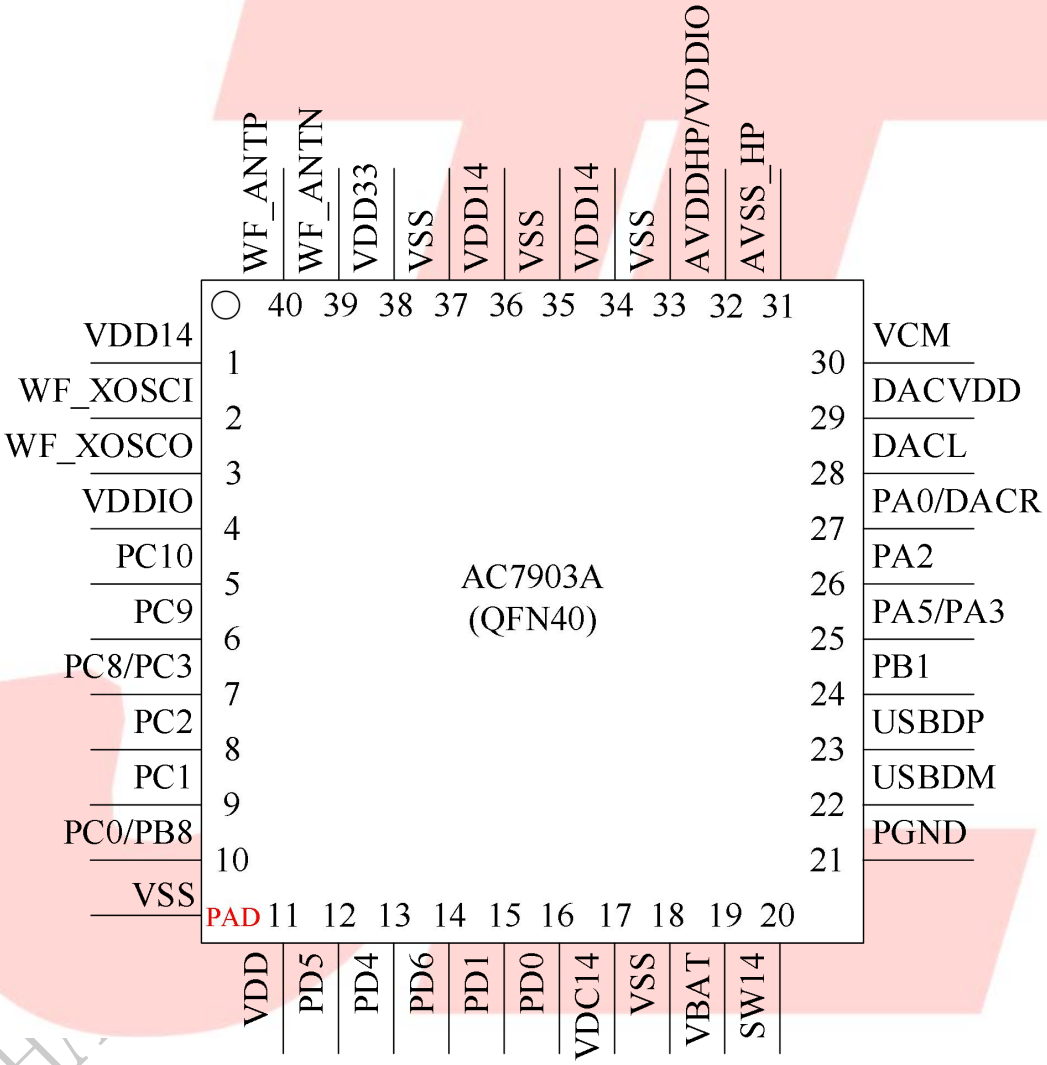



**Figure 1-1 AC7903A_QFN40 Package Diagram**

## 1.2 Pin Description

**Table 1-1 AC7903A_QFN40 Pin Description**

| PIN NO. | Name | I/O Type | Drive (mA) | Function | Other Function |
|---|---|---|---|---|---|
| 1 | VDD14 | P | / | RF Power 1.4V | - |
| 2 | WF_XOSCI | I | / | RF OSCI | - |
| 3 | WF_XOSCO | O | / | RF OSCO | - |
| 4 | VDDIO | P | / | IO Power 3.3V | - |
| 5 | PC10 | I/O | 24/16/8/2.4 | GPIO | SD0_CLKD: SD0 Clock(D)<br>SPI1_DOB: SPI1 Data Out(B)<br>Q-decoder1<br>UART2_RXB: Uart2 Data In(B)<br>ADC9: ADC Channel 9<br>TMR5CK(MCPWM)<br>PWM3: Timer3 PWM Output<br>TOUCH10: Touch Input Channel 10 |
| 6 | PC9 | I/O | 24/16/8/2.4 | GPIO | SD0_CMDD: SD0 CMD(D)<br>SPI1_CLKB: SPI1 Clock(B)<br>Q-decoder0<br>UART2_TXB: Uart2 Data Out(B)<br>ADC8: ADC Channel 8<br>TMR4CK(MCPWM)<br>TOUCH9: Touch Input Channel 9 |
| | PC8 | I/O | 24/16/8/2.4 | GPIO | SD0_DAT0D: SD0 Data0(D)<br>SPI1_DIB: SPI1 Data In(B)<br>SPDIF_B<br>PWMCH2L(MCPWM)<br>CAP5: Timer5 Capture<br>TOUCH8: Touch Input Channel 8 |
| 7 | PC3 | I/O | 24/16/8/2.4 | GPIO | UART1_TXB: Uart1 Data Out(B)<br>ALNK0_DAT0A: Audio Link0 Data0(A)<br>ALNK1_DAT0A: Audio Link1 Data0(A)<br>SD1_DAT1B: SD1 Data1(B)<br>FPIN6(MCPWM)<br>TMR4: Timer4 Clock In<br>TOUCH3: Touch Input Channel 3 |

| PIN NO. | Name | I/O Type | Drive (mA) | Function | Other Function |
|---|---|---|---|---|---|
| 8 | PC2 | I/O | 24/16/8/2.4 | GPIO | IIC_SDA_C: IIC SDA(C)<br>ALNK0_LRCKA: Audio Link0 Word Select(A)<br>ALNK1_LRCKA: Audio Link1 Word Select(A)<br>SD1_DAT0B: SD1 Data0(B)<br>PWMCH4L(MCPWM)<br>CAP1: Timer1 Capture<br>TOUCH2: Touch Input Channel 2 |
| 9 | PC1 | I/O | 24/16/8/2.4 | GPIO | IIC_SCL_C: IIC SCL(C)<br>ALNK0_SCLKA: Audio Link0 Serial Clock(A)<br>ALNK1_SCLKA: Audio Link1 Serial Clock(A)<br>SD1_CLKB: SD1 Clock(B)<br>ADC7: ADC Channel 7<br>PWM1: Timer1 PWM Output<br>Wakeup11: Port Wakeup 11<br>TOUCH1: Touch Input Channel 1 |
| 10 | PC0 | I/O | 24/16/8/2.4 | GPIO | CLKOUT0: Clock Out0<br>ALNK0_MCKA: Audio Link0 Master Clock(A)<br>ALNK1_MCKA: Audio Link1 Master Clock(A)<br>SD1_CMDB: SD1 CMD(B)<br>ADC6: ADC Channel 6<br>PWMCH4H(MCPWM)<br>Wakeup10: Port Wakeup 10<br>TOUCH0: Touch Input Channel 0 |
| | PB8 | I/O | 24/16/8/2.4 | GPIO | SDGAT: SD Power Gate |
| 11 | VDD | P | / | Core Power 1.2V | - |
| 12 | PD5 | I/O | 24/16/8/2.4 | GPIO | SPI0_DOA(0): SPI0 Data Out(A)<br>SFC_DOA(0): SFC Data Out(A) |
| 13 | PD4 | I/O | 24/16/8/2.4 | GPIO | SPI0_CLKA: SPI0 Clock(A)<br>SFC_CLKA: SFC Clock(A) |
| 14 | PD6 | I/O | 24/16/8/2.4 | GPIO | SFGAT: Flash Power Gate |
| 15 | PD1 | I/O | 24/16/8/2.4 | GPIO | SPI0_DIA(1): SPI0 Data In(A)<br>SFC_DIA(1): SFC Data In(A) |
| 16 | PD0 | I/O | 24/16/8/2.4 | GPIO (pull up) | SPI0_CSA: SPI0 Chip Select(A)<br>SFC_CSA: SFC Chip Select(A) |

| PIN NO. | Name | I/O Type | Drive (mA) | Function | Other Function |
|---|---|---|---|---|---|
| 17 | VDC14 | P | / | Core Power 1.4V | - |
| 18 | VSS | P | / | Ground | - |
| 19 | VBAT | P | / | LDO Power | - |
| 20 | SW14 | P | / | DC-DC Switch Pin | - |
| 21 | PGND | P | / | PMU Ground | - |
| 22 | USBDM | I/O | 10 | USB Negative Data (pull down) | UART1_RXD: Uart1 Data In(D)<br>ISP_DI_A<br>SPI2_DOB: SPI2 Data Out(B)<br>IIC_SDA_A: IIC SDA(A)<br>ADC12: ADC Channel 12<br>SDTAP_DATB |
| 23 | USBDP | I/O | 10 | USB Positive Data (pull down) | UART1_TXD: Uart1 Data Out(D)<br>ISP_CLK_A<br>SPI2_CLKB: SPI2 Clock(B)<br>IIC_SCL_A: IIC SCL(A)<br>ADC13: ADC Channel 13<br>SDTAP_CLKB |
| 24 | PB1 | I/O | 24/16/8/2.4 | GPIO (pull up) | ISP_DO<br>UART0_TXB: Uart0 Data Out(B)<br>ADC3: ADC Channel 3<br>Long Press reset<br>TMR1: Timer1 Clock In<br>Wakeup8: Port Wakeup 8 |
| 25 | PA5 | I/O | 24/16/8/2.4 | GPIO | UART0_TXA: Uart0 Data Out(A)<br>AMUX2: Simulator Channel 2<br>CAP3: Timer3 Capture |
| | PA3 | I/O | 24/16/8/2.4 | GPIO | MIC2P: MIC2 P Channel<br>UART0_TXC: Uart0 Data Out(C)<br>PWMCH0H(MCPWM) |
| 26 | PA2 | I/O | 24/16/8/2.4 | GPIO | MIC0P: MIC0 P Channel<br>TMR0CK(MCPWM) |
| 27 | PA0 | I/O | 24/16/8/2.4 | GPIO | AMUX0: Simulator Channel 0<br>TMR1CK(MCPWM)<br>Wakeup2: Port Wakeup 2 |
| | DACR | O | / | DAC Right Channel | - |
| 28 | DACL | O | / | DAC Left Channel | - |
| 29 | DACVDD | P | / | DAC Power | - |

| PIN NO. | Name | I/O Type | Drive (mA) | Function | Other Function |
|---|---|---|---|---|---|
| 30 | VCM | P | / | VCM | - |
| 31 | AVSS_HP | P | / | Audio Ground | - |
| 32 | AVDD_HP | P | / | Audio Power | - |
| 33 | VSS | P | / | Ground | - |
| 34 | VDD14 | P | / | RF Power 1.4V | - |
| 35 | VSS | P | / | Ground | - |
| 36 | VDD14 | P | / | RF Power 1.4V | - |
| 37 | VSS | P | / | Ground | - |
| 38 | VDD33A | P | / | RF Power 3.3V | - |
| 39 | WF_ANTN | - | / | RF Antenna Positive | - |
| 40 | WF_ANTP | - | / | RF Antenna Negative | - |
| PAD | | P | / | VSS | - |

# 2. Electrical Characteristics

## 2.1 Absolute Maximum Ratings

**Table** 2-1

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Tamb | Ambient Temperature | -40 | +85 | ℃ |
| Tstg | Storage temperature | -65 | +150 | ℃ |
| VBAT | Supply Voltage | -0.3 | 5.5 | V |
| VDD33A | RF Power 3.3V Voltage | -0.3 | 3.6 | V |
| AVDDHP | Audio Power Voltage | -0.3 | 3.6 | V |
| VDD14 | RF Power 1.4V Voltage | -0.3 | 1.55 | V |
| $V_{3.3IO}$ | 3.3V IO Input Voltage | -0.3 | VDDIO+0.3 | V |

## 2.2 PMU Characteristics

**Table** 2-2

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| VBAT | Voltage Input | 2.2 | 3.7 | 5.5 | V | _ |
| VDDIO | Voltage output | 2.1 | 3.3 | 3.6 | V | LDO5V = 5V, 200mA loading |
| VDC14 | Voltage output | 1.2 | 1.4 | 1.55 | V | LDO mode: 70mA loading<br>DC-DC mode: 120mA loading |
| VDD | Voltage output | 0.87 | 1.2 | 1.32 | V | LDO5V=5V, 100mA loading |
| VDD33A | Voltage Input | 2.1 | 3.3 | 3.6 | V | _ |
| AVDDHP | Voltage Input | 2.1 | 3.3 | 3.6 | V | _ |
| VDD14 | Voltage Input | 1.2 | 1.4 | 1.55 | V | _ |

## 2.3 IO Input/Output Electrical Logical Characteristics

**Table** 2-3

| **IO input characteristics** | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| $V_{IL}$ | Low-Level Input Voltage | -0.3 | – | 0.3* VDDIO | V | VDDIO = 3.3V |
| $V_{IH}$ | High-Level Input Voltage | 0.7* VDDIO | – | VDDIO+0.3 | V | VDDIO = 3.3V |
| **IO output characteristics** | | | | | | |
| $V_{OL}$ | Low-Level Output Voltage | – | – | 0.33 | V | VDDIO = 3.3V |
| $V_{OH}$ | High-Level Output Voltage | 2.7 | – | – | V | VDDIO = 3.3V |

## 2.4 Internal Resistor Characteristics

**Table** 2-4

| **Port** | **General Output** | **High Drive** | **Internal Pull-Up Resistor** | **Internal Pull-Down Resistor** | **Comment** |
|---|---|---|---|---|---|
| PA, PC, PD PB1, PB8 | 8mA | 24mA | 10K | 10K | 1.PB1&PD0 default pull up<br>2.USBDM & USBDP default pull down<br>3. Internal pull-up/pull-down resistance \| accuracy ±20% |
| USBDP USBDM | 10mA | – | 1.5K | 15K | |

## 2.5 DAC Characteristics

**Table** 2-5

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Frequency Response | 20 | _ | 20K | Hz | |
| THD+N | _ | -78 | _ | dB | 1KHz/0dB |
| S/N | _ | 92 | _ | dB | 10Kohm loading |
| Crosstalk | _ | -80 | _ | dB | With A-Weighted Filter |
| Output Swing | _ | 0.75 | _ | Vrms | |
| Dynamic Range | _ | 90 | _ | dB | 1KHz/-60dB<br>10Kohm loading<br>With A-Weighted Filter |
| DAC Output Power | 11 | _ | _ | mW | 32ohm loading |

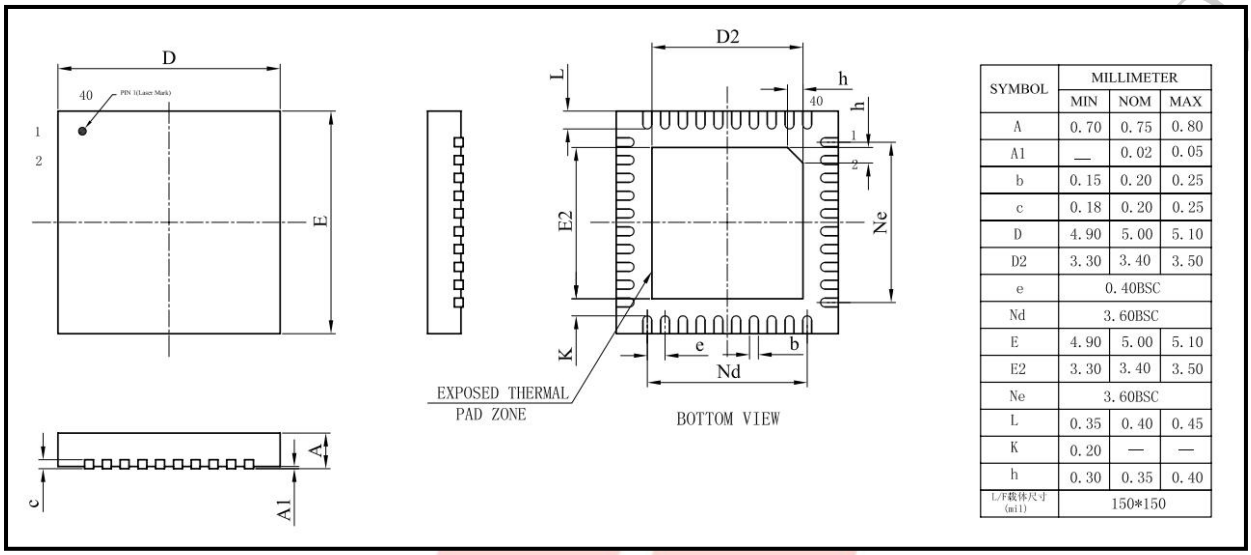
## 2.6 ADC Characteristics

**Table** 2-6

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Dynamic Range | _ | 87 | _ | dB | 1KHz/-60dB<br>10Kohm loading<br>With A-Weighted Filter |
| S/N | _ | 90 | _ | dB | 1KHz/-60dB |
| THD+N | _ | -72 | _ | dB | 10Kohm loading |
| Crosstalk | _ | -80 | _ | dB | With A-Weighted Filter |

# 3. Package Information

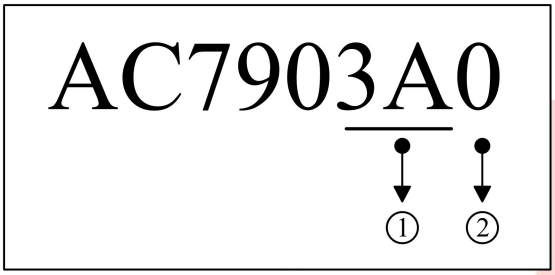
## 3.1 QFN40(5mm*5mm)




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | — | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.18 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.30 | 3.40 | 3.50 |
| e | 0.40BSC | | |
| Nd | 3.60BSC | | |
| E | 4.90 | 5.00 | 5.10 |
| E2 | 3.30 | 3.40 | 3.50 |
| Ne | 3.60BSC | | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — |
| h | 0.30 | 0.35 | 0.40 |
| L/F载体尺寸 (mil) | 150*150 | | |

**Figure 3-1 AC7903A_QFN40 Package**

# 4. Package Type Specification




①Represents different chips (different packages or bindings)

②Represents different memory sizes

0: No memory
2: 2Mbit Flash
4: 4Mbit Flash
8: 8Mbit Flash
6: 16Mbit Flash
3: 32Mbit Flash
5: 64Mbit Flash
7: 128Mbit Flash
A: 1Mx16 SDRAM
B: 4Mx16 SDRAM
C: 16M bit PSRAM
D: 64M bit PSRAM

# 5. Revision History

| Date | Revision | Description |
|---|---|---|
| 2019.10.21 | V1.0 | Initial Release |
| 2020.05.19 | V1.1 | Update Format |
| 2021.06.02 | V1.2 | Modify transmit power parameters<br>Modify DAC performance parameters<br>Modify the absolute maximum rating<br>Add SPDIF function description |