AC7913A0 Datasheet

Zhuhai Jieli Technology Co.,LTD

Version：V1.0

Date：2021.10.08

AC7913A0 Features

High performance 32-bit RISC CPU

- Double core RISC 32-bit CPU(Support FPU)
- 24KB D-Cache 6 way, 32KB I-Cache 8way
- DC-320MHz operation
- 128 Vectored interrupts
- Four Levels interrupt priority

Flexible I/O

- 18 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level Schmitt triggered input
- External wake up/interrupt on all GPIOs

Peripheral Feature

- FUSB 1.1 OTG controller
- Audio interface supports IIS, left adjusted, right adjusted and DSP mode
- Multi-function 32-bit timers, support capture and PWM mode
- 16-bit PWM generator for motor driving
- Three full-duplex advanced UART
- Two SPI interface supports host and device mode
- Two SD Card Host controller
- One IIC interface supports host and device mode
- One SPDIF receiving interface without analog amplify
- Quadrate decoder
- Watchdog
- One Crystal Oscillator
- Two channel 16-bit DAC with headphone amplifier
- Three channels Audio 16-bit ADC
- Three channels MIC amplifier
- Two channels analog MUX
- Nine channels 10-bit ADC
- Power-on reset
- Embedded PMU support low power mode

Bluetooth Feature

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth V5.0+BR+EDR+ BLE specification
- Bluetooth Piconet and Scatternet support
- Meet class2 and class3 transmitting power requirement
- Support GFSK and π/4 DQPSK all paket types
- Provides +15dbm transmitting power
- Receiver with -93dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp \att\gap\gatt\rfcomm\sdp\l2cap profile

WIFI Feature

- Support all mandatory IEEE 802.11b data rates of 1, 2, 5.5 and 11 Mbps, all 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11n MCS0~ MCS7, MCS32, 20MHz/40MHz BW, 800ns and 400ns guard interval.
- Support advanced 1x1 802.11n features:
  Full / Half Guard Interval
  Frame Aggregation
  Reduced Inter-frame Space (RIFS)
  Space Time Block Coding (STBC)
  Greenfield mode

- Support WEP/WPA-PSK(TKIP/CCMP) /WPA2-PSCK/AES256/AES128/SHA256 /SHA128
- Support apply to AP/STA
- Transmitter power:

DSSS 1M/S	17	dBm
MCS0	16	dBm
MCS7	13	dBm

- Receiver sensitivity:

DSSS 1M/S	-95	dBm
MCS0	-92	dBm
MCS7	-74	dBm

Packages

- QFN40(5mm*5mm)

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃
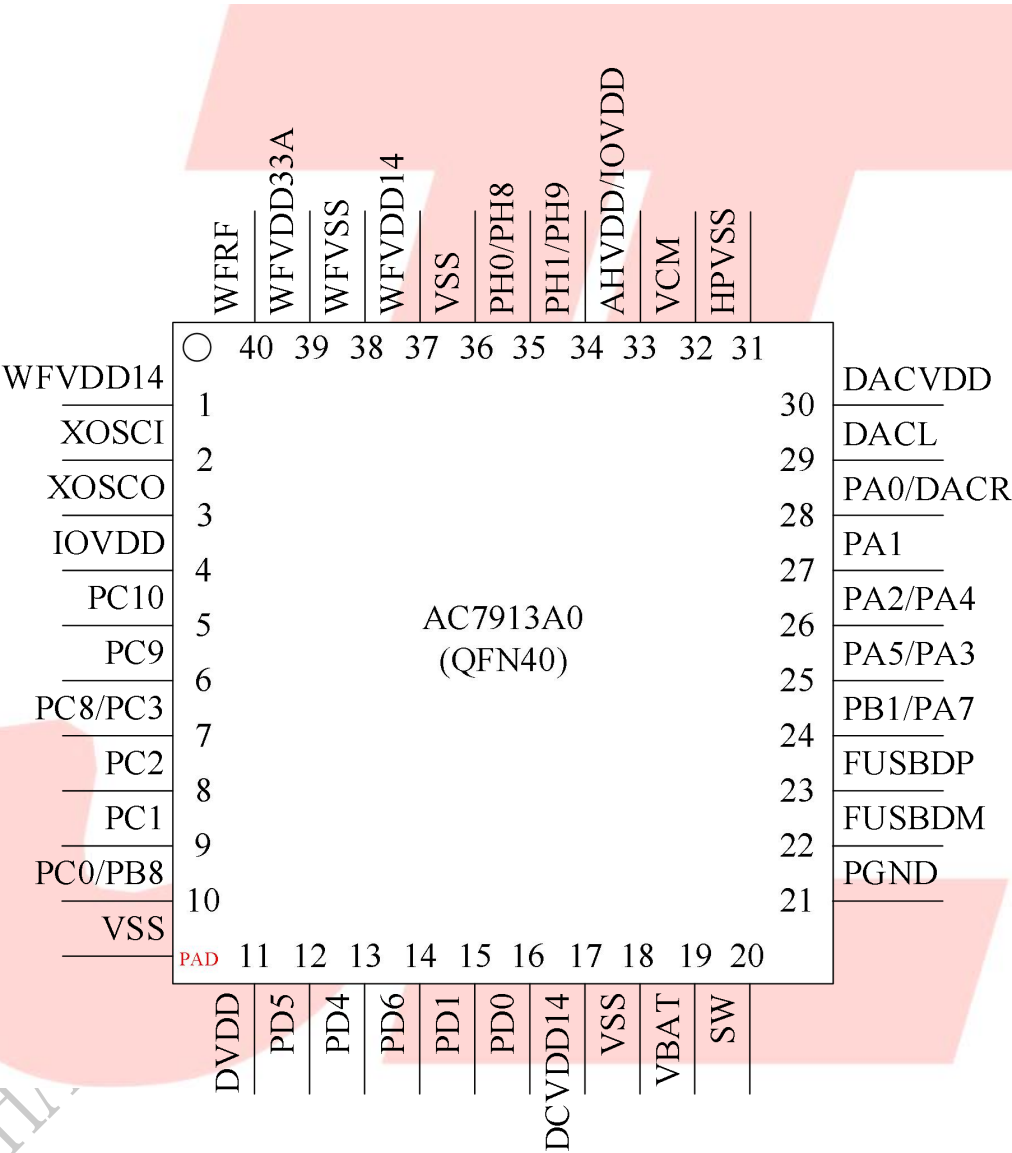
1. Pin Definition

1.1 Pin Assignment

Figure 1-1   AC7913A0_QFN40 Package Diagram

1.2 Pin Description

Table 1-1   AC7913A0_QFN40 Pin Description

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	WFVDD14	P	/	RF Power 1.4V	-
2	XOSCI	I	/	RF OSCI	-
3	XOSCO	O	/	RF OSCO	-
4	IOVDD	P	/	IO Power 3.3V	-
5	PC10	I/O	24/16/8/2.4	GPIO	SD0_CLKD: SD0 Clock(D) SPI1_DOB: SPI1 Data Out(B) ISP_DI_B Q-decoder1 UART2_RXB: Uart2 Data In(B) ADC9: ADC Channel 9 TMR5CK(MCPWM) PWM3: Timer3 PWM Output TOUCH10: Touch Input Channel 10 SDTAP_DATA
6	PC9	I/O	24/16/8/2.4	GPIO	SD0_CMDD: SD0 CMD(D) SPI1_CLKB: SPI1 Clock(B) ISP_CLK_B Q-decoder0 UART2_TXB: Uart2 Data Out(B) ADC8: ADC Channel 8 TMR4CK(MCPWM) TOUCH9: Touch Input Channel 9 SDTAP_CLKA
7	PC8	I/O	24/16/8/2.4	GPIO	SD0_DAT0D: SD0 Data0(D) SPI1_DIB: SPI1 Data In(B) SPDIF_B PWMCH2L(MCPWM) CAP5: Timer5 Capture TOUCH8: Touch Input Channel 8
	PC3	I/O	24/16/8/2.4	GPIO	UART1_TXB: Uart1 Data Out(B) ALNK0_DAT0A: Audio Link0 Data0(A) ALNK1_DAT0A: Audio Link1 Data0(A) SD1_DAT1B: SD1 Data1(B) FPIN6(MCPWM) TMR4: Timer4 Clock In TOUCH3: Touch Input Channel 3

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
8	PC2	I/O	24/16/8/2.4	GPIO	IIC_SDA_C: IIC SDA(C) ALNK0_LRCKA: Audio Link0 Word Select(A) ALNK1_LRCKA: Audio Link1 Word Select(A) SD1_DAT0B: SD1 Data0(B) PWMCH4L(MCPWM) CAP1: Timer1 Capture TOUCH2: Touch Input Channel 2
9	PC1	I/O	24/16/8/2.4	GPIO	IIC_SCL_C: IIC SCL(C) ALNK0_SCLKA: Audio Link0 Serial Clock(A) ALNK1_SCLKA: Audio Link1 Serial Clock(A) SD1_CLKB: SD1 Clock(B) ADC7: ADC Channel 7 PWM1: Timer1 PWM Output Wakeup11: Port Wakeup 11 TOUCH1: Touch Input Channel 1
10	PC0	I/O	24/16/8/2.4	GPIO	CLKOUT0: Clock Out0 ALNK0_MCKA: Audio Link0 Master Clock(A) ALNK1_MCKA: Audio Link1 Master Clock(A) SD1_CMDB: SD1 CMD(B) ADC6: ADC Channel 6 PWMCH4H(MCPWM) Wakeup10: Port Wakeup 10 TOUCH0: Touch Input Channel 0
	PB8	I/O	24/16/8/2.4	GPIO	SDGAT: SD Power Gate
11	DVDD	P	/	Core Power 1.2V	-
12	PD5	I/O	24/16/8/2.4	GPIO	SPI0_DOA(0): SPI0 Data Out(A) SFC_DOA(0): SFC Data Out(A)
13	PD4	I/O	24/16/8/2.4	GPIO	SPI0_CLKA: SPI0 Clock(A) SFC_CLKA: SFC Clock(A)
14	PD6	I/O	24/16/8/2.4	GPIO	SFGAT: Flash Power Gate
15	PD1	I/O	24/16/8/2.4	GPIO	SPI0_DIA(1): SPI0 Data In(A) SFC_DIA(1): SFC Data In(A)
16	PD0	I/O	24/16/8/2.4	GPIO (pull up)	SPI0_CSA: SPI0 Chip Select(A) SFC_CSA: SFC Chip Select(A)
17	DCVDD14	P	/	Core Power 1.4V	-
18	VSS	P	/	Ground	-

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
19	VBAT	P	/	LDO Power	-
20	SW	P	/	DC-DC Switch Pin	-
21	PGND	P	/	PMU Ground	-
22	FUSBDM	I/O	10	USB Negative Data (pull down)	UART1_RXD: Uart1 Data In(D) ISP_DI_A SPI2_DOB: SPI2 Data Out(B) IIC_SDA_A: IIC SDA(A) ADC12: ADC Channel 12 SDTAP_DATB
23	FUSBDP	I/O	10	USB Positive Data (pull down)	UART1_TXD: Uart1 Data Out(D) ISP_CLK_A SPI2_CLKB: SPI2 Clock(B) IIC_SCL_A: IIC SCL(A) ADC13: ADC Channel 13 SDTAP_CLKB
24	PB1	I/O	24/16/8/2.4	GPIO (pull up)	ISP_DO UART0_TXB: Uart0 Data Out(B) ADC3: ADC Channel 3 Long Press reset TMR1: Timer1 Clock In Wakeup8: Port Wakeup 8
24	PA7	I/O	24/16/8/2.4	GPIO	SPDIF_C ADC0: ADC Channel 0 PWMCH1H(MCPWM) TMR0: Timer0 Clock In Wakeup3: Port Wakeup 3 SDTAP_CLKD
25	PA5	I/O	24/16/8/2.4	GPIO	UART0_TXA: Uart0 Data Out(A) AMUX2: Simulator Channel 2 CAP3: Timer3 Capture
25	PA3	I/O	24/16/8/2.4	GPIO	SPI2_CLKC: SPI2 Clock(C) MIC2P: MIC2 P Channel UART0_TXC: Uart0 Data Out(C) PWMCH0H(MCPWM)
26	PA2	I/O	24/16/8/2.4	GPIO	MIC0P: MIC0 P Channel TMR0CK(MCPWM)
26	PA4	I/O	24/16/8/2.4	GPIO	CLKOUT1: Clock Out1 SPI2_DOC: SPI2 Data Out(C) MIC2N: MIC2 N Channel UART0_RXC: Uart0 Data In(C) PWMCH0L(MCPWM)

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
27	PA1	I/O	24/16/8/2.4	GPIO	MIC0N: MIC0 N Channel PWM0: Timer0 PWM Output
28	PA0	I/O	24/16/8/2.4	GPIO	AMUX0: Simulator Channel 0 TMR1CK(MCPWM) Wakeup2: Port Wakeup 2
	DACR	O	/	DAC Right Channel	-
29	DACL	O	/	DAC Left Channel	-
30	DACVDD	P	/	DAC Power	-
31	HPVSS	P	/	Audio Ground	-
32	VCM	P	/	VCM	-
33	AHVDD	P	/	Audio Power	-
	IOVDD	P	/	IO Power 3.3V	-
34	PH1	I/O	24/16/8/2.4	GPIO	IIC_SDA_D: IIC SDA(D) SPI2_DOA: SPI2 Data Out(A) UART0_RXD: Uart0 Data In(D) PWMCH3L(MCPWM) TOUCH12: Touch Input Channel 12
	PH9	I/O	24/16/8/2.4	GPIO	MIC1P: MIC1 P Channel
35	PH0	I/O	24/16/8/2.4	GPIO	IIC_SCL_D: IIC SCL(D) SPI2_CLKA: SPI2 Clock(A) UART0_TXD: Uart0 Data Out(D) ADC10: ADC Channel 10 PWMCH3H(MCPWM) Wakeup12: Port Wakeup 12 TOUCH11: Touch Input Channel 11
	PH8	I/O	24/16/8/2.4	GPIO	MIC1N: MIC1 N Channel
36	VSS	P	/	Ground	-
37	WFVDD14	P	/	RF Power 1.4V	-
38	WFVSS	P	/	RF Ground	-
39	WFVDD33A	P	/	RF Power 3.3V	-
40	WFRF	-	/	RF Antenna	-
	PAD	P	/	VSS	-

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	5.5	V
WFVDD33A	RF Power 3.3V Voltage	-0.3	3.5	V
AHVDD	Audio Power Voltage	-0.3	3.5	V
WFVDD14	RF Power 1.4V Voltage	-0.3	1.55	V
$V_{3.3IO}$	3.3V IO Input Voltage	-0.3	IOVDD+0.3	V

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	5.5	V	_
IOVDD	Voltage output	2.1	3.3	3.5	V	LDO5V = 5V, 200mA loading
DCVDD14	Voltage output	1.2	1.4	1.55	V	LDO mode: 70mA loading DC-DC mode: 120mA loading
DVDD	Voltage output	0.87	1.2	1.32	V	LDO5V=5V, 100mA loading
WFVDD33A	Voltage Input	2.1	3.3	3.5	V	_
AHVDD	Voltage Input	2.1	3.3	3.5	V	_
WFVDD14	Voltage Input	1.2	1.4	1.55	V	_

2.3 IO Input/Output Electrical Logical Characteristics

Table 2-3

IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	–	0.3* IOVDD	V	IOVDD = 3.3V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	–	IOVDD+0.3	V	IOVDD = 3.3V
IO output characteristics						
V_{OL}	Low-Level Output Voltage	–	–	0.33	V	IOVDD = 3.3V
V_{OH}	High-Level Output Voltage	2.7	–	–	V	IOVDD = 3.3V

2.4 Internal Resistor Characteristics

Table 2-4

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA,PC,PD, PH, PB1,PB8	8mA	24mA	10K	10K	1.PB1&PD0 default pull up 2.FUSBDM & FUSBDP default pull down
FUSBDP FUSBDM	10mA	–	1.5K	15K	3. Internal pull-up/pull-down resistance | accuracy ±20%

2.5 DAC Characteristics

Table 2-5

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	_	20K	Hz	
THD+N	_	-72	_	dB	1KHz/0dB
S/N	_	99	_	dB	10Kohm loading
Crosstalk	_	-90	_	dB	With A-Weighted Filter
Output Swing	_	0.9	_	Vrms	
Dynamic Range	_	93	_	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
DAC Output Power	15	_	_	mW	32ohm loading

2.6 ADC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	_	87	_	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
S/N	_	90	_	dB	1KHz/0dB
THD+N	_	-72	_	dB	10Kohm loading
Crosstalk	_	-80	_	dB	With A-Weighted Filter

3. Package Information

3.1 QFN40(5mm*5mm)

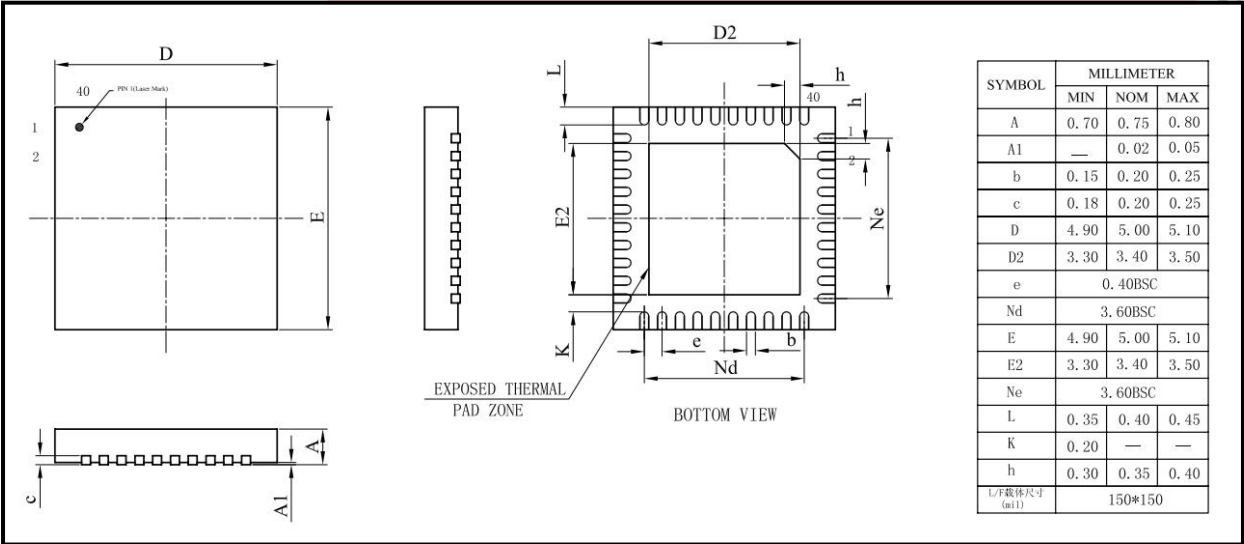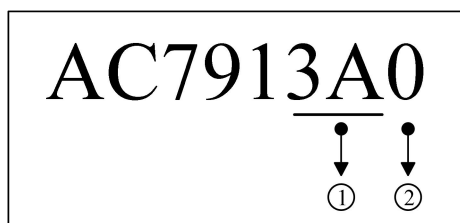| SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.50
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
Ne	3.60BSC		
L	0.35	0.40	0.45
K	0.20	—	—
h	0.30	0.35	0.40
L/F载体尺寸(mil)	150*150		

Figure 3-1　AC7913A0_QFN40 Package

4. Package Type Specification

AC7913<u>A</u><u>0</u>
        ①   ②

①Represents different chips (different packages or bindings)

②Represents different memory sizes

    0: No memory

    2: 2Mbit Flash

    4: 4Mbit Flash

    8: 8Mbit Flash

    6: 16Mbit Flash

    3: 32Mbit Flash

    5: 64Mbit Flash

    7: 128Mbit Flash

    A: 1Mx16 SDRAM

    B: 4Mx16 SDRAM

    C: 16M bit PSRAM

    D: 64M bit PSRAM

5. Revision History

Date	Revision	Description
2021.10.08	V1.0	Initial Release