AC7902A Datasheet

Zhuhai Jieli Technology Co.,LTD

Version：V1.2

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AC7902A Features

High performance 32-bit RISC CPU

- Double core RISC 32-bit CPU(Support FPU)
- 24KB D-Cache 6 way, 32KB I-Cache 8way
- DC-280MHz operation
- 128 Vectored interrupts
- Four Levels interrupt priority

Image Signal Processor

- Support DVP and BT656 interface timing
- Support YUV422 format (Input)
- Support YUV422 and YUV420 format (Output)
- Support 720p@30fps input size

Flexible I/O

- 46 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level Schmitt triggered input
- External wake up/interrupt on all GPIOs

Peripheral Feature

- USB 1.1 OTG controller
- Audio interface supports IIS, left adjusted, right adjusted and DSP mode
- Multi-function 32-bit timers, support capture and PWM mode
- 16-bit PWM generator for motor driving
- 16-bit active parallel port
- Three full-duplex advanced UART
- Three SPI interface supports host and device mode
- Two SD Card Host controller
- One IIC interface supports host and device mode
- One SPDIF receiving interface without analog amplify
- One Quadrate decoder
- Watchdog
- Two Crystal Oscillator
- Two channels 16-bit DAC with headphone amplifier
- Four channels Audio 16-bit ADC
- Four channels MIC amplifier
- Four channels analog MUX
- Fourteen channels 10-bit ADC
- Power-on reset
- Embedded PMU support low power mode

Bluetooth Feature

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth V5.0+BR+EDR+ BLE specification
- Bluetooth Piconet and Scatternet support
- Meet class2 and class3 transmitting power requirement
- Support GFSK and π/4 DQPSK all paket types
- Provides +15dbm transmitting power
- Receiver with -93dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp \att\gap\gatt\rfcomm\sdp\l2cap profile

WIFI Feature

- Support all mandatory IEEE 802.11b data rates of 1, 2, 5.5 and 11 Mbps, all 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11n MCS0~ MCS7, 20MHz, 800ns and 400ns guard interval.
- Support advanced 1x1 802.11n features:
  Full / Half Guard Interval
  Frame Aggregation
  Reduced Inter-frame Space (RIFS)
  Space Time Block Coding (STBC)
  Greenfield mode

- Support WEP/WPA-PSK(TKIP/CCMP)/WPA2-PSCK AES256/AES128/SHA256/SHA128
- Support apply to AP/STA
- Transmitter power:

DSSS 1M/S	17	dBm
MCS0	15	dBm
MCS7	12	dBm

- Receiver sensitivity:

DSSS 1M/S	-95	dBm
MCS0	-93	dBm
MCS7	-72	dBm

Power Supply

- VBAT is 2.2V to 5.5V
- VDDIO is 2.1V to 3.6V
- AVDDHP is 2.1V to 3.6V

Packages

- QFN68(8mm*8mm)

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

1. Pin Definition

1.1 Pin Assignment

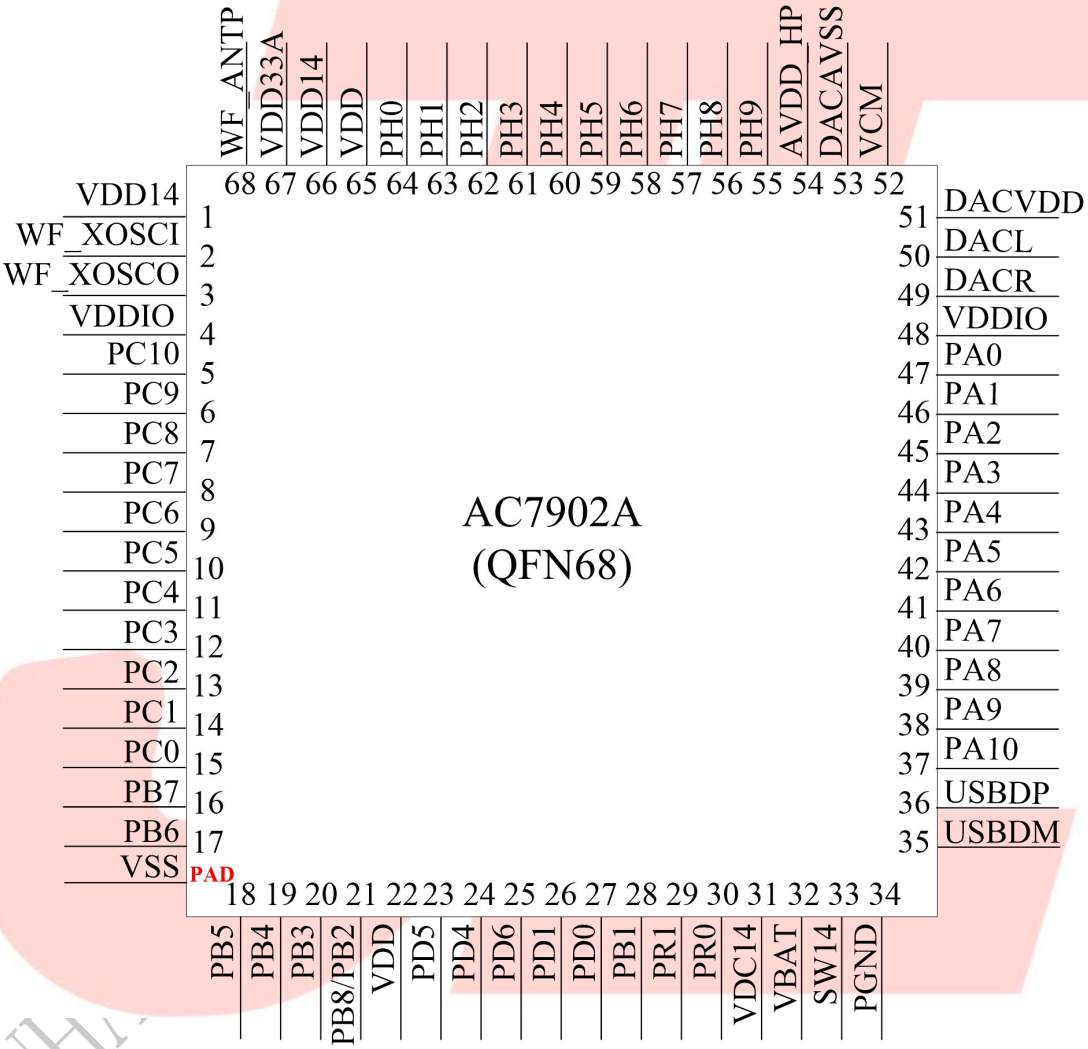


Figure 1-1 AC7902A_QFN68 Package Diagram

1.2 Pin Description

Table 1-1 AC7902A_QFN68 Pin Description

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	VDD14	P	/	RF Power 1.4V	-
2	WF_XOSCI	I	/	RF OSCI	-
3	WF_XOSCO	O	/	RF OSCO	-
4	VDDIO	P	/	IO Power 3.3V	-
5	PC10	I/O	24/16/8/2.4	GPIO	SENSOR_VSYN_B: Sensor Vertical Synchronization(B) SD0_CLKD: SD0 Clock(D) EMI_WR: EMI Write PAP_RD_A: PAP Read(A) SPI1_DOB: SPI1 Data Out(B) Q-decoder1 UART2_RXB: Uart2 Data In(B) ADC9: ADC Channel 9 TMR5CK(MCPWM) PWM3: Timer3 PWM Output TOUCH10: Touch Input Channel 10
6	PC9	I/O	24/16/8/2.4	GPIO	SENSOR_HSYN_B: Sensor Horizontal Synchronization(B) SD0_CMDD: SD0 CMD(D) PAP_WR_A: PAP Write(A) SPI1_CLKB: SPI1 Clock(B) Q-decoder0 UART2_TXB: Uart2 Data Out(B) ADC8: ADC Channel 8 TMR4CK(MCPWM) TOUCH9: Touch Input Channel 9
7	PC8	I/O	24/16/8/2.4	GPIO	SENSOR_CLK_B: Sensor Clock(B) SD0_DAT0D: SD0 Data0(D) EMI_D7: EMI Data7 PAP_D15_A: PAP Data15(A) SPI1_DIB: SPI1 Data In(B) SPDIF_B PWMCH2L(MCPWM) CAP5: Timer5 Capture TOUCH8: Touch Input Channel 8

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
8	PC7	I/O	24/16/8/2.4	GPIO	SENSOR_D7_B: Sensor Data7(B) SD0_DAT1D: SD0 Data1(D) EMI_D6: EMI Data6 PAP_D14_A: PAP Data14(A) SPDIF_A PWMCH2H(MCPWM) CAP4: Timer4 Capture TOUCH7: Touch Input Channel 7
9	PC6	I/O	24/16/8/2.4	GPIO	SENSOR_D6_B: Sensor Data6(B) SD0_DAT2D: SD0 Data2(D) EMI_D5: EMI Data5 PAP_D13_A: PAP Data13(A) ALNK0_DAT3A: Audio Link0 Data3(A) ALNK1_DAT3A: Audio Link1 Data3(A) TMR3CK(MCPWM) PWM5: Timer5 PWM Output TOUCH6: Touch Input Channel 6
10	PC5	I/O	24/16/8/2.4	GPIO	SENSOR_D5_B: Sensor Data5(B) SD0_DAT3D: SD0 Data3(D) EMI_D4: EMI Data4 PAP_D12_A: PAP Data12(A) ALNK0_DAT2A: Audio Link0 Data2(A) ALNK1_DAT2A: Audio Link1 Data2(A) SPI0_CSB: SPI0 Chip Select(B) SD1_DAT3B: SD1 Data3(B) TMR2CK(MCPWM) PWM4: Timer4 PWM Output TOUCH5: Touch Input Channel 5
11	PC4	I/O	24/16/8/2.4	GPIO	SENSOR_D4_B: Sensor Data4(B) UART1_RXB: Uart1 Data In(B) EMI_D3: EMI Data3 PAP_D11_A: PAP Data11(A) ALNK0_DAT1A: Audio Link0 Data1(A) ALNK1_DAT1A: Audio Link1 Data1(A) SPI0_DOB(0): SPI0 Data Out(B) SD1_DAT2B: SD1 Data2(B) FPIN7(MCPWM) TMR5: Timer5 Clock In TOUCH4: Touch Input Channel 4

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
12	PC3	I/O	24/16/8/2.4	GPIO	SENSOR_D3_B: Sensor Data3(B) UART1_TXB: Uart1 Data Out(B) EMI_D2: EMI Data2 PAP_D10_A: PAP Data10(A) ALNK0_DAT0A: Audio Link0 Data0(A) ALNK1_DAT0A: Audio Link1 Data0(A) SPI0_CLKB: SPI0 Clock(B) SD1_DAT1B: SD1 Data1(B) FPIN6(MCPWM) TMR4: Timer4 Clock In TOUCH3: Touch Input Channel 3
13	PC2	I/O	24/16/8/2.4	GPIO	SENSOR_D2_B: Sensor Data2(B) IIC_SDA_C: IIC SDA(C) EMI_D1: EMI Data1 PAP_D9_A: PAP Data9(A) ALNK0_LRCKA: Audio Link0 Word Select(A) ALNK1_LRCKA: Audio Link1 Word Select(A) SPI0_DAT3B(3): SPI0 Data3 In(B) SD1_DAT0B: SD1 Data0(B) PWMCH4L(MCPWM) CAP1: Timer1 Capture TOUCH2: Touch Input Channel 2
14	PC1	I/O	24/16/8/2.4	GPIO	SENSOR_D1_B: Sensor Data1(B) IIC_SCL_C: IIC SCL(C) EMI_D0: EMI Data0 PAP_D8_A: PAP Data8(A) ALNK0_SCLKA: Audio Link0 Serial Clock(A) ALNK1_SCLKA: Audio Link1 Serial Clock(A) SPI0_DAT2B(2): SPI0 Data2 In(B) SD1_CLKB: SD1 Clock(B) ADC7: ADC Channel 7 PWM1: Timer1 PWM Output Wakeup11: Port Wakeup 11 TOUCH1: Touch Input Channel 1

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
15	PC0	I/O	24/16/8/2.4	GPIO	SENSOR_D0_B: Sensor Data0(B) CLKOUT0: Clock Out0 ALNK0_MCKA: Audio Link0 Master Clock(A) ALNK1_MCKA: Audio Link1 Master Clock(A) SPI0_DIB(1): SPI0 Data In(B) SD1_CMDB: SD1 CMD(B) ADC6: ADC Channel 6 PWMCH4H(MCPWM) Wakeup10: Port Wakeup 10 TOUCH0: Touch Input Channel 0
16	PB7	I/O	24/16/8/2.4	GPIO	UART1_RTS:Uart1 Receive Bit Stream Control SD0_CLKA: SD0 Clock(A) SPI1_DOA: SPI1 Data Out(A) UART2_RXC: Uart2 Data In(C) ADC5: ADC Channel 5 PWMCH7L(MCPWM) SDTAP_DATC
17	PB6	I/O	24/16/8/2.4	GPIO	UART1_CTS:Uart1 Transmit Bit Stream Control SD0_CMDA: SD0 CMD(A) SPI1_CLKA: SPI1 Clock(A) UART2_TXC: Uart2 Data Out(C) ADC4: ADC Channel 4 PWMCH7H(MCPWM) Wakeup9: Port Wakeup 9 SDTAP_CLKC
18	PB5	I/O	8	GPIO (High Voltage Resistance)	PLNK0_DAT1: PLNK0 Data1 SD0_DAT0A: SD0 Data0(A) PLNK1_DAT1: PLNK1 Data1 SPI1_DIA: SPI1 Data In(A) FPIN2(MCPWM) CAP0: Timer0 Capture
19	PB4	I/O	8	GPIO (High Voltage Resistance)	SD0_DAT1A: SD0 Data1(A) PLNK1_SCLK: PLNK1 Serial Clock FPIN1(MCPWM) TMR2: Timer2 Clock In

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
20	PB3	I/O	8	GPIO (High Voltage Resistance)	PLNK0_SCLK: PLNK0 Serial Clock SD0_DAT2A: SD0 Data2(A) PWMCH6L(MCPWM)
21	PB2	I/O	8	GPIO (High Voltage Resistance)	PLNK0_DAT0: PLNK0 Data0 SD0_DAT3A: SD0 Data3(A) PLNK1_DAT0: PLNK1 Data0 UART0_RXB: Uart0 Data In(B) PWMCH6H(MCPWM) CAP2: Timer2 Capture
	PB8	I/O	24/16/8/2.4	GPIO	SDGAT: SD Power Gate
22	VDD	P	/	Core Power 1.2V	-
23	PD5	I/O	24/16/8/2.4	GPIO	SPI0_DOA(0): SPI0 Data Out(A) SFC_DOA(0): SFC Data Out(A)
24	PD4	I/O	24/16/8/2.4	GPIO	SPI0_CLKA: SPI0 Clock(A) SFC_CLKA: SFC Clock(A)
25	PD6	I/O	24/16/8/2.4	GPIO	SFGAT: Flash Power Gate
26	PD1	I/O	24/16/8/2.4	GPIO	SPI0_DIA(1): SPI0 Data In(A) SFC_DIA(1): SFC Data In(A)
27	PD0	I/O	24/16/8/2.4	GPIO (pull up)	SPI0_CSA: SPI0 Chip Select(A) SFC_CSA: SFC Chip Select(A)
28	PB1	I/O	24/16/8/2.4	GPIO (pull up)	ISP_DO UART0_TXB: Uart0 Data Out(B) ADC3: ADC Channel 3 Long Press reset TMR1: Timer1 Clock In Wakeup8: Port Wakeup 8
29	PR1	I/O	16/2.4	RTCIO1	OSC32KO
30	PR0	I/O	16/2.4	RTCIO0	OSC32KI
31	VDC14	P	/	Core Power 1.4V	-
32	VBAT	P	/	LDO Power	-
33	SW14	P	/	DC-DC Switch Pin	-
34	PGND	P	/	PMU Ground	
35	USBDM	I/O	10	USB Negative Data (pull down)	UART1_RXD: Uart1 Data In(D) ISP_DI_A SPI2_DOB: SPI2 Data Out(B) IIC_SDA_A: IIC SDA(A) ADC12: ADC Channel 12 SDTAP_DATB

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
36	USBDP	I/O	10	USB Positive Data (pull down)	UART1_TXD: Uart1 Data Out(D) ISP_CLK_A SPI2_CLKB: SPI2 Clock(B) IIC_SCL_A: IIC SCL(A) ADC13: ADC Channel 13 SDTAP_CLKB
37	PA10	I/O	24/16/8/2.4	GPIO	SENSOR_VSYN_A: Sensor Vertical Synchronization(A) SD0_DAT1B: SD0 Data1(B) ALNK0_DAT3B1: Audio Link0 Data3(B1) ALNK1_DAT3B1: Audio Link1 Data3(B1) ADC2: ADC Channel 2 TMR7CK(MCPWM)
38	PA9	I/O	24/16/8/2.4	GPIO	SENSOR_HSYN_A: Sensor Horizontal Synchronization(A) SD0_DAT0B: SD0 Data0(B) ALNK0_DAT2B1: Audio Link0 Data2(B1) ALNK1_DAT2B1: Audio Link1 Data2(B1) TMR6CK(MCPWM)
39	PA8	I/O	24/16/8/2.4	GPIO	SENSOR_CLK_A: Sensor Clock(A) IIC_SDA_B: IIC SDA(B) SD0_CLKB: SD0 Clock(B) ALNK0_DAT1B1: Audio Link0 Data1(B1) ALNK1_DAT1B1: Audio Link1 Data1(B1) SPDIF_D ADC1: ADC Channel 1 PWMCH1L(MCPWM) Wakeup4: Port Wakeup 4 SDTAP_DATD
40	PA7	I/O	24/16/8/2.4	GPIO	SENSOR_D7_A: Sensor Data7(A) IIC_SCL_B: IIC SCL(B) SD0_CMDB: SD0 CMD(B) ALNK0_DAT0B1: Audio Link0 Data0(B1) ALNK1_DAT0B1: Audio Link1 Data0(B1) SPDIF_C ADC0: ADC Channel 0 PWMCH1H(MCPWM) TMR0: Timer0 Clock In Wakeup3: Port Wakeup 3 SDTAP_CLKD

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
41	PA6	I/O	24/16/8/2.4	GPIO	SENSOR_D6_A: Sensor Data6(A) UART0_RXA: Uart0 Data In(A) SD0_DAT3B: SD0 Data3(B) ALNK0_LRCKB1: Audio Link0 Word Select (B1) ALNK1_LRCKB1: Audio Link1 Word Select(B1) FPIN0(MCPWM)
42	PA5	I/O	24/16/8/2.4	GPIO	SENSOR_D5_A: Sensor Data5(A) UART0_TXA: Uart0 Data Out(A) SD0_DAT2B: SD0 Data2(B) AMUX2: Simulator Channel 2 ALNK0_SCLKB1: Audio Link0 Serial Clock(B1) ALNK1_SCLKB1: Audio Link1 Serial Clock(B1) CAP3: Timer3 Capture
43	PA4	I/O	24/16/8/2.4	GPIO	SENSOR_D4_A: Sensor Data4(A) CLKOUT1: Clock Out1 SPI2_DOC: SPI2 Data Out(C) MIC2N: MIC2 N Channel ALNK0_MCKB1: Audio Link0 Master Clock(B1) ALNK1_MCKB1: Audio Link1 Master Clock(B1) UART0_RXC: Uart0 Data In(C) PWMCH0L(MCPWM)
44	PA3	I/O	24/16/8/2.4	GPIO	SENSOR_D3_A: Sensor Data3(A) SPI2_CLKC: SPI2 Clock(C) MIC2P: MIC2 P Channel UART0_TXC: Uart0 Data Out(C) PWMCH0H(MCPWM)
45	PA2	I/O	24/16/8/2.4	GPIO	SENSOR_D2_A: Sensor Data2(A) SPI2_DIC: SPI2 Data In(C) MIC0P: MIC0 P Channel TMR0CK(MCPWM)
46	PA1	I/O	24/16/8/2.4	GPIO	SENSOR_D1_A: Sensor Data1(A) MIC0N: MIC0 N Channel PWM0: Timer0 PWM Output
47	PA0	I/O	24/16/8/2.4	GPIO	SENSOR_D0_A: Sensor Data0(A) AMUX0: Simulator Channel 0 TMR1CK(MCPWM) Wakeup2: Port Wakeup 2

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
48	VDDIO	P	/	IO Power 3.3V	-
49	DACR	O	/	DAC Right Channel	-
50	DACL	O	/	DAC Left Channel	-
51	DACVDD	P	/	DAC Power	-
52	VCM	P	/	VCM	-
53	AVSS_HP	P	/	Audio Ground	-
54	AVDD_HP	P	/	Audio Power	-
55	PH9	I/O	24/16/8/2.4	GPIO	MIC1P: MIC1 P Channel
56	PH8	I/O	24/16/8/2.4	GPIO	MIC1N: MIC1 N Channel
57	PH7	I/O	24/16/8/2.4	GPIO	AMUX1: Simulator Channel 1 UART1_RXA: Uart1 Data In(A) PAP_D7_AB: PAP Data7(AB) SD1_CLKA: SD1 Clock(A) PWMCH5L(MCPWM) Wakeup13: Port Wakeup 13
58	PH6	I/O	24/16/8/2.4	GPIO	MIC3P: MIC3 P Channel UART1_TXA: Uart1 Data Out(A) PAP_D6_AB: PAP Data6(AB) SD1_CMDA: SD1 CMD(A) FPIN3(MCPWM) PWM2: Timer2 PWM Output
59	PH5	I/O	24/16/8/2.4	GPIO	MIC3N: MIC3 N Channel SD0_DAT3C: SD0 Data3(C) PAP_D5_AB: PAP Data5(AB) SD1_DAT0A: SD1 Data0(A) FPIN5(MCPWM)
60	PH4	I/O	24/16/8/2.4	GPIO	AMUX3: Simulator Channel 3 SD0_DAT2C: SD0 Data2(C) PAP_D4_AB: PAP Data4(AB) SD1_DAT1A: SD1 Data1(A) FPIN4(MCPWM)
61	PH3	I/O	24/16/8/2.4	GPIO	SD0_DAT1C: SD0 Data1(C) PAP_D3_AB: PAP Data3(AB) UART2_RXA: Uart2 Data In(A) SD1_DAT2A: SD1 Data2(A) ADC11: ADC Channel 11 PWMCH5H(MCPWM) TOUCH14: Touch Input Channel 14

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
62	PH2	I/O	24/16/8/2.4	GPIO	SD0_CLKC: SD0 Clock(C) PAP_D2_AB: PAP Data2(AB) SPI2_DIA: SPI2 Data In(A) UART2_TXA: Uart2 Data Out(A) SD1_DAT3A: SD1 Data3(A) TOUCH13: Touch Input Channel 13
63	PH1	I/O	24/16/8/2.4	GPIO	IIC_SDA_D: IIC SDA(D) SD0_CMDC: SD0 CMD(C) PAP_D1_AB: PAP Data1(AB) SPI2_DOA: SPI2 Data Out(A) UART0_RXD: Uart0 Data In(D) PWMCH3L(MCPWM) TOUCH12: Touch Input Channel 12
64	PH0	I/O	24/16/8/2.4	GPIO	IIC_SCL_D: IIC SCL(D) SD0_DAT0C: SD0 Data0(C) PAP_D0_AB: PAP Data0(AB) SPI2_CLKA: SPI2 Clock(A) UART0_TXD: Uart0 Data Out(D) ADC10: ADC Channel 10 PWMCH3H(MCPWM) Wakeup12: Port Wakeup 12 TOUCH11: Touch Input Channel 11
65	VDD	P	/	Core Power 1.2V	-
66	VDD14	P	/	RF Power 1.4V	-
67	VDD33A	P	/	RF Power 3.3V	-
68	WF_ANTP	-	/	RF Antenna	-
PAD		P	/	VSS	-

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-40	+85	℃
Tstg	Storage temperature	-65	+150	℃
VBAT	Supply Voltage	-0.3	5.5	V
VDD33A	RF Power 3.3V Voltage	-0.3	3.6	V
AVDDHP	Audio Power Voltage	-0.3	3.6	V
VDD14	RF Power 1.4V Voltage	-0.3	1.55	V
$V_{3.3IO}$	3.3V IO Input Voltage	-0.3	VDDIO+0.3	V

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	5.5	V	_
VDDIO	Voltage output	2.1	3.3	3.6	V	LDO5V = 5V, 200mA loading
VDC14	Voltage output	1.2	1.4	1.55	V	LDO mode: 70mA loading DC-DC mode: 120mA loading
VDD	Voltage output	0.87	1.2	1.32	V	LDO5V=5V, 100mA loading
VDD33A	Voltage Input	2.1	3.3	3.6	V	_
AVDDHP	Voltage Input	2.1	3.3	3.6	V	_
VDD14	Voltage Input	1.2	1.4	1.55	V	_

2.3 IO Input/Output Electrical Logical Characteristics

Table 2-3

IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	–	0.3* VDDIO	V	VDDIO = 3.3V
V_{IH}	High-Level Input Voltage	0.7* VDDIO	–	VDDIO+0.3	V	VDDIO = 3.3V
IO output characteristics						
V_{OL}	Low-Level Output Voltage	–	–	0.33	V	VDDIO = 3.3V
V_{OH}	High-Level Output Voltage	2.7	–	–	V	VDDIO = 3.3V

2.4 Internal Resistor Characteristics

Table 2-4

Port	**General Output**	**High Drive**	**Internal Pull-Up Resistor**	**Internal Pull-Down Resistor**	**Comment**
PA,PC, PD,PH, PB1,PB6, PB7,PB8	8mA	24mA	10K	10K	1.PB1&PD0 default pull up 2.USBDM & USBDP default pull down 3. Internal pull-up/pull-down resistance | accuracy ±20%
PB2,PB3, PB4,PB5	8mA	–	10K	10K	
PR0,PR1	2.4mA	16mA	10K	10K	
USBDP USBDM	10mA	–	1.5K	15K	

2.5 DAC Characteristics

Table 2-5

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	_	20K	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	_	-78	_	dB	
S/N	_	92	_	dB	
Crosstalk	_	-80	_	dB	
Output Swing	_	0.75	_	Vrms	
Dynamic Range	_	90	_	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
DAC Output Power	11	_	_	mW	32ohm loading

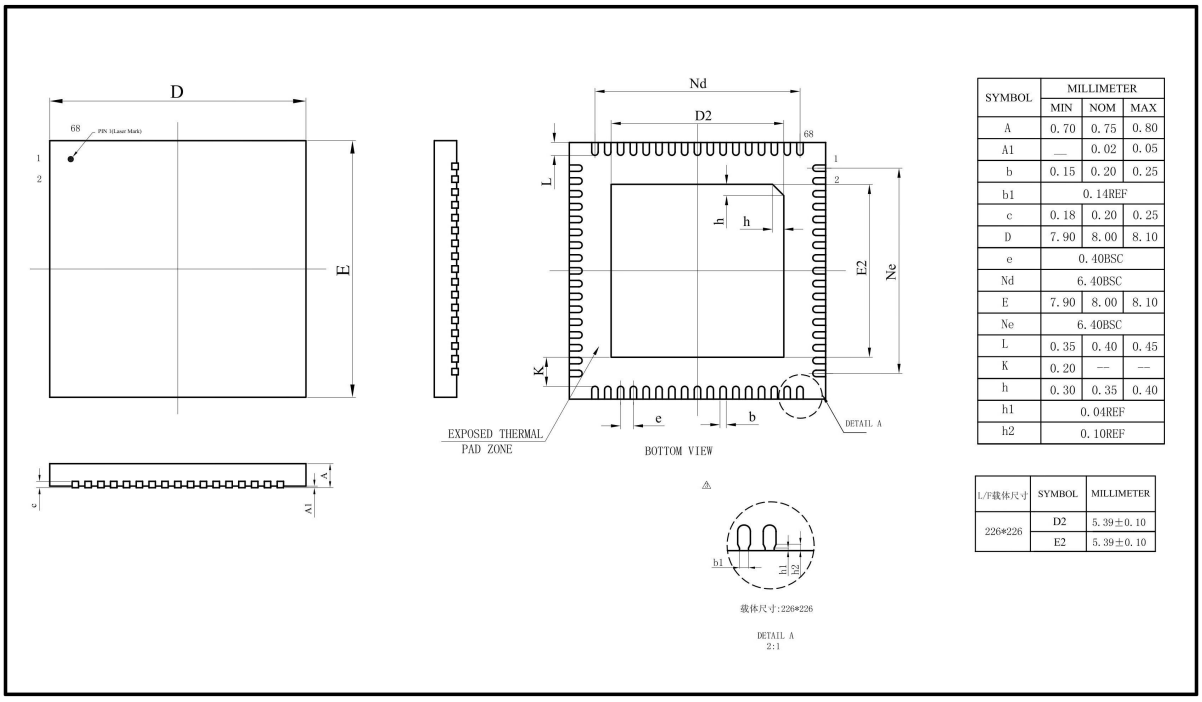
2.6 ADC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	_	87	_	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
S/N	_	90	_	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
THD+N	_	-72	_	dB	
Crosstalk	_	-80	_	dB	

3. Package Information

3.1 QFN68(8mm*8mm)

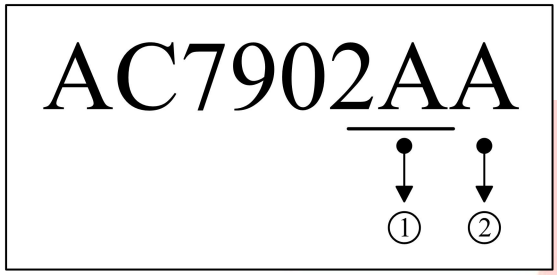


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.25
D	7.90	8.00	8.10
e	0.40BSC		
Nd	6.40BSC		
E	7.90	8.00	8.10
Ne	6.40BSC		
L	0.35	0.40	0.45
K	0.20	—	—
h	0.30	0.35	0.40
h1	0.04REF		
h2	0.10REF		

L/F载体尺寸	SYMBOL	MILLIMETER
226*226	D2	5.39±0.10
	E2	5.39±0.10

Figure 3-1 AC7902A_QFN68 Package

4. Package Type Specification



①Represents different chips (different packages or bindings)

②Represents different memory sizes

0: No memory
2: 2Mbit Flash
4: 4Mbit Flash
8: 8Mbit Flash
6: 16Mbit Flash
3: 32Mbit Flash
5: 64Mbit Flash
7: 128Mbit Flash
A: 1Mx16 SDRAM
B: 4Mx16 SDRAM
C: 16M bit PSRAM
D: 64M bit PSRAM

5. Revision History

Date	Revision	Description
2019.12.04	V1.0	Initial Release
2020.05.19	V1.1	Update Format
2021.06.02	V1.2	Modify transmit power parameters Modify DAC performance parameters Modify the absolute maximum rating Delete the PF and PG port driver descriptions in Table 2-4