# 14 Things Your Fab-House Needs to Know





The artwork behind the physical PCB is one thing — the fab drawing is the other. Fab drawing conveys the physical and the electrical properties manifest in the "Gerber data" circuit pattern. Neither is complete without the other.

# Defining options and exceptions is the job of the notes.

While there are specifications that drive the process, there are nearly unlimited options within those specs. There is a rule for everything, but there is also an exception to nearly every one of those rules. Defining these options and exceptions is the job of the notes or as the terminology goes...

# NOTES: UNLESS OTHERWISE SPECIFIED.

"Otherwise specified" are the weasel words that allow for a hierarchy of cascading rules. The legal and contractual documents live at the top of the chain, followed by supporting purchase orders, and then the specific design notes with the standards forming the base of the pyramid. It's the design notes that populate the fabrication drawing as well as the assembly drawing — which we'll cover at another time.

General fabrication notes for rigid boards can be gleaned from the IPC-6012, while IPC-6013 covers flex circuits. IPC-600 is an umbrella document concerning workmanship across the board. By reference, dozens of other standards also apply — unless otherwise specified. So, our goal with the creation of the notes is to increase Design For Manufacturability (DFM), while adhering to the higher level goals handed down by the laws on the land, the contract, and the P.O.

Every note on the fabrication drawing should define something unique about that particular board. One of the first notes on the drawing should define the class of the PCB.



Yes, I play with toys!

If you don't already know, the class stems from the intended use-case and is based on the penalty for failure. If a toy helicopter won't lift off anymore because the battery connector came off, that's a Class 1 use-case which made a child cry. We can tolerate that up to a point.



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If a real estate agent is using a drone to generate fly-over video of a new resort and the drone lawn-darts into the ground, causing the agent to have to go on with the show without the centerpiece footage, it could cause a grown-up to cry. That's a Class 2 issue. We should not have used a Class 1 call-out even if it saved a few bucks on the cost of the drone. Pay to play with Class 2 being the default for most applications.

# And then, there's Class 3

Now, if Marine One is carrying an important person (let's not debate that

here) and it auto-rotates into the rose garden, well, the rose gardener is going to be quite upset. The passenger and pilot may also be ticked and we can't have that, so we ratchet the PCB requirement to Class 3. There's actually something new to me called Class 3A for avionics which will be applied to the <u>stuff I'm doing for autonomous vehicles</u>. Basically, when lives are on the line, we can't take shortcuts.



Getty Images — Tim Brown

Class 3 adds a lot of test coupons to the fabrication panel so that the vendors can perform a whole mess of different tests. The tolerance for defects goes way down, so price and reliability go way up or, at least, we hope so.

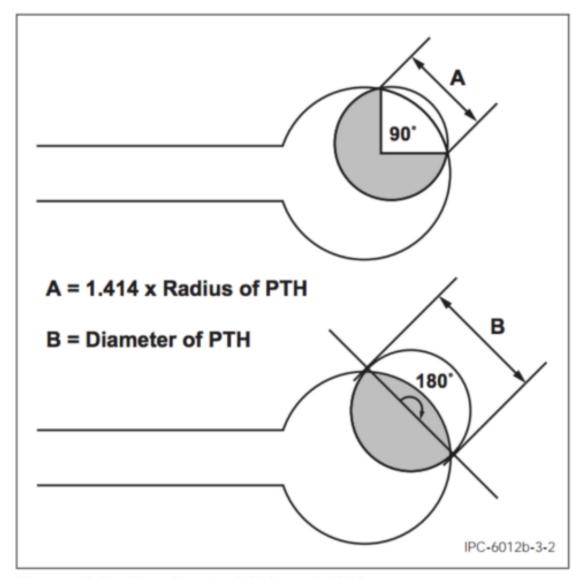


Figure 3-2 Breakout of 90° and 180°

IPC-6012 B

One of the key differentiators of the classes is how the plated holes register within the capture pad. Straight from the relevant IPC spec is this diagram. Class 1 is the bottom of the barrel, with half of the hole escaping the pad. We get root-2 "break-out" for Class 2 and none for Class 3. In fact, we need some metal to spare around the drill in Class 3. A lot of designs adhere to the default Class 2, but then specify tangency instead of allowing break-out. This extra requirement will be in a note.

You can see that specifications will take us in the right direction. From there, we need to address the specifics, such as solder-mask and ink color, dielectric and plating composition, packaging and shipping, and whatever other requirements fall outside of the specs or are not included. Pretty much everything is included, but the industry sometimes gets ahead of the standards body. For example, there are two working groups (one too many) working on specs for Organic Surface Protection (OSP) so at this point, there is no documentation to call-out for this process. This is where an informal chat with your fabricator will help suss out the details.

Let's get down to why you're here in the first place. You're looking for a comprehensive list of notes that have been vetted for accuracy and facilitate DFM.

Think of DFM as "Design For Money," and realize that every note could be a cost driver or a cost saver depending on the actual requirements and end-use case as stated above. Unnecessary notes will overburden the factory while missing ones will leave them calling back for clarity.

In one camp, we have the <u>Occam's razor</u> where the fewer notes, the better. In the other, we have the folks who want to cover every eventuality. Everything that's ever gone wrong ends up with a note to prevent it from happening again. The first page of a Qualcomm fab drawing is nothing but notes, so you know where they stand.

I pen this list of standard notes and then just cross out the ones that do not apply to the board at hand. I'm not shouting — using all-caps is what architects do. Their traditions have been handed down through time. Milspecs probably need it for their traditional micro-film archives to be legible but either way, it's what we do.

### NOTES: UNLESS OTHERWISE SPECIFIED.

- 1. STANDARDS:
- A. FABRICATE PCB IN ACCORDANCE WITH THE CURRENT REVISION OF IPC-6012, CLASS 2.
- B. INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH THE CURRENT REVISION OF ASME Y14.5M.
- C. DO NOT SCALE DRAWING.
- 2. MATERIAL:
- A. FR4 Tg 180 C OR EQUIVALENT.
- B. EQUIVALENT MATERIAL SHALL BE ROHS COMPLIANT, HALOGEN FREE AND APPROVED BY *YourCo*.
- C. THICKNESS OF INDIVIDUAL COPPER CLAD SHEETS SHALL BE IN AS

### DEFINED IN STACK-UP. SEE DETAIL A.

### 3. FLATNESS:

A. BOW AND TWIST OF ASSEMBLY SUB-PANEL OR SINGULATED PWB SHALL NOT EXCEED .025 MM PER MM.

B. TEST IN ACCORDANCE WITH THE CURRENT REVISION OF IPC-TM-650 2.4.22

### 4. ETCH GEOMETRY:

- A. MEASURE WIDTH FROM THE BASE OF THE METALLIZATION.
- B. MINIMUM LINE WIDHT: 0.nn MM OUTER, 0.nn MM INNER LAYERS.
- C. FINISHED LINE WIDTH AND TERMINAL AREA SHALL NOT DEVIATE FROM THE 1-TO-1 MASTER PATTERN IMAGE BY MORE THAN +/-0.025 MM OR 20%, WHICHEVER IS LESS.
- 5. SURFACE FINISH: (SELECT APPROPRIATE FINISH(ES))
  A. ENEPIG PLATING IN ACCORDANCE WITH CURRENT REVISION OF

IPC4556. EXPOSED METAL SHALL HAVE 118–236 MICRO INCHES

ELECTROLESS NICKEL, 2–6 MICRO INCHES ELECTROLESS PALLADIUM, AND 1.2MICRO INCHES GOLD.

B. ENIG PLATING PER CURRENT REVISION OF IPC-4552. EXPOSED METAL SHALL HAVE 118–236 MICRO INCHES ELECTROLESS NICKEL AND 2–5 MICRO INCHES GOLD.

### 6. DESTRUCTIVE TESTING:

A. MICRO SECTION SAMPLE AND REPORT SHALL BE PROVIDED TO YourCo DESIGN ENGINEERING.

- B. SOLDER SAMPLE PROCESSED THROUGH LEAD-FREE SOLDERING SHALL BE INCLUDED WITH EACH SHIPMENT.
- C. X-OUT PANELS MAY BE USED FOR SOLDER SAMPLE.

### 7. HOLES:

- A. PLATING IN HOLES SHALL BE CONTINUOUS ELECTROLYTIC COPPER WITH 0.025 MM MINIMUM BARREL THICKNESS.
- B. MINIMUM FINISHED HOLE SIZE: 0.nn MM
- C. HOLE SIZE MEASURED AFTER PLATING.
- D. SEE DRILL CHART FOR FINISHED HOLE SIZE AND TOLERANCE.
- E. ALL HOLES SHALL BE LOCATED WITHIN 0.08 MM OF TRUE POSITION AS SUPPLIED IN CAD DATA.

# 8. SOLDERMASK:

A. SOLDERMASK OVER BARE COPPER (SMOBC) ON PRIMARY AND SECONDARY SIDES USING SUPPLIED ARTWORK IN ACCORDANCE WITH CURRENT REVISION OF IPC-SM-840 TYPE B.

- B. COLOR: MATTE GREEN
- C. LIQUID PHOTO-IMAGEABLE (LPI) 0.001 MM TO 0.002 MM THICKNESS, HALOGEN FREE
- D. NO BLEED-OUT ALLOWED OVER EXPOSED SMD PADS.
- E. NO EXPOSED TRACES.

# 9. SILKSCREEN:

A. SILKSCREEN PRIMARY AND SECONDARY SIDE WITH WHITE EPOXY, NON-CONDUCTIVE, NON-NUTRIENT INK.

B. ANY UNSPECIFIED STROKE WIDTH SHALL BE 0.13 MM

- C. CLIP SILKSCREEN AWAY FROM ANY EXPOSED METAL.
- D. VENDOR DATE CODE, LOGO, UL AND ANY ADDITIONAL MARKING TO BE LOCATED ON THE SECONDARY SIDE.
- E. BAG AND TAG ACCEPTABLE FOR PWBS THAT ARE TOO SMALL FOR MARKING.
- 10. REMOVE ALL BURRS AND BREAK SHARP EDGES R0.003 MIN.
- 11. NON-DESTRUCTIVE EVALUATION:
- A. ALL PWBS SHALL PASS 100% ELECTRICAL TEST USING SUPPLIED IPC-356 NETLIST IN ACCORDANCE WITH CURRENT REVISION OF IPC-9252, CLASS 2.
- B. CERTIFICATE OF CONFORMANCE SHALL BE SUPPLIED WITH EACH SHIPMENT.

### 12. X-OUTS:

- A. X-OUT BOARDS THAT DO NOT MEET ALL SPECIFICATIONS USING PERMANENT MARKING ON BOTH SIDES OF THE AFFECTED PCB.
- B. PANELS THAT DO NOT HAVE ANY X-OUTS SHALL BE PACKAGED TOGETHER.
- C. PANELS THAT HAVE n OR FEWER X-OUTS SHALL BE PACKAGED SEPARATE FROM NON-X-OUT PANELS.
- D. PANELS WITH MORE THAN *n* X-OUTS SHALL BE REJECTED.
- 13. PACKAGING REQUIREMENTS:
- A. PWBS SHALL BE PACKAGED IN VACUUM SEALED INNER CONTAINERS.
- B. OUTER CONTAINERS SHALL BE SUFFICIENT TO PREVENT DAMAGE DURING SHIPPING AND HANDLING.
- 14. IMPEDANCE (ALL TOLERANCES +/- 10%)
- A. ALL 0.nn MM WIDE TRACES ON OUTER LAYERS SHALL BE 50 OHMS.
- B. ALL 0.nn MM WIDE/0.nn MM SPACE PAIRS ON OUTER LAYERS SHALL BE 90 OHMS.
- C. ALL 0.nn MM WIDE/0.nn MM SPACE PAIRS ON INNER LAYERS SHALL BE 90 OHMS.
- D. VENDOR MAY ADJUST DESIGN GEOMETRIES UP TO +/-20% TO
- Hardware E Pcb C Pcb Design I Design Process J Fabrication S BEYOND 20% OF LINE WIDTH, SPACING OR DIELECTRIC THICKNESS SHALL REQUIRE

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