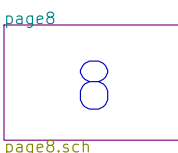
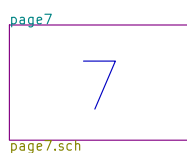
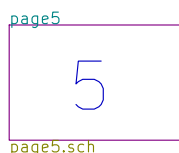
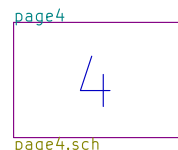
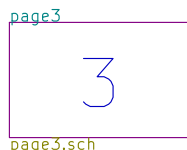
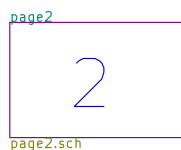
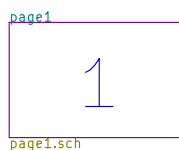


68000 Single Board Computer

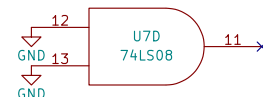
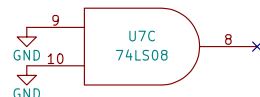
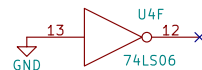
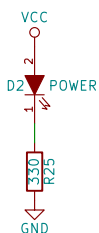
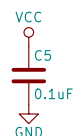
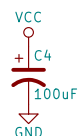
from

"Microprocessor Systems Design" by Alan Clements

Modified by Jeff Tranter



Bypass caps,
one per IC



Spare Gates

Top Level Schematic

Jeff Tranter

Sheet: /

File: ts2.sch

Title: TS2 68000 Single Board Computer

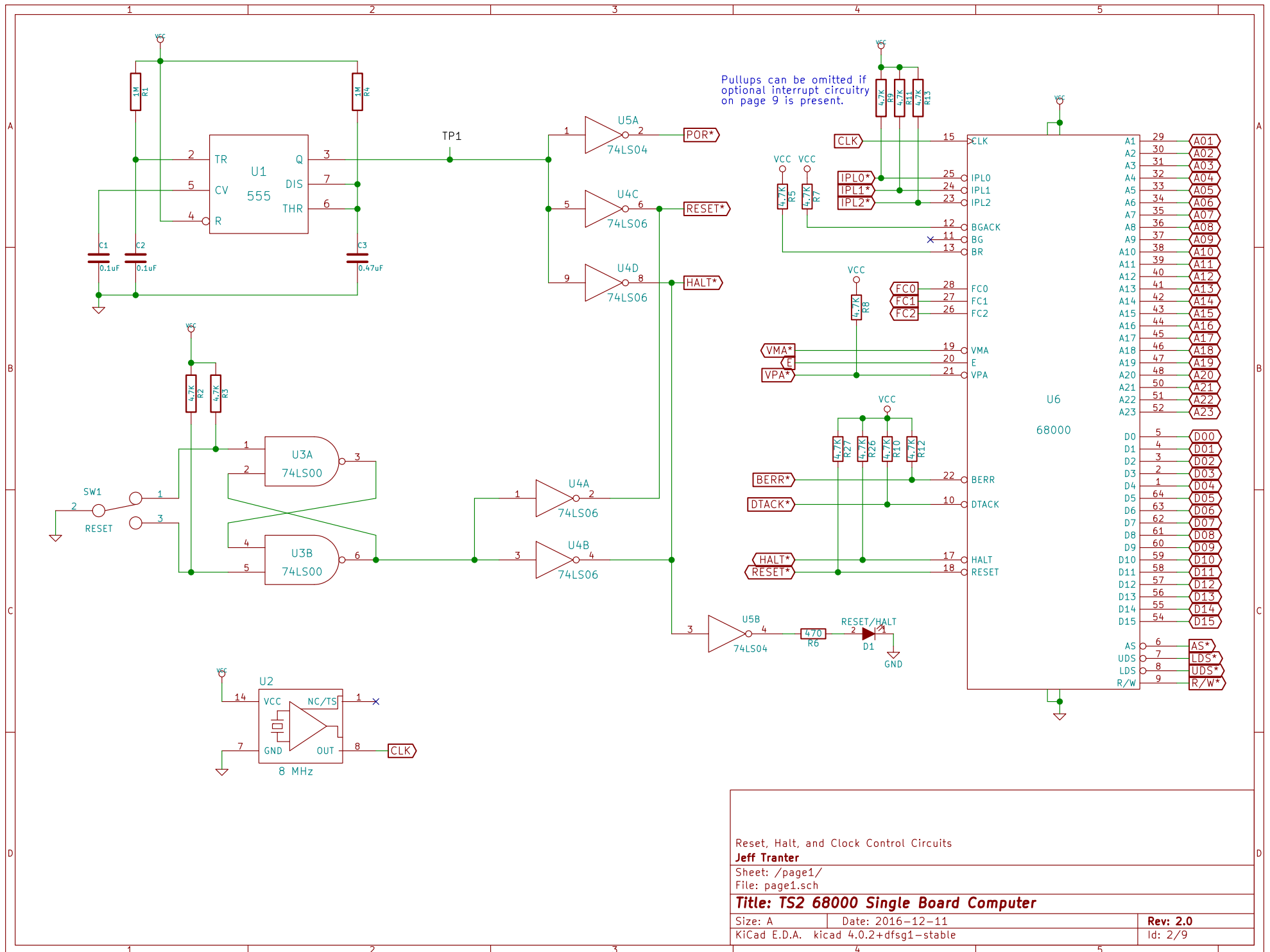
Size: A

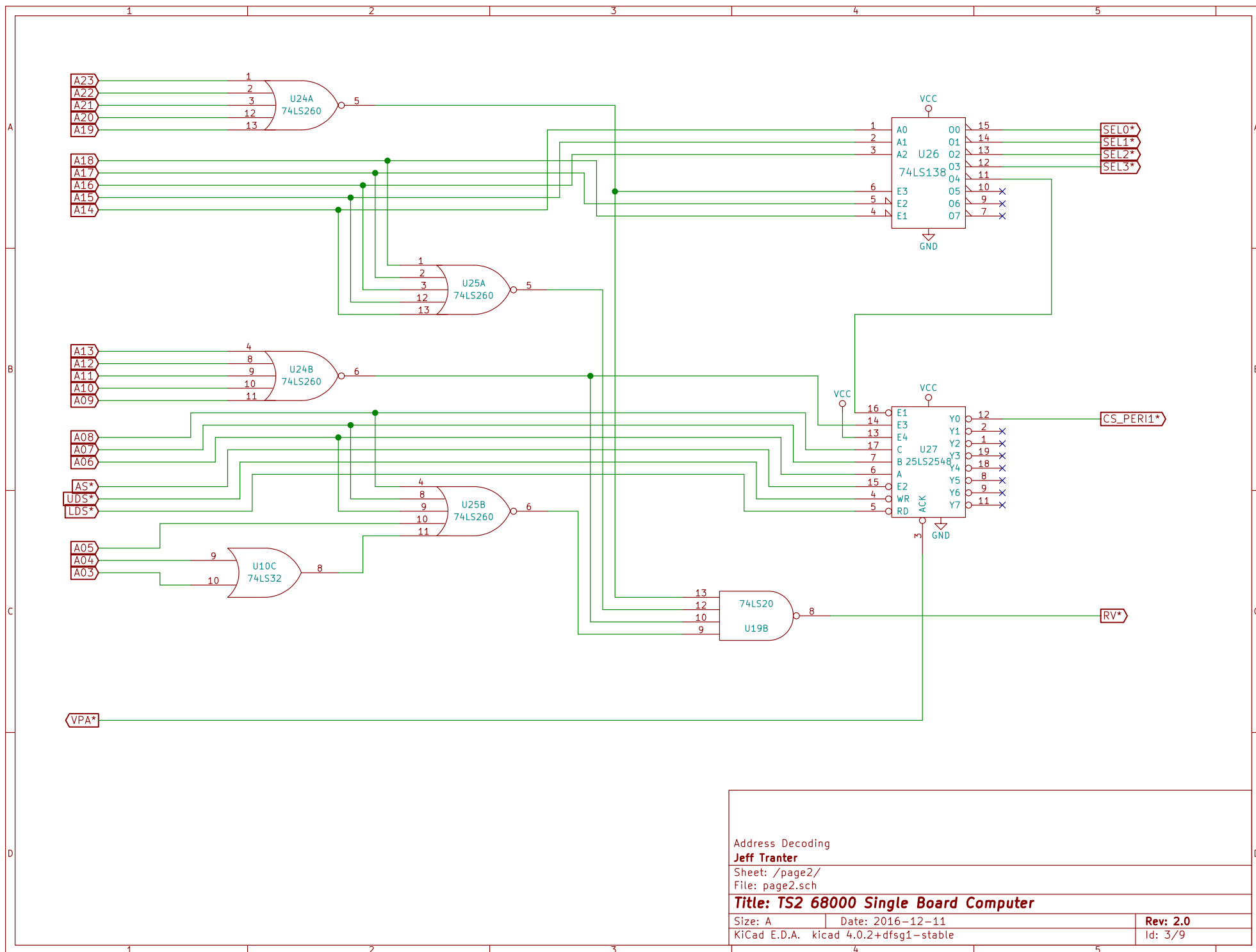
Date: 2016-12-11

Rev: 2.0

KiCad E.D.A. kicad 4.0.2+dfsg1-stable

Id: 1/9





Address Decoding

Jeff Tranter

Sheet: /page2/

File: page2.sch

Title: TS2 68000 Single Board Computer

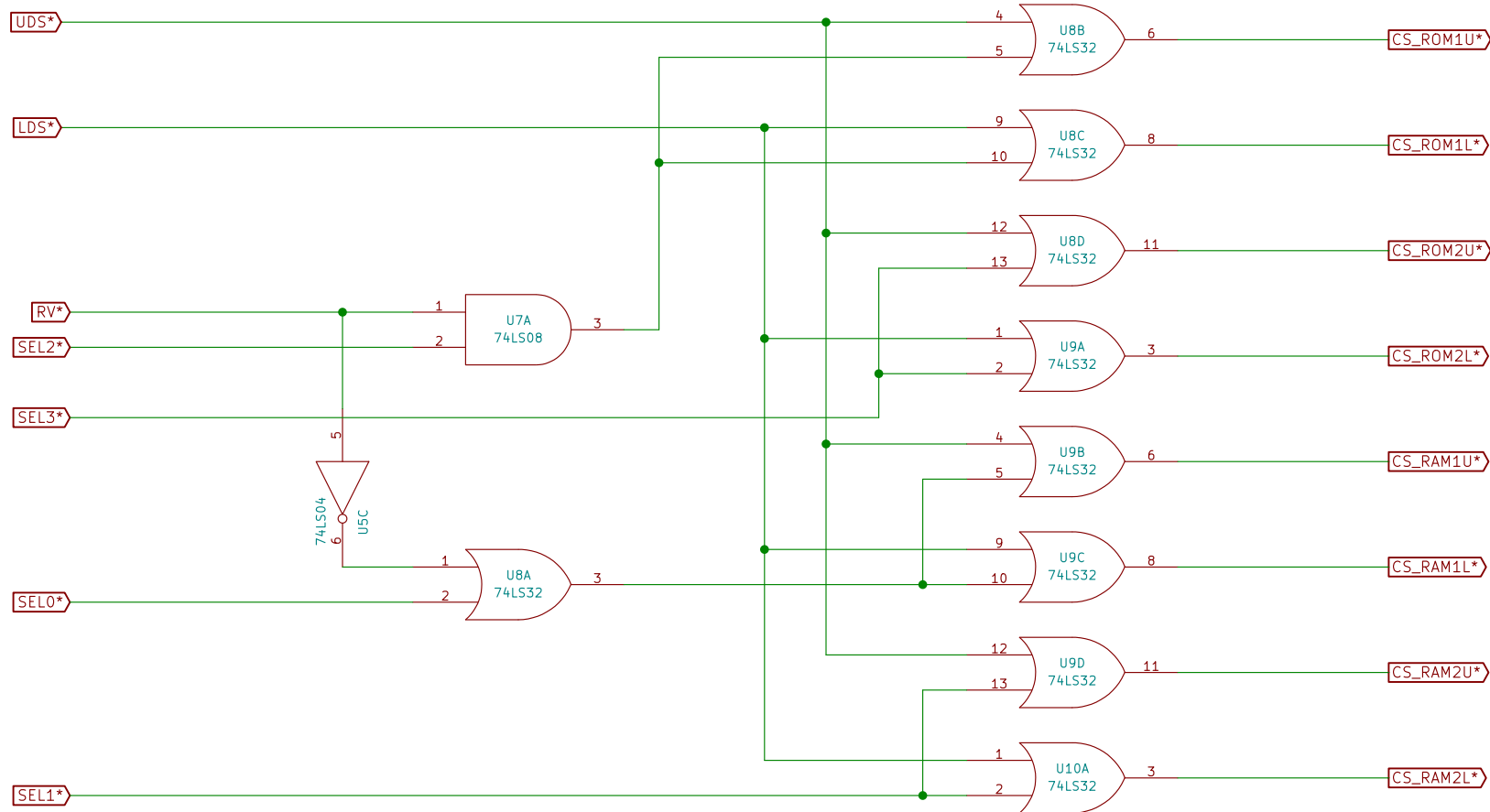
Size: A

Date: 2016-12-11

Rev: 2.0

KiCad E.D.A. kicad 4.0.2+dfsg1-stable

Id: 3/9



RAM and ROM Address Select

Jeff Tranter

Sheet: /page3/

File: page3.sch

Title: TS2 68000 Single Board Computer

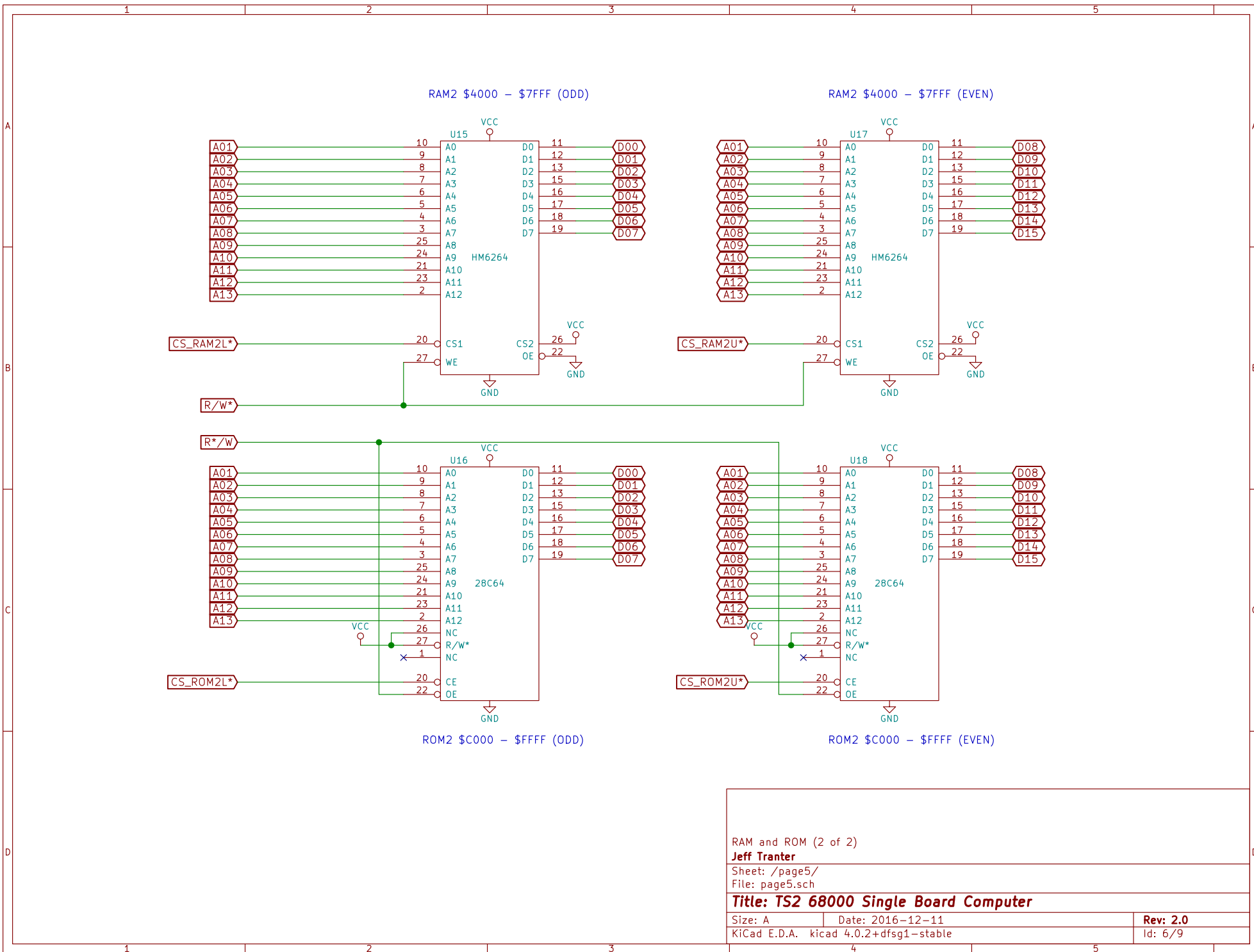
Size: A

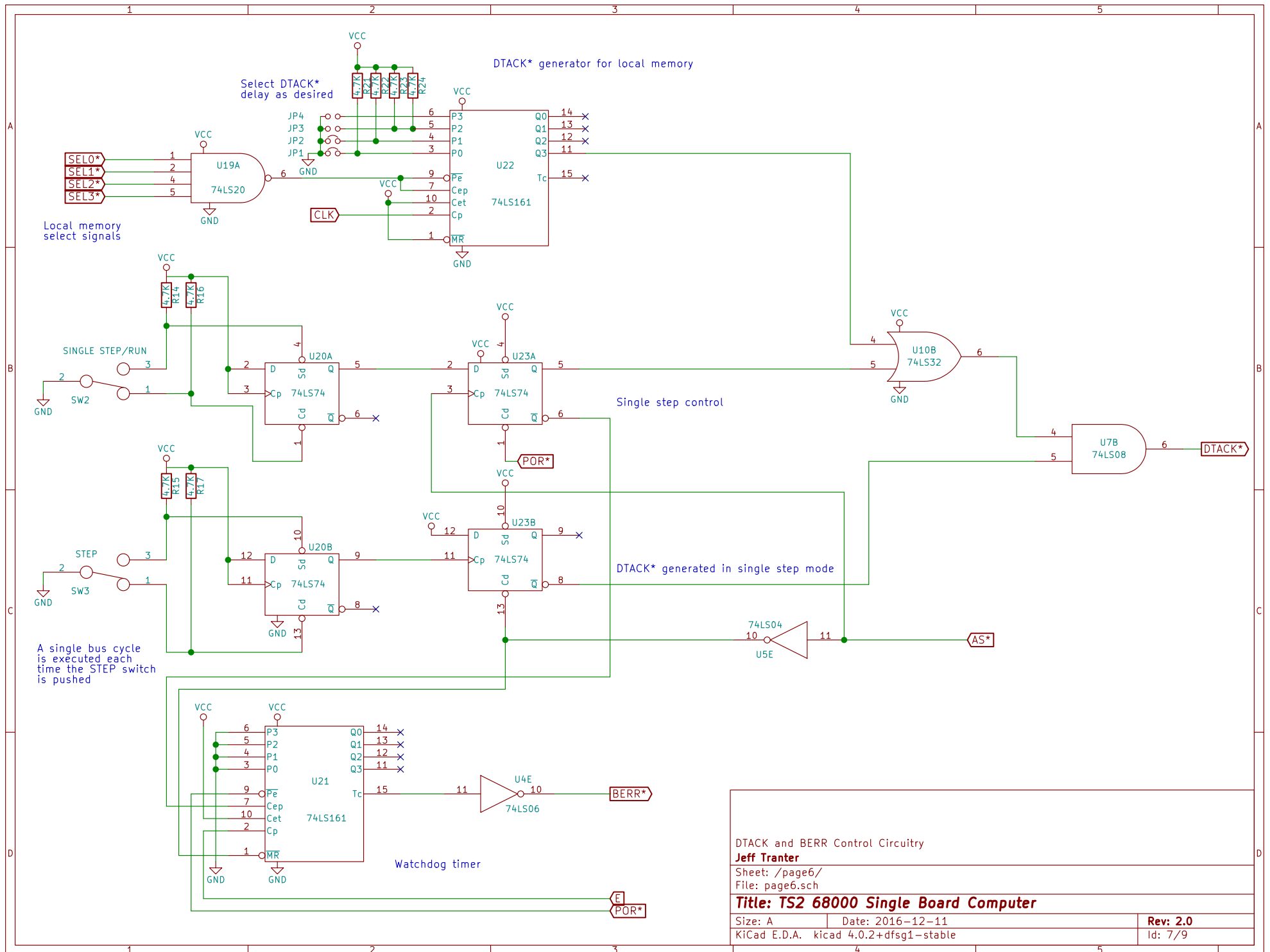
Date: 2016-12-11

Rev: 2.0

KiCad E.D.A. kicad 4.0.2+dfsg1-stable

Id: 4/9





DTACK and BERR Control Circuitry

Jeff Tranter

Sheet: /page6/

File: page6.sch

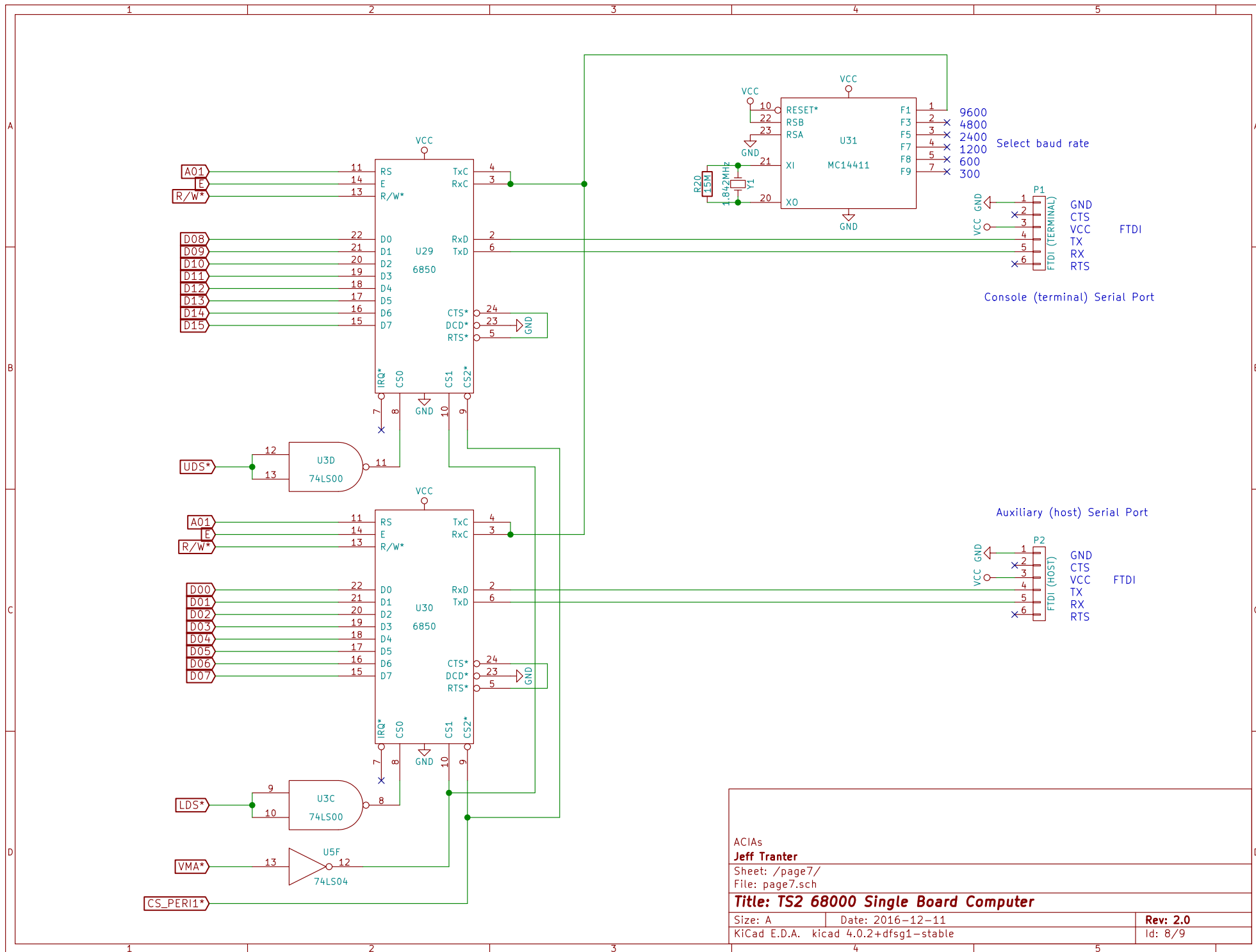
Title: TS2 68000 Single Board Computer

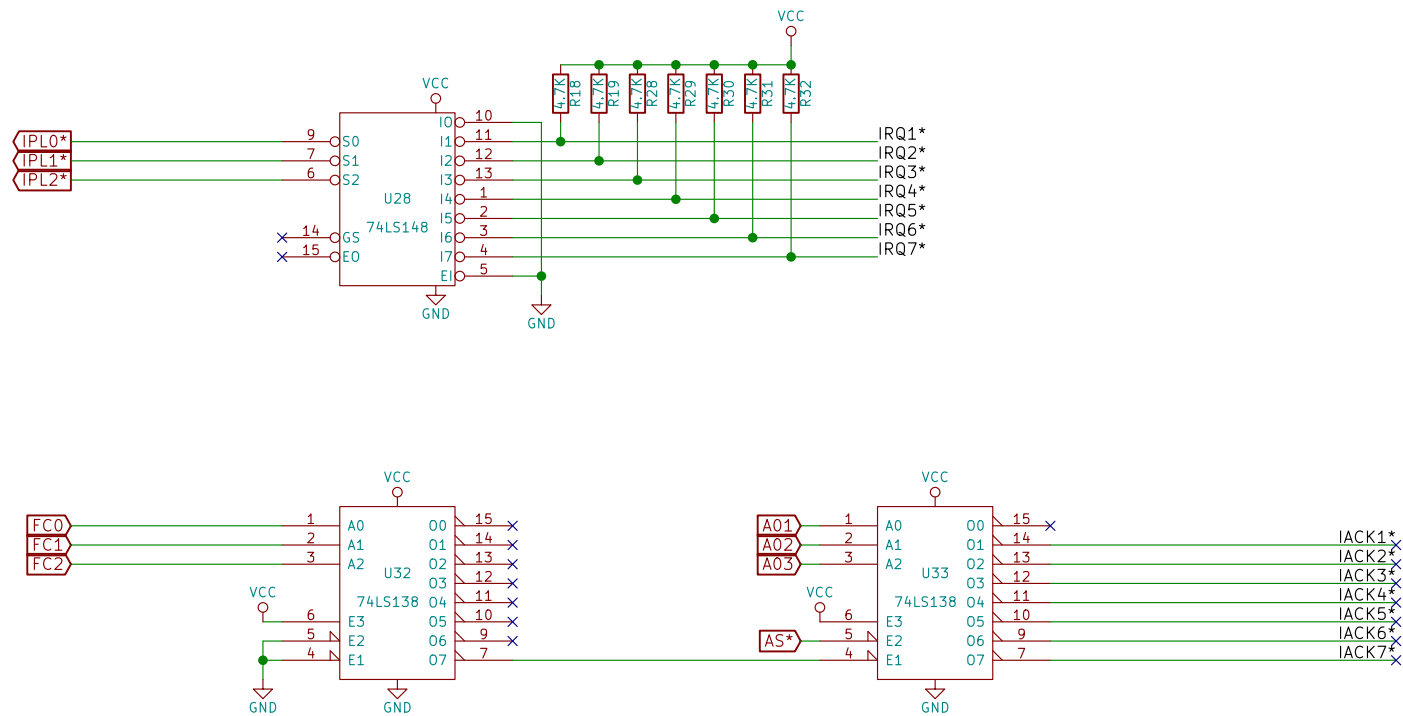
Size: A Date: 2016-12-11

KiCad E.D.A. kicad 4.0.2+dfsg1-stable

Rev: 2.0

Id: 7/9





Interrupt Control Circuitry (optional)

Jeff Tranter

Sheet: /page8/

File: page8.sch

Title: TS2 68000 Single Board Computer

Size: A4

Date: 2016-12-11

Rev: 2.0

KiCad E.D.A. kicad 4.0.2+dfsg1-stable

Id: 9/9