68000 Single Board Computer
from
"Microprocessor Systems Design" by Alan Clements
Modified by Jeff Tranter

page1
1
page1.sch

page2
2
page2.sch

page3
3
page3.sch

page4
4
page4.sch

page5
5
page5.sch

page6
6
page6.sch

page7
7
page7.sch
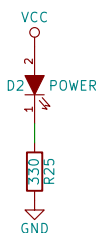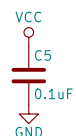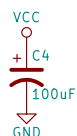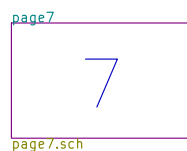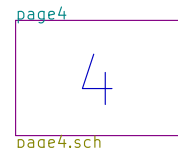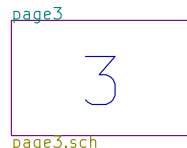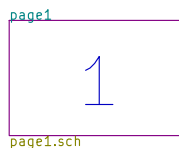
Bypass caps,
one per IC

Spare Gates

VCC
PWR_FLAG

VCC
+ C4
100uF
GND

VCC
C5
0.1uF
GND

VCC
D2 POWER
330 R25
GND

PWR_FLAG
GND

13 U4F 12
74LS06
GND

12 U10D 11
GND 13 74LS32
GND

9 U7C 8
GND 10 74LS08
GND

12 U7D 11
GND 13 74LS08
GND
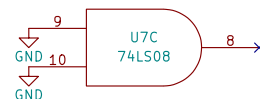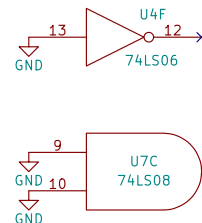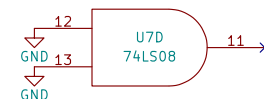
Top Level Schematic
Jeff Tranter
Sheet: /
File: ts2.sch
Title: TS2 68000 Single Board Computer
Size: A | Date: 2016−12−04 | **Rev: 2.0**
KiCad E.D.A. kicad 4.0.2+dfsg1−stable | Id: 1/8

Reset, Halt, and Clock Control Circuits

Jeff Tranter

Sheet: /page1/
File: page1.sch

Title: TS2 68000 Single Board Computer

Size: A	Date: 2016-12-04	**Rev: 2.0**
KiCad E.D.A. kicad 4.0.2+dfsg1-stable		Id: 2/8

A23
A22
A21
A20
A19

U24A
74LS260

A18
A17
A16
A15
A14

U25A
74LS260

U26
74LS138

SEL0*
SEL1*
SEL2*
SEL3*

A13
A12
A11
A10
A09

U24B
74LS260

A08
A07
A06

AS*
UDS*
LDS*

U25B
74LS260

U27
25LS2548

CS_PERI1*

A05
A04
A03

U10C
74LS32

74LS20
U19B

RV*

VPA*

UDS*

LDS*

RV*

SEL2*

SEL3*

SEL0*

SEL1*

U8B
74LS32
4
5
6
CS_ROM1U*

U8C
74LS32
9
10
8
CS_ROM1L*

U8D
74LS32
12
13
11
CS_ROM2U*

U7A
74LS08
1
2
3

U9A
74LS32
1
2
3
CS_ROM2L*

U9B
74LS32
4
5
6
CS_RAM1U*

74LS04
U5C
5
6

U8A
74LS32
1
2
3

U9C
74LS32
9
10
8
CS_RAM1L*

U9D
74LS32
12
13
11
CS_RAM2U*

U10A
74LS32
1
2
3
CS_RAM2L*
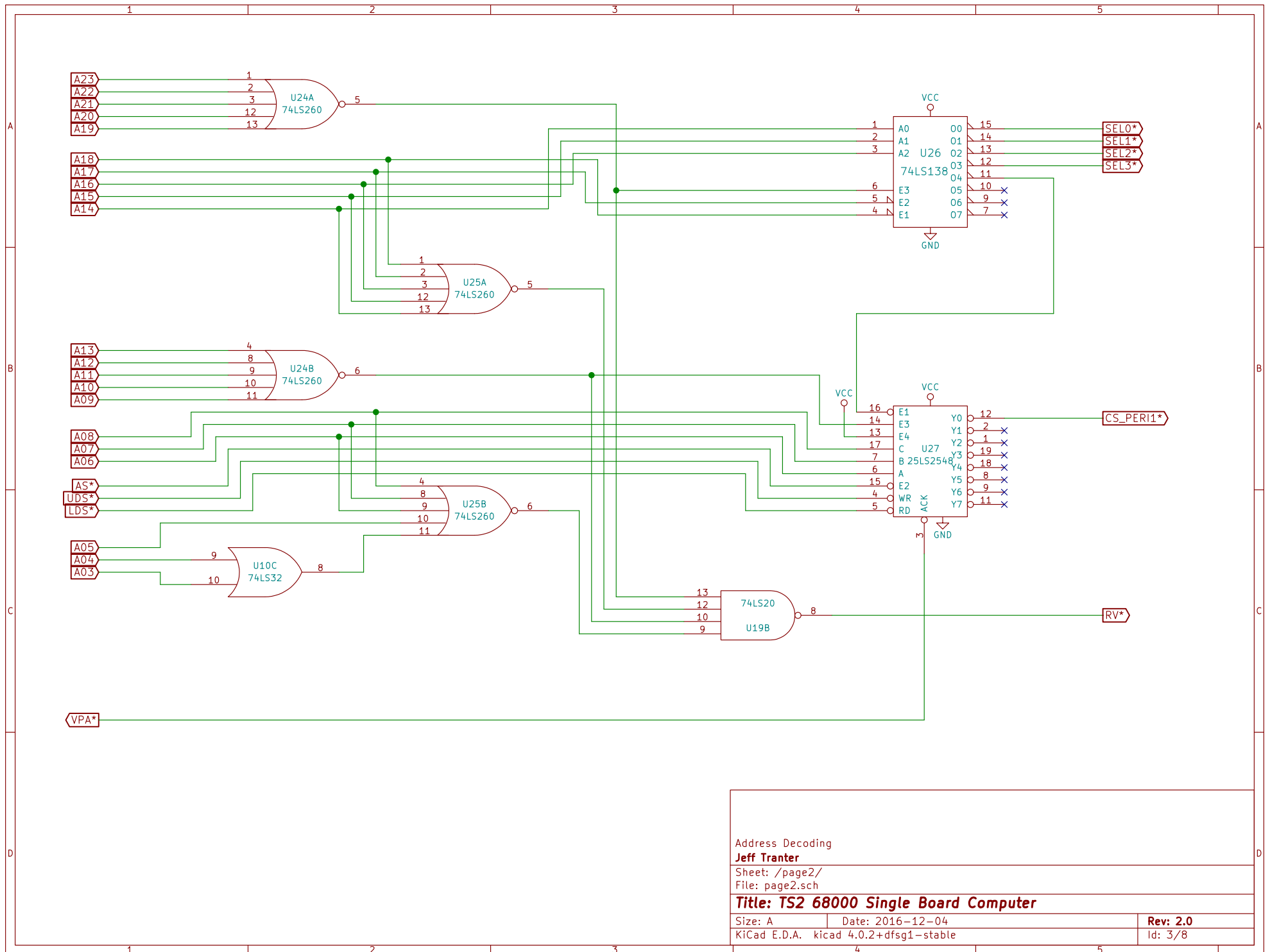
RAM and ROM Address Select
Jeff Tranter
Sheet: /page3/
File: page3.sch
Title: **TS2 68000 Single Board Computer**
Size: A
Date: 2016-12-04
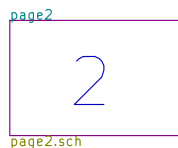**Rev: 2.0**
KiCad E.D.A.   kicad 4.0.2+dfsg1-stable
Id: 4/8

RAM1 $0008 – $3FFF (ODD)

RAM1 $0008 – $3FFF (EVEN)

VCC

U11

HM6264

A01	10	A0	D0	11	D00
A02	9	A1	D1	12	D01
A03	8	A2	D2	13	D02
A04	7	A3	D3	15	D03
A05	6	A4	D4	16	D04
A06	5	A5	D5	17	D05
A07	4	A6	D6	18	D06
A08	3	A7	D7	19	D07
A09	25	A8			
A10	24	A9			
A11	21	A10			
A12	23	A11			
A13	2	A12			

CS_RAM1L* 20 CS1   CS2 26 VCC

27 WE   OE 22 GND

GND

VCC

U13

HM6264

A01	10	A0	D0	11	D08
A02	9	A1	D1	12	D09
A03	8	A2	D2	13	D10
A04	7	A3	D3	15	D11
A05	6	A4	D4	16	D12
A06	5	A5	D5	17	D13
A07	4	A6	D6	18	D14
A08	3	A7	D7	19	D15
A09	25	A8			
A10	24	A9			
A11	21	A10			
A12	23	A11			
A13	2	A12			

CS_RAM1U* 20 CS1   CS2 26 VCC

27 WE   OE 22 GND

GND

R/W*

R*/W   U5D
9 ▷ 8
74LS04

VCC

U12

28C64

A01	10	A0	D0	11	D00
A02	9	A1	D1	12	D01
A03	8	A2	D2	13	D02
A04	7	A3	D3	15	D03
A05	6	A4	D4	16	D04
A06	5	A5	D5	17	D05
A07	4	A6	D6	18	D06
A08	3	A7	D7	19	D07
A09	25	A8			
A10	24	A9			
A11	21	A10			
A12	23	A11			
A13	2	A12			

VCC 26 NC
27 R/W*
1 NC

CS_ROM1L* 20 CE
22 OE

GND

VCC

U14

28C64

A01	10	A0	D0	11	D08
A02	9	A1	D1	12	D09
A03	8	A2	D2	13	D10
A04	7	A3	D3	15	D11
A05	6	A4	D4	16	D12
A06	5	A5	D5	17	D13
A07	4	A6	D6	18	D14
A08	3	A7	D7	19	D15
A09	25	A8			
A10	24	A9			
A11	21	A10			
A12	23	A11			
A13	2	A12			

VCC 26 NC
27 R/W*
1 NC

CS_ROM1U* 20 CE
22 OE

GND

ROM1 $8000 – $BFFF (ODD)

ROM1 $8000 – $BFFF (EVEN)

RAM and ROM (1 of 2)
Jeff Tranter
Sheet: /page4/
File: page4.sch
Title: TS2 68000 Single Board Computer
Size: A   Date: 2016-12-04   **Rev: 2.0**
KiCad E.D.A. kicad 4.0.2+dfsg1-stable   Id: 5/8

RAM2 $4000 — $7FFF (ODD)

U15
HM6264

Pin	Signal		Signal	Pin
10	A0	D0	11	
9	A1	D1	12	
8	A2	D2	13	
7	A3	D3	15	
6	A4	D4	16	
5	A5	D5	17	
4	A6	D6	18	
3	A7	D7	19	
25	A8			
24	A9			
21	A10			
23	A11			
2	A12			

A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13

D00 D01 D02 D03 D04 D05 D06 D07

VCC

CS_RAM2L* — 20 CS1   CS2 26 VCC
27 WE   OE 22 GND
GND

R/W*

RAM2 $4000 — $7FFF (EVEN)

U17
HM6264

Pin	Signal		Signal	Pin
10	A0	D0	11	
9	A1	D1	12	
8	A2	D2	13	
7	A3	D3	15	
6	A4	D4	16	
5	A5	D5	17	
4	A6	D6	18	
3	A7	D7	19	
25	A8			
24	A9			
21	A10			
23	A11			
2	A12			

A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13

D08 D09 D10 D11 D12 D13 D14 D15

VCC

CS_RAM2U* — 20 CS1   CS2 26 VCC
27 WE   OE 22 GND
GND

R*/W

U16
28C64

Pin	Signal		Signal	Pin
10	A0	D0	11	
9	A1	D1	12	
8	A2	D2	13	
7	A3	D3	15	
6	A4	D4	16	
5	A5	D5	17	
4	A6	D6	18	
3	A7	D7	19	
25	A8			
24	A9			
21	A10			
23	A11			
2	A12			

A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13

D00 D01 D02 D03 D04 D05 D06 D07

VCC

26 NC
VCC 27 R/W*
1 NC
CS_ROM2L* — 20 CE
22 OE
GND

ROM2 $C000 — $FFFF (ODD)

U18
28C64

Pin	Signal		Signal	Pin
10	A0	D0	11	
9	A1	D1	12	
8	A2	D2	13	
7	A3	D3	15	
6	A4	D4	16	
5	A5	D5	17	
4	A6	D6	18	
3	A7	D7	19	
25	A8			
24	A9			
21	A10			
23	A11			
2	A12			

A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13

D08 D09 D10 D11 D12 D13 D14 D15

VCC

26 NC
VCC 27 R/W*
1 NC
CS_ROM2U* — 20 CE
22 OE
GND

ROM2 $C000 — $FFFF (EVEN)

RAM and ROM (2 of 2)
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Sheet: /page5/
File: page5.sch
Title: TS2 68000 Single Board Computer
Size: A   Date: 2016-12-04   **Rev: 2.0**
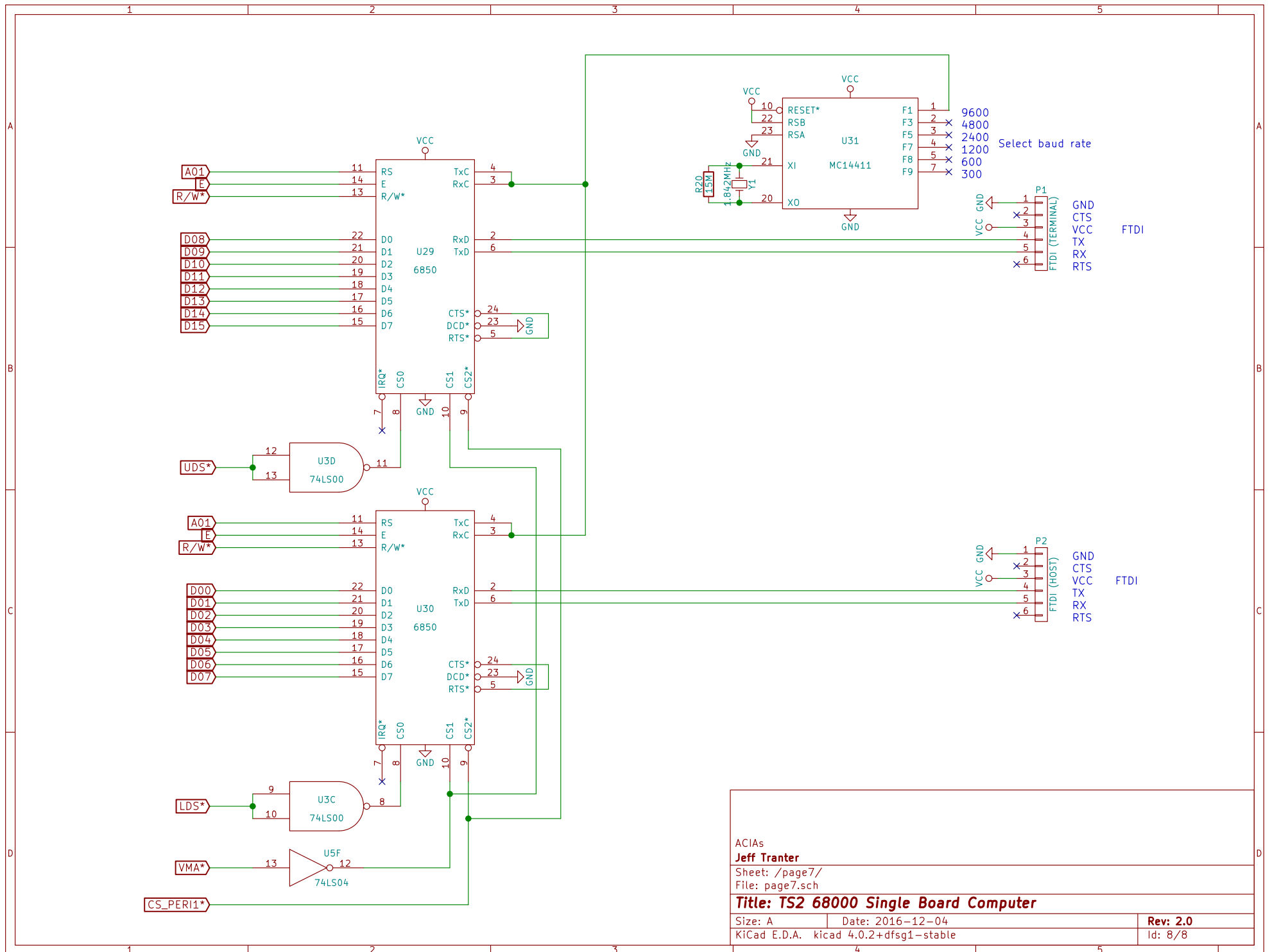KiCad E.D.A. kicad 4.0.2+dfsg1-stable   Id: 6/8

DTACK* generator for local memory

Select DTACK*
delay as desired

VCC

470Ω R23 470Ω R22 220Ω R25 2.2K R24

JP4
JP3
JP2
JP1

GND

VCC

P3 6
P2 5
P1 4
P0 3

Pe 9
Cep 7
Cet 10
Cp 2

U22
74LS161

Q0 14
Q1 13
Q2 12
Q3 11

Tc 15

MR 1

GND

CLK

VCC

SEL0* 1
SEL1* 2
SEL2* 4
SEL3* 5

U19A
74LS20

GND

6

Local memory
select signals

VCC

R14 4.7K R16 4.7K

SINGLE STEP/RUN

SW2
GND
2
1
3

U20A
74LS74

D 2
Cp 3
Sd 4
Cd 1
Q 5
Q̄ 6

VCC

U23A
74LS74

D 2
Cp 3
Sd 4
Cd 1
Q 5
Q̄ 6

Single step control

POR*

VCC

U10B
74LS32

5
4
6

GND

VCC

U7B
74LS08

4
5
6

DTACK*

VCC

R15 4.7K R17 4.7K

STEP

SW3
GND
2
1
3

U20B
74LS74

D 12
Cp 11
Sd 10
Cd 13
Q 9
Q̄ 8

GND

VCC

U23B
74LS74

D 12
Cp 11
Sd 10
Cd 13
Q 9
Q̄ 8

DTACK* generated in single step mode

74LS04
U5E
10 11

AS*

A single bus cycle
is executed each
time the STEP switch
is pushed

VCC   VCC

P3 6
P2 5
P1 4
P0 3

Pe 9
Cep 7
Cet 10
Cp 2

U21
74LS161

Q0 14
Q1 13
Q2 12
Q3 11

Tc 15

MR 1

GND   GND

Watchdog timer

U4E
74LS06
11 10

BERR*

E
POR*

DTACK and BERR Control Circuitry
Jeff Tranter
Sheet: /page6/
File: page6.sch

Title: TS2 68000 Single Board Computer

Size: A   Date: 2016-12-04   Rev: 2.0
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Select baud rate

1 — 9600
2 — 4800
3 — 2400
4 — 1200
5 — 600
7 — 300

U31
MC14411

U29
6850

U30
6850

U3D
74LS00

U3C
74LS00

U5F
74LS04

FTDI

P1
FTDI (TERMINAL)
1 GND
2 CTS
3 VCC
4 TX
5 RX
6 RTS

P2
FTDI (HOST)
1 GND
2 CTS
3 VCC
4 TX
5 RX
6 RTS

ACIAs
Jeff Tranter
Sheet: /page7/
File: page7.sch

Title: TS2 68000 Single Board Computer

Size: A | Date: 2016-12-04 | **Rev: 2.0**
KiCad E.D.A. kicad 4.0.2+dfsg1-stable | Id: 8/8