68000 Single Board Computer
from
"Microprocessor Systems Design" by Alan Clements
Modified by Jeff Tranter
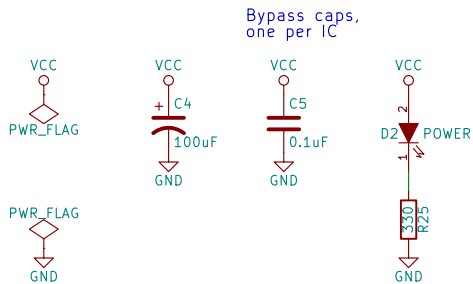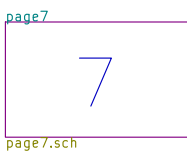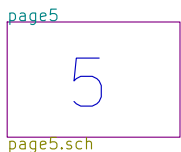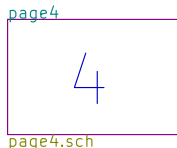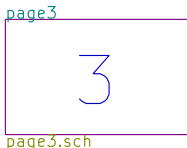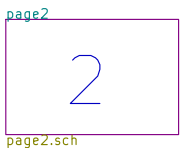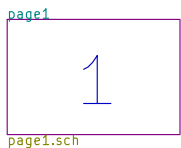
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Bypass caps,
one per IC

VCC
PWR_FLAG

VCC
+ C4
100uF
GND

VCC
C5
0.1uF
GND

VCC
D2 POWER
2
1
330 R25
GND

PWR_FLAG
GND
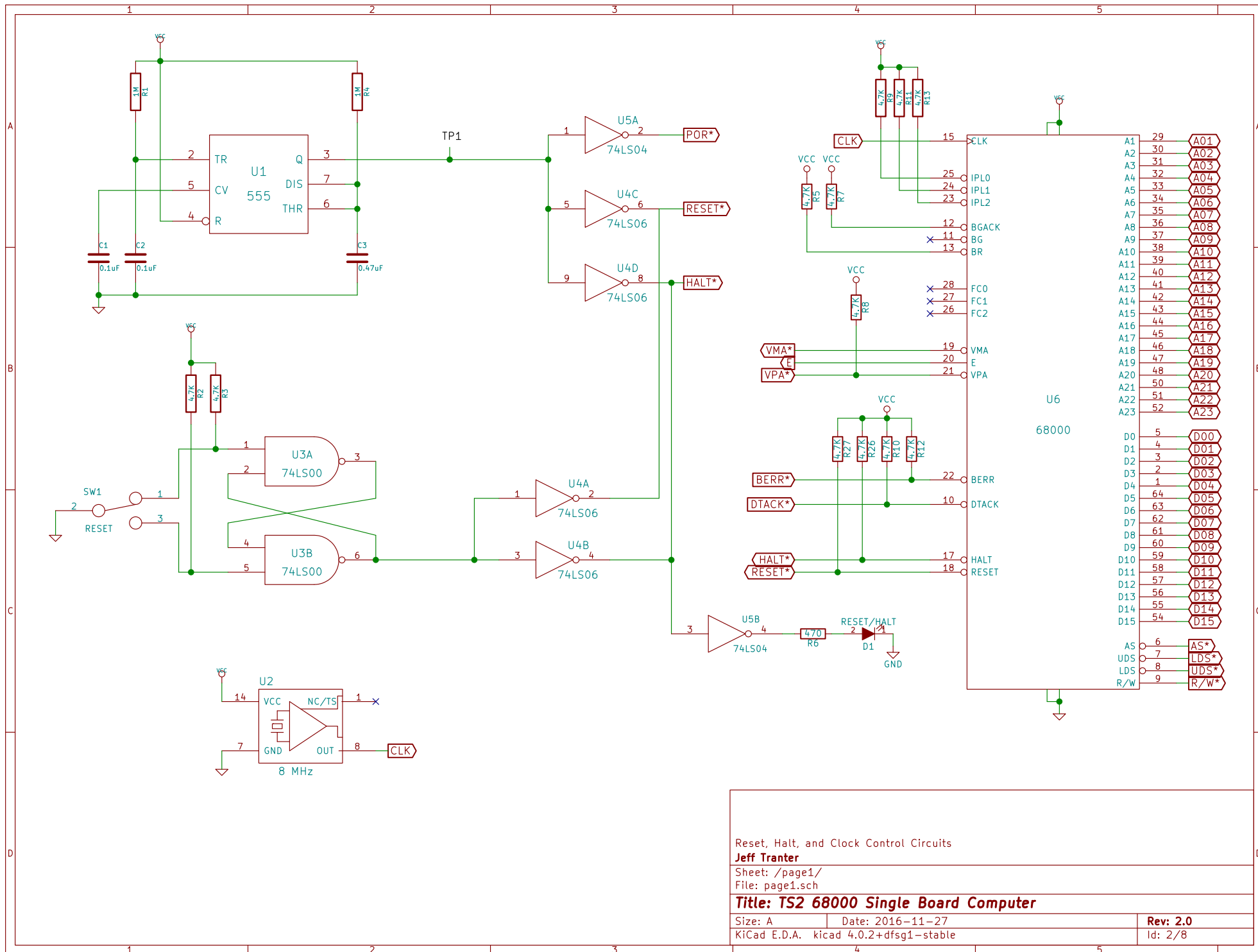
Reset, Halt, and Clock Control Circuits

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Title: TS2 68000 Single Board Computer

| Size: A | Date: 2016-11-27 | Rev: 2.0 |
| KiCad E.D.A. kicad 4.0.2+dfsg1-stable | | Id: 2/8 |

Schematic labels and text

U24A 74LS260
U25A 74LS260
U24B 74LS260
U25B 74LS260
U10C 74LS32
U19B 74LS20
U26 74LS138
U27 25LS2548

A23, A22, A21, A20, A19
A18, A17, A16, A15, A14
A13, A12, A11, A10, A09
A08, A07, A06
A05, A04, A03
AS*, UDS*, LDS*
VPA*

SEL0*, SEL1*, SEL2*, SEL3*
CS_PERI1*
RV*

VCC, GND

U26 pins: A0, A1, A2, E3, E2, E1, O0, O1, O2, O3, O4, O5, O6, O7

U27 pins: E1, E3, E4, C, B, A, E2, WR, RD, ACK, Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7
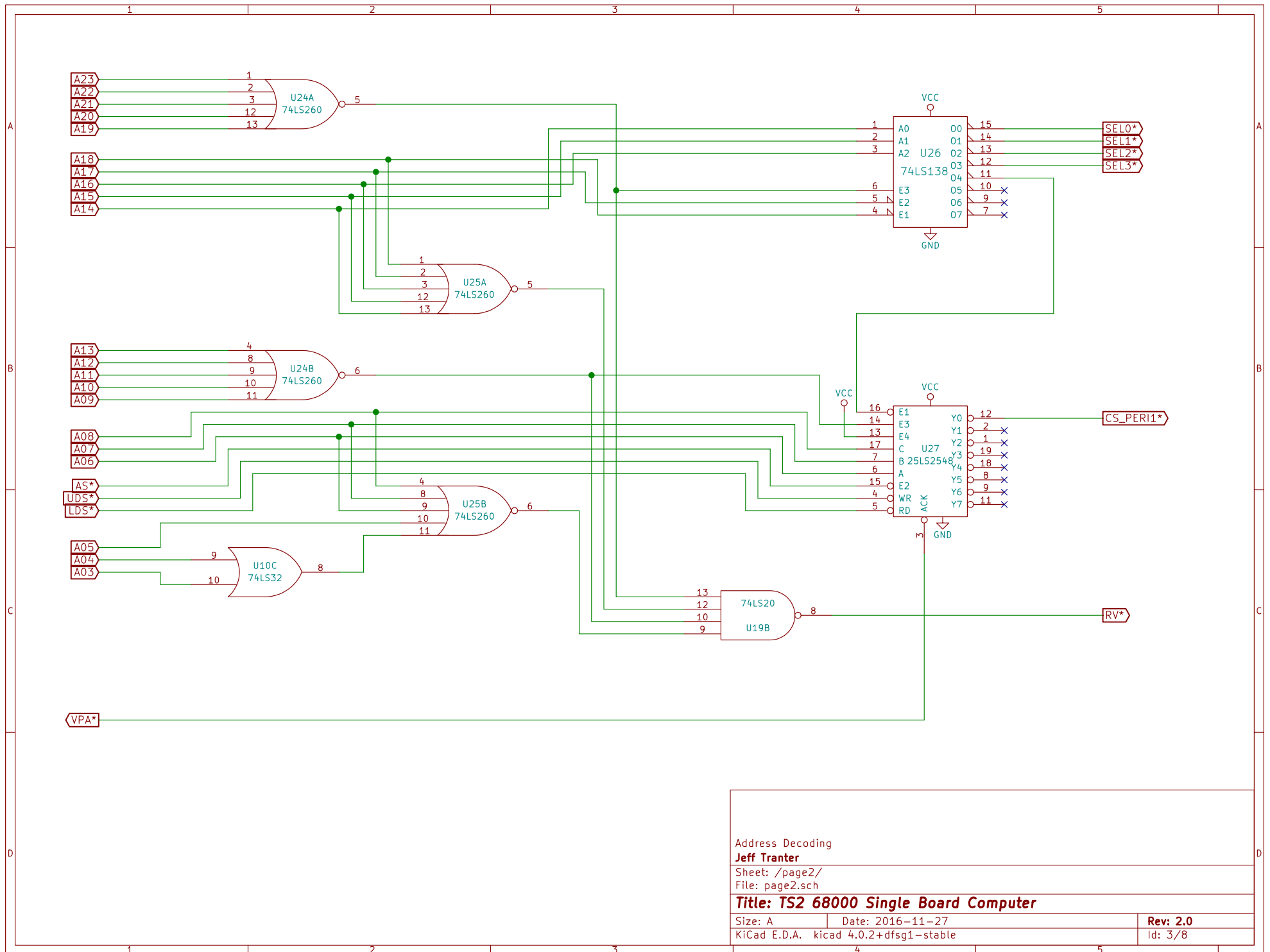
Address Decoding
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Sheet: /page2/
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Title: TS2 68000 Single Board Computer
Size: A | Date: 2016-11-27 | **Rev: 2.0**
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UDS*

LDS*

RV*

SEL2*

SEL3*

SEL0*

SEL1*

U7A
74LS08
1
2
3

U5C
74LS04
5
6

U8A
74LS32
1
2
3

U8B
74LS32
4
5
6

U8C
74LS32
9
10
8

U8D
74LS32
12
13
11

U9A
74LS32
1
2
3

U9B
74LS32
4
5
6

U9C
74LS32
9
10
8

U9D
74LS32
12
13
11

U10A
74LS32
1
2
3

CS_ROM1U*

CS_ROM1L*

CS_ROM2U*

CS_ROM2L*

CS_RAM1U*

CS_RAM1L*

CS_RAM2U*

CS_RAM2L*
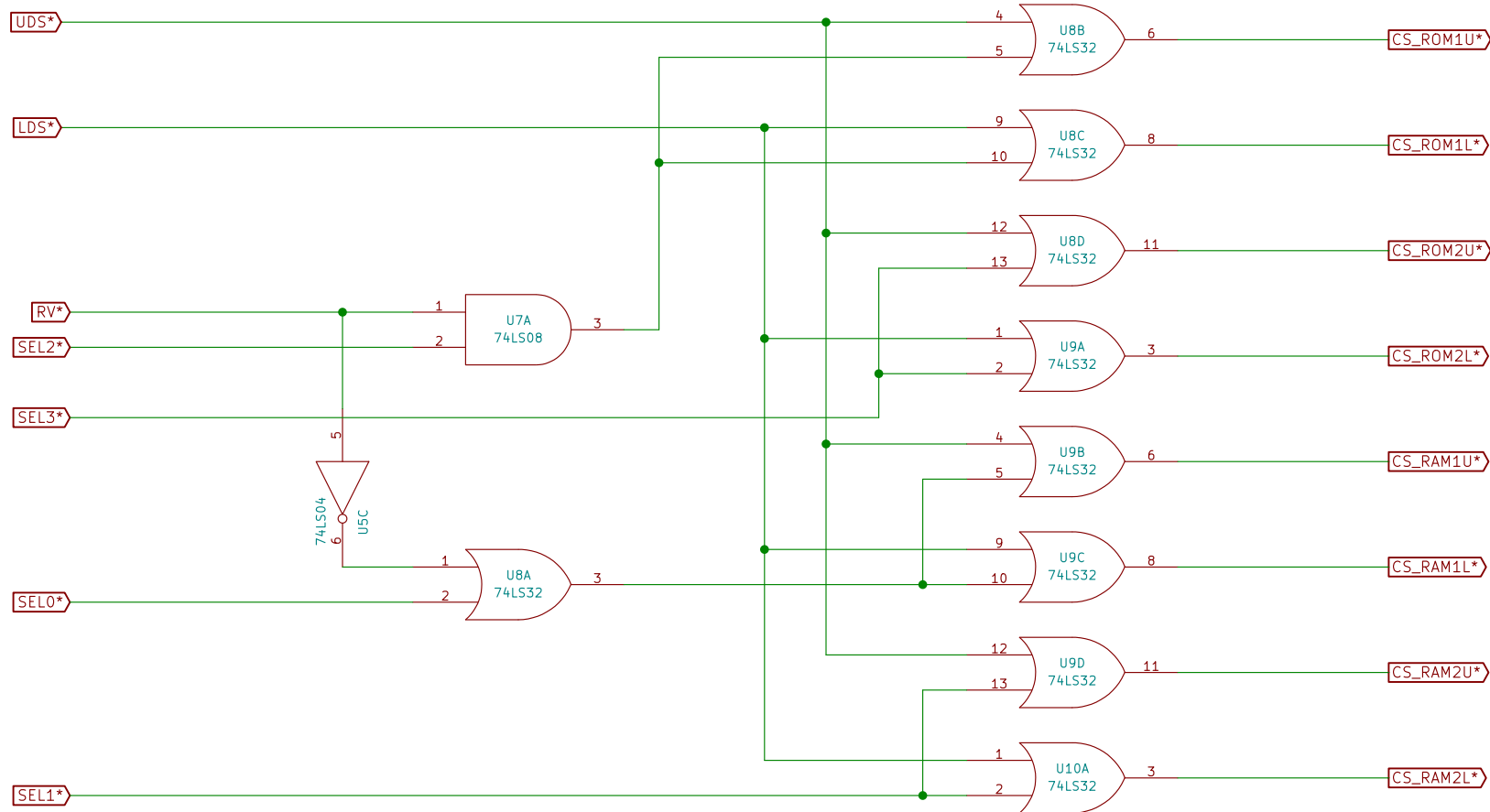
RAM and ROM Address Select

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Title: TS2 68000 Single Board Computer

Size: A | Date: 2016-11-27 | **Rev: 2.0**
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RAM1 $0008 — $3FFF (ODD)

U11 — HM6264

Pin	Signal		Pin	Signal
10	A0		11	D00
9	A1		12	D01
8	A2		13	D02
7	A3		15	D03
6	A4		16	D04
5	A5		17	D05
4	A6		18	D06
3	A7		19	D07
25	A8			
24	A9			
21	A10			
23	A11			
2	A12			

A01–A13 (address inputs)

CS_RAM1L* — 20 CS1
27 WE
CS2 26 VCC
OE 22 GND
GND

RAM1 $0008 — $3FFF (EVEN)

U13 — HM6264

Pin	Signal		Pin	Signal
10	A0		11	D08
9	A1		12	D09
8	A2		13	D10
7	A3		15	D11
6	A4		16	D12
5	A5		17	D13
4	A6		18	D14
3	A7		19	D15
25	A8			
24	A9			
21	A10			
23	A11			
2	A12			

CS_RAM1U* — 20 CS1
27 WE
CS2 26 VCC
OE 22 GND
GND

R/W*

R*/W — U5D 74LS04 (9, 8)

ROM1 $8000 — $BFFF (ODD)

U12 — 28C64

Pin	Signal		Pin	Signal
10	A0		11	D00
9	A1		12	D01
8	A2		13	D02
7	A3		15	D03
6	A4		16	D04
5	A5		17	D05
4	A6		18	D06
3	A7		19	D07
25	A8			
24	A9			
21	A10			
23	A11			
2	A12			

26 NC
VCC 27 R/W*
1 NC
CS_ROM1L* — 20 CE
22 OE
GND

ROM1 $8000 — $BFFF (EVEN)

U14 — 28C64

Pin	Signal		Pin	Signal
10	A0		11	D08
9	A1		12	D09
8	A2		13	D10
7	A3		15	D11
6	A4		16	D12
5	A5		17	D13
4	A6		18	D14
3	A7		19	D15
25	A8			
24	A9			
21	A10			
23	A11			
2	A12			

26 NC
VCC 27 R/W*
1 NC
CS_ROM1U* — 20 CE
22 OE
GND

RAM and ROM (1 of 2)
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Title: TS2 68000 Single Board Computer
Size: A | Date: 2016—11—27 | **Rev: 2.0**
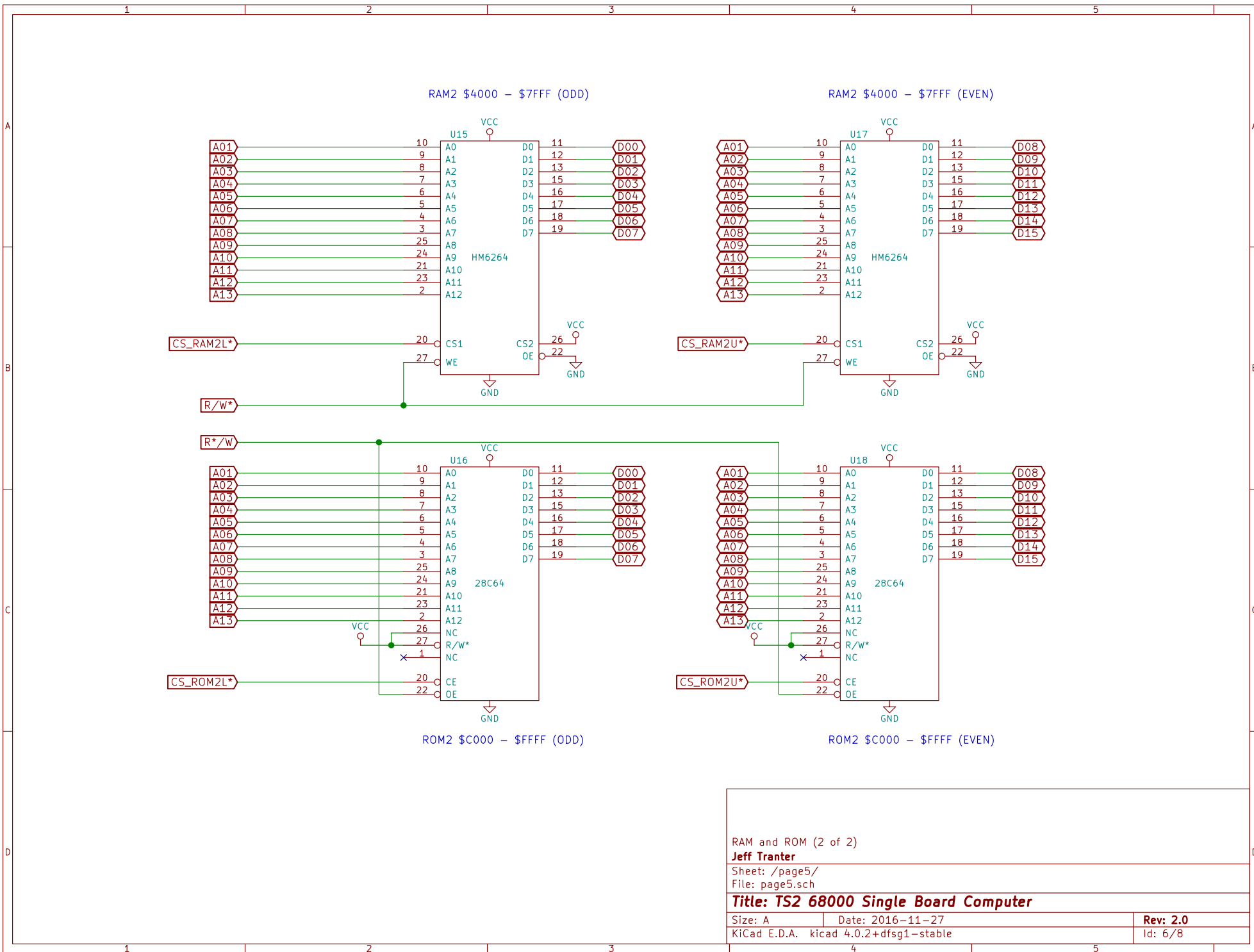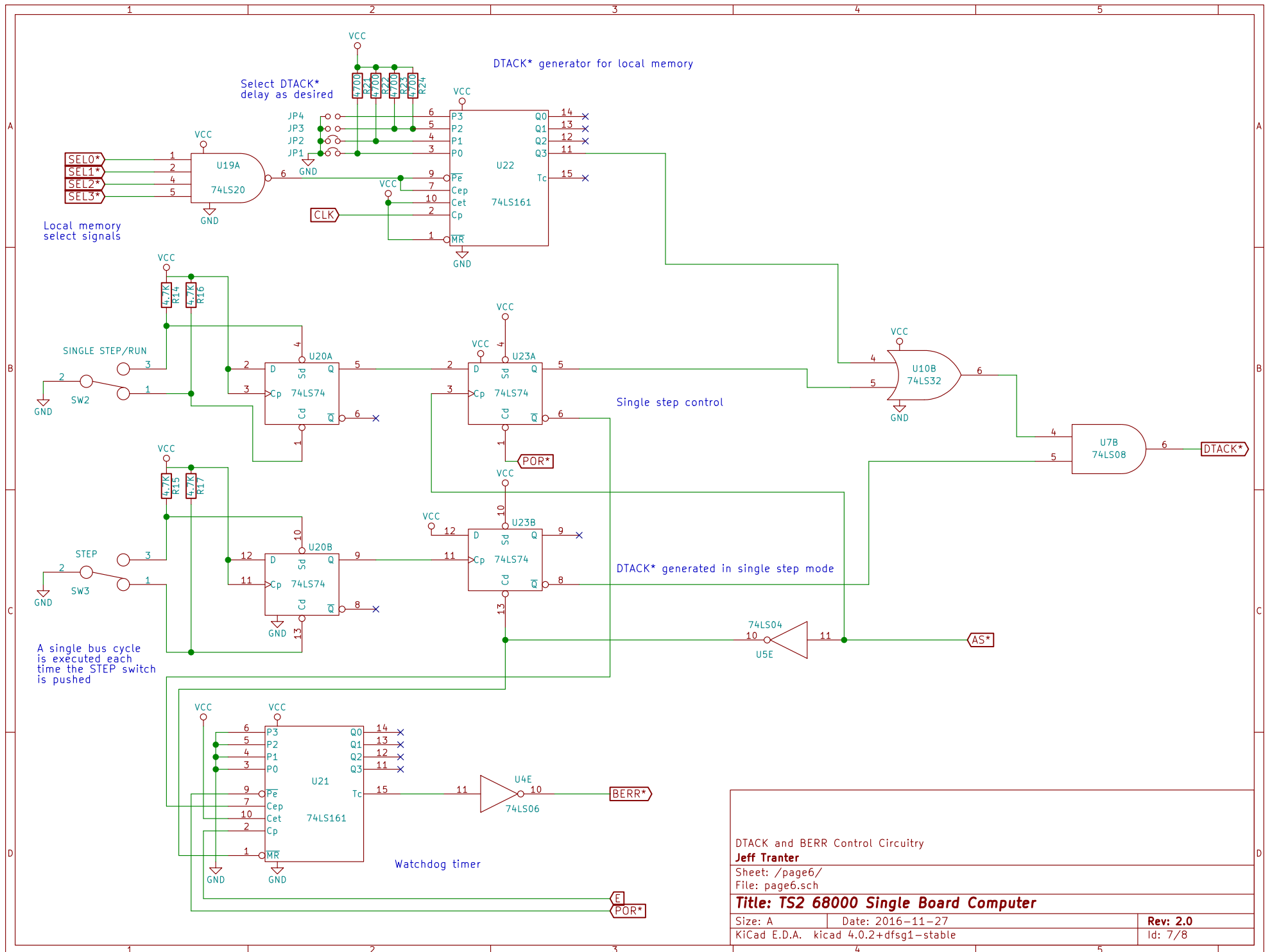KiCad E.D.A. kicad 4.0.2+dfsg1—stable | Id: 5/8

RAM2 $4000 – $7FFF (ODD)

RAM2 $4000 – $7FFF (EVEN)

U15 — HM6264

Pin	Signal		Signal	Pin
10	A0	D0	11	D00
9	A1	D1	12	D01
8	A2	D2	13	D02
7	A3	D3	15	D03
6	A4	D4	16	D04
5	A5	D5	17	D05
4	A6	D6	18	D06
3	A7	D7	19	D07
25	A8			
24	A9			
21	A10			
23	A11			
2	A12			

A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13

VCC

CS_RAM2L* — 20 CS1
27 WE

CS2 26 VCC
OE 22 GND

GND

R/W*

U17 — HM6264

A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13

10	A0	D0	11	D08
9	A1	D1	12	D09
8	A2	D2	13	D10
7	A3	D3	15	D11
6	A4	D4	16	D12
5	A5	D5	17	D13
4	A6	D6	18	D14
3	A7	D7	19	D15
25	A8			
24	A9			
21	A10			
23	A11			
2	A12			

VCC

CS_RAM2U* — 20 CS1
27 WE

CS2 26 VCC
OE 22 GND

GND

R*/W

U16 — 28C64

A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13

10	A0	D0	11	D00
9	A1	D1	12	D01
8	A2	D2	13	D02
7	A3	D3	15	D03
6	A4	D4	16	D04
5	A5	D5	17	D05
4	A6	D6	18	D06
3	A7	D7	19	D07
25	A8			
24	A9			
21	A10			
23	A11			
2	A12			

VCC

26 NC
27 R/W*
1 NC

CS_ROM2L* — 20 CE
22 OE

GND

ROM2 $C000 – $FFFF (ODD)

U18 — 28C64

A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13

10	A0	D0	11	D08
9	A1	D1	12	D09
8	A2	D2	13	D10
7	A3	D3	15	D11
6	A4	D4	16	D12
5	A5	D5	17	D13
4	A6	D6	18	D14
3	A7	D7	19	D15
25	A8			
24	A9			
21	A10			
23	A11			
2	A12			

VCC

26 NC
27 R/W*
1 NC

CS_ROM2U* — 20 CE
22 OE

GND

ROM2 $C000 – $FFFF (EVEN)

DTACK* generator for local memory

Select DTACK*
delay as desired

SELO*
SEL1*
SEL2*
SEL3*

U19A

74LS20

Local memory
select signals

U22

74LS161

CLK

SINGLE STEP/RUN

SW2

U20A

74LS74

U23A

74LS74

Single step control

POR*

STEP

SW3

U20B

74LS74

U23B

74LS74

DTACK* generated in single step mode

A single bus cycle
is executed each
time the STEP switch
is pushed

U10B
74LS32

U7B
74LS08

DTACK*

74LS04

U5E

AS*

Watchdog timer

U21

74LS161

U4E

74LS06

BERR*

E

POR*

Select baud rate

9600
4800
2400
1200
600
300

FTDI

FTDI

ACIAs
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