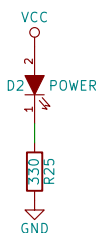
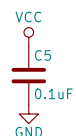
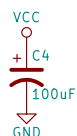
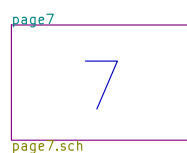
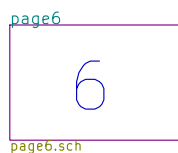
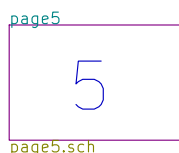
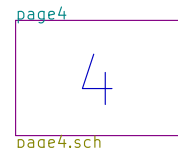
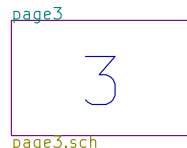
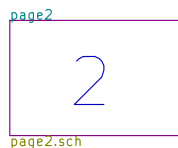
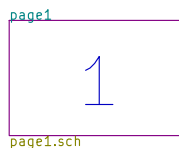
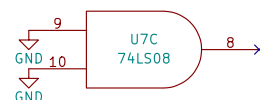
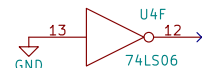


68000 Single Board Computer

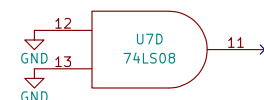
from "Microprocessor Systems Design" by Alan Clements Modified by Jeff Tranter



Bypass caps,
one per IC



Spare Gates



Top Level Schematic

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Sheet: /

File: ts2.sch

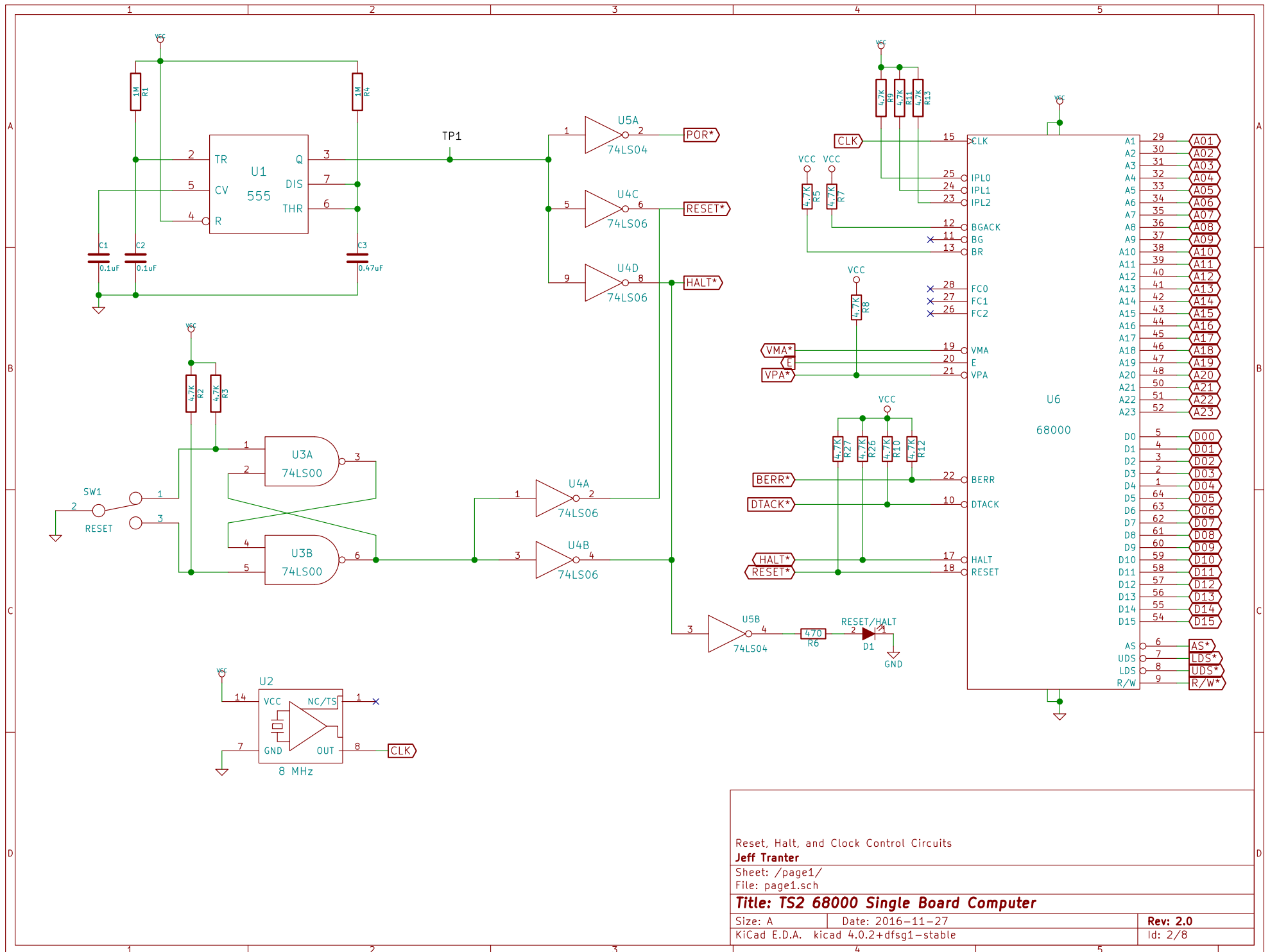
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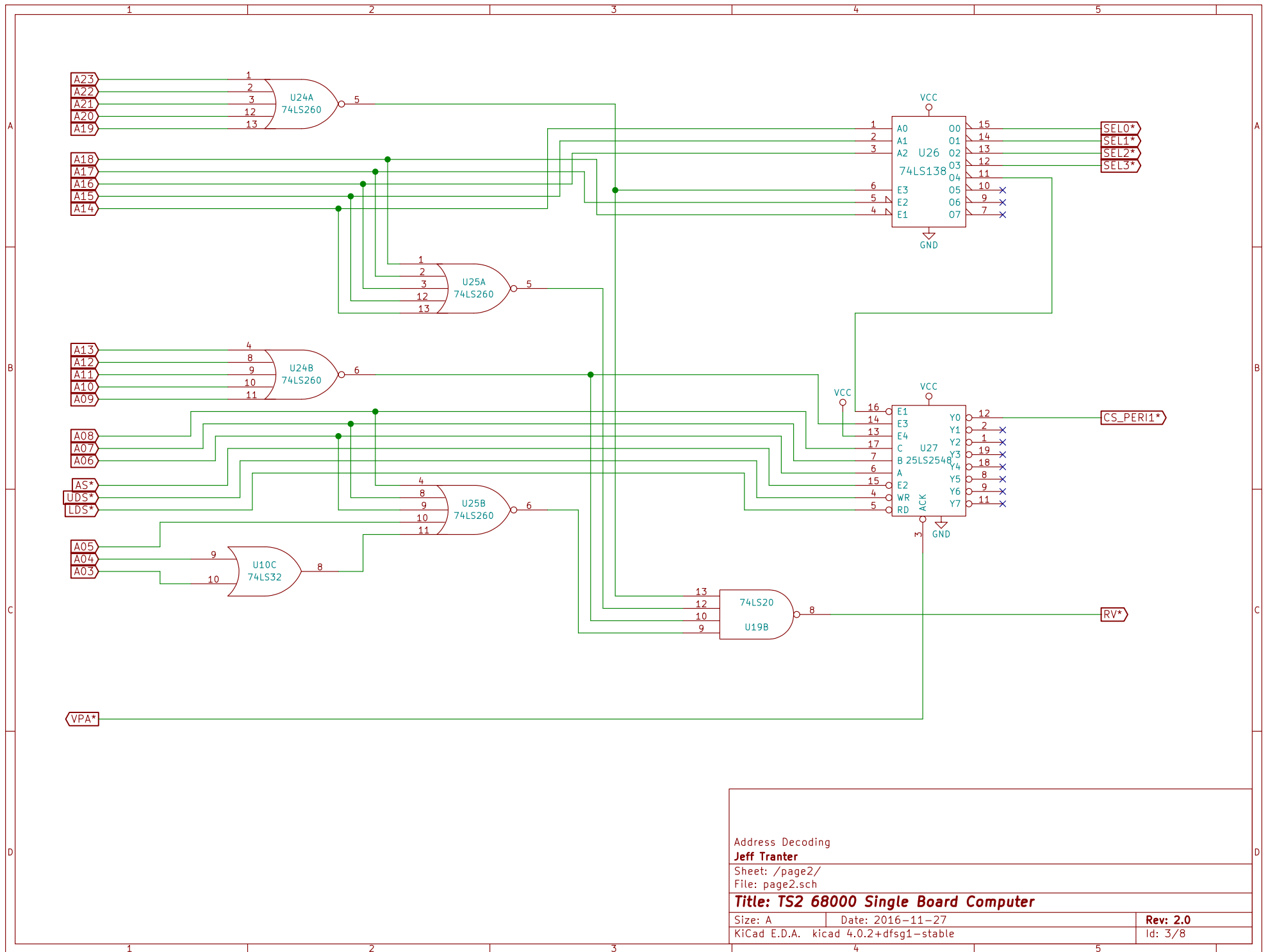
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Rev: 2.0

Id: 1/8





Address Decoding

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File: page2.sch

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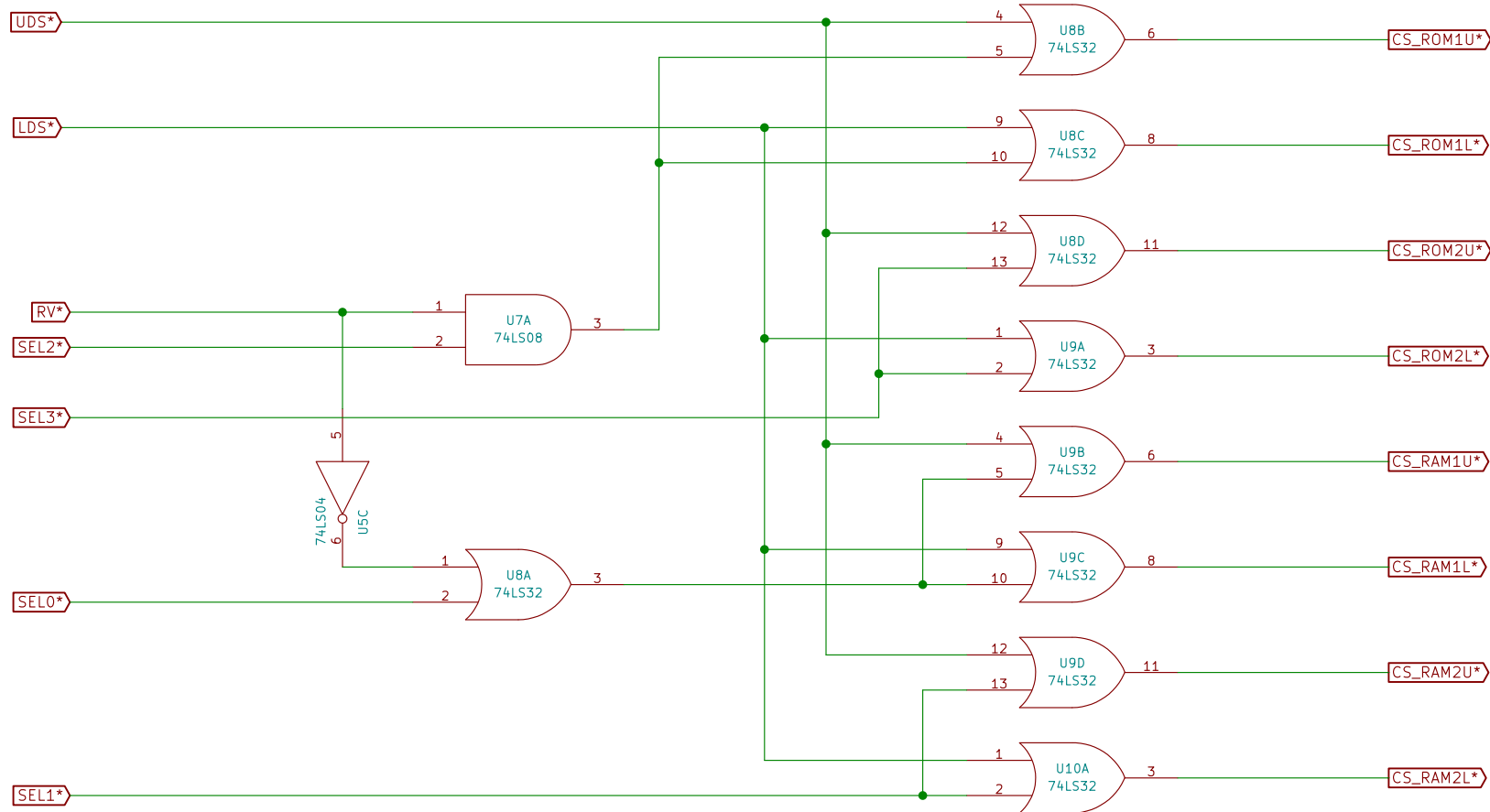
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Date: 2016-11-27

Rev: 2.0

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Id: 3/8



RAM and ROM Address Select

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File: page3.sch

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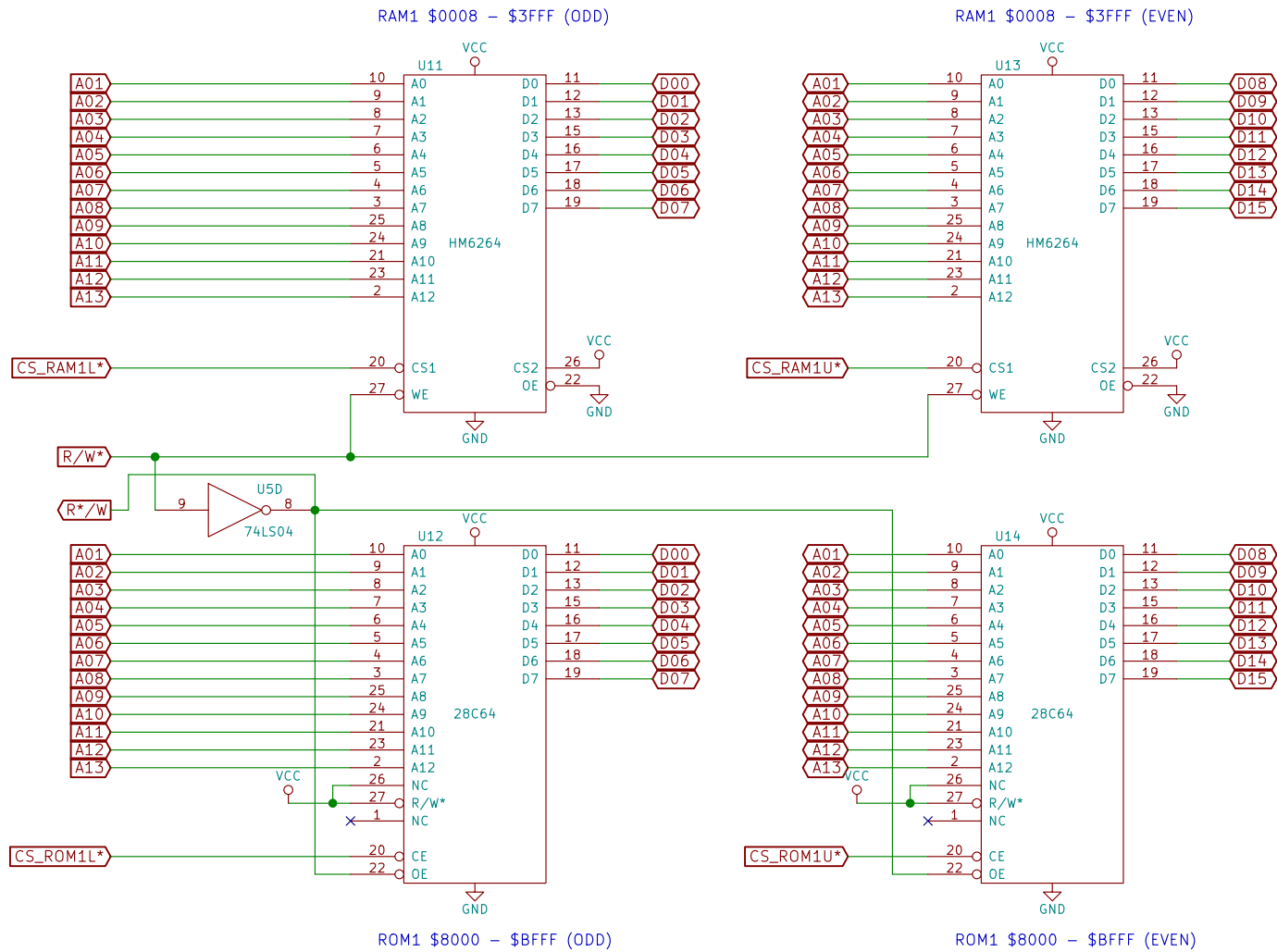
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Rev: 2.0

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RAM and ROM (1 of 2)

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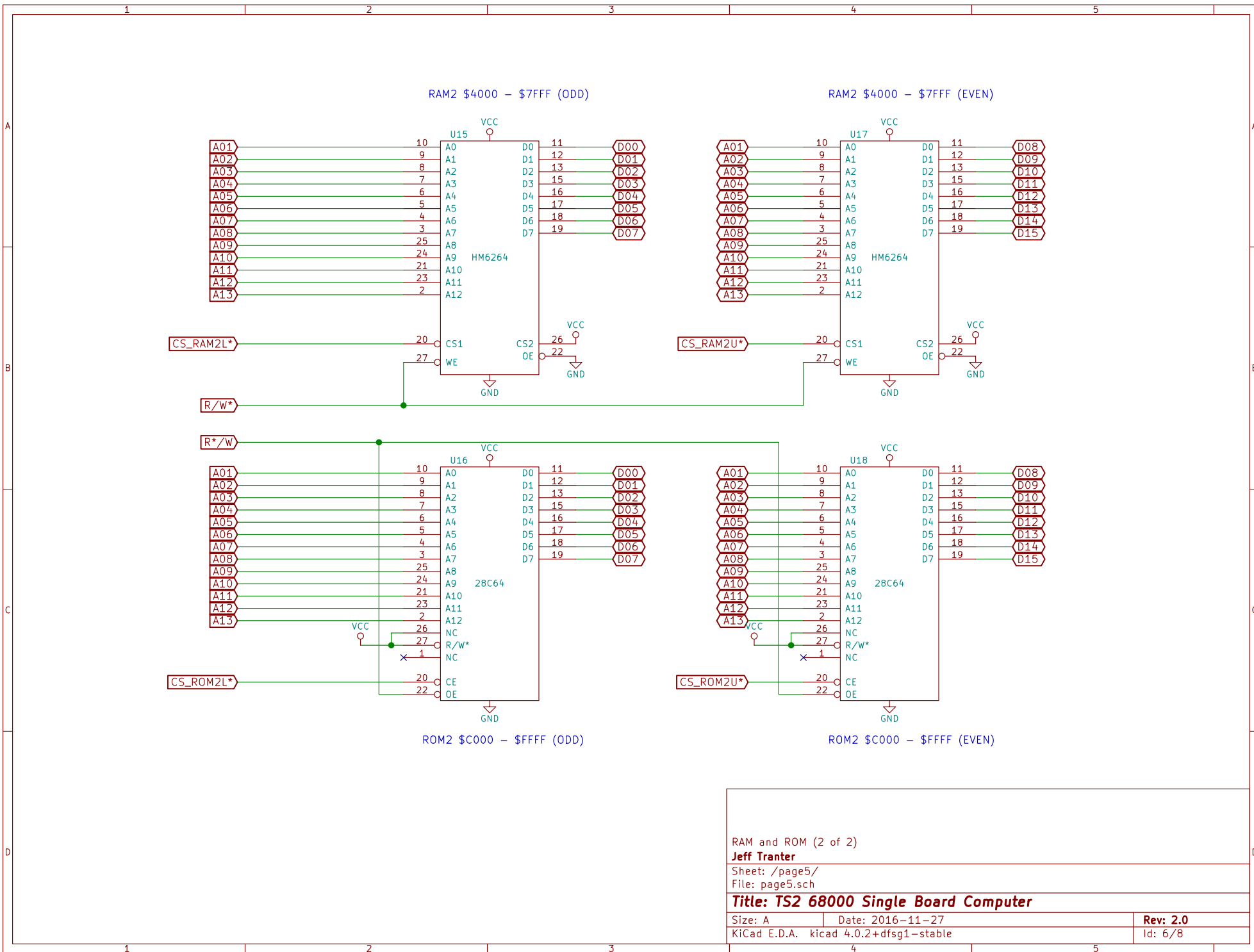
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Rev: 2.0
Id: 5/8



RAM and ROM (2 of 2)

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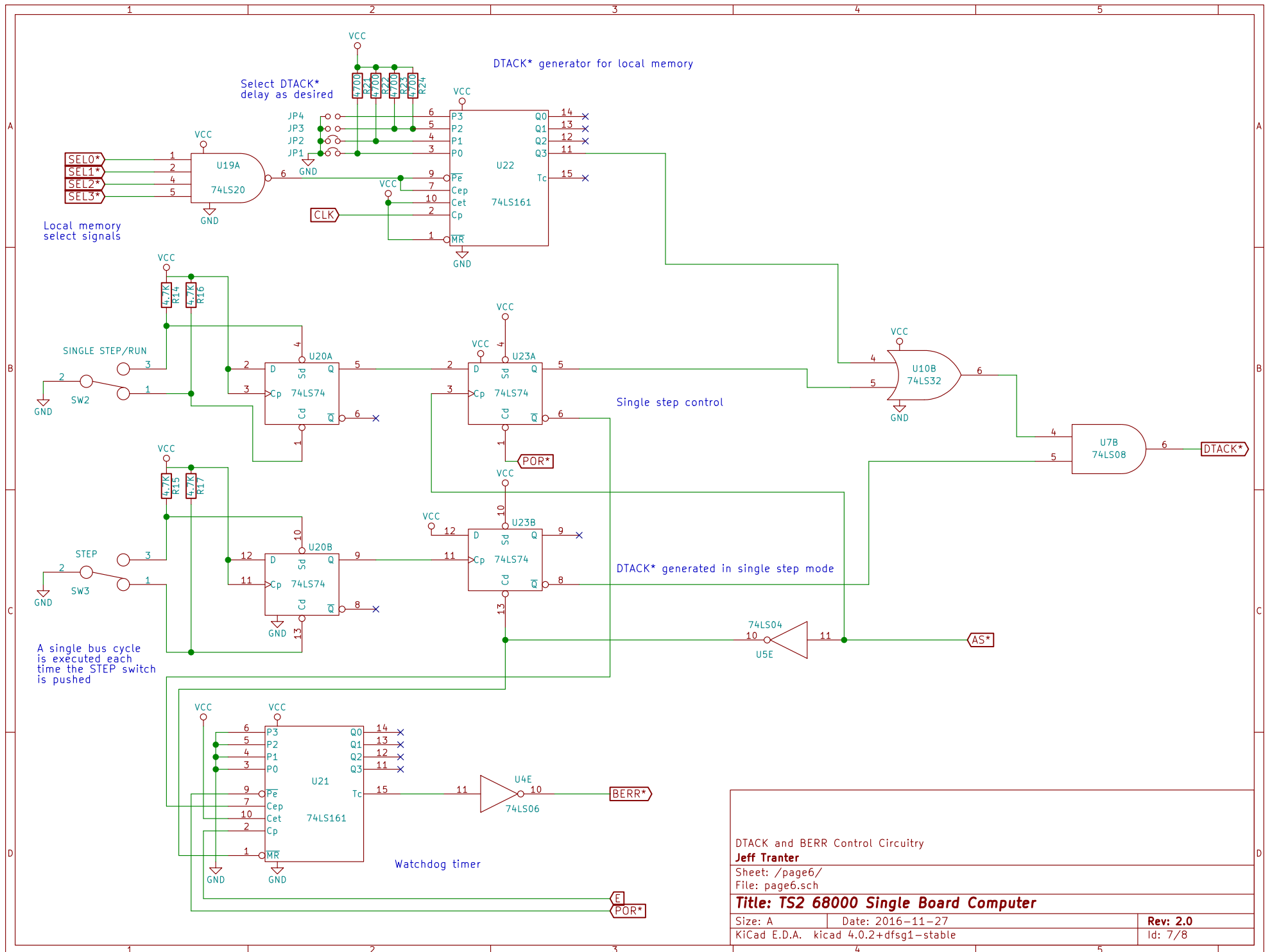
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Rev: 2.0
Id: 6/8



DTACK and BERR Control Circuitry

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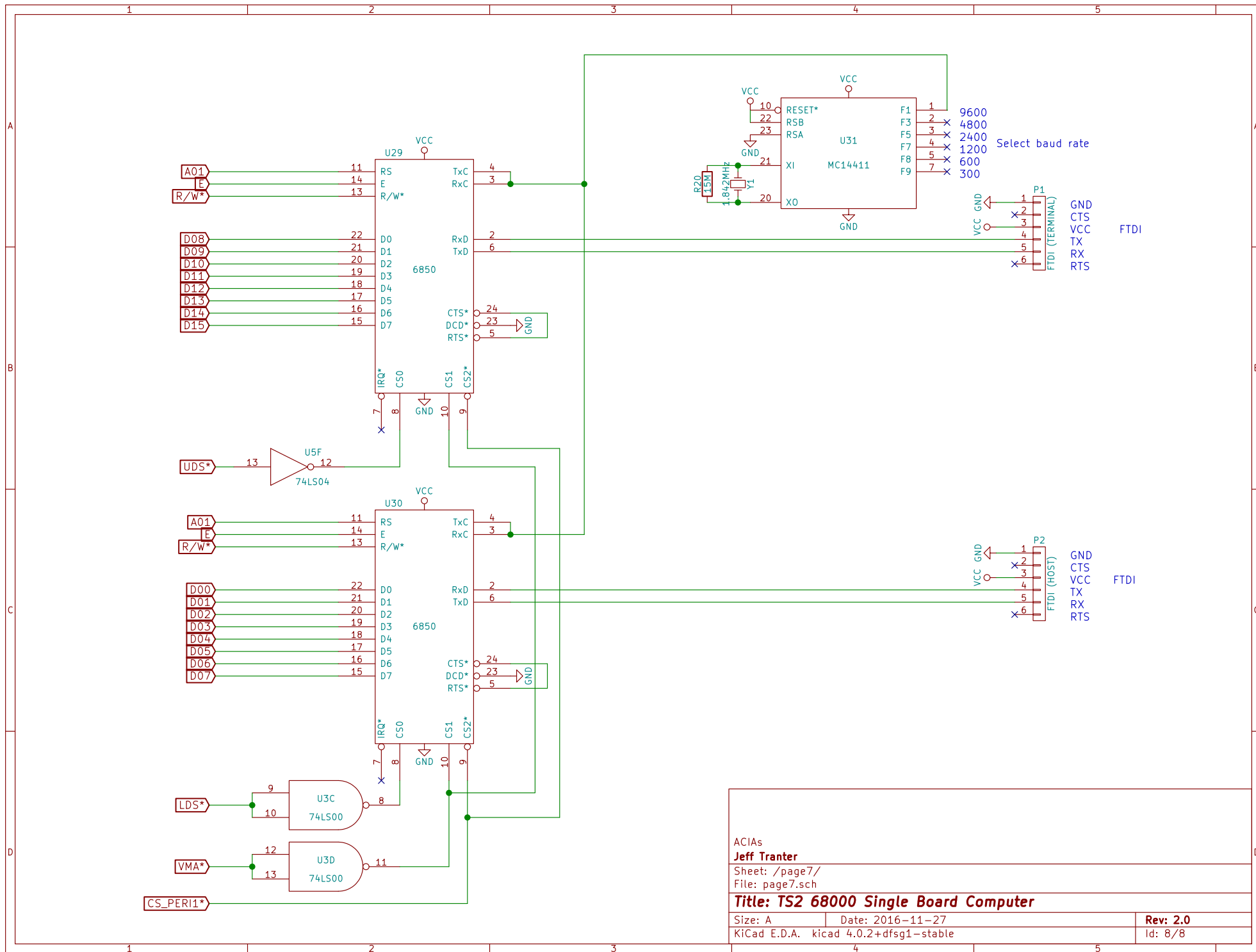
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Rev: 2.0

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Id: 7/8



ACIAs

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Title: TS2 68000 Single Board Computer

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Date: 2016-11-27

Rev: 2.0

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