68000 Single Board Computer
from
"Microprocessor Systems Design" by Alan Clements
Modified by Jeff Tranter

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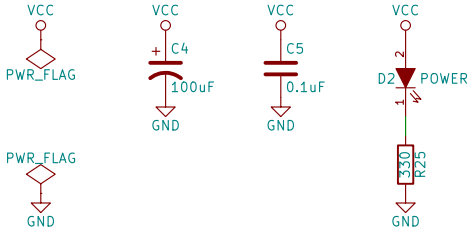
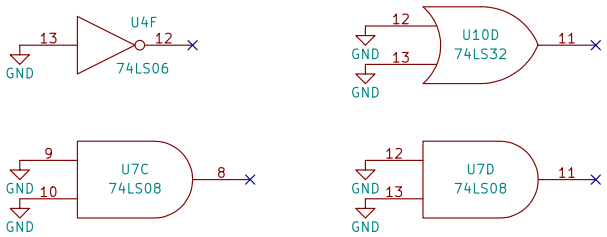
Bypass caps,
one per IC



Spare Gates



Top Level Schematic
Jeff Tranter
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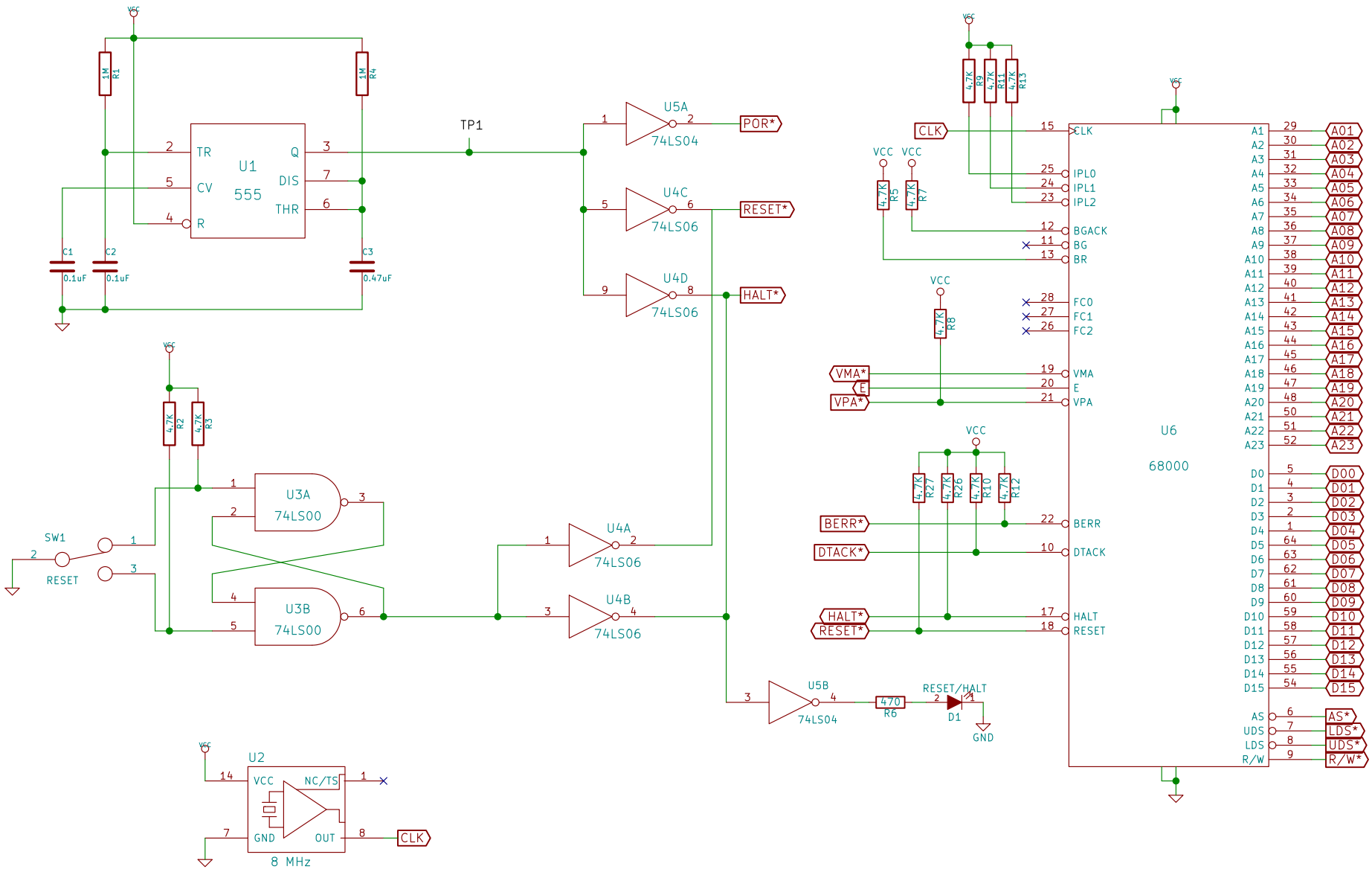
File: ts2.sch

Title: TS2 68000 Single Board Computer

Size: A	Date: 2016-11-27	**Rev: 2.0**
KiCad E.D.A. kicad 4.0.2+dfsg1-stable		Id: 1/8



Reset, Halt, and Clock Control Circuits

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Title: TS2 68000 Single Board Computer

Size: A	Date: 2016-11-27	**Rev: 2.0**
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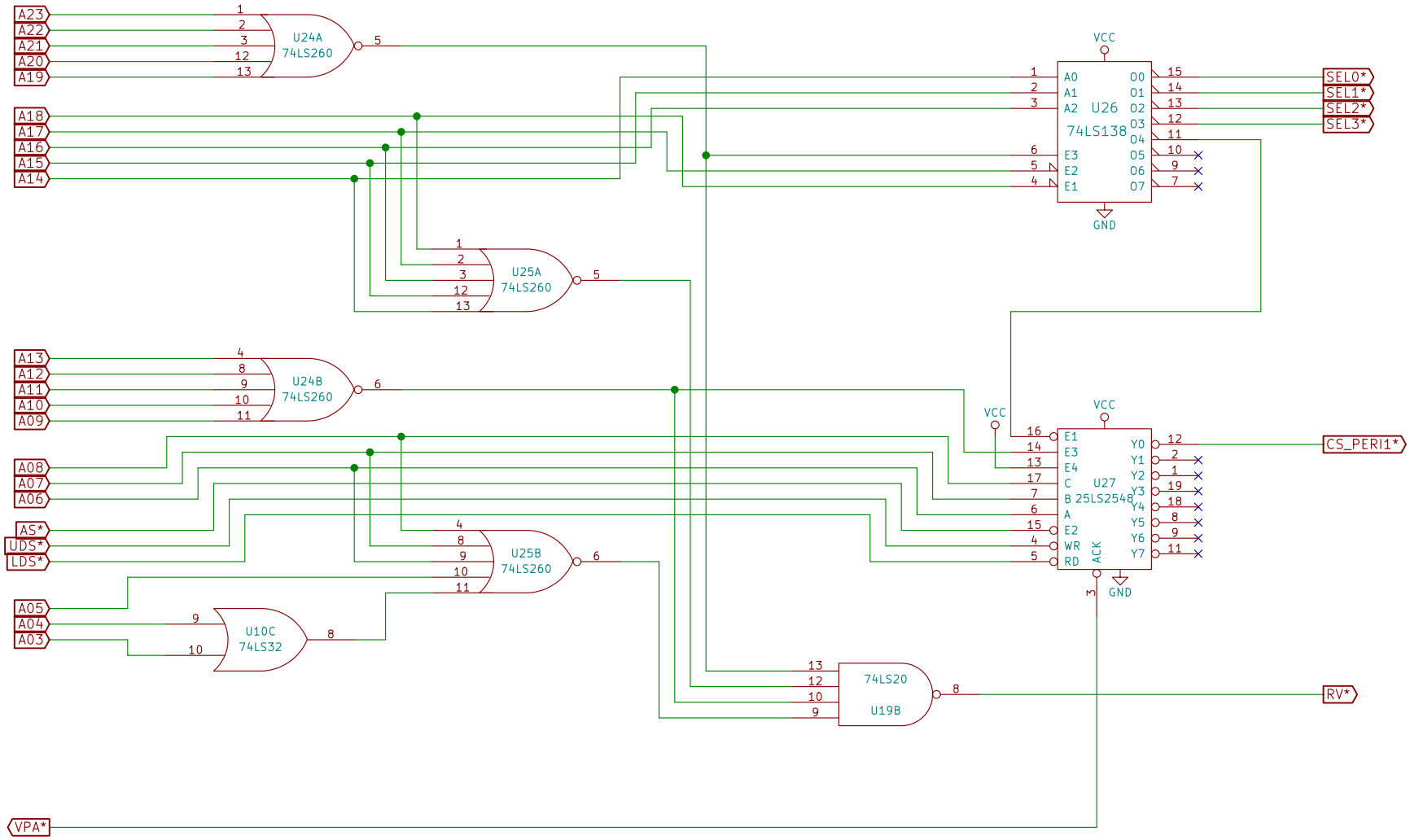

Address Decoding
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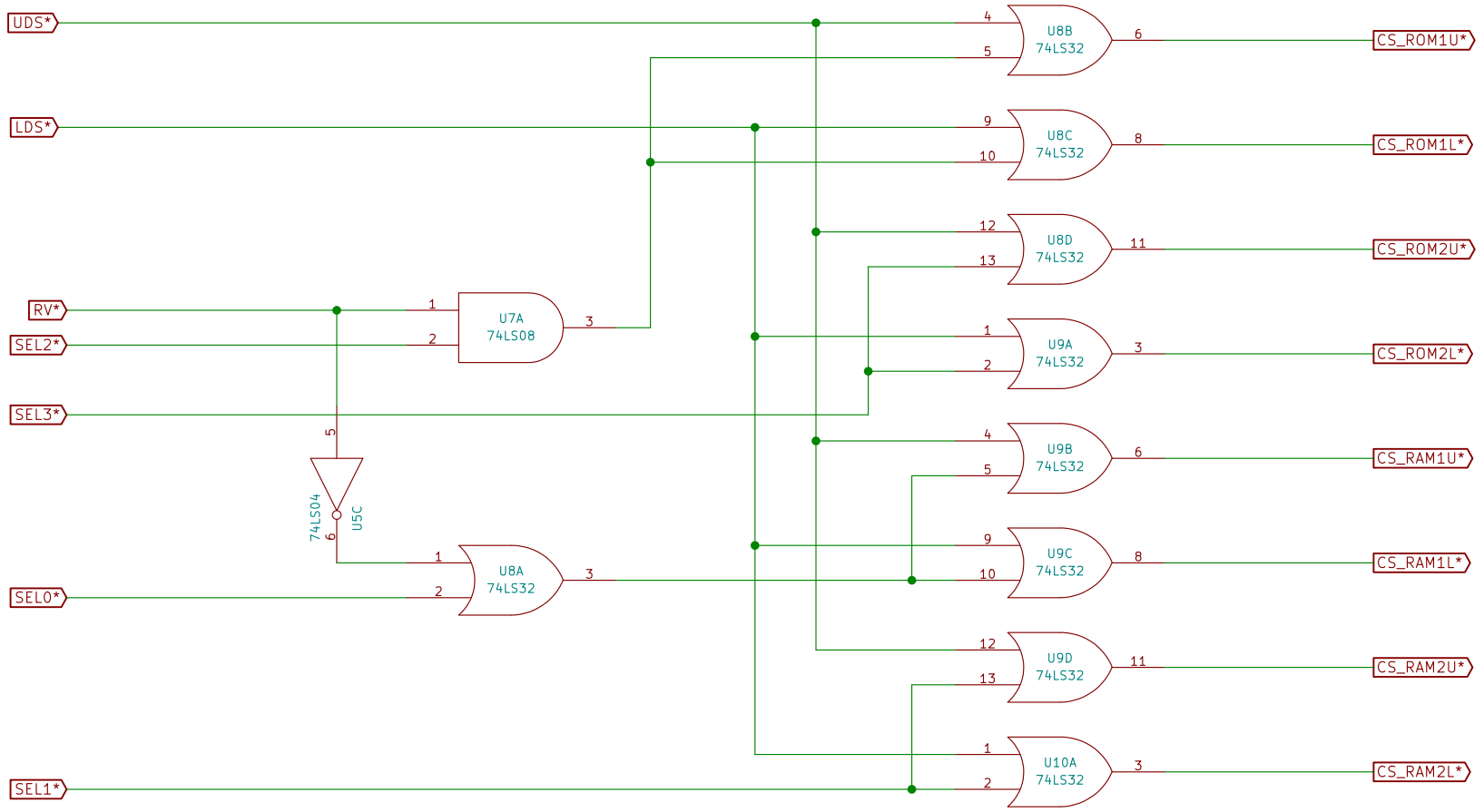
File: page2.sch

Title: TS2 68000 Single Board Computer

Size: A	Date: 2016-11-27	**Rev: 2.0**
KiCad E.D.A. kicad 4.0.2+dfsg1-stable		Id: 3/8



RAM and ROM Address Select

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Title: TS2 68000 Single Board Computer

Size: A	Date: 2016-11-27	**Rev: 2.0**
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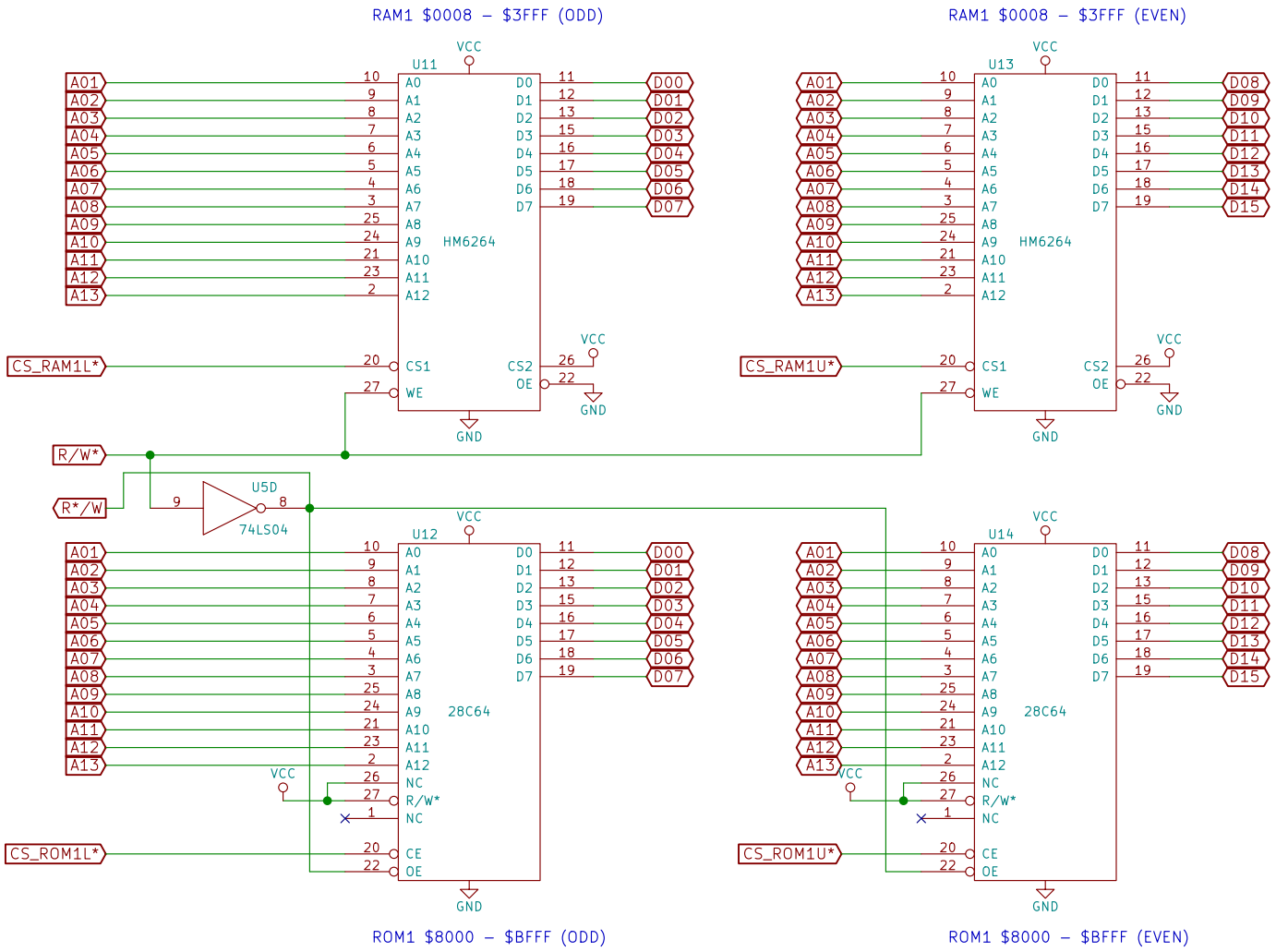

RAM and ROM (1 of 2)

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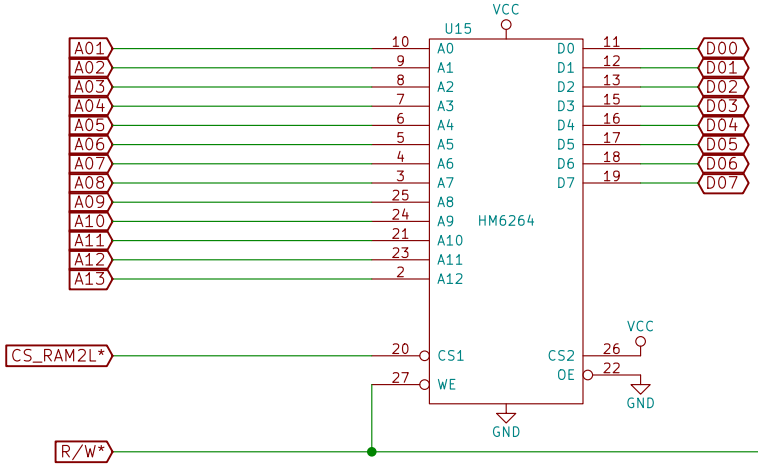
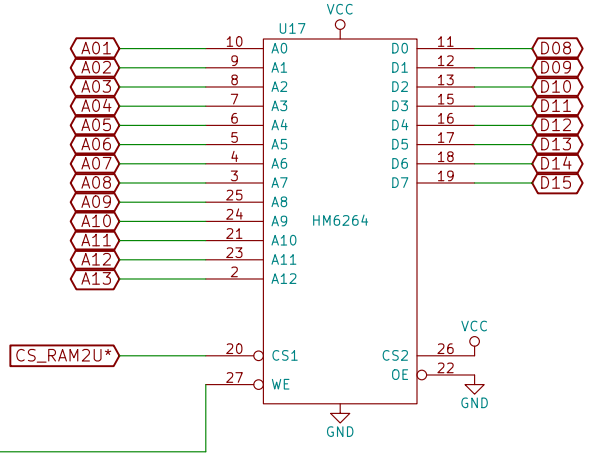
Title: TS2 68000 Single Board Computer

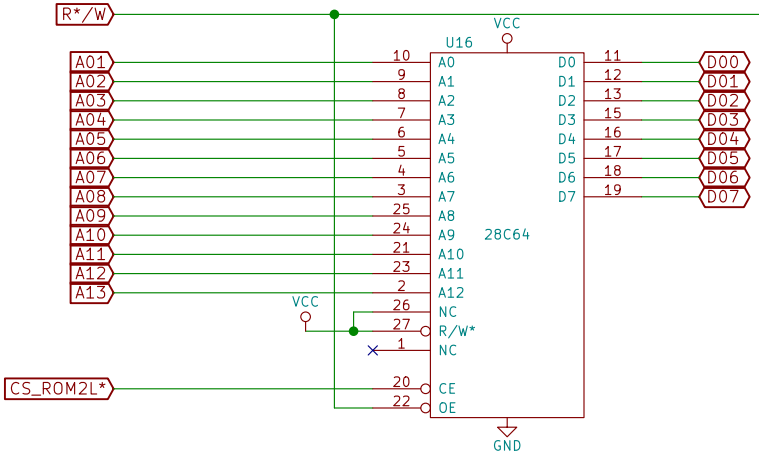
Size: A	Date: 2016-11-27	**Rev: 2.0**
KiCad E.D.A. kicad 4.0.2+dfsg1-stable		Id: 5/8

RAM2 $4000 – $7FFF (ODD)

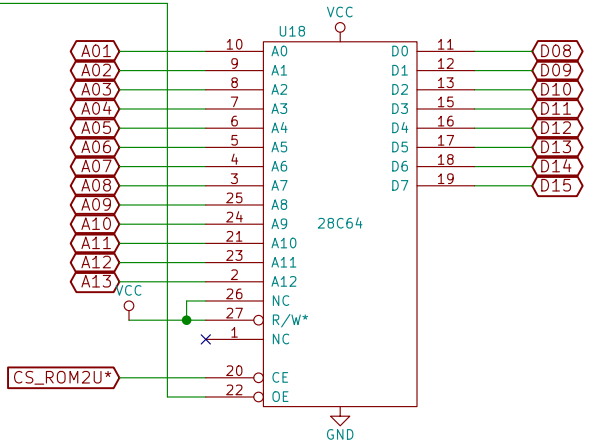


RAM2 $4000 – $7FFF (EVEN)





ROM2 $C000 – $FFFF (ODD)



ROM2 $C000 – $FFFF (EVEN)

RAM and ROM (2 of 2)
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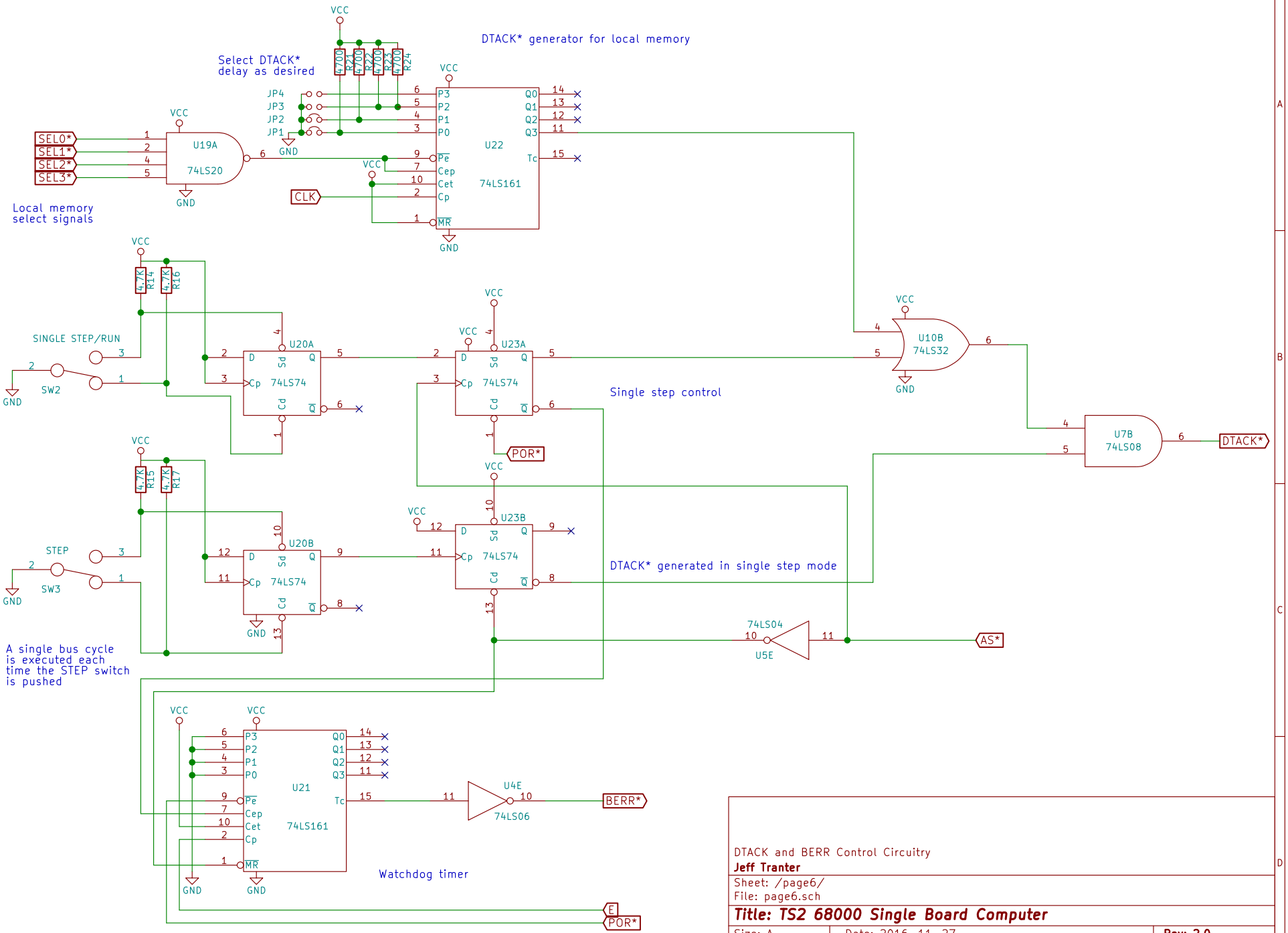
Title: TS2 68000 Single Board Computer

Size: A	Date: 2016-11-27	**Rev: 2.0**
KiCad E.D.A. kicad 4.0.2+dfsg1-stable		Id: 6/8


DTACK* generator for local memory
Select DTACK*
delay as desired
VCC
4700
R21
R22
R23
R24
JP4
JP3
JP2
JP1
GND
U22
74LS161
P3
P2
P1
P0
Pe
Cep
Cet
Cp
MR
Q0
Q1
Q2
Q3
Tc
CLK
SEL0*
SEL1*
SEL2*
SEL3*
U19A
74LS20
Local memory
select signals
4.7K
R14
R16
SINGLE STEP/RUN
SW2
U20A
74LS74
D
Cp
Sd
Cd
Q
U23A
POR*
Single step control
U10B
74LS32
U7B
74LS08
DTACK*
R15
R17
STEP
SW3
U20B
U23B
DTACK* generated in single step mode
74LS04
U5E
AS*
A single bus cycle
is executed each
time the STEP switch
is pushed
U21
Watchdog timer
U4E
74LS06
BERR*
E
POR*
DTACK and BERR Control Circuitry
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Title: TS2 68000 Single Board Computer
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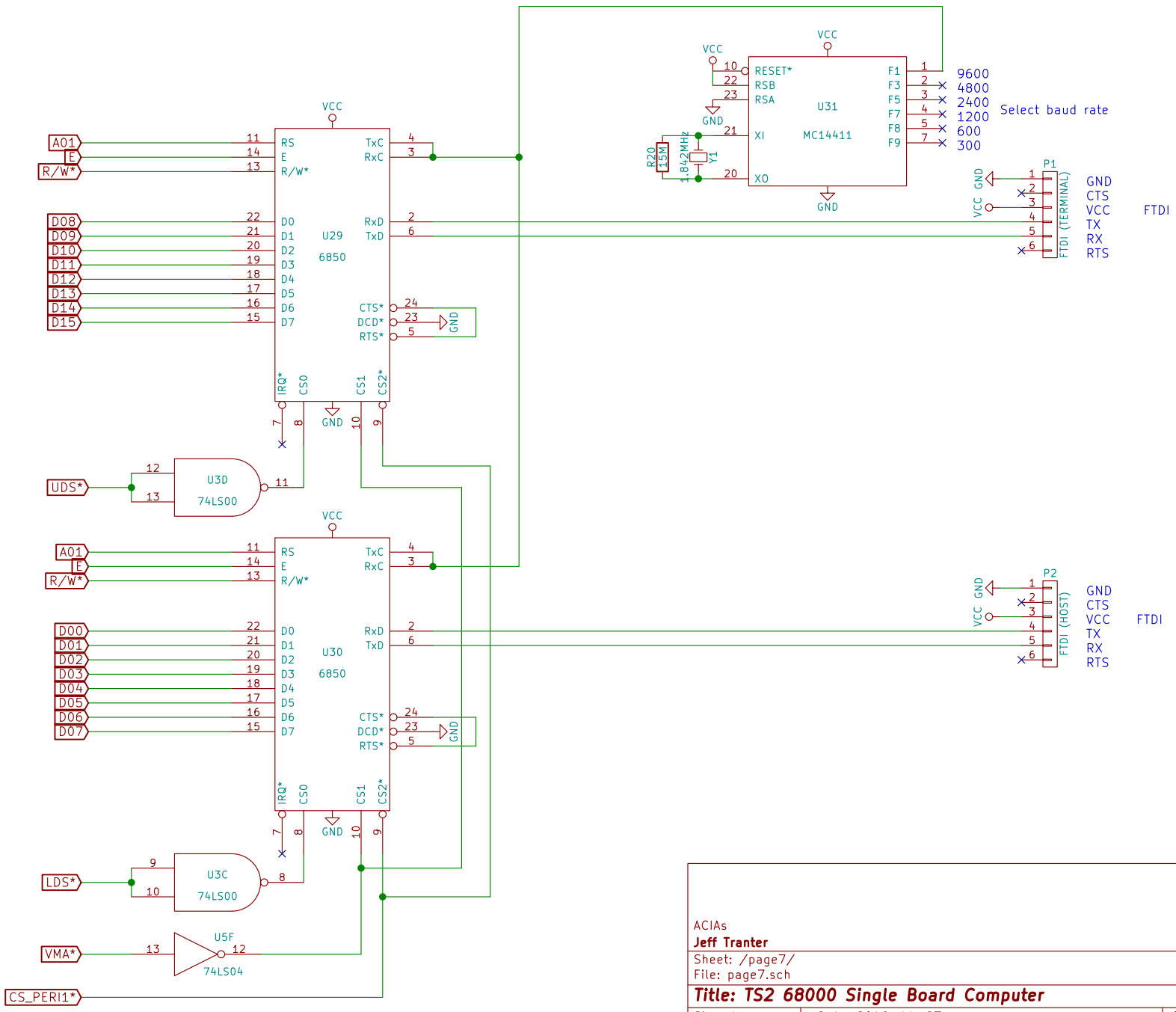
KiCad E.D.A. kicad 4.0.2+dfsg1-stable
Id: 7/8



ACIAs

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Title: TS2 68000 Single Board Computer

Size: A	Date: 2016-11-27	**Rev: 2.0**
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