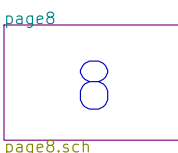
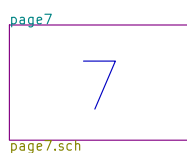
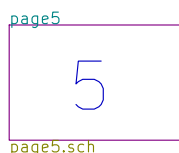
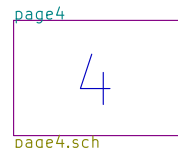
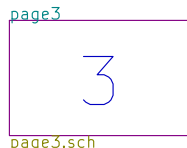
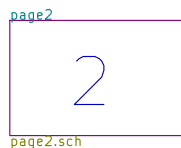
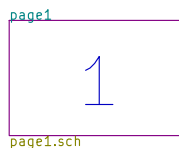


68000 Single Board Computer

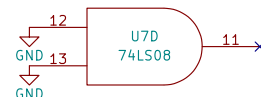
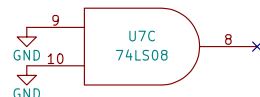
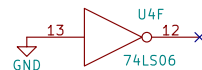
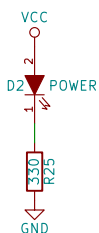
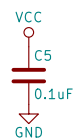
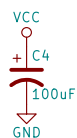
from

"Microprocessor Systems Design" by Alan Clements

Modified by Jeff Tranter



Bypass caps,
one per IC



Spare Gates

Top Level Schematic

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Sheet: /

File: ts2.sch

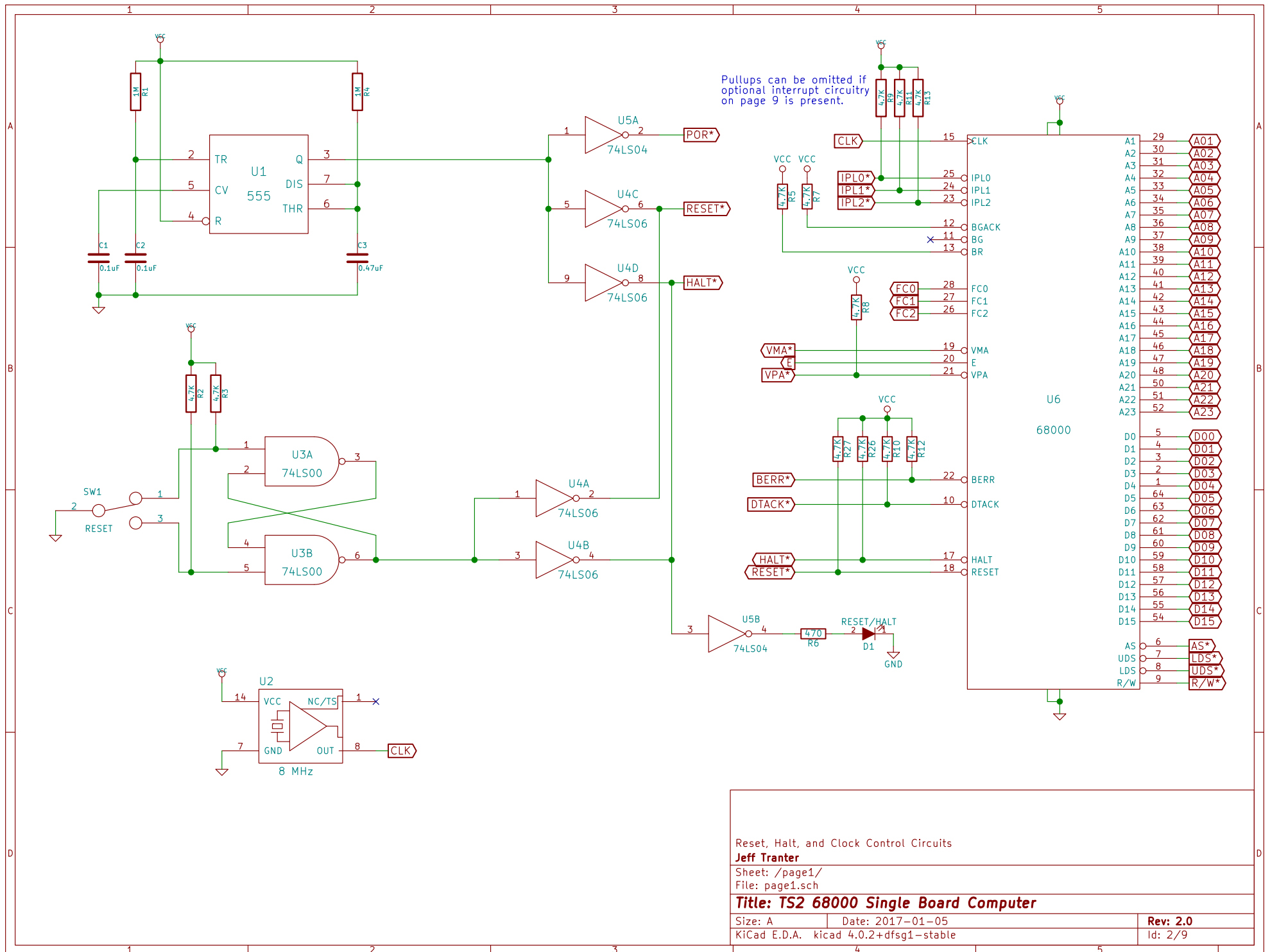
Title: TS2 68000 Single Board Computer

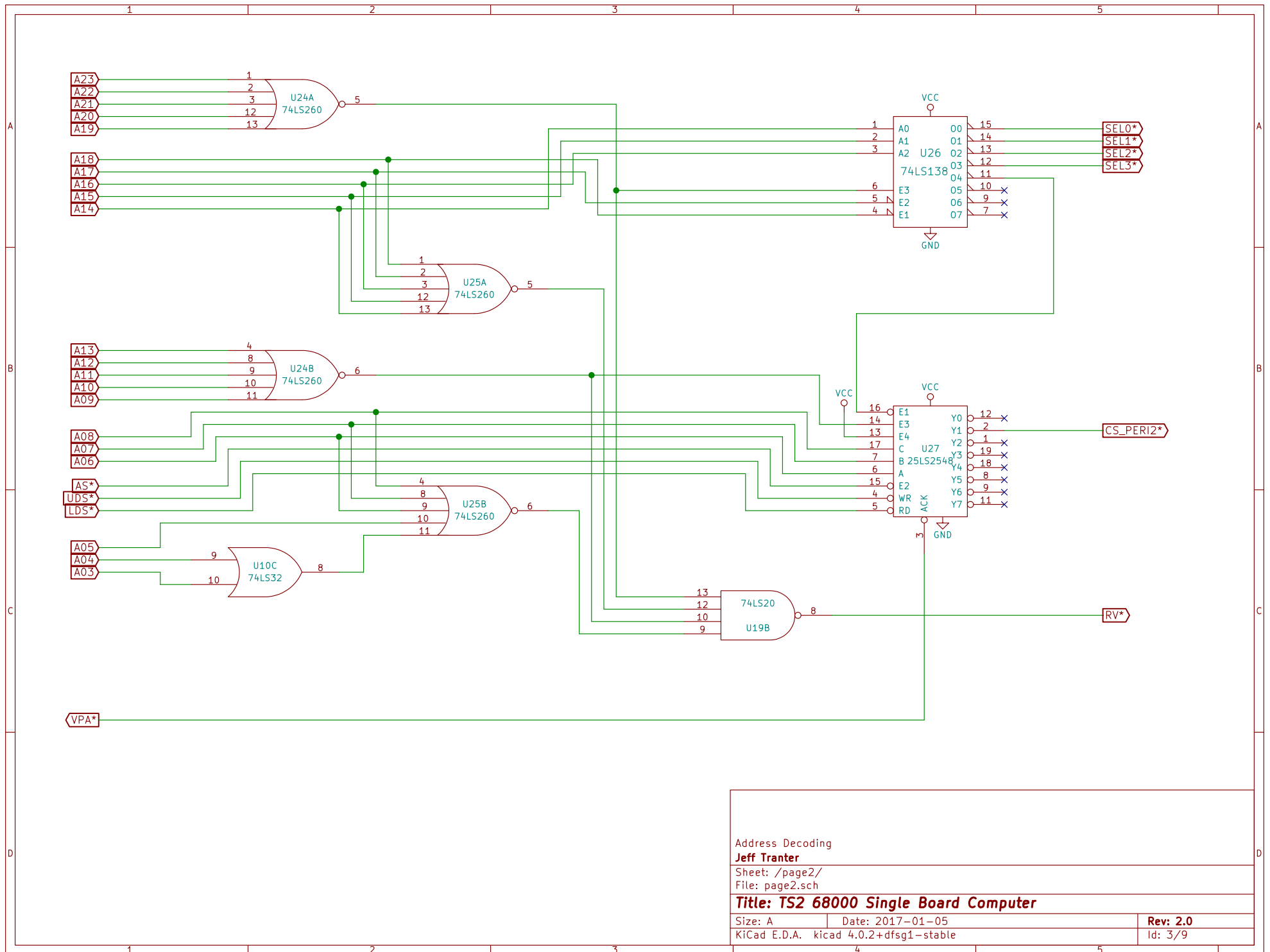
Size: A Date: 2017-01-05

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Id: 1/9





Address Decoding

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Sheet: /page2/

File: page2.sch

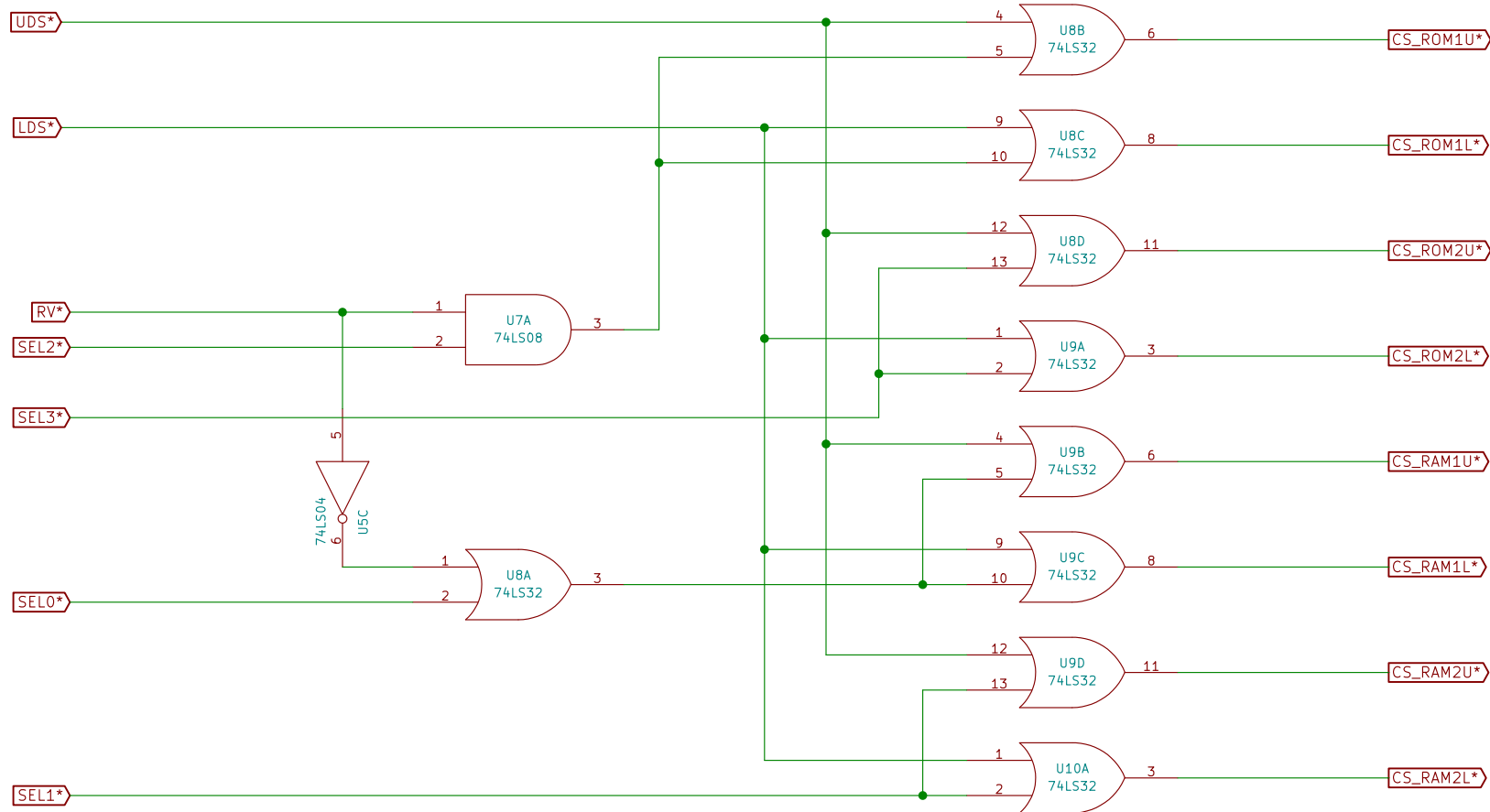
Title: TS2 68000 Single Board Computer

Size: A Date: 2017-01-05

KiCad E.D.A. kicad 4.0.2+dfsg1-stable

Rev: 2.0

Id: 3/9



RAM and ROM Address Select

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Sheet: /page3/

File: page3.sch

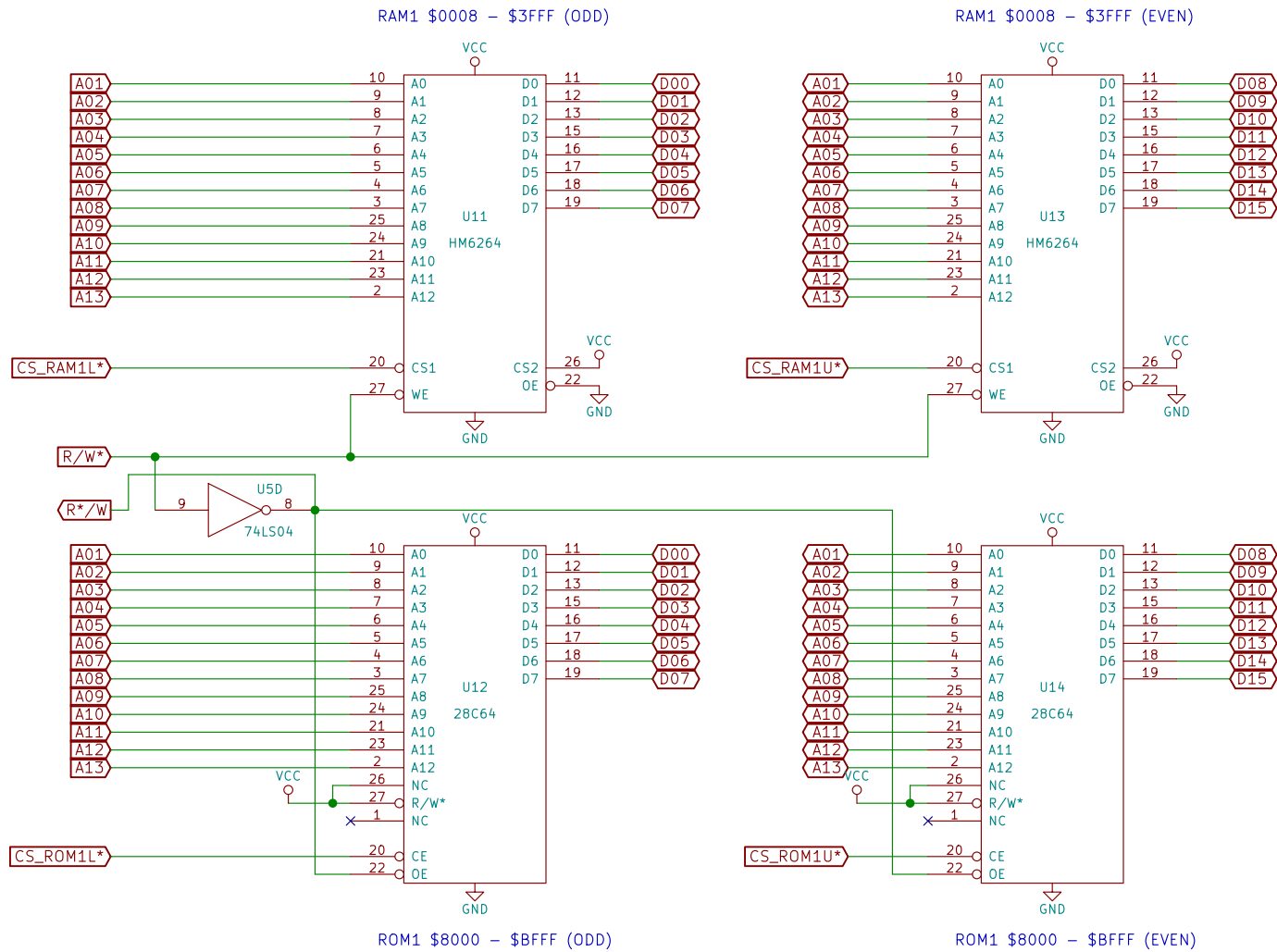
Title: TS2 68000 Single Board Computer

Size: A Date: 2017-01-05

KiCad E.D.A. kicad 4.0.2+dfsg1-stable

Rev: 2.0

Id: 4/9



RAM and ROM (1 of 2)

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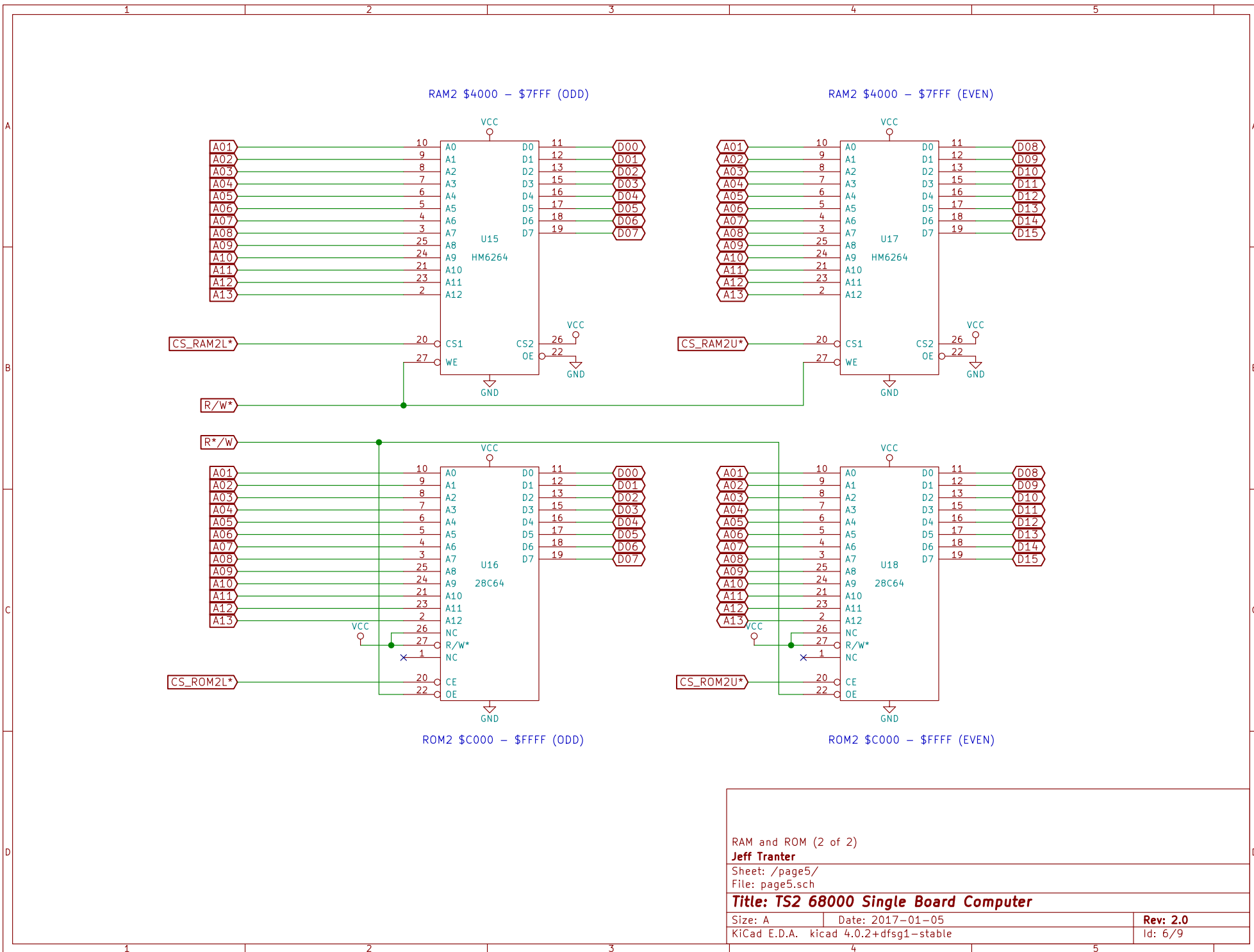
Sheet: /page4/

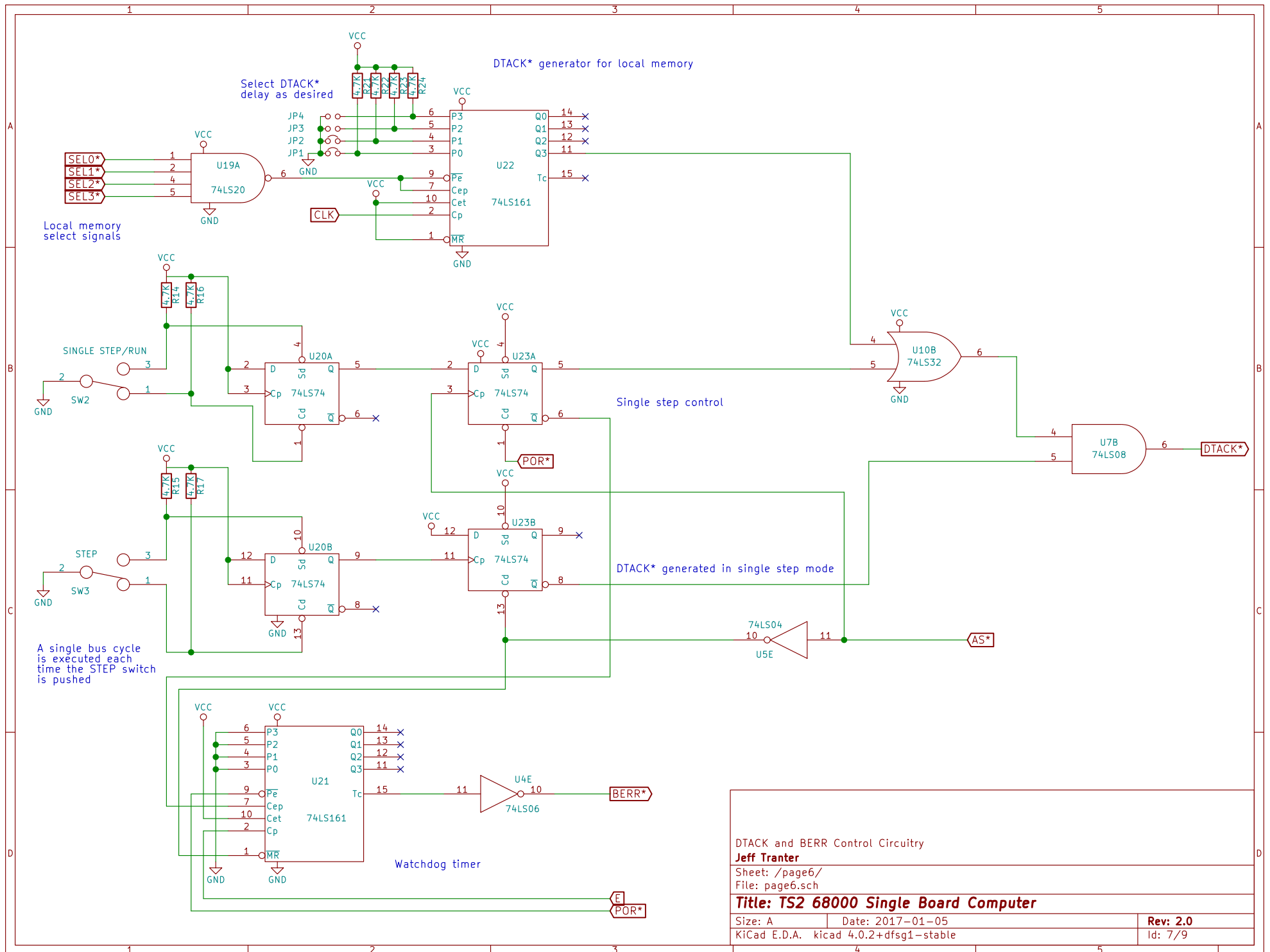
File: page4.sch

Title: TS2 68000 Single Board Computer

Size: A Date: 2017-01-05
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Rev: 2.0
Id: 5/9





DTACK and BERR Control Circuitry

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Sheet: /page6/

File: page6.sch

Title: TS2 68000 Single Board Computer

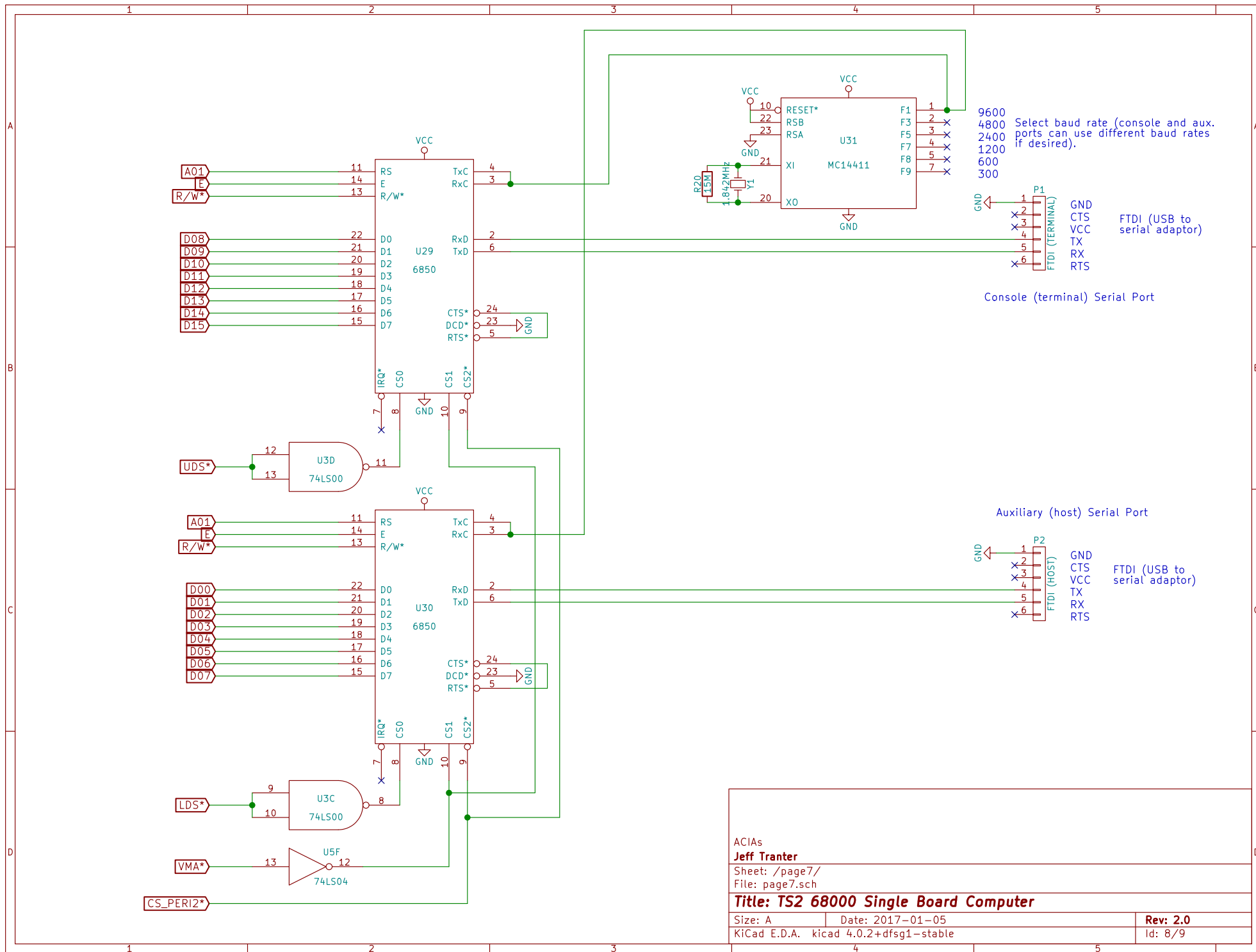
Size: A

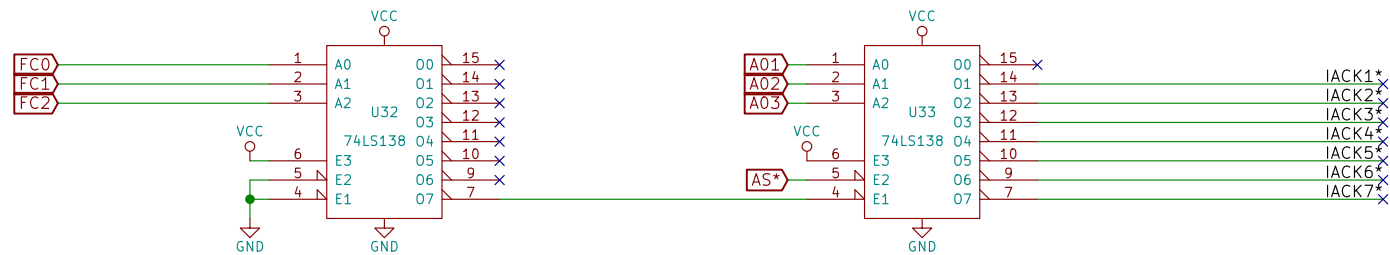
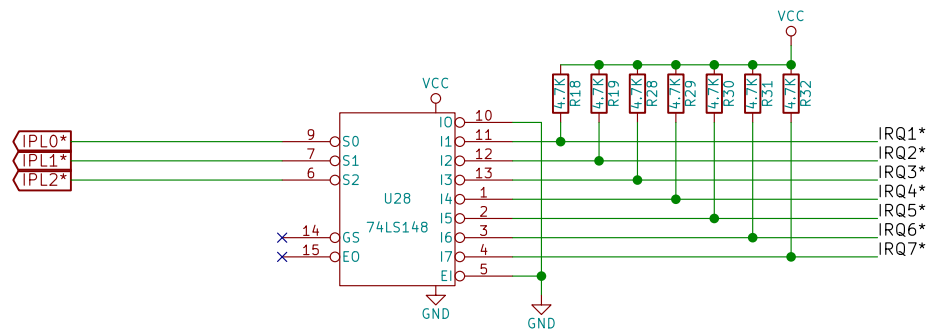
Date: 2017-01-05

Rev: 2.0

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Id: 7/9





Interrupt Control Circuitry (optional)

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Sheet: /page8/

File: page8.sch

Title: TS2 68000 Single Board Computer

Size: A4

Date: 2017-01-05

Rev: 2.0

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Id: 9/9