THE ARMADEUS PROJECT

DATASHEET

APF9328 DEV LIGHT

o.D

8. November 2006

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Edition	*Date*	*Changes*
Edition 0.A (PCB ed 1)	16. February 2006	Initial version
Edition 0.B (PCB ed 1)	4. September 2006	Add signal tables
Edition 0.C (PCB ed 1)	8. September 2006	Fix error in signal tables concerning DAC_REF and DAC_OUT2. Rename DAC_OUT1 to DAC_OUTA and DAC_OUT2 to DAC_OUTB according to the DAC datasheet
Edition 0.D (PCB ed 1.1)	8. November 2006	Add APFDevLight photo

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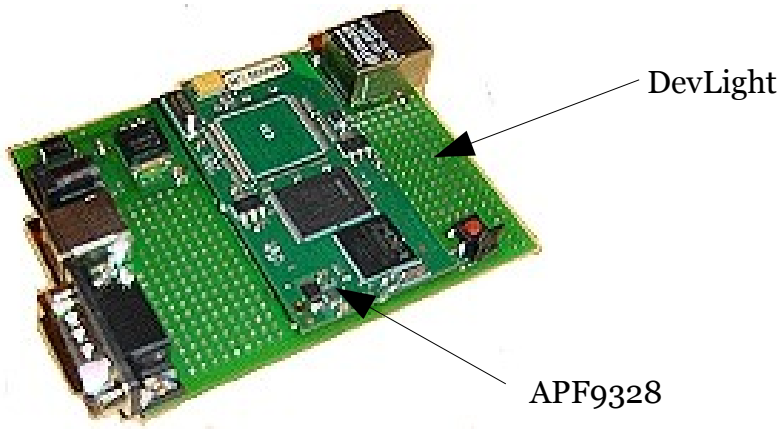
Chapter 1: APF9328 DevLight Overview

1.1 Introduction

The APF9328 Dev Light is low cost development board dedicated to the APF9328 single board computer.

This board offers access to the most used functionalities of the APF9328. It's price and prototyping zones makes it ideal for rapid development of simple applications.



Note: an APF9328 is mounted on the DevLight for this photo.

1.2 Mechanical Overview

Size: 100 mm x 75 mm (3.9” x 3”)

1.3 APF9328 Dev Light Features

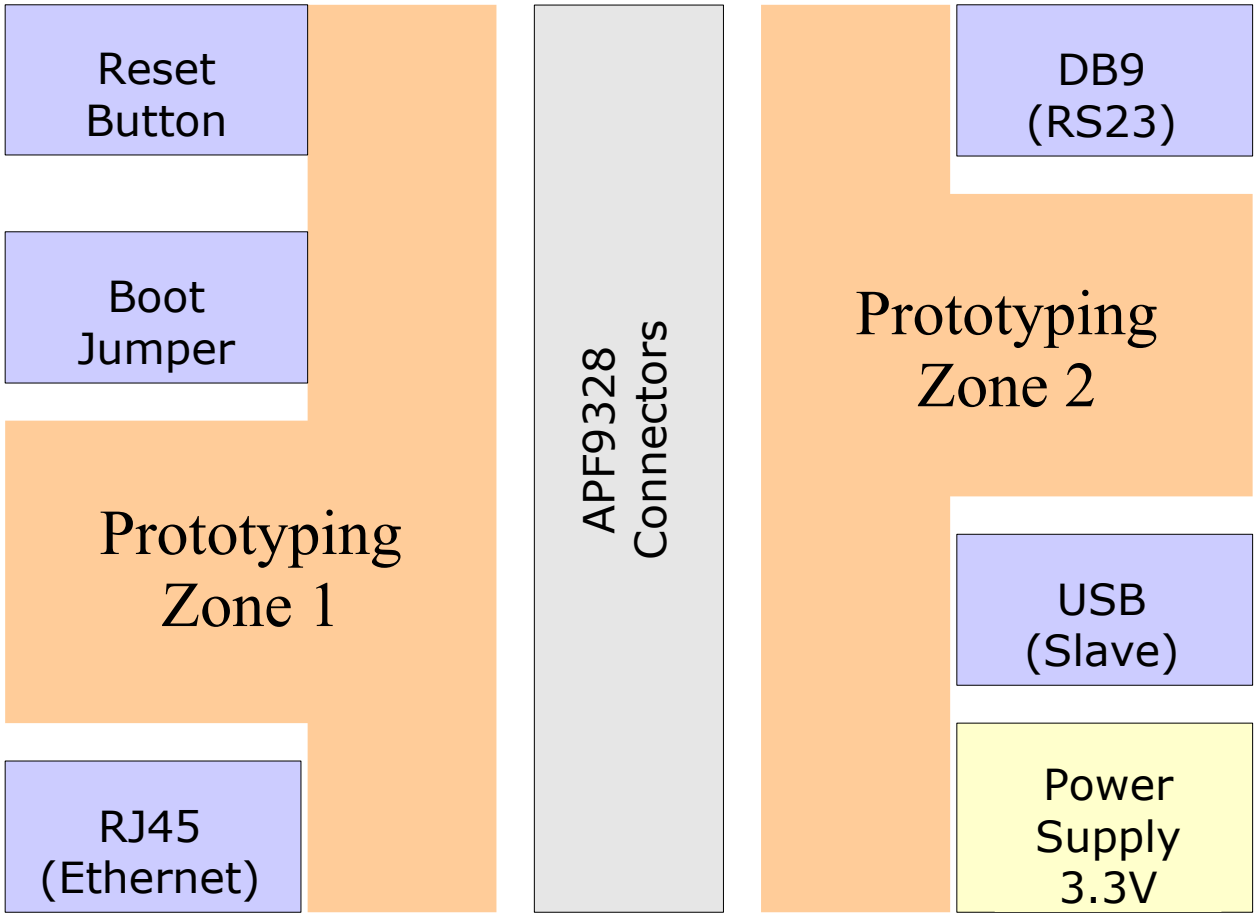
Input Power supply	7 to 12V DC with resettable fuse
On board regulator	3.3V / 1A max
Connectors	
	Ethernet (RJ45) with integrated isolation transformer
	USB slave (type B)
	DB9 header (RS232)
	Jack 2.5mm for power supply
	Two hirose receptacles for APF9328
Reset	Tact switch
Boot	Jumper for selecting the boot mode
Prototyping zone	Two prototyping zone with 2.54mm pitch holes
Silkscreen	Allows to easily recognize the APF9328 pins

1.4 Handling precautions

Please ensure that should a board need to be returned to Armadeus, it is adequately packed, preferably in the original packing material.

Chapter 2: Hardware Description

The following section provides a detailed description of the functions available on the APF9328.



2.1 Connectors

2.1.1 RS232 (DB9)

This connector provides a standard RS232 interface without RTS and CTS signals. ESD and overvoltage protections are located on the APF9328.

Remark: a RS232 cable has to be used to connect the APF9328 DevLight to a PC

2.1.2 USB (Slave)

The USB slave connector allows connecting the APFDevLight to your PC. The board, if correctly configured, will be seen as a slave device.

The USB transceiver is located on the APF9328 board and no protection against ESD have to be foreseen as they are already provided by the transceiver.

2.1.3 Ethernet (RJ45)

If the APF9328 is equipped with the Ethernet controller (-E option) the Ethernet connector can be used to connect your APF9328 DevLight to your network.

2.1.4 Boot Jumper

If a jumper is mounted on this 2 pin connector, the APF9328 will start in bootstrap mode. This mode can be useful if the APF9328 bios (uBoot) has been corrupted or lost. The RS232 is used to transfer uBoot from your PC to the internal flash of the APF9328. For more information please see the APF9328 Software Guide.

Reminder! Do not forget to remove the jumper after uBoot recovery

2.2 Power Supply

A linear regulator provides supply voltage (+3.3V) required by the APF9328. You can use the output for your experiments but take care to not sink more current that the maximum allowed (see Features chapter)

This regulator accept an external voltage between 5 and 12V.

It has to be noted that the board input is protected against short circuits by means of a resettable fuse.

2.3 Prototyping Zones and Silkscreen

Two prototyping zones have been foreseen to quickly test your application without having to create a new PCB. The pitch between pads is 2.54mm.

You will see that between the two Hirose receptacles (connectors for the APF9328) several pads are provided. They are connected to the main functions of the APF9328 board (see table below for details). You can simply connect some wrapping wires between these pads and the ones of the two prototyping zones. For this purpose, the bottom side of the APF9328 DevLight provides a silkscreen allowing to quickly identify the function of each pads.

The table below described the placement of the signals (bottom view)

CSI_D2	CSI_D1	CSI_D0	LD3_B3	LD2_B2	LD1_B1	LD0_B0
CSI_D5	CSI_D4	CSI_D3	LD7_G2	LD6_G1	LD5_G0	LD4_B4
CSI_PIXCLK	CSI_D7	CSI_D6	LD11_R0	LD10_G5	LD9_G4	LD8_G3
CSI_PIXCLK	CSI_VSYNC	CSI_HSYNC	LD15_R4	LD14_R3	LD13_R2	LD12_R1
UART1_CTS	UART1_RTS	CONTRAST	REV	CLS	PS	SPL_SPR
UART2_RTS	UART2_TX	UART2_RX	LSCLK	FLM_VSYNC	OE_ACD	LP_HSYNC
UART2_CTS		SPI_RDY	SPI_SSN	SPI_SCLK	SPI_MOSI	SPI_MISO
SSI0_RXFS	SSI0_TXFS	SSI0_TXCLK	SSI0_RXCLK	SSI0_RXDAT	SSI0_TXDAT	CLKO
SSI1_RXFS	SSI1_TXFS	SSI1_TXCLK	SSI1_RXCLK	SSI1_RXDAT	SSI1_TXDAT	
	SD_CMD	SD_CLK	SD_DAT3	SD_DAT2	SD_DAT1	SD_DAT0
TOUT2	TIN	PWM0		VREF5	I2C_SCL	I2C_SDA
L24N_3	L24P_3	L23N_3	L01N_5	L01P_5	L28P_5	L28N_5
L40P_2	L40N_3	L40P_3	L31P_5	L31N_5	L32P_5	L32N_5
L24N_2	L24P_2	L40N_2	L32N_4	L01N_3	L01P_3	IO_3
L22P_2	L23N_2	L23P_2	L20P_3	L20N_3	L21P_3	L21N_3
L21N_2	L21P_2	L22N_2	L22N_3	L22P_3	L23P_3	
L01P_2	L20N_2	L20P_2	AIN7	AIN6	AIN5	AIN4
L32N_0	L32P_0	L01N_2	AIN3	AIN2	AIN1	AIN0
L31P_0	L31N_0	L32N_1	EOCN	REFP	DAC_REF	DAC_OUTA
L30P_0	L30N_0	L27P_0	L27N_0	L01P_0	L01N_0	DAC_OUTB
L28N_1	L28P_1	IO1	L31P_1	L31N_1	L32P_1	
L01P_1	L01N_1					

On the left prototyping zone (bottom view) the vias are free excepted the ones placed near the hirose connectors.

TRSTN
TDO
TDI
TCK
TMS
CS5N
RWN
OEN
EB3N
D7
D6
D5
D4
D3
D2
D1
D0

On the right prototyping zone (bottom view) the vias are free excepted the ones placed near the hirose connectors (address labeled).

A4
A3
A2
A1
A0

2.3.1 APF9328 Features not accessible from the APF9328 DevLight

All the features of the APF9328 are accessible from the APF9328 DevLight excepted the following ones:

X1			***X2***		
Pin	Name	Function	Pin	Name	Function
24..32 / 88..97	A5..A23	Address Bus	28..35	D8..D15	Data Bus
36	CS1n	Chips Select 1	98	PA17	CS5n ready pin
			118	EXTAL16M	External 16M clock input
			23	EB2n	Enable for 16Bits write access
			26	CS3n	Chips Select 3
			25	CS4n	Chips Select 3