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# DATASHEET

## APF6_DEV

## V1.1

23. July 2015

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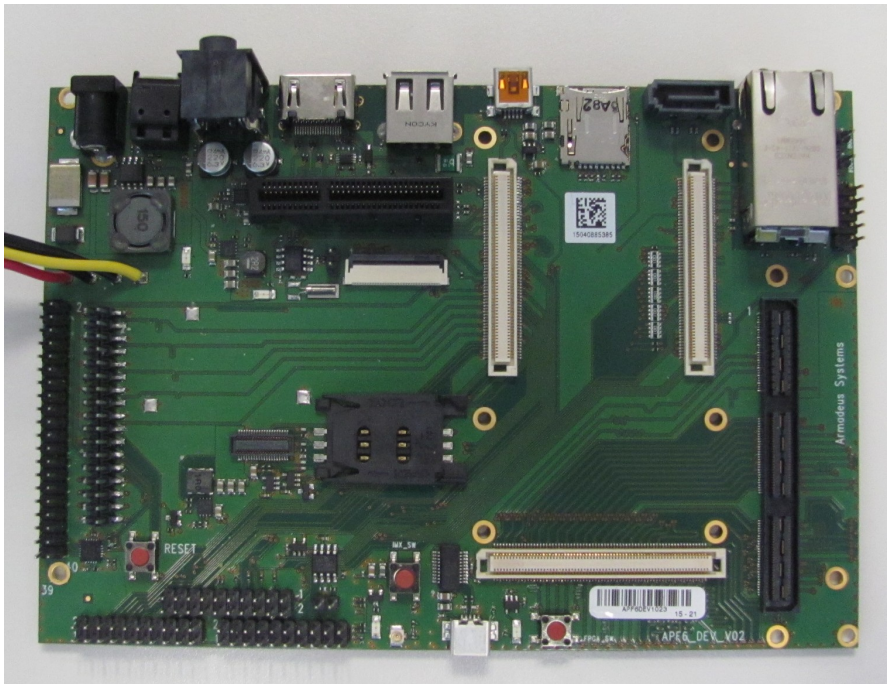
| *Edition* | *Date* | *Changes* |
|---|---|---|
| Edition 0.A (PCB ed 1) | 26/08/14 | Initial version |
| Edition 0.B (PCB ed 1) | 21/10/14 | Verification by FabienM |
| Edition 1.0 (PCB ed V02) | 29/06/15 | Published, FPGA led/button pinout correction |
| Edition 1.1 (PCB ed V02) | 10/07/15 | Add FPGA connector descriptions |

# 1 - APF6_Dev Overview

## 1.1 - Introduction

The APF6Dev/ APF6_SP_Dev is a full featured development board dedicated to the APF6 and APF6_SP single board computer.

This board offers access to the whole functionalities of the APF6 and provides several additional features. Its price and its connectors make it ideal for rapid development of embedded applications.



# 1.2 - APF6Dev Features

| | |
|---|---|
| Input Power supply | 12Vdc |
| On board regulators | 5V / 3A max DC/DC converter<br>3.3V / 3A max DC/DC converter |
| High speed USB HOST 2.0 | 1 port |
| USB OTG 2.0 | 1 port |
| Debug interface | USB miniB port. USB to serial converter present on the board |
| Ethernet | 10/100/1000 Mbits autoMDX with LEDs |
| TFT | CMOS and LVDS interfaces |
| Touchscreen | 4 wires resistive touch panel available on the CMOS TFT interface |
| Stereo Audio In/Out Controller | Headset stereo audio in/out |
| RTC | RTC backup with external battery |
| MicroSD | 1 port |
| CAN Controller | CAN 2.0b |
| SATA II | SATA data + power |
| PCI express Gen2 | 1 Lane **(can not be used if APF6_SP board mounted)** |
| HDMI | HDMI 1.4 |
| GPIOs | up to 64 gpios (through FPGA) |
| GSM/GPRS/3G | **Optional**. External antenna required. On boad SIM card connector |
| GPS | **Optional**. External antenna required |
| Standard Connectors | Jack 2.5mm for power supply<br>high speed USB host 2.0 (type A)<br>OTG high speeed USB (miniAB)<br>USB miniB for debug (serial emulation)<br>10/100/1000 Mbits Ethernet (RJ45) with leds<br>HDMI<br>SATA data + power<br>PCI express<br>dual 3,5mm stereo jack for audio in and out<br>microSD |
| Specific connectors | TFT interface including touchscreen (2.54mm header)<br>TFT LVDS interface<br>Extensions with CAN, GPIOs, UARTs, SPI, I2C, Keypad,<br>CMOS Sensor (FPC/FFC 33pin)<br>GPS antenna connector (Hirose U.FL)<br>GSM/GPRS/3G connector<br>SIM card socket<br>JTAG for iMX (2.54mm header)<br>JTAG for FPGA<br>HSMC connector for FPGA |
| User LEDs | 2x (one connected to the i.MX and the other to the FPGA) |
| User switches | 2x (one connected to the i.MX and the other to the FPGA) |
| Reset | Switch |

# 1.3 - Handling precautions

Please ensure that should a board need to be returned to Armadeus systems, it is adequately packed, preferably in the original packing material.

# 2 - Quick Start

At first an APF6 module needs to be plugged on **J7**.

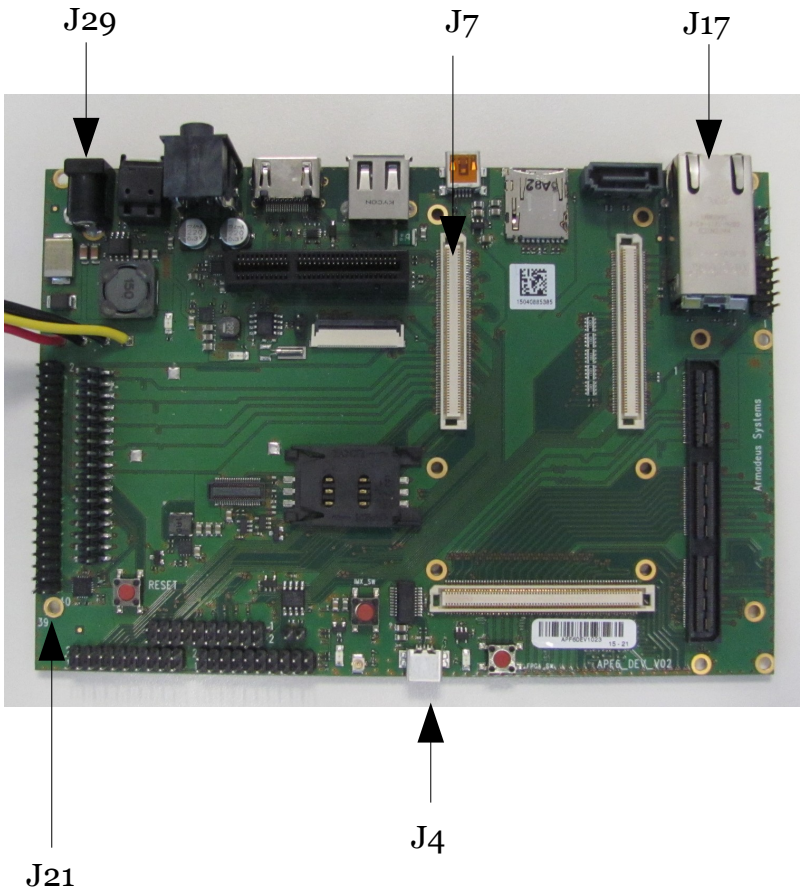
Once done, a power supply has to be connected to **J29**. The main characteristics of this input supply can be found in the section 3.1.1 below.

A micro-USB AB cable has to be connected between your PC and the micro USB connector (**J4**) of the board to get access to the debug console. See section 3.9 for details of the serial communication settings.

Ethernet cable can be connected to **J17**.

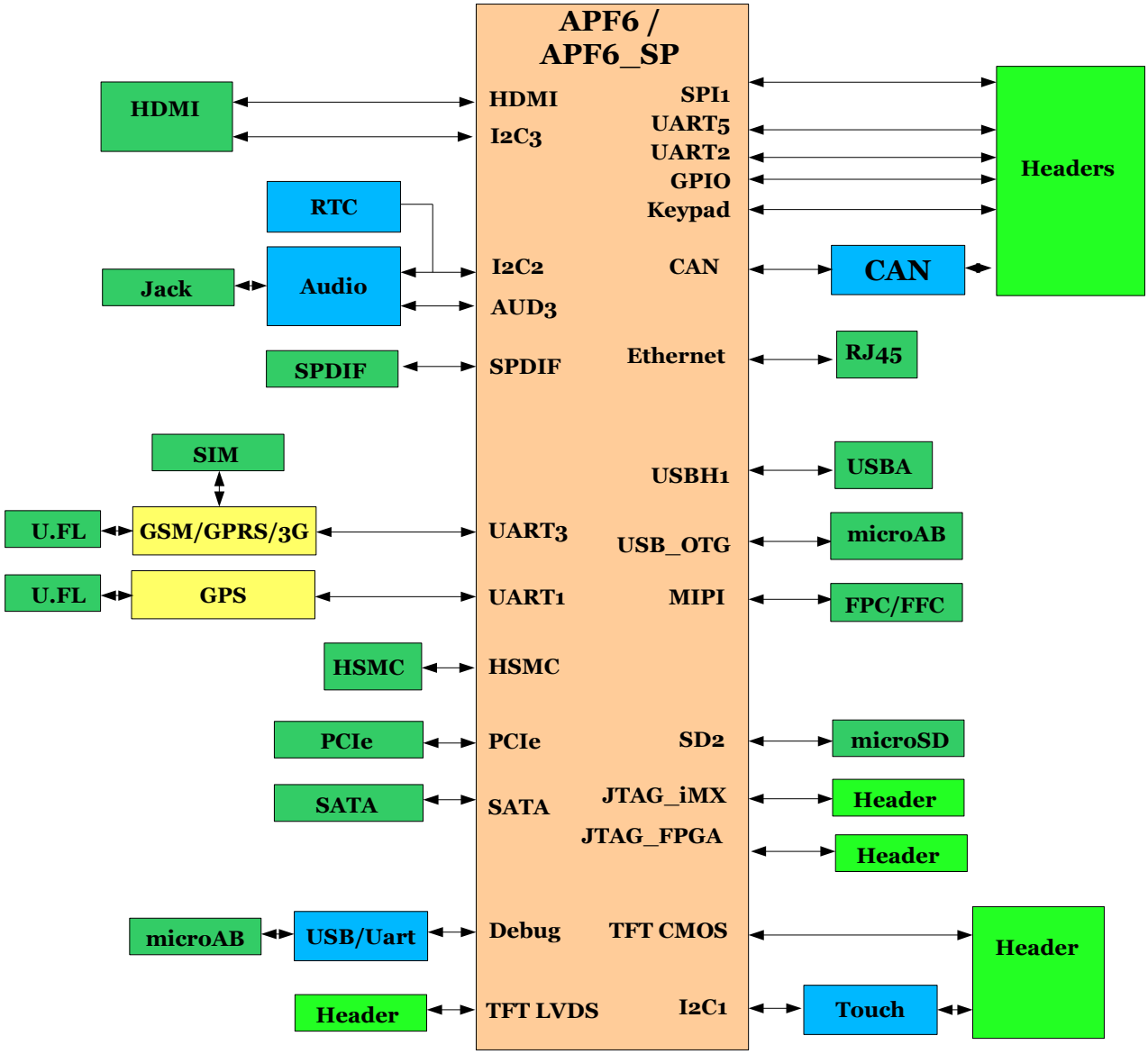
If a TFT has to be connected do not forget to align pin 1 of the TFT connector (**J21**) with pin 1 of the TFT flat cable (red line).

Please consult our wiki for initial setup (http://www.armadeus.com/wiki/index.php?title=Setup).



# 3 - Hardware Description

The following section provides a detailed description of the functions available on the APF6Dev.

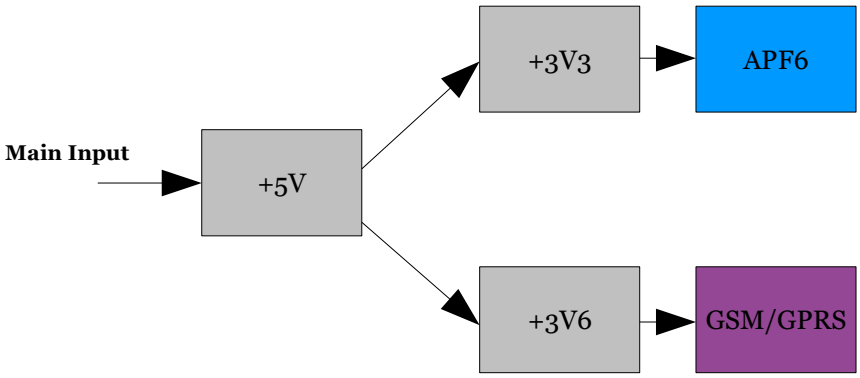



U.FL: Antenna

Wireless option

# 3.1 - Power Supplies

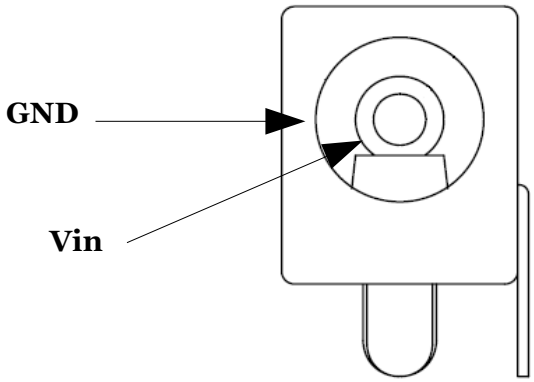
Three supplies are present on the board: +5Vdc, +3.3Vdc and +3.6Vdc.




## 3.1.1 - Main input supply (J29)

This input is protected against over and reverse voltages

- Connector type: 2.5mm mono jack (internal plug: positive supply, external ring: GND)
- Input voltage: 12Vdc 2A max




## 3.1.2 - 5Vdc

This supply is directly generated from the main input supply by means of a DC/DC converter. It is mainly used to power the two USB host ports (500mA each) and the GSM/GPRS supply.

## 3.1.3 - 3.3Vdc

This supply is generated from the local 5Vdc supply and uses a 3A DC/DC converter. The APF6 is powered by this supply.

### 3.1.4 - 3.6Vdc

This supply is generated from the localc 5Vdc supply and uses a 3A DC/DC converter. It is used to power the GSM/GPRS module.

## 3.2 - System LEDs

| LED | Description |
|---|---|
| D18 | 5V supply presence |
| D19 | 3.3V supply presence |

## 3.3 - User LEDs

| LED | Description |
|---|---|
| D6 | FPGA user LED. Directly connected to HSMC_D0/ PIN_M10 ball of the FPGA. A high level will light the LED |
| D30 | i.MX user LED. A high level on GPIO7_12 pin of the i.MX will light the LED |

## 3.4 - User switches

| Switch | Description |
|---|---|
| S1 | FPGA user switch. Directly connected to HSMC_D2 / PIN_L9 ball of the FPGA. An FPGA internal pull up is required. |
| S6 | i.MX user switch. Connected to GPIO1_9 pin of the i.MX. |

## 3.5 - Jumpers

### 3.5.1 - Boot mode jumpers (J31/J32)

These two jumpers are used to select the APF6 boot mode.

By default (normal boot) only BOOT0 (J31) must be mounted. For U-Boot recovery, only BOOT1 (J32) must be mounted.

***Reminder: Do not forget to set again jumper BOOT0 (J31) after U-Boot recovery !***

### 3.5.2 - CAN jumper (J8)

If mounted, a 120 termination is placed between CANH and CANL signals.

## 3.6 - Ethernet 10/100/1000 Mbits (J17)

The Ethernet connector can be used to connect your APF6_Dev to your network.

Two LEDs (orange/green) respectively indicate the presence/activity of the link and the speed of this link.

Connector type: shielded RJ45

## 3.7 - SATA data / SATA power (J10/J13)

Standard SATA devices can be connected to these interfaces.

Connector type: SATA 7 pins

## 3.8 - PCI express (J42)

Standard 1 lane PCI express boards can be connected to this interface. 3.3V and 12V supplies are present on this connector. The interface does not support I2C/Wake signals

Connector type: PCI express 64 pins.

**Remark: this connector can not be used if an APF6SP board is mounted**

## 3.9 - Console/Debug (J4)

The console interface is available through an UART to USB converter (FTDI 231x). Default baud rate is 115200 ( 8bits data, parity none, 1 stop bit and no flow control)

Connector type: USB microAB

Signal level: USB

## 3.10 - TFT CMOS Interface

The LCD interface (24bits data wide) allows connecting to the APF6_Dev board:

- TFT displays
- Resistive touch panels

For compatibility reasons with the previous development kits, only 18bits of the 24bits interface are available on this interface.

### 3.10.1 - Connector (J21)

| Pin | Description | Type | Pin | Description | Type |
|---|---|---|---|---|---|
| 1 | CLK | Output 3.3V | 2 | 3.3V | Power |
| 3 | Not connected | | 4 | 5V | Power |
| 5 | Not connected | | 6 | CONTRAST | Output 3.3V |
| 7 | Not connected | | 8 | DE | Output 3.3V |
| 9 | Not connected | | 10 | HSYNC | Output 3.3V |
| 11 | GND | Bidir | 12 | VSYNC | Output 3.3V |
| 13 | B1 | Output 3.3V | 14 | GND | Power |
| 15 | B3 | Output 3.3V | 16 | B2 | Output 3.3V |
| 17 | B5 | Output 3.3V | 18 | B4 | Output 3.3V |
| 19 | G1 | Output 3.3V | 20 | G0 | Output 3.3V |
| 21 | G3 | Output 3.3V | 22 | G2 | Output 3.3V |
| 23 | G5 | Output 3.3V | 24 | G4 | Output 3.3V |
| 25 | R2 | Output 3.3V | 26 | R1 | Output 3.3V |
| 27 | R4 | Output 3.3V | 28 | R3 | Output 3.3V |
| 29 | R5 | Output 3.3V | 30 | GND | Power |
| 31 | B0 | Output 3.3V | 32 | R0 | Output 3.3V |
| 33 | GND | Power | 34 | GND | Power |
| 35 | NC | | 36 | NC | |
| 37 | Touch X+ | Analog | 38 | Touch Y+ | Analog |
| 39 | Touch X- | Analog | 40 | Touch Y- | Analog |

Connector type: 2.54mm 30 pin dual rows

# 3.11 - TFT LVDS connector (J2)

A LVDS TFT display can be connected to this interface. An I2C bus and 2 GPios are although present on this connector for touch panel support.

## 3.11.1 - connector (J2)

| Pin | Description | Type | Pin | Description | Type |
|---|---|---|---|---|---|
| 1 | GND | Power | 2 | GND | Power |
| 3 | DISP_TX0P | LVDS 3.3V | 4 | DISP_TX0N | LVDS 3.3V |
| 5 | GND | Power | 6 | GND | Power |
| 7 | DISP_TX1P | LVDS 3.3V | 8 | DISP_TX1N | LVDS 3.3V |
| 9 | GND | Power | 10 | GND | Power |
| 11 | DISP_TX2P | LVDS 3.3V | 12 | DISP_TX2N | LVDS 3.3V |
| 13 | GND | Power | 14 | GND | Power |
| 15 | DISP_TX3P | LVDS 3.3V | 16 | DISP_TX3N | LVDS 3.3V |
| 17 | GND | Power | 18 | GND | Power |
| 19 | DISP_CLKP | LVDS 3.3V | 20 | DISP_CLKN | LVDS 3.3V |
| 21 | GND | Power | 22 | GND | Power |
| 23 | I2C1_SCL | iMX6 I2C1 clock output (3.3Vdc) | 24 | I2C1_SCL | iMX6 I2C1 data line (3.3Vdc) |
| 25 | GPIO5_21 | iMX6 GPIO 5_21 (3.3Vdc) | 26 | GPIO5_18 | iMX6 GPIO 5_18 (3.3Vdc) |
| 27 | +12V | Power | 28 | +12V | Power |
| 29 | +5V | Power | 30 | +5V | Power |
| 31 | +3V3 | Power | 32 | +3V3 | Power |
| 33 | GND | Power | 34 | GND | Power |

Connector type: 2.54mm 30 pin dual rows

# 3.12 - microSD (J6)

A standard microSD card can be connected to the APF6Dev providing additional storage capacity.

Connector type: Hirose DM3ATxxx

# 3.13 - Audio In / Audio Out (J23)

A complete audio stereo codec (Freescake SGTL5000) is present on the APF6Dev board providing a stereo HP output and one microphone input.

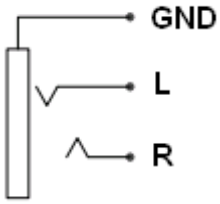
A synchronous serial interface (SSI) is used to exchange the audio data between the codec and the i.MX. The configuration of the SGTL5000 is done through the I2C2 interface.

Details concerning the SGTL5000 can be found in the References Chapter

## 3.13.1 - HP Audio Connector (J23 up)

Connector type: 3.5mm stereo jack

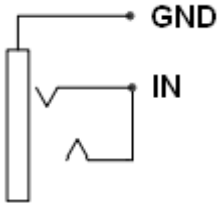
Signal level for headset output: 0.8Vrms full scale, 1.5V output common mode




## 3.13.2 - Microphone Audio Connector (J23 down)

Connector type: 3.5mm stereo jack

Signal level for headset input: 0.7Vrms full scale, 1.5V output common mode




# 3.14 - SPDIF Output (U16)

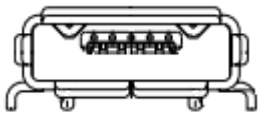
A standard SPIDF output is available on U16.

## 3.15 - USB Hosts Interfaces (J22)

One high speed USB host interface is available.

Connector type: dual USB A

Signal level: USB



## 3.16 - USB OTG Interface (J1)

One high speed USB OTG interface is available through **J1**.

Connector type: USB microAB

Signal level: USB

## 3.17 - HDMI Interface (J15)

One HDMI interface is available through **J15**. This interface is directly connected to the APF6 HDMI output.

Connector type: HDMI

## 3.18 - CAN

The CAN 2.0 controller of the APF6 is connected to a CAN transceiver (MCP2551) which converts the CMOS signals of the iMX6 into CAN differential signals.

A 120 ohms termination between CANH and CANL can be enabled by mounting **J8**.

Can signals are available on **J18**

## 3.19 - RTC

A RTC is present on the APF6_Dev boad. This RTC (MCP79400) is connected on the I2C2 bus of the APF6.

RTC backup can be done by connecting a battery cell to **J3** (Pin 1: VCC, Pin 2: GND)

# 3.20 - GSM/GPRS/3G U2 (optional)

An optional GSM/GPRS/3G module (Sagem Hilo series) can be connected to the APF6_Dev.

The communication with the module is done through the APF6 UART3 interface.

A SIM card support is although located on the APF6_Dev.

## 3.20.1 - Characteristics

Frequency bands: GSM850, EGSM900, DCS1800, PCS1900 and UMTS 900/1900/2100 (3G only)

Voice codec: Half rate, full rate, enhanced full rate, adaptative multi rate

Transmit power:

Class 4 (2W) for GSM850 / EGSM900

Class 1 (1W) for DCS 1800 / PCS 1900

Class E2 EDGE 900 / 1800 (3G only)

Class 3 for UMTS 900/1900/2100 (3G only)

SIM: ISO7816-3 card support

Data / Command multiplexing: GSM 07.10 standard with AT_Command

Data services: GPRS, CSD, Fax. HSDPA and EDGE for 3G module

GPRS: SMG 31bis, multi slot class 10, class B terminal, PBCCH support

EDGE: multi slot class 12 (3G only)

UMTS/HSDPA: class E2, voice and data in parallel for UMTS/HSDPA, 4 logical channels (3G only)

HSPDA: 3.6Mbps (3G only)

## 3.20.2 - Interfaces

UART: TX, RX, CTS, RTS 115200 bps and 921600 bps for 3G module

SIM: support 1.8 and 3V sim cards

## 3.20.3 - Antenna

An U.FL connector allows connecting an external antenna. Take care about the frequency range when choosing the external antenna. **Do not place the GSM/GPRS antenna near the GPS one !**

# 3.21 - GPS (optional)

An optional GPS module from U-Blox (or equivalent, NEO 5/6 model) can be mounted.

The communication with this module is done through the APF6 UART1.

## 3.21.1 - Characteristics

- 50-channel with over 1 million effective correlators
- <1 second Time To First Fix for Hot and Aided starts
- -160dBm Supersense acquisition and tracking sensitivity
- Cold start: 32s
- Horizontal position accuracy: < 2.5m
- A-GPS, NMEA and UBX support
- High immunity to jamming
- 4Hz position update rate
- GPS sleep

## 3.21.2 - Interfaces

UART: TX, RX 38400 bps

## 3.21.3 - Antenna (J25)

An U.FL connector allows connecting an external antenna. **Do not place the GPS antenna near the GSM one !**

# 3.22 - CMOS Sensor Interface (J12)

This interface can be used to connect a standard MIPI CMOS sensor for image acquisition. Usually an adapter board/cable will be required.

Communication with the CMOS sensor is done through the I2C2 interface while image data are transferred on a dedicated bus (MIPI).

| Pin | Description | Type |
|---|---|---|
| 1 | CSI_CLKoP | MIPI CLKP line |
| 2 | CSI_CLKoM | MIPI CLKN line |
| 3 | GND | Power |
| 4 | CSI_DoP | MIPI D1P line |
| 5 | CSI_DoM | MIPI D1N line |

| | | |
|---|---|---|
| 6 | GND | Power |
| 7 | CSI_D1P | MIPI D1P line |
| 8 | CSI_D1M | MIPI D1N line |
| 9 | GND | Power |
| 10 | CSI_D2P | MIPI D2P line |
| 11 | CSI_D2M | MIPI D2N line |
| 12 | GND | Power |
| 13 | CSI_D3P | MIPI D3P line |
| 14 | CSI_D3M | MIPI D3N line |
| 15 | GND | Power |
| 16 | NC | Not connected |
| 17 | NC | Not connected |
| 18 | GND | Power |
| 19 | NC | Not connected |
| 20 | NC | Not connected |
| 21 | GND | Power |
| 22 | NC | Not connected |
| 23 | NC | Not connected |
| 24 | GND | Power |
| 25 | I2C1_SCL | iMX6 I2C clock. 3.3Vdc |
| 26 | I2C2_SDA | iMX6 I2C data line. 3.3Vdc |
| 27 | +3V3 | Power |
| 28 | +3V3 | Power |
| 29 | CSI_MCLK | Clock output. 3.3Vdc |
| 30 | GPIO5_20 | iMX6 gpio5_20. 3.3Vdc |
| 31 | GPIO5_19 | iMX6 gpio5_19. 3.3Vdc |
| 32 | +5V | Power |
| 33 | +5V | Power |

Connector type:  FPC/FFC 33pin 0.5mm pitch Top/bottom contacts

Signal levels:  MIPI standard levels and 3.3V level for other signals

# 3.23 -  JTAG iMX (J36)

A standard JTAG connector is available for debug purpose of the iMX processor.

This connector is compatible with most of the JTAG debugger

| Pin | Description | Type | Pin | Description | Type |
|---|---|---|---|---|---|
| 1 | JTAG_VREF | Power (3.3Vdc) | 2 | +3V3 | Power |
| 3 | JTAG_TRSTB | Input 3.3Vdc | 4 | GND | Power |
| 5 | JTAG_TDI | Input 3.3Vdc | 6 | GND | Power |
| 7 | JTAG_TMS | Input 3.3Vdc | 8 | GND | Power |
| 9 | JTAG_TCK | Input 3.3Vdc | 10 | GND | Power |
| 11 | Not connected | | 12 | GND | Power |
| 13 | JTAG_TDO | Output 3.3Vdc | 14 | GND | Power |
| 15 | RESET# | Bidirectional | 16 | GND | Power |
| 17 | Not connected | | 18 | GND | Power |
| 19 | Not connected | | 20 | GND | Power |

Connector type: 2.54mm 20 pin  dual row header

Signal levels: 3.3Vdc

# 3.24 -  Extension1 (J18)

This connector is foreseen for APF6_Dev extensions and can be used for rapid prototyping of specific products.

| Pin | Description | Type | Pin | Description | Type |
|---|---|---|---|---|---|
| 1 | +3V3 | Power | 2 | +3V3 | Power |
| 3 | UART3_TX | GPIO (3.3V)* | 4 | UART3_RX | GPIO (3.3V)* |
| 5 | UART3_CTS | GPIO (3.3V)* | 6 | UART3_RTS | GPIO (3.3V)* |
| 7 | GPIO5_12 (DISP0_DAT18) | GPIO (3.3V)* | 8 | GPIO5_13 (DISP0_DAT19) | GPIO (3.3V)* |

| | | | | | |
|---|---|---|---|---|---|
| 9 | GPIO5_14 (DISP0_DAT20) | GPIO (3.3V)* | 10 | GPIO5_15 (DISP0_DAT21) | GPIO (3.3V)* |
| 11 | GPIO5_16 (DISP0_DAT22) | GPIO (3.3V)* | 12 | GPIO5_17 (DISP0_DAT23) | GPIO (3.3V)* |
| 13 | GPIO5_18** (CSI0_PIXCLK) | GPIO (3.3V)* | 14 | GPIO5_19* (CSI0_MCLK) | GPIO (3.3V)* |
| 15 | GPIO5_20* (CSI0_DATA_EN) | GPIO (3.3V)* | 16 | GPIO5_21** (CSI0_VSYNC) | GPIO (3.3V)* |
| 17 | CANL | CAN differential pair | 18 | CANH | CAN differential pair |
| 19 | GND | Power | 20 | GND | Power |

available although on J22
available although on J2
*multiplexed GPIO. See APF6 datasheet J3/J4 connector definitions for multiplexing details

Connector type: 2.54mm 20 pin dual row header

# 3.25 - Extension2 (J5)

This connector is foreseen for APF6_Dev extensions and can be used for rapid prototyping of specific products.

| Pin | Description | Type | Pin | Description | Type |
|---|---|---|---|---|---|
| 1 | +3V3 | Power | 2 | +3V3 | Power |
| 3 | I2C1_SDA | iMX6 I2C1 data line (3.3V) | 4 | I2C1_SCL | iMX6 I2C1 clock line (3.3V) |
| 5 | SPI1_SCLK | GPIO (3.3V)* | 6 | SPI1_MISO | GPIO (3.3V)* |
| 7 | SPI1_SS1 | GPIO (3.3V)* | 8 | SPI1_SS2 | GPIO (3.3V)* |
| 9 | SPI1_SS0 | GPIO (3.3V)* | 10 | SPI1_MOSI | GPIO (3.3V)* |
| 11 | GPIO7_11 | GPIO (3.3V)* | 12 | GPIO4_20 (DI0_PIN4) | GPIO (3.3V)* |
| 13 | UART2_TX | GPIO (3.3V)* | 14 | UART2_RX | GPIO (3.3V)* |
| 15 | UART5_CTS | GPIO (3.3V)* | 16 | UART5_RTS | GPIO (3.3V)* |
| 17 | UART5_RX | GPIO (3.3V)* | 18 | UART5_TX | GPIO (3.3V)* |
| 19 | GND | Power | 20 | GND | Power |

*multiplexed GPIO. See APF6 datasheet J3/J4 connectors definitions for multiplexing details

Connector type: 2.54mm 20 pin dual row header

# 3.26 - JTAG FPGA (J14)

A JTAG connector is available for debug purpose of the FPGA on the APF6_SP_Dev boards.

This connector is compatible with Altera USB blaster

| Pin | Description | Type | Pin | Description | Type |
|---|---|---|---|---|---|
| 1 | JTAG_TCK | Input 3.3Vdc | 2 | GND | Power |
| 3 | JTAG_TDO | Output 3.3Vdc | 4 | +3V3 | Power |
| 5 | JTAG_TMS | Input 3.3Vdc | 6 | nc | |
| 7 | nc | | 8 | nc | |
| 9 | JTAG_TDI | Input 3.3Vdc | 10 | GND | Power |

Connector type: 2.54mm 10 pin dual row header

Signal levels: 3.3Vdc

# 3.27 - HSMC (J19)

This connector is only available on the APF6_SP_Dev boards and is compatible with the Altera HSMC standard.

Complete HSMC standard can be found here: www.altera.com/literature/ds/hsmc_spec.pdf

| Pin | Function | FPGA pin | Pin | Function | FPGA pin | Description |
|---|---|---|---|---|---|---|
| 1 | nc | | 2 | nc | | |
| 3 | nc | | 4 | nc | | |
| 5 | nc | | 6 | nc | | |
| 7 | nc | | 8 | nc | | |
| 9 | nc | | 10 | nc | | |
| 11 | nc | | 12 | nc | | |
| 13 | nc | | 14 | nc | | |
| 15 | nc | | 16 | nc | | |
| 17 | nc | | 18 | nc | | |
| 19 | nc | | 20 | nc | | |
| 21 | XCVR_TXP2 | J2 | 22 | XCVR_RXP2 | L2 | Transceiver |
| 23 | XCVR_TXN2 | J1 | 24 | XCVR_RXN2 | L1 | Transceiver |

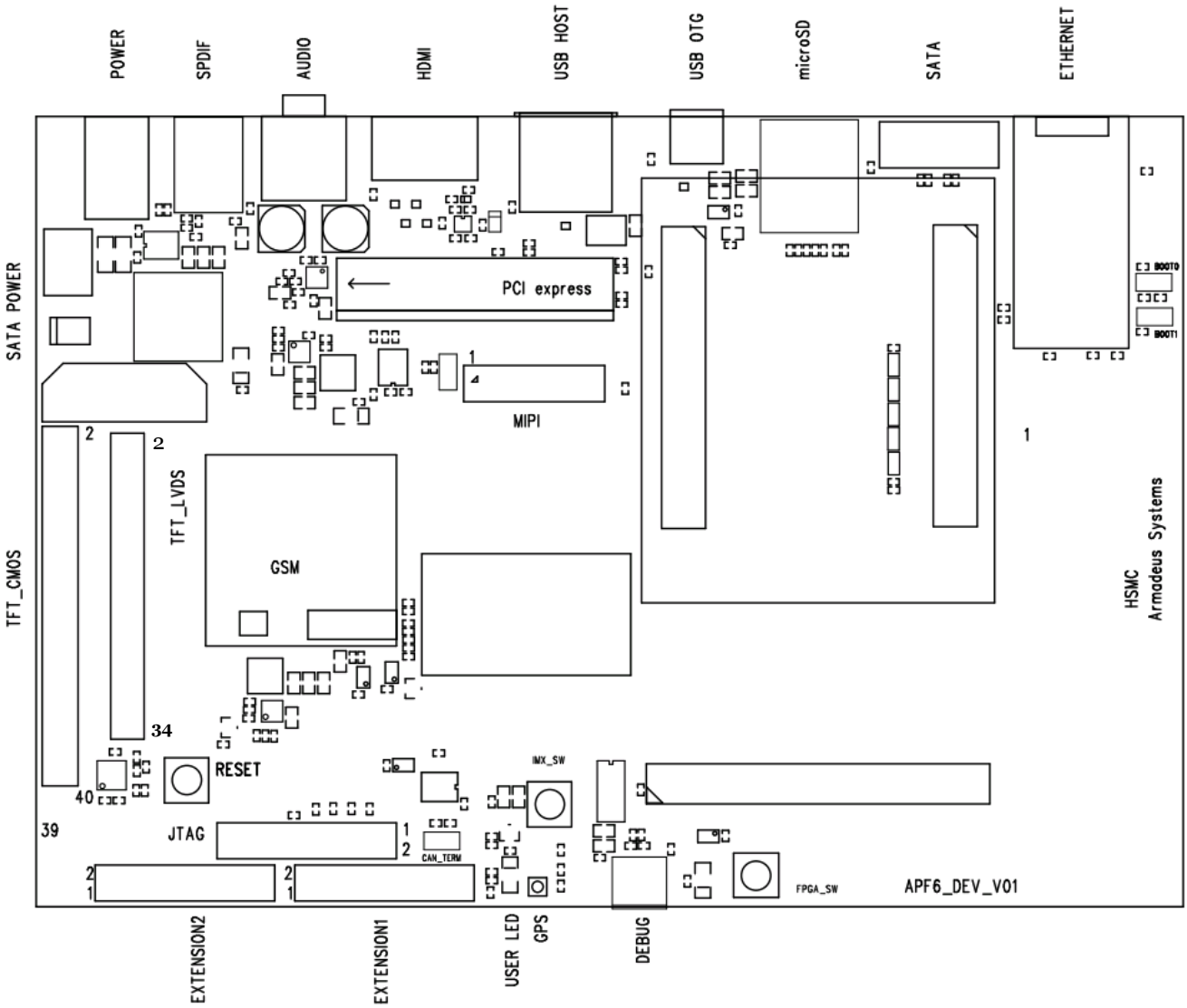
| | | | | | | |
|---|---|---|---|---|---|---|
| 25 | XCVR_TXP1 | N2 | 26 | XCVR_RXP1 | R2 | Transceiver |
| 27 | XCVR_TXN1 | N1 | 28 | XCVR_RXN1 | R1 | Transceiver |
| 29 | XCVR_TXP0 | U2 | 30 | XCVR_RXP0 | W2 | Transceiver |
| 31 | XCVR_TXN0 | U1 | 32 | XCVR_RXN0 | W1 | Transceiver |
| 33 | nc | | 34 | nc | | |
| 35 | nc | | 36 | nc | | |
| 37 | nc | | 38 | nc | | |
| 39 | CLKOUT0 | R10 | 40 | CLKIN0 | T10 | CMOS CLK |
| 41 | D0 | M10 | 42 | D1 | K15 | CMOS |
| 43 | D2 | L9 | 44 | D3 | L15 | CMOS |
| 45 | 3.3V | | 46 | 12V | | |
| 47 | LVDS_TX_P0 | Y11 | 48 | LVDS_RX_P0 | Y9 | CMOS/LVDS |
| 49 | LVDS_TX_N0 | W11 | 50 | LVDS_RX_N0 | AA9 | CMOS/LVDS |
| 51 | 3.3V | | 52 | 12V | | |
| 53 | LVDS_TX_P1 | T13 | 54 | LVDS_RX_P1 | U11 | CMOS/LVDS |
| 55 | LVDS_TX_N1 | R12 | 56 | LVDS_RX_N1 | U10 | CMOS/LVDS |
| 57 | 3.3V | | 58 | 12V | | |
| 59 | LVDS_TX_P2 | AB13 | 60 | LVDS_RX_P2 | V9 | CMOS/LVDS |
| 61 | LVDS_TX_N2 | AA13 | 62 | LVDS_RX_N2 | U8 | CMOS/LVDS |
| 63 | 3.3V | | 64 | 12V | | |
| 65 | LVDS_TX_P3 | AB11 | 66 | LVDS_RX_P3 | T12 | CMOS/LVDS |
| 67 | LVDS_TX_N3 | AB10 | 68 | LVDS_RX_N3 | U12 | CMOS/LVDS |
| 69 | 3.3V | | 70 | 12V | | |
| 71 | LVDS_TX_P4 | AA10 | 72 | LVDS_RX_P4 | V13 | CMOS/LVDS |
| 73 | LVDS_TX_N4 | Y10 | 74 | LVDS_RX_N4 | W13 | CMOS/LVDS |
| 75 | 3.3V | | 76 | 12V | | |
| 77 | LVDS_TX_P5 | Y15 | 78 | LVDS_RX_P5 | Y12 | CMOS/LVDS |
| 79 | LVDS_TX_N5 | AA15 | 80 | LVDS_RX_N5 | W12 | CMOS/LVDS |

| | | | | | | |
|---|---|---|---|---|---|---|
| 81 | 3.3V | | 82 | 12V | | |
| 83 | LVDS_TX_P6 | AB16 | 84 | LVDS_RX_P6 | W14 | CMOS/LVDS |
| 85 | LVDS_TX_N6 | AB15 | 86 | LVDS_RX_N6 | Y14 | CMOS/LVDS |
| 87 | 3.3V | | 88 | 12V | | |
| 89 | LVDS_TX_P7 | P12 | 90 | LVDS_RX_P7 | U17 | CMOS/LVDS |
| 91 | LVDS_TX_N7 | R11 | 92 | LVDS_RX_N7 | U16 | CMOS/LVDS |
| 93 | 3.3V | | 94 | 12V | | |
| 95 | CLKOUT_1P | G18 | 96 | CLKIN_1P | P9 | LVDS CLKp/CMOS |
| 97 | CLKOUT_1N | G17 | 98 | CLKIN_1N | R9 | LVDS CLKn/CMOS |
| 99 | 3.3V | | 100 | 12V | | |
| 101 | LVDS_TX_P8 | AB17 | 102 | LVDS_RX_P8 | Y17 | CMOS/LVDS |
| 103 | LVDS_TX_N8 | AA17 | 104 | LVDS_RX_N8 | Y16 | CMOS/LVDS |
| 105 | 3.3V | | 106 | 12V | | |
| 107 | LVDS_TX_P9 | AA18 | 108 | LVDS_RX_P9 | W17 | CMOS/LVDS |
| 109 | LVDS_TX_N9 | AB18 | 110 | LVDS_RX_N9 | W16 | CMOS/LVDS |
| 111 | 3.3V | | 112 | 12V | | |
| 113 | LVDS_TX_P10 | Y19 | 114 | LVDS_RX_P10 | W18 | CMOS/LVDS |
| 115 | LVDS_TX_N10 | AA19 | 116 | LVDS_RX_N10 | V18 | CMOS/LVDS |
| 117 | 3.3V | | 118 | 12V | | |
| 119 | LVDS_TX_P11 | R20 | 120 | LVDS_RX_P11 | V20 | CMOS/LVDS |
| 121 | LVDS_TX_N11 | R21 | 122 | LVDS_RX_N11 | V19 | CMOS/LVDS |
| 123 | 3.3V | | 124 | 12V | | |
| 125 | LVDS_TX_P12 | AB21 | 126 | LVDS_RX_P12 | T17 | CMOS/LVDS |
| 127 | LVDS_TX_N12 | AB20 | 128 | LVDS_RX_N12 | T18 | CMOS/LVDS |
| 129 | 3.3V | | 130 | 12V | | |
| 131 | LVDS_TX_P13 | Y20 | 132 | LVDS_RX_P13 | J17 | CMOS/LVDS |
| 133 | LVDS_TX_N13 | AA20 | 134 | LVDS_RX_N13 | J18 | CMOS/LVDS |
| 135 | 3.3V | | 136 | 12V | | |

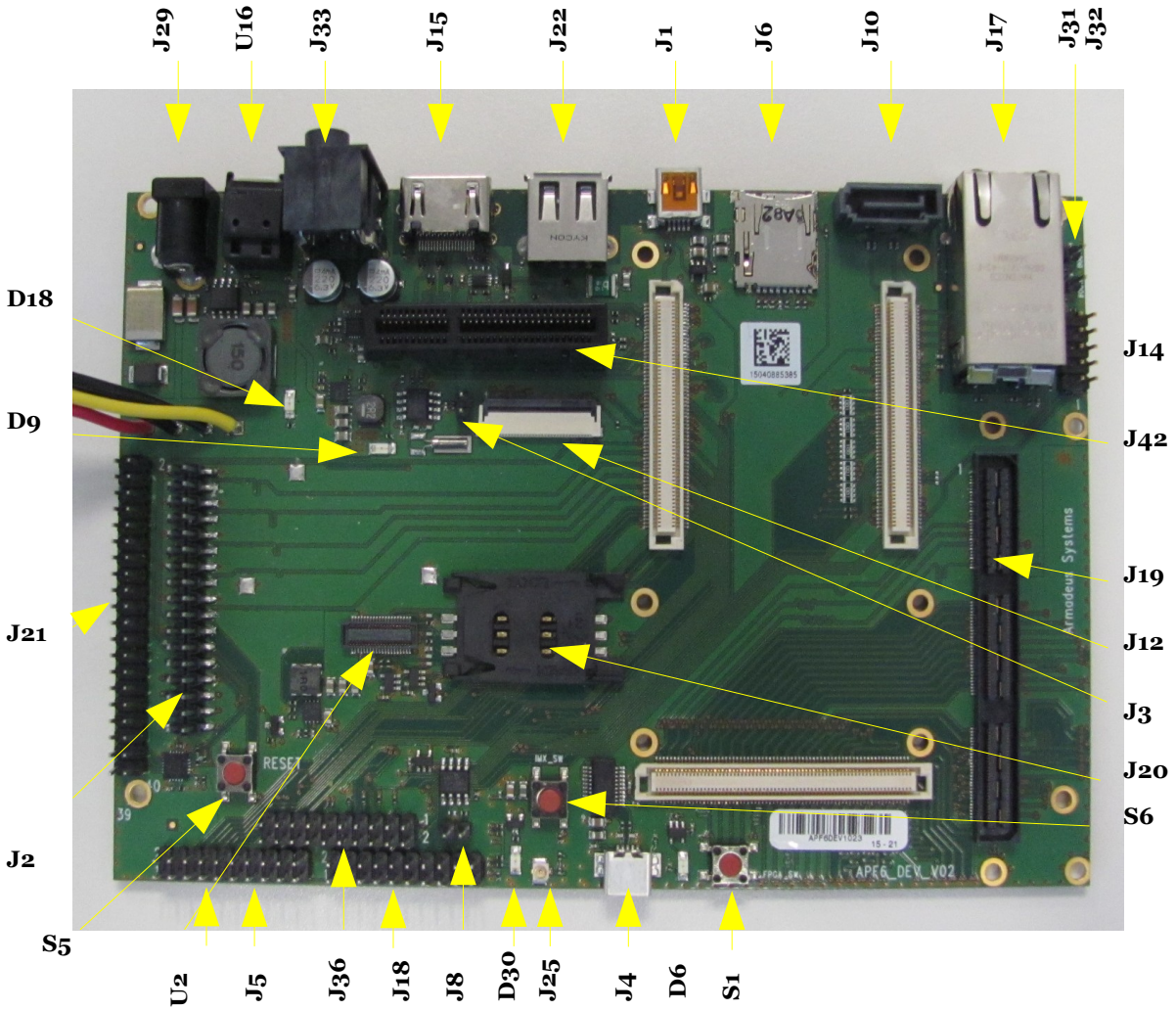
| | | | | | | |
|---|---|---|---|---|---|---|
| 137 | LVDS_TX_P14 | U22 | 138 | LVDS_RX_P14 | L18 | CMOS/LVDS |
| 139 | LVDS_TX_N14 | U21 | 140 | LVDS_RX_N14 | K19 | CMOS/LVDS |
| 141 | 3.3V | | 142 | 12V | | |
| 143 | LVDS_TX_P15 | T22 | 144 | LVDS_RX_P15 | L19 | CMOS/LVDS |
| 145 | LVDS_TX_N15 | R22 | 146 | LVDS_RX_N15 | L20 | CMOS/LVDS |
| 147 | 3.3V | | 148 | 12V | | |
| 149 | LVDS_TX_P16 | G22 | 150 | LVDS_RX_P16 | R19 | CMOS/LVDS |
| 151 | LVDS_TX_N16 | G21 | 152 | LVDS_RX_N16 | P19 | CMOS/LVDS |
| 153 | 3.3V | | 154 | 12V | | |
| 155 | CLKOUT_2P | AA22 | 156 | CLKIN_2P | T15 | LVDS CLKp/CMOS |
| 157 | CLKOUT_2N | AB22 | 158 | CLKIN_2N | R15 | LVDS CLKn/CMOS |
| 159 | 3.3V | | 160 | GND | | |

# 4 - Mechanical and Assembly drawing

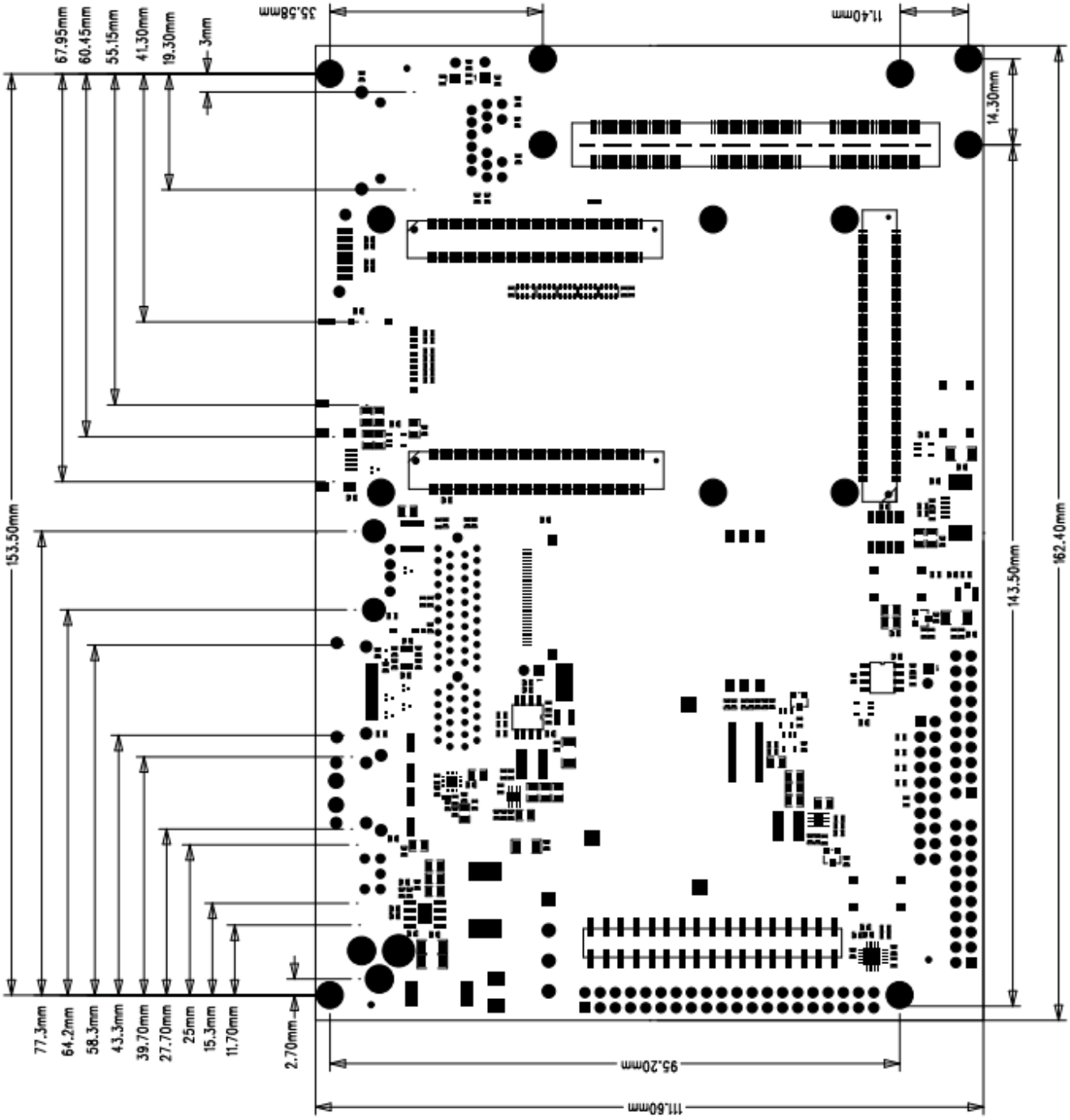
## 4.1 - Top Assembly



# 4.2 - Connectors and jumpers



# 4.3 - Mechanical



# 5 - Web Link

Armadeus Systems general documentation: http://www.armadeus.org

APF6_Dev wiki page: http://www.armadeus.com/wiki/index.php?title=APF6_Dev

APF6 wiki page: http://www.armadeus.com/wiki/index.php?title=APF6

# 6 - Component Link

**MCP2551**: http://ww1.microchip.com/downloads/en/DeviceDoc/21667f.pdf

**MCP79400:** http://ww1.microchip.com/downloads/en/DeviceDoc/20005009D.pdf

**SGTL5000**: http://cache.freescale.com/files/analog/doc/data_sheet/SGTL5000.pdf

**Hilo2**: http://support.sagemcom.com/site/modele_fax.php?page=spec_gen&prd=HiloV2&pays=uk

**Hilo3G**: http://support.sagemcom.com/site/modele_fax.php?page=spec_gen&prd=Hilo3g&pays=uk

**Neo6**: http://www.ublox.com/images/downloads/Product_Docs/NEO-6_DataSheet_%28GPS.G6-HW-09005%29.pdf