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APF51DEV

APF51DEV DATASHEET

V0.D

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Table of Contents

Edition	*Date*	*Changes*
Edition 0.A (PCB ed 1)	28. January 2011	Initial version
Edition 0.B (PCB ed 1.1)	8. March 2011	Fix after review
Edition 0.C (PCB ed 1.1)	18. March 2011	OTG and debug connectors are miniB type
Edition 0.D (PCB ed 1.1)	'17. October 2011	Add "Quick start"and Connectors chapters.

1 - APF51Dev Overview

1.1 - Introduction

The APF51Dev is a full featured development board dedicated to the APF51single board computer.

This board offers access to the whole functionalities of the APF51 and provides several additional features. Its price and its connectors make it ideal for rapid development of embedded applications.

1.2 - APF51Dev Features

Input Power supply (restricted	5 to 28 Vdc or lithium-Ion/Polymer for mobile applications fonctionnalities)
On board regulators	5V / 2,5A max high efficiency DC/DC converter
	3.1V / 1,5A max high efficiency DC/DC converter for industrial applications
	3.1V/1,5A max high efficiency DC/DC converter for mobile applications
High speed USB HOST 2.0	2 ports
USB OTG 2.0	1 port
Debug interface	USB miniB port. USB to serial converter present on the board
Ethernet	10/100Mbits autoMDX with LEDs
TFT	CMOS interface.
Touchscreen	4/5 wire resistive touch panel
Stereo Audio In/Out Controller	Headset stereo audio in/out
RTC with backup battery	lithium Cell CR2032
MicroSD	1 port
RS232	1 port (TX/RX/CTS/RTS)
CAN Controller	CAN 2.0b
ADC	8 x 12 bits SPI ADC (300ksps)
DAC	2 x 10bits DAC (5us settling time)
HDMI	HDMI 1.2a, up to 1080i
WiFi	b/g. SDIO interface.
Bluetooth	2.0 EDR. External antenna required
GPIOs	up to 64 gpios (through FPGA)
GSM/GPRS/3G connector	**Optional**. External antenna required. On boad SIM card
GPS	**Optional**. External antenna required
HMS Anybus CompactCom ControlNet, EtherNet/IP, Modbus-TCP,	**Optional**. BACnet MSTP, CANopen, CC-Link, compoNet, DeviceNet, Modbus-RTU, Profibus, EtherCat, Profinet-IO, Sercos III
HMS Anybus-M or -S	**Optional**.
	-M: AS-Interface, DeviceNet, Profibus DPV1, EtherNet/IP.
	-S: CANopen, CC-Link, ControlNet, DeviceNet, FIPIO, Interbus, Fiber Optic, Lonworks, Modbus Plus, Modbus-RTU, Profibus-DP, Profibus-DPV1, EthertCAT, EtherNet/IP, FL-NET, Modbus-TCP, Profinet-IO, Profinet-IRTx
Standard Connectors	Jack 2.5mm for power supply
	2x high speed USB host 2.0 (type A)
	1x OTG high speeed USB (miniB)
	1x USB miniB for debug (serial emulation)
	RS232 DSub 9pts (i.MX UART1)
	10/100Mbits Ethernet (RJ45) with integrated isolation transformer and LEDs
	HDMI
	dual 3,5mm stereo jack for audio in and out
	microSD
Specific connectors	LCD interface including touchscreen (2.54mm header)
	CAN (2.54mm header)
	ADC/DAC (2.54mm header)
	FPGA signals (2.54mm header)
	CMOS Sensor (FPC/FFC 26pin)
	WiFi antenna connector (Hirose U.FL)

	Bluetooth antenna connector (Hirose U.FL) GPS antenna connector (Hirose U.FL) GSM/GPRS/3G connector SIM card socket Keypad (2.54mm header) JTAG (2.54mm header) HMS Anybus ((2mm female embase) HMS CompactCOM (compact flash connector)
User LEDs	2xone connected to the i.MX and the other to the FPGA
User switches	2x one connected to the i.MX and the other to the FPGA
Reset	Switch
On/off	Switch

1.3 - Handling precautions

Please ensure that should a board need to be returned to Armadeus systems, it is adequately packed, preferably in the original packing material.

2 - Quick Start

At first an APF51 module needs to be plugged on J5.

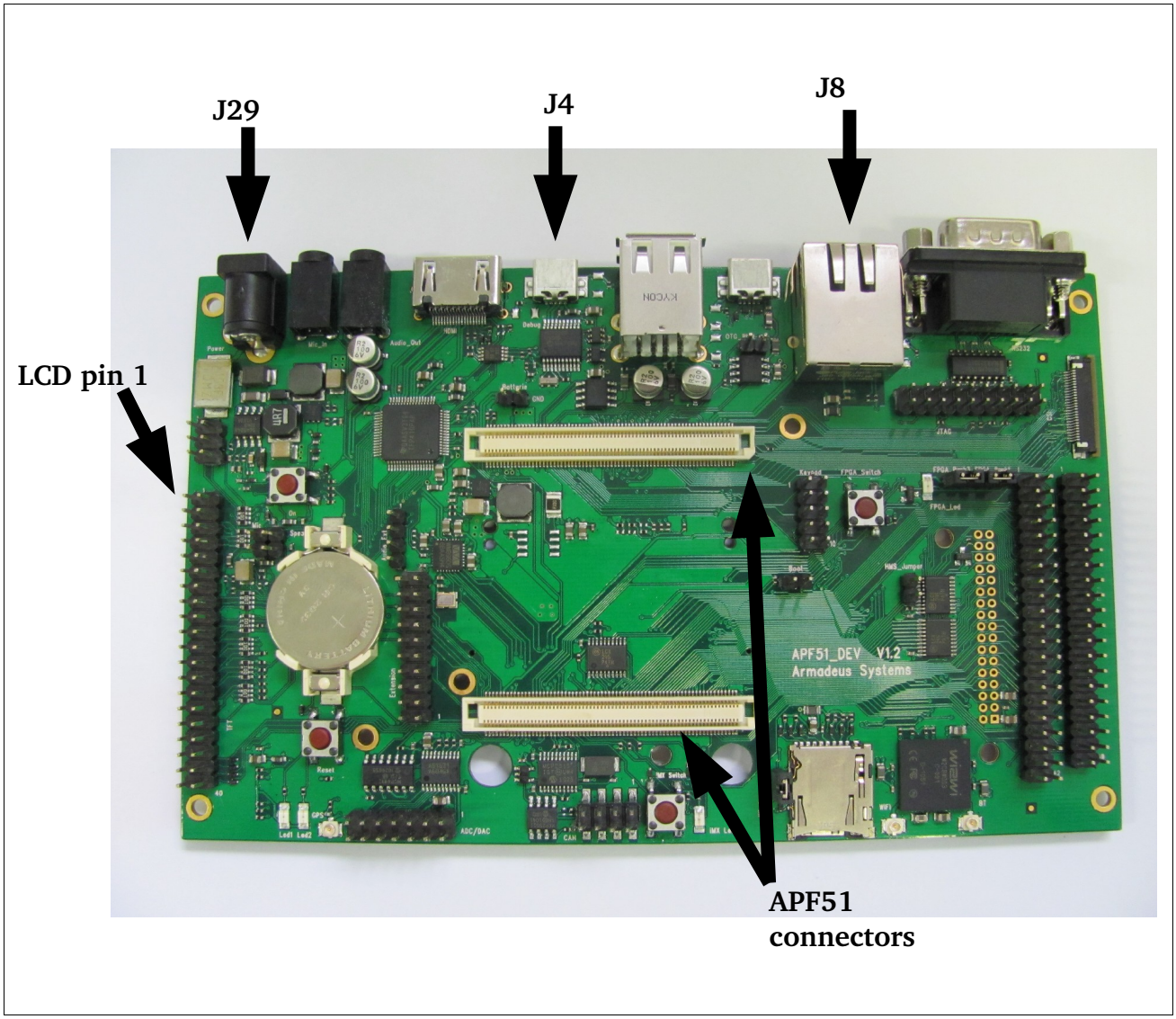
Once done, a power supply has to be connected to J29. The main characteristics of this input supply can be found in the section 3.1.1 below.

An micro-USB AB cable has to be connected between your PC and the micro USB connector (J4) of the board to get access to the debug console. See section 3.9 for details of the serial communication settings.

Ethernet cable can be connected to J8.

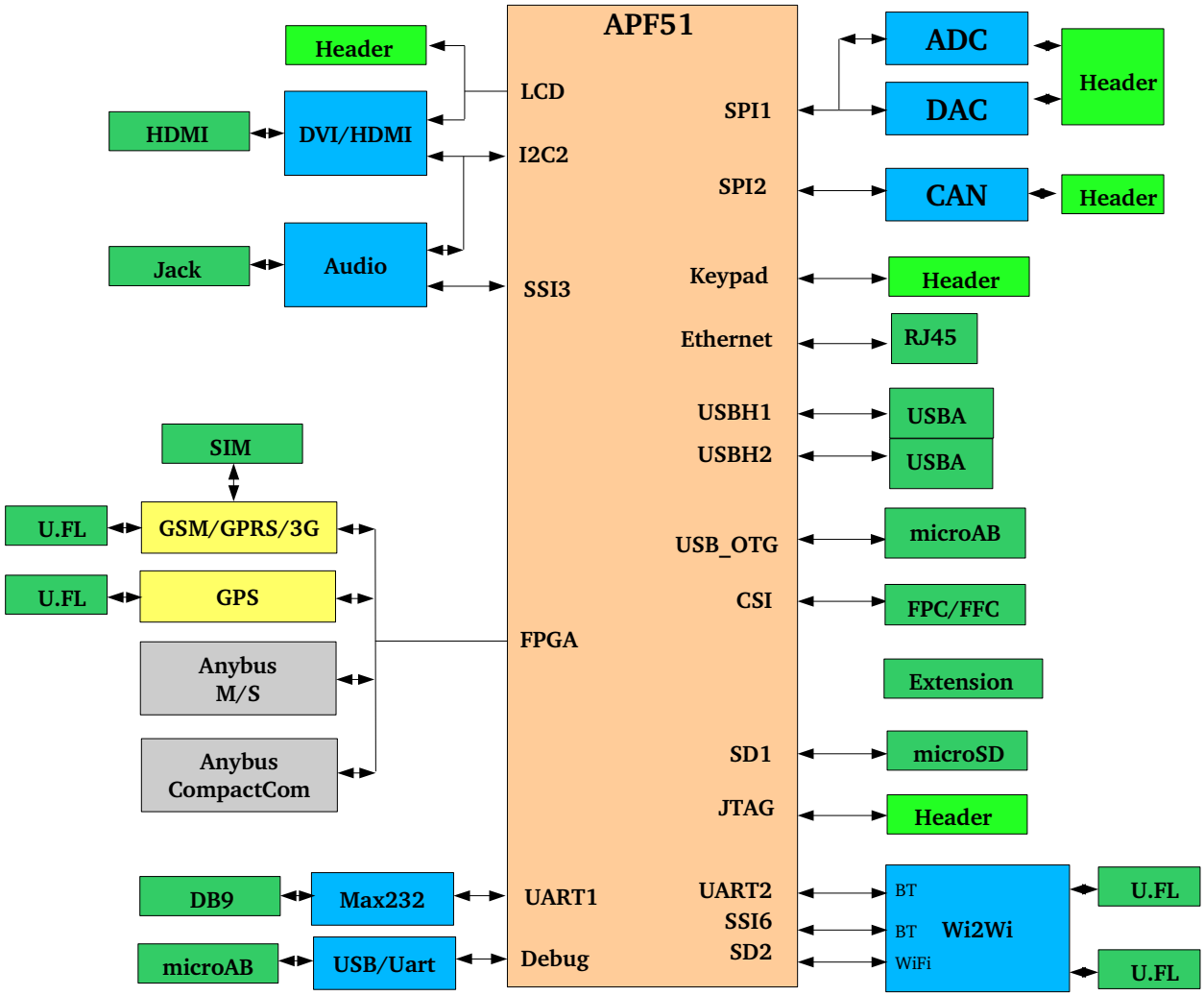
If a LCD has to be connected do not forget to align pin 1 of the LCD connector (J2) with pin 1 of the LCD flat cable (red line).

Please consult our wiki for initial setup (http://www.armadeus.com/wiki/index.php?title=Setup) and section Erreur : source de la référence non trouvée for details about the connectors/jumpers.



3 - Hardware Description

The following section provides a detailed description of the functions available on the APF51Dev.



U.FL: Antenna

Wireless option

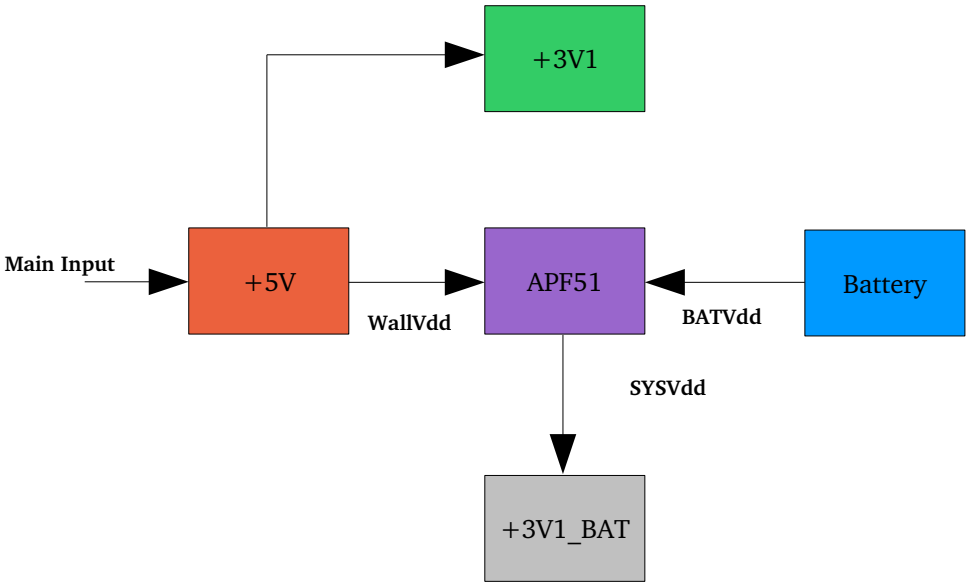
Anybus option

3.1 - Power Supplies

Three supplies are present on the board: +5V, +3V1 and +3V1_BAT. The +3V1_BAT is generated by either the +5V or by an external battery for mobile applications. The arbitration is automatically performed by the APF51 PMIC.

It has to be noted that up to 5W are reserved for the two USB ports.

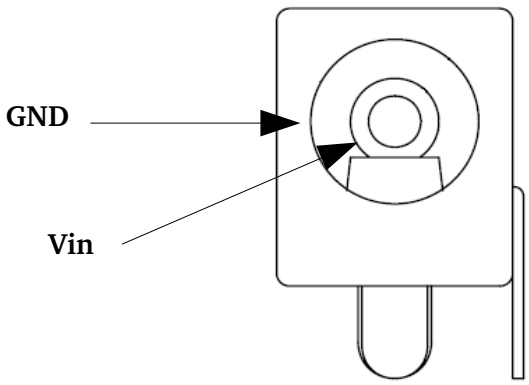
Care must be taken not to overpass the power supply limits !!



3.1.1 - Main input supply (J29)

This input is protected against over and reverse voltages

- Connector type: 2.5mm mono jack (internal plug: positive supply, external ring: GND)
- Input voltage: 8 to 28Vdc 2A max



3.1.2 - 5Vdc (onboard generated)

This supply is directly generated from the main input supply by means of a DC/DC converter. It is mainly used to power the two USB host ports (500mA each) and to power the APF51 (WALLVDD input)

3.1.3 - 3.1Vdc (onboard generated)

This supply is generated from the local 5Vdc supply and uses a 1,5A DC/DC converter.

The goal of this supply is to power the “industrial” parts of the board:

- Ethernet port
- DVI
- DAC/ADC
- CAN controller
- CompactCom and Anybus HMS modules
- Extension port
- FPGA bank1 & bank3
- FPGA User LED

3.1.4 - 3.1Vdc (3V1_BAT) (onboard generated)

This supply is generated from the SYSVdd supply and uses a 1,5A DC/DC converter.

The goal of this supply is to power the “mobile” parts of the board:

- PMIC_LEDs
- TFT interface J2 (3.1V only)
- microSD
- WiFi
- Bluetooth
- RS232 transceiver
- GPS
- GSM
- Audio (except for the speaker outputs which are powered by the 5v)
- CSI interface
- i.MX User LED

3.1.5 - Battery Connector (J11)

The “mobile” part of the board can be powered by means of an external single cell Li-Ion/ Li-Po battery connected to J11. This battery can also be charged when the main DC supply is applied. Do not try to charge other type of battery.

⇒ **Charging current has to be adjusted in the PMIC according to the battery characteristics**

⇒ **No reverse protection is foreseen on this input**

3.2 - System LEDs

LED	Description
D18	This LED is connected to the PMIC (power management unit) LED1 signal of the APF51. This LED can be configured to indicate the system states (sleep mode, charging etc...)
D30	This LED is connected to the PMIC (power management unit) LED1 signal of the APF51. This LED can be configured to indicate the system states (sleep mode, charging etc...)

The following configurations are available:

- LED off
- LED indicates the Power State Status (see below)
- LED indicates the Charger Status (see below)
- LED in manual mode (off, constant on, continuous pulsed, pulsed sequence)

3.2.1 - System LEDs “Power Status Mode”

LED DRIVER	DESCRIPTION	DRIVE MODE	LED 'ON' TIME	ON:OFF DUTY CYCLE
LED1 or LED2	Power Sequence Failure	Pulsed sequence (4 pulses)	1s	1:1
	SYSVDD Low	Continuous pulsed	250ms	1:3
	ON state	Constant	n/a	n/a
	SLEEP state	Continuous pulsed	250ms	1:7

3.2.2 - System LEDs “Charger Status Mode”

LED DRIVER	DESCRIPTION	DRIVE MODE	LED 'ON' TIME	ON:OFF DUTY CYCLE
LED1 or LED2	Charger Complete	Constant	n/a	n/a
	Charger On	Continuous pulsed	1s	1:2

For details please see the PMIC datasheet (Reference chapter)

3.3 - System switches

Switch	Description
S2	Board Reset
S6	APF51 ON/OFF. Used to wake up the APF51 when in sleep mode. Pressing the button for more than 10sec will force a complete shutdown of the APF51

3.4 - User LEDs

LED	Description
D3	FPGA user LED. Directly connected to IO_L41P_GCLK9 pin of the FPGA. A high level will light the LED
D2	i.MX user LED. A high level on PWM1 (GPIO2 group1) pin of the i.MX will light the LED

3.5 - User switches

Switch	Description
S2	FPGA user switch. Directly connected to IO_L41N_GCLK8 pin of the FPGA. An external pullup is present on this line
S1	i.MX user switch. Connected to PWM2 (GPIO3 group1) pin of the i.MX. An external pullup is present on this line

3.6 - Jumpers

3.6.1 - Boot mode jumper (J13)

If a jumper is mounted on this 2 pin connector, the APF51 will start in bootstrap mode. This mode can be useful if the APF51 BIOS (U-Boot) is corrupted. The debug port is used to transfer U-Boot from your PC to the internal FLASH of the APF51. For more information please see the APF51 datasheet.

Reminder: Do not forget to remove the jumper after U-Boot recovery !

3.6.2 - Wireless jumper (J42)

Place this jumper if the GPS and/or the GSM modules have to be used. In this case the following FPGA lines will be reserved for the GPS/GSM:

IO_L39N_M3LDQSN_3
IO_L39P_M3LDQS_3
IOL_40P_M3DQ6_3
IO_L40N_M3DQ7_3
IO_L41P_GCLK7_M3DQ4_3
IO_L41N_GCLK26_M3DQ5_3
IO_L42N_GCLK24_M3LDM_3

3.6.3 - HMS jumper (J18)

Place this jumper if one of the ANYBUS HMS modules is used.

⇒ **In order to use the HMS Modules, J34 and J39 have to placed !!!**

In this case the following FPGA lines will be reserved :

Module	FPGA line used
CompactCom	IO_L32N_A16_M1A9_1
	IO_L47P_FWE_B_M1DQ0_1
	IO_L46P_FCS_B_M1DQS2_1
	IO_L39P_M1A3_1
ANYBUS M/S	IO_L43P_GCLK5_M1DQ4_1
	IO_L43N_GCLK4_M1DQ5_1
	IO_L45P_A1_M1LDQS_1
	IO_L45N_A0_M1LDQSN_1

	IO_L30P_A21_M1RESET_1
	IO_L30N_A20_M1A11_1
	IO_L31P_A19_M1CKE_1
	IO_L31N_A18_M1A12_1
	IO_L32P_A17_M1A8_1
	IO_L32N_A16_M1A9_1
	IO_L83P_3
	IO_L40N_M3DQ7_3
	IO_L53P_M3CKE_3
	IO_L40P_M3DQ6_3
	IO_L44N_GCLK20_M3A6_3
	IO_L42N_GCLK24_M3LDM_3
	IO_L34P_A13_M1WE_1
	IO_L34N_A12_M1BA2_1
	IO_L36P_A9_M1BA0
	IO_L36N_A8_M1BA1
	IO_L38P_A5_M1CLK_1
	IO_L38N_A4_M1CLKN_1
	IO_L40P_GCLK11_M1A5_1
	IO_L40N_GCLK10_M1A6_1
	IO_L46P_FCS_B_M1DQS2_1
	IO_L46N_FOE_B_M1DQ0_1

3.6.4 - FPGA Bank Power jumper (J34/J39)

These two jumpers are used to respectively power the BANK1 and the BANK3 of the APF51 FPGA. In this case the applied voltage is 3.1V (3V1_BAT).

⇒ In order to be used, the banks have to be powered !!!

3.7 - Ethernet 10/100 (J8)

The Ethernet connector can be used to connect your APF51Dev to your network.

Two LEDs (orange/green) respectively indicate the presence of the link and the activity on this link.

Connector type: shielded RJ45

3.8 - RS232 (J22)

A RS232 interface (RX/TX/CTS/RTS only) is accessible on J22. This RS232 is connected to the UART1 of the i.MX51.

The RS232 is fully protected against ESD.

Pin	Description	Type	Pin	Description	Type
1	Not Used		6	Not Used	
2	RX (i.MX51 side)	RS232 level	7	RTS (i.MX51 side)	RS232 level
3	TX (i.MX51 side)	RS232 level	8	CTS (i.MX51 side)	RS232 level
4	Not Used		9	Not Used	
5	GND	Power	Shield		

Connector type: DB9 Male

Signal level: RS232

3.9 - Console/Debug (J4)

The console interface is available through an UART to USB converter (Microchip MCP2200). Default baud rate is 115200 (8bits data, parity none, 1 stop bit and no flow control)

Connector type: USB microAB

Signal level: USB

Details concerning the MCP2200 can be found in the References Chapter

3.10 - LCD Interface

The LCD interface (24bits data wide) allows connecting to the APF51Dev board:

- STN/TFT displays
- Resistive touch panels

For compatibility reasons with the previous development kits, two connectors are used. The first one gathers the signals for TFT up to 18bits while the second connector adds the 6 bits for 24bits wide TFT.

When using a 24bits TFT, a simple 2x25 IDC ribbon cable is preferred (3M IDC ribbon cable socket 0.050” pitch)

3.10.1 - Connector (J2)

Pin	Description	Type	Pin	Description	Type
1	LSCLK	Output 3.1V	2	3.1V	Power
3	Not connected		4	5V	Power
5	1wire	Bidir 3.1V	6	CONTRAST	Output 3.1V
7	Not connected		8	OE_ACD	Output 3.1V
9	Not connected		10	HSYNC	Output 3.1V
11	GND	Bidir	12	VSYNC	Bidir
13	B1	Output 3.1V	14	GND	Power
15	B3	Output 3.1V	16	B2	Output 3.1V
17	B5	Output 3.1V	18	B4	Output 3.1V
19	G1	Output 3.1V	20	G0	Output 3.1V
21	G3	Output 3.1V	22	G2	Output 3.1V
23	G5	Output 3.1V	24	G4	Output 3.1V
25	R2	Output 3.1V	26	R1	Output 3.1V
27	R4	Output 3.1V	28	R3	Output 3.1V
29	R5	Output 3.1V	30	GND	Power
31	B0	Output 3.1V	32	R0	Output 3.1V

33	GND	Power	34	GND	Power
35	NC		36	NC	
37	Touch X+	Analog	38	Touch Y+	Analog
39	Touch X-	Analog	40	Touch Y-	Analog

Connector type: 2.54mm 30 pin dual rows

3.10.2 - Connector (J16)

Pin	Description	Type	Pin	Description	Type
1	TFT_24B0	Output 3.1V	2	TFT24B1	Output 3.1V
3	TFT_24B2	Output 3.1V	4	TFT_24B3	Output 3.1V
5	TFT_24B4	Output 3.1V	6	TFT_24B5	Output 3.1V

Connector type: 2.54mm 6 pin dual rows

3.11 - microSD (J6)

A standard microSD card can be connected to the APF51Dev providing additional storage capacity.

Connector type: Hirose DM3ATxxx

3.12 - Audio In / Audio Out

A complete audio stereo codec (Wolfson WM8960) is present on the APF51Dev board providing a stereo headset output, an amplified stereo speaker output (Class D amplifier 1W max under 8 ohms) and one microphone input.

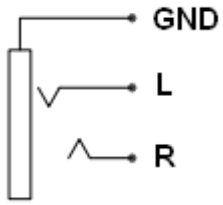
A synchronous serial interface (SSI) is used to exchange the audio data between the codec and the i.MX. The configuration of the WM8960 is done through the I2C2 interface (i2c address 1Ah).

Details concerning the WM8960 can be found in the References Chapter

3.12.1 - Headset Audio Connector (J26)

Connector type: 3.5mm stereo jack

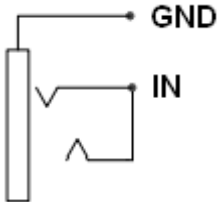
Signal level for headset output: 0.8Vrms full scale, 1.5V output common mode



3.12.2 - Microphone Audio Connector (J28)

Connector type: 3.5mm stereo jack

Signal level for headset input: 0.7Vrms full scale, 1.5V output common mode



3.12.3 - Speaker Audio Connector (J33)

Connector type: 2.54mm 4 pin single row header

Signal level: 1Wmax under 8 ohms (AC coupled output)

Pin	Description	Type
1	SPK_LP	Analog
2	SPK_LN	Analog
3	SPK_RP	Analog

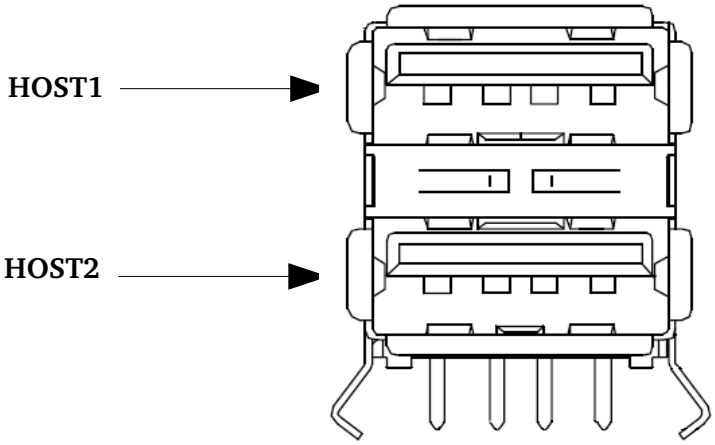
4	SPK_RN	Analog

3.13 - USB Hosts Interfaces (J1)

Two high speed USB host interfaces are available. Both have independent current monitors and are protected against ESD.

Connector type: dual USB A

Signal level: USB

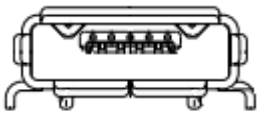


3.14 - USB OTG Interface (J3)

One high speed USB OTG interface is available through J3. A current monitor and ESD protections are provided.

Connector type: USB microAB

Signal level: USB



3.15 - DVI/HDMI Interface (J15)

The video controller of the APF51Dev board (TFP410 from TI) provides a fully compliant DVI/HDMI interface which can be used to display color images on a TV or a display (up to 1920x1080). The output HDMI/DVI resolution is the same as the one of TFT interface (no dual display support).

The controller is directly connected to the LCD interface. The I2C2 bus allows programming the controller parameters (i2c address 38h).

EDID support is also provided. The EDID informations can be read on the I2C2 bus at address 50h.

Details concerning the TFP410 can be found in the References Chapter

Remark: a converter cable can be used to convert the HDMI output into a DVI output.

Connector type: HDMI

3.16 - ADC / DAC interfaces

3.16.1 - ADC

A 8 inputs multiplexed ADC (AS1531 Austria Microsystems) is present on the APF51Dev board. It is a 12bits version with up to 300ksps per channel. It is connected to the SPI1 bus of the i.MX

By default the internal reference voltage of the AS1531 is used for the conversions. This means that the voltage level of the analog inputs (AINx) can not be greater than 2.5V. This can be changed by applying an other reference voltage on the REF pin (J5 pin 5) and by progamming the AS1531 to use the external reference. Care must be taken not to exceed the AS1531 and MCP4912 specification.

Details concerning the AS1531 can be found in the References Chapter

3.16.2 - DAC

A dual 10bits voltage DAC (MCP4912) is used to control external analog devices. The output values can be changed through the SPI1 interface of the i.MX. The external reference voltage is generated by the AS1531.

Details concerning the MCP4912 can be found in the References Chapter

3.16.3 - ADC/DAC Connector (J5)

Pin	Description	Type	Pin	Description	Type
1	DAC OUTA	Analog output (2.5V max with internal ref)	2	+3V1	Power
3	DAC OUTB	Analog output (2.5V max with internal ref)	4	ADC AIN7	Analog input (2.5V max with internal ref)
5	DAC REF	2.5V output if internal ref used otherwise external ref connection	6	ADC AIN6	Analog input (2.5V max with internal ref)
7	GND	Power	8	ADC AIN5	Analog input (2.5V max with internal ref)
9	ADC AIN3	Analog input (2.5V max with internal ref)	10	ADC AIN4	Analog input (2.5V max with internal ref)
11	ADC AIN1	Analog input (2.5V max with internal ref)	12	ADC AIN2	Analog input (2.5V max with internal ref)
13	GND	Power	14	ADC AIN0	Analog input (2.5V max with internal ref)

Connector type: 2.54mm 14 pin dual row header

Signal levels: 2.5V with internal reference voltage

3.17 - CAN (J8)

The CAN 2.0 controller is based on the MCP2515 from Microchip which is connected to the SPI2 bus of the i.MX processor. A CAN transceiver (SN65HVD234) converts the CMOS signals of the MCP2515 into CAN differential signals.

A 120 ohms termination between CANH and CANL can be enabled by connecting together pin 7 and 8 of J8.

Details concerning the MCP2515 and the SN65HVD234 can be found in the References Chapter

3.17.1 - CAN Connector

Pin	Description	Type	Pin	Description	Type
1	+5Vdc	Power	2	Not connected	
3	CANL	Diff	4	CANH	Diff
5	GND	Power	6	GND	Power
7	120 ohms jumper	Power	8	120 ohms jumper	

Connector type: 4 pins 2.54mm dual row header

Signal levels: CAN levels

3.18 - Backup Battery (J30)

A cell battery (type CR2032) can be placed in this holder to maintain the RTC information of the APF51, the GPS/GPRS/3G and the GPS modules even if the board is no more powered.

Remark: the cell battery has to be placed on the dedicated support according to the polarity indicated on this support !

3.19 - WiFi / Bluetooth

A combo Bluetooth/WiFi IC from Wi2Wi (W2CBW003) is used to provide Wireless connectivity to the APF51Dev board.

The Bluetooth part is connected to UART2 and to SSI6 (digital audio signals) of the i.MX

The WiFi part is connected to SDIO2 of the i.MX

Details concerning the W2CBW003 can be found in the References Chapter

3.19.1 - Bluetooth Characteristics

- GFSK modulation for Bluetooth 2.0
- DQPSK, 8 DPSK modulation for Bluetooth EDR
- Data rate up to 1Mbps for Bluetooth version 2.0
- Data rate up to 3Mbps for Bluetooth EDR

3.19.2 - WiFi Characteristics

- WiFi 802.11b/g, 15dBm transmit power
- 1, 2, 5.5 and 11 Mbps data rates for 802.11b (DSSS/CCK modulation)
- 6, 9, 12, 18, 24, 36, 48 and 54 Mbps data rates for 802.11g (QFDM modulation)

3.19.3 - Bluetooth Interfaces

- UART: TX, RX, CTS, RTS 115200 bps
- PCM: PCM_IN, PCM_CLK, PCM_SYNC, PCM_OUT
- Reset: Bluetooth reset

3.19.4 - WiFi Interfaces

SDIO: CMD, CLK, DAT0, DAT1, DAT2, DAT3

PWRDN#: WiFi power down

3.19.5 - Antenna (J7/J10)

Two U.FL connectors allow connecting external antenna (J7: WiFi, J10: Bluetooth).

3.20 - GSM/GPRS/3G (optional)

An optional GSM/GPRS/3G module (Sagem Hilo series) can be connected to the APF51Dev.

The communication with the module is done through an UART interface provided by the APF51 FPGA. This allows high speed communications in case of 3G module usage. FPGA IP and Linux drivers are provided by Armadeus. Further details can be found on our Wiki.

A SIM card support is located at the bottom side of the APF51Dev.

Two user connectors (J23 and J21) are used for speaker output and microphone input.

⇒ **Do not forget to place jumpers J42 and J39 if module is used**

3.20.1 - Characteristics

Frequency bands: GSM850, EGSM900, DCS1800, PCS1900 and UMTS 900/1900/2100 (3G only)

Voice codec: Half rate, full rate, enhanced full rate, adaptative multi rate

Transmit power:

Class 4 (2W) for GSM850 / EGSM900

Class 1 (1W) for DCS 1800 / PCS 1900

Class E2 EDGE 900 / 1800 (3G only)

Class 3 for UMTS 900/1900/2100 (3G only)

SIM: ISO7816-3 card support

Data / Command multiplexing: GSM 07.10 standard with AT_Command

Data services: GPRS, CSD, Fax. HSDPA and EDGE for 3G module

GPRS: SMG 31bis, multi slot class 10, class B terminal, PBCCH support

EDGE: multi slot class 12 (3G only)

UMTS/HSDPA: class E2, voice and data in parallel for UMTS/HSDPA, 4 logical channels (3G only)

HSPDA: 3.6Mbps (3G only)

3.20.2 - Interfaces

UART: TX, RX, CTS, RTS 115200 bps and 921600 bps for 3G module

SIM: support 1.8 and 3V sim cards

Audio out: differential pair headset (32 ohms)

Audio in: single ended microphone

VBackup: connected to the backup battery

3.20.3 - Antenna

An U.FL connector allows connecting an external antenna. Take care about the frequency range when choosing the external antenna. **Do not place the GSM/GPRS antenna near the GPS one !**

3.20.4 - Microphone Connector (J21)

Pin	Name	Description
1	INTMIC_P	Mic IN
2	GND	Ground

3.20.5 - Speaker Connector (J23)

Pin	Name	Description
1	HSET_OUT_P	Positive Headset output
2	HSET_OUT_N	Negative Headset output

3.21 - GPS (optional)

An optional GPS module from U-Blox (or equivalent, NEO 5/6 model) is foreseen.

The communication with this module is done through an UART interface provided by the APF51 FPGA.

FPGA IP and Linux drivers are provided by Armadeus. Further details can be found on our Wiki.

The GPS_TIME_PULSE signal is also connected to the FPGA (IO_L40N_M3DQ7_3).

⇒ Do not forget to place jumpers J42 and J39 if module is used

3.21.1 - Characteristics

- 50-channel with over 1 million effective correlators
- <1 second Time To First Fix for Hot and Aided starts
- -160dBm Supersense acquisition and tracking sensitivity
- Cold start: 32s
- Horizontal position accuracy: < 2.5m
- A-GPS, NMEA and UBX support
- High immunity to jamming
- 4Hz position update rate
- GPS sleep

3.21.2 - Interfaces

UART: TX, RX 38400 bps

GPS_TIME_PULSE: CMOS 3.1V output. 1PPS

3.21.3 - Antenna (J25)

An U.FL connector allows connecting an external antenna. **Do not place the GPS antenna near the GSM one !**

3.22 - CMOS Sensor Interface (J38)

This interface can be used to connect a standard CMOS sensor for image acquisition. Usually an adapter board/cable will be required.

Communication with the CMOS sensor is done through the I2C2 interface while image data are transferred on a dedicated bus (CSI).

Pin	Description	Type
1	+3V1dc_BAT	Power

2	+1V8	Power
3	GND	Power
4	CSI_D0	Input 3.1Vdc
5	CSI_D1	Input 3.1Vdc
6	CSI_D2	Input 3.1Vdc
7	CSI_D3	Input 3.1Vdc
8	GND	Power
9	CSI_D4	Input 3.1Vdc
10	CSI_D5	Input 3.1Vdc
11	CSI_D6	Input 3.1Vdc
12	CSI_D7	Input 3.1Vdc
13	GND	Power
14	CSI_D8	Input 3.1Vdc
15	CSI_D9	Input 3.1Vdc
16	CSI_VSYNC	Input 3.1Vdc
17	CSI_HSYNC	Input 3.1Vdc
18	GND	Power
19	CSI_MCLK	Output 3.1Vdc
20	GND	Power
21	CSI_PIXCLK	Input 3.1Vdc
22	GND	Power
23	CSI_SPARE1	GPIO 3.1Vdc
24	CSI_SPAR2	GPIO 3.1Vdc
25	I2C2_SCL	Output 3.1Vdc
26	I2C2_SDA	IO 3.1Vdc

Connector type: FPC/FFC 26pin 0.5mm pitch bottom contacts

Signal levels: 3.1Vdc levels

3.23 - JTAG (J36)

A standard JTAG connector is available for debug purpose. Two components are present on the JTAG chain: the i.MX and the FPGA.

This connector is compatible with most of the JTAG debugger

Pin	Description	Type	Pin	Description	Type
1	JTAG_VREF	Power (3.1Vdc)	2	+3V1	Power
3	JTAG_TRSTB	Input 3.1Vdc	4	GND	Power
5	JTAG_TDI	Input 3.1Vdc	6	GND	Power
7	JTAG_TMS	Input 3.1Vdc	8	GND	Power
9	JTAG_TCK	Input 3.1Vdc	10	GND	Power
11	Not connected		12	GND	Power
13	JTAG_TDO	Output 3.1Vdc	14	GND	Power
15	RESET#	Bidirectional	16	GND	Power
17	Not connected		18	GND	Power
19	Not connected		20	GND	Power

Connector type: 2.54mm 20 pin dual row header

Signal levels: 3.1Vdc

3.24 - Extension (J35)

This connector is foreseen for APF51Dev extensions and can be used for rapid prototyping of specific products.

3.24.1 - Interfaces

- SPI2: standard SPI. The SPI2 is also connected to the CAN controller. SPI2_SS2 can be used as chip select or as a general purpose IO
- PWM1: connected to the user LED D2. Can also be used as a PWM output or as a general purpose IO
- PMW2: connected to the user switch S1. Can also be used as a PWM output or as a general purpose IO

- AUXADCIN1 to3: connected to the APF51 PMIC low speed 12bits ADC. Maximum input voltage is SysVDD
- AUXADCIN4: connected to the APF51 PMIC low speed 12bits ADC. Maximum input voltage is 2.5V
- 1Wire: this signal is also present on the TFT connector. Can be used as a general purpose IO
- PMIC_GPIO6: this signal is connected to the GSM/GPRS module. If this module is not use, then this signal can be configured as a general purpose IO
- PMIC_GPIO7: if the audio codec is not used, this signal can be configured as a general purpose IO
- GPIO2_30: general purpose IO connected to the i.MX

Pin	Description	Type	Pin	Description	Type
1	SPI2_SCLK	Output 3.1Vdc	2	+5V	Power
3	SPI2_MOSI	Output 3.1Vdc	4	+3V1	Power
5	SPI2_MISO	Input 3.1Vdc	6	PWM1 (connected to i.MX user LED D2)	
7	SPI2_SS2	GPIO 3.1Vdc	8	PWM2 (connected to i.MX user switch S1)	
9	GND	Power	10	GND	Power
11	AUXADCIN1	Analog input. SysVDD	12	PMIC_GPIO6 (shared with GSM/GPRS/3G module)	GPIO 3.1Vdc
13	AUXADCIN2	Analog input. SysVDD	14	PMIC_GPIO7 (shared with audio code)	GPIO 3.1Vdc
15	AUXADCIN3	Analog input. SysVDD	16	GPIO2_30	GPIO 3.1Vdc
17	AUXADCIN4	Analog input (2.5V level)	18	1Wire	GPIO 3.1Vdc
19	GND	Power	20	GND	Power

Connector type: 2.54mm 20 pin dual row header

3.25 - Keypad (J9)

A keypad matrix (up to 24 keys) can be connected to this interface. The keypad signals can also be used as general purpose IOs but will require a specific driver.

⇒ **No ESD protection is present on this interface. ESD diodes have to be added depending on final usage**

Pin	Description	Type	Pin	Description	Type
1	KEYPAD_COL0	GPIO 3.1Vdc	2	KEYPAD_ROW3	GPIO 3.1Vdc
3	KEYPAD_COL1	GPIO 3.1Vdc	4	KEYPAD_ROW2	GPIO 3.1Vdc
5	KEYPAD_COL2	GPIO 3.1Vdc	6	KEYPAD_ROW1	GPIO 3.1Vdc
7	KEYPAD_COL3	GPIO 3.1Vdc	8	KEYPAD_ROW0	GPIO 3.1Vdc
9	KEYPAD_COL4	GPIO 3.1Vdc	10	KEYPAD_COL5	GPIO 3.1Vdc

Connector type: 2.54mm 10 pin dual row header

Signal levels: 3.1Vdc

3.26 - Anybus® CompactCom

Anybus-CC has been designed to fit into many types of industrial automation devices. HMI's, robot controllers, drives, micro PLC's, valve manifolds, instruments, weigh scales, temperature controllers, bar-code scanners, I/O blocks, welding controllers and RFID applications are just some of todays automation devices that are using Anybus-CC technology for their network option interface.

Pre-certified for full interoperability and network compliance with, CE, UL and RoHS conformance

⇒ Do not forget to place jumpers J18 and J34 if module is used

3.26.1 - Supported industrial bus

- Fieldbus versions: BACnet MSTP, CANopen, CC_Link, CompoNet, ControlNet, DeviceNet, Modbus-RTU, Profibus
- Industrial Ethernet versions: BACnet/IP 2-port, EtherCAT, EtherNET/IP, EtherNET/IP 2-port, Modbus-TCP, Profinet-IO, Profinet-IO 2-port, Sercos III

3.27 - Anybus®-M

The Anybus-M modules are ready-to-use full featured master/scanner interfaces. The complete protocol functionality is implemented inside the communication module. The powerful on-oboard microprocessor handles the complete network protocol and thus off-load the microprocessor of the host automation device from all time-critical protocol handling.

Pre-certified for full interoperability and network compliance with, CE, UL and RoHS conformance

⇒ Do not forget to place jumpers J18, J39 and J34 if module is used

3.27.1 - Supported industrial bus

- Fieldbus versions: AS-Interface, DeviceNet, Profibus DPV1
- Industrial Ethernet versions: EtherNet/IP

3.28 - Anybus®-S

Anybus-S has been designed to fit into many types of industrial automation devices. HMI's, robot controllers, drives, micro PLC's, valve manifolds, instruments, weigh scales, temperature controllers, bar-code scanners, I/O blocks, welding controllers and RFID applications are just some of todays automation devices that are using Anybus-S for their network option interface.

Designed for demanding application with up to 512 bytes input and 512 bytes output data

⇒ Do not forget to place jumpers J18, J39 and J34 if module is used

3.28.1 - Supported industrial bus

- Fieldbus versions: CANopen, CC-Link, ControlNet, DeviceNet, FIPIO, Interbus, Interbus Fiber Optic, Lonworks, Modbus Plus, Modbus-RTU, Profibus-DP, Profibus-DPV1

- Industrial Ethernet versions: EtherCAT, EtherNet/IP, EtherNet/IP/MB-TCP 2-port, FL-net, Modbus-TCP, Profinet-IO, Profinet-IRT 2-port, Profinet-IRT Fibre Optic

3.29 - Anybus Usage

Complete software stack provided with the module. No additional costs.

3.30 - FPGA interfaces

Two large connectors provide access to the FPGA signals.

Up to 64 signals can be configured as single ended and differential lines. For more information have a look at the FPGA specification located at the end of this document.

It has to be noted that several signals are shared with the GPS, GSM and ANYBUS modules.

3.30.1 - FPGA Bank supplies

⇒The FPGA bank1 and bank3 need to be powered by an external supply which can be applied at any time (hot plug).

The FPGA bank1 can be powered by an external power supply (Pin 2 of J34) or can be powered by the local 3.1V_BAT supply if a jumper is mounted on J34.

The FPGA bank3 can be powered by an external power supply (Pin 2 of J39) or can be powered by the local 3.1V_BAT supply if a jumper is mounted on J39.

3.30.2 - FPGA Connector (J17)

Pin	Description	Type	Supply domain	Pin	Description	Type	Supply domain
1	FPGA_BANK3_PWR	Power	BANK3	2	IO_L39N_M3LDQSN_3	GPIO	BANK3
3	IO_L39P_M3LDQS_3	GPIO	BANK3	4	IO_L41N_GCLK26_M3DQ5_3	GPIO	BANK3
5	IO_L41P_GCLK27_M3DQ4_3	GPIO	BANK3	6	IO_L43N_GCLK22_IRDY2_M3CASN_3	GPIO	BANK3
7	IO_L43P_GCLK23_M3RASN_3	GPIO	BANK3	8	IO_L45N_M3ODT_3	GPIO	BANK3
9	IO_L45P_M3A3_3	GPIO	BANK3	10	IO_L83N_VREF_3	GPIO	BANK3
11	IO_L83P_3	GPIO	BANK3	12	IO_L53N_M3A12_3	GPIO	BANK3
13	IO_L53P_M3CKE_3	GPIO	BANK3	14	IO_L40N_M3DQ7_3	GPIO	BANK3
15	IO_L40P_M3DQ6_3	GPIO	BANK3	16	IO_L42N_GCLK24_M3LDM_3	GPIO	BANK3
17	IO_L42P_GCLK25_TRDY2_M3UDM_3	GPIO	BANK3	18	IO_L44N_GCLK20_M3A6_3	GPIO	BANK3
19	IO_L44P_GCLK21_M3A5_3	GPIO	BANK3	20	IO_L46N_M3CLKN_3	GPIO	BANK3
21	IO_L46P_M3CLK_3	GPIO	BANK3	22	IO_L54N_M3A11_3	GPIO	BANK3
23	IO_L54P_M3RESET_3	GPIO	BANK3	24	IO_L52N_M3A9_3	GPIO	BANK3
25	IO_L52P_M3A8_3	GPIO	BANK3	26	IO_L44N_A2_M1DQ7_1	GPIO	BANK1
27	IO_L42P_GCLK7_M1UDM_1	GPIO	BANK1	28	IO_L42N_GCLK6_TRDY1_M1LDM	GPIO	BANK1

29	IO_L44P_A3_M1DQ6_1	GPIO	BANK1	30	IO_L39N_M1ODT_1	GPIO	BANK1
31	GND	Power		32	IO_L39P_M1A3_1	GPIO	BANK1
33	Not connected			34	GND	Power	
35	Not connected			36	Not connected		
37	Not connected			38	Not connected		
39	Not connected			40	GND	Power	
41	+3V1	Power		42	GND	Power	

Connector type: 2.54mm 42pin dual row header

Used by the GPS/GSM modules if jumper J42 mounted

Used by the ANYBUS-M/S if jumper J18 mounted

Used by the CompactCom if jumper J18 mounted

3.30.3 - FPGA Connector (J24)

Pin	Description	Type	Supply domain	Pin	Description	Type	Supply domain
1	FPGA_BANK1_PWR	Power	BANK1	2	IO_L74N_DOUT_BUSY_1	GPIO	BANK1
3	IO_L74P_AWAKE_1	GPIO	BANK1	4	IO_L47N_LDC_M1DQ1_1	GPIO	BANK1
5	IO_L47P_FWE_B_M1DQ0_1	GPIO	BANK1	6	IO_L46N_FOE_B_M1DQ3_1	GPIO	BANK1
7	IO_L46P_FCS_B_M1DQS2_1	GPIO	BANK1	8	IO_L40N_GCLK10_M1A6_1	GPIO	BANK1
9	IO_L40P_GCLK11_M1A5_1	GPIO	BANK1	10	GND	Power	
11	GND	Power		12	FPGA_BANK1_PWR	Power	BANK1
13	IO_L38P_A5_M1CLK_1	GPIO	BANK1	14	IO_L38N_A4_M1CLKN_1	GPIO	BANK1
15	IO_L36P_A9_M1BA0_1	GPIO	BANK1	16	IO_L36N_A8_M1BA1_1	GPIO	BANK1
17	IO_L34P_A13_M1WE_1	GPIO	BANK1	18	IO_L34N_A12_M1BA2_1	GPIO	BANK1
19	IO_L32P_A17_M1A8_1	GPIO	BANK1	20	IO_L32N_A16_M1A9_1	GPIO	BANK1
21	IO_L31P_A19_M1CKE_1	GPIO	BANK1	22	IO_L31N_A18_M1A12_1	GPIO	BANK1
23	IO_L30P_A21_M1RESET_1	GPIO	BANK1	24	IO_L30N_A20_M1A11_1	GPIO	BANK1
25	IO_L45P_A1_M1LDQS_1	GPIO	BANK1	26	IO_L45N_A0_M1LDQSN_1	GPIO	BANK1
27	IO_L43P_GCLK5_M1DQ4_1	GPIO	BANK1	28	IO_L43N_GCLK4_M1DQ5_1	GPIO	BANK1

29	IO_L41P_GCLK9_IRDY1_M1RASN_1	GPIO	BANK1	30	IO_L41N_GCLK8_M1CASN_1	GPIO	BANK1
31	IO_L37P_A7_M1A0_1	GPIO	BANK1	32	IO_L37N_A6_M1A1_1	GPIO	BANK1
33	IO_L35P_A11_M1A7_1	GPIO	BANK1	34	IO_L35N_A10_M1A2_1	GPIO	BANK1
35	IO_L33P_A15_M1A10_1	GPIO	BANK1	36	IO_L33N_A14_M1A4_1	GPIO	BANK1
37	IO_L1P_A25_1	GPIO	BANK1	38	IO_L1N_A24_VREF_1	GPIO	BANK1
39	+3V1	Power			GND	Power	

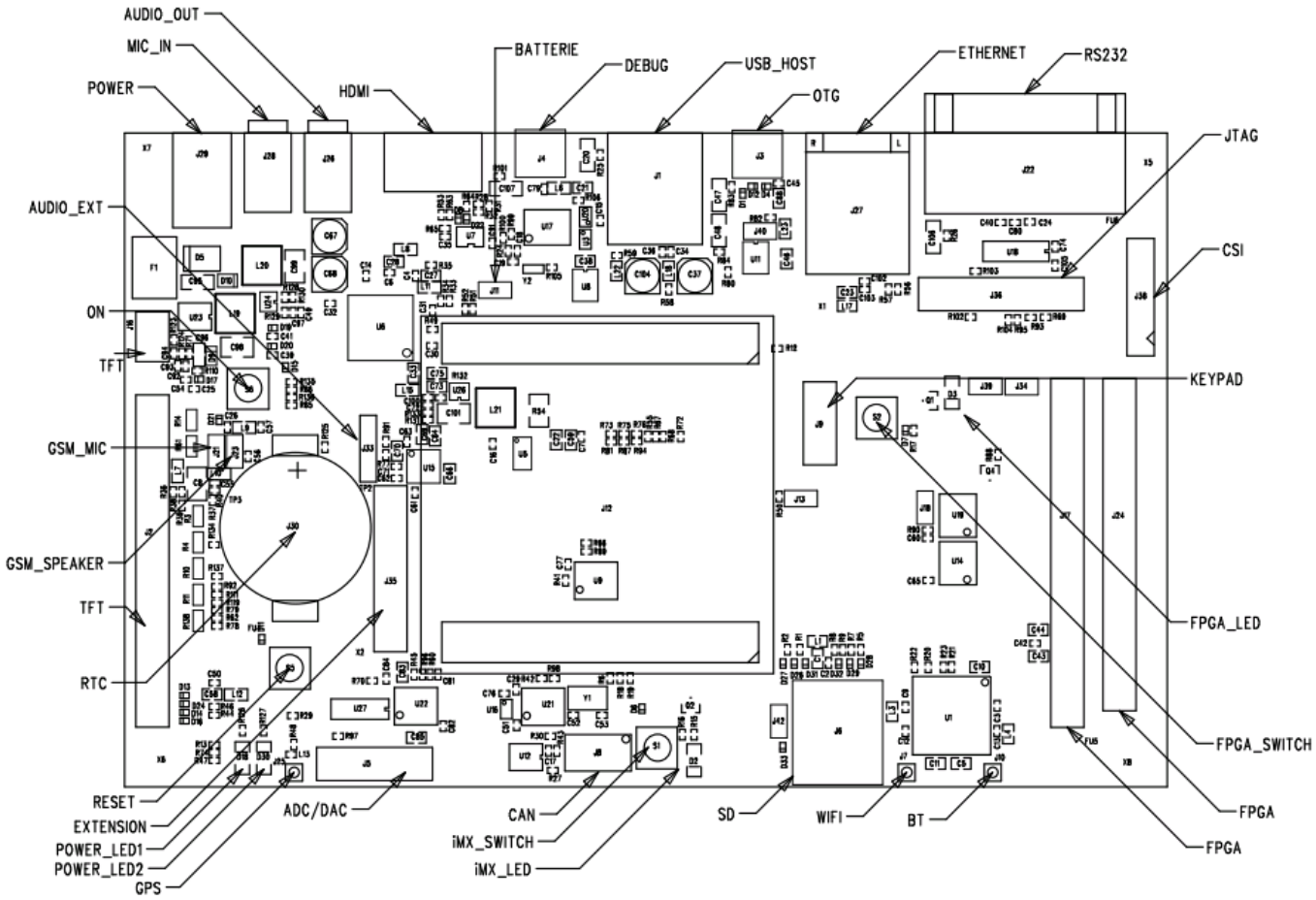
Connector type: 2.54mm 42pin dual row header

Used by the ANYBUS-M/S if jumper J18 mounted

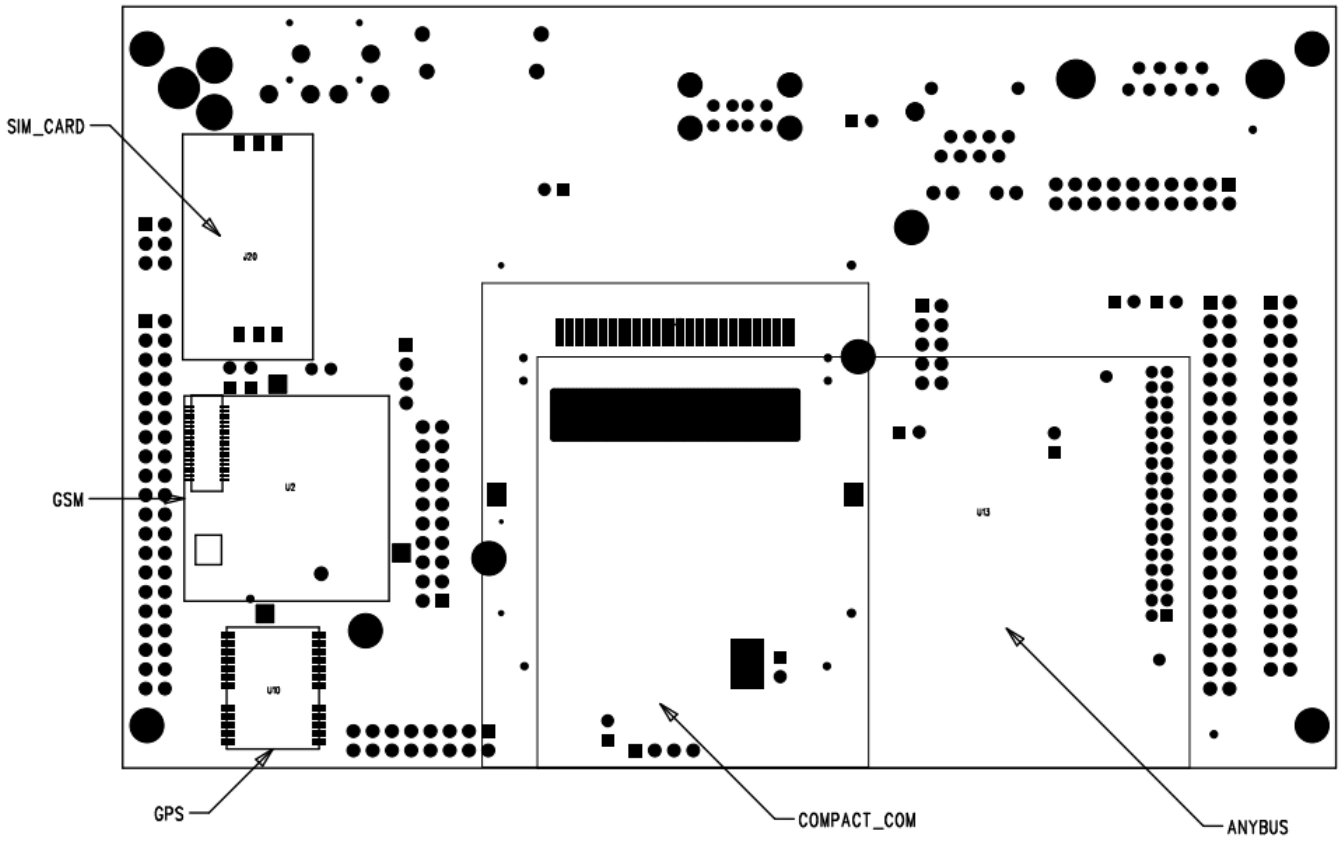
Used by the CompactCom if jumper J18 mounted

4 - Mechanical and Assembly drawing

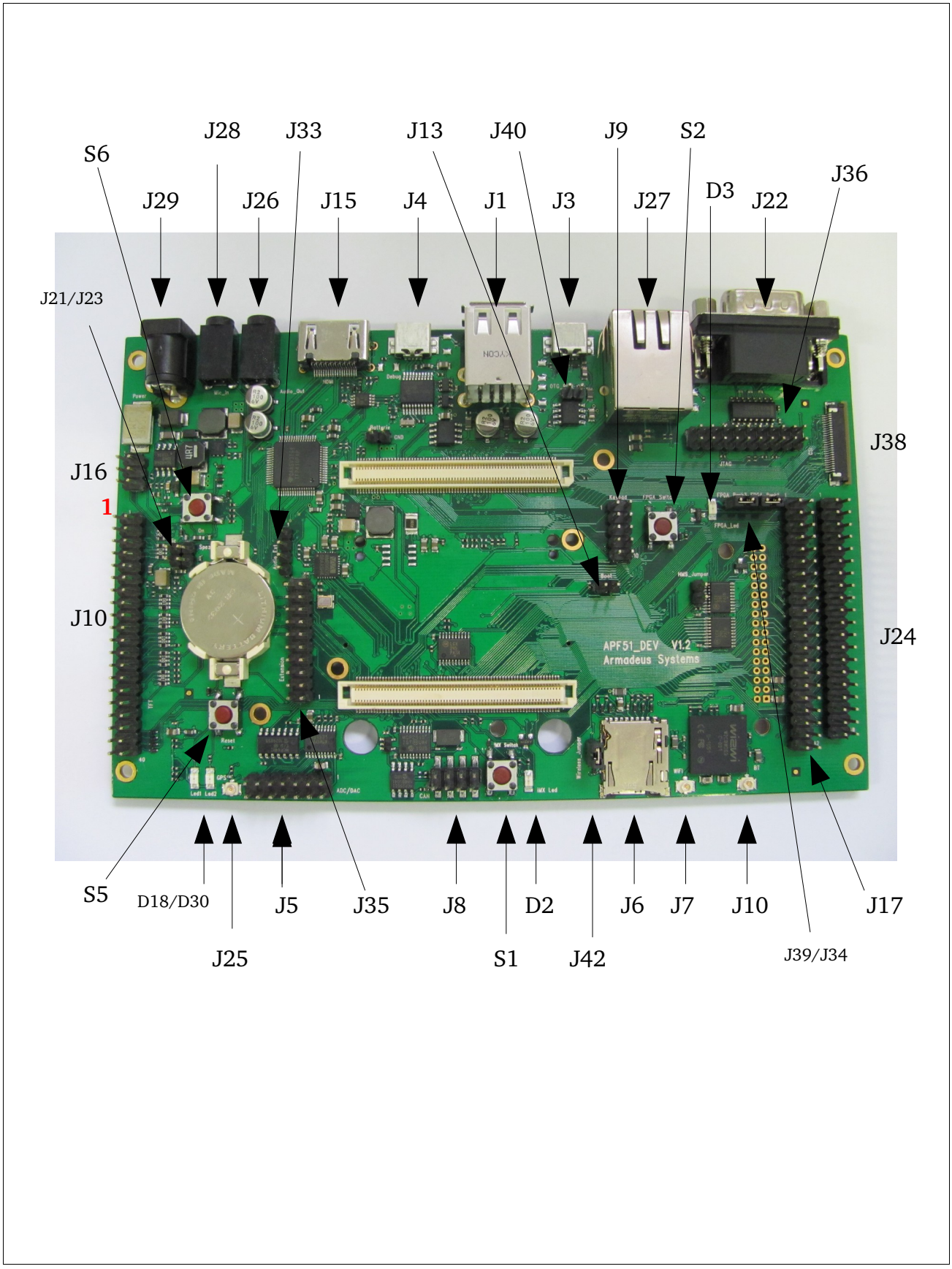
4.1 - Top Assembly

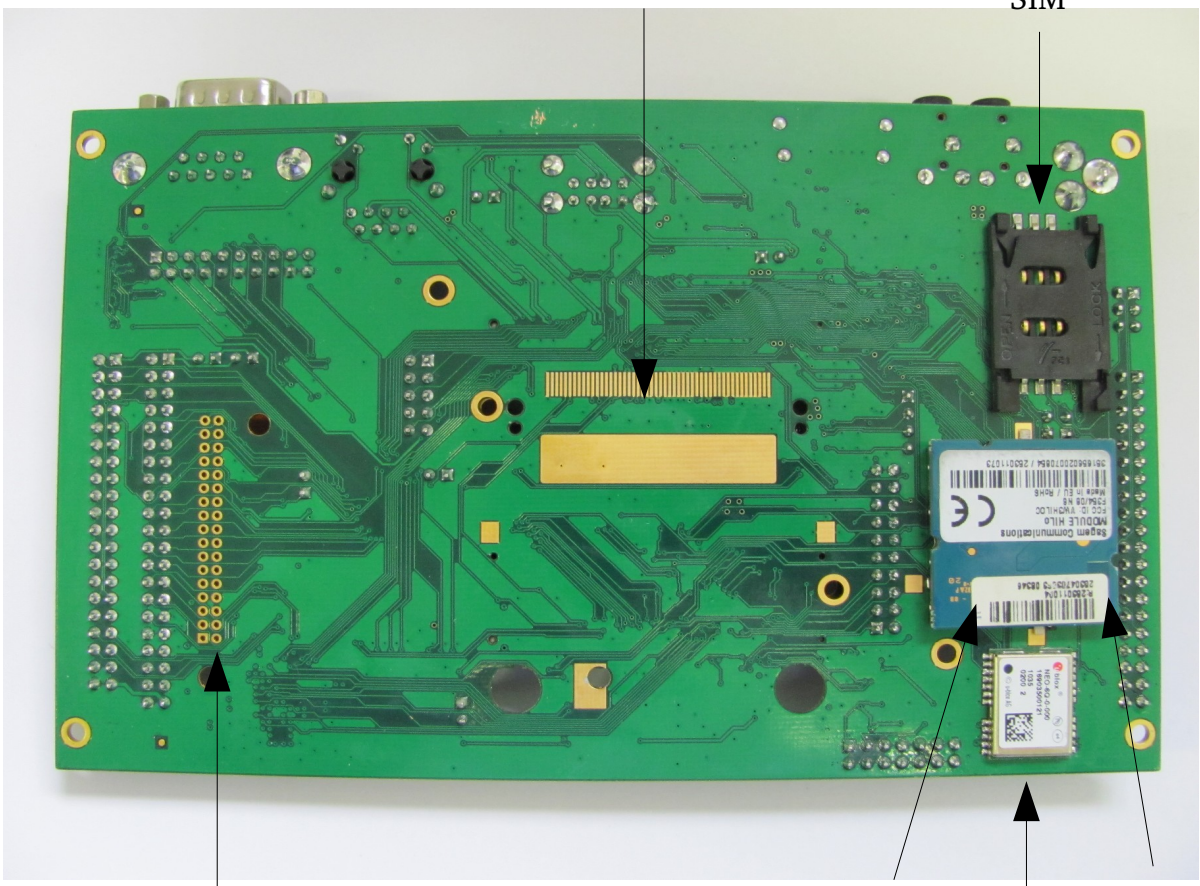


4.2 - Bottom Assembly

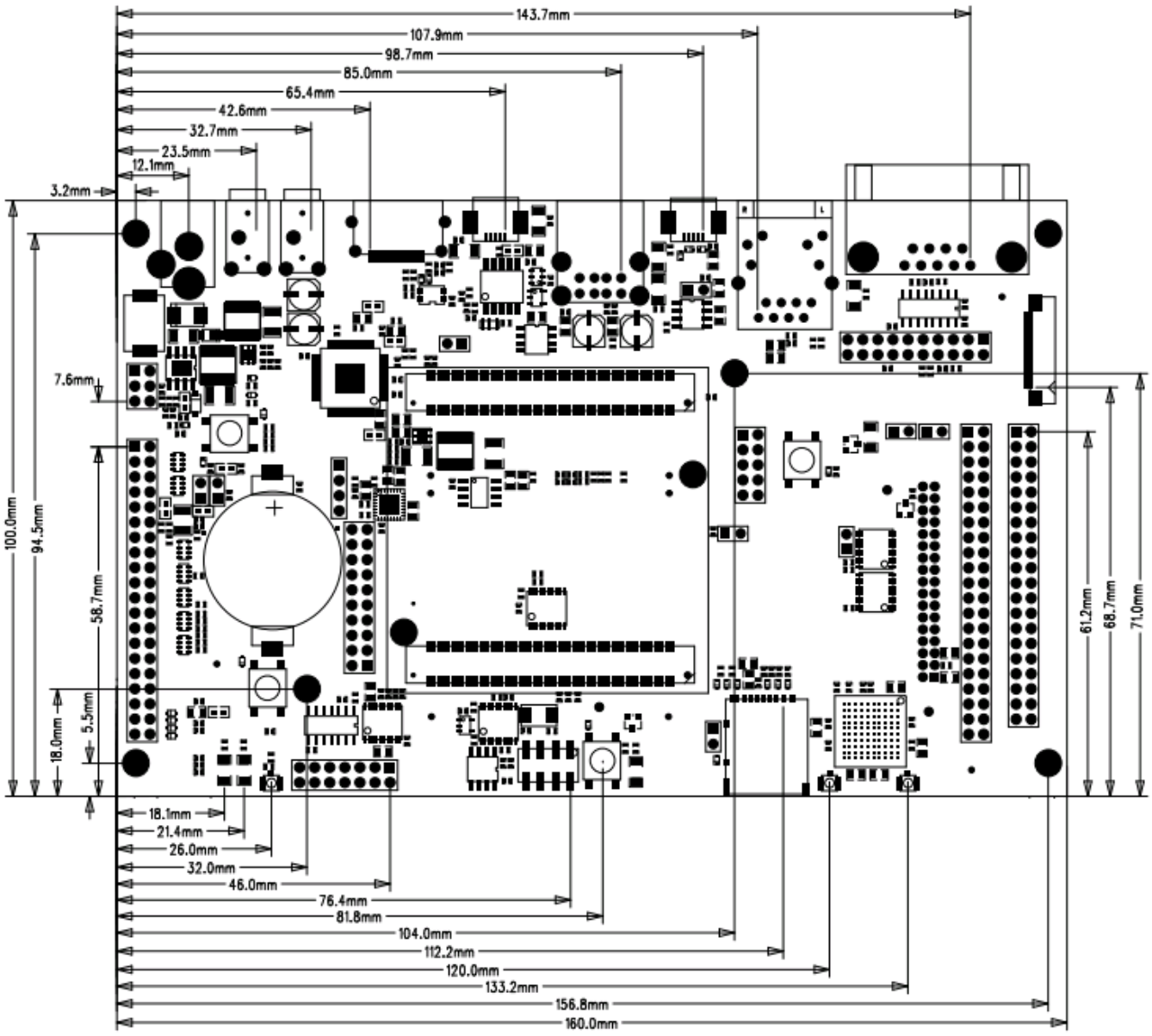


4.3 - Connectors and jumpers




ANYBUS S
connector
SIM
ANYBUS M
connector
GSM/GPRS/3G
GPS
GSM
Antenna
(under the
module)

4.4 - Mechanical



5 - Web Link

Armadeus Systems general documentation: http://www.armadeus.org

APF51Dev wiki page: http://www.armadeus.com/wiki/index.php?title=APF51Dev

APF51 wiki page: http://www.armadeus.com/wiki/index.php?title=APF51

6 - Component Link

MCP2515: http://ww1.microchip.com/downloads/en/DeviceDoc/21801e.pdf

SN65HVD234: http://www.ti.com/lit/gpn/sn65hvd234

PMIC: http://www.wolfsonmicro.com/documents/uploads/data_sheets/en/WM8311.pdf

MCP2200: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en546923

WM8960: http://www.wolfsonmicro.com/products/codecs/WM8960

TFP410: http://focus.ti.com/lit/ds/symlink/tfp410.pdf

AS1531 :http://www.austriamicrosystems.com/eng/Products/Data-Converters/A-D-Converter/AS1531

W2CBW0003: http://www.wi2wi.com/products/datasheets/W2CBW003_PB%20rev1.2.pdf.

Hilo2: http://support.sagemcom.com/site/modele_fax.php?page=spec_gen&prd=HiloV2&pays=uk

Hilo3G: http://support.sagemcom.com/site/modele_fax.php?page=spec_gen&prd=Hilo3g&pays=uk

Anybus-M: http://www.anybus.com/products/abm.shtml

Anybus-S: http://www.anybus.com/products/abs.shtml

CompactCom: http://www.anybus.com/products/abcc.shtml

Neo6: http://www.ublox.com/images/downloads/Product_Docs/NEO-6_DataSheet_%28GPS.G6-HW-09005%29.pdf