Atheros WiFi Update
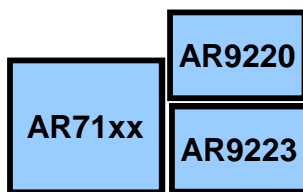
There is Here.™
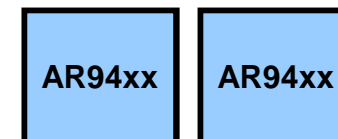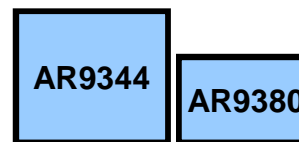
Product Roadmap

**Dual-Band Concurrent**

AR71xx
AR9220
AR9223

- **2x2 + 2x2 11n DB concurrent**
- 680MHz MIPS 24K NPU
- R/GMII, 2x USB 2.0

- **3x3 + 2x2 11n DB concurrent**
- Full offload
- 550MHz+ MIPS 74K
- Advanced features
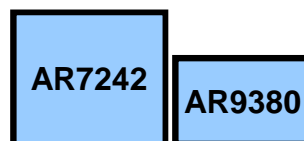
AR9344
AR9380

AR94xx
AR94xx

- **3x3+ 3x3 11n DB concurrent**
- 600+ MHz MIPS 74K
- Int. PA/LNA
- RGMII/SGMII/MII
- USB2.0x2 Host/Device

- **2x2 + 2x2 DB concurrent**
- Full offload
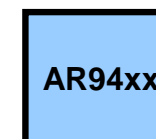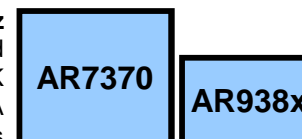- 550MHz+ MIPS74K
- Int. PA/LNA
- Advanced features

AR9344
AR9382

3x3

AR7242
AR9380
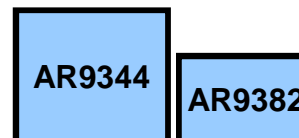
- **3x3 11n 2.4/5GHz**
- 440MHz MIPS 24K NPU
- Int. PA/LNA
- USB 2.0
- Ext. GbE switch

- **3x3 11n 2.4/5GHz**
- Full offload
- 550MHz+ MIPS74K
- Int. PA/LNA
- Advanced features

AR7370
AR938x

AR94xx

- **3x3 11n 2.4/5GHz SOC**
- 600+ MHz MIPS74K NPU
- Int. PA/LNA
- RGMII/SGMII/MII
- USB2.0 x2 Host/Device

2x2

AR7242
AR9280/ AR9287
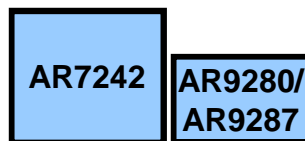
- **2x2 11n 2.4GHz or 2.4/5GHz**
- 400MHz MIPS 24K NPU
- Int. FE switch w USB 2.0

- **2x2 11n 2.4/5GHz**
- Full offload
- 550MHz+ MIPS74K
- Int. PA/LNA
- Advanced features
- USB2.0

AR9342

1x1

AR7240 Python
AR9285 Kite
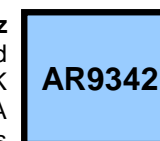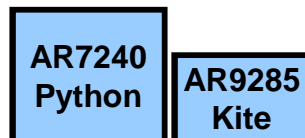
- **1x1 11n 2.4GHz**
- 400MHz MIPS 24K NPU
- Int. FE switch
- Int. PA/LNA

AR9333 Hornet
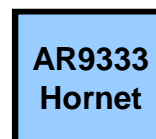
- **1x1 11n 2.4GHz**
- Full offload
- 400MHz MIPS 24K NPU
- Int. FE switch
- Int. PA/LNA
- USB 2.0

| Production | NOW | Q4'10 | Q1'11 | Q2'11 |

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WLAN Update
Atheros New Radio - Osprey

There is Here.™

Radio Part No.	AR9380 - 802.11n 3x3, 2.4/5GHz
	AR9381 - 802.11n 3x3, 2.4GHz
	AR9382 - 802.11n 2x2, 2.4/5GHz
Host Interface	PCIe
Certifications & Standards	IEEE a,b,d,e,g,h,i,j,k,n,r,s,w WMM, WPS, FCC, ETSI
Key Features	§ 65nm CMOS § Up to 3 spatial streams § Up to 450Mbps data rate § ML Demodulation § Up to 3xMRC § LDPC § TxBF § Integrated 2.4 & 5GHz PA/LNA
Key Value Proposition	§ Extended range/robustness § Increased data rate and throughput § Low system power § Highest level of integration § Smallest footprint
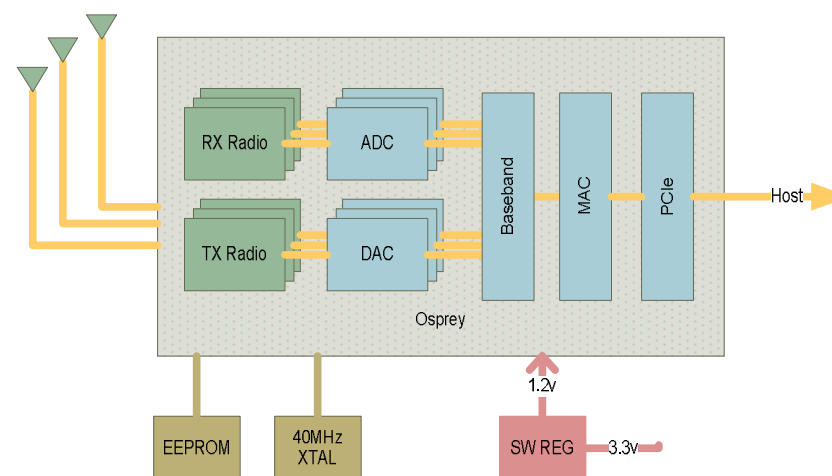
There is Here.

ATHEROS

SST3 packs the best technologies
and features from 802.11n
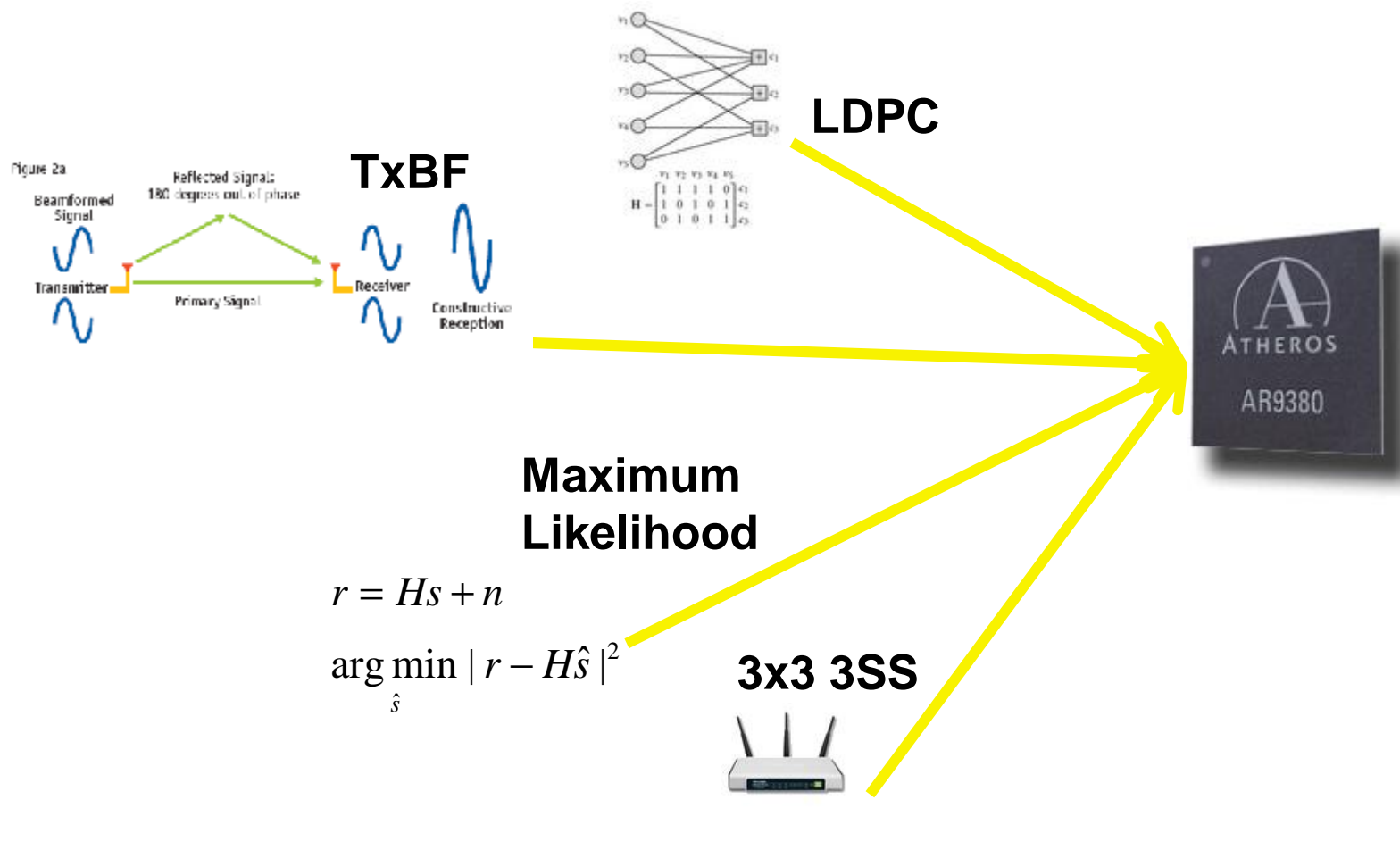
LDPC

TxBF

**Maximum
Likelihood**

$$r = Hs + n$$

$$\arg \min_{\hat{s}} | r - H\hat{s} |^2$$

3x3 3SS

ATHEROS
AR9380

XSPAN
ATHEROS

There is Here.

XSPAN's coverage enhancements result in a 50% average increase in rate-over-range across the entire link vs. 2SS

While the 3SS increases the throughput by 50%, the unique combination of 3x3, LDPC and….
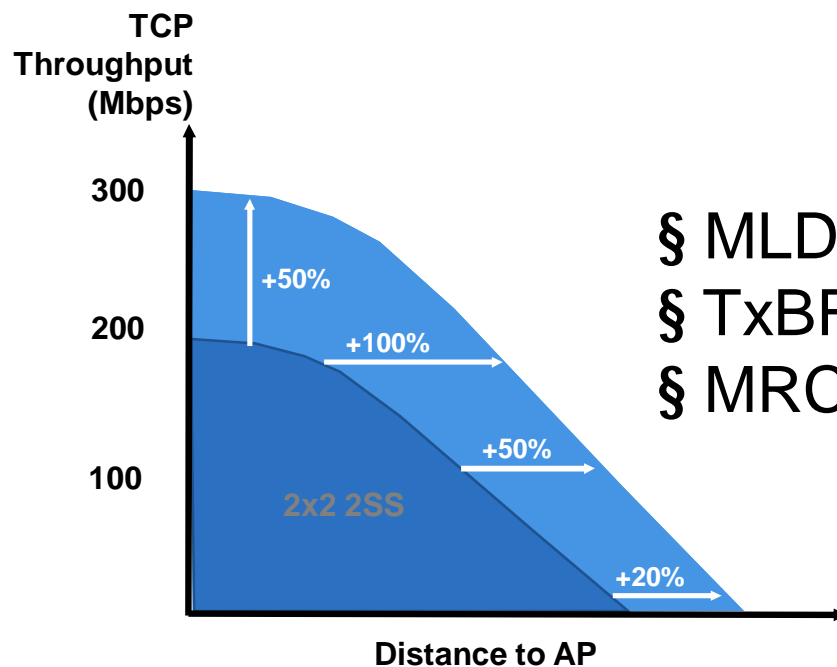
§ MLD at close range deliver +100%
§ TxBF at mid range deliver +50%
§ MRC at long range deliver +20%

The industry's ONLY combination of 3-stream 11n with SST, Atheros' 11n rate-over-range enhancement suite

MLD	TxBF	MRC
	Low Density Parity Check	
	3x3 MIMO Configuration	

Short Range | Mid-Range | Long-Range
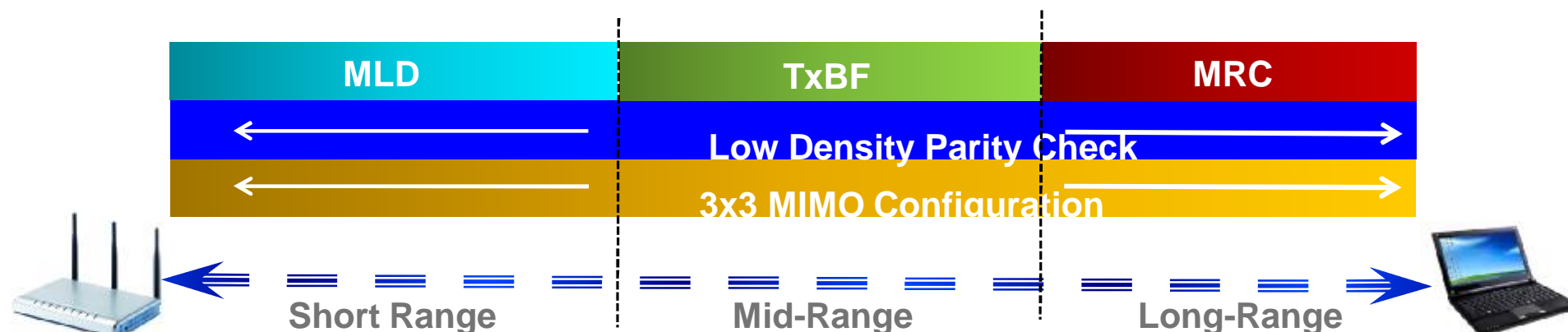
- At short range: **Maximum Likelihood Demodulation** (MLD) optimally demodulates the MIMO signal vs. the more common demodulation scheme, Zero Forcing, providing additional 6dB gain
- At mid-range: **Transmit Beamforming** (TxBF) focuses the transmit energy to the receive antenna, executed at sub-carrier level to optimize signal reception
- At long-range: **Maximal Ratio Combining** (MRC) enables the receiver to optimally combine different signal paths
- Across the entire link continuum: **Low Density Parity Check** (LDPC) – provides Forward Error Control coding to more efficiently guard against the loss of information during transmissions

There is Here.™

Transmit Beamforming (TxBF)
Increased data throughput at medium/long range

u **3x3 3SS**

u No TxBF

u **AR9380**

u Both Explicit TxBF and Implicit TxBF are implemented to enable best interoperability

TCP Throughput (Mbps)

TxBF

AR9380
3x3 3SS

No TxBF

300

200

100

2x2 2SS

Distance

There is Here.
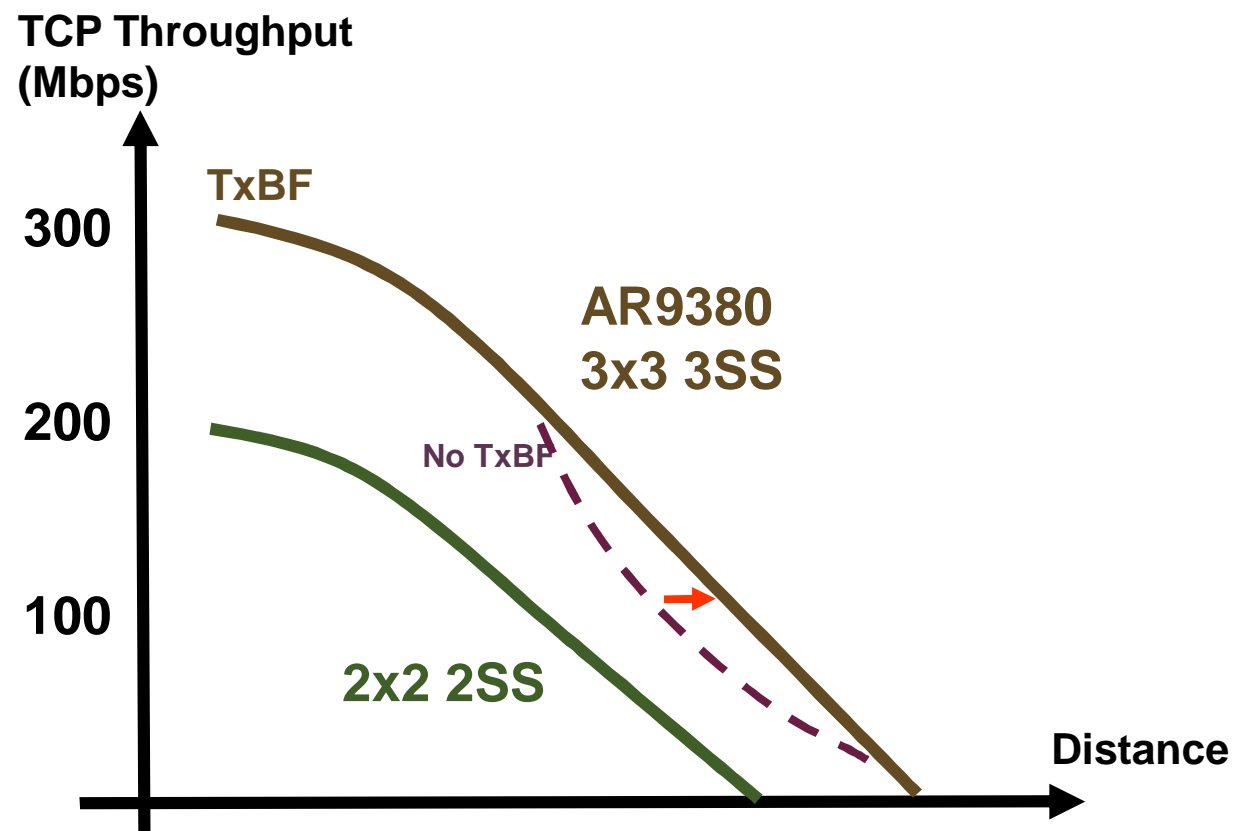
Maximum Likelihood (ML) Demodulation
Increased data throughput at short range

u **3x3 3SS**

- u Zero Forcing (ZF) Demodulation
- u Each receiver chain demodulates its own received symbol

u **AR9380**

- u ML Demodulation
- u All three receivers jointly demodulator the received symbols

TCP Throughput (Mbps)

300

ML

ZF

AR9380 3x3 3SS

200

100

2x2 2SS

Distance

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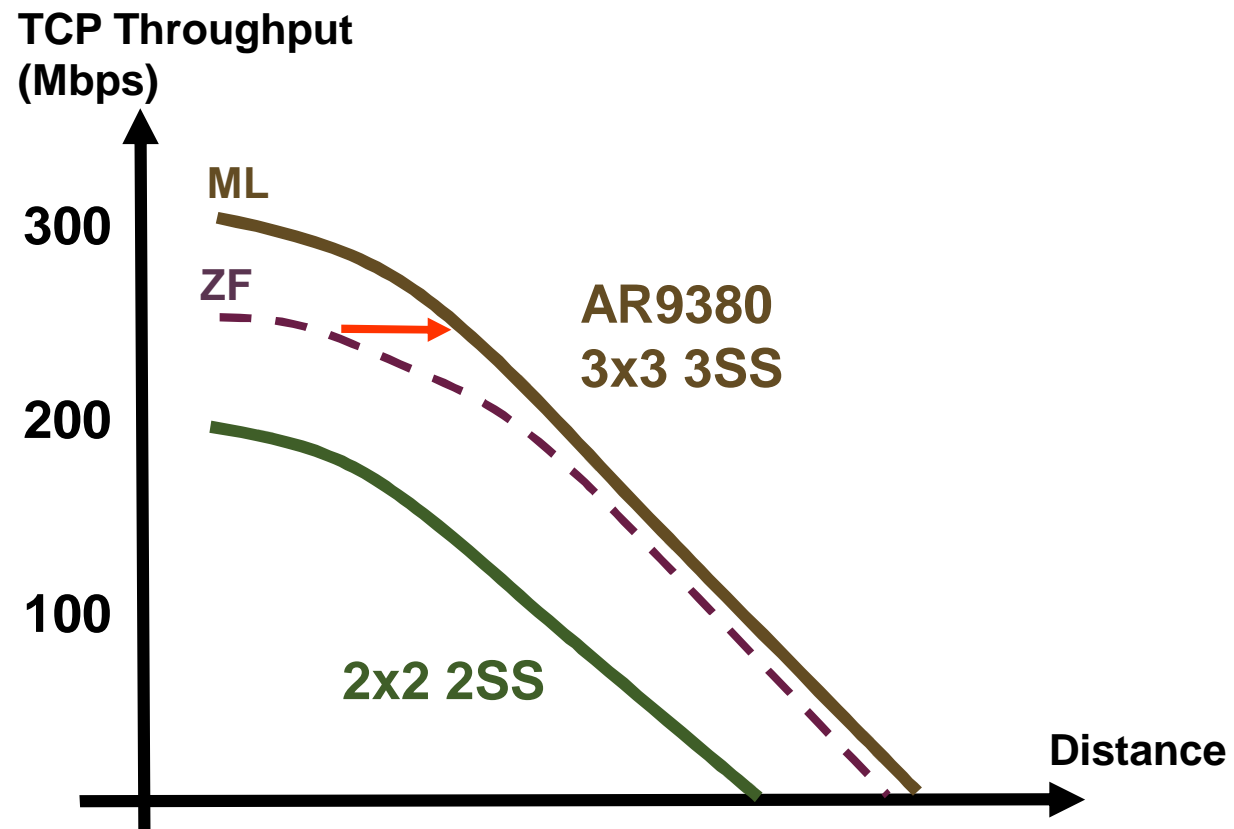
Low Density Parity Check (LDPC) code
Increased data throughput at all range

u**3x3 3SS**

u Convolutional Code (CC)

u**AR9380**

u LDPC code

TCP Throughput (Mbps)

LDPC

CC

AR9380 3x3 3SS

300

200

100

2x2 2SS

Distance

There is Here.

u **2x2 2SS**

u 2x MRC

u **AR9380**

u 3x MRC

**TCP Throughput
(Mbps)**

300

200

100

**AR9380
3x3 3SS**

2x2 2SS

+20%

Distance

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TCP Throughput (w/ 11% collision), Channel D, HT40, 32 A-MPDUs

There is Here.™

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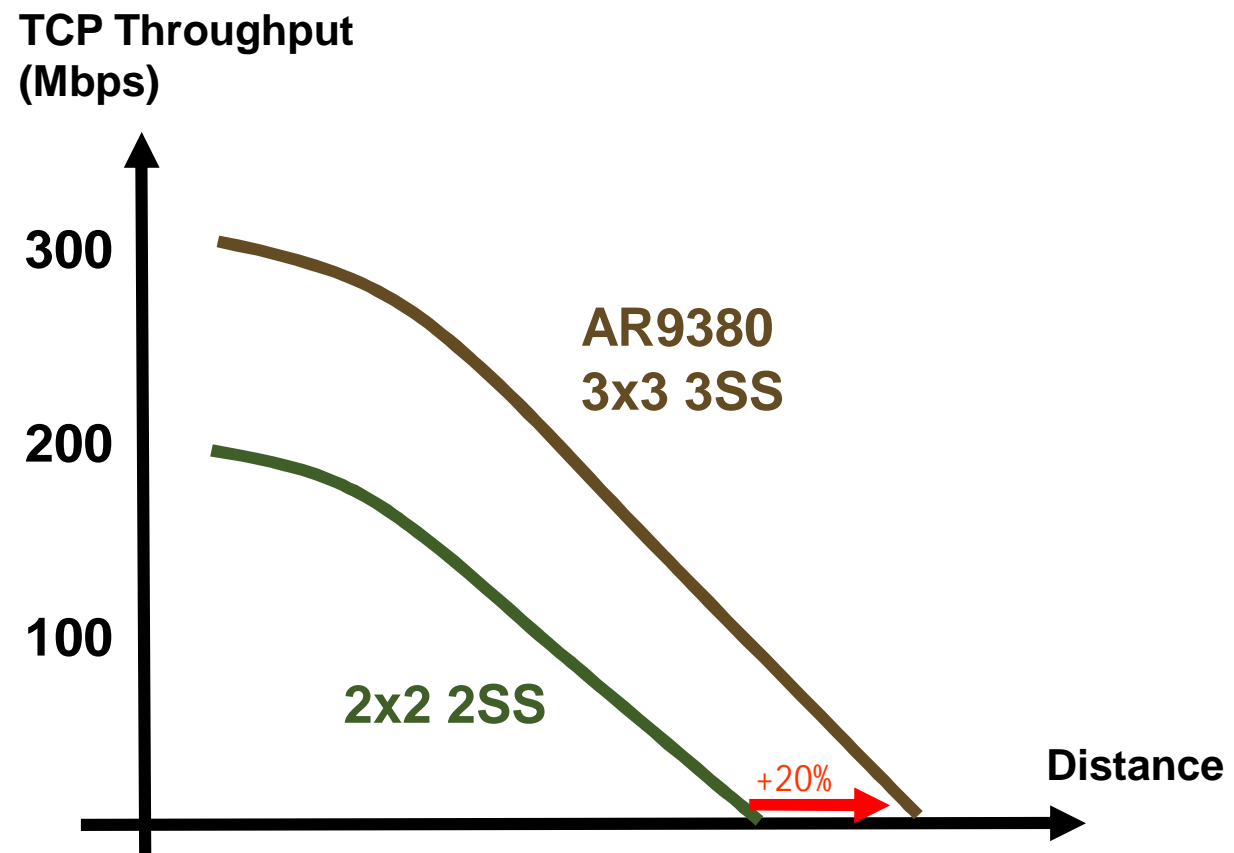
Atheros' latest 11n radio does not just integrate external components to minimize the board complexity and to reduce cost. All integrated components have better performance than previous external parts.

HB92 based on AR9280

AR9380

2GHz PA

PA

Switching Regulator

EEPROM

There is Here.
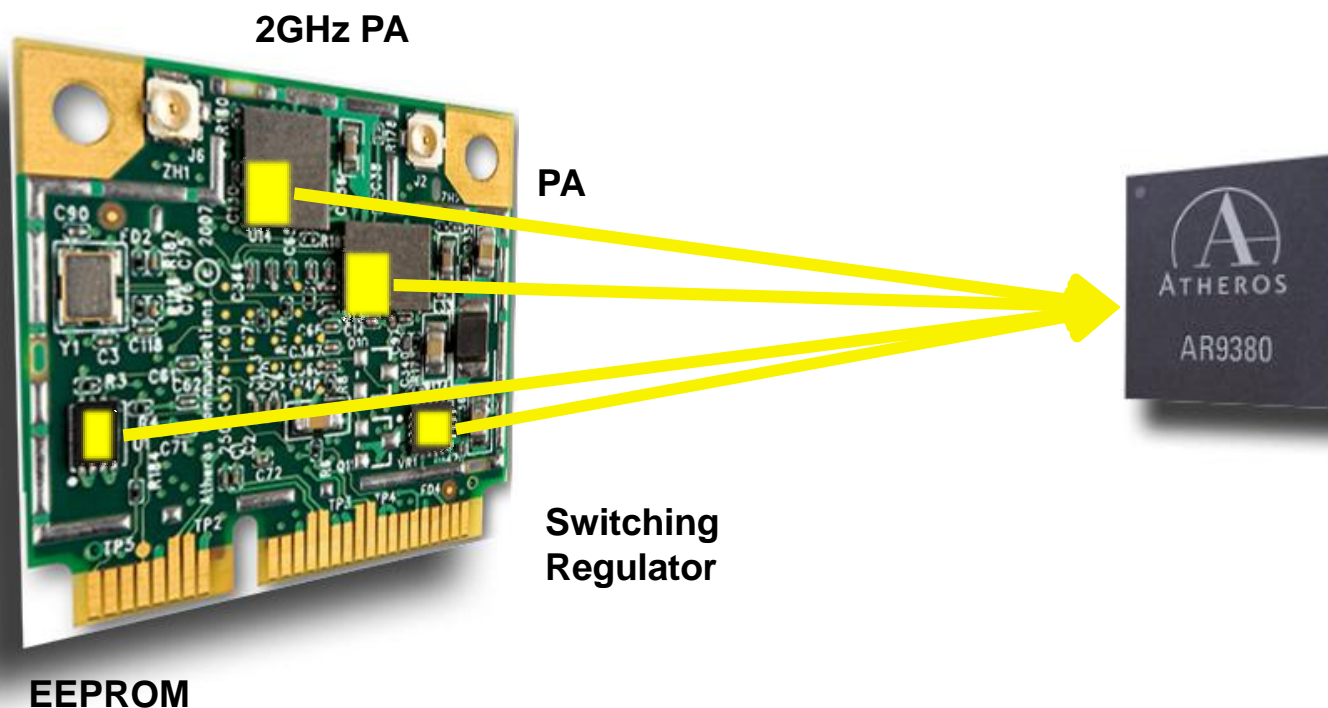
XB112 Measured Performance

Subject	Latest Result
OTA TCP throughput	280Mbps
Cabled TCP throughput	290Mbps
OTA UDP throughput	320Mbps
Cabled UDP throughput	340Mbps
Transmit Power Consumption	3.3w
Receive Power Consumption	782mw
Idle-associated power consumption	35mw
Max Total Tx Power per chain @ 2GHz	18dBm
Max Total Tx Power per chain@ 5GHz	13dBm

Wasp AR934x – 11n 2x2 SOC

AR934x (Wasp) Diagram

SOC

- On-Chip CPU-boost SRAM
- Asynchronous CPU/DDR/AHB clock boundaries
- On-the-fly clock change for CPU/DDR/AHB domains

WLAN

- Enhanced MAC & BB HW Architecture streamline CPU efficiency for 1SS/2SS 11n traffic
- Advanced Optional 11n Features increase range/coverage & accelerate throughput w/o CPU overhead
  - Tx Beamforming
  - LDPC, MLD, MRC CCK

2x2 DB SOC

NOR / NAND Flash	On-Chip CPU	PCIE-RC
SDR/DDR1/2		2x2 DB MAC/BB Radio STBC, LDPC, TxBF, ML, MRC
USB2.0 Host or Device	64KB I-Cache 32KB D-Cache	
I2S/SPDIF/SLIC	Boot ROM / OTP	Internal PA / LNA (Opt xPA/LNA)
PCIE-EP	HW Acceleration Engines	
UART JTAG, GPIOs		Opt'l Antenna Diversity
MII / RMII /. RGMII	4+1 FE Switch + PHYs	Power Mgmt
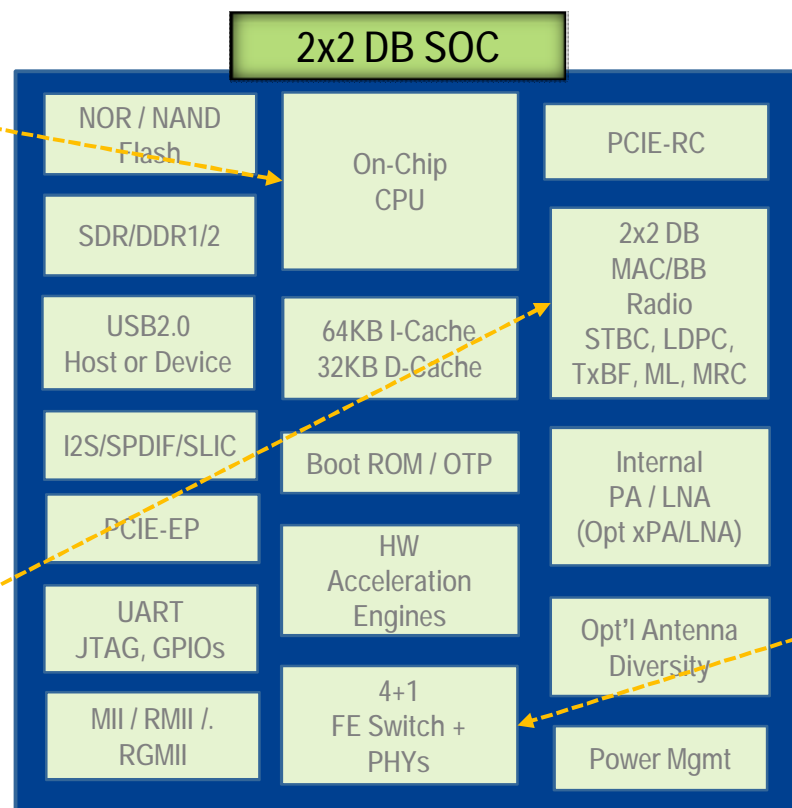
Ethernet/WLAN

- L2 Lookup Engine
  - 32-entry pseudo-CAM engine
  - 48-bit key field & 8-bit data field
- Ingress TCP/UDP Checksum Engine
  - Auto-computation of TCP & UDP Checksum on Ingress at WAN port
- Segmentation/de-segmentation & fragmentation/de-fragmentation
  - Separate HW accelerators for seg'n, deseg'n, frag'n, defrag'n
  - If NAT frag'n support disabled, HW supports up to 96 p-CAM entries
- HW NAT Engine
  - 512-entry deep NAT accelerators for both ingress & egress traffic on WAN port
- HW ACL Engine
  - 64-entry deep high-configurable ACL engine for both ingress & egress traffic on WAN port
- HW Firewall Accelerator

There is Here.

AR934x Product Family & Features

SOC Part Numbers
§AR9341
§AR9342
§AR9344
§AR7360
§AR7370

Schedule
§Sampling Now
§Production Q1'11

Features At-a-Glance

§ 2x2 11n Dual-Band AP-SOC

§ Integrated 2.4GHz & 5GHz RFFE (PAs & LNAs)

§ Advanced 11n features: LDPC, TxBF, MRC-CCK, ML

§ MIPS 74K CPU (up to 600MHz)

§ 64KB I-cache, 32KB D-cache

§ SDR/DDR1/DDR2 DRAM

§ SPI NOR flash & NAND flash support

§ OTP & host boot ROM

§ S17 Ethernet switch (4+1 ports)

§ NAT, ACL, FW HW acceleration, IPv4 & IPv6

§ HW accelerator for AES, WAPI, TKIP

§ USB 2.0 OTG (1)

§ PCI, PCIE-RC, MII, RMII, RGMII

§ I2S/SPDIF/SLIC with audio PLL

§ Advanced power management

§ 2/8 small-OS memory footprint Linux & eCos

§ Most designs require no heat-sinks & no shields

§ Asynchronous CPU / memory boundary

§ Advanced AP sleep modes (MIMO-PS …)

§ Clock dithering - spread-spectrum on memory clock for EMI

There is Here.

Wifi 11n 2x2 AP & Full-Offload SOC Solutions

Target Segment	2x2 SB AP or Router	2x2 DB Basic Gateway/Router	2x2 DB Premium Gateway/Router
Part Number	AR9341	AR9342	AR9344
CPU	MIPS 74K 400MHz	MIPS 74K 550MHz	MIPS 74K 550MHz
Memory Sub-system	SDR/DDR1/2	SDR/DDR1/2	SDR/DDR1/2
Boot	NOR flash	NOR / ext Host	NOR / ext Host / NAND
WLAN Sub-system	2x2 SB	2x2 DB	2x2 DB
	Int PAs, LNAs	Int PAs, LNAs	Int PAs, LNAs
	Opt'l xPA/LNA	Opt'l xPA/LNA	Opt'l xPA/LNA
Ethernet Sub-system	4+1 FE	0 FE	4+1 FE
	Configurable WAN port	xMII	xMII Config WAN port
PCIE		PCIE-EP or RC (1)	PCIE-EP & RC (2)
USB	2.0 Host/Device	2.0 Host/Device	2.0 Host/Device
Audio & Peripherals	I2S, SPDIF, GPIOs, UART, JTAG	I2S, SPDIF, GPIOs, UART, JTAG	I2S, SPDIF, GPIOs, UART, JTAG
VoIP	PCM/SLIC i/f	PCM/SLIC i/f	SLIC/PCM i/f
Power Management	Integrated	Integrated	Integrated
Package	148 DRQFN	148 DRQFN	288 BGA

There is Here.

Wifi 11n High-Performance NPUs & Enterprise Solutions

Target Segment	High-Performance NPU	High-Performance NPU w/ NAND	2x2 DB SOC for Enterprise
Part Number	**AR7360**	**AR7370**	**AR9350**
CPU	MIPS 74K 550MHz	MIPS 74K 550MHz	MIPS 74K 550MHz
Memory Sub-system	SDR/DDR1/2	SDR/DDR1/2	SDR/DDR1/2
Boot	NOR / ext Host	NOR / ext Host / NAND	NOR / ext Host / NAND
WLAN Sub-system	None	None	2x2 DB
			Int PAs, LNAs
			Opt'l xPA/LNA
Advanced Features for Enterprise	N	N	Y
Ethernet Sub-system	xMII	4+1 FE	4+1 FE
		xMII	xMII
		Config WAN port	Config WAN port
PCIE	PCIE-EP or RC	PCIE-EP & RC (2)	PCIE-EP & RC (2)
USB	2.0 Host/Device	2.0 Host/Device	2.0 Host/Device
Audio & Peripherals	I2S, SPDIF, GPIOs, UART, JTAG	I2S, SPDIF, GPIOs, UART, JTAG	I2S, SPDIF, GPIOs, UART, JTAG
VoIP	PCM/SLIC i/f	PCM/SLIC i/f	PCM/SLIC i/f
Power Management	Integrated	Integrated	Integrated
Package	148 DRQFN	288 BGA	288 BGA

There is Here.

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Ethernet Wireless Router

11n 2x2 FE Platform

11n 2x2 GbE or 2x2 + 3x3 DBDC GbE
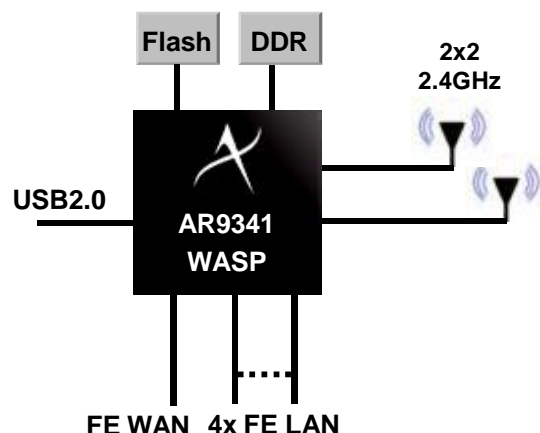
Features
§ Single-chip 2x2 FE router platform
§ High-level integration à cost-effective RBOM
§ MIPS74K CPU
§ Int. PA/LNA
§ USB 2.0
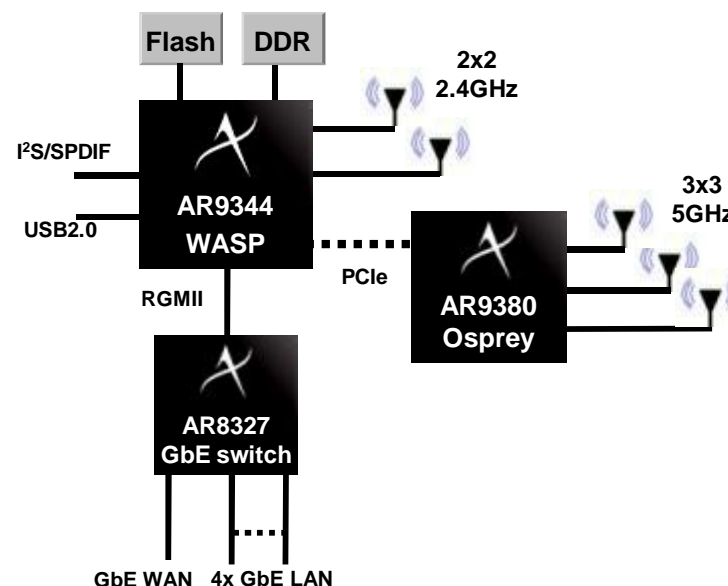
Features
§ Single board design for two different SKUs
§ 2x2 SB Gigabit platform
§ 2x2 + 3x3 DBDC Gigabit platform
§ AR9380 (3x3 DB) and AR9382 (2x2 DB) are pin-compatible
§ CPU frequency – 550+MHz (MIPS74K)
§ Int. PA/LNA
§ USB 2.0

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AR934x in Carrier Gateways

11n 2x2 DB Direct Attach

Features
§ Full-offload single-chip 11n 2x2
§ MIPS74K CPU
§ 2x2 dual-band
§ Int. PA/LNA
§ USB2.0, PCIe , xMII

Target Market
§ DB xDSL/Cable gateway
§ IPTV Set-top Box
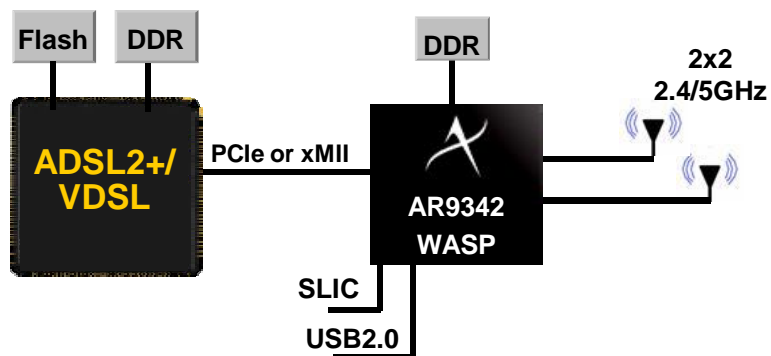
11n 2x2 GbE or 2x2 + 2x2/3x3 DBDC GbE

Features
§ Full-offload DBDC solution
§ CPU Frequency – 550+MHz (MIPS74K)
§ 2x2+2x2/3x3 Dual-Concurrent
§ Int. PA/LNA
§ USB2.0

Target Market
§ DBDC xDSL/Cable gateway
§ Video gateway

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Wasp Reference Designs

There is Here.

DB120

AR9344 / AR7370

AR938x
2x2 / 3x3 DB

PCIE Connector to WLAN Radio

NAND

NOR

DDR2 DRAM

NOR / NAND Flash	MIPS R74K CPU ~600MHz	PCIE-RC
SDR/DDR1/2		2x2 Dual-Band MAC/Baseband & Radio
USB2.0 Host or Device	64KB I-Cache 32KB D-Cache	Integrated 2.4/5GHz PAs & LNAs (Optional xPA/LNA)
I2S/SPDIF/SLIC	Boot ROM & On-Chip Cal	
PCIE-EP	HW Acceleration Engines	Range & Robustness STBC, LDPC, TxBF, MLD, MRC
UART JTAG, GPIOs		
MII / RMII / RGMII	4+1 FE Switch + PHYs	Power Mgmt

USB Host or Device

Connect to Host CPU via USB, xMII, or PCIE

AR8316,17/S17
4+1 GbE Switch

a b g **WiFi** n
CERTIFIED®

dual stream n

Flexible Development Platform for:

Carrier WiFi-Enabled Gateway

ʊ *xMII, PCIE, or USB interface to Host CPU in Embedded Platform*

ʊ *2x2 Single-Band , 2x2 Dual-Band Switchable , and 2x2+2x2/3x3 Dual-Band Concurrent*

WiFi+PLC Solutions

ʊ *Full-Offload 2x2 DB Plus PLC*

A

Interface to External Host CPU

AR9344

PCIE to 2nd Radio

USB 4+1 GbE 4+1 FE
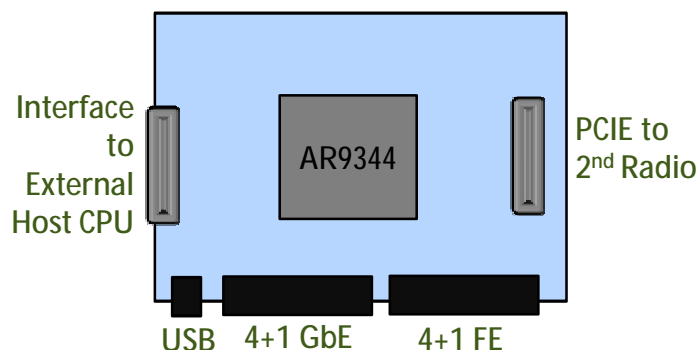
(A) Possible Configurations:
- 2x2 SB FE
- 2x2 DB FE
- 2x2 SB GbE
- 2x2 DB GbE

+

B

AR938x
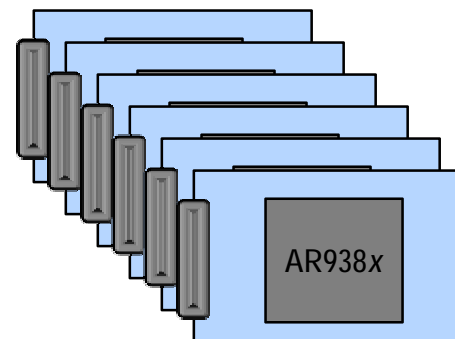
(A+B) Possible Configurations:
- + HB116: 2x2+2x2 DBDC with Normal Power
- + XB112: 2x2+3x3 DBDC with Normal Power
- + XB113: 2x2+3x3 DBDC with High Power
- All can be either FE or GbE

- *All configurations leverage common PCB & SW & all footprint-compatible Atheros solutions*
- *All configurations can support USB 2.0 Host & Device, NAND flash for Boot or Storage, & boot from external Host CPU via USB, xMII, or PCIE*

There is Here.

Reference Design MI124:
2x2 DB (2.4GHz or 5GHz) Full-Offload iNIC

ATHEROS

MI124

a b g **Wi Fi** n
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dual stream n

AR9342

Flash	SPI (NOR Flash)	MIPS R74K CPU ~600MHz	PCIE-RC or EP
DRAM	SDR/DDR1/2		2x2 Dual-Band MAC/Baseband & Radio
	I2S/SPDIF/SLIC	64KB I-Cache 32KB D-Cache	
USB	USB2.0 Host or Device	Boot ROM & On-Chip Cal	Integrated 2.4/5GHz PAs & LNAs (Optional xPA/LNA)
	UART JTAG, GPIOs	HW Acceleration Engines	Range & Robustness *STBC, LDPC, TxBF, MLD, MRC*
	MII / RMII / RGMII	Power Mgmt	

Optional USB Interface to Host CPU

xMII Interface to Host CPU

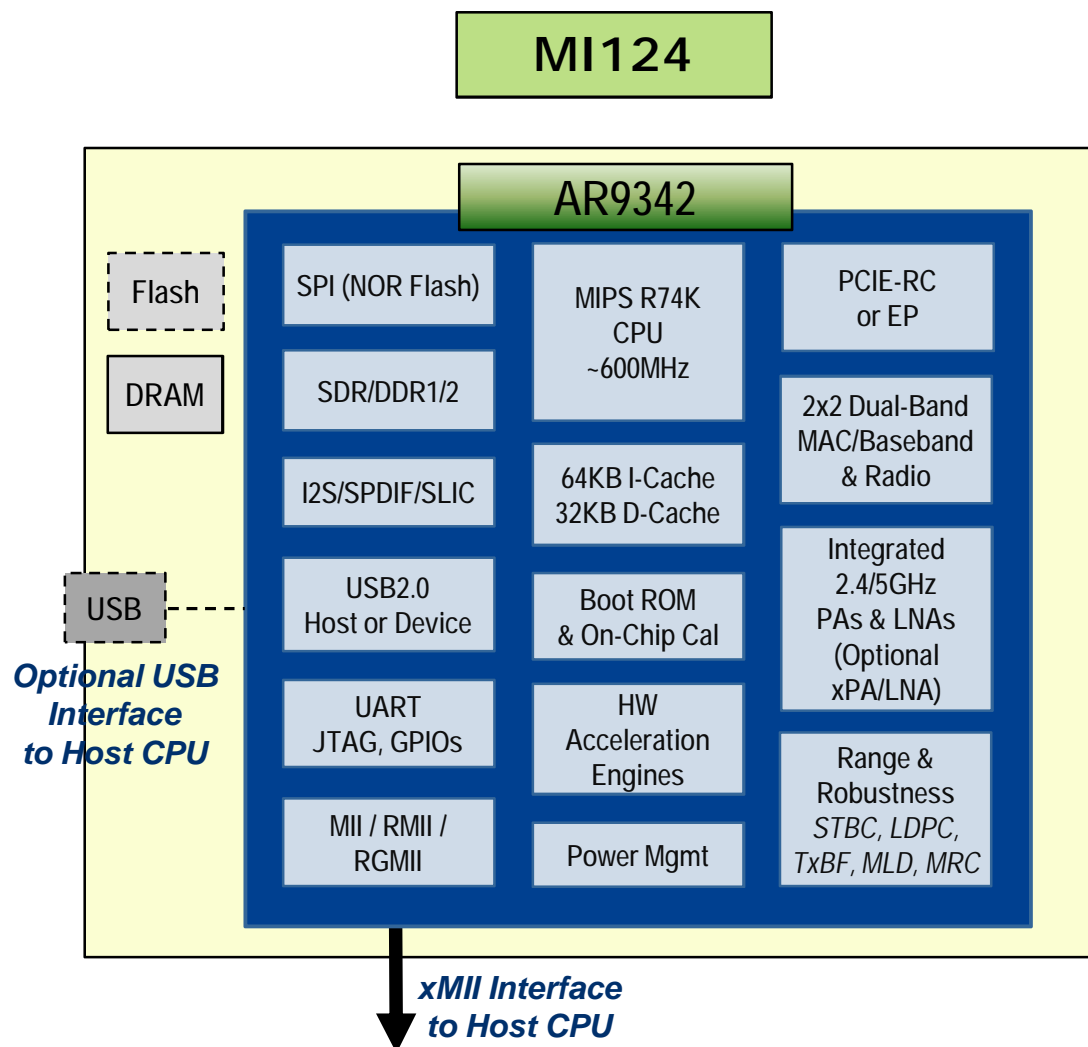**« *World's Most Cost-Effective 2x2 Dual-Band Full-Offload iNIC* «**

- Form-factor ~ 4cm x 4.5cm
- Wifi Mode AP or Full-Offload Client
- Embeddable in Carrier or CE platform
- Host CPU Interface via USB, PCIE, xMII
- Flash-less boot
- 4-Layer PCB
- OS Linux, eCos, others
- Memory Footprint 8 or 16MB DRAM, optional Flash
- Antennas external
- RF Front-End: xPA for optimal range performance (internal LNA)
- Power Consumption Compliant to EU CoC

There is Here.
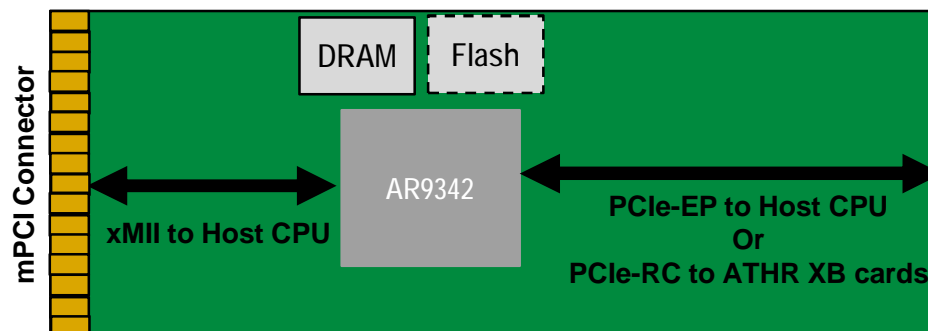
Configuration 1: CM Gateway, Repeater (DB)

Puma-5 — AR8317 — *RGMII* — AR9342
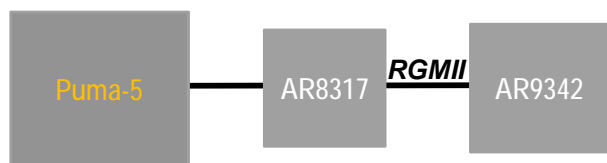
Configuration 2: CM Gateway (DBDC)

Puma-5 — AR8317 — *RGMII* — AR9344 — *PCIe* — AR9382/AR9380

Configuration 3: xDSL Gateway (DB)

VRX288 — *PCIe* — AR9342

ATHEROS

UB124

Ultra small form-factor 2x2 DB USB Dongle/Embedded

abg **WiFi** n
CERTIFIED®

dual stream n

AR9342

SPI (NOR Flash)	MIPS R74K CPU ~600MHz	PCIE-RC or EP
SDR/DDR1/2		2x2 Dual-Band MAC/Baseband & Radio
I2S/SPDIF/SLIC	64KB I-Cache 32KB D-Cache	Integrated 2.4/5GHz PAs & LNAs (Optional xPA/LNA)
USB2.0 Host or Device	Boot ROM & On-Chip Cal	
UART JTAG, GPIOs	HW Acceleration Engines	Range & Robustness *STBC, LDPC, TxBF, MLD, MRC*
MII / RMII / RGMII	Power Mgmt	

Flash

DRAM

USB Interface to Host CPU
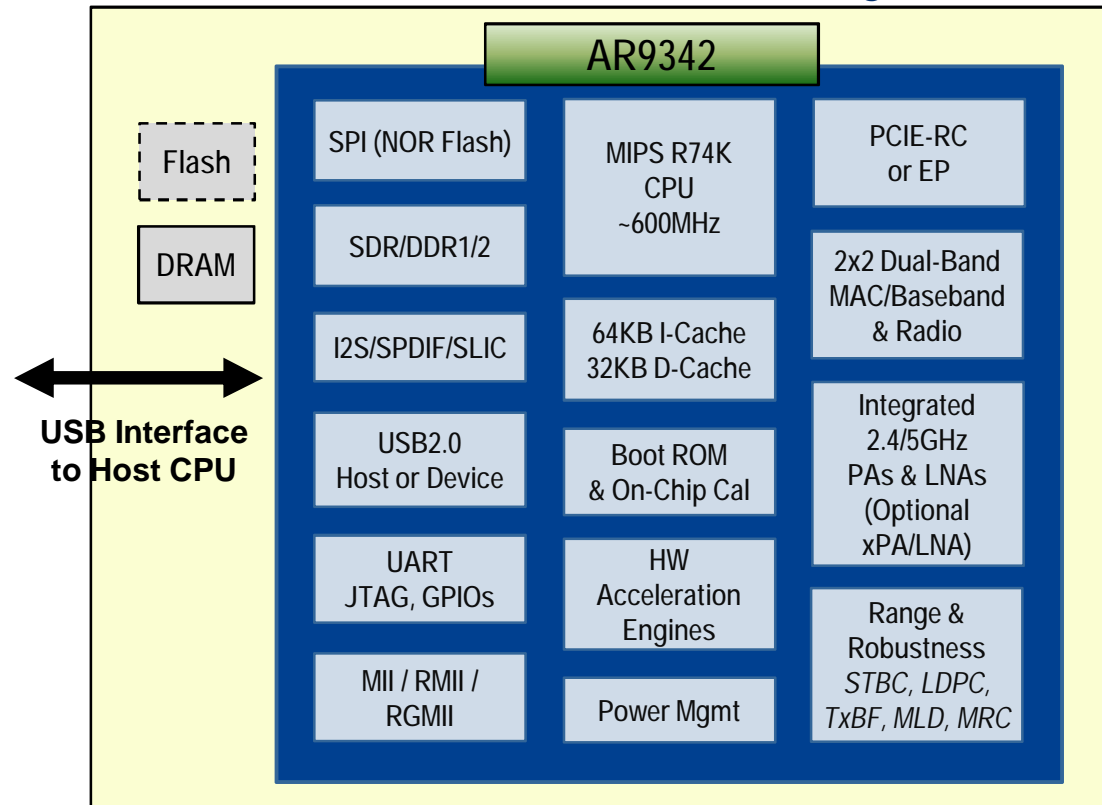
« *World's Most Cost-Effective 2x2 Dual-Band Full-Offload USB AP or Client* «
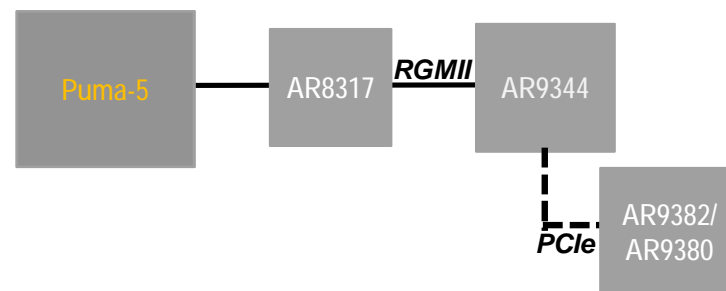
- Form-factor: ~ 4cmx4cm
- 2-Layer PCB
- OS: Linux, eCos
- Wifi Mode AP or Full-Offload Client
- Embeddable in Carrier or CE platform Memory Footprint: Target 1/4 or less
- Antennas: printed, stamped, or external
- Optional: xPA, xLNA
- Fully USB Spec Compliant Host or Client
- Power Consumption: <2.5W average, <12.5mW USB-suspend
- Full compliance to USB spec

There is Here.™

Hornet AR933x – 11n 1x1 SOC

Wifi 11n 1x1 AP & Full-Offload SOC Solutions

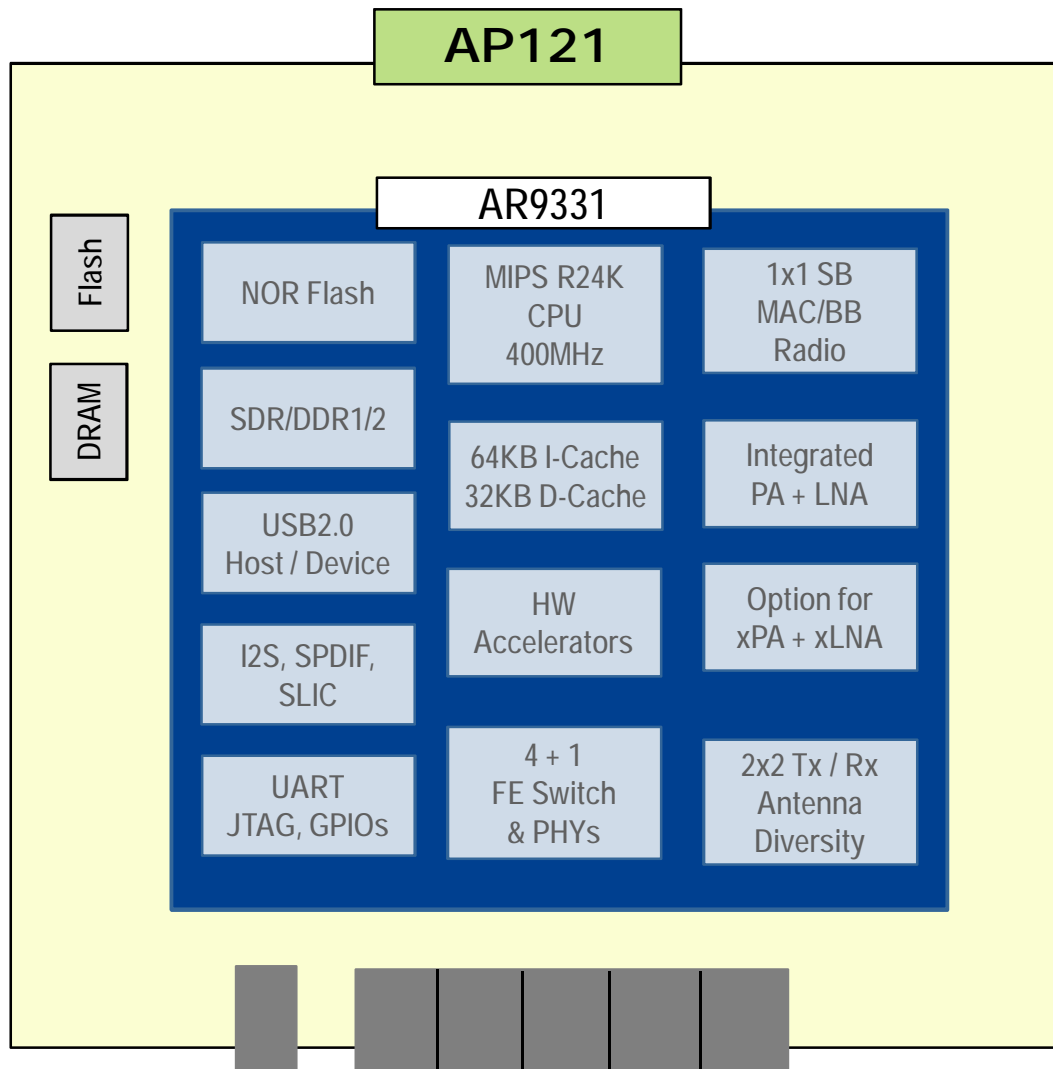| Target Segment	1x1 SB AP or Router	1x1 SB USB& Embedded
Part Number	AR9331	AR9333
CPU	MIPS 24K 400MHz	MIPS 24K 400MHz
Memory Sub-system	SDR/DDR1/2	SDR/DDR1/2
Boot	NOR flash	NOR / ext Host
WLAN Sub-system	1x1 SB	1x1 SB
	Int PAs, LNAs	Int PAs, LNAs
	Opt'l xPA/LNA Antenna Diversity	Opt'l xPA/LNA Antenna Diversity
Ethernet Sub-system	4+1 FE	4 FE
	Configurable WAN port	xMII
USB	2.0 Host/Device	2.0 Host/Device
Audio & Peripherals	I2S, SPDIF, GPIOs, UART, JTAG	I2S, SPDIF, GPIOs, UART, JTAG
VoIP	PCM/SLIC i/f	PCM/SLIC i/f
Power Management	Integrated	Integrated
Package	148 DRQFN	148 DRQFN

There is Here.

Hornet Reference Designs

There is Here.

AP121

AR9331

NOR Flash	MIPS R24K CPU 400MHz	1x1 SB MAC/BB Radio
SDR/DDR1/2	64KB I-Cache 32KB D-Cache	Integrated PA + LNA
USB2.0 Host / Device	HW Accelerators	Option for xPA + xLNA
I2S, SPDIF, SLIC		
UART JTAG, GPIOs	4 + 1 FE Switch & PHYs	2x2 Tx / Rx Antenna Diversity

Flash

DRAM

align ™
ATHEROS

« Single-*Chip Solution for Complete High-Performance 1x1 SB Router* «

ս **Small Form-factor**: 10cm x 8cm

ս **2-Layer PCB**

ս **OS**: Linux, eCos

ս **Memory Footprint**: 2/8

ս **Antennas**: printed, stamped, or external

ս **Optional**: xPA, xLNA, antenna diversity, USB 2.0 Host, I2S/SPDIF for audio, SLIC/PCM for VOIP

ս **Power Supply**: 5v/1a

ս **Peak Power**: <2.5W

ս **Idle Power**: < 0.8W

ս **RBOM / PCBA**: Industry's lowest

UB121

Ultra small form-factor 1x1 USB Dongle/Embedded

align
ATHEROS

AR9333

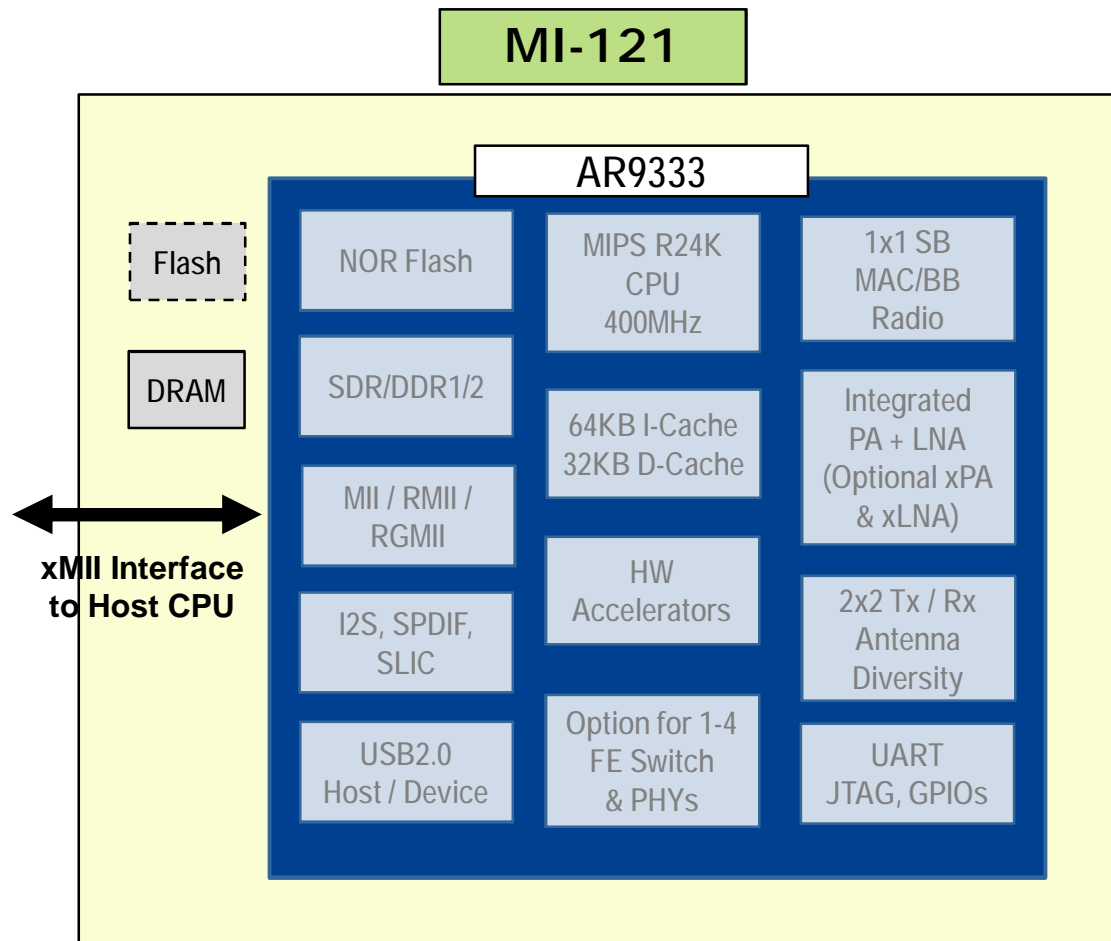| Flash	SPI Interface	MIPS R24K CPU 400MHz	1x1 SB MAC/BB Radio
DRAM	SDR/DDR1/2	64KB I-Cache 32KB D-Cache	Integrated PA + LNA (Optional xPA & xLNA)
	xMII	HW Accelerators	2x2 via Tx / Rx Antenna Diversity
USB Interface to Host CPU	USB2.0 Device		
	I2S, SPDIF, SLIC	Optional1-4 FE *(Available/ Not Populated)*	UART JTAG, GPIOs
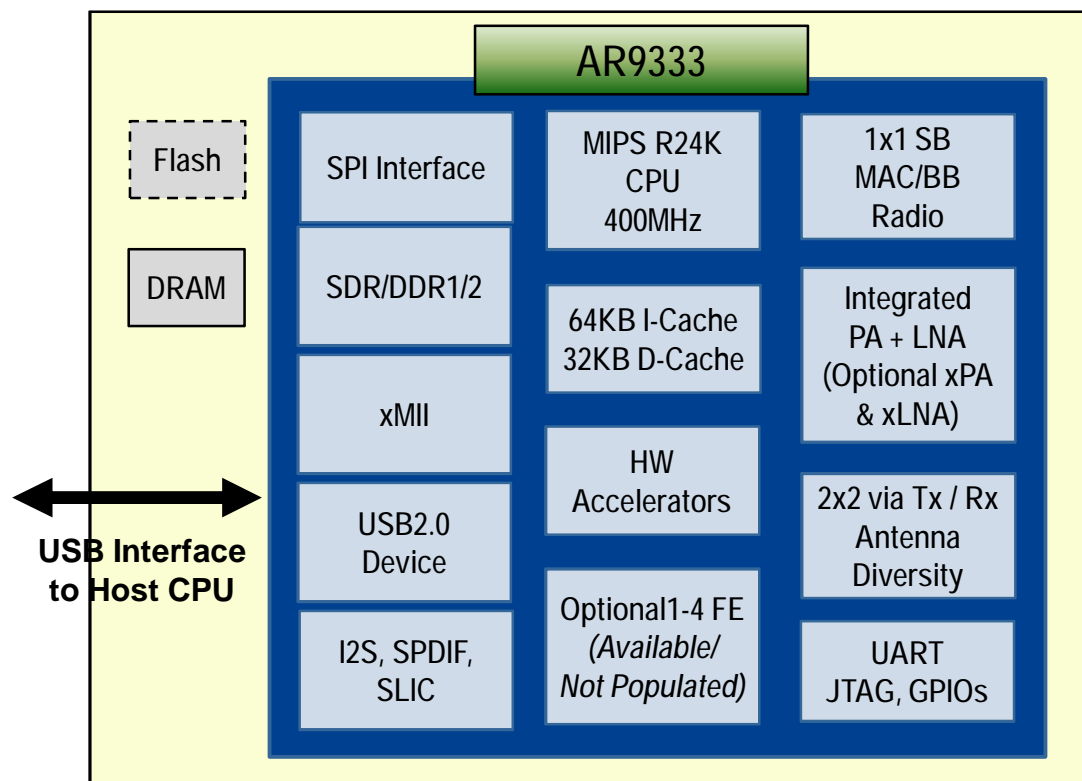
« *World's Most Cost-Effective 1x1 Full-Offload Client* »

u <u>Form-factor</u>: 2cm x 6cm

u 4-Layer PCB

u <u>OS</u>: Linux

u <u>Memory Footprint</u>: optional flash, SDRAM or DDR1, small memory footprint

u <u>Antennas</u>: printed, stamped, or external

u <u>Optional</u>: xPA, xLNA, & antenna diversity

u <u>Fully USB Spec Compliant</u>

u <u>Power Consumption</u>: <2.5W average, <12.5mW suspend

MI-121

align
ATHEROS

AR9333

NOR Flash	MIPS R24K CPU 400MHz	1x1 SB MAC/BB Radio
SDR/DDR1/2	64KB I-Cache 32KB D-Cache	Integrated PA + LNA (Optional xPA & xLNA)
MII / RMII / RGMII	HW Accelerators	2x2 Tx / Rx Antenna Diversity
I2S, SPDIF, SLIC		
USB2.0 Host / Device	Option for 1-4 FE Switch & PHYs	UART JTAG, GPIOs

Flash

DRAM

xMII Interface to Host CPU

« *Low-Cost 1x1 WiFi Connectivity for xMII Embedded Applications* «

- u Form-factor: Standard MB, to be verified with PB47
- u OS: Linux
- u Memory Footprint: 2MB or 8MB SDRAM, optional Flash
- u Antennas: printed, stamped, dipole
- u Optional: xPA, xLNA, antenna diversity
- u Power Supply:
- u Peak Power: < 2.5W
- u Idle Power: < 0.9W

Thank YOU!