April 2011

AR7242: A High Performance And Cost-Effective Network Processor

General Description

The Atheros AR7242 is a high performance and cost effective network processor for access point, router, and gateway applications. It includes a MIPS 24Kc processor, PCI Express 1.1 host interface, integrated 10/100 Mbps Fast Ethernet MAC/PHY, one RGMII port, one USB 2.0 MAC/PHY, and external memory interface for serial Flash, DDR1 or DDR2 interface, an I^2S audio interface, a high-speed UART, and GPIOs that can be used for LED controls or other general purpose interface configurations.

The AR7242 is a memory-centric architecture including various DMA controlled interfaces that access the DDR memory.

The AR7242 network processor, when paired with the AR928x/AR938x/AR939x single chip 802.11n MAC/BB/Radio family, provides the best-in-class WLAN solution capable of supporting 802.11b/g/n standards.

Features

- Integrated MIPS 24 K 32-bit processor operating at up to 400 MHz
- 64 K instruction cache and 32 K data cache
- Integrated 10/100 802.3 Ethernet LAN port and one RGMII port
- 16-bit DDR1 or DDR2 memory interface supporting up to 400 M transfers per second
- An external serial Flash memory interface (maximum 16 MBytes)
- One USB 2.0 controller with built-in MAC/PHY
- High-speed UART and multiple GPIO pins for general purpose I/O or LED control
- A single lane PCI Express 1.1 interface that can be used for interfacing to the AR928x/AR938x/AR939x single chip 802.11n MAC/BB/Radio
- JTAG port support for processor core
- 14 mm x 14 mm 128-pin LQFP lead-free package

System Block Diagram

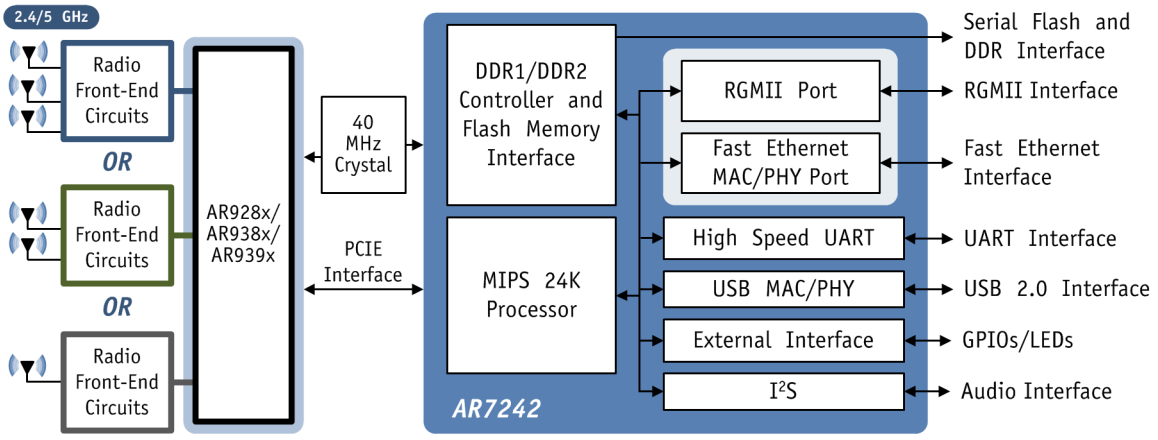

Table of Contents

1. Pin Descriptions

This section contains a package pinout (see Figure 1-1 and Table 1-2) and a tabular listing of the signal descriptions.

This nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

This nomenclature is used for signal types:

I	Digital input signal
I/O	A digital bidirectional signal
IA	Analog input signal
IA/OA	Analog bidirectional signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
O	A digital output signal
OA	An analog output signal
OD	A digital output signal with open drain
P	A power or ground signal

Figure 1-1 shows the LQFP AR7242 pinout.

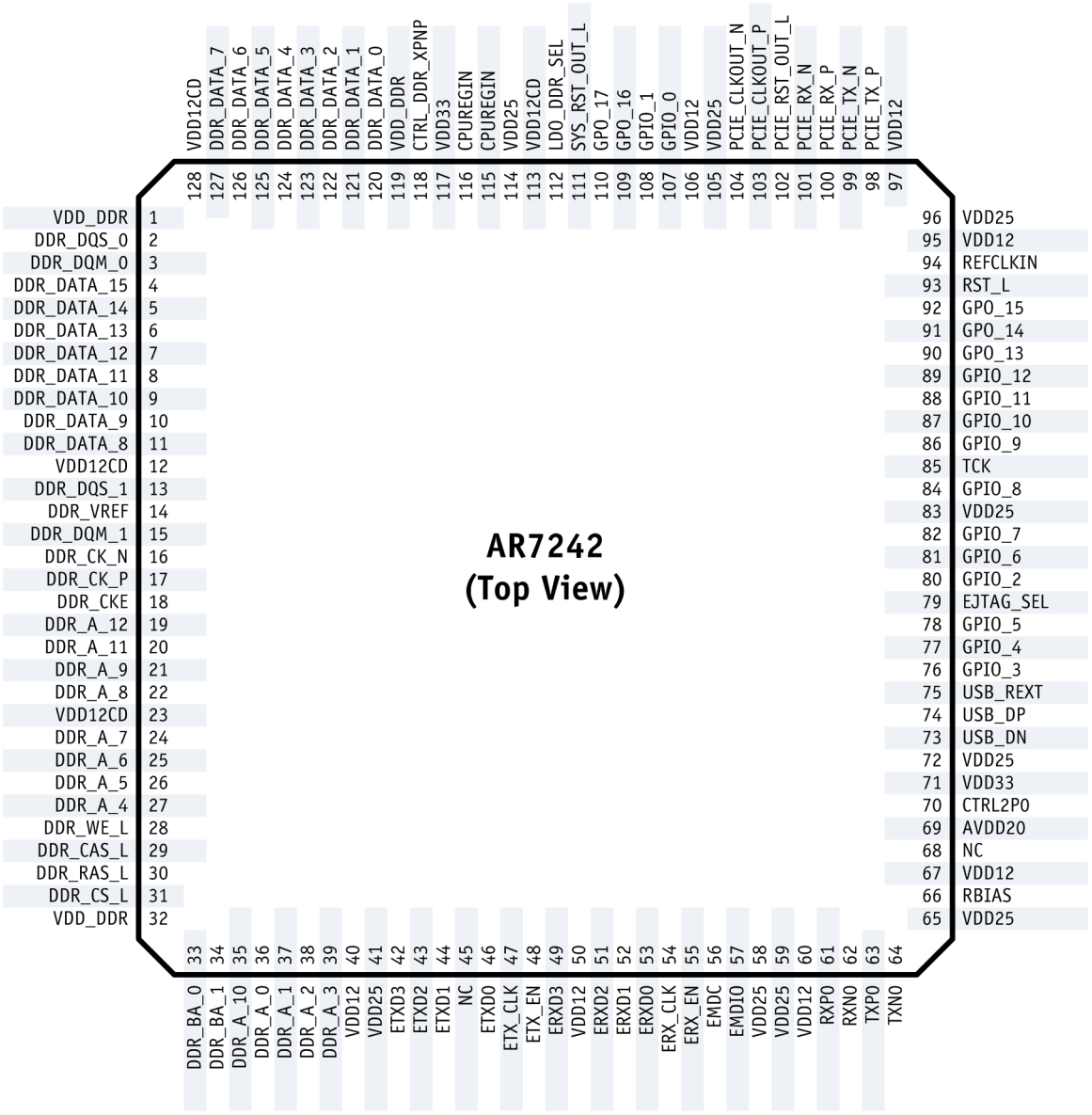

Figure 1-1. **LQFP-128 Package Pinout**

Table 1-1 shows the multiplexed pins for the AR7242,

Table 1-1. **Multiplexed Pins[1][2]**

LQFP-128 Pin	GPIO Pin	EJTAG Pin	LED Pin	SPDIF/I²S Pin	SPI Pin	UART Pin
107	GPIO_0			I2S_WS (FN2, 4)	SPI_CS_EN1 (FN1, 13)	
108	GPIO_1			I2S_CK (FN2, 3)		
80	GPIO_2				SPI_CS_EN0 (FN1, 18)	
76	GPIO_3				SPI_CLK (FN1, 18)	
77	GPIO_4				SPI_MOSI (FN1, 18)	
78	GPIO_5				SPI_MISO (FN1, 18)	
81	GPIO_6	TDI (FN1, 0)		I2S_CK (FN1, 26)		
82	GPIO_7	TDO (FN1, 0)		I2S_WS (FN1, 26)		
84	GPIO_8	TMS (FN1, 0)		I2S_SD (FN1, 26)		
86	GPIO_9					UART_SIN (FN1, 1)
87	GPIO_10					UART_SOUT (FN1, 1)
88	GPIO_11			I2S_MCK (FN1, 26, 27)		UART_RTS (FN1, 2)
	GPIO_12			I2S_MICIN (FN1, 26)		UART_CTS (FN1, 2)
89				I2S_SD (FN2, 5)		
90	GPO_13		LED_0 (FN1, 3)	SPDIF_OUT (FN1, 30)		
91	GPO_14			I2S_SD (FN2, 1)		
92	GPO_15			I2S_WS (FN2, 1)		
109	GPO_16			I2S_CK (FN2, 1)		
110	GPO_17					

[1]Multiplexing of the GPIO pins is controlled by the "GPIO Function (GPIO_FUNCTION_1)" on page 48 and "Extended GPIO Function Control (GPIO_FUNCTION_2)" on page 49.

[2]Notations of (FN*x*, *y*) indicate that the pin is controlled by the particular register and bit. For example, (FN1, 30, 31) indicates the GPIO_FUNCTION_1 register, bit [30] and bit [31], and (FN2, 1) indicates the GPIO_FUNCTION_2 register, bit [1].

Table 1-2. **Signal-to-Pin Relationships and Descriptions**

Symbol	Pin	Type	Description
Reset and Clock			
REFCLKIN	94	I	40 MHz reference clock input, AC coupled, can be sine wave or square wave. An external 100 pF capacitor should connect between REFCLKIN and the clock source. See Table 5-8 and Table 5-9 on page 184 for more information.
RST_L	93	IH	Power on reset with internal weak pull-up. Refer to reference design schematics
SYS_RST_OUT_L	111	OD	System reset out, open drain, pull up is required
PCI Express			
PCIE_CLKOUT_N	104	OA	Differential reference clock (100 MHz)
PCIE_CLKOUT_P	103	OA	
PCIE_RST_OUT_L	102	OD	PCI Express reset, open drain
PCIE_RX_N	101	IA	Differential receive
PCIE_RX_P	100	IA	
PCIE_TX_N	99	OA	Differential transmit
PCIE_TX_P	98	OA	
Serial Interface			
SPI_CLK[1]	76	O	Serial interface clock
SPI_CS_EN0[1]	80	O	SPI chip select
SPI_CS_EN1[1]	107	O	
SPI_CS_EN2[1]	108	O	
SPI_MOSI[1]	77	O	Data transmission from the AR7242 to an external device. On reset, SPI_MISO (GPIO_5) is input and SPI_MOSI (GPIO_4) is output so it can directly interface with a SPI device such as a serial flash. If a serial flash is not used, these pins may be used as GPIO pins.
SPI_MISO[1]	78	IL	Data transmission from an external device to the AR7242. On reset, SPI_MISO (GPIO_5) is input and SPI_MOSI (GPIO_4) is output so that it can directly interface with a SPI device such as a serial flash. If a serial flash is not used, these pins may be used as GPIO pins.
USB			
USB_DM	73	A	USB 2.0
USB_DP	74	A	USB 2.0
USB_REXT	75	A	USB 2.0
UART			
UART_CTS[1]	89	I	UART clear to send signal
UART_RTS[1]	88	O	UART ready to send signal (optional UART interface pin)
UART_SIN[1]	86	I	Serial data in
UART_SOUT[1]	87	O	Serial data out

Table 1-2. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
DDR			
DDR_A_0	36	O	DDR address
DDR_A_1	37	O	
DDR_A_2	38	O	
DDR_A_3	39	O	
DDR_A_4	27	O	
DDR_A_5	26	O	
DDR_A_6	25	O	
DDR_A_7	24	O	
DDR_A_8	22	O	
DDR_A_9	21	O	
DDR_A_10	35	O	
DDR_A_11	20	O	
DDR_A_12	19	O	
DDR_BA_0	33	O	DDR bank address
DDR_BA_1	34	O	
DDR_CS_L	31	O	DDR chip select
DDR_CK_N	16	O	DDR clock
DDR_CK_P	17	O	
DDR_CKE	18	O	DDR clock enable
DDR_DATA_0	120	I/O	DDR data bus
DDR_DATA_1	121	I/O	
DDR_DATA_2	122	I/O	
DDR_DATA_3	123	I/O	
DDR_DATA_4	124	I/O	
DDR_DATA_5	125	I/O	
DDR_DATA_6	126	I/O	
DDR_DATA_7	127	I/O	
DDR_DATA_8	11	I/O	
DDR_DATA_9	10	I/O	
DDR_DATA_10	9	I/O	
DDR_DATA_11	8	I/O	
DDR_DATA_12	7	I/O	
DDR_DATA_13	6	I/O	
DDR_DATA_14	5	I/O	
DDR_DATA_15	4	I/O	
DDR_DQM_0	3	O	DDR data mask
DDR_DQM_1	15	O	

Table 1-2. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description	
DDR_DQS_0	2	I/O	DDR data strobe In DDR2, both polarity signals need to be driven.	
DDR_DQS_1	13	I/O		
DDR_CAS_L	29	O	DDR column address strobe	
DDR_RAS_L	30	O	DDR row address strobe	
DDR_WE_L	28	O	DDR write enable	
DDR_VREF	14	I	DDR reference level for SSTL signals	
LED				
LED_0[1]	90	OD	If LED0_EN is set, it becomes open drain and provides drive strength of 10 mA	
JTAG				
EJTAG_SEL	79	I	0	JTAG
			1	EJTAG (enhanced JTAG)
TCK	85	I	JTAG/EJTAG clock	
TDI[1]	81	I	JTAG/EJTAG data input	
TDO[1]	82	O	JTAG/EJTAG data output	
TMS[1]	84	I	JTAG/EJTAG mode select	
Ethernet				
RBIAS	66	OA	Connect to 2.37 KΩ resistor to ground	
RXN0	62	IA/OA	Port 0	
RXP0	61	IA/OA		
TXN0	64	IA/OA		
TXP0	63	IA/OA		
GPIO				
GPIO_0[1]	107	I/O	General purpose input/output with drive strength of 2 mA.	
GPIO_1[1]	108	I/O		
GPIO_2[1]	80	I/O		
GPIO_3[1]	76	I/O		
GPIO_4[1]	77	I/O		
GPIO_5[1]	78	I/O		
GPIO_6[1]	81	I/O	GPIO pin multiplexed as TDI by default	
GPIO_7[1]	82	I/O	GPIO pin multiplexed as TDO by default	
GPIO_8[1]	84	I/O	GPIO pin multiplexed as TMS by default	

Table 1-2. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
GPIO_9[1]	86	I/O	General purpose input/output with drive strength of 2 mA
GPIO_10[1]	87	I/O	
GPIO_11[1]	88	I/O	
GPIO_12[1]	89	I/O	
GPO_14[1]	91	O	
GPO_15[1]	92	O	
GPO_16[1]	109	O	
GPO_17[1]	110	O	
Multiplexed Output Pins			
GPO_13[1]	90	O	This pin is intended for driving Ethernet LEDs and cannot be used as input. See the pin descriptions for "LED" on page 14.
I^2S/SPDIF			
I2S_CK[1]	81, 108, 109	O	Stereo clock
I2S_MCK[1]	88	O	Master clock
I2S_MICIN[1]	89	I	Data input
I2S_SD[1]	84, 89, 91	I/O	Serial data input/output
I2S_WS[1]	82, 92, 107	O	Word select for stereo 0 Left 1 Right
SPDIF_OUT[1]	90	O	Speaker output
Regulator Control			
CPUREGIN	115, 116	I	CPU regulator control inputs. Minimum voltage is 1.8 V. A 1 Ω resistor may be used in series between these pins and VDD_DDR pins in DDR1 mode (LDO_DDR_SEL=1).
CTRL_DDR_XPNP	118	OA	External PNP Control. Connect to the base of an external PNP: collector to VDD_DDR and emitter to VDD33.
CTRL2P0	70	OA	External PNP control. Connect to the base of an external PNP: collector to AVDD20 and emitter to VDD33.
LDO_DDR_SEL	112	I	Selects the regulated DDR voltage, see VDD_DDR description 0 DDR2 voltage, 1.8V 1 DDR1 voltage, 2.6 V
RGMII Interface			
EMDC	56	O	Management control interface clock
EMDIO	57	I/O	Management control interface data
ERX_CLK	54	I	Receive clock

Table 1-2. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
ERXD0	53	I	Receive data
ERXD1	52	I	
ERXD2	51	I	
ERXD3	49	I	
ERX_EN	55	I	Receive enable
ETX_CLK	47	O	Transmit clock
ETXD0	46	O	Transmit data
ETXD1	44	O	
ETXD2	43	O	
ETXD3	42	O	
ETX_EN	48	O	Transmit enable

[1]This pin is multiplexed. See Table 1-1.

Symbol	Pin	Description
Power		
AVDD20	69	Regulated 2.0 V from the AR7242; connect to the external PNP collector
VDD_DDR	1, 32, 119	Regulated 2.6 V or 1.8 V output from the AR7242, for DDR1 or DDR2, respectively; connect to the external PNP collector.
VDD12	40, 50, 60, 67, 95, 97, 106	Regulated 1.2 V output from the AR7242
VDD12CD	12, 23, 113, 128	Regulated 1.28 V output from the AR7242; core voltage of CPU/DDR blocks, connect pins 12 and 23 to pins 113 and 128
VDD25	41, 58, 59, 65, 72, 83, 96, 105, 114	Regulated 2.62 V output from the AR7242; I/O voltage
VDD33	71, 117	3.3 V power supply
Ground Pad		
Exposed Ground Pad		Tied to GND (see "Package Dimensions" on page 202)
No Connection		
NC	45, 68	No connection

2. System Architecture

Figure 2-1 illustrates the AR7242 system architecture.

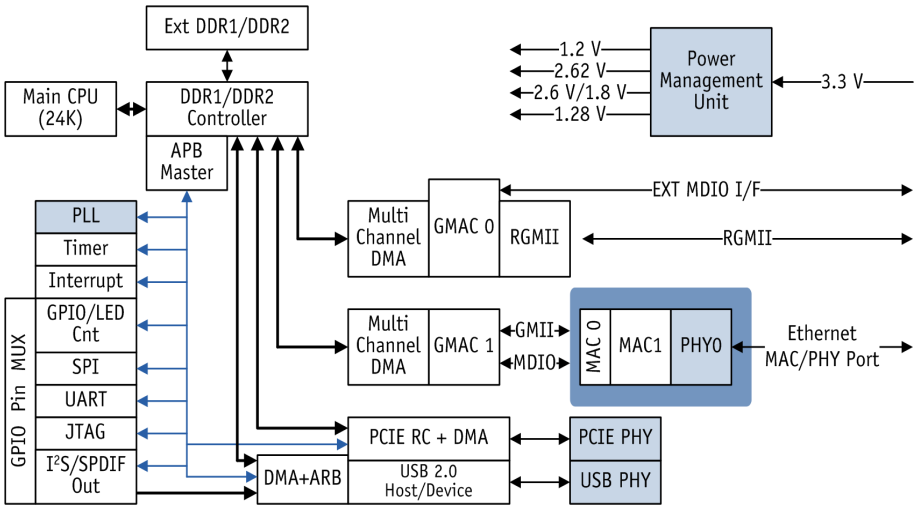

Figure 2-1. **AR7242 Functional Block Diagram**

Table 2-1 summarizes the functional blocks that comprise the AR7242.

Table 2-1. **Functional Block Descriptions**

Block	Description
CPU	This MIPS 24 K processor can run up to 400 MHz. It includes a 64 K 4-way set associative instruction cache, 32 K 4-way set associative data cache, single cycle multiply-accumulate, and MIPS32 and MIPS16 instruction sets. Non-blocking cache reads are also supported. See "MIPS Processor" on page 18.
DDR Memory Controller	The AR7242 supports a 16-bit DDR1/ DDR2 memory interface of up to 400Mbps/pin. It supports one dedicated point-to-point interface for the CPU and similarly dedicated point-to-point interfaces for the USB, Ethernet and PCIE master devices. See "DDR Memory Controller" on page 19.
Ethernet Port/ GMAC	One Ethernet port with integrated MAC/PHY. LED indication for the port is supported. The Ethernet MAC/PHY port connect to the CPU through the GE1 GMII interface, and four Tx queue priorities are supported in the this port. The GMAC connects to the CPU using the GE0 interface. The GMAC also can support up to four priority queues, with either simple priority or a weighted round robin arbitration mechanism.
Bus Bridge	High speed peripheral bus; the APB connects peripherals such as GPIO, UART, and SPI for Flash to the bus bridge. The AHB connects high-performance peripheral interfaces such as the GB Ethernet and USB interfaces to the bus bridge. See "AHB Master Bus" on page 19 and "APB Bridge" on page 19.
GPIO/ GPO	20 multiplexed GPIO/GPO pins that can be used for general purpose controls, SPI, I^2S, SPDIF, UART, and LED. See Table 1-1 on page 11 for GPIO/GPO multiplexing.

Table 2-1. **Functional Block Descriptions (continued)**

I^2S/ SPDIF	AR7242 audio support consists of: ■ I^2S/SPDIF out audio interface that support up to 48 KHz sampling clock and a serial clock of more than 512 * sampling frequency. It also supports seamless switching of the audio out stream from I2S to SPDIF. I2S MIC is also supported. ■ A dedicated audio PLL to generate serial clock for various sampling frequencies. See "Audio Interface" on page 29.
PCIE	The root complex single lane interface can support up to 2.56 Gbps and supports both the message-based and MSI interrupt mechanism.
PLL	The PLL block consists of six PLLs used to generate: ■ A clock for CPU/DDR, tunable from 300 MHz to 400 MHz ■ PLL for 48 MHz reference clock for the USB core and to generate a 25 MHz reference clock for the Ethernet port ■ PCIE 100 MHz clocks with dither support ■ PCIE PHY PLL generates 250 MHz and 2.5 GHz clock for the PCIE interface ■ Ethernet 125 MHz clock generated from a 25 MHz clock ■ Audio PLL to generate the master clock for I^2S/SPDIF out
SPI	SPI interface that can be used for serial Flash
UART	16650 equivalent UART for debug/console
USB	Universal Serial Bus 2.0 interface support

2.1 MIPS Processor

The AR7242 integrates an embedded MIPS 24Kc processor. For complete information on the 24Kc processor, visit: http://www.mips.com/products/cores/32-64-bit-cores/mips32-24k/

Under Processor Cores-24K Family, refer to:

- MIPS32 24Kc Processor Core Datasheet v4.00
- MIPS32 24Kc Processor Core Family Software User's Manual v3.11

2.2 Configuration

Table 2-2 summarizes the configuration settings used by the AR7242. Upon reset, the CPU puts out an address of 0xBFC00000 which is mapped to the flash address space.

The AR7242 processor supports a clock frequency of up to 400 MHz.

Table 2-2. **Core Processor Configuration Settings**

Setting	Description
Cache Size	The AR7242 implements 64 KB 4-way set associative instruction cache and 32 KB four-way set associative data cache. It supports single cycle multiply-accumulate, MIPS32 and MIPS16 instruction sets and non-blocking cached reads.
Endian	The AR7242 implements big Endian addressing.
Block Addressing	The AR7242 implements sequential ordering.

2.3 AR7242 Address MAP

The address space for the AR7242 is divided into two 256 MBytes (MB) regions. The lower region maps to the DDR memory. The upper region maps to the AHB bus bridge. The 512 MBytes decoded region is repeated through the 4 GBytes of the processor's address space. Figure 2-2 shows the address space allocation.

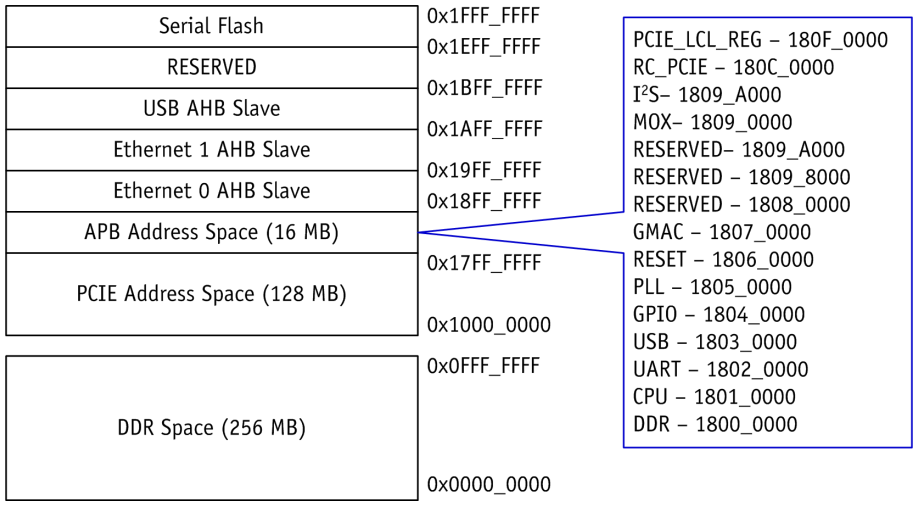

Figure 2-2. **Address Space Allocation**

2.4 AHB Master Bus

The 256 MByte region of address space for the AHB devices is divided into two major windows, 128 MByte for the PCIE and the remainder for the internal DDR AHB master interfaces such as APB, GE0, GE1, and serial flash.

2.5 APB Bridge

One 16 MByte window of the AHB address space is devoted to an APB device mapper. The APB space contains the register address spaces of most of the interfaces, including PCIE, serial flash, GPIO, and UART. This space also provides access to the watchdog timer and four general purpose timers.

2.6 DDR Memory Controller

The AR7242 supports a 16-bit DDR1/DDR2 memory interface of up to 64 MBytes of memory in a single device. It supports one dedicated point-to-point interface for the CPU and similarly dedicated point-to-point interfaces for the CPU, USB, Ethernet and PCIE master devices. Write transactions are buffered at each interface. It implements separate arbitration for each bank thus allowing efficient pipelined RAS/CAS/precharge scheduling.

The DDR block has five AHB-slave interfaces for: GE0, GE1, USB, PCIE, and CPU. External DDR is powered by the AR7242 using an external power transistor. Depending on the LDO_DDR_SEL input, the AR7242 internal regulator generates VDD_DDR output voltage to power the external DDR memory. Table 2-3 shows the LDO_DDR_SEL configurations.

Table 2-3. **LDO_DDR_SEL Voltage Configuration**

LDO-DDR_SEL Input	DDR Voltage	Device Type
0	1.8 V	DDR2
1	2.6 V	DDR1

See Figure 5-1, "Output Voltages Regulated by the AR7242," on page 185.

Table 2-4 shows the DDR configurations.

Table 2-4. **DDR Configurations**

Device Type/Total Cap.	Device Count	Device Type
64 Mbits (4 M x 16)	1	DDR1
128 Mbits (8 M x 16)	1	DDR1
256 Mbits (16 M x 16)	1	DDR1
512 Mbits (32 M x 16)	1	DDR1
256 Mbits (16 M x 16)	1	DDR2
512 Mbits (32 M x 16)	1	DDR2

Table 2-5 shows the correspondence of the internal CPU address, the DDR interface address, and the physical memory address.

Table 2-5. **Address Mapping**

CPU Address Bit	AR7242 DDR Interface Address	Corresponding 16-bit DDR Memory Address[1]
0	DDR_A_0, Unused (x16 DRAM)	
1	DDR_A_1	CAS0
2	DDR_A_2	CAS1
3	DDR_A_3	CAS2
4	DDR_A_4	CAS3
5	DDR_A_5	CAS4
6	DDR_A_6	CAS5
7	DDR_A_7	CAS6
8	DDR_A_8	CAS7
9	DDR_A_9	CAS8
10	DDR_A_0	RAS0
11	DDR_BA_0	BA0
12	DDR_BA_1	BA1
13	DDR_A_1	RAS1
14	DDR_A_2	RAS2
15	DDR_A_3	RAS3
16	DDR_A_4	RAS4
17	DDR_A_5	RAS5
18	DDR_A_6	RAS6
19	DDR_A_7	RAS7
20	DDR_A_8	RAS8
21	DDR_A_9	RAS9
22	DDR_A_10	RAS10
23	DDR_A_11	RAS11
24	DDR_A_12	RAS12
25	DDR_A_11	CAS9
26	DDR_A_12	CAS11

[1]CAS10 is a precharge bit, typically 0.

2.7 PCIE Root Complex

2.7.1 Overview

The PCI Express device used in the AR7242 is a root complex (RC) supporting a single-lane PCIE link at 2.5 Gbps. See Figure 2-3.

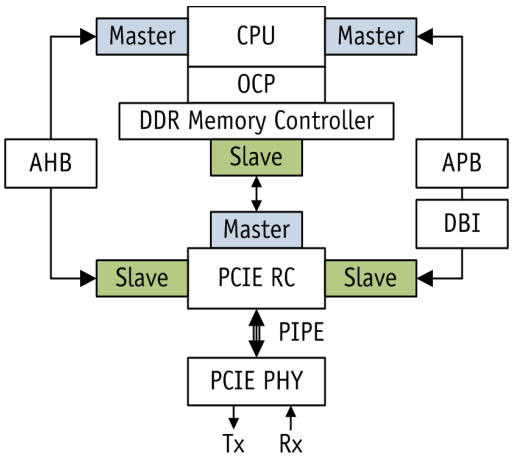

Figure 2-3. **System Level Overview**

The RC core implements the three PCI Express protocol layers: the transaction layer, the data link layer, and the physical layer (PHY).

The PHY splits across the PIPE, which is the standard interface between the PHY and the RC Core. MAC functionality is in the RC core and the PHY functionality is implemented in the PIPE-compliant PHY external to the RC.

The PHY sideband interface, or data bus interface (DBI), is controlled by the CPU via APB and programs the PCIE RC core configuration space. DBI delivers a read/write request from the application logic to the internal core registers.

The CPU controls configuration and memory requests to an external endpoint, through the AHB.

For the PCIE root complex registers, see the "PCIE Control Registers" on page 79 and "PCIE Configuration Space Registers" on page 72.

2.7.2 PCIE Root Complex Initialization Sequence

1. Deassert the "Reset (RST_RESET)" register bits PCIE_PHY_RESET and PCIE_RESET.
2. Remove the reset of the PCIE PLL to enable generation of 125 MHz and 100 MHz.
3. Deassert bypass for the PCIE PLL.
4. Deassert reset for the root complex.
5. Set "PCIE Application Control (PCIE_APP)" register bit LTSSM_ENABLE within 10 ms of reset deassertion.
6. Set the PCIE bus master enable and memory space enable in the "Command" and "Status" registers.
7. Program the registers "Memory Base", "Memory Limit", "Prefetchable Memory Base", and "Prefetchable Memory Limit" such that the 0–256 Mb DDR space is available for access for memory transactions from the endpoint to the root complex.
8. Pull the external PCIE endpoint out of reset.
9. Continue polling the linkup bit to check whether it is set to indicate a successful training sequence and entry of the LTSSM into L0. After this, PCIE transactions can be issued.

2.7.3 Power Management

The PCIE RC supports L0s and L1 active state power management. L0s is the low power standby state with lower entry and exit latencies. L1 saves power, but at the cost of increased entry and exit latencies.

In addition, reference clocks going to the endpoint can be shut down and RC PCIE PLL in L1 mode can be powered down.

2.7.4 Interrupts

PCIE RC supports legacy INTX interrupts generated through PCIE message transactions. The application monitors the interrupt assert and deassert signals for inbound legacy interrupt (from the downstream component) handling. It also supports MSI based interrupt signalling through posted memory write transfers (only one can be active at any time).

2.7.5 Error Reporting Capability and Status Checking

PCIE RC supports advanced error reporting (AER) and can capture fatal and non-fatal errors in Tx and Rx. All Rx correctable and uncorrectable errors can be captured and the interrupts can be sent to the CPU.

2.8 PLL

2.8.1 Basic Clocking

Figure 2-4 shows the basic clocking diagram.

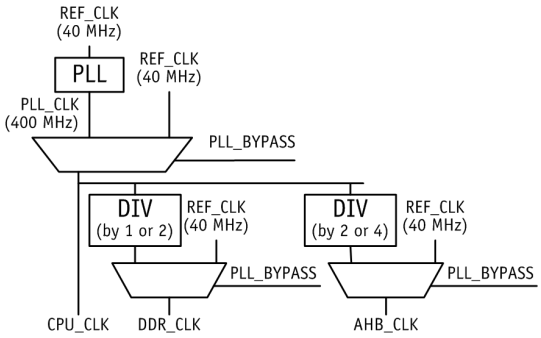

Figure 2-4. **Basic Clocking Diagram**

2.8.2 PLL INITIALIZATION SEQUENCE

PLL initialization switches the CPU, DDR, and AHB clocks from REF_CLK to high-speed clocks (from the PLL):

1. After RST_L pin is deasserted, all CPU, DDR, and AHB clocks are initially equal to REF_CLK upon boot (with the PLLs being powered down).
2. Then CPU PLL should be configured for desired clock frequency and pulled out of reset. This triggers an internal counter that counts down from 1024 to zero with respect to REF_CLK. This counter enables the PLL clock to settle down.
3. The CPU sets the "CPU Clock Configuration (CPU_CLOCK_CONTROL)" bit RESET_SWITCH to 1 then sets the bit CLOCK_SWITCH to 1. Setting these bits:
   - Causes the CPU reset to be asserted
   - Changes the CPU clock to 400 MHz (per PLL settings)
   - Waits for 8 clocks
   - Deasserts the CPU reset

   The reset assertion during clock switching ensures that any glitches in the clock during the transition do not affect the CPU.
4. The CPU restarts. The state information that initial reset/clock switch has been done is stored, keeping the CPU from looping around the same boot code.

The CPU can be operated up to 400 MHz, derived from the PLL locking range. The CPU-to-DDR clock ratio can be 1:1 or 2:1. Similarly CPU_CLK to AHB_CLK can be 2:1 or 4:1. All operate at REF_CLK in PLL bypass mode.

2.8.3 400 MHz Setup Procedure

This example procedure covers operating the CPU at 400 MHz, DDR at 400 MHz and AHB at 200 MHz. Note that the "CPU Phase Lock Loop Configuration (CPU_PLL_CONFIG)" register is located at 0x18050000 and the "CPU Clock Configuration (CPU_CLOCK_CONTROL)" register is located at 0x18050008.

1. If the CPU_CLOCK_CONTROL register bit RESET_SWITCH (bit [1]) is set to 1, jump directly to Step 5.
2. Initialize the CPU PLL in the CPU_PLL_CONFIG register:
   - RESET (bit [25]) = 0
   - DDR_DIV_SEL (bit [22]) = 0
   - AHB_DIV (bit [19]) = 0
   - NOPWD (bit [18]) = 1
   - BYPASS (bit [16]) = 0
   - REFDIV (bits [13:10]) = 4
   - DIV (bits [9:0]) = 80

   These settings enable the PLL to generate the 800 MHz clock. An internal divider inside the PLL divides it by 2 to generate a 400 MHz clock (CLK400).

   The reference clock input to PLL is 40 MHz from primary input.

   The above settings aid in operation of the CPU clock at 400 MHz, the DDR clock at 400 MHz. and the AHB clock at 200 MHz.
3. Wait for PLL to lock. Poll the register CPU_PLL_CONFIG bit UPDATING (bit [17]) until it returns to zero, indicating that the PLL has locked.
4. Enable switching from REF_CLK to PLL clocks by setting in the CPU_CLOCK_CONTROL register:
   - Set RESET_SWITCH (bit [1]) to 1 to enable CPU reset during switching
   - Set CLOCK_SWITCH (bit [0]) to 1 to start the switching process

   The CPU clock switches from REF_CLK to PLL_CLK and the CPU resets, causing the CPU to restart at Step 1 and the process to jump to Step 5.
5. Set the register CPU_CLOCK_CONTROL bits:
   - Set RESET_SWITCH (bit [1]) and CLOCK_SWITCH (bit [0]) to 0.

Continue boot code.

2.9 Serial Flash (SPI)

The single SPI chip select is dedicated to an external flash to boot the chip. Two configurable chip selects are available to bit-bang using GPIOs that configure external components. As an AHB slave, the SPI controller only supports word transactions. Because serial flash supports cached read (but not cached write) functionality, the CPU must perform uncached writes, but a read can be accelerated by performing cached reads. By default, the register "SPI Control (SPI_CONTROL)" bit REMAP_DISABLE is set to 0 and only 4 MBytes are accessible. Setting it to 1 makes up to 16 MBytes of flash space accessible.

2.10 UART

The AR7242 contains a single 16550 equivalent UART port for debug/console. The UART pins are multiplexed with GPIO pins, therefore the "GPIO Function (GPIO_FUNCTION_1)" register bits control which GIPIO pins are used for UART functions.

2.11 GE0 and GE1

The AR7242 integrates two GB Ethernet MACs. The GE0 and GE1 support 2K transmit FIFO and 2K receive FIFO. The RGMII interface connects directly to GE0. The Ethernet MAC/PHY connects through GE1. See Figure 2-5.

Each fast Ethernet MACs support four Tx queues, each with its own descriptor chain. A priority of DMA_TX_Q0 is higher than DMA_TX_Q1 and so on. The DMA configuration registers are separate for each queue. Two arbitration mechanisms are supported: one is a simple priority and the other is a weighted round robin arbitration.

The other queues work similarly. In case of round robin arbitration on a long term, the number of packets sent per queue is guaranteed to be in the ratio of the weights programmed. A weight of 0 is prohibited. Note that the weights are based on packets and not on the number of bytes transmitted on that queue. Also, a 19-bit free running counter (running on AHB_CLK) value is updated on the descriptor field as shown on the Tx and Rx descriptors. This update is part of the descriptor update the MAC DMA core already does on completion of a transmit or receive. Software can track the latency on per-packet basis using the descriptor timestamp and the free timer register.

2.12 MDC/MDIO Interface

The MDC/MDIO interface, which is internal to the AR7242, allows users to access the internal registers of the Ethernet MAC/PHY. Table 2-6 shows the format required to access the MII registers in the embedded PHY. The PHY-address is 0x00. The OP code 10 indicates the read command and 01 indicates the write command.

Table 2-6. **MDC/MDIO Interface Format**

start	Op	2'b0	Phy-addr [2.0]	reg_addr [4:0]	TA [1:0]	Data [15:0]

The internal MAC registers are 32 bits wide, but MDIO access is only 16 bits wide, so two access cycles are required to access all 32 bits of the internal registers. Address spacing is more than the MDIO-supported 10 bits, thus upper address bits must be written to the internal registers, similar to the page mode access method. For example, register address bits [18:9] are treated as a page address and written out first as High_addr [9:0] (see Table 2-7). Then the register would be accessed via Table 2-6, where Low_addr [7:1] is the register address bit [8:2] and Low_addr [0] is 0 for Data [15:0] or Low_addr [0] is 1 for Data [31:16].

Table 2-7. **Initial Register Address Bits**

start	Op	2'b11	8'b0	6'b0	High_addr [9:0]

2.13 Ethernet MAC/PHY Controller

Figure 2-5 shows the Ethernet MAC/PHY block diagram.

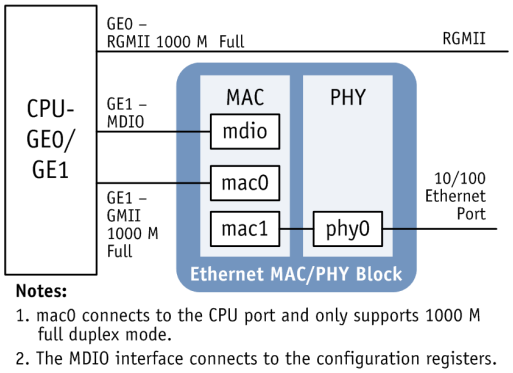

Figure 2-5. **Ethernet MAC/PHY Block Diagram**

The Ethernet MAC/PHY controller performs the most AR7242 Ethernet functions. It contains a 10/100 Mbps Fast Ethernet port, supporting four levels of QoS, 802.1Q VLANs, port based VLANs and RMON statistic counters. The AR7242 integrates one 10/100 dual speed Ethernet transceiver (PHY) and a single-port 10/100/1000 MAC as well as a wire-speed, bi-directional buffered memory.

The Ethernet MAC/PHY controller supports flow control in full-duplex and back pressure in half duplex, 802.3 auto-negotiation, port locking, MIB counters, ingress and egress rate limitation, and automatic speed and duplex communication between PHY and MAC. See Table 2-8.

Table 2-8. **Ethernet MAC/PHY Functions**

Block	Description
Media Access Controllers (MAC)	Integrates an Ethernet MAC that perform all functions in the IEEE 802.3 and IEEE 802.3u specs, including frame formatting, frame stripping, CRC checking, CSMA/CD, collision handling, flow control, etc. The MAC supports 10 or 100 Mbps operation in full- or half duplex mode.
Full-Duplex Flow Control	The AR7242 supports IEEE 802.3x full-duplex flow control, and force-mode full-duplex flow control. If the link partner supports auto-negotiation, the 802.3x full-duplex flow control auto-negotiates between the remote node and the AR7242. If full-duplex flow control is enabled, when free buffer space is almost empty, the AR7242 sends out an IEEE 802.3x compliant PAUSE frame to stop the remote device from sending more frames.
Half-Duplex Flow Control	Half-duplex flow control regulates the remote STA to avoid dropping packets during network congestion. A back pressure function is supported for half-duplex operations. When free buffer space is almost empty, the AR7242 transmits a jam pattern on the port and forces a collision. If half-duplex flow control is not set, incoming packets drop if no buffer space is available.
Inter-Packet Gap (IPG)	The IPG is the idle time between any to successive packets from the same port. The typical IPG is 9.6 µs for 10 Mbps Ethernet and 960 µs for 100 Mbps Fast Ethernet.
Illegal Frames	The AR7242 discards all illegal frames such as CRC error, oversized packets (length greater than maximum length), and runt packets (length less than 64 bytes).
VLANs	See "VLAN Support" on page 25.
QoS	See "Quality of Service (QoS) For MAC/PHY Port" on page 26.

2.13.4 VLAN Support

The AR7242 supports 16 IEEE 802.1Q VLANs and port-based VLAN functionality for all frames, including management frames when 802.1Q is enabled on the ingress port. Untagged frames conform to the port-based VLAN even if the ingress port has 802.1Q mode enabled. See Table 2-9.

Table 2-9. **Ethernet Port VLAN**

VLAN	Description
Port-Based	Each ingress port contains a register restricting the output (or egress) ports it can send frames to. This port-based VLAN register has a field called PORT_VID_MEM that contains the port based setting. If bit [0] of PORT_VID_MEM is set to one, the port is allowed to send frames to Port 0, while bit [1] allows transmission from the PHY. At reset, the port's PORT_VID_MEM is set to a value of all 1s, except for the port's own bit, which clears to zero. Note that the CPU port is port 0.
IEEE 802.1Q VLANs	The AR7242 supports a maximum of 16 entries in the VLAN table. The device supports 4096 VLAN ID range from 0 to 4095. The AR7242 only supports shared VLAN learning (SVL). This means that forwarding decisions are based on the frame's destination MAC address, which should be unique among all VLANs.

Tagging and untagging egress frames is supported using 802.1Q VLANs, or statically using Port Based VLANs. Frames may go out from the Ethernet port in three methods:

- Transmit Unmodified
  Untagged frames egress a port untagged while tagged frames leave tagged.
- Transmit Untagged
  Untagged frames leave a port unmodified while tagged frames leave untagged.
- Transmit Tagged
  Tagged frames leave a port unmodified while an IEEE tag is added to untagged frames before leaving.

When a tag is added to an untagged frame, the frame inserts directly after the frame's source address and includes four bytes.

- The first byte is always 0x81.
- The second byte is always 0x00.
- PRI bits indicate frame priority determined by the source port's priority setting.
- The CFI bit is always set to 0.

VID bits indicate the VID assigned to the frame as determined in the source port default VID.

A tagged frame leaving a port tagged may have its VID bits modified. If the ingressing frame's VID was 0x000, the ingress port's default VID is assigned to the frame instead.

Double Tagging is a method of isolating one IEEE 802.1Q VLAN from other IEEE 802.1Q VLANs in a hierarchical fashion that is compatible with IEEE 802.1Q ready switches, as long as those switches support a maximum frame size of 1526 bytes or more. In this way, an extra, or double, tag is placed in front of a frame's normal tag thereby increasing the frame's size by four bytes.

Ingress double tagging can be selected on a port-by-port basis. Typically, any port that has ingress double tagging enabled will also have egress double tagging enabled. Ingress double tagging enabled ports expect all ingress frames to contain an extra tag that must be removed from the frame before performing the port's ingress policy on the frame. In this mode, the ingress policy removes the first IEEE 802.3ac tag that appears after the source address in every frame. If the untagged frame is not modified, all data from the removed tags is ignored by the switch.

2.13.5 Quality of Service (QoS) For MAC/PHY Port

The AR7242 recognizes the QoS information of ingress frames and map to different egress priority levels. The AR7242 determines the priority of the frames based on DA, TOS/TC, VLAN, and port. Each has an enable bit that can be applied. When more than one type of priority is selected, the order in which the frame priority should be applied can be determined. Priority enable bits and select order bits are set by port base at 0x110 for port 0, 0x210 for port 1, and so on.

Priority Determined	Description
DA	Set DA_PRI_EN bit [18] to 1 and add the address to the ARL table-set priority_over_en to 1. ARL priority bits [59:58] can be used as DA priority.
ToS/TC	Set IP_PRI_EN bit [16] to 1, and set the IP priority mapping register (0x60–0x6C).
VLAN	Set VLAN_PRI_EN (bit [17]) to 1, and set the TAG priority mapping register (0x70).
Port's Default Authority	Set PORT_PRI_EN to 1, and set port base register ING_PORT_PRIORITY (bits [19:28] in 0x108, 0x208, etc.).

When more than one priority enable bit is set to 1, bits [7:0] in 0x110, 0x210, etc. (DA_PRI_SEL, IP_PRI_SEL, VLAN_PRI_SEL, PORT_PRI_SEL) can determine the order in which the frame priority should be applied. If *_PRI_SEL is set to 00, frame priority is determined by that first. Otherwise, priority is determined by which *_PRI_SEL is set to 01, then 10, 11, etc.

On arrival, packets are directed into one of the four available priority queues based on:

- Priority bits in the header field
- The frame destination address (if in the ARL table with a defined priority with the priority bit is enabled)
- The frame VID (if in the VLAN table and the priority override is enabled)
- The 802.3 tag containing 802.1p priority information (if enabled on the port)
- The port's default priority as defined in the register

Each of the priority classification rules have enables so designers may use any combination; priority can be disabled or the order may be selected separately on a per-port basis.

Congestion in the flow of packets for an extended period of time forces frames to drop without flow control. Higher priority flows receive a higher percentage of the open buffers, and this percentage is determined by the scheduling mode. Features such as back pressure and pause-frame control are implemented to supports zero packet loss during traffic congestion.

QoS for the AR7242 may follow one of three priority schemes, either fixed, weighted fair, or a mixed mode scheme. In the fixed priority scheme, all egress packets leave the port starting with the highest priority queue. Once that queue has been emptied, the next highest priority queue begins its packet dispersal until it has been emptied and so on. This method insures that all high priority packets will be sent out from the port as soon as possible.

For the weighted fair scheme, packets are egressed from the chip in the order of 8, 4, 2, 1 packets for the four priorities queue of the AR7242. (eight packets egress from the highest priority queue, then four from the second highest queue, and so on). This method allows the highest priority to get its packets out first and the other remaining queues are not totally starved from egressing.

The mixed mode scheme mixes both the weighted fair and fixed schemes. The highest priority queue disperses its packets first until the queue has been emptied, and the remaining queues will follow the 4, 2, 1 weighted egress scheme as mentioned previously. This ensures that the highest priority queue will egress its packets as soon as possible, while the remaining queues equally disperse their packets without queue starvation.

2.14 Rate Limiting

The AR7242 supports port-based ingress and egress rate limiting. All frames may be limited but management frames and known multicast frames are the only types that can be selected by the user. The ingress limit rate may be set from zero to 1 Gbps in steps of 32 Kbps. The port base register is used to determine the limited bytes to count. The default setting for rate limiting is to include the frame's bytes from the beginning of the preamble to the end of the RCS with a added minimum IFG.

2.15 Broadcast Storm Control

The AR7242 supports broadcast storm control. Some switch designs may require limiting the reception rate of frames. The types of frames to be limited can be selected separately on a per-port basis.The maximum rate desired needs to be selected by the user and then programmed. Eleven different frame rates from 1k (2^0K) to 2^{10}K per second.

The statistics counter block maintains a set of forty MIB counters per port. These counters provide a set of Ethernet statistics for frames received on ingress and transmitted on egress. A register interface allows the CPU to capture, read, or clear the counter values.

The counters support:

- RMON MIB
- Ethernet-like MIB
- MIB II
- Bridge MIB
- RFC2819

The CPU interface supports:

- Autocast MIB counters after half-full
- Autocast MIB counters after time out
- Autocast MIB counters when requested
- Clearing all MIB counters

GE0 and GE1 CPU ports and the MAC/PHY port each have a set of MIB counters.

2.16 Port Operation

Two tables embedded in the AR7242 aid in allocation of ingress packets, the ARL table and the VLAN table.

The address database is stored in the embedded SRAM and can store up to 1024 address entries. The default aging time for this table is 300 seconds. One address can be searched in the table and it may be used to get the next read out of the whole table. Entries in the table may be loaded and purged. All entries maybe be flushed, and this may be divided to flush just non-static entries, all entries per port or all non-static entries per port.

The VLAN table supports a single search, and it may be used to get the next read out of the whole table. Entries may be loaded or purged and entries may be flushed, either as a whole or per port.

2.17 Port States

Table 2-10 shows the port states supported by the AR7242.

Table 2-10. **Port States**

State	Description
Disabled	Frames are not allowed to enter or leave a disabled port. Learning does not take place on disabled ports.
Blocking	Only MGMP frames are allowed to enter a blocked port. All other frame types are discarded. Learning is disabled on blocked ports.
Listening	Only management frames may enter or leave a listening port. All other frame types are discarded. Learning is disabled on listening ports.
Learning	Only management frames may enter or leave a learning port. All other frame types are discarded but learning occurs on all good frames, including non-management frames.
Forwarding	Normal operation. All frames may enter or leave a forwarding port. Learning occurs on all good frames.

3. Audio Interface

3.1 Overview

Figure 3-1 shows a block diagram of the AR7242 audio interface.

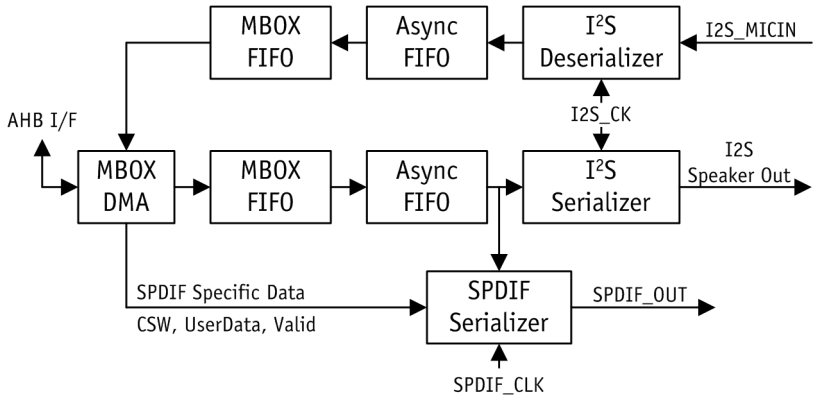

Figure 3-1. **Audio Interface**

The AR7242 includes an I²S speaker and microphone interface as well as an SPDIF speaker interface. The I²S and SPDIF clocks are generated by the audio PLL block.

3.2 Audio PLL

Figure 3-2 shows the AR7242 audio PLL block diagram.

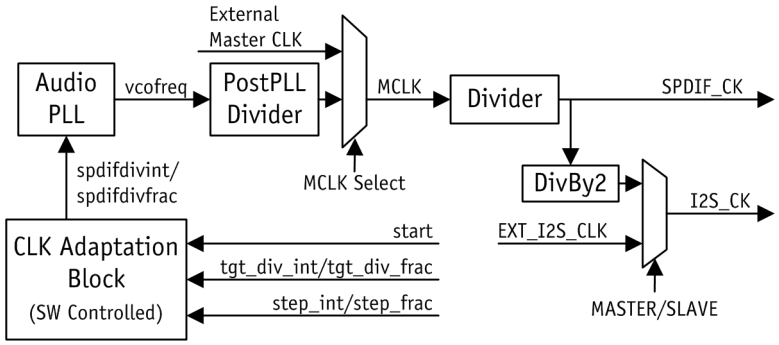

Figure 3-2. **Audio PLL Block Diagram**

The audio PLL can support generation of all the audio master clock frequencies. It accepts two inputs, SPDIFDIVINT and SPDIFDIVFRAC, which are generated by a clock adaptation module. The clock adaptation module enables slow changing of the audio clock by changing SPDIFDIVINT/ SPDIFDIVFRAC in small steps from the current value to a target value. The target TGT_DIV_INT/TGT_DIV_FRAC and step size are software programmable. The clock adaptation module changes the value of the SPDIFDIVINT/SPDIFDIVFRAC values with respect to a slow SPDIFCLKSDM clocks. This small step size ensures that the audio PLL tracks the small variation. The resolution of DIVFRAC ensures that the clock can be varied with steps less than 200 ppb. Following the audio PLL come three dividers: postPLL divider and ExtDiv controlled through the register AUDIO_PLL_CONFIG, PostPLLDivide field, and another posedge divider inside the I²S STEREO_CONFIG register. The final clock relations is:

(40 MHz/3) * (int.frac) = vcofreq
vcofreq/(PostPLLDiv * ExtDiv) = MCLK
MCLK/posedge = SPDIF_CLK

If the master must be modified from the current value to another value, it is software's responsibility to recompute and program the new TGT_DIV_INT/TGT_DIV_FRAC values.

3.3 I²S Interface

The AR7242 I²S supports a two-channel digital audio subsystem. This interface uses the I²S pins listed in Table 1-2, "Signal-to-Pin Relationships and Descriptions," on page 12.

3.3.1 External DAC

An external DAC receives I²S digital audio streams and converts them to analog output to drive speaker or headphones. This data stream is PCM data which is serialized and sent with a left channel/right channel select and synchronization signal. The I²S serializer can be programmed to support a few different variants of the I²S data format to be compatible with a larger number of external DAC components, including various PCM data word sizes, serialization boundaries, and clocking options.

I²S can also operate in a slave mode where the stereo clock and word select are driven by external master (DAC or external controller). External DAC parts are often controlled by a separate serial 2-wire or 3-wire interface. This interface often controls volume and configuration of the external DAC. This can be attached to the AR7242 serial interface controllers.

3.3.2 Sample Sizes and Rates

The stereo audio path supports PCM sample sizes of 8, 16, 24, or 32 bits for speaker out and PCM sample sizes of 16 and 32 bits for MICIN. The serializer supports serialization sizes of 16 or 32 bits. The sample size and serialization size need not be the same, LSBs will be padded with 0's. If the AR7242 is programmed to be a slave, word select and stereo clock (the bit clock) are inputs from the external DAC/ADC.

Along with configuration information, a sample counter provides the number of samples transmitted per second through the I²S SpeakerOut interface. This sample counter can be used and cleared by software as required.

3.3.3 Stereo Software Interface

To play music, software configures the stereo subsystem and sends interleaved (LRLR....) PCM data to the mailbox DMA. To record music, software configures the stereo subsystem and the PCM samples (interleaved) are written into the memory.

To send data PCM samples on the I²S interface:

1. Program GPIO_FUNCTION register to enable I²S.
2. Program the STEREO_CONFIG register to enable the stereo.
3. Configure other parameters.
   For example, sample size, word size, mono/stereo mode, master/slave mode, clk divider (if the AR7242 is master), and so on.
4. Issue a stereo reset.
5. Configure the DMA to send SpeakerOut from the AR7242.

To receive data PCM samples:

1. Program the GPIO_FUNCTION register to enable I²S.
2. Program STEREO_CONFIG register to enable the stereo.
3. Issue a MICIN reset to reset Micin buffers.
4. Configure other parameters.
   For example, sample size, word size, mono/stereo mode, master/slave mode, clk divider (if the AR7242 is master), and so on.
5. Configure the DMA to receive PCM samples.

3.4 SPDIF INTERFACE

The AR7242 also includes a SPDIF interface for audio. The SPDIF interface only includes SPDIF_OUT to the speakers. SPDIF_IN is not supported in the AR7242.

The SPDIF interface operates on the same sample as I²S, so it always in sync with audio played on the I²S interface. All configuration information to the SPDIF block, such as the sampling frequency, sample size, word size, and so on, are inherited from the programming of the I²S interface. If only the SPDIF interface is required to operate and the I²S audio interface is not required, the programming still only needs to be done using I²S configuration registers. The I²S interface can be disabled using the GPIO function register.

The SPDIF specific data that forms part of each SPDIF audio subframe such as the valid, CSW, and user data are provided through the DMA descriptor directly to the SPDIF Module. The DMA controller describes how the data is provided through the descriptor.

3.5 MAILBOX (DMA CONTROLLER)

A MBOX DMA Controller is used in the AR7242 for I^2S and SPDIF interface. The MBOX channel is a duplex channel that can operate simultaneously for Rx and Tx.

3.5.1 Mailboxes

The AR7242 supports one duplex mailbox to move data between the DDR memory and audio interfaces I^2S and SPDIF through the AHB interface. Flow control of the DMA must be managed by software.

3.5.2 MBOX DMA Operation

The AR7242 MBOX DMA engine has one channel for Tx and one channel for Rx. Each mailbox DMA channel follows a list of linked descriptors.

Figure 3-3 and Table 3-1 show the descriptor format and description.

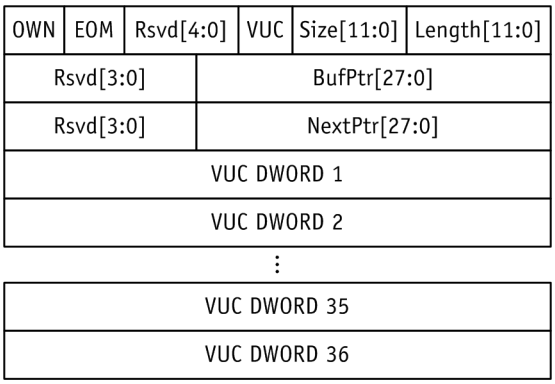

Figure 3-3. **DMA Descriptor Structure**

Table 3-1. **Descriptor Fields**

Name	Bits	Description
Length	12	Length of data in memory buffer. If EOM=0, the Length = Size.
Size	12	Size of memory buffer.
VUC	1	When this bit set, the SPDIF block uses the VUC data for the audio block fetched from the previous descriptor.
EOM	1	End of message indicator.
OWN	1	Descriptor is owned by the CPU or DMA engine. (If set, it is owned by the DMA engine).
BufPtr	28	Points to memory buffer pointer. Byte aligned address.
NextPtr	28	Points to next descriptor in the list. Must be word aligned.
VUC DWORD 1 to 36	36 * 32 bits	These are the VUC data for each audio block of the SPDIF. 192 Bits each of Valid, UserData and Channel Status Word for two channels of audio corresponds to 36 Dwords. These data are SPDIF specific and software does not need to provide this data if I^2S is the only active interface and SPDIF is disabled.

Once the DMA engine is started, it will follow its descriptor chain until it arrives at a descriptor that has its owner bit set to CPU (bit [31] of the status word is not set). The DMA engine then stops until the CPU restarts it.

The DMA control registers include stop and start commands, a programmable descriptor chain base address, DMA policies to use, and so on. DMA status registers inform the CPU when the engine is running, done, or encountered an error.

3.5.3 Software Flow Control

To configure the MBOX channel to send data from the AR7242 (Rx as referred in MBOX):

1. Set up the MBOX Rx descriptors. The owner should be set to indicate it is owned by the DMA controller. Hardware resets this once DMA is complete.
2. Load the corresponding buffers with the data to transmit.
3. Program the register MBOX_DMA_TX_DESCRIPTOR_BASE_ADDRESS with the base descriptor address.
4. Reset the corresponding MBOX FIFO.
5. Enable the DMA by setting the START bit in the MBOX_DMA_RX_CONTROL register. This register has a provision to stop and resume at any time.
6. On DMA completion, the RX_DMA_COMPLETE interrupt is asserted.

To configure the MBOX channel for the AR7242 to receive data (Tx as referred in MBOX):

1. Set up the MBOX Tx descriptors. The owner should be set to indicate it is owned by the DMA controller. Hardware resets this once DMA is complete.
2. Program the register MBOX_DMA_TX_DESCRIPTOR_BASE_ADDRESS with the base descriptor address.
3. Reset the corresponding MBOX FIFO.
4. Enable the DMA by setting START bit in MBOX_DMA_TX_CONTROL register. This register has a provision to stop and resume at any time.
5. On DMA completion, the TX_DMA_COMPLETE interrupt is asserted.

3.5.4 Mailbox Error Conditions

If flow control synchronization is lost for any reason, these mailbox error conditions could arise:

Table 3-2.

Tx Mailbox Overflow	If no DMA descriptors are available on the AR7242 Tx side, but an message is coming in from the corresponding interface, the Tx mailbox stalls the host physical interface. If the host interface remains stalled with the Tx FIFO full for a timeout period specified other than FIFO_TIMEOUT, a timeout error occurs. An interrupt is sent to CPU. As long as the host status overflow bit is set, any mailbox Tx bytes that arrive from the host when the mailbox is full are discarded. When the host clears the overflow interrupt, mailbox FIFOs return to normal operation. Software must then either resynchronize flow control state or reset the AR7242 to recover.
Rx Mailbox Underflow	If I^2S reads a mailbox that does not contain any data and this condition persists for more than a timeout period, the CPU is sent an underflow error interrupt. As long as status underflow bit is set, any mailbox reads which arrive when the mailbox is empty return garbage data. Software must then either resynchronize flow control state or reset the AR7242 to recover.

3.5.5 MBOX-Specific Interrupts

All MBOX specific interrupts can be masked by control registers (MBOX_INT_ENABLE).

MBOX sends an interrupt to MIPS in these cases (if they are enabled):

- Tx DMA complete, Rx DMA complete
- Tx overflow, Tx not empty (incoming traffic)
- Rx underflow, Rx not full (outgoing traffic)

The status of these interrupts can be read from the MBOX_INT_STATUS register.

4. Register Descriptions

These sections describe the internal registers for the various AR7242 blocks. Table 4-1 summarizes the AR7242 registers.

Table 4-1. **Registers Summary**

Address	Description	Page
0x18000000–0x18000094	DDR Registers	page 34
0x18020000–0x18020018	UART Registers	page 39
0x18040000–0x18040030	GPIO Registers	page 45
0x18050000–0x1805003C	PLL Control Registers	page 50
0x18060000–0x18060044	Reset Registers	page 57
0x180A0004–0x180A002C	MBOX Registers	page 62
0x180B0000–0x180B0018	I^2S Registers	page 68
0x180C0000–0x180C003C	PCIE Configuration Space Registers	page 72
0x180F0000–0x180F0050	PCIE Control Registers	page 79
0x19000000–0x190001D8 0x1A000000–0x1A0001D8	Ethernet Registers	page 88
0x1B000100–0x1B00017C	USB Controller Registers	page 127
0x1F000000–0x1F00000C	SPI Registers	page 156
0x0000–0x201A4	Ethernet MAC/PHY Port Registers	page 158

4.1 DDR Registers

Table 4-2 summarizes the DDR registers for the AR7242.

Table 4-2. **DDR Registers Summary**

Address	Name	Description	Page
0x18000000	DDR_CONFIG	DDR DRAM Configuration	page 34
0x18000004	DDR_CONFIG2	DDR DRAM Configuration	page 35
0x18000008	DDR_MODE_REGISTER	DDR Mode Value	page 35
0x1800000C	DDR_EXTENDED_MODE _REGISTER	DDR Extended Mode Value	page 35
0x18000010	DDR_CONTROL	DDR Control	page 36
0x18000014	DDR_REFRESH	DDR Refresh Control and Configuration	page 36
0x18000018	DDR_RD_DATA_THIS_CYCLE	DDR Read Data Capture Bit Mask	page 36
0x1800001C	TAP_CONTROL_0	DQS Delay Tap Control for Byte 0	page 36
0x18000020	TAP_CONTROL_1	DQS Delay Tap Control for Byte 1	page 37
0x1800007C	DDR_WB_FLUSH_GE0	Write Buffer Flush for GE0 Interface	page 37
0x18000080	DDR_WB_FLUSH_GE1	Write Buffer Flush for GE1 Interface	page 37
0x18000084	DDR_WB_FLUSH_USB	Write Buffer Flush for USB Interface	page 37
0x18000088	DDR_WB_FLUSH_PCIE	Write Buffer Flush for PCIE Interface	page 38
0x1800008C	DDR_DDR2_CONFIG	DDR2 Configuration	page 38
0x18000090	DDR_EMR2	DDR EMR2 Value	page 38
0x18000094	DDR_EMR3	DDR EMR3 Value	page 38

4.1.1 DDR DRAM Configuration (DDR_CONFIG)

Address: 0x18000000
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31	CAS_LATENCY_MSB	0x0	MSB bit of 4-bit CAS_LATENCY field
30	OPEN_PAGE	0x1	Controller open page policy; open page policy increases bus efficiency if accesses are local to a page but increase random read/write latency. 0 Page open 1 Page closed
29:27	CAS_LATENCY	0x6	DRAM CAS latency parameter (first 3 bits) rounded up in memory core clock cycles; CAS_LATENCY is used by the hardware to estimate the internal DDR clock latency of a read; it should be greater than or equal to GATE_OPEN_LATENCY as specified in the DDR_CONFIG2 register. The value of this register should be memory cas_latency * 2 or cas_latency * 2 +1/2/3.
26:23	TMRD	0xF	DRAM tMRD parameter rounded up in memory core clock cycles
22:17	TRFC	0x1E	DRAM tRFC parameter rounded up in memory core clock cycles
16:13	TRRD	0x4	DRAM tRRD parameter rounded up in memory core clock cycles
12:9	TRP	0x6	DRAM tRP parameter rounded up in memory core clock cycles
8:5	TRCD	0x6	DRAM tRCD parameter rounded up in memory core clock cycles
4:0	TRAS	0x10	DRAM tRAS parameter rounded up in memory core clock cycles

4.1.2 DDR DRAM Configuration (DDR_CONFIG2)

Address: 0x18000004
Access: Read/Write
Reset: See field description

GATE_OPEN_LATENCY is separated from CAS_LATENCY to separately control the write and read sides of the DQS/DQ memory inputs.

Bit	Bit Name	Reset	Description	
31	HALF_WIDTH_LOW	0x1	Controls which part of the 32-bit DDR DQ bus is populated with DRAM in a 16-bit memory system	
			0	31:16
			1	15:0
30	RES	0x0	Reserved	
29:26	GATE_OPEN_LATENCY	0x6	Memory CAS LATENCY * 2	
25:21	TWTR	0xE	DRAM tWTR parameter rounded up in memory core clock cycles	
20:17	TRTP	0x8	DRAM read to precharge parameter rounded up in memory core clock cycles; normal value is 2 control cycles	
16:12	TRTW	0x10	DRAM tRTW parameter rounded up in memory core clock cycles; the value should be CAS LATENCY + BURST LENGTH + BUS TURNAROUND TIME	
11:8	TWR	0x6	DRAM tWR parameter rounded up in memory core clock cycles	
7	CKE	0x0	DRAM CKE bit	
6	PHASE_SELECT	0x0	Select output phase	
5	CNTL_OE_EN	0x1	Control bit to allow the memory controller to tri-state the address/ control outputs	
4	BURST_TYPE	0x0	DRAM burst type	
			0	Sequential
			1	Interleaved
3:0	BURST_LENGTH	0x8	DRAM burst length setting (2, 4, or 8; only 8 is supported)	

4.1.3 DDR Mode Value (DDR_MODE_REGISTER)

Address: 0x18000008
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:13	RES	0x0	Reserved
12:0	VALUE	0x133	Mode register value Reset to CAS 3, BL=8, sequential, DLL reset off

4.1.4 DDR Extended Mode Value (DDR_EXTENDED_MODE_REGISTER)

Address: 0x1800000C
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:13	RES	0x0	Reserved
12:0	VALUE	0x2	Extended mode register value Reset to weak driver, DLL on

4.1.5 DDR Control (DDR_CONTROL)

Address: 0x18000010
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:6	RES	Reserved
5	EMR3	Force a EMR3S update cycle
4	EMR2	Force a EMR2S update cycle
3	PREA	Force a PRECHARGE ALL cycle
2	REF	Force an AUTO REFRESH cycle
1	EMRS	Force an EMRS update cycle
0	MRS	Force a MRS update cycle

4.1.6 DDR Refresh Control and Configuration (DDR_REFRESH)

Address: 0x18000014
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:15	RES	0x0	Reserved
14	ENABLE	0x0	Refresh enable
13:0	PERIOD	0x2000	Refresh period

4.1.7 DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE)

Address: 0x18000018
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved
23:0	VEC	0xFF	Each bit represents a cycle of valid data

4.1.8 DQS Delay Tap Control for Byte 0 (TAP_CONTROL_0)

Address: 0x1800001C
Access: Read/Write
Reset: See field description

This register is used along with DQ LANE 0, DQ[7:0], DQS_0.

Bit	Bit Name	Reset	Description
31:7	RES	0x0	Reserved
6	BYPASS_EN	0x0	Bypass enable. Short circuits the first four taps directly to the output; only used in the very slow corner for the absolute minimum delay
5	RES	0x0	Reserved
4:0	TAP	0x5	Tap setting for delay chain

4.1.9 DQS Delay Tap Control for Byte 1 (TAP_CONTROL_1)

Address: 0x18000020
Access: Read/Write
Reset: See field description

This register is used along with DQ LANE 1, DQ[7:0], DQS_1.

Bit	Bit Name	Reset	Description
31:7	RES	0x0	Reserved
6	BYPASS_EN	0x0	Bypass enable. Short circuits the first four taps directly to the output; only used in the very slow corner for the absolute minimum delay
5	RES	0x0	Reserved
4:0	TAP	0x5	Tap setting for delay chain

4.1.10 Write Buffer Flush for GE0 Interface (DDR_WB_FLUSH_GE0)

Address: 0x1800007C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	FLUSH	Set to 1 to flush; will reset to 0 when flush is complete

4.1.11 Write Buffer Flush for GE1 Interface (DDR_WB_FLUSH_GE1)

Address: 0x18000080
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	FLUSH	Set to 1 to flush; will reset to 0 when flush is complete

4.1.12 Write Buffer Flush for USB Interface (DDR_WB_FLUSH_USB)

Address: 0x18000084
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	FLUSH	Set to 1 to flush; will reset to 0 when flush is complete

4.1.13 Write Buffer Flush for PCIE Interface (DDR_WB_FLUSH_PCIE)

Address: 0x18000088
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	FLUSH	Set to 1 to flush; will reset to 0 when flush is complete

4.1.14 DDR2 Configuration (DDR_DDR2_CONFIG)

Address: 0x1800008C
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31:13	RES	0x0	Reserved	
12:10	DR2_TWL	0x2	Delay between WE_L/CAS_L assertion on DQS, DQ assertion for a DDR2 write transaction (in DDR_CLK cycles)	
9:8	RES	0x0	Reserved	
7:2	DDR2_TFAW	0x16	tFAW parameter in core DDR_CLK cycles	
0	ENABLE_DDR2	0x0	0	DDR1
			1	DDR2

4.1.15 DDR EMR2 Value (DDR_EMR2)

Address: 0x18000090
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:13	RES	Reserved
12:0	VALUE	Extended mode register 2 value

4.1.16 DDR EMR3 Value (DDR_EMR3)

Address: 0x18000094
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:13	RES	Reserved
12:0	VALUE	Extended mode register 3 value

4.2 UART Registers

Table 4-3 summarizes the UART registers for the AR7242.

Table 4-3. **UART Registers Summary**

Address	Name	Description	Page
0x18020000	RBR	Receive Buffer	page 39
0x18020000	THR	Transmit Holding	page 39
0x18020000	DLL	Divisor Latch Low	page 40
0x18020004	DLH	Divisor Latch High	page 40
0x18020004	IER	Interrupt Enable	page 40
0x18020008	IIR	Interrupt Identity	page 41
0x18020008	FCR	FIFO Control	page 41
0x1802000C	LCR	Line Control	page 42
0x18020010	MCR	Modem Control	page 42
0x18020014	LSR	Line Status	page 43
0x18020018	MSR	Modem Status	page 44

4.2.1 Receive Buffer (RBR)

Address: 0x18020000
Access: Read-Only
Reset: 0x0

This read-only register contains the data byte received on the serial input port (SIN). The data in this register is only valid if the Data Ready (DR) bit in the Line Status Register (LSR) is set. In the non-FIFO mode (FIFO_MODE = 0), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. In FIFO mode (FIFO_MODE = 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already residing in the FIFO is full and this register will be preserved but any incoming data will be lost. An overrun will error will also occur.

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	RBR	The receive buffer register value

4.2.2 Transmit Holding (THR)

Address: 0x18020000
Access: Write-Only
Reset: 0x0

This write-only register contains data to be transmitted on the serial port (s_{OUT}). Data can be written to the THR any time the THR Empty (THRE) bit of the Line Status Register is set. If FIFOs are not enabled and the THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled and the THRE is set, up to sixteen characters of data may be written to the THR before the FIFO is full. Attempting to write data when the FIFO is full results in the write data being lost.

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	THR	The transmit buffer value

4.2.3 Divisor Latch Low (DLL)

Address: 0x18020000
Access: Read/Write
Reset: 0x0

This register, in conjunction with the "Divisor Latch High (DLH)" register forms a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. It is accessed by first setting the DLAB bit (bit [7]) in the "Line Control (LCR)" register. The output baud rate is equal to the input clock frequency divided by sixteen times (*16) the value of the baud rate divisor:

baud = (clock freq)/ (16 * divisor)

Bit	Bit Name	Type	Reset	Description
31:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	DLL	RW	0x0	Divisor latch low

4.2.4 Divisor Latch High (DLH)

Address: 0x18020004
Access: Read/Write
Reset: 0x0

This register, in conjunction with the "Divisor Latch Low (DLL)" register forms a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. It is accessed by first setting the DLAB bit (bit 7) in the "Line Control (LCR)" register. The output baud rate is equal to the input clock frequency divided by sixteen times (*16) the value of the baud rate divisor:

baud = (clock freq)/ (16 * divisor)

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	DLH	Divisor latch high

4.2.5 Interrupt Enable (IER)

Address: 0x18020004
Access: Read/Write
Reset: 0x0

This register contains four bits that enable the generation of interrupts.

Bit	Bit Name	Description
31:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	EDDSI	Enable modem status interrupt
2	ELSI	Enable receiver line status interrupt
1	ETBEI	Enable register empty interrupt
0	ERBFI	Enable received data available interrupt

4.2.6 Interrupt Identity (IIR)

Address: 0x18020008
Access: Read-Only
Reset: 0x0

This register identifies the source of an interrupt. The two upper bits of the register are FIFO-enabled bits.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7:6	FIFO_STATUS	FIFO enable status bits	
		00	FIFO disabled
		11	FIFO enabled
5:4	RES	Reserved. Must be written with zero. Contains zeros when read.	
3:0	IID	Used to identify the source of the interrupt	
		0000	Modem status changed
		0001	No interrupt pending
		0010	THR empty
		0100	Received data available
		0110	Receiver status
		1100	Character time out

4.2.7 FIFO Control (FCR)

Address: 0x18020008
Access: Write-Only
Reset: 0x0

This register sets the parameters for FIFO control. This register will also return current time values.

If FIFO mode is 0, this register has no effect. If FIFO mode is 1, this register will control the read and write data FIFO operation and the mode of operation for the DMA signals TXRDY_N and RXRDY_N.

If FIFO mode is enabled (FIFO mode = 1 and bit [0] is set to 1), bit [3], bit [6], and bit [7] are active.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7:6	RCVR_TRIG	Sets the trigger level in the receiver FIFO for both the RXRDY_N signal and the Enable received data available interrupt (ERBFI)	
		00	1 byte in FIFO
		01	4 bytes in FIFO
		10	8 bytes in FIFO
		11	14 bytes in FIFO
5:4	RES	Reserved	
3	DMA_MODE	This bit determines the DMA signalling mode for TXRDY_N and RXRDY_N output signals	
2	XMIT_FIFO_RST	Writing this bit resets and flushes data in the transmit FIFO	
1	RCVR_FIFO_RST	Writing this bit resets and flushes data in the receive FIFO	
0	FIFO_EN	Setting this bit enables the transmit and receive FIFOs. The FIFOs are also reset any time this bit changes its value.	

4.2.8 Line Control (LCR)

Address: 0x1802000C
Access: Read/Write
Reset: 0x0

This register controls the format of the data that is transmitted and received by the UART controller.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7	DLAB	The divisor latch address bit. Setting this bit enables reading and writing of the "Divisor Latch Low (DLL)" and "Divisor Latch High (DLH)" registers to set the baud rate of the UART. This bit must be cleared after the initial baud rate setup in order to access the other registers.	
6	BREAK	Setting this bit sends a break signal by holding the SOUT line low (when not in loopback mode, as determined by "Modem Control (MCR)" register bit [4]), until the BREAK bit is cleared. When in loopback mode, the break condition is internally looped back to the receiver.	
5	RES	Reserved	
4	EPS	Used to set the even/odd parity. If parity is enabled, this bit selects between even and odd parity. If this bit is a logic 1, an even number of logic 1s are transmitted or checked. If this bit is a logic 0, an odd number of logic 1s are transmitted or checked.	
3	PEN	Used to enable parity when set	
2	STOP	Used to control the number of stop bits transmitted. If this bit is a logic 0, one-stop bit is transmitted in the serial data. If this bit is a logic 1 and the data bits are set to 5, one and a half stop bits are generated. Otherwise, two stop bits are generated and transmitted in the serial data out.	
1:0	CLS	Used to control the number of bits per character	
		00	5 bits
		01	6 bits
		10	7 bits
		11	8 bits

4.2.9 Modem Control (MCR)

Address: 0x18020010
Access: Read/Write
Reset: See field description

This register controls the interface with the modem.

Bit	Bit Name	Reset	Description
31:6	RES	0x0	Reserved
5	LOOPBACK	0x1	When set, the data on the SOUT line is held HIGH, while the serial data output is looped back to the SIN line, internally. In this mode, all the interrupts are fully functional. This feature is also used for diagnostic purposes. The modem control inputs (DSR_L, CTS_L, RI_L, DCD_L) are disconnected and the four modem control outputs (DTR_L, RTS_L, OUT1_L, OUT1_L) are looped back to the inputs, internally.
4	RES	0x0	Reserved
3	OUT2	0x1	Used to drive the UART output UART_OUT2_L
2	OUT1	0x1	Used to drive the UART output UART_OUT1_L
1	RTS	0x1	Used to drive the UART output RTS_L
0	DTR	0x1	Used to drive the UART output DTR_L. Not supported.

4.2.10 Line Status (LSR)

Address: 0x18020014
Access: Read/Write
Reset: 0x0

This register contains the status of the receiver and transmitter data transfers. This status may be read by the user at any time.

Bit	Bit Name	Description
31:8	RES	Reserved
7	FERR	The error in receiver FIFO bit. This bit is only active when the FIFOs are enabled. This bit is set when there is at least one parity error, framing error or break in the FIFO. This bit is cleared when the LSR is read AND the character with the error is at the top of the receiver FIFO AND there are no subsequent errors in the FIFO.
6	TEMT	The transmitter empty bit. This bit is set in FIFO mode whenever the Transmitter Shift Register and the FIFO are both empty. In non-FIFO mode, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	THRE	The transmitter holding register empty bit. When set, indicates the UART controller can accept a new character for transmission. This bit is set whenever data is transferred from the THR to the transmit shift register and no new data has been written to the THR. This also causes a THRE Interrupt to occur, if enabled.
4	BI	The break interrupt bit. This bit is set whenever the serial input (SIN) is held in a logic zero state for longer than the sum of (start time + data bits + parity + stop bits). A break condition on SIN causes one, and only one character, consisting of all zeros which will be received by the UART. In FIFO mode, the character associated with the break condition is carried through FIFO and revealed when the character reaches the top of FIFO. Reading the LSR clears the BI bit. In non-FIFO mode, the BI direction occurs immediately and continues until the LSR has been read.
3	FE	The framing error bit. This bit is set whenever there is a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In FIFO mode, the framing error associated with the character received will come to the top of FIFO so it can be noticed. The OE, PE and FE bits are reset when a read of the LSR is performed.
2	PE	The parity error bit. This bit is set whenever there is a parity bit error in the receiver if the Parity Enable (PEN) bit in the LCR is set. In FIFO mode, the parity error associated with the character received will come to the top of FIFO so it can be noticed.
1	OE	The overrun error bit. When set, indicates an overrun error has occurred because a new data character was received before the previous data was read. In non-FIFO mode, this bit is set when a new character arrives in the receiver before the previous character has been read from the RBR. In FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives in the receiver. The data in FIFO is retained and the data in the receive shift register is lost.
0	DR	The data ready bit. When set, indicates that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty when in FIFO mode.

4.2.11 Modem Status (MSR)

Address: 0x18020018
Access: Read/Write
Reset: 0x0

This register contains the current status of the modem control input lines and notes whether they have changed.

Bit	Bit Name	Description
31:8	RES	Reserved
7	DCD	Contains information on the current state of the modem control lines; this bit is the compliment of DCD_L
6	RI	Contains information on the current state of the modem control lines; this bit is the compliment of RI_L
5	DSR	Contains information on the current state of the modem control lines; this bit is the compliment of DSR_L
4	CTS	Contains information on the current state of the modem control lines; this bit is the compliment of CTS_L
3	DDCD	Notes whether the modem control line DCD_L has changed since the last time the CPU read the MSR
2	TERI	Indicates whether RI_L has changed from an active low to an inactive high state since the last time the MSR was read
1	DDSR	Notes whether the modem control line DSR_L has changed since the last time the CPU read the MSR
0	DCTS	Notes whether the modem control line CTS_L has changed since the last time the CPU read the MSR

4.3 GPIO Registers

Table 4-4 summarizes the GPIO registers for the AR7242.

Table 4-4. **GPIO Registers Summary**

Address	Name	Description	Page
0x18040000	GPIO_OE	General Purpose I/O Output Enable	page 45
0x18040004	GPIO_IN	General Purpose I/O Input Value	page 45
0x18040008	GPIO_OUT	General Purpose I/O Output Value	page 46
0x1804000C	GPIO_SET	General Purpose I/O Per Bit Set	page 46
0x18040010	GPIO_CLEAR	General Purpose I/O Per Bit Clear	page 46
0x18040014	GPIO_INT	General Purpose I/O Interrupt Enable	page 46
0x18040018	GPIO_INT_TYPE	General Purpose I/O Interrupt Type	page 46
0x1804001C	GPIO_INT_POLARITY	General Purpose I/O Interrupt Polarity	page 47
0x18040020	GPIO_INT_PENDING	General Purpose I/O Interrupt Pending	page 47
0x18040024	GPIO_INT_MASK	General Purpose I/O Interrupt Mask	page 47
0x18040028	GPIO_FUNCTION_1	General Purpose I/O Function	page 48
0x1804002C	ETH_LED	General Purpose I/O Input Value	page 48
0x18040030	GPIO_FUNCTION_2	Extended GPIO Function Control	page 49

4.3.1 General Purpose I/O Output Enable (GPIO_OE)

Address: 0x18040000
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:20	RES	Must to set to zero	
19:0	OE	Per bit output enable; bits [19:18] must be set to 0x3 by software; bits [17:13] cannot be set as inputs.	
		0	The bit is used as input
		1	Enables the bit as output

4.3.2 General Purpose I/O Input Value (GPIO_IN)

Address: 0x18040004
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:20	RES	Reserved
19:18	IN	Current values of each of the GPIO pins (along with bits [12:0])
17:13	RES	Reserved; output only
12:0	IN	Current values of each of the GPIO pins (along with bits [19:18])

4.3.3 General Purpose I/O Output Value (GPIO_OUT)

Address: 0x18040008
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:20	RES	Reserved
19:0	OUT	Driver output value If the corresponding bit in the OE register is set to 1, the GPIO pin will drive the value in the corresponding bit of this register

4.3.4 General Purpose I/O Per Bit Set (GPIO_SET)

Address: 0x1804000C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:20	RES	Reserved
19:0	SET	On a write, any bit that is set causes the corresponding GPIO bit to be set; any bit that is not set will have no effect

4.3.5 General Purpose I/O Per Bit Clear (GPIO_CLEAR)

Address: 0x18040010
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:20	RES	Reserved
19:0	CLEAR	On a write, any bit that is set causes the corresponding GPIO bit to be cleared; any bit that is not set will have no effect. Bits [19:18] must be set to 0x3 initially to cause these output values to be 0.

4.3.6 General Purpose I/O Interrupt Enable (GPIO_INT)

Address: 0x18040014
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:20	RES	Reserved
19:0	INT	Each bit that is set is considered an interrupt ORd into the GPIO interrupt line

4.3.7 General Purpose I/O Interrupt Type (GPIO_INT_TYPE)

Address: 0x18040018
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:20	RES	Reserved	
19:0	TYPE	0	Indicates the bit is a edge-sensitive interrupt
		1	Indicates the bit is an level-sensitive interrupt

4.3.8 General Purpose I/O Interrupt Polarity (GPIO_INT_POLARITY)

Address: 0x1804001C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:20	RES	Reserved	
19:0	POLARITY	0	Indicates that the interrupt is active low (level) or falling edge (edge)
		1	Indicates that the interrupt is active high (level) or rising edge (edge)

4.3.9 General Purpose I/O Interrupt Pending (GPIO_INT_PENDING)

Address: 0x18040020
Access: Read/Write (See field description)
Reset: 0x0

Bit	Bit Name	Description
31:20	RES	Reserved
19:0	PENDING	For each bit, indicates that an interrupt is currently pending; for edge-sensitive interrupts, this register is read-with-clear

4.3.10 General Purpose I/O Interrupt Mask (GPIO_INT_MASK)

Address: 0x18040024
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:20	RES	Reserved
19:0	MASK	For each bit that is set, the corresponding interrupt in the register "General Purpose I/O Interrupt Pending (GPIO_INT_PENDING)" is passed on to the central interrupt controller

4.3.11 GPIO Function (GPIO_FUNCTION_1)

Address: 0x18040028
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31	SPDIF2TCK	Enable SPDIF_OUT on the pin TCK	
30	SPDIF_EN	Enable GPIO_13 or TCK as the SPDIF serial output	
29:28	RES	Reserved; must be set to zero	
27	I2S_MCKEN	Enable master audio CLK_MCK to be output through GPIO_11; works only if I2S0_EN (bit [26]) is also set	
26	I2S0_EN	Enable bits [12:11] and bits [8:6] as I^2S interface pins:	
		Bit [6]	BITCLK (Input/Output)
		Bit [7]	WS (Input/Output)
		Bit [8]	SD (Output)
		Bit [11]	MCK (Input/Output)
		Bit [12]	MICIN (Input)
25	LED_DUPL	LED signal to select whether Link, Activity, or both must be indicated in the LED. Selects the LED_DUPLEXN_O signal to go out as LED signals; if inactive, LED_LINK100N_O and LED_LINK10N_O is the default signal going out	
24	LED_COLL	LED signal to select whether Link, Activity, or both must be indicated in the LED. Select the LED_COLN_O signal to go out as LED signals; if inactive, LED_LINK100N_O and LED_LINK10N_O is the default signal going out	
23	LED_ACTV	LED signal to select whether Link, Activity, or both must be indicated in the LED. Select the LED_ACTN_O signal to go out as LED signals; if inactive, LED_LINK100N_O and LED_LINK10N_O is default signal going out	
22:19	RES	Reserved	
18	SPI_EN	Enables SPI Interface signals in GPIO_2, GPIO_3, GPIO_4, and GPIO_5	
17:16	RES	Reserved	
15	RES	Reserved; set to 1	
14	RES	Reserved	
13	SPI_CS_EN1	Enables additional SPI chip select on GPIO_0	
12:8	RES	Reserved	
7:4	RES	Reserved; set to 0	
3	LED0_EN	Enable Ethernet MAC/PHY LED data on GPIO_13	
2	UART_RTS_CTS_EN	Enable UART RTS/CTS IO on GPIO_11 (RTS) and GPIO_12 (CTS)	
1	UART_EN	Enable UART IO on GPIO_9 (SIN) and GPIO_10 (SOUT)	
0	EJTAG_DISABLE	Disable EJTAG port functionality to enable GPIO functionality; can be set to 1 to enable using GPIO_5, GPIO_6, and GPIO_7 as GPIO pins	

4.3.12 General Purpose I/O Input Value (ETH_LED)

Address: 0x1804002C
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:20	RES	Reserved
19:15	LINK	Current value of LED_LINK100N_O and LED_LINK10N_O
14:10	DUPL	Current value of LED_DUPLEXN_O
9:5	COLL	Current value of LED_COLN_O
4:0	ACTV	Current value of LED_ACTN_O

4.3.13 Extended GPIO Function Control (GPIO_FUNCTION_2)

Address: 0x18040030
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:6	RES	Reserved
5	I2SD_ON_12	Enables I2S_SD output signal on GPIO_12
4	EN_I2WS_ON_0	Enables I2S_WS on GPIO_0
3	EN_I2SCK_ON_1	Enables I2S_CK Out on GPIO_1
2	RES	Reserved
1	I2S_ON_LED	Brings out I^2S-related signals on the pins GPIO_14, GPIO_15, and GPIO_16
0	DIS_MIC	Disables MIC

4.4 PLL Control Registers

Table 4-5 summarizes the PLL registers for the AR7242.

Table 4-5. **PLL Control Registers Summary**

Address	Name	Description	Page
0x18050000	CPU_PLL_CONFIG	CPU Phase Lock Loop Configuration	page 51
0x18050004	ETH_USB_PLL_CONFIG	ETH_USB Phase Lock Loop Configuration	page 52
0x18050008	CPU_CLOCK_CONTROL	CPU Clock Configuration	page 52
0x18050010	PCIE_PLL_CONFIG	PCIE Phase Lock Loop Configuration	page 53
0x18050014	PCIE_PLL_MAX_LIMIT	PCIE PLL Dither Max Limit	page 53
0x18050018	PCIE_PLL_MIN_LIMIT	PCIE PLL Dither Min Limit	page 54
0x1805001C	PCIE_PLL_DITHER_STEP	PCIE PLL Dither Update Step	page 54
0x18050020	LDO_POWER_CONTROL	LDO Power Control	page 54
0x18050028	CURRENT_PCIE_PLL_DITHER	Current PCIE PLL Dither	page 54
0x18050030	AUDIO_PLL_CONFIG	AUDIO Phase Lock Loop Configuration	page 55
0x18050034	AUDIO_PLL_MODULATION	Audio PLL Modulation	page 55
0x18050038	AUDIO_PLL_MOD_STEP	Audio PLL Frequency Control Step	page 56
0x1805003C	CURRENT_AUDIO_PLL _MODULATION	Current Audio Modulation Logic Output	page 56

4.4.1 CPU Phase Lock Loop Configuration (CPU_PLL_CONFIG)

Address: 0x18050000
Access: Read/Write
Reset: 0x0

This register provides access to the PLL setup control signals. Any write to this register freezes all high speed clocks for 61 µs; clock select lines and PLL control lines change after 30.5 µs, then another 30.5 µs passes before enabling to allow the clocks to settle.

CPU clock frequency, CPU_CLK = (DIV/REFDIV)*REF_CLK/2. For example, REF_CLK is 400 MHz, DIV is 100, REFDIV is 5; (100/5) * 40/2 = 400 MHz. Changing the DIV to 105 gets 21 * 20 = 420 MHz.

To update the PLL, following is an example:

- Set RESET[25] = 1, BYPASS[16] = 1, required frequency set DIV[9:0] = 0x28 (for 400 MHz operation), write 0x02090828 to register 0x18050000
- Take it out of reset, write 0x00090828 to register 0x18050000
- Take it out of bypass, write 0x00000828 to register 0x18050000

This sets CPU_CLK to 400 MHz, AHB clock = CPU_CLK/2 = 200 MHz, DDR_CLK = dual edge = 400 MHz.

Bit	Bit Name	Reset	Description	
31:26	RES	0x0	Reserved	
25	RESET	0x1	CPU PLL reset	
24:23	RES	0x0	Reserved	
22	DDR_DIV_SEL	0x1	DDR clock divisor	
			0	Divide-by-1
			1	Divide-by-2
21:20	RES	0x0	Reserved	
19	AHB_DIV	0x1	AHB clock divisor	
			0	Divide-by-2
			1	Divide-by-4
18	NOPWD	0x0	Prevents the PLL from being powered down when PLL bypass is asserted or when in light sleep	
17	UPDATING	0x0	Set during the PLL update process; after software writes PLL_CONTROL, it takes ~45 µs for the update to occur. Software may poll this bit to see if the update has taken place.	
			0	PLL update is pending
			1	PLL update is complete
16	BYPASS	0x1	Bypass PLL Defaults to 1 for test purposes; software must enable the PLL for normal operation	
15:14	RES	0x0	Reserved	
13:10	REFDIV	0x2	Reference clock divider	
9:0	DIV	0x1E	Primary multiplier	

4.4.2 ETH_USB Phase Lock Loop Configuration (ETH_USB_PLL_CONFIG)

Address: 0x18050004
Access: Read/Write
Reset: See field description

This register provides access to the PLL setup control signals. Any write to this register freezes all high speed clocks for 61 µs. The clock select lines and PLL control lines will change after 30.5 µs, then another 30.5 µs passes before enable to allow the clocks to settle. This PLL generates 24 MHz and 25 MHz for USB and Ethernet, respectively. These REFDIV and DIV values should not be changed at any point.

Bit	Bit Name	Reset	Description
31:26	RES	0x0	Reserved
25	RESET	0x1	USB PLL reset
24:20	RES	0x0	Reserved
19	PLL_RESET	0x1	Reset the PLL dividers
18	NOPWD	0x0	Prevents the PLL from being powered down when PLL bypass is asserted or when in light sleep
17	UPDATING	0x0	[Read-only bit] Set during the PLL update process; after software writes PLL_CONTROL, it takes ~45 µs for the update to occur. Software may poll this bit to see if the update has taken place. 0 PLL update is pending 1 PLL update is complete
16	BYPASS	0x1	Bypass PLL Defaults to 1 for test purposes; software must enable the PLL for normal operation
15:14	RES	0x0	Reserved
13:10	REFDIV	0x2	Reference clock divider
9:0	DIV	0x2E	Primary multiplier

4.4.3 CPU Clock Configuration (CPU_CLOCK_CONTROL)

Address: 0x18050008
Access: Read/Write
Reset: 0x0

This register controls the clock and reset to the CPU. These bits are controlled by driver software.

Bit	Bit Name	Description
31:2	RES	Reserved
1	RESET_SWITCH	Reset during clock switch trigger
0	CLOCK_SWITCH	Clock switch enables switching from the basic REF_CLK to the CPU_PLL clock after the CPU_PLL clock is stable

4.4.4 PCIE Phase Lock Loop Configuration (PCIE_PLL_CONFIG)

Address: 0x18050010
Access: Read/Write
Reset: See field description

This register provides access to the PLL setup control signals. Any write to this register freezes all high speed clocks for 61 µs. The clock select lines and PLL control lines will change after 30.5 µs, then another 30.5 µs passes before enable to allow the clocks to settle.

Bit	Bit Name	Reset	Description
31:26	RES	0x0	Reserved
25	RESET	0x1	PCIE PLL reset
24:19	RES	0x0	Reserved
18	NOPWD	0x0	Prevents the PLL from being powered down when pllbypass is asserted or when in light sleep
17	UPDATING	0x0	[Read-only bit] This bit is set during the PLL update process After software writes PLL_CONTROL, it takes about 45 µs for the update to occur; software may poll this bit to see if the update has taken place 0 PLL update is complete 1 PLL update is pending
16	BYPASS	0x1	Bypass PLL This defaults to 1 for test purposes; software must enable the PLL for normal operation
15:14	RES	0x0	Reserved
13:10	REFDIV	0x4	Reference clock divider
9:0	DIV	0x50	Primary multiplier

4.4.5 PCIE PLL Dither Max Limit (PCIE_PLL_MAX_LIMIT)

Address: 0x18050014
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31	EN_DITHER	1	Disables Dither logic If disabled, either the MAX value or the MIN value is used, depending on the USE_MAX bit setting.
30	USE_MAX	1	Forces the Max value specified to be used. This bit is effective only when EN_DITHER (bit [31]) is set to zero.
29:25	RES	0x0	Reserved
24:15	DIVINT_MAX	19	Integer part max limit; ideally this should be set to 19
14:0	DIVFRAC_MAX	0x0	Fractional part max limit; ideally this should be set to 32758

4.4.6 PCIE PLL Dither Min Limit (PCIE_PLL_MIN_LIMIT)

Address: 0x18050018
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved
23:16	DIVINT_MIN	19	Integer part min limit
15:0	DIVFRAC_MIN	29498	Fractional part min limit

4.4.7 PCIE PLL Dither Update Step (PCIE_PLL_DITHER_STEP)

Address: 0x1805001C
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:28	UPDATE_COUNT	0x0	Specifies the number of sigma-delta clocks per update
24:15	STEP_INT	0x0	Integer part of the step value of the divider
14:0	STEP_FRAC	010	Specifies the quantum by which the fractional part of the fractional divider needs to be updated for each update

4.4.8 LDO Power Control (LDO_POWER_CONTROL)

Address: 0x18050020
Access: Read-Only
Reset: See field description

Bit	Bit Name	Reset		Description
31:3	RES	0x0	Reserved	
2:1	CPU_REFSEL	0x3	Indicates the CPU/DDR reference voltage selected	
0	DDR1_SEL	0x1	This bit indicates whether DDR1 or DDR2 is selected on the board	
			0	DDR2 is selected
			1	DDR1 is selected

4.4.9 Current PCIE PLL Dither (CURRENT_PCIE_PLL_DITHER)

Address: 0x18050028
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:25	RES	Reserved
24:15	INT	Indicates the integer part of the DivInt to the PCIE PLL
14:0	FRAC	Indicates the fractional part of the DivFrac to the PCIE PLL

4.4.10 ETH_XMII

Address: 0x1805002C
Access: Read/Write
Reset: See field description

Controls the Tx and Rx clock for the MII/GMII/RGMII master mode of GE0. This register should be modified only when GE0 is in reset.

Bit	Bit Name	Reset	Description
31	TX_INVERT	0x0	Determines whether to invert the GTX clock after the TX_DELAY (bits [27:26])
30	GIGE_QUAD	0x0	Determines whether to give a 2 ns shift (clock in the middle of data) to the GTX clock; effective only when GIGE (bit [25]) is set
29:28	RX_DELAY	0x0	Delay buffers in the Rx clock path to adjust against edge/middle-aligned RGMII inputs
27:26	TX_DELAY	0x0	Delay line setting for the GTX clock that goes out with the data
		00	Minimum
		11	Maximum
25	GIGE	0x0	Set only after negotiating for 1000 Mbps connection
24	OFFSET_PHASE	0x0	Start from positive or negative phase, i.e., whether to have a 180° change in addition to phase-delay in bits [11:8]
23:16	OFFSET_COUNT	0x0	Counter value to begin with to phase-delay the GTX clock with respect to the XMII Tx/Rx clock
15:8	PHASE1_COUNT	0x1	No of CLK100 – 1 cycles in the negative-cycle of the XMII Tx/Rx clock
7:0	PHASE0_COUNT	0x1	No of CLK100 – 1 cycles in the positive-cycle of the XMII Tx/Rx clock

4.4.11 AUDIO Phase Lock Loop Configuration (AUDIO_PLL_CONFIG)

Address: 0x18050030
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:10	RES	0x0	Reserved
14:12	EXT_DIV	0x1	External digital divider after AUDIO_PLL_CLK output from audio PLL. A value of 0x1 bypasses the input clock.
11:10	RES	0x0	Reserved; should be set to zero
9:7	POSTPLLDIV	0x8	POST-PLL audio divider
		0x1	Bypass
		0x2	Divide-by-2
		0x3	Divide-by-3
		0x4	Divide-by-4
		0x5	Divide-by-6
		0x6	Divide-by-8
		0x7	Divide-by-12
6	RESET	0x1	AUDIO PLL reset
5	NOPWD	0x1	Prevents the PLL from being powered down
4	BYPASS	0x1	Bypass PLL; defaults to 1 for test purposes. Software must enable the PLL for normal operation.
3:0	REFDIV	0x3	Reference clock divider; should not be changed

4.4.12 Audio PLL Modulation (AUDIO_PLL_MODULATION)

Address: 0x18050034
Access: Read/Write
Reset: See field description

Controls the Jitter behavior of the AUDIO PLL

Bit	Bit Name	Reset	Description	
31:29	RES	0x0	Reserved	
28:11	TGT_DIV_FRAC	0x148FE	Target value of the fractional portion of DIV for audio PLL	
10:1	TGT_DIV_INT	0x14	Target value of the integer portion of DIV for audio PLL	
0	START	0x0	Enable audio modulation	
			0	If this bit is not set, the DIV INT and DIV FRAC inputs to the PLL are directly controlled by the TGT_DIV_INT and TGT_DIV_FRAC bits of this register.
			1	If this bit is set, then the clock modulation logic slowly changes the current INT/FRAC towards TGT_DIV_INT/ TGT_DIV_FRAC in steps specified in the register AUDIO_PLL_MOD_STEP.

4.4.13 Audio PLL Frequency Control Step (AUDIO_PLL _MOD_STEP)

Address: 0x18050038
Access: Read/Write
Reset: See field description

Controls the step size by which the clock modulation logic updates the div int/frac parts when it detects that the current int/frac is different from the target int/frac.

Bit	Bit Name	Reset	Description	
31:14	FRAC	0x1	Fractional part of the divider step value	
13:4	INT	0x0	Integer part of the divider step value	
3:0	UPDATE_CNT	0x0	Update frequency	
			0	Every clock

4.4.14 Current Audio Modulation Logic Output (CURRENT_AUDIO_PLL_MODULATION)

Address: 0x1805003C
Access: Read-Only
Reset: See field description

Current audio modulation logic output.

Bit	Bit Name	Reset	Description
31:29	RES	0x0	Reserved
27:10	FRAC	0x0	Fractional part
9:0	INT	0x1	Integer part

4.5 Reset Registers

Table 4-6 summarizes the reset registers for the AR7242.

Table 4-6. **Reset Registers Summary**

Address	Name	Description	Page
0x18060000	RST_GENERAL_TIMER0	General Purpose Timer 0	page 57
0x18060004	RST_GENERAL_TIMER0_RELOAD	General Purpose Timer 0 Reload	page 57
0x18060008	RST_WATCHDOG_TIMER_CONTROL	Watchdog Timer Control	page 58
0x1806000C	RST_WATCHDOG_TIMER	Watchdog Timer	page 58
0x18060010	RST_MISC_INTERRUPT_STATUS	Miscellaneous Interrupt Status	page 59
0x18060014	RST_MISC_INTERRUPT_MASK	Miscellaneous Interrupt Mask	page 60
0x18060018	RST_GLOBAL_INTERRUPT_STATUS	Global Interrupt Status	page 60
0x1806001C	RST_RESET	Reset	page 61
0x18060090	RST_REVISION_ID	Chip Revision ID	page 61
0x18060094	RST_GENERAL_TIMER1	General Purpose Timer 1	page 57
0x18060098	RST_GENERAL_TIMER1_RELOAD	General Purpose Timer 1 Reload	page 57
0x1806009C	RST_GENERAL_TIMER2	General Purpose Timer 2	page 57
0x180600A0	RST_GENERAL_TIMER2_RELOAD	General Purpose Timer 2 Reload	page 57
0x180600A4	RST_GENERAL_TIMER3	General Purpose Timer 3	page 57
0x180600A8	RST_GENERAL_TIMER3_RELOAD	General Purpose Timer 3 Reload	page 57

4.5.1 General Purpose Timers (RST_GENERAL_TIMERx)

Timer0 Address: 0x18060000
Timer1 Address: 0x18060094
Timer2 Address: 0x1806009C
Timer3 Address: 0x180600A4
Access: Read/Write
Reset: 0x0

This timer counts down to zero, sets, interrupts, and then reloads from the register "General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx)". This definition holds true for timer0, timer1, timer2, and timer3.

Bit	Bit Name	Description
31:0	TIMER	Timer value

4.5.2 General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx)

Timer0 Reload Address: 0x18060004
Timer1 Reload Address: 0x18060098
Timer2 Reload Address: 0x180600A0
Timer3 Reload Address: 0x180600A8
Access: Read/Write
Reset: 0x0

This register contains the value that will be loaded into the register "General Purpose Timers (RST_GENERAL_TIMERx)" when it decrements to zero. This definition holds true for timer0, timer1, timer2, and timer3.

Bit	Bit Name	Description
31:0	RELOAD_VALUE	Timer reload value

4.5.3 Watchdog Timer Control Register (RST_WATCHDOG_TIMER_CONTROL)

Address: 0x18060008
Access: See field description
Reset: 0x0

Sets the action to take when the watchdog timer reaches zero. The options are reset, non-maskable interrupt and general purpose interrupt after reaching zero.

Bit	Bit Name	Type	Description	
31	LAST	RO	Indicates if the last reset was due to a watchdog timeout	
30:2	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
1:0	ACTION	RW	The action to be taken after the timer reaches zero	
			00	No action
			01	General purpose interrupt
			10	Non-maskable interrupt
			11	Full chip reset, same as power-on reset

4.5.4 Watchdog Timer Register (RST_WATCHDOG_TIMER)

Address: 0x1806000C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	TIMER	Counts down to zero and stays at zero until the software sets this timer to another value. These bits should be set to a non-zero value before updating the "Watchdog Timer Control Register (RST_WATCHDOG_TIMER_CONTROL)" register to a non-zero number.

4.5.5 Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS)

Address: 0x18060010
Access: Read/Write-to-Clear
Reset: 0x0

Sets the current state of the interrupt lines that are combined to form the MiscInterupt to the processor. All bits of this register need a write to clear.

Bit	Bit Name	Description
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.
12	ETH_MAC_INT	The interrupt generated by the Ethernet MAC/PHY.
11	RES	Reserved. Must be written with zero. Contains zeros when read.
10	TIMER3_INT	The interrupt corresponding to General Purpose Timer3. This bit is cleared after being read. The timer has been immediately reloaded from the "General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx)" register.
9	TIMER2_INT	The interrupt corresponding to General Purpose Timer2. This bit has been cleared after being read. The timer will be immediately reloaded from the "General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx)" register.
8	TIMER1_INT	The interrupt corresponding to General Purpose Timer1. This bit has been cleared after being read. The timer will be immediately reloaded from the "General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx)" register.
7:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PC_INT	CPU performance counter interrupt. Generated whenever either of the internal CPU performance counters have bit [31] set. The relevant performance counter must be reset to clear this interrupt.
4	WATCHDOG_ INT	The watchdog timer interrupt. This interrupt is generated when the watchdog timer reaches zero and the watchdog configuration register is configured to generate a general-purpose interrupt.
3	UART_INT	The UART interrupt. UART interrupt registers must be read before this interrupt can be cleared.
2	GPIO_INT	The GPIO interrupt. Individual lines must be masked before this interrupt can be cleared.
1	RES	Reserved
0	TIMER_INT	Interrupt occurring in correspondence to the general purpose timer0. This bit is cleared after being read. The timer has already been reloaded from the "General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx)" register.

4.5.6 Miscellaneous Interrupt Mask (RST_MISC_INTERRUPT_MASK)

Address: 0x18060014
Access: Read/Write
Reset: 0x0

Enables or disables a propagation of interrupts in the "Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS)" register.

Bit	Bit Name	Description
31:11	RES	Reserved. Must be written with zero. Contains zeros when read.
12	ETH_MAC_INT_MASK	Enables the interrupt generated by the Ethernet MAC/PHY
11	RES	Reserved
10	TIMER3_MASK	When set, enables Timer3 interrupt
9	TIMER2_MASK	When set, enables Timer2 interrupt
8	TIMER1_MASK	When set, enables Timer1 interrupt
7	MBOX_MASK	When set, enables MBOX interrupt
6	RES	Reserved
5	PC_MASK	When set, enables CPU performance counter interrupt
4	WATCHDOG_ MASK	When set, enables watchdog interrupt
3	UART_MASK	When set, enables UART interrupt
2	GPIO_MASK	When set, enables GPIO interrupt
1	RES	Reserved
0	TIMER_MASK	When set, enables timer interrupt

4.5.7 Global Interrupt Status (RST_GLOBAL_INTERRUPT_STATUS)

Address: 0x18060018
Access: Read-Only
Reset: 0x0

This register reflects the CPU 6-bit interrupt input.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	TIMER_INT	Internal count/compare timer interrupt
4	MISC_INT	Miscellaneous interrupt; source of the interrupt available on the "Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS)" register
3	GE1_INT	Ethernet1 interrupt; information available in the Ethernet1 register space
2	GE0_INT	Ethernet0 interrupt; information available in the Ethernet0 register space
1	USB_INT	USB interrupt
0	PCIE_INT	PCIE interrupt

4.5.8 Reset (RST_RESET)

Address: 0x1806001C
Access: Read/Write
Reset: See field description

This register individually controls the reset to each of the chip's submodules.

Bit	Bit Name	Reset	Description
31:29	RES	0x0	Reserved
28	EXTERNAL_RESET	0x0	Commands an external reset (SYS_RST_L pin) immediately; inverted before being sent to the pin.
27:25	RES	0x0	Reserved
24	FULL_CHIP_RESET	0x0	Used to command a full chip reset. This is the software equivalent of pulling the reset pin. The system will reboot with PLL disabled. Always zero when read.
23:22	RES	0x0	Reserved
21	CPU_NMI	0x0	Used to send an NMI to the CPU. Always zero when read. The watchdog timer can also be used to generate NMI/full chip reset.
20	CPU_COLD_RESET	0x0	Used to cold reset the entire CPU. This bit will be cleared automatically immediately after the reset. Always zero when read.
19:17	RES	0x0	Reserved
16	RES	0x0	Reserved
15:14	RES	0x0	Reserved
13	GE1_MAC_RESET	0x1	Used to reset the GE1 MAC
12:11	RES	0x0	Reserved
10	PCIE_PHY_SERIAL_ RESET	0x1	Resets the PCIE PHY Shift reset
9	GE0_MAC_RESET	0x1	Resets the GE0 MAC
8	ETH_MACPHY_ RESET	0x1	Resets the Ethernet MAC/PHY
7	PCIE_PHY_RESET	0x1	Used to reset the PCIE PHY
6	PCIE_RESET	0x1	Used to reset the PCIE host controller. This bit will reset the Endpoint as well.
5	USB_HOST_RESET	0x1	Used to reset the USB controller
4	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
3:0	RES	0x0	Reserved

4.5.9 Chip Revision ID (RST_REVISION_ID)

Address: 0x18060090
Access: Read-Only
Reset: See field description

This register is the revision ID for the chip.

Bit	Bit Name	Reset	Description
31:20	RES	0x0	Reserved
19:4	MAJOR	0x1100	Major revision ID
3:0	MINOR	0x0	Minor revision ID

4.6 MBOX Registers

Table 4-7 summarizes the MBOX registers for the AR7242.

Table 4-7. **MBOX Registers Summary**

Address	Name	Description	Page
0x180A0004	MBOX_FIFO_STATUS	Non-Destructive FIFO Status Query	page 63
0x180A0008	MBOX_DMA_POLICY	Mailbox DMA Engine Policy Control	page 63
0x180A000C	MBOX0_DMA_RX_DESCRIPTOR_BASE	Mailbox 0 Rx DMA Descriptors Base Address	page 64
0x180A0010	MBOX0_DMA_RX_CONTROL	Mailbox 0 Rx DMA Control	page 64
0x180A0014	MBOX0_DMA_TX_DESCRIPTOR_BASE	Mailbox 0 Tx DMA Descriptors Base Address	page 65
0x180A0018	MBOX0_DMA_TX_CONTROL	Mailbox 0 Tx DMA Control	page 65
0x180A001C	MBOX_FRAME	Mailbox FIFO Status	page 65
0x180A0020	FIFO_TIMEOUT	FIFO Timeout Period	page 66
0x180A0024	MBOX_INT_STATUS	MBOX Related Interrupt Status	page 66
0x180A0028	MBOX_INT_ENABLE	MBOX Related Interrupt Enables	page 67
0x180A002C	MBOX_FIFO_RESET	Reset and Clear MBOX FIFOs	page 67

4.6.1 Non-Destructive FIFO Status Query (MBOX_FIFO_STATUS)

Address: 0x180A0004
Access: Read-Only
Reset: 0x0

This register returns the status of the mailbox FIFOs. This register may be read at any time without changing the mailbox state.

Bit	Bit Name	Reset	Description	
31:4	RES	0x0	Reserved	
3:2	EMPTY	0x3	On a read: returns an empty status for the Tx mailbox	
			Bit [3]	MBOX 1 Tx FIFO is empty (I2S1)
			Bit [2]	MBOX 0 Tx FIFO is empty (I2S0)
1:0	FULL	0x3	On a read: returns a full status for the Rx mailbox	
			Bit [1]	MBOX 1 Tx FIFO is full (I2S1)
			Bit [0]	MBOX 0 Tx FIFO is full (I2S0)

4.6.2 Mailbox DMA Engine Policy Control (MBOX_DMA_POLICY)

Address: 0x180A0008
Access: Read/Write
Reset: See field description

Controls the queue service policy of the mailbox DMA engines. The Rx and Tx engines can be programmed independently to service their queues in round robin or strict priority order. The engines can also be programmed to make a new queue choice at the end of messages or individual descriptors. The default mode is round robin decisions being made at the end of each message.

Bit	Bit Name	Reset		Description
31:12	RES	0x0		Reserved
11:8	TX_FIFO_THRESH1	0x4		Threshold for MBOX TX FIFO1 in units of word (a value of 0 maps to 0 bytes, a value of 1 maps to 4 bytes, etc.). Only if this threshold is reached, the MBOX DMA engine will take Tx Chain1 into consideration while making queue service choices
7:4	TX_FIFO_THRESH0	0x4		Threshold for MBOX TX FIFO0 in units of word (a value of 0 maps to 0 bytes, a value of 1 maps to 4 bytes, etc.). Only if this threshold is reached, the MBOX DMA engine will take Tx Chain0 into consideration while making queue service choices
3	TX_QUANTUM	0x0	0	Programming this field to 0 forces the Tx mailbox DMA engine to make queue service choices only at the end of messages (i.e., upon completing descriptors with the EOM bit set)
			1	Programming this field to 1 allows it to make choices upon the completion of every descriptor
2	TX_ORDER	0x0	0	Programming this field to 0 chooses roundrobin and programming
			1	Programming this field to 1 chooses strict priority (queue 0 is the highest priority) service ordering of mailbox Tx queues
1	RX_QUANTUM	0x0	0	Programming this field to 0 forces the Rx mailbox DMA engine to make queue service choices only at the end of messages (i.e., upon completing descriptors with the EOM bit set)
			1	Programming this field to 1 allows it to make choices upon the completion of every descriptor
0	RX_ORDER	0x0	0	Programming this field to 0 chooses round robin and programming
			1	Programming this field to 1 chooses strict priority (queue 0 is the highest priority) service ordering of mailbox Rx queues

4.6.3 Mailbox 0 Rx DMA Descriptors Base Address (MBOX0_DMA_RX_DESCRIPTOR_BASE)

Address: 0x180A000C
Access: Read/Write
Reset: 0x0

Holds the starting address of the descriptor chain for mailbox 0's Rx direction transfers. The DMA engine starts by fetching a descriptor from this address when the START bit in the MBOX0_DMA_RX_CONTROL register is set. All DMA descriptors must be 4-byte aligned, so the register's bottom two bits of the contents, as well as the bottom two bits of the next descriptor field of the individual descriptors are ignored and assumed to be zeros by the DMA engine. For the purposes of the DMA engine, RX direction is defined to be transfers from the chip to the host interface (nominally, data received from the antenna) and the Tx direction is defined to be transfers from the host interface to the chip (nominally, data to be transmitted to the antenna).

Bit	Bit Name	Description
31:28	RES	Reserved
27:2	ADDRESS	Most significant 26 bits of the 4-byte-aligned address of the first descriptor in the DMA chain
1:0	RES	Reserved

4.6.4 Mailbox 0 Rx DMA Control (MBOX0_DMA_RX_CONTROL)

Address: 0x180A0010
Access: Read/Write
Reset: 0x0

Controls the operational state of the DMA engine for mailbox 0's Rx direction transfers. The register should always be written in a one shot manner (only one of the operations should be specified) and can be polled to see if the desired operation has taken effect (indicated by the clearing of the corresponding bit). The DMA engine starts out stopped and must be kicked off for the first time with a START operation. The START operation causes the DMA engine to start fetching a descriptor at the address specified by the "Mailbox 0 Rx DMA Descriptors Base Address (MBOX0_DMA_RX_DESCRIPTOR_BASE)" register. Once this first descriptor has been fetched, if the DMA engine ever catches up with a CPU-owned descriptor, it can be requested to refetch the descriptor that it stalled on by programming the RESUME operation. Software can stop the operation of the DMA engine by programming the STOP operation. When the STOP operation is programmed, the DMA engine stops transfers immediately if it was already idle or at the end of the transfer of the current descriptor it is working on if it was busy. Note that this may leave incomplete messages in the mailbox FIFOs if the message in progress is scattered or gathered across multiple descriptors.

Bit	Bit Name	Description
31:3	RES	Reserved
2	RESUME	Programming a 1 to this field causes a potentially stalled (due to having caught up with CPU-owned descriptors) DMA engine to resume its transfers by refetching the last descriptor it had fetched and found to be CPU-owned. Software can use RESUME operations to add descriptors to the end of the descriptor chain (only modifying CPU-owned descriptors) in a race-free atomic manner. If the RESUME operation is programmed and the DMA engine is not stalled, it has no effect and is automatically cleared.
1	START	Programming a one to this field causes the DMA engine to start transferring data by fetching the descriptor pointed to by the "Mailbox 0 Rx DMA Descriptors Base Address (MBOX0_DMA_RX_DESCRIPTOR_BASE)" register. The START operation should usually be used only when the DMA engine is known to be stopped (after poweron or SOC reset) or after an explicit STOP operation.
0	STOP	Programming a one to this field causes the DMA engine to stop transferring any more data from this descriptor chain (after the current descriptor is completed, if a transfer is already in progress).

4.6.5 Mailbox 0 Tx DMA Descriptors Base Address (MBOX0_DMA_TX_DESCRIPTOR_BASE)

Address: 0x180A0014
Access: Read/Write
Reset: 0x0

See the description for the register "Mailbox 0 Rx DMA Descriptors Base Address (MBOX0_DMA_RX_DESCRIPTOR_BASE)", as applied to mailbox 0's Tx direction transfers.

Bit	Bit Name	Description
31:28	RES	Reserved
27:2	ADDRESS	Most significant 26 bits of the 4-byte-aligned address of the first descriptor in the DMA chain
1:0	RES	Reserved

4.6.6 Mailbox 0 Tx DMA Control (MBOX0_DMA_TX_CONTROL)

Address: 0x180A0018
Access: Read/Write
Reset: 0x0

See the description for the register "Mailbox 0 Rx DMA Control (MBOX0_DMA_RX_CONTROL)".

Bit	Bit Name	Description
31:3	RES	Reserved
2	RESUME	Programming a one to this field causes a potentially stalled (due to having caught up with CPUowned descriptors) DMA engine to resume its transfers by refetching the last descriptor it had fetched and found to be CPU-owned. Software can use RESUME operations to keep adding descriptors to the end of the descriptor chain (only modifying CPUowned descriptors) in a race free atomic manner. If the RESUME operation is programmed and the DMA engine is not stalled, it has no effect and is automatically cleared.
1	START	Programming a one to this field causes the DMA engine to start transferring data by fetching the descriptor pointed to by the "Mailbox 0 Tx DMA Descriptors Base Address (MBOX0_DMA_TX_DESCRIPTOR_BASE)" register. The START operation should usually be used only when the DMA engine is known to be stopped (after poweron or SOC reset) or after an explicit STOP operation.
0	STOP	Programming a one to this field causes the DMA engine to stop transferring any more data from this descriptor chain (after the current descriptor is completed, if a transfer is already in progress).

4.6.7 Mailbox FIFO Status (MBOX_FRAME)

Address: 0x180A001C
Access: Read-Only
Reset: See field description

Bit	Bit Name	Reset	Description
31:4	RES	0x0	Reserved
3:2	RX_EOM	0x0	Rx FIFO contains a data byte with the EOM marker set in the corresponding mailbox
1:0	RX_SOM	0x3	Rx FIFO contains a data byte with the SOM marker set in the corresponding mailbox; a SOM byte always follows an EOM byte from the previous message

4.6.8 FIFO Timeout Period (FIFO_TIMEOUT)

Address: 0x180A0020
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31:9	RES	0x0	Reserved	
8	ENABLE	0x1	0	FIFO timeouts are disabled
			1	FIFO timeouts are enabled
7:0	VALUE	0xFF	Timeout value (in ms) when CORE_CLK = 40 MHz, or in 0.5 ms when CORE_CLK=80 MHz; should never be set to 0	

4.6.9 MBOX Related Interrupt Status (MBOX_INT_STATUS)

Address: 0x180A0024
Access: Read/Write-1-to-Clear
Reset: 0x0

Bit	Bit Name	Description	
31:12	RES	Reserved	
11:10	RX_DMA_COMPLETE	Per-mailbox Rx DMA completion (one descriptor completed) interrupts	
9:8	TX_DMA_EOM_COMPLETE	Per-mailbox Tx DMA completion of EOM (descriptor with EOM flag completed) interrupts	
7:6	TX_DMA_COMPLETE	Per-mailbox Tx DMA completion (one descriptor completed) interrupts	
5	TX_OVERFLOW	MBOX Tx overflow error; the overflow condition is the same as the host interface overflow error	
4	RX_UNDERFLOW	MBOX Rx underflow error; the underflow condition is the same as the host interface underflow error	
3:2	TX_NOT_EMPTY	TX_NOT_EMPTY pending interrupt for each of the Tx mailboxes; bit sets when the MBOX FIFO has no room	
		Bit [0]	MBOX 0 TX_NOT_EMPTY interrupt
		Bit [1]	MBOX 1 TX_NOT_EMPTY interrupt
1:0	RX_NOT_FULL	RX_NOT_FULL pending interrupt for each of the Rx mailboxes; bit sets when one or more exist	
		Bit [0]	MBOX 0 TX_NOT_EMPTY interrupt
		Bit [1]	MBOX 1 TX_NOT_EMPTY interrupt

4.6.10 MBOX Related Interrupt Enables (MBOX_INT_ENABLE)

Address: 0x180A0028
Access: Read/Write
Reset: 0x0

This register is used to mask/enable interrupts to the CPU.

Bit	Bit Name	Description	
31:12	RES	Reserved	
11:10	RX_DMA_COMPLETE	Enable per mailbox Rx DMA completion interrupts	
9:8	TX_DMA_EOM_COMPLETE	Enable per mailbox Tx DMA completion of end of message interrupts	
7:6	TX_DMA_COMPLETE	Enable per mailbox Tx DMA completion interrupts	
5	TX_OVERFLOW	Enable MBOX Tx overflow error	
4	RX_UNDERFLOW	Enable MBOX Rx overflow error	
3:2	TX_NOT_EMPTY	Enable TX_NOT_EMPTY interrupts from MBOX Tx FIFOs	
		Bit [0]	Enable MBOX 0 TX_NOT_EMPTY interrupt
		Bit [1]	Enable MBOX 1 TX_NOT_EMPTY interrupt
1:0	RX_NOT_FULL	Enable RX_NOT_EMPTY interrupts from MBOX RX FIFOs	
		Bit [0]	Enable MBOX 0 RX_NOT_EMPTY interrupt
		Bit [1]	Enable MBOX 1 RX_NOT_EMPTY interrupt

4.6.11 Reset and Clear MBOX FIFOs (MBOX_FIFO_RESET)

Address: 0x180A002C
Access: Read/Write
Reset: 0x0

Resets and clears data from MBOX FIFOs. This register should only be written to when no DMAs are in progress. For stereo applications, it is recommended that MBOX FIFOs be reset at the beginning of each new audio stream (new VoIP call, new song, etc.) The stereo block should also be reset when the FIFOs are reset, to maintain byte alignment.

Bit	Bit Name	Description	
31:4	RES	Reserved	
3:2	RX_INIT	Writing a 1 causes a Rx FIFO reset. The register is automatically reset to 0, and will always return 0 on a read.	
		RX_INIT[0]	Resets MBOX 0
		RX_INIT[1]	Resets MBOX 1
1:0	TX_INIT	Writing a 1 will cause a TX FIFO reset. The register is automatically reset to 0, and will always return 0 on a read.	
		TX_INIT[0]	Resets MBOX 0
		TX_INIT[1]	Resets MBOX 1

4.7 I²S Registers

Table 4-8 summarizes the I²S registers for the AR7242.

Table 4-8. **I²S Registers Summary**

Address	Name	Description	Page
0x180B0000	STEREO0_CONFIG	Configure Stereo Block	page 68
0x180B0004	STEREO0_VOLUME	Set Stereo Volume	page 70
0x180B000C	STEREO0_TX_SAMPLE_CNT_LSB	Tx Sample Counter	page 71
0x180B0010	STEREO0_TX_SAMPLE_CNT_MSB	Tx Sample Counter	page 71
0x180B0014	STEREO0_RX_SAMPLE_CNT_LSB	Rx Sample Counter	page 71
0x180B0018	STEREO0_RX_SAMPLE_CNT_MSB	Rx Sample Counter	page 71

4.7.1 Configure Stereo Block (STEREO0_CONFIG)

Address: 0x180B0000
Access: Read/Write
Reset: See field description

This register controls the basic configuration of the stereo block.

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved
23	SPDIF_ENABLE	0x0	Enables the SPDIF stereo block for operation
22	REFCLK_SEL	0x0	Enables the stereo to choose between an external ref. clock through GPIO and crystal input clock This clock is used as the STEREO_CLK input to the stereo module:
		0	Crystal input
		1	Ref clock provided by the external source through GPIO
21	ENABLE	0x0	Enables operation of the I²S stereo block
20	MIC_RESET	0x0	Resets the MIC buffers
19	RESET	0x0	Resets the stereo buffers and I²S state Should be written to 1 when any of the data word sizes change, or if data synchronization is lost. Hardware will automatically clear to 0.
18	I2S_DELAY	0x1	Delay the Word Select (I2S_WS) output in master mode by one clock of I2S bit clock (I2S_CK)
		0	One I2S_CK delay
		1	No delay
17	PCM_SWAP	0x0	This bit is used for swapping byte order of PCM samples
16	MIC_WORD_SIZE	0x0	Causes configures microphone word size:
		0	16-bit PCM words
		1	32-bit PCM words

15:14	STEREO_MONO	0x0	Causes configures stereo or mono	
			0x0	Stereo
			0x1	Mono from channel 0
			0x2	Mono from channel 1
			0x3	Reserved
13:12	DATA_WORD_SIZE	0x0	Controls the word size loaded into the PCM register from the MBOX FIFO. Data word size:	
			0x0	8 bits/word
			0x1	16 bits/word
			0x2	24 bits/word
			0x3	32 bits/word
11	I2S_WORD_SIZE	0x0	Controls the word size sent to the external I^2S DAC. When set to 32 bit words, the PCM data will be left justified in the I^2S word. I^2S word size:	
			0	16 bits per I^2S word
			1	32 bits per I^2S word
10	MCK_SEL	0x0	When a DAC master clock is required, this field selects the raw clock source between divided audio PLL clock and input master clk (MCLK_IN)	
			0	Raw master clock is divided audio PLL clock
			1	Raw master clock is MCLK_IN
9	SAMPLE_CNT _CLEAR_TYPE	0x0	Indicates the strategy used to clear the sample counter Tx and Rx registers	
			0	Write an explicit zero data through software to the Tx and Rx sample counter registers
			1	A software read of the Tx and Rx sample counter registers clears the counter registers
8	MASTER	0x1	This field controls the I2S_CK and I2S_WS master	
			0	External DAC is the master and drives I2S_CK and I2S_WS
			1	The AR7242 is the master and drives I2S_CK and I2S_WS
7:0	POSEDGE	0x2	Counts in units of MCLK and can be calculated as follows: ■ Identify the relationship between MCLK and I^2S bit clock (I2S_SCK): I2S_SCK = MCLK / DIV Where DIV = MCLK/(SAMPLE_RATE * I2S_WORD_SIZE * 2 channels); a common example: A 44.1 KSps sample rate with 32 bits/word and a 11.2896 MHz MCLK would yield: DIV = 11.2896MHz/(44.1 KSps * 32 bits/word * 2) = 4 ■ Identify the relationship between I2S_SCK and SPDIF_SCK: If I2S_WORD_SIZE=16, then I2S_SCK = SPDIF_SCK / 4 If I2S_WORD_SIZE=32, then I2S_SCK = SPDIF_SCK / 2 Note that SPDIF is always 32 bits per word. ■ Determine the value of this register (POSEDGE): SPDIF_SCK = MCLK/POSEDGE	

4.7.2 Set Stereo Volume (STEREO0_VOLUME)

Address: 0x180B0004
Access: Read/Write
Reset: 0x0

This register digitally attenuates or increases the volume level of the stereo output. Volume is adjusted in 3-db steps. If the gain is set too high, the PCM values saturate and waveform clipping occurs.

Bit	Bit Name	Description	
31:13	RES	Reserved	
12:8	CHANNEL1	Channel 1 gain/attenuation. Setting the gain above +7 is not supported. A 5 bit number; the MSB is a sign bit, the others are magnitude:	
		Binary (Decimal)	**Result**
		11111 (–16)	Maximum attenuation
		11110 (–14)	–84 dB
		...	...
		10001 (–1)	–6 dB
		10000 (0)	0 dB
		00000 (0)	0 dB
		00001 (+1)	+6 dB
		...	...
		00111 (+7)	+42 dB (maximum gain)
		01000 (+8)	Reserved
		...	...
		01111 (+15)	Reserved
7:5	RES	Reserved	
4:0	CHANNEL0	Channel 0 gain/attenuation. Setting the gain above +7 is not supported. A 5 bit number; the MSB is a sign bit, the others are magnitude:	
		Binary (Decimal)	**Result**
		11111 (–16)	Maximum attenuation
		11110 –14)	–84 dB
		...	...
		10001 (–1)	–6 dB
		10000 (0)	0 dB
		00000 (0)	0 dB
		00001 (+1)	+6 dB
		...	...
		00111 (+7)	+42 dB (maximum gain)
		01000 (+8)	Reserved
		...	...
		...	...
		01111 (+15)	Reserved

4.7.3 Tx Sample Counter (STEREO0_TX_SAMPLE_CNT_LSB)

Address: 0x180B000C
Access: Read/Write
Reset: 0x0

This register counts the number of Tx samples transmitted by stereo. This register holds the 16 LSBs of the sample counter.

Bit	Bit Name	Description
31:16	CH1	Holds the 16 LSBs of Tx CH1 sample counter
15:0	CH0	Holds the 16 LSBs of Tx CH0 sample counter; also, these are the 16 LSBs of the sample counter

4.7.4 Tx Sample Counter (STEREO0_TX_SAMPLE_CNT_MSB)

Address: 0x180B0010
Access: Read/Write
Reset: 0x0

This register counts the number of Tx samples transmitted by stereo. This register holds only the 16 MSBs of the sample counter.

Bit	Bit Name	Description
31:16	CH1	Holds the 16 MSBs of Tx CH1 sample counter
15:0	CH0	Holds the 16 MSBs of Tx CH0 sample counter; also, these are the 16 LSBs of the sample counter

4.7.5 Rx Sample Counter (STEREO0_RX_SAMPLE_CNT_LSB)

Address: 0x180B0014
Access: Read/Write
Reset: 0x0

This register counts the number of Rx samples transmitted by stereo. This register holds only the 16 LSBs of the sample counter.

Bit	Bit Name	Description
31:16	CH1	Holds the 16 LSBs of Rx CH1 sample counter
15:0	CH0	Holds the 16 LSBs of Rx CH0 sample counter

4.7.6 Rx Sample Counter (STEREO0_RX_SAMPLE_CNT_MSB)

Address: 0x180B0018
Access: Read/Write
Reset: 0x0

This register counts the number of Rx samples transmitted by stereo. This register holds only the 16 MSBs of the sample counter.

Bit	Bit Name	Description
31:16	CH1	Holds the 16 MSBs of Rx CH1 sample counter
15:0	CH0	Holds the 16 MSBs of Rx CH0 sample counter

4.8 PCIE Configuration Space Registers

Table 4-9 shows the PCI Express configuration space registers for the AR7242.

Table 4-9. **PCIE Configuration Space Registers**

Offset	Description	Page
0x180C0000	Vendor ID	page 72
0x180C0002	Device ID	page 72
0x180C0004	Command	page 73
0x180C0006	Status	page 73
0x180C0008	Revision ID	page 74
0x180C0009	Class Code	page 74
0x180C000C	Cache Line Size	page 74
0x180C000D	Master Latency Timer	page 74
0x180C000E	Header Type	page 74
0x180C0010	Base Address 0 (Read-Only)	page 75
0x180C0010	BAR0 Mask (Write-Only)	page 75
0x180C0018	Bus Number	page 76
0x180C001E	Secondary Status	page 76
0x180C0020	Memory Base	page 76
0x180C0022	Memory Limit	page 76
0x180C0024	Prefetchable Memory Base	page 77
0x180C0026	Prefetchable Memory Limit	page 77
0x180C0034	Capability Pointer	page 77
0x180C003C	Interrupt Line	page 77
0x180C003D	Interrupt Pin	page 78
0x180C003E	Bridge Control	page 78

4.8.1 Vendor ID

Address: 0x180C000
Access: Read-Only

The default value is the hardware configuration parameter.

Bit	Bit Name	Description
15:0	CX_VENDOR_ID_0	Vendor ID

4.8.2 Device ID

Address: 0x180C0002
Access: Read-Only

The default value is the hardware configuration parameters.

Bit	Bit Name	Description
15:0	CX_DEVICE_ID_0	Device ID

4.8.3 Command

Address: 0x180C0004
Access: See field description
Reset: 0

Bit	Access	Description
15:11	RO	Reserved
10	R/W	INTx assertion disable
9	RO	Fast back-to-back enable Not applicable for PCIE. Hardwired to 0.
8	R/W	SERR# enable
7	RO	IDSEL stepping/wait cycle control Not applicable for PCIE. Hardwired to 0.
6	R/W	Parity error response
5	RO	VGA palette snoop Not applicable for PCIE. Hardwired to 0.
4	RO	Memory write and invalidate Not applicable for PCIE. Hardwired to 0.
3	RO	Special cycle enable Not applicable for PCIE. Hardwired to 0.
2	R/W	Bus master enable
1	R/W	Memory space enable
0	R/W	I/O space enable

4.8.4 Status

Address: 0x180C0006
Access: See field description
Reset: See field description

Bit	Access	Reset	Description
15	RW1C	0	Detected parity error
14	RW1C	0	Signalled system error
13	RW1C	0	Received master abort
12	RW1C	0	Received target abort
11	RW1C	0	Signalled target abort
10:9	RO	0x0	DEVSEL timing; not applicable for PCIE. Hardwired to 0.
8	RW1C	0	Master data parity error
7	RO	0	Fast back-to-back capable; not applicable for PCIE. Hardwired to 0.
6	RO	0	Reserved
5	RO	0	66 MHz capable; not applicable for PCIE. Hardwired to 0.
4	RO	1	Capabilities list Indicates presence of an extended capability item. Hardwired to 1.
3	RO	0	INTx status
2:0	RO	0x0	Reserved

4.8.5 Revision ID

Address: 0x180C0008
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
7:0	CX_REVISION_ID_0	Revision ID

4.8.6 Class Code

Address: 0x180C0009
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
23:16	BASE_CLASS_CODE_0	Base class code
15:8	SUB_CLASS_CODE_0	Sub class code
7:0	IF_CODE_0	Programming interface

4.8.7 Class Line Size

Address: 0x180C000C
Access: Read/Write
Reset: 0x0

Bit	Description
7:0	Cache line size This register is R/W for legacy compatibility purposes and is not applicable to PCI Express device functionality. Writing to the Cache Line Size register does not impact functionality of the RC.

4.8.8 Master Latency Timer

Address: 0x180C000D
Access: Read-Only
Reset: 0x0

Bit	Description
7:0	Master latency timer; not applicable to PCIE. Hardwired to 0.

4.8.9 Header Type

Address: 0x180C000E
Access: Read-Only
Reset: See field descriptions

Bit	Reset	Description
7	0x0	Multi-function device
6:0	0x01	Configuration header format. Hardwired to 0x01.

4.8.10 Base Address 0 (BAR0)

Address: 0x180C0010
Access: Read-Only
Reset: See field descriptions

The RC Core provides one 32-bit base address register.

Bit	Reset	Description	
31:4	0x0000000	BAR0 base address bits. The BAR0 mask value determines which address bits are masked.	
3	PREFETCHABLE0_0 for memory BAR	If BAR0 is a memory BAR, indicates if the memory region is prefetchable:	
		0	Non-prefetchable
		1	Prefetchable
2:1	BAR0_TYPE_0 for memory BAR	If BAR 0 is a memory BAR, bits [2:1] determine the BAR type:	
		00	32-bit BAR
		10	Unused
0	MEM0_SPACE _DECODER_0	0	BAR0 is a memory BAR
		1	Unused

4.8.11 BAR0 Mask

Address: 0x180C0010 (same as "Base Address 0 (BAR0)"
Access: Write-Only
Reset: See field descriptions

Determines which bits in the BAR are non-writable by host software, which determines the size of the address space claimed by the BAR. This register only exists when the corresponding BAR*n*_MASK_WRITABLE_0 value is 1. Otherwise, the BAR*n*_MASK_0 value sets the BAR Mask value in hardware.

BAR Mask values indicate the range of low-order bits in each implemented BAR to not use for address matching. The BAR Mask value also indicates the range of low-order bits in the BAR that cannot be written from the host. The application can write to all BAR bits to set memory, I/O, and other BAR options. To disable a BAR, the application can write a 0 to bit [0] of the BAR Mask register. To change the BAR Mask value for a disabled BAR, the application must first enable the BAR by writing 1 to bit [0]. After enabling the BAR, the application can write a new value to the BAR Mask register. If the BAR Mask value for a BAR is less than that required for the BAR type, the RC Core uses the minimum BAR type value:

- BAR bits [11:0] are always masked for a memory BAR. The RC Core requires each memory BAR to claim at least 4 KB
- BAR bits [7:0] are always masked for an I/O BAR. The RC Core requires each I/O BAR to claim at least 256 bytes

Bit	Bit Name	Description	
31:1	BAR0 _MASK_0	Indicates which BAR0 bits to mask (make nonwritable) from host software, which in turn determines the size of the BAR. For example, writing 0xFFF to the BAR0 Mask register claims a 4096-byte BAR by masking bits 11:0 of the BAR from writing by host software. Application write access depends on the value of BAR0_MASK_WRITABLE_0: ■ If BAR0_MASK_WRITABLE_0 = 1, the BAR0 Mask register is writable ■ If BAR0_MASK_WRITABLE_0 = 0, BAR0 Mask is not writable	
0	BAR0 _ENABLED _0	BAR0 enable	
		0	BAR0 is disabled
		1	BAR0 is enabled
		Bit [0] is interpreted as BAR enable when writing to the BAR Mask register rather than as a mask bit because bit [0] of a BAR is always masked from writing by host software.	

4.8.12 Bus Number

Address: 0x180C0018
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
31:24	RO	Secondary latency timer; not applicable to PCI Express, hardwired to 0x00.
23:16	R/W	Subordinate bus number
15:8	R/W	Secondary bus number
7:0	R/W	Primary bus number

4.8.13 Secondary Status

Address: 0x180C001E
Access: See field descriptions
Reset: 0

Bit	Access	Description
15	RW1C	Detected parity error
14	RW1C	Received system error
13	RW1C	Received master abort
12	RW1C	Received target abort
11	RW1C	Signalled timer abort
10:9	RO	DEVSEL timing; not applicable to PCIE. Hardwired to 0.
8	RW1C	Master data parity error
7	RO	Fast back-to-back capable; not applicable to PCIE. Hardwired to 0.
6	RO	Reserved
5	RO	66 MHz; not applicable to PCIE. Hardwired to 0.
4:0	RO	Reserved

4.8.14 Memory Base

Address: 0x180C0020
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
15:4	R/W	Memory base address
3:0	RO	Reserved

4.8.15 Memory Limit

Address: 0x180C0022
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
15:5	R/W	Memory limit address
4:0	RO	Reserved

4.8.16 Prefetchable Memory Base

Address: 0x180C0024
Access: See field descriptions
Reset: See field descriptions

Bit	Access	Default	Description	
15:4	R/W	0x000	Upper 12 bits of 32-bit prefetchable memory start address	
3:1	RO	0x0	Reserved	
0	RO	MEM_DECODE_64_0	64-bit memory addressing	
			0	32-bit memory addressing
			1	Unused

4.8.17 Prefetchable Memory Limit

Address: 0x180C0026
Access: See field descriptions
Reset: See field descriptions

Bit	Access	Default	Description	
15:4	R/W	0x000	Upper 12 bits of 32-bit prefetchable memory end address	
3:1	RO	0x0	Reserved	
0	RO	MEM_DECODE_64_0	64-bit memory addressing	
			0	32-bit memory addressing
			1	Unused

4.8.18 Capability Pointer

Address: 0x180C0034
Access: Read-Only
Reset: 0x40

Bit	Description
7:0	First capability pointer Points to power management capability structure by default.

4.8.19 Interrupt Line

Address: 0x180C003C
Access: Read/Write
Reset: 0xFF

Bit	Description
7:0	Interrupt line

4.8.20 Interrupt Pin

Address: 0x180C003D
Access: Read-Only
Reset: 0x1

Bit	Description	
7:0	Interrupt pin. Identifies the legacy interrupt Message that the device uses. Valid values are:	
	00	The device does not use legacy interrupt
	01	The device uses INTA

4.8.21 Bridge Control

Address: 0x180C003E
See field descriptions
Reset: 0x0

Bit	Access	Description
15:12	RO	Reserved
11	RO	Discard timer SERR enable status; not applicable to PCIE. Hardwired to 0.
10	RO	Discard timer status; not applicable to PCIE. Hardwired to 0.
9	RO	Secondary discard timer; not applicable to PCIE. Hardwired to 0.
8	RO	Primary discard timer; not applicable to PCIE. Hardwired to 0.
7	RO	Fast back-to-back transactions enable; not applicable to PCIE. Hardwired to 0.
6	R/W	Secondary bus reset
5	RO	Master abort mode; not applicable to PCIE. Hardwired to 0.
4	R/W	VGA 16-bit decode
3	R/W	VGA enable
2	R/W	ISA enable
1	R/W	SERR enable
0	R/W	Parity error response enable

4.9 PCIE Control Registers

Table 4-10 summarizes the PCIE control registers for the AR7242.

Table 4-10. **PCIE Control Registers Summary**

Address	Name	Description	Page
0x180F0000	PCIE_APP	PCIE Application Control	page 80
0x180F0004	PCIE_AER	PCIE Interrupt and Error	page 80
0x180F0008	PCIE_PWR_MGMT	PCIE Power Management	page 81
0x180F000C	PCIE_ELEC	PCIE Electromechanical	page 81
0x180F0010	PCIE_CFG	PCIE Configuration	page 82
0x180F0014	PCIE_RX_CNTL	PCIE Receive Completion	page 82
0x180F0018	PCIE_RESET	PCIE Reset	page 83
0x180F002C	PCIE_PHY_CFG_DATA	PCIE PHY Configuration Data	page 83
0x180F0030	PCIE_MAC_PHY	PCIE MAC-PHY Interface Signals	page 83
0x180F0034	PCIE_PHY_MAC	PCIE PHY-MAC Interface Signals	page 84
0x180F0038	PCIE_SIDEBAND1	PCIE Sideband Bus1	page 84
0x180F003C	PCIE_SIDEBAND2	PCIE Sideband Bus2	page 84
0x180F0040	PCIE_SPARE	PCIE Spare Bits	page 85
0x180F0044	PCIE_MSI_ADDR	PCIE MSI Lower Address	page 85
0x180F0048	PCIE_MSI_DATA	PCIE MSI Data Value	page 85
0x180F004C	PCIE_INT_STATUS	PCIE Interrupt Status	page 86
0x180F0050	PCIE_INT_MASK	PCIE Interrupt Mask	page 87

4.9.1 PCIE Application Control (PCIE_APP)

Address: 0x180F0000
Access: Read/Write
Reset: See field description

This register is used to map error responses and generate unlock messages.

Bit	Bit Name	Reset	Description
31:12	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
11:6	SLV_RESP_ERR_MAP	0x3F	AHB slave response error map**.** This signal allows the application to select a slave response error report mechanism received from a PCIE completion. There are six kinds of PCIE completion errors that the core can report to the AHB interface. The application can choose to not assert the AHB response error as a slave. 6 bits == {completion_tlp_abort, completion_ecrc, completion_ep, completion_crs, completion_ca, completion_ur}, where: 0 SLVERR 1 DECERR
5:4	MSTR_RESP_ERR_MAP	0x0	AHB master response error map. This signal allows the application to select a master response error report mechanism received from an AHB response channel to the CPL status of native PCIE core transmissions. MSB is not currently used. ■ When the LSB is set to 1, it will set an AHB response error to a UR of a PCIE completion. ■ When the LSB is set to 0, it will set an AHB response error to a CA of a PCIE completion: 2 bits == {decerr, slverr} 0 ERR goes to completed aborts 1 ERR goes to unsupported requests
3	INIT_RST	0x0	Application request to initiate a training reset
2	PM_XMT_TURN OFF	0x0	Application signal to generate PM turnoff messages for power management
1	UNLOCK_MSG	0x0	Application signal to generate unlock message. This is to support legacy PCI Lock transactions. If the RC has sent a lock transaction it would need to assert this signal to unlock the path through the PCIE fabric which is locked.
0	LTSSM_ENABLE	0x0	Application signal to enable the LTSSM. If set to zero, it indicates that the application is not ready.

4.9.2 PCIE Interrupt and Error (PCIE_AER)

Address: 0x180F0004
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:5	RES	Reserved
4:0	INT_MSG_NUM	Advanced error interrupt message number Used when MSI or MSI-X is enabled

4.9.3 PCIE Power Management (PCIE_PWR_MGMT)

Address: 0x180F0008
Access: See field description
Reset: 0x0

Bit	Bit Name	Access	Description
31:5	RES	RW	Reserved
4	AUX_PM_EN	RO	AUX power PM enable; enable device to draw auxiliary power independent of PME AUX power
3	READY_ENTR_L23	RW	Indication from the application that it is ready to enter the L2/L3 state
2	REQ_EXIT_L1	RW	Request from the application to exit ASPM state L1, only effective if L1 is enabled
1	REQ_ENTRY_L1	RW	Capability for applications to request PM state to enter L1; only effective if ASPM of L1 is enabled
0	AUX_PWR_DET	RW	Auxiliary power detected; indicates that auxiliary power is present

4.9.4 PCIE Electromechanical (PCIE_ELEC)

Address: 0x180F000C
Access: See field description
Reset: 0x0

Bit	Bit Name	Access	Description	
31:3	RES	RW	Reserved	
2	SYS_ATTEN_BUTTON _PRESSED	RW	Attention button pressed Indicates that the system attention button was pressed, sets the attention button pressed bit in the Slot Status register	
1	CLK_REQ_N	RO	Clock enable Allows the application clock generation module to turn off CORE_CLK based on the current power management state:	
			0	CORE_CLK must be active for the current power state
			1	Current power state allows CORE_CLK to be shut down
0	WAKE_N	RO	Wake up from power management unit. PCIE RC core generates WAKE_L to request the system to restore power and clock when a beacon has been detected. Assertion of WAKE_L could be a clock or multiple clock cycles.	

4.9.5 PCIE Configuration (PCIE_CFG)

Address: 0x180F0010
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved. Must be written with zero. Contains zeros when read.
23:22	ATTEN_IND	The attention indicator control. These bits control the system attention indicator (from bits [7:6] of the Slot Control Register in the PCIE RC).
21:17	PBUS_DEV_NUM	The configured device number. These bits denotes the device number assigned to the device.
25	EML_CONTROL	The electromechanical interlock control. This bit denotes the state of the Electromechanical Interlock Control bit in the Slot Control Register.
24	PWR_CTRLER_ CTRL	The power controller control. This bit controls the system power controller (from bit [10] of the Slot Control Register in the PCIE RC).
16:9	PBUS_NUM	The configured primary bus number. These bits denote the primary bus number assigned to the device.
8	RCB	The read completion boundary (RCB). This bit denotes the value of the RCB bit in the Link Control register in the PCIE RC.
7:5	MAX_PAYLOAD_SIZE	The maximum payload size. This bit denotes the value of the MAX_PAYLOAD_SIZE field in the Device Control register in the PCIE RC.
4:2	MAX_RDREQ_ SIZE	The maximum read request size. This bit denotes the value of the MAX_READ_REQUEST_SIZE field in the Device Control register in the PCIE RC.
1	MEM_SPACE_EN	Memory space enable. This bit denotes the state of the Memory Space Enable bit in the PCI-compatible Command register in the PCIE RC.
0	BUS_MASTER_ EN	Bus master enable. This bit denotes the state of the Bus Master Enable bit in the PCI-compatible Command register in the PCIE RC.

4.9.6 PCIE Receive Completion (PCIE_RX_CNTL)

Address: 0x180F0014
Access: Read-Only
Reset: 0x0

This register is used to denote the field values related to the completion timeout of the PCIE.

Bit	Bit Name	Description
31:29	RES	Reserved. Must be written with zero. Contains zeros when read.
28:21	TIMEOUT_CPL_ TAG	The tag field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted
20:9	TIMEOUT_CPL_ LEN	The length field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted.
8:7	TIMEOUT_CPL _ATTR	The attributes field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted.
6:4	TIMEOUT_CPL_ TC	The traffic class of the timed out completion. This bit is valid when the PCIE core Rx timeout signal is asserted.
3:1	TIMEOUT_FN_ NUM	The function number of the timed out completion. This bit is valid when the PCIE core Rx timeout signal is asserted.
0	CPL_TIMEOUT	The completion timeout. This bit indicates that the completion TLP for a request has not been received within the expected time window.

4.9.7 PCIE Reset (PCIE_RESET)

Address: 0x180F0018
Access: Read/Write
Reset: See field description

This register is used to set the bits for the PCIE reset.

Bit	Bit Name	Reset	Description
31:3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
2	EP_RESET_L	0x1	The reset bit for indicating an endpoint reset through the PCIE PHY
1	LINK_REQ_ RESET	0x0	The reset request due to a Link down status. A high-to-low transition indicates that the RC Core is requesting external logic to reset the RC Core because the PHY link is down.
0	LINK_UP	0x0	Indicates if the PHY link is up or down
			0 Link is down
			1 Link is up

4.9.8 PCIE PHY Configuration Data (PCIE_PHY_CFG_DATA)

Address: 0x180F002C
Access: Read/Write
Reset: See field description

This register holds the PCIE PHY configuration data.

Bit	Bit Name	Reset	Description
31:0	PHY_CFG_DATA	0x5	The PCIE PHY configuration data

4.9.9 PCIE MAC-PHY Interface Signals (PCIE_MAC_PHY)

Address: 0x180F0030
Access: Read-Only
Reset: See field description

This register is used to denote the interface signals for the MAC-PHY interface.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:22	PWRDOWN	The power control. Power control bits to the PHY. The MAC_PHY_POWERDOWN is a 2-bit signal that is shared by all Lanes.
		00 P0 (L0: normal)
		01 P0s (L0s: Low recovery time, power saving)
		10 P1 (L1: longer recovery time, additional power saving)
		11 P2 (L2: lowest power state)
21	RXPOLARITY	Inverted polarity on receive. This bit directs the PHY to perform a polarity inversion on the received data on the specified Lanes.
20	TXCOMPLIANCE	The transmit compliance pattern. This bit sets the running disparity to negative. This is used when the transmitting compliance is patterned.
19	TXELECIDLE	The electrical idle transmit. This bit forces the transmit output to Electrical Idle for each Lane on which is it asserted.
18	TXDETRX_ LOOPBACK	The combined loopback and transmit detection control
17:16	TXDATAK	The control indicator for the transmit data
15:0	TXDATA	The parallel data for transmission. Bits [7:0] correspond to the first symbol of Lane 0. Bits [15:8] correspond to the second symbol of Lane 0. (16-bit PHY interface)

4.9.10 PCIE PHY-MAC Interface Signals (PCIE_PHY_MAC)

Address: 0x180F0034
Access: Read-Only
Reset: 0x0

This register is used to denote the interface signals for the PHY-MAC interface.

Bit	Bit Name	Description	
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.	
23	RXVALID	Receive data invalid. Indicates the symbol lock and valid data for each lane.	
22	PHYSTATUS	The PHY status. This bit communicates completion of the PHY functions including power management transitions and receiver detection	
21:19	RXSTATUS	The receive status and error codes for each lane	
		000	Received data OK
		001	1 SKP added
		010	1 SKP removed
		011	Receiver detected
		100	8b/10b decode error
		101	Elastic buffer overflow
		110	Elastic buffer underflow
		111	Receive disparity error
18	RXELECIDLE	Electrical Idle Receive. This bit indicates the receiver detection of an electrical idle for each lane	
17:16	RXDATAK	The control indicator for the receive data.	
15:0	RXDATA	The parallel receive data. Bits [7:0] correspond to the first symbol of Lane 0. Bits [15:8] correspond to the second symbol of Lane 0. (16-bit PHY interface)	

4.9.11 PCIE Sideband Bus1 (PCIE_SIDEBAND1)

Address: 0x180F0038
Access: Read-Only
Reset: 0x0

This register is used to control additional PHY purposes.

Bit	Bit Name	Description
31:0	CFG_PHY_ CONTROL	The output bus that can be used for additional PHY control purposes. The CFG_PHY_CONTROL bus maps to the PHY Control register.

4.9.12 PCIE Sideband Bus2 (PCIE_SIDEBAND2)

Address: 0x180F003C
Access: Read-Only
Reset: 0x0

This register is used to read the PHY status from the PCIE-PHY.

Bit	Bit Name	Description
31:0	PHY_CFG_ STATUS	Used to read the PHY status from the PCIE-PHY. The PHY_CFG_STATUS bus maps to the PHY Status register.

4.9.13 PCIE Spare Bits (PCIE_SPARE)

Address: 0x180F0040
Access: Read/Write
Reset: 0x0

This register holds the spare bits for the PCIE.

Bit	Bit Name	Description
31:0	BITS	The spare bits for the PCIE

4.9.14 PCIE MSI Lower Address (PCIE_MSI_ADDR)

Address: 0x180F0044
Access: Read/Write
Reset: 0x0

This register holds the lower address for the MSI.

Bit	Bit Name	Description
31:0	LADDR	The lower address register for the MSI

4.9.15 PCIE MSI Data Value (PCIE_MSI_DATA)

Address: 0x180F0048
Access: Read/Write
Reset: 0x0

This register is used to hold the data for the MSI including vector.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	VALUE	These bits hold the data for the MSI including vector [4:0]. The pattern assigned by the system software.

4.9.16 PCIE Interrupt Status (PCIE_INT_STATUS)

Address: 0x180F004C
Access: See field description
Reset: 0x0

This register is used to generate interrupts from PCIE functions or errors.

Bit	Bit Name	Type	Description
31:26	RES	RO	Reserved. Must be written with zero. Contains zeros when read.
25:22	MSI_VEC	RW	Indicates which MSI interrupt has happened
21	CPU_INTD	RO	The status bit to indicate that an INTD assertion has occurred and the client needs to send a deassert interrupt
20	CPU_INTC	RO	The status bit to indicate that an INTC assertion has occurred and the client needs to send a deassert interrupt
19	CPU_INTB	RO	The status bit to indicate that an INTB assertion has occurred and the client needs to send a deassert interrupt
18	CPU_INTA	RO	The status bit to indicate that an INTA assertion has occurred and the client needs to send a deassert interrupt
17	INTDL	RO	The level triggered assertion and deassertion of INTD virtual wire used for PCI 3.0 compatible INTx
16	INTCL	RO	The level triggered assertion and deassertion of INTC virtual wire used for PCI 3.0 compatible INTx
15	INTBL	RO	The level triggered assertion and deassertion of INTB virtual wire used for PCI 3.0 compatible INTx
14	INTAL	RO	The level triggered assertion and deassertion of INTA virtual wire used for PCI 3.0 compatible INTx
13	SYS_ERR	RW	A system error. The RC Core asserts CFG_SYS_ERR_RC if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL.
12	AER_MSI_INT	RW	AER MSI interrupt; set if MSI interrupt is enabled and an AER occurs
11	AER_INT	RW	The AER interrupt
10	MSI_ERR	RW	The interrupt generated by an MSI error
9	MSI	RW	The interrupt caused by the MSI
8	INTD	RW	The edge-triggered INTD virtual wire used for the PCI 3.0 compatible INTx emulation
7	INTC	RW	The edge-triggered INTC virtual wire used for the PCI 3.0 compatible INTx emulation
6	INTB	RW	The edge-triggered INTB virtual wire used for the PCI 3.0 compatible INTx emulation
5	INTA	RW	The edge-triggered INTA virtual wire used for PCI 3.0 compatible INTx emulation
4	RADMX_COMP_ LOOKUP_ERR	RW	The RADMX response composer TAG lookup error. This is a fatal error condition.
3	GM_COMP_ LOOKUP_ERR	RW	GM response composer TAG lookup error. This is a fatal error condition.
2	FATAL_ERR	RW	The received fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_FATAL message
1	NONFATAL_ERR	RW	The received non-fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_NONFATAL message
0	CORR_ERR	RW	The received correctable error message. One clock cycle pulse that indicates that the RC core received an ERR_COR message.

4.9.17 PCIE Interrupt Mask (PCIE_INT_MASK)

Address: 0x180F0050
Access: See field description
Reset: 0x0

This register is used to selectively enable or disable propagation of interrupts.

Bit	Bit Name	Type	Description
31:18	RES	RO	Reserved. Must be written with zero. Contains zeros when read.
17	INTDL	RO	The level triggered assertion and deassertion of INTD virtual wire used for PCI 3.0 compatible INTx
16	INTCL	RO	The level triggered assertion and deassertion of INTC virtual wire used for PCI 3.0 compatible INTx
15	INTBL	RO	The level triggered assertion and deassertion of INTB virtual wire used for PCI 3.0 compatible INTx
14	INTAL	RO	The level triggered assertion and deassertion of INTA virtual wire used for PCI 3.0 compatible INTx
13	SYS_ERR	RW	A system error. The RC Core asserts CFG_SYS_ERR_RC if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL.
12	AER_MSI	RW	AER MSI interrupt
11	AER_INT	RW	The AER interrupt
10	MSI_ERR	RW	The interrupt generated by an MSI error
9	MSI	RW	The interrupt caused by the MSI
8	INTD	RW	The edge-triggered INTD virtual wire used for the PCI 3.0 compatible INTx emulation
7	INTC	RW	The edge-triggered INTC virtual wire used for the PCI 3.0 compatible INTx emulation
6	INTB	RW	The edge-triggered INTB virtual wire used for the PCI 3.0 compatible INTx emulation
5	INTA	RW	The edge-triggered INTA virtual wire used for PCI 3.0 compatible INTx emulation
4	RADMX_COMP_ LOOKUP_ERR	RW	The RADMX response composer TAG lookup error. This is a fatal error condition.
3	GM_COMP_ LOOKUP_ERR	RW	GM response composer TAG lookup error. This is a fatal error condition.
2	FATAL_ERR	RW	The received fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_FATAL message
1	NONFATAL_ERR	RW	The received non-fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_NONFATAL message
0	CORR_ERR	RW	The received correctable error message. One clock cycle pulse that indicates that the RC core received an ERR_COR message.

4.10 Ethernet Registers

Table 4-11 summarizes the Ethernet registers for the AR7242.

Table 4-11. **Ethernet Registers Summary**

GE0 Address	GE1 Address	Description		Page
0x19000000	0x1A000000	MAC Configuration 1		page 91
0x19000004	0x1A000004	MAC Configuration 2		page 92
0x19000008	0x1A000008	IPG/IFG		page 93
0x1900000C	0x1A00000C	Half-Duplex		page 94
0x19000010	0x1A000010	Maximum Frame Length		page 94
0x19000020	0x1A100020	MII Configuration		page 95
0x19000024	0x1A000024	MII Command		page 95
0x19000028	0x1A000028	MII Address		page 96
0x1900002C	0x1A00002C	MII Control		page 96
0x19000030	0x1A000030	MII Status		page 96
0x19000034	0x1A000034	MII Indicators		page 96
0x19000038	0x1A000038	Interface Control		page 97
0x1900003C	0x1A00003C	Interface Status		page 98
0x19000040	0x1A000040	STA Address 1		page 99
0x19000044	0x1A000044	STA Address 2		page 99
0x19000048	0x1A000048	ETH Configuration 0		page 100
0x1900004C	0x1A00004C	ETH Configuration 1		page 101
0x19000050	0x1A000050	ETH Configuration 2		page 101
0x19000054	0x1A000054	ETH Configuration 3		page 102
0x19000058	0x1A000058	ETH Configuration 4		page 103
0x1900005C	0x1A00005C	ETH Configuration 5		page 103
0x19000080	0x1A000080	TR64	Tx/Rx 64 Byte Frame Counter	page 104
0x19000084	0x1A000084	TR127	Tx/Rx 65-127 Byte Frame Counter	page 104
0x19000088	0x1A000088	TR255	Tx/Rx 128-255 Byte Frame Counter	page 104
0x1900008C	0x1A00008C	TR511	Tx/Rx 256-511 Byte Frame Counter	page 104
0x19000090	0x1A000090	TR1K	Tx/Rx 512-1023 Byte Frame Counter	page 105
0x19000094	0x1A000094	TRMAX	Tx/Rx 1024-1518 Byte Frame Counter	page 105
0x19000098	0x1A000098	TRMGV	Tx/Rx 1519-1522 Byte VLAN Frame Counter	page 105
0x1900009C	0x1A00009C	RBYT	Receive Byte Counter	page 105
0x190000A0	0x1A0000A0	RPKT	Receive Packet Counter	page 106
0x190000A4	0x1A0000A4	RFCS	Receive FCS Error Counter	page 106
0x190000A8	0x1A0000A8	RMCA	Receive Multicast Packet Counter	page 106
0x190000AC	0x1A0000AC	RBCA	Receive Broadcast Packet Counter	page 106

Table 4-11. **Ethernet Registers Summary (continued)**

GE0 Address	GE1 Address	Description		Page
0x190000B0	0x1A0000B0	RXCF	Receive Control Frame Packet Counter	page 107
0x190000B4	0x1A0000B4	RXPF	Receive Pause Frame Packet Counter	page 107
0x190000B8	0x1A0000B8	RXUO	Receive Unknown OPCode Packet Counter	page 107
0x190000BC	0x1A0000BC	RALN	Receive Alignment Error Counter	page 107
0x190000C0	0x1A0000C0	RFLR	Receive Frame Length Error Counter	page 108
0x190000C4	0x1A0000C4	RCDE	Receive Code Error Counter	page 108
0x190000C8	0x1A0000C8	RCSE	Receive Carrier Sense Error Counter	page 108
0x190000CC	0x1A0000CC	RUND	Receive Undersize Packet Counter	page 108
0x190000D0	0x1A0000D0	ROVR	Receive Oversize Packet Counter	page 109
0x190000D4	0x1A0000D4	RFRG	Receive Fragments Counter	page 109
0x190000D8	0x1A0000D8	RJBR	Receive Jabber Counter	page 109
0x190000DC	0x1A0000DC	RDRP	Receive Dropped Packet Counter	page 109
0x190000E0	0x1A0000E0	TBYT	Transmit Byte Counter	page 110
0x190000E4	0x1A0000E4	TPKT	Transmit Packet Counter	page 110
0x190000E8	0x1A0000E8	TMCA	Transmit Multicast Packet Counter	page 110
0x190000EC	0x1A0000EC	TBCA	Transmit Broadcast Packet Counter	page 110
0x190000F0	0x1A0000F0	TXPF	Transmit Pause Control Frame Counter	page 111
0x190000F4	0x1A0000F4	TDFR	Transmit Deferral Packet Counter	page 111
0x190000F8	0x1A0000F8	TEDF	Transmit Excessive Deferral Packet Counter	page 111
0x190000FC	0x1A0000FC	TSCL	Transmit Single Collision Packet Counter	page 111
0x19000100	0x1A000100	TMCL	Transmit Multiple Collision Packet	page 112
0x19000104	0x1A000104	TLCL	Transmit Late Collision Packet Counter	page 112
0x19000108	0x1A000108	TXCL	Transmit Excessive Collision Packet Counter	page 112
0x1900010C	0x1A00010C	TNCL	Transmit Total Collision Counter	page 112
0x19000110	0x1A000110	TPFH	Transmit Pause Frames Honored Counter	page 113
0x19000114	0x1A000114	TDRP	Transmit Drop Frame Counter	page 113
0x19000118	0x1A000118	TJBR	Transmit Jabber Frame Counter	page 113
0x1900011C	0x1A00011C	TFCS	Transmit FCS Error Counter	page 113
0x19000120	0x1A000120	TXCF	Transmit Control Frame Counter	page 114
0x19000124	0x1A000124	TOVR	Transmit Oversize Frame Counter	page 115
0x19000128	0x1A000128	TUND	Transmit Undersize Frame Counter	page 115
0x1900012C	0x1A00012C	TFRG	Transmit Fragment Counter	page 115

Table 4-11. **Ethernet Registers Summary (continued)**

GE0 Address	GE1 Address	Description		Page
0x19000130	0x1A000130	CAR1	Carry Register 1	page 116
0x19000134	0x1A000134	CAR2	Carry Register 2	page 117
0x19000138	0x1A000138	CAM1	Carry Mask Register 1	page 118
0x1900013C	0x1A00013C	CAM2	Carry Mask Register 2	page 119
0x19000180	0x1A000180	DMATXCNTRL_Q0	DMA Transfer Control for Queue 0	page 119
0x19000184	0x1A000184	DMATXDESCR_Q0	Descriptor Address for Queue 0 Tx	page 120
0x19000188	0x1A000188	DMA Tx Status		page 120
0x1900018C	0x1A00018C	DMARXCTRL	Rx Control	page 120
0x19000190	0x1A000190	DMARXDESCR	Pointer to Rx Descriptor	page 121
0x19000194	0x1A000194	DMARXSTATUS	Rx Status	page 121
0x19000198	0x1A000198	DMAINTRMASK	Interrupt Mask	page 122
0x1900019C	0x1A00019C	Interrupts		page 123
0x190001A0	0x1A0001A0	ETH_TX_BURST	Ethernet Tx burst	page 124
0x190001A4	0x1A0001A4	ETH_TXFIFO_TH	Ethernet Tx FIFO Max and Min Threshold	page 124
0x190001A8	0x1A0001A8	ETH_XFIFO_DEPTH	Current Tx and Rx FIFO Depth	page 124
0x190001AC	0x1A0001AC	ETH_RXFIFO_TH	Ethernet Rx FIFO	page 124
0x190001B8	0x1A0001B8	ETH_FREE_TIMER	Ethernet Free Timer	page 125
0x190001C0	0x1A0001C0	DMATXCNTRL_Q1	DMA Transfer Control for Queue 1	page 125
0x190001C4	0x1A0001C4	DMATXDESCR_Q1	Descriptor Address for Queue 1 Tx	page 125
0x190001C8	0x1A0001C8	DMATXCNTRL_Q2	DMA Transfer Control for Queue 2	page 126
0x190001CC	0x1A0001CC	DMATXDESCR_Q2	Descriptor Address for Queue 2 Tx	page 126
0x190001D0	0x1A0001D0	DMATXCNTRL_Q3	DMA Transfer Control for Queue 3	page 126
0x190001D4	0x1A0001D4	DMATXDESCR_Q3	Descriptor Address for Queue 3 Tx	page 126
0x190001D8	0x1A0001D8	DMATXARBCFG	DMA Tx Arbitration Configuration	page 126

4.10.1 MAC Configuration 1

GE0 Address: 0x19000000
GE1 Address: 0x1A000000
Access: See field description
Reset: See field description

This register is used to set the actions for transmitting and receiving frames.

Bit	Bit Name	Type	Reset	Description
31	SOFT_RESET	RW	0x1	Setting this bit resets all modules except the host interface. The host interface is reset via HRST.
30	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
29:20	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
19	RESET_RX_MAC_ CONTROL	RW	0x0	Resets the receive (Rx) MAC control block
18	RESET_TX_MAC_ CONTROL	RW	0x0	Resets the transmit (Tx) MAC control
17	RESET_RX_ FUNCTION	RW	0x0	Resets the Rx function
16	RESET_TX_ FUNCTION	RW	0x0	Resets the Tx function
15:9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
8	LOOP_BACK	RW	0x0	Setting this bit causes MAC Rx outputs to loop back to the MAC Rx inputs. Clearing this bit results in normal operation.
7:6	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
5	RX_FLOW _CONTROL	RW	0x0	Setting this bit causes the Rx MAC control to detect and act on pause flow control frames.
4	TX_FLOW_ CONTROL	RW	0x0	Setting this bit causes the Tx MAC control to send requested flow control frames. Clearing this bit prevents the MAC from sending flow control frames. The default is 0.
3	SYNCHRONIZED_RX	RO	0x0	Rx enable synchronized to the receive stream
2	RX_ENABLE	RW	0x0	Setting this bit will allow the MAC to receive frames from the PHY. Clearing this bit will prevent the reception of frames.
1	SYNCHRONIZED_TX	RO	0x0	Tx enable synchronized to the Tx stream
0	TX_ENABLE	RW	0x0	Allows the MAC to transmit frames from the system. Clearing this bit will prevent the transmission of frames.

4.10.2 MAC Configuration 2

GE0 Address: 0x19000004
GE1 Address: 0x1A000004
Access: Read/Write
Reset: See field description

This register is used to set the parameters relating to the MAC, including duplex, CRC, and oversized frames.

Bit	Bit Name	Reset	Description
31:16	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:12	PREAMBLE_ LENGTH	0x7	Determines the length of the preamble field of the packet, in bytes.
11:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:8	INTERFACE_ MODE	0x0	Determines the type of interface to which the MAC is connected.

Interface Mode	Bit [9]	Bit [8]
RESERVED	0	0
Nibble Mode (10/100 Mbps MII/RMII/SMII...)	0	1
RESERVED	1	0
RESERVED	1	1

7:6	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
5	HUGE_FRAME	0x0	Set this bit to allow frames longer than the MAXIMUM FRAME LENGTH to be transmitted and received. Clear this bit to have the MAC limit the length of frames at the MAXIMUM FRAME LENGTH value, which is contained in the "Maximum Frame Length" register.
4	LENGTH_FIELD	0x0	Set this bit to cause the MAC to check the frame's length field to ensure it matches the actual data field length. Clear this bit if no length field checking is desired.
3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
2	PAD/CRC ENABLE	0x0	Set this bit to have the MAC pad all short frames and append a CRC to every frame whether or not padding was required. Clear this bit if frames presented to the MAC have a valid length and contain a CRC.
1	CRC_ENABLE	0x0	Set this bit to have the MAC append a CRC to all frames. Clear this bit if frames presented to the MAC have a valid length and contain a valid CRC.
0	FULL_DUPLEX	0x0	Setting this bit configures the MAC to operate in full-duplex mode. Clearing this bit configures the MAC to operate in half-duplex mode only.

4.10.3 IPG/IFG

GE0 Address: 0x19000008
GE1 Address: 0x1A000008
Access: Read/Write
Reset: See field description

This register is used to configure settings for the inter-packet gap and the inter-frame gap.

Bit	Bit Name	Reset	Description
31	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
30:24	NON BACK-TO-BACK INTER-PACKET GAP 1	0x40	This programmable field represents the carrier sense window. If a carrier is detected, the MAC will defer to the carrier. If, however, the carrier becomes active, the MAC will continue timing and transmission, knowingly causing a collision and ensuring fair access to the medium.
23	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
22:16	NON BACK-TO-BACK INTER-PACKET GAP 2	0x60	This programmable field represents the non-back-to-back inter-packet gap in bit times
15:8	MINIMUM_IFG_ ENFORCEMENT	0x50	This programmable field represents the minimum IFG size to enforce between frames (expressed in bit times). Frames whose IFG is less than that programmed, are dropped.
7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:0	BACK-TO-BACK INTER-PACKET_GAP	0x60	This programmable field represents the IPG between back-to-back packets (expressed in bit times). This IPG parameter is used in full-duplex mode when two Tx packets are sent back-to-back. Set this field to the desired number of bits.

4.10.4 Half-Duplex

GE0 Address: 0x1900000C
GE1 Address: 0x1A00000C
Access: Read/Write
Reset: See field description

This register is used to configure the settings for half-duplex, including backpressure, excessive defer and collisions.

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
23:20	ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION	0xA	Used when bit [19] is set. The value programmed is substituted for the Ethernet standard value of ten.
19	ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE	0x0	Setting this bit will configure the Tx MAC to use the setting of bits [23:20] instead of the tenth collision. Clearing this bit will cause the TX MAC to follow the standard binary exponential backoff rule, which specifies that any collision after the tenth uses 210-1 as the maximum backoff time.
18	BACKPRESSURE_NO_BACKOFF	0x0	Setting this bit will configure the Tx MAC to immediately retransmit following a collision during backpressure operation. Clearing this bit will cause the Tx MAC to follow the binary exponential backoff rule.
17	NO_BACKOFF	0x0	Setting this bit will configure the Tx MAC to immediately retransmit following a collision. Clearing this bit will cause the Tx MAC to follow the binary exponential backoff rule.
16	EXCESSIVE_ DEFER	0x1	Setting this bit will configure the Tx MAC to allow the transmission of a packet that has been excessively deferred. Clearing this bit will cause the Tx MAC to abort the transmission of a packet that has been excessively deferred.
15:12	RETRANSMISSION _MAXIMUM	0xF	This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The maximum number of attempts is defined by 802.11 standards as 0xF.
11:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:0	COLLISION_ WINDOW	0x37	This programmable field represents the slot time or collision window during which collisions might occur in a properly configured network. Since the collision window starts at the beginning of a transmission, the preamble and SFD are included. The reset value (0x37) corresponds to the count of frame bytes at the end of the window. If the value is larger than 0x3F the TPST single will no longer work correctly.

4.10.5 Maximum Frame Length

GE0 Address: 0x19000010
GE1 Address: 0x1A000010
Access: Read/Write
Reset: 0x600

This register is used to set the maximum allowable frame length.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	MAX_FRAME _LENGTH	This programmable field sets the maximum frame size in both the Tx and Rx directions

4.10.6 MII Configuration

GE0 Address: 0x19000020
GE1 Address: 0x1A000020
Access: Read/Write
Reset: 0x0

This register is used to set the MII management parameters.

Bit	Bit Name	Description
31	RESET_MII_ MGMT	Setting this bit resets the MII Management. Clearing this bit allows MII Management to perform management read/write cycles as requested by the Host interface.
30:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	SCAN_AUTO_ INCREMENT	Setting this bit causes MII Management to continually read from a set of contiguous PHYs. The starting address of the PHY is specified by the PHY address field recorded in the MII Address register. The next PHY to be read will be PHY address + 1. The last PHY to be queried in this read sequence will be the one residing at address 0x31, after which the read sequence will return to the PHY specified by the PHY address field.
4	PREAMBLE_ SUPRESSION	Setting this bit causes MII Management to suppress preamble generation and reduce the management cycle from 64 clocks to 32 clocks. Clearing this bit causes MII Management to perform Management read/write cycles with the 64 clocks of preamble.
3:0	MGMT_CLOCK_ SELECT	This field determines the clock frequency of the management clock (MDC).

Management Clock Select	3	2	1	0
Source clock divided by 4	0	0	0	0
Source clock divided by 4	0	0	0	1
Source clock divided by 6	0	0	1	0
Source clock divided by 8	0	0	1	1
Source clock divided by 10	0	1	0	0
Source clock divided by 14	0	1	0	1
Source clock divided by 20	0	1	1	0
Source clock divided by 28	0	1	1	1
Source clock divided by 34	1	0	0	0
Source clock divided by 42	1	0	0	1
Source clock divided by 50	1	0	1	0
Source clock divided by 58	1	0	1	1
Source clock divided by 66	1	1	0	0
Source clock divided by 74	1	1	0	1
Source clock divided by 82	1	1	1	0
Source clock divided by 98	1	1	1	1

4.10.7 MII Command

GE0 Address: 0x19000024
GE1 Address: 0x1A000024
Access: Read/Write
Reset: 0x0

This register is used to cause MII management to perform read cycles.

Bit	Bit Name	Description
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	SCAN_CYCLE	Causes MII management to perform read cycles continuously (e.g. to monitor link fail).
0	READ_CYCLE	Causes MII management to perform a single read cycle.

4.10.8 MII Address

GE0 Address: 0x19000028
GE1 Address: 0x1A000028
Access: Read/Write
Reset: 0x0

All MAC/PHY registers are accessed via the MII address and MII control registers of GE0 only. GE1 MII address and control registers are not used. The details of the Ethernet MAC/PHY that are accessible through the MAC 0 MII address.

Bit	Bit Name	Description
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.
12:8	PHY_ADDRESS	Represents the five-bit PHY address field used in management cycles. Up to 31 PHYs can be addressed (0 is reserved).
7:5	RES	Reserved. Must be written with zero. Contains zeros when read.
4:0	REGISTER ADDRESS	Represents the five-bit register address field used in management cycles. Up to 32 registers can be accessed.

4.10.9 MII Control

GE0 Address: 0x1900002C
GE1 Address: 0x1A00002C
Access: Write-Only
Reset: 0x0

All MAC/PHY registers are accessed via the MII Address and MII Control registers.

This register is used to perform write cycles using the information in the MII Address register.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	MII_MGMT_ CONTROL	When written, an MII management write cycle is performed using the 16-bit data and the pre-configured PHY and register addresses from ""MII Address"" (0x0A).

4.10.10 MII Status

GE0 Address: 0x19000030
GE1 Address: 0x1A000030
Access: Read-Only
Reset: 0x0

This register is used to read information following an MII management read cycle.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	MII_MGMT_ STATUS	After an MII management read cycle, 16-bit data can be read from this register.

4.10.11 MII Indicators

GE0 Address: 0x19000034
GE1 Address: 0x1A000034
Access: Read-Only
Reset: 0x0

This register is used indicate various functions of the MII management are currently being performed.

Bit	Bit Name	Description
31:3	RES	Reserved. Must be written with zero. Contains zeros when read.
2	NOT_VALID	When a 1 is returned, this bit indicates that the MII management read cycle has not yet completed and that the read data is not yet valid
1	SCANNING	When a 1 is returned, this bit indicates that a scan operation (continuous MII management read cycles) is in progress
0	BUSY	When a 1 is returned, this bit indicates that the MII management block is currently performing an MII management read or write cycle

4.10.12 Interface Control

MAC 0 Address: 0x19000038
MAC 1 Address: 0x1A000038
Access: Read/Write
Reset: 0x0

This register is used to configure and set the interface modules.

Bit	Bit Name	Description	
31	RESET_ INTERFACE_ MODULE	Setting this bit resets the interface module. Clearing this bit allows for normal operation. This bit can be used in place of bits [23], [15] and [7] when any interface module is connected.	
30:28	RES	Reserved. Must be written with zero. Contains zeros when read.	
27	TBIMODE	Setting this bit configures the A-RGMII module to expect TBI signals at the GMII interface. This bit should not be asserted unless this mode is being used.	
26	GHDMODE	Setting this bit configures the A-RGMII to expect half-duplex at the GMII interface. It also enables the use of CRS and COL signals.	
25	LHDMODE	Setting this bit configures the A-RGMII module to expect 10 or 100 Mbps half-duplex MII at the GMII interface and will enable the use of CRS and COL signals. This bit should not be asserted unless this mode is being used.	
24	PHY_MODE	Setting this bit configures the serial MII module to be in PHY Mode. Link characteristics are taken directly from the RX segments supplied by the PHY.	
23	RESET_PERMII	Setting this bit resets the PERMII module. Clearing this bit allows for normal operation.	
22:17	RES	Reserved. Must be written with zero. Contains zeros when read.	
16	SPEED	This bit configures the reduced MII module with the current operating speed.	
		0	Selects 10 Mbps mode
		1	Selects 100 Mbps mode
15	RESET_PE100X	This bit resets the PE100X module, which contains the 4B/5B symbol encipher/ decipher code.	
14:11	RES	Reserved. Must be written with zero. Contains zeros when read.	
10	FORCE_QUIET	Affects PE100X module only.	
		0	Normal operation
		1	Tx data is quiet, allowing the contents of the cipher to be output
9	NO_CIPHER	Affects PE100X module only.	
		0	Normal ciphering occurs
		1	The raw transmit 5B symbols are transmitting without ciphering
8	DISABLE_LINK_ FAIL	Affects PE100X module only.	
		0	Normal Operation
		1	Disables the 330-ms link fail timer, allowing shorter simulations. Removes the 330-ms link-up time before stream reception is allowed.
7	RESET GPSI	This bit resets the PE10T module which converts MII nibble streams to the serial bit stream of ENDEC PHYs. Affects PE10T module only.	
6:1	RES	Reserved. Must be written with zero. Contains zeros when read.	
0	ENABLE_ JABBER_ PROTECTION	This bit enables the Jabber Protection logic within the PE10T in ENDEC mode. Jabber is the condition where a transmitter is on for longer than 50 ms preventing other stations from transmitting. Affects PE10T module only.	

4.10.13 Interface Status

GE0 Address: 0x1900003C
GE1 Address: 0x1A00003C
Access: Read-Only
Reset: 0x0

Identifies the interface statuses. The range of bits that are active are dependant upon the optional interfaces connected at the time.

Bit	Bit Name	Description	
31:10	RES	Reserved. Must be written with zero. Contains zeros when read.	
9	EXCESS_DEFER	This bit sets when the MAC excessively defers a transmission. It clears when read. This bit latches high.	
8	CLASH	Used to identify the serial MII module mode	
		0	In PHY mode or in a properly configured MAC to MAC mode
		1	MAC to MAC mode with the partner in 10 Mbps and/or half-duplex mode indicative of a configuration error
7	JABBER	Used to identify a jabber condition as detected by the serial MII PHY	
		0	No jabber condition detected
		1	Jabber condition detected
6	LINK_OK	Used to identify the validity of a serial MII PHY link	
		0	No valid link detected
		1	Valid link detected
5	FULL_DUPLEX	Used to identify the current duplex of the serial MII PHY	
		0	Half-duplex
		1	Full-duplex
4	SPEED	Used to identify the current running speed of the serial MII PHY	
		0	10 Mbps
		1	100 Mbps
3	LINK_FAIL	Used to read the PHY link fail register. For asynchronous host accesses, this bit must be read at least once every scan read cycle of the PHY.	
		0	The MII management module has read the PHY link fail register to be 0
		1	The MII management module has read the PHY link fail register to be 1
2	CARRIER_LOSS	Carrier status. This bit latches high.	
		0	No carrier loss detection
		1	Loss of carrier detection
1	SQE_ERROR	0	Has not detected an SQE error. Latches high.
		1	Has detected an SQE error.
0	JABBER	0	Has not detected a Jabber condition. Latches high.
		1	Has detected a Jabber condition

4.10.14 STA Address 1

GE0 Address: 0x19000040
GE1 Address: 0x1A000040
Access: Read/Write
Reset: 0x0

This register holds the first four octets of the station address.

Bit	Bit Name	Description
31:24	STATION_ ADDRESS_1	This field holds the first octet of the station address
23:16	STATION_ ADDRESS_2	This field holds the second octet of the station address
15:8	STATION_ ADDRESS_3	This field holds the third octet of the station address
7:0	STATION_ ADDRESS_4	This field holds the fourth octet of the station address

4.10.15 STA Address 2

GE0 Address: 0x19000044
GE1 Address: 0x1A000044
Access: Read/Write
Reset: 0x0

This register holds the last two octets of the station address.

Bit	Bit Name	Description
31:24	STATION_ ADDRESS_5	This field holds the fifth octet of the station address
23:16	STATION_ ADDRESS_6	This field holds the sixth octet of the station address
15:0	RES	Reserved

4.10.16 ETH_FIFO RAM Configuration 0

GE0 Address: 0x19000048
GE1 Address: 0x1A000048
Access: See field description
Reset: 0x0

This register is used to assert and negate functions concerning the ETH module.

Bit	Bit Name	Access	Description	
31:21	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
20	FTFENRPLY	RO	Asserted	The eth_fab module is enabled
			Negated	The eth_fab module is disabled
19	STFENRPLY	RO	Asserted	The eth_sys module is enabled
			Negated	The eth_sys module is disabled
18	FRFENRPLY	RO	Asserted	The eth_fab module is enabled
			Negated	The eth_fab module is disabled
17	SRFENRPLY	RO	Asserted	The eth_sys module is enabled
			Negated	The eth_sys module is disabled
16	WTMENRPLY	RO	Asserted	The eth_wtm module is enabled
			Negated	The eth_wtm module is disabled
15:13	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
12	FTFENREQ	RW	Asserted	Requests enabling of the eth_fab module
			Negated	Requests disabling of the eth_fab module
11	STFENREQ	RW	Asserted	Requests enabling of the eth_sys module
			Negated	Requests disabling of the eth_sys module
10	FRFENREQ	RW	Asserted	Requests enabling of the eth_fab module
			Negated	Requests disabling of the eth_fab module
9	SRFENREQ	RW	Asserted	Requests enabling of the eth_sys module
			Negated	Requests disabling of the eth_sys module
8	WTMENREQ	RW	Asserted	Requests enabling of the eth_wtm module
			Negated	Requests disabling of the eth_wtm module
7:5	RES	RW	Reserved. Must be written with zero. Contains zeros when read.	
4	HSTRSTFT	RW	When asserted, this bit places the eth_fab module in reset	
3	HSTRSTST	RW	When asserted, this bit places the eth_sys module in reset	
2	HSTRSTFR	RW	When asserted, this bit places the eth_fab module in reset	
1	HSTRSTSR	RW	When asserted, this bit places the eth_sys module in reset	
0	HSTRSTWT	RW	When asserted, this bit places the eth_wtm module in reset	

4.10.17 ETH Configuration 1

GE0 Address: 0x1900004C
GE1 Address: 0x1A00004C
Access: Read/Write
Reset: See field description

This register is used to configure the ETH storage area.

Bit	Bit Name	Reset	Description
31:28	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
27:16	CFGFRTH [11:0]	0xFFFF	This hex value represents the minimum number of 4-byte locations to store simultaneously in the receive RAM, relative to the beginning of the frame being input, before FRRDY may be asserted. Note that FRRDY will be latent a certain amount of time due to fabric transmit clock to system transmit clock time domain crossing, and conditional on FRACPT assertion. When set to the maximum value, FRRD may be asserted only after the completion of the input frame. The value of this register must be greater than 18D when HSTDRPLT64 is asserted.
15:0	CFGXOFFRTX	0xFFFF	This hexadecimal value represents the number of pause quanta (64-bit times) after an XOFF pause frame has been acknowledged until the ETH reasserts TCRQ if the ETH receive storage level has remained higher than the low watermark.

4.10.18 ETH Configuration 2

MAC 0 Address: 0x19000050
MAC 1 Address: 0x1A000050
Access: Read/Write
Reset: See field description

This register is used to number the minimum amount of 8-byte words in the Rx RAM before pause frames are transmitted.

Bit	Bit Name	Reset	Description
31:29	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
28:16	CFGHWM [12:0]	0xAAA	This hex value represents the maximum number of 8-byte words to store simultaneously in the Rx RAM before TCRQ and PSVAL facilitates an XOFF pause control frame.
15:13	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
12:0	CFGLWM [12:0]	0x555	This hex value represents the minimum number of 8-byte words to store simultaneously in the Rx RAM before TCRQ and PSVAL facilitate an XON pause control frame in response to a previously transmitted XOFF pause control frame.

4.10.19 ETH Configuration 3

GE0 Address: 0x19000054
GE1 Address: 0x1A000054
Access: Read/Write
Reset: See field description

This register is used denote the minimum number of 4-byte locations to simultaneously store in the Tx RAM before assertion.

Bit	Bit Name	Type	Reset	Description
31:28	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
27:16	CFGHWMFT [11:0]	RW	0x555	This hex value represents the maximum number of 4-byte locations to store simultaneously in the Tx RAM before FTHWM is asserted. Note that FTHWM has two FTCLK clock periods of latency before assertion or negation, as should be considered when calculating headroom required for maximum size packets.
15:12	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
11:0	CFGFTTTH [11:0]	RW	0xFFF	This hex value represents the minimum number of 4-byte locations to store simultaneously in the Tx RAM, relative to the beginning of the frame being input, before TPSF is asserted. Note that TPSF is latent for a certain amount of time due to fabric Tx clock system Tx clock time domain crossing. When set to the maximum value, TPSF asserts only after the completion of the input frame.

4.10.20 ETH Configuration 4

GE0 Address: 0x19000058
GE1 Address: 0x1A000058
Access: Read/Write
Reset: 0x0

This register is used to signal drop frame conditions internal to the Ethernet.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17	Unicast MAC address match	In combination with "ETH Configuration 5", bits [17:0] of this register control which frames are dropped and which are sent to the DMA engine. If the bit is set in "ETH Configuration 5" and it does not match the value in this bit, then the frame is dropped.
16	Truncated frame	
15	VLAN tag	
14	Unsupported op-code	
13	Pause frame	
12	Control frame	
11	Long event	
10	Dribble nibble	
9	Broadcast	
8	Multicast	
7	OK	
6	Out of range	
5	Length mismatch	
4	CRC error	
3	Code error	
2	False carrier	
1	RX_DV event	
0	Drop event	

4.10.21 ETH Configuration 5

GE0 Address: 0x1900005C
GE1 Address: 0x1A00005C
Access: Read/Write
Reset: See field description

This register is used to assert or negate bits of the ETH component.

Bit	Bit Name	Reset	Description
31:20	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
19	Byte/Nibble	0x0	This bit should be set to 1 for GE0 or set to 0 for GE1.
18	Short Frame	0x0	If set to 1, all frames under 64 bytes are dropped.
17:0	Rx Filter[17:0]	0x3FFFF	If set in this vector, the corresponding field must match exactly in "ETH Configuration 4" for the packet to pass on to the DMA engine.

4.10.22 Tx/Rx 64 Byte Frame Counter (TR64)

GE0 Address: 0x19000080
GE1 Address: 0x1A000080
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were up to 64 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR64	The transmit and receive 64 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which is 64 bytes in length inclusive (excluding framing bits but including FCS bytes).

4.10.23 Tx/Rx 65-127 Byte Frame Counter (TR127)

GE0 Address: 0x19000084
GE1 Address: 0x1A000084
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 65–127 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR127	The transmit and receive 65–127 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 65-127 bytes in length inclusive (excluding framing bits but including FCS bytes).

4.10.24 Tx/Rx 128-255 Byte Frame Counter (TR255)

GE0 Address: 0x19000088
GE1 Address: 0x1A000088
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 128–255 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR255	The transmit and receive 128-255 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 128-255 bytes in length inclusive (excluding framing bits but including FCS bytes).

4.10.25 Tx/Rx 256-511 Byte Frame Counter (TR511)

GE0 Address: 0x1900008C
GE1 Address: 0x1A00008C
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 256–511 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR511	The transmit and receive 256–511 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 256–511 bytes in length inclusive (excluding framing bits but including FCS bytes).

4.10.26 Tx/Rx 512-1023 Byte Frame Counter (TR1K)

GE0 Address: 0x19000090
GE1 Address: 0x1A000090
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 512–1023 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR1K	The transmit and receive 512–1023 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 512–1023 bytes in length inclusive (excluding framing bits but including FCS bytes).

4.10.27 Tx/Rx 1024-1518 Byte Frame Counter (TRMAX)

GE0 Address: 0x19000094
GE1 Address: 0x1A000094
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 1024–1518 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TRMAX	The transmit and receive 1024-1518 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 1024-1518 bytes in length inclusive (excluding framing bits but including FCS bytes).

4.10.28 Tx/Rx 1519-1522 Byte VLAN Frame Counter (TRMGV)

GE0 Address: 0x19000098
GE1 Address: 0x1A000098
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 1519–1522 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TRMGV	The transmit and receive 1519–1522 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 1519–1522 bytes in length inclusive (excluding framing bits but including FCS bytes).

4.10.29 Receive Byte Counter (RYBT)

GE0 Address: 0x1900009C
GE1 Address: 0x1A00009C
Access: Read/Write
Reset: 0x0

This register is used to count incoming frames and then increment this register accordingly.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:0	RBYT	The receive byte counter. This statistic count register is incremented by the byte count of all frames received, including bad packets but excluding framing bits but including FCS bytes.

4.10.30 Receive Packet Counter (RPKT)

GE0 Address: 0x190000A0
GE1 Address: 0x1A0000A0

Access: Read/Write
Reset: 0x0

This register is used to count packets received.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	RPKT	The receive packet counter. This register is incremented for each received packet (including bad packets, all Unicast, broadcast and Multicast packets).

4.10.31 Receive FCS Error Counter (RFCS)

GE0 Address: 0x190000A4
GE1 Address: 0x1A0000A4
Access: Read/Write
Reset: 0x0

This register is used to count frames received between 64–1518 in length and has a FCS error.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RFCS	The received FCS error counter. This register is incremented for each frame received that has an integral 64–1518 length and contains a frame check sequence error.

4.10.32 Receive Multicast Packet Counter (RMCA)

GE0 Address: 0x190000A8
GE1 Address: 0x1A0000A8
Access: Read/Write
Reset: 0x0

This register is used to count received good standard multicast packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	RMCA	The receive multicast packet counter. This register is incremented for each multicast good frame of lengths smaller than 1518 (non-VLAN) or 1522 (VLAN) excluding broadcast frames. This does not include range/length errors.

4.10.33 Receive Broadcast Packet Counter (RBCA)

GE0 Address: 0x190000AC
GE1 Address: 0x1A0000AC
Access: Read/Write
Reset: 0x0

This register is used to count received good broadcast frames.

Bit	Bit Name	Description
31:22	RES	Reserved. Must be written with zero. Contains zeros when read.
21:0	RBCA	The receive broadcast packet counter. This register is incremented for each broadcast good frame of lengths smaller than 1518 (non-VLAN) or 1522 (VLAN) excluding multicast frames. This does not include range or length errors.

4.10.34 Receive Control Frame Packet Counter (RXCF)

GE0 Address: 0x190000B0
GE1 Address: 0x1A0000B0
Access: Read/Write
Reset: 0x0

This register is used to count received MAC control frames.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	RXCF	The receive control frame packet counter. This register is incremented for each MAC control frame received (pause and unsupported).

4.10.35 Receive Pause Frame Packet Counter (RXPF)

GE0 Address: 0x190000B4
GE1 Address: 0x1A0000B4
Access: Read/Write
Reset: 0x0

This register is used to count received pause frame packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RXPF	The receive pause frame packet counter. This register is incremented each time a valid pause MAC control frame is received.

4.10.36 Receive Unknown OPCode Packet Counter (RXUO)

GE0 Address: 0x190000B8
GE1 Address: 0x1A0000B8
Access: Read/Write
Reset: 0x0

This register is used to count received MAC control frames that contain an opcode.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RXUO	The receive unknown OPcode counter. This bit is incremented each time a MAC control frame is received which contains an opcode other than a pause.

4.10.37 Receive Alignment Error Counter (RALN)

GE0 Address: 0x190000BC
GE1 Address: 0x1A0000BC
Access: Read/Write
Reset: 0x0

This register is used to count received packets with an alignment error.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RALN	The receive alignment error counter. This register is incremented for each received frame from 64–1518 bytes that contains an invalid FCS and is not an integral number of bytes.

4.10.38 Receive Frame Length Error Counter (RFLR)

GE0 Address: 0x190000C0
GE1 Address: 0x1A0000C0
Access: Read/Write
Reset: 0x0

This register is used to count received frames that have a length error.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	RFLR	The received frame length error counter. this register is incremented for each received frame in which the 802.3 length field did not match the number of data bytes actually received (46–1500 bytes). The counter is not incremented if the length field is not a valid 802.3 length, such as an EtherType value.

4.10.39 Receive Code Error Counter (RCDE)

GE0 Address: 0x190000C4
GE1 Address: 0x1A0000C4
Access: Read/Write
Reset: 0x0

This register is used to count the number of received frames that had a code error counter.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RCDE	The receive code error counter. This register is incremented each time a valid carrier was present and at least one invalid data symbol was detected.

4.10.40 Receive Carrier Sense Error Counter (RCSE)

GE0 Address: 0x190000C8
GE1 Address: 0x1A0000C8
Access: Read/Write
Reset: 0x0

This register is used to count the number of frames received that had a false carrier.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RCSE	The receive false carrier counter. This register is incremented each time a false carrier is detected during idle, as defined by a 1 on RX_ER and an 0xE on RXD. This event is reported along with the statistics generated on the next received frame. Only one false carrier condition can be detected and logged between frames.

4.10.41 Receive Undersize Packet Counter (RUND)

GE0 Address: 0x190000CC
GE1 Address: 0x1A0000CC
Access: Read/Write
Reset: 0x0

This register is used to count the number of received packets that were undersized.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RUND	The receive undersize packet counter. This register is incremented each time a frame is received which is less than 64 bytes in length and contains a valid FCS and were otherwise well formed. This does not include Range Length errors

4.10.42 Receive Oversize Packet Counter (ROVR)

GE0 Address: 0x190000D0
GE1 Address: 0x1A0000D0
Access: Read/Write
Reset: 0x0

This register is used to count received packets that were oversized.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	ROVR	The receive oversize packet counter., This register is incremented each time a frame is received which exceeded 1518 (non-VLAN) or 1522 (VLAN) and contains a valid FCS and were otherwise well formed. This does not include Range Length errors.

4.10.43 Receive Fragments Counter (RFRG)

GE0 Address: 0x190000D4
GE1 Address: 0x1A0000D4
Access: Read/Write
Reset: 0x0

This register is used to count received fragmented frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RFRG	The receive fragments counter. This register is incremented for each frame received which is less than 64 bytes in length and contains an invalid FCS. This includes integral and non-integral lengths.

4.10.44 Receive Jabber Counter (RJBR)

GE0 Address: 0x190000D8
GE1 Address: 0x1A0000D8
Access: Read/Write
Reset: 0x0

This register is used to count received jabber frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RJBR	The received jabber counter. This register is incremented for frames which exceed 1518 (non-VLAN) or 1522 (VLAN) bytes and contains an invalid FCS, including alignment errors.

4.10.45 Receive Dropped Packet Counter (RDRP)

GE0 Address: 0x190000DC
GE1 Address: 0x1A0000DC
Access: Read/Write
Reset: 0x0

This register is used to count received dropped packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RDRP	The received dropped packets counter. this register is incremented for frames received which are streamed to the system but are later dropped due to a lack of system resources.

4.10.46 Transmit Byte Counter (TBYT)

GE0 Address: 0x190000E0
GE1 Address: 0x1A0000E0
Access: Read/Write
Reset: 0x0

This register is used to count transmitted bytes.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:0	TYBT	The transmit byte counter. This register is incremented by the number of bytes that were put on the wire including fragments of frames that were involved with collisions. This count does not include preamble/SFD or jam bytes.

4.10.47 Transmit Packet Counter (TPKT)

GE0 Address: 0x190000E4
GE1 Address: 0x1A0000E4
Access: Read/Write
Reset: 0x0

This register is used to count transmitted packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TPKT	The transmit packet counter. This register is incremented for each transmitted packet (including bad packets, excessive deferred packets, excessive collision packets, late collision packets, all Unicast, Broadcast and Multicast packets.

4.10.48 Transmit Multicast Packet Counter (TMCA)

GE0 Address: 0x190000E8
GE1 Address: 0x1A0000E8
Access: Read/Write
Reset: 0x0

This register is used to count transmitted multicast packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TMCA	Transmit multicast packet counter. Incremented for each multicast valid frame transmitted (excluding broadcast frames).

4.10.49 Transmit Broadcast Packet Counter (TBCA)

GE0 Address: 0x190000EC
GE1 Address: 0x1A0000EC
Access: Read/Write
Reset: 0x0

This register is used to count transmitted broadcast packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TBCA	Transmit broadcast packet counter. Incremented for each broadcast frame transmitted (excluding multicast frames).

4.10.50 Transmit Pause Control Frame Counter (TXPF)

GE0 Address: 0x190000F0
GE1 Address: 0x1A0000F0
Access: Read/Write
Reset: 0x0

This register is used to count transmitted pause control frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TXPF	Transmit pause frame packet counter. Incremented each time a valid pause MAC control frame is transmitted.

4.10.51 Transmit Deferral Packet Counter (TDFR)

GE0 Address: 0x190000F4
GE1 Address: 0x1A0000F4
Access: Read/Write
Reset: 0x0

This register is used to count transmitted deferral packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TDFR	Transmit deferral packet counter. Incremented for each frame that was deferred on its first transmission attempt. Does not include frames involved in collisions.

4.10.52 Transmit Excessive Deferral Packet Counter (TEDF)

GE0 Address: 0x190000F8
GE1 Address: 0x1A0000F8
Access: Read/Write
Reset: 0x0

This register is used to count excessive transmitted deferral packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TEDF	Transmit excessive deferral packet counter. Incremented for frames aborted that were deferred for an excessive period of time (3036 byte times).

4.10.53 Transmit Single Collision Packet Counter (TSCL)

GE0 Address: 0x190000FC
GE1 Address: 0x1A0000FC
Access: Read/Write
Reset: 0x0

This register is used to count transmitted single collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TSCL	Transmit single collision packet counter. Incremented for each frame transmitted that experienced exactly one collision during transmission.

4.10.54 Transmit Multiple Collision Packet (TMCL)

GE0 Address: 0x19000100
GE1 Address: 0x1A000100
Access: Read/Write
Reset: 0x0

This register is used to count transmitted multiple collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TMCL	Transmit multiple collision packet counter. Incremented for each frame transmitted that experienced 2–15 collisions (including any late collisions) during transmission as defined using the RETRY[3:0] field of the Tx function control register.

4.10.55 Transmit Late Collision Packet Counter (TLCL)

GE0 Address: 0x19000104
GE1 Address: 0x1A000104
Access: Read/Write
Reset: 0x0

This register is used to count transmitted late collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TLCL	Transmit late collision packet counter. Incremented for each frame transmitted that experienced a late collision during a transmission attempt. Late collisions are defined using the LCOL[5:0] field of the Tx function control register.

4.10.56 Transmit Excessive Collision Packet Counter (TXCL)

GE0 Address: 0x19000108
GE1 Address: 0x1A000108
Access: Read/Write
Reset: 0x0

This register is used to count excessive transmitted collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TXCL	Transmit excessive collision packet counter. Incremented for each frame that experienced 16 collisions during transmission and was aborted.

4.10.57 Transmit Total Collision Counter (TNCL)

GE0 Address: 0x1900010C
GE1 Address: 0x1A00010C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted total collision packets.

Bit	Bit Name	Description

31:13	RES	Reserved. Must be written with zero. Contains zeros when read.
12:0	TNCL	Transmit total collision counter. Incremented by the number of collisions experienced during the transmission of a frame as defined as the simultaneous presence of signals on the DO and RD circuits (i.e., transmitting and receiving at the same time). Note, this register does not include collisions that result in an excessive collision condition).

4.10.58 Transmit Pause Frames Honored Counter (TPFH)

GE0 Address: 0x19000110
GE1 Address: 0x1A000110
Access: Read/Write
Reset: 0x0

This register is used to count honored transmitted pause frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TPFH	Transmit pause frames honored counter. Incremented each time a valid pause MAC control frame is transmitted and honored.

4.10.59 Transmit Drop Frame Counter (TDRP)

GE0 Address: 0x19000114
GE1 Address: 0x1A000114
Access: Read/Write
Reset: 0x0

This register is used to count transmitted drop frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TDRP	Transmit drop frame counter. Incremented each time input PFH is asserted.

4.10.60 Transmit Jabber Frame Counter (TJBR)

GE0 Address: 0x19000118
GE1 Address: 0x1A000118
Access: Read/Write
Reset: 0x0

This register is used to count transmitted jabber frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TJBR	Transmit jabber frame counter. Incremented for each oversized transmitted frame with an incorrect FCS value.

4.10.61 Transmit FCS Error Counter (TFCS)

GE0 Address: 0x1900011C
GE1 Address: 0x1A00011C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted FCS errors.

Bit	Bit Name	Description

31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TFCS	Transmit FCS error counter. Incremented for every valid sized packet with an incorrect FCS value.

4.10.62 Transmit Control Frame Counter (TXCF)

GE0 Address: 0x19000120
GE1 Address: 0x1A000120
Access: Read/Write
Reset: 0x0

This register is used to count transmitted control frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TXCF	Transmit control frame counter. Incremented for every valid size frame with a type field signifying a control frame.

4.10.63 Transmit Oversize Frame Counter (TOVR)

GE0 Address: 0x19000124
GE1 Address: 0x1A000124000128
Access: Read/Write
Reset: 0x0

This register is used to count transmitted oversize frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TOVR	Transmit oversize frame counter. Incremented for each oversized transmitted frame with an correct FCS value.

4.10.64 Transmit Undersize Frame Counter (TUND)

GE0 Address: 0x19000128
GE1 Address: 0x1A000128
Access: Read/Write
Reset: 0x0

This register is used to count transmitted undersize frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TUND	Transmit undersize frame counter. Incremented for every frame less then 64 bytes, with a correct FCS value.

4.10.65 Transmit Fragment Counter (TFRG)

GE0 Address: 0x1900012C
GE1 Address: 0x1A00012C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted fragments.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TFRG	Transmit fragment counter. Incremented for every frame less then 64 bytes, with an incorrect FCS value.

4.10.66 Carry Register 1 (CAR1)

GE0 Address: 0x19000130
GE1 Address: 0x1A000130
Access: Read-Only
Reset: 0x0

Carry register bits are cleared on carry register write while the respective bit is asserted.

Bit	Bit Name	Description
31	C1_64	Carry register 1 TR64 counter carry bit
30	C1_127	Carry register 1 TR127 counter carry bit
29	C1_255	Carry register 1 TR255 counter carry bit
28	C1_511	Carry register 1 TR511 counter carry bit
27	C1_1K	Carry register 1 TR1K counter carry bit
26	C1_MAX	Carry register 1 TRMAX counter carry bit
25	C1_MGV	Carry register 1 TRMGV counter carry bit
24:17	RES	Reserved. Must be written with zero. Contains zeros when read.
16	C1_RBY	Carry register 1 RBYT counter carry bit
15	C1_RPK	Carry register 1 RPKT counter carry bit
14	C1_RFC	Carry register 1 RFCS counter carry bit
13	C1_RMC	Carry register 1 RMCA counter carry bit
12	C1_RBC	Carry register 1 RBCA counter carry bit
11	C1_RXC	Carry register 1 RXCF counter carry bit
10	C1_RXP	Carry register 1 RXPF counter carry bit
9	C1_RXU	Carry register 1 RXUO counter carry bit
8	C1_RAL	Carry register 1 RALN counter carry bit
7	C1_RFL	Carry register 1 RFLR counter carry bit
6	C1_RCD	Carry register 1 RCDE counter carry bit
5	C1_RCS	Carry register 1 RCSE counter carry bit
4	C1_RUN	Carry register 1 RUND counter carry bit
3	C1_ROV	Carry register 1 ROVR counter carry bit
2	C1_RFR	Carry register 1 RFRG counter carry bit
1	C1_RJB	Carry register 1 RJBR counter carry bit
0	C1_RDR	Carry register 1 RDRP counter carry bit

4.10.67 Carry Register 2 (CAR2)

GE0 Address: 0x19000134
GE1 Address: 0x1A000134
Access: Read-Only
Reset: 0x0

Carry register bits are cleared on carry register write while the respective bit is asserted.

Bit	Bit Name	Description
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.
19	C2_TJB	Carry register 2 TJBR counter carry bit
18	C2_TFC	Carry register 2 TFCS counter carry bit
17	C2_TCF	Carry register 2 TXCF counter carry bit
16	C2_TOV	Carry register 2 TOVR counter carry bit
15	C2_TUN	Carry register 2 TUND counter carry bit
14	C2_TFG	Carry register 2 TFRG counter carry bit
13	C2_TBY	Carry register 2 TBYT counter carry bit
12	C2_TPK	Carry register 2 TPKT counter carry bit
11	C2_TMC	Carry register 2 TMCA counter carry bit
10	C2_TBC	Carry register 2 TBCA counter carry bit
9	C2_TPF	Carry register 2 TXPF counter carry bit
8	C2_TDF	Carry register 2 TDFR counter carry bit
7	C2_TED	Carry register 2 TEDF counter carry bit
6	C2_TSC	Carry register 2 TSCL counter carry bit
5	C2_TMA	Carry register 2 TMCL counter carry bit
4	C2_TLC	Carry register 2 TLCL counter carry bit
3	C2_TXC	Carry register 2 TXCL counter carry bit
2	C2_TNC	Carry register 2 TNCL counter carry bit
1	C2_TPH	Carry register 2 TPFH counter carry bit
0	C2_TDP	Carry register 2 TDRP counter carry bit

4.10.68 Carry Mask Register 1 (CAM1)

GE0 Address: 0x19000138
GE1 Address: 0x1A000138
Access: Read/Write
Reset: 0x1

When one of these mask bits is set to zero, the corresponding interrupt bit is allowed to cause interrupt indications on output CARRY.

Bit	Bit NaM1e	Description
31	M1_64	Mask register 1 TR64 counter carry bit
30	M1_127	Mask register 1 TR127 counter carry bit
29	M1_255	Mask register 1 TR255 counter carry bit
28	M1_511	Mask register 1 TR511 counter carry bit
27	M1_1K	Mask register 1 TR1K counter carry bit
26	M1_MAX	Mask register 1 TRMAX counter carry bit
25	M1_MGV	Mask register 1 TRMGV counter carry bit
24:17	RES	Reserved. Must be written with zero. Contains zeros when read.
16	M1_RBY	Mask register 1 RBYT counter carry bit
15	M1_RPK	Mask register 1 RPKT counter carry bit
14	M1_RFC	Mask register 1 RFCS counter carry bit
13	M1_RMC	Mask register 1 RMCA counter carry bit
12	M1_RBC	Mask register 1 RBCA counter carry bit
11	M1_RXC	Mask register 1 RXCF counter carry bit
10	M1_RXP	Mask register 1 RXPF counter carry bit
9	M1_RXU	Mask register 1 RXUO counter carry bit
8	M1_RAL	Mask register 1 RALN counter carry bit
7	M1_RFL	Mask register 1 RFLR counter carry bit
6	M1_RCD	Mask register 1 RCDE counter carry bit
5	M1_RCS	Mask register 1 RCSE counter carry bit
4	M1_RUN	Mask register 1 RUND counter carry bit
3	M1_ROV	Mask register 1 ROVR counter carry bit
2	M1_RFR	Mask register 1 RFRG counter carry bit
1	M1_RJB	Mask register 1 RJBR counter carry bit
0	M1_RDR	Mask register 1 RDRP counter carry bit

4.10.69 Carry Mask Register 2 (CAM2)

GE0 Address: 0x1900013C
GE1 Address: 0x1A00013C
Access: Read/Write
Reset: 0x1

When one of these mask bits is set to zero, the corresponding interrupt bit is allowed to cause interrupt indications on output CARRY.

Bit	Bit Name	Description
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.
19	M2_TJB	Mask register 2 TJBR counter carry bit
18	M2_TFC	Mask register 2 TFCS counter carry bit
17	M2_TCF	Mask register 2 TXCF counter carry bit
16	M2_TOV	Mask register 2 TOVR counter carry bit
15	M2_TUN	Mask register 2 TUND counter carry bit
14	M2_TFG	Mask register 2 TFRG counter carry bit
13	M2_TBY	Mask register 2 TBYT counter carry bit
12	M2_TPK	Mask register 2 TPKT counter carry bit
11	M2_TMC	Mask register 2 TMCA counter carry bit
10	M2_TBC	Mask register 2 TBCA counter carry bit
9	M2_TPF	Mask register 2 TXPF counter carry bit
8	M2_TDF	Mask register 2 TDFR counter carry bit
7	M2_TED	Mask register 2 TEDF counter carry bit
6	M2_TSC	Mask register 2 TSCL counter carry bit
5	M2_TMA	Mask register 2 TMCL counter carry bit
4	M2_TLC	Mask register 2 TLCL counter carry bit
3	M2_TXC	Mask register 2 TXCL counter carry bit
2	M2_TNC	Mask register 2 TNCL counter carry bit
1	M2_TPH	Mask register 2 TPFH counter carry bit
0	M2_TDP	Mask register 2 TDRP counter carry bit

4.10.70 DMA Transfer Control for Queue 0 (DMATXCNTRL_Q0)

GE0 Address: 0x19000180
GE1 Address: 0x1A000180
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 0

4.10.71 Descriptor Address for Queue 0 Tx (DMATXDESCR_Q0)

GE0 Address: 0x19000184
GE1 Address: 0x1A000184
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 0
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

4.10.72 Transmit Status (DMATXSTATUS)

GE0 Address: 0x19000188
GE1 Address: 0x1A000188
Access: Read/Write
Reset: 0x0

This register is used to set the bits and flags regarding the DMA controller and its transferring status.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:16	TXPKTCOUNT	This 8-bit TX packet counter increments when the DMA controller transfers a packet successfully, and decrements when the host writes a 1 to TX_PKT_SENT (bit [0]).
15:12	RES	Reserved.
11	TX_UNDERRUN_Q3	Indicates TXUNDERRUN_Q3 as an interrupt source
10	TX_UNDERRUN_Q2	Indicates TXUNDERRUN_Q2 as an interrupt source
9	TX_UNDERRUN_Q1	Indicates TXUNDERRUN_Q1 as an interrupt source
8:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	BUS_ERROR	Indicates that the DMA controller received a host/slave split, error, or retry response
2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	TXUNDERRUN_Q0	This bit is set when the DMA controller reads a set (”1”) Empty Flag in the descriptor it is processing
0	TXPKTSENT	Indicates that one or more packets transferred successfully. This bit is cleared when TXPKTCOUNT (bits [23:16]) is zero. Writing a 1 to this bit reduces TXPKTCOUNT by one.

4.10.73 Receive Control (DMARXCTRL)

GE0 Address: 0x1900018C
GE1 Address: 0x1A00018C
Access: Read/Write
Reset: 0x0

This register is used to enable the DMA to receive packets.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	RXENABLE	Allows the DMA to receive packet transfers. When set, the built-in DMA controller begins receiving packets as the FIFO indicates they are available (FRSOF asserted). The DMA controller clears this bit when it encounters an RX overflow or bus error state.

4.10.74 Pointer to Receive Descriptor (DMARXDESCR)

GE0 Address: 0x19000190
GE1 Address: 0x1A000190
Access: Read/Write
Reset: 0x0

This register is used to find the location of the first TX packet descriptor in the memory.

Bit	Bit Name	Description
31:2	DESCRIPTOR_ ADDRESS	The descriptor address. When the RXENABLE (bit [0] of the "Receive Control (DMARXCTRL)" register) is set by the host, the DMA controller reads this register to find the host memory location of the first receive packet descriptor.
1:0	RES	Ignored by the DMA controller, because it is a requirement of the system that all descriptors are 32-bit aligned in the host memory.

4.10.75 Receive Status (DMARXSTATUS)

GE0 Address: 0x19000194
GE1 Address: 0x1A000194
Access: Read/Write
Reset: 0x0

This register is used to set the bits and flags regarding the DMA controller and its receiving status.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:16	RXPKTCOUNT	This 8-bit receive packet counter increments when the DMA controller transfers a packet successfully, and decrements when the host writes a 1 to RXPKTRECEIVED (bit [0]).
15:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	BUSERROR	Indicates that the DMA controller received a host/slave split, error, or retry response
2	RXOVERFLOW	This bit is set when the DMA controller reads a set empty flag in the descriptor it is processing
1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	RXPKT RECEIVED	Indicates that one or more packets were received successfully. This bit is cleared when the RXPKTCOUNT (bits [23:16]) is zero. Writing a 1 to this bit reduces RXPKTCOUNT by one.

4.10.76 Interrupt Mask (DMAINTRMASK)

GE0 Address: 0x19000198
GE1 Address: 0x1A000198
Access: Read/Write
Reset: 0x0

This register is used to configure interrupt masks for the DMA. Setting a bit to 1 enables the corresponding status signal as an interrupt source. The register "DMA Interrupts" is the AND of DMA status bits with this register.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11	TX_UNDERRUN_Q3_MASK	Setting this bit 1 enables TXUNDERRUN_Q3(bit [11] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
10	TX_UNDERRUN_Q2_MASK	Setting this bit 1 enables TXUNDERRUN_Q2 (bit [10] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
9	TX_UNDERRUN_Q1_MASK	Setting this bit 1 enables TXUNDERRUN_Q1 (bit [9] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
8	RES	Reserved. Must be written with zero. Contains zeros when read.
7	BUS_ERROR_MASK	Setting this bit to 1 enables BUSERROR (bit [3] in the "Receive Status (DMARXSTATUS)" register) as an interrupt source
6	RX_OVERFLOW_MASK	Setting this bit to 1 enables RXOVERFLOW (bit [1] in the "Receive Status (DMARXSTATUS)" register) as in interrupt source
5	RES	Reserved. Must be written with zero. Contains zeros when read.
4	RXPKTRECEIVED_MASK	Enables RXPKTRECEIVED (bit [0] in the "Receive Status (DMARXSTATUS)" register) as an interrupt source
3	BUSERROR_MASK	Setting this bit to 1 enables BUSERROR (bit [3] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	TX_UNDERRUN_Q0_MASK	Setting this bit 1 enables TXUNDERRUN_Q0 (bit [1] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
0	TXPKTSENT_MASK	Setting this bit to 1 enables TXPKTSENT (bit [0] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source

4.10.77 Interrupts (DMAINTERRUPT)

GE0 Address: 0x1900019C
GE1 Address: 0x1A00019C
Access: Read/Write
Reset: 0x0

This register is used to configure interrupts for the DMA. Flags in this register clear when their corresponding Status bit is cleared.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11	TX_UNDERRUN_Q3	Setting this bit 1 enables TXUNDERRUN_Q3(bit [11] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
10	TX_UNDERRUN_Q2	Setting this bit 1 enables TXUNDERRUN_Q2 (bit [10] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
9	TX_UNDERRUN_Q1	Setting this bit 1 enables TXUNDERRUN_Q1 (bit [9] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
8	RES	Reserved. Must be written with zero. Contains zeros when read.
7	BUS_ERROR_MASK	Setting this bit to 1 records an Rx bus error interrupt when BUS_ERROR (bit [3] in the "Receive Status (DMARXSTATUS)" register) and BUS_ERROR_MASK (bit [7] of the "Interrupt Mask (DMAINTRMASK)" register) are both set
6	RX_OVERFLOW_MASK	Setting this bit to 1 records an Rx overflow error interrupt when RX_OVERFLOW (bit [1] in the "Receive Status (DMARXSTATUS)" register) and RX_OVERFLOW_MASK (bit [6] of the "Interrupt Mask (DMAINTRMASK)" register) are both set
5	RES	Reserved. Must be written with zero. Contains zeros when read.
4	RXPKT_RECEIVED_MASK	Records a RX_PKT_RECEIVED error interrupt when RX_PKT_RECEIVED (bit [0] in the "Receive Status (DMARXSTATUS)" register) and RXPKT_RECEIVED_MASK (bit [4] of the "Interrupt Mask (DMAINTRMASK)" register) are both set
3	BUS_ERROR	Setting this bit to 1 enables BUSERROR (bit [3] in the "Transmit Status (DMATXSTATUS)" register) and BUSERROR_MASK (bit [3] of the "Interrupt Mask (DMAINTRMASK)" register) are both set
2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	TX_UNDERRUN_Q0	Setting this bit to 1 enables TX_UNDERRUN (bit [1] in the "Transmit Status (DMATXSTATUS)" register) and TX_UNDERRUN_MASK (bit [1] of the "Interrupt Mask (DMAINTRMASK)" register) are both set
0	TXPKTSENT	Set this bit to 1 enables TXPKTSENT (bit [0] in the "Transmit Status (DMATXSTATUS)" register) and TXPKTSENT_MASK (bit [0] of the "Interrupt Mask (DMAINTRMASK)" register) are both set

4.10.78 Ethernet TX Burst (ETH_ARB_TX_BURST)

GE0 Address: 0x190001A0
GE1Address: 0x1A0001A0
Access: Read/Write
Reset: 0x48

Tx and Rx requests are arbitrated based on these parameters. These parameters ensure DDR bandwidth is available to both Tx and Rx until the specified number of DWs transfer. Note that this affects the bandwidth/latency of the data for transmit and receive.

Bit	Bit Name	Description
31:26	RES	Reserved
25:16	MAX_RCV_BURST	Maximum number of DWs to be continuously allowed for Rx
15:10	RES	Reserved
9:0	MAX_TX_BURST	Maximum number of DWs to be continuously allowed for Tx

4.10.79 Current Tx and Rx FIFO Depth (ETH_XFIFO_DEPTH)

GE0 Address: 0x190001A8
GE1Address: 0x1A0001A8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25:16	CURRENT_RX_FIFO_DEPTH	Current Rx FIFO depth
15:10	RES	Reserved
9:0	CURRENT_TX_FIFO_DEPTH	Current Tx FIFO depth

4.10.80 Ethernet Transmit FIFO Throughput (ETH_TXFIFO_TH)

GE0 Address: 0x190001A4
GE1 Address: 0x1A0001A4
Access: Read/Write
Reset: See field description

This Ethernet register has a 2 KB Tx FIFO. It is use to determine the minimum and maximum levels of the transfer FIFO and correspondingly keep the transmit levels within the range to keep a continuous data transfer flowing.

Bit	Bit Name	Reset	Description
31:26	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
25:16	TXFIFO_MAXTH	0x1D8	This bit represents the maximum number of double words in the Tx FIFO, and once this limit is surpassed, this bit should be de-asserted
15:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:0	TXFIFO_MINTH	0x160	This bit specifies the minimum number of double words in the Tx FIFO, and if it is less than this value, this bit needs to be asserted.

4.10.81 Ethernet Receive FIFO Threshold (ETH_RXFIFO_TH)

GE0 Address: 0x190001AC
GE1 Address: 0x1A0001AC
Access: Read/Write
Reset: See field description

This Ethernet register has a 2 KB Rx FIFO. It is used to determine the minimum and maximum levels of the transfer FIFO and correspondingly keep the transmit levels within the range to keep a continuous data transfer flowing.

Bit	Bit Name	Reset	Description
31:10	SCRATCHREG_0	0x28	This bit is a pure scratch pad register that can be used by the CPU for any general purpose.
9:0	RCVFIFO_MINTH	0x0	The minimum number of double words in the receive FIFO. Once this number is reached, this bit needs to be asserted.

4.10.82 Ethernet Free Timer

GE0 Address: 0x190001B8
GE1 Address: 0x1A0001B8
Access: Read/Write
Reset: See field description

This register updates the Ethernet descriptors with time stamps

Bit	Bit Name	Reset	Description	
31	TIMER_UPDATE	0x1	0	Timer update at the AHB_CLK
			1	Free timer at the AHB_CLK/4
30:21	SCRATCHREG_1	0x0	The pure general purpose register for use by the CPU	
20:0	FREE_TIMER	0x3FFFFF	Free timer	

4.10.83 DMA Transfer Control for Queue 1 (DMATXCNTRL_Q1)

GE0 Address: 0x190001C0
GE1 Address: 0x1A0001C0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 1

4.10.84 Descriptor Address for Queue 1 Tx (DMATXDESCR_Q1)

GE0 Address: 0x190001C4
GE1 Address: 0x1A0001C4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 1
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

4.10.85 DMA Transfer Control for Queue 2 (DMATXCNTRL_Q2)

GE0 Address: 0x190001C8
GE1 Address: 0x1A0001C8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 2

4.10.86 Descriptor Address for Queue 2 Tx (DMATXDESCR_Q2)

GE0 Address: 0x190001CC
GE1 Address: 0x1A0001CC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 2
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

4.10.87 DMA Transfer Control for Queue 3 (DMATXCNTRL_Q3)

GE0 Address: 0x190001D0
GE1 Address: 0x1A0001D0 Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 3

4.10.88 Descriptor Address for Queue 3 Tx (DMATXDESCR_Q3)

GE0 Address: 0x190001D4
GE1 Address: 0x1A0001D4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 3
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

4.10.89 DMA Transfer Arbitration Configuration (DMATXARBCFG)

GE0 Address: 0x190001D8
GE1 Address: 0x1A0001D8
Access: Read/Write
Reset: See field description

This register is used to select the type of arbitration used for the QoS feature and the weight to be assigned to a particular queue. Note that a weight of zero is not permitted and causes the hardware to misbehave.

Bit	Bit Name	Reset	Description	
31:26	WGT3	0x1	The weight for Queue 3, if WRR has been selected	
25:20	WGT2	0x2	The weight for Queue 2, if WRR has been selected	
19:14	WGT1	0x4	The weight for Queue 1, if WRR has been selected	
13:8	WGT0	0x8	The weight for Queue 0, if WRR has been selected	
7:1	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	RRMODE	0x4	Round robin mode	
			0	Simple priority (Q0 highest priority)
			1	Weighted round robin (WRR)

4.11 USB Controller Registers

Table 4-12 summarizes the USB controller registers and the modes they support.

Table 4-12. **USB Controller Registers** [1]

Offset	Access	Name	Description	DEV	SPH	Page
Identification Registers Declare the slave interface presence						
0x1B000000	RO	ID	Identification	X	X	page 129
0x1B000004	RO	HWGENERAL	General Hardware Parameters	X	X	page 129
0x1B000008	RO	HWHOST	Host Hardware Parameters		X	page 129
0x1B00000C	RO	HWDEVICE	Device Hardware Parameters	X		page 130
0x1B000010	RO	HWTXBUF	Tx Buffer Hardware Parameters	X	X	page 130
0x1B000014	RO	HWRXBUF	Rx Buffer Hardware Parameters	X	X	page 130
Device/Host Timer Registers Measure time-related activities						
0x1B000080	RW	GPTIMER0LD	General Purpose Timer 0 Load	X	X	page 130
0x1B000084	Varies	GPTIMER0CTRL	General Purpose Timer 0 Control	X	X	page 131
0x1B000088	RW	GPTIMER1LD	General Purpose Timer 1 Load	X	X	page 131
0x1B00008C	RW	GPTIMER1CTRL	General Purpose Timer 1 Control	X	X	page 132
Device/Host Capability Registers Specify the software limits, restrictions, and capabilities of the host/device controller implementation						
0x1B000100	RO	CAPLENGTH	Capability Register Length	X	X	page 132
0x1B000102	RO	HCIVERSION	Host Interface Version Number		X	page 133
0x1B000104	RO	HCSPARAMS	Host Control Structural Parameters		X	page 133
0x1B000108	RO	HCCPARAMS	Host Control Capability Parameters		X	page 134
0x1B000120	RO	DCIVERSION	Device Interface Version Number	X		page 134
0x1B000122	RO	DCCPARAMS	Device Control Capability Parameters	X		page 134

Table 4-12. **USB Controller Registers (continued)[1]**

Offset	Access	Name	Description	DEV	SPH	Page
Device/Host Operational Registers						
0x1B000140	Varies	USBCMD	USB Command	X	X	page 135
0x1B000144	Varies	USBSTS	USB Status	X	X	page 137
0x1B000148	RW	USBINTR	USB Interrupt Enable	X	X	page 139
0x1B00014C	Varies	FRINDEX	USB Frame Index	X	X	page 141
0x1B000154	RW	PERIODICLISTBASE	Frame List Base Address		X	page 142
—	RW	DEVICEADDR	USB Device Address	X		page 142
0x1B000158	RW	ASYNCLISTADDR	Next Asynchronous List Address		X	page 142
—	RW	ENDPOINTLIST_ ADDR	Address at Endpoint List in Memory	X		page 143
0x1B00015C	RW	TTCTRL	TT Status and Control		X	page 143
0x1B000160	RW	BURSTSIZE	Programmable Burst Size	X	X	page 143
0x1B000164	RW	TXFILLTUNING	Host Tx Pre-Buffer Packet Tuning		X	page 144
0x1B000178	RWC	ENDPTNAK	Endpoint NAK	X		page 145
0x1B00017C	RW	ENDPTNAKEN	Endpoint NAK Enable	X		page 145
0x1B000184	Varies	PORTSC0	Port/Status Control	X	X	page 146
0x1B0001A8	RW	USBMODE	USB Mode	X	X	page 151
0x1B0001AC	RWC	ENDPTSETUPSTAT	Endpoint Setup Status	X		page 152
0x1B0001B0	RWC	ENDPTPRIME	Endpoint Initialization	X		page 152
0x1B0001B4	WC	ENDPTFLUSH	Endpoint De-Initialization	X		page 153
0x1B0001B8	RO	ENDPTSTATUS	Endpoint Status	X		page 153
0x1B0001BC	RWC	ENDPTCOMPLETE	Endpoint Complete	X		page 154
0x1B0001C0	RW	ENDPTCTRL0	Endpoint Control 0	X		page 154
0x1B0001C4	RW	ENDPTCTRL1	Endpoint Control 1	X		page 155
0x1B0001C8	RW	ENDPTCTRL2	Endpoint Control 2	X		page 155
0x1B0001CC	RW	ENDPTCTRL3	Endpoint Control 3	X		page 155
0x1B0001D0	RW	ENDPTCTRL4	Endpoint Control 4	X		page 155
0x1B0001D4	RW	ENDPTCTRL5	Endpoint Control 5	X		page 155

[1]DEV = Device Mode
SPH = Single-Port Host

4.11.1 Identification (ID)

Offset: 0x1B000000
Access: Read-Only
Reset Value: 0x42FA05

Provides a simple way to determine whether the system provides the USB-HS USB 2.0 core and identifies the USB-HS USB 2.0 core and revision number.

Bit	Name	Description
31:24	RES	Reserved. Must be set to 0.
23:16	REVISION[7:0]	Core revision number
15:14	RES	Reserved. Must be set to 1.
13:8	NID[5:0]	Complement version of ID bits [5:0]
7:6	RES	Reserved. Must be set to 0.
5:0	ID	Configuration number; Set to 0x05 Indicates that the peripheral is the USB-HS USB 2.0 core.

4.11.2 General Hardware Parameters (HWGENERAL)

Offset: 0x1B000004
Access: Read-Only
Reset Value: 0x22

Bit	Name	Description
31:10	RES	Reserved. Must be set to 0.
9	SM	VUSB_HS_PHY_SERIAL
8:6	PHYM	VUSB_HS_PHY_TYPE
5:4	PHYW	VUSB_HS_PHY16_8
3	RES	Reserved
2:1	CLKC	VUSB_HS_CLOCK_CONFIGURATION
0	RT	VUSB_HS_RESET_TYPE

4.11.3 Host Hardware Parameters (HWHOST)

Offset: 0x1B000008
Access: Read-Only
Reset Value: 0x1002001

Bit	Name	Description
31:24	TTPER	VUSB_HS_TT_PERIODIC_CONTEXTS
23:16	TTASY	VUSB_HS_TT_ASYNC_CONTEXTS
15:4	RES	Reserved. Must be set to 0.
3:1	NPORT	VUSB_HS_NUM_PORT – 1
0	HC	VUSB_HS_HOST

4.11.4 Device Hardware Parameters (HWDEVICE)

Offset: 0x1B00000C
Access: Read-Only
Reset Value: 0xD

Bit	Name	Description
31:6	RES	Reserved. Must be set to 0.
5:1	DEVEP	VUSB_HS_DEV_EP
0	DC	Device capable; [0 ≥ VUSB_HS_DEV]

4.11.5 Tx Buffer Hardware Parameters (HWTXBUF)

Offset: 0x1B000010
Access: Read-Only
Reset Value: 0x80060908

Bit	Name	Description
31:24	RES	Reserved. Must be set to 0.
23:16	TXCHANADD	VUSB_HS_TX_CHAN_ADD
15:8	TXADD	VUSB_HS_TX_ADD
7:0	TXBURST	VUSB_HS_TX_BURST

4.11.6 Rx Buffer Hardware Parameters (HWRXBUF)

Offset: 0x1B000014
Access: Read-Only
Reset Value: 0x608

Bit	Name	Description
31:16	RES	Reserved. Must be set to 0.
15:8	RXADD	VUSB_HS_RX_ADD
7:0	RXBURST	VUSB_HS_RX_BURST

4.11.7 General Purpose Timer 0 Load (GPTIMEROLD)

Offset: 0x1B000080
Access: Read/Write
Reset Value: 0

Contains the timer duration or load value.

Bit	Name	Description
31:24	RES	Reserved. Must be set to 0.
23:0	GPTLD	General purpose timer load value The value to load into the GPTCNT countdown timer on a reset action. This value in this register represents the time (in ms minus 1) for the timer duration.

4.11.8 General Purpose Timer 0 Control (GPTIMER0CTRL)

Offset: 0x1B000084
Access: See Field Descriptions
Reset Value: 0

Contains the timer control. A data field can be queried to determine the running count value. This timer has granularity on 1 µs and can be programmed to over 16 s. This timer supports two modes: a one-shot and a looped count. When the timer counter value goes to zero an interrupt can be generated using the timer interrupts in the USBSTS and USBINTR registers.

Bit	Name	Description	
31	GPTRUN	General purpose timer run (read/write) Enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.	
		0	Timer stop
		1	Timer run
30	GPTRST	General purpose timer reset (write-only)	
		0	No action
		1	Load counter value Writing a one to this bit reloads GPTCNT with the value in GPTLD.
29:25	RES	Reserved. Must be set to 0.	
24	GPTMODE	General purpose timer mode (read/write) Selects between a single-timer (one-shot) countdown and a looped countdown.	
		0	One-shot The timer counts down to zero, generates an interrupt, and stops until the counter is reset by software.
		1	Repeat The timer counts down to zero, generates an interrupt, and automatically reloads the counter to restart.
23:0	GPTCNT	General purpose timer counter (read-only) The running timer value.	

4.11.9 General Purpose Timer 1 Load (GPTIMER1LD)

Offset: 0x1B000088
Access: Read/Write
Reset Value: 0

See also "General Purpose Timer 0 Load (GPTIMER0LD)" on page 130.

Bit	Name	Description
31:24	RES	Reserved. Must be set to 0.
23:0	GPTLD	General purpose timer load value The value to load into the GPTCNT countdown timer on a reset action. This value in this register represents the time (in ms minus 1) for the timer duration.

4.11.10 General Purpose Timer 1 Control (GPTIMER1CTRL)

Offset: 0x1B00008C
Access: Read/Write
Reset Value: 0

See also "General Purpose Timer 0 Control (GPTIMER0CTRL)" on page 131.

Bit	Name	Description	
31	GPTRUN	General purpose timer run (read/write) Enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.	
		0	Timer stop
		1	Timer run
30	GPTRST	General purpose timer reset (write-only)	
		0	No action
		1	Load counter value Writing a one to this bit reloads GPTCNT with the value in GPTLD.
29:25	RES	Reserved. Must be set to 0.	
24	GPTMODE	General purpose timer mode (read/write) Selects between a single-timer (one-shot) countdown and a looped countdown.	
		0	One-shot The timer counts down to zero, generates an interrupt, and stops until the counter is reset by software.
		1	Repeat The timer counts down to zero, generates an interrupt, and automatically reloads the counter to restart.
23:0	GPTCNT	General purpose timer counter (read-only) The running timer value.	

4.11.11 Capability Register Length (CAPLENGTH)

Offset: 0x1B000100
Access: Read-Only
Reset Value: 0x40

Bit	Name	Description
31:8	RES	Reserved. Must be set to 0.
7:0	CAPLENGTH	Capability register length Indicates which offset to add to the beginning of the register base address of the operational registers (see Table 4-12, "Device/Host Operational Registers" on page 128)

4.11.12 Host Interface Version Number (HCIVERSION)

Offset: 0x1B000102
Access: Read-Only

Bit	Name	Description
31:16	RES	Reserved. Must be set to 0.
15:0	HCIVERSION	This two-byte register contains a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision, and the least significant byte is the minor revision.

4.11.13 Host Control Structural Parameters (HCSPARAMS)

Offset: 0x1B000104
Access: Read-Only

Bit	Name	Description
31:28	RES	Reserved. Must be set to 0.
27:24	N_TT	Number of transaction translators Indicates the number of embedded transaction translators associated with the USB2.0 host controller. Always set to 0.
23:20	N_PTT	Number of ports per transaction translator Indicates the number of ports assigned to each transaction translator within the USB2.0 host controller.
19:17	RES	Reserved. Must be set to 0.
16	PI	Port indicator Indicates whether ports support port indicator control. This field is always set to 1, so the port status and control registers include a read/writable field for controlling the port indicator state.
15:12	N_CC	Number of companion controllers Indicates the number of companion controllers associated with this USB 2.0 host controller. A value larger than zero in this field indicates there are companion USB1.1 host controller(s) and port-ownership hand-offs are supported. High, Full- and Low-speed devices are supported on the host controller root ports.
11:8	N_PCC	Number of ports per companion controller Indicates the number of ports supported per internal companion controller; used to indicate the port routing configuration to the system software.
7:5	RES	Reserved. Must be set to 0.
4	PPC	Port power control Indicates whether the host controller implementation includes port power control.
		0 — Indicates the ports do not have port power switches. The value of this field affects the functionality of the port power field in each port status and control register.
		1 — Indicates the ports have port power switches
3:0	N_PORTS	Number of downstream ports Specifies the number of physical downstream ports implemented on this host controller. The value determines how many port registers are addressable in the operational registers (see Table 4-12, "Device/Host Operational Registers" on page 128). Valid values range from 0x1–0xF. A zero in this field is undefined.

4.11.14 Host Control Capability Parameters (HCCPARAMS)

Offset: 0x1B000108
Access: Read-Only
Reset Value: 0x0006

Identifies multiple mode control addressing capability.

Bit	Name	Description	
31:16	RES	Reserved. Must be set to 0.	
15:8	EECP	EHCI extended capabilities pointer (default = 0) This optional field indicates the existence of a capabilities list.	
7:4	IST	Isochronous scheduling threshold; Indicates where software can reliably update the isochronous schedule relative to the current position of the executing host controller.	
		bit[7] = 0	The value of the least significant three bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures (one or more) before flushing the state
		bit[7] = 1	Host software assumes the host controller may cache an isochronous data structure for an entire frame
3	RES	Reserved. Must be set to 0.	
2	ASP	Asynchronous schedule park capability (default = 1) The feature can be disabled or enabled and set to a specific level by using the asynchronous schedule park mode enable and asynchronous schedule park mode count fields in the register "USB Command (USBCMD)" on page 135.	
		1	The host controller supports the park feature for high-speed queue heads in the asynchronous schedule
1	PFL	Programmable frame list flag	
		0	System software must use a frame list length of 1024 elements with this host controller. The frame list size field in the register "USB Command (USBCMD)" is read-only and must be set to zero.
		1	System software can specify and use a smaller frame list and configure the host controller via the frame list size field in the register "USB Command (USBCMD)". The frame list must always be aligned on a 4K-page boundary, ensuring the frame list is always physically contiguous.
0	ADC	64-bit addressing capability; must be set to 0. 64-bit addressing capability is not supported.	

4.11.15 Device Interface Version Number (DCIVERSION)

Offset: 0x1B000120
Access: Read-Only

Bit	Name	Description
31:16	RES	Reserved. Must be set to 0.
15:0	DCIVERSION	The device controller interface conforms to the two-byte BCD encoding of the interface version number contained in this register.

4.11.16 Device Control Capability Parameters (DCCPARAMS)

Offset: 0x1B000124
Access: Read-Only

Bit	Name	Description
31:9	RES	Reserved. Must be set to 0.
8	HC	Host capable; the controller can operate as an EHCI-compatible USB 2.0 host controller.
7	DC	Device capable; when set to 1, this controller is capable of operating as a USB 2.0 device.
6:5	RES	Reserved. Must be set to 0.
4:0	DEN	Device endpoint number Indicates the number of endpoints (0–16) built into the device controller. If this controller is not device capable, this field is zero.

4.11.17 USB Command (USBCMD)

Offset: 0x1B000140
Access: See Field Descriptions
Reset Value: 00080B00h (host mode)
00080000h (device mode)

Bit	Name	Description		
31:24	RES	Reserved. Must be set to zero.		
23:16	ITC	RW	Interrupt threshold control System software uses this field to set the max. rate the host/device controller issues interrupts at. ITC contains the maximum interrupt interval measured in micro-frames.	
			0x0	Immediate (no threshold)
			0x1	1 micro-frame
			0x2	2 micro-frames
			0x4	4 micro-frames
			0x8	8 micro-frames
			0x10	16 micro-frames
			0x20	32 micro-frames
			0x40	64 micro-frames
15	FS2	RW /RO	Frame list size Read/write if programmable frame list flag in the register "Host Control Structural Parameters (HCSPARAMS)" on page 133 is set to one. Specifies the size of the frame list that controls which bits in the register "USB Frame Index (FRINDEX)" on page 141 to use for the frame list current index. This field is made up of bits [15, 3:2] of this register.	
			000	1024 elements (4096 bytes) (default)
			001	512 elements (2048 bytes)
			010	256 elements (1024 bytes)
			011	128 elements (512 bytes)
			100	64 elements (256 bytes)
			101	32 elements (128 bytes)
			110	16 elements (64 bytes)
			111	8 elements (32 bytes)
14	ATDTW	RW	Add dTD tripwire (device mode only) Used as a semaphore to ensure the to proper addition of a new dTD to an active (primed) endpoint's linked list. This bit is set and cleared by software. This bit shall also be cleared by hardware when its state machine is hazard region for which adding a dTD to a primed endpoint may go unrecognized.	
13	SUTW	RW	Setup tripwire (device mode only) Used as a semaphore to ensure the 8-byte setup data payload is extracted from a QH by the DCD without being corrupted. If the setup lockout mode is off, a hazard exists when new setup data arrives while the DCD is copying the setup data payload from the QH for a previous setup packet. This bit is set and cleared by software and cleared by hardware when a hazard exists.	
12	RES	Reserved. Must be set to zero.		
11	ASPE	RW /RO	Asynchronous schedule park mode enable (Host mode only) If the asynchronous park capability bit in the register "Host Control Structural Parameters (HCSPARAMS)" is a one, this bit defaults to 0x1 and is R/W. Otherwise the bit must be a zero and is RO. Software uses this bit to enable or disable park mode.	
			0	Park mode is disabled
			1	Park mode is enabled
10	RES	Reserved. Must be set to zero.		

Bit	Name	Description		
9 8	ASP1 ASP0	RW /RO	Asynchronous schedule park mode count (optional) If the asynchronous park capability bit in the register "Host Control Structural Parameters (HCSPARAMS)" is a one, this field defaults to 0x3 and is R/W. Otherwise it defaults to zero and is RO. Contain a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule before continuing traversal of the asynchronous schedule. Valid values are 0x1–0x3. Software should not write a zero to this bit when park mode is enabled.	
7	RES	Reserved. Must be set to zero.		
6	IAA	RW	Interrupt on asynchronous advance doorbell (host mode only) Used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule states, it sets the interrupt on the asynchronous advance status bit in the register "USB Status (USBSTS)". If the interrupt on synchronous advance enable bit in the register "USB Interrupt Enable (USBINTR)" is set to one, the host controller asserts an interrupt at the next interrupt threshold. The host controller sets this bit to zero after setting the interrupt on the synchronous advance status bit in the register "USB Status (USBSTS)" to one. Software should not write a one to this bit if asynchronous schedule is inactive.	
5	ASE	RW	Asynchronous schedule enable (host mode only)	
			0	Do not process the asynchronous schedule (default)
			1	Use the register "Next Asynchronous List Address (ASYNCLISTADDR)" to access the asynchronous schedule
4	PSE	RW	Periodic schedule enable (host mode only)	
			0	Do not process the periodic schedule (default)
			1	Use the register "Frame List Base Address (PERIODICLISTBASE)" on page 142 to access the asynchronous schedule
3 2	FS1 FS0	RW /RO	Frame list size See bit [15], "FS2", for description.	
1	RST	RW	Controller reset (RESET) Software uses this bit to reset the controller. This bit is set to zero by the host/device controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register.	
			Host	When this bit is set by software, the host controller resets internal pipelines, timers, etc. to the initial values. Any transaction in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. SW should not set this bit to 1 when HCHalted in the register "USB Status (USBSTS)" is set to 0.
			Device	When software writes a 1 to this bit, the device controller resets internal pipelines, timers, etc. to the initial values. Writing a 1 to this bit when the device is in the attached state is not recommended. To ensure the device is not in attached state before initiating a device controller reset, primed endpoints must be flushed and the run/stop bit [0] set to 0.
0	RS	RW	Run/Stop (1 = Run, 0 = stop (default))	
			Host	When set to a 1, the host controller proceeds with the schedule and continues as long as this bit is set to 1. When this bit is set to 0, the host controller completes the current transaction on the USB then halts. The HCHalted bit in the register "USB Status (USBSTS)" indicates when the host controller has completed the transaction and stopped. Software should not write a one to this field unless the host controller is stopped.
			Device	Writing a 1 to this bit causes the device controller to enable a pull-up on D+ and initiates an attach event. This bit is not connected to pull-up enable, as the pull-up becomes disabled on transitioning to high-speed mode. This bit to prevents an attach event before the device controller is properly initialized. Writing a 0 causes a detach event.

4.11.18 USB Status (USBSTS)

Offset: 0x1B000144
Access: See Field Descriptions
Reset Value: 0

Indicates various states of the host/device controller and pending interrupts. This register does not indicate status resulting from a transaction on the serial bus. Software clears some bits in this register by writing a 1 to them.

Bit	Name	Description	
31:26	RES	Reserved. Must be set to zero.	
25	TI	RWC	General purpose timer interrupt 1 Set when the counter in the register "General Purpose Timer 1 Control (GPTIMER1CTRL)" on page 132 transitions to zero. Write-one-to-clear.
24	TI0	RWC	General purpose timer interrupt 0 Set when the counter in the register "General Purpose Timer 0 Control (GPTIMER0CTRL)" on page 131 transitions to zero. Write-one-to-clear.
23:20	RES	Reserved. Must be set to zero.	
19	UPI	RWC	USB host periodic interrupt Set by the host controller when the cause of an interrupt is a completion of a USB transaction where the transfer descriptor (TD) has an interrupt on complete (IOC) bit set and the TD was from the periodic schedule. This bit is also set by the host controller when a short packet (the actual number of bytes received was less than the expected number of bytes) is detected and the packet is on the periodic schedule. Write-one-to-clear.
18	UAI	RWC	USB host asynchronous interrupt Set by the host controller when the cause of an interrupt is a completion of a USB transaction where the TD has an interrupt on complete (IOC) bit set AND the TD was from the asynchronous schedule. This bit is also set by the host controller when a short packet (the actual number of bytes received was less than the expected number of bytes) is detected and the packet is on the asynchronous schedule. Write-one-to-clear.
17	RES	Reserved. Must be set to zero.	
16	NAKI	RO	Set by hardware when for one endpoint, both the Tx/Rx endpoint NAK bit and the corresponding Tx/Rx endpoint NAK enable bit are set. Automatically cleared by hardware when the all enabled Tx/Rx endpoint NAK bits are cleared.
15	AS	RO	Reports the real status of the asynchronous schedule (host mode only) The host controller is not required to immediately disable or enable the asynchronous schedule when software transitions the asynchronous schedule enable bit in the register "USB Command (USBCMD)" on page 135. When this bit and the asynchronous schedule enable bit are the same value, the asynchronous schedule is either enabled (1) or disabled (0 = Default).
14	PS	RO	Reports the real status of the periodic schedule (host mode only) The host controller is not required to immediately disable or enable the periodic schedule when software transitions the periodic schedule enable bit in the register "USB Command (USBCMD)". When this bit and the periodic schedule enable bit are the same value, the periodic schedule is either enabled (1) or disabled (0 = Default).
13	RCL	RO	Reclamation (host mode only) Used to detect an empty asynchronous schedule.
12	HCH	RO	HCHaIted (host mode only) This bit is a zero whenever the run/stop bit in the register "USB Command (USBCMD)" is set to one. The host controller sets this bit to one (default setting) after it has stopped executing because the run/stop bit is set to 0, either by software or by the host controller hardware.

Bit	Name	Description		
11	RES	Reserved. Must be set to zero.		
10	ULPII	RWC	ULPI interrupt Only present in designs where the configuration constant VUSB_HS_PHY_ULPI = 1.	
9	RES	Reserved. Must be set to zero.		
8	SLI	RWC	DCSuspend When a device controller enters a suspend state from an active state, this bit is set to 1. Cleared by the device controller upon exiting from a suspend state. Write-one-to-clear.	
7	SRI	RWC	Start-of-(micro-)frame (SOF) received When the device controller detects a SOF, this bit is set to 1. When a SOF is late, the device controller automatically sets this bit to indicate that an SOF was expected, thus this bit is set about every 1 ms in device FS mode and every 125 ms in HS mode, and synchronized to the received SOF. Because the device controller initializes to FS before connect, this bit is set at an interval of 1 ms during the prelude to connect and chirp. Write-one-to-clear.	
6	URI	RWC	USB reset received (device controller only) When the device controller detects a USB Reset and enters the default state (0), this bit is set to 1. Write-one-to-clear.	
5	AAI	RWC	Interrupt on asynchronous advance (Host mode only) System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a 1 to the interrupt on asynchronous advance doorbell bit in the register "USB Command (USBCMD)". Indicates the assertion of that interrupt source. Write-one-to-clear.	
4	RES	Reserved. Must be set to zero.		
3	FRI	RWC	Frame list rollover (Host mode only) The host controller sets this bit to a 1 when the frame list index rolls over from its maximum value to 0. The exact value at which the rollover occurs depends on frame list size, e.g, if the size (as programmed in the frame list size field of the register "USB Command (USBCMD)") is 1024, the frame index register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the host controller sets this bit to 1 every time FHINDEX [12] toggles. Write-one-to-clear.	
2	PCI	RWC	Port change detect	
			Host	The host controller sets this bit to 1 when on any port, a connect status or a port enable/disable change occurs, or the force port resume bit is set as the result of a transition on the suspended port.
			Device	The device controller sets this bit to1 when the port controller enters full- or high-speed operational state. When the port controller exits full- or high-speed operation states due to reset or suspend events, the notification mechanisms are the USB Reset Received bit and the DCSuspend bits respectively. Write-one-to-clear.
1	UEI	RWC	USB error interrupt When completion of a USB transaction results in an error condition, this bit along with the USBINT bit is set by the host/device controller if the TD on which the error interrupt occurred also had its interrupt on complete (IOC) bit set. Write-one-to-clear.	
0	UI	RWC	USB interrupt Set by the host/device controller when the cause of an interrupt is a completion of a USB transaction where the TD has an interrupt on complete (IOC) bit set. Also set by the host/device controller when a short packet (the actual number of bytes received was less than the expected number of bytes) is detected. Write-one-to-clear.	

4.11.19 USB Interrupt Enable (USBINTR)

Offset: 0x1B000148
Access: Read/Write
Reset Value: 0

Interrupts to software are enabled with this register. An interrupt is generated when a bit is set and the corresponding interrupt is active. The "USB Status (USBSTS)" register still shows interrupt sources even if they are disabled by this register, allowing polling of interrupt events by software.

Bit	Name	Description		
31:26	RES	Reserved. Must be set to zero.		
25	TIE1	General purpose timer interrupt enable 1; when enabled:		
		This bit:	**USBSTS bit:**	**Controller:**
		= 1	GPTINT1 = 1	Issues an interrupt at acknowledged by software clearing the general purpose timer interrupt 1 bit.
24	TIE0	General purpose timer interrupt enable 0; when enabled:		
		This bit:	**USBSTS bit:**	**Controller:**
		= 1	GPTINT0 = 1	Issues an interrupt at acknowledged by software clearing the general purpose timer interrupt 0 bit.
23:20	RES	Reserved. Must be set to zero.		
19	UPIE	USB host periodic interrupt enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host controller:**
		= 1	USBHSTPERINT = 1	Issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USB host periodic interrupt bit.
18	UAIE	USB host asynchronous interrupt enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host controller:**
		= 1	USBHSTASYNCINT = 1	Issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USB host asynchronous interrupt bit.
17	RES	Reserved. Must be set to zero.		
16	NAKE	NAK interrupt enable. Set by software if it wants to enable the hardware interrupt for the NAK interrupt bit. When enabled:		
		This bit:	**USBSTS bit:**	**Interrupt:**
		= 1	NAKI = 1	A hardware interrupt is generated.
15:11	RES	Reserved. Must be set to zero.		
10	ULPIE	ULPI enable; when enabled:		
		This bit:	**USBSTS bit:**	**Device Controller:**
		= 1	ULPII = 1	Issues an interrupt acknowledged by software writing a one to the ULPI interrupt bit.
9	RES	Reserved. Must be set to zero.		

Bit	Name	Description		
8	SLE	DC suspend interrupt enable; when enabled: When this bit is 1, and the bit in the register "USB Status (USBSTS)" transitions, the device controller issues an interrupt acknowledged by software DCSuspend bit.		
		This bit:	**USBSTS bit:**	**Device Controller:**
		= 1	SLI = 1	Issues an interrupt acknowledged by software writing a one to the DCSuspend bit.
7	SRE	SOF received enable; when enabled:		
		This bit:	**USBSTS bit:**	**Device Controller:**
		= 1	SRI = 1	Issues an interrupt acknowledged by software clearing the interrupt on the SOF received bit.
6	URE	USB reset enable; when enabled:		
		This bit:	**USBSTS bit:**	**Device Controller:**
		= 1	URI = 1	Issues an interrupt acknowledged by software clearing USB reset received bit.
5	AAE	Interrupt on asynchronous advance enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host Controller:**
		= 1	AAI = 1	Issues an interrupt acknowledged by software clearing the interrupt on the asynchronous advance bit.
4	SEE	System error enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host/Device Controller:**
		= 1	SEI = 1	Issues an interrupt acknowledged by software clearing the system error bit.
3	FRE	Frame list rollover enable (host controller only); when enabled:		
		This bit:	**USBSTS bit:**	**Host Controller:**
		= 1	FRI = 1	Issues an interrupt acknowledged by software clearing the frame list rollover bit.
2	PCE	Port change detect enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host/Device Controller:**
		= 1	PCE = 1	Issues an interrupt acknowledged by software clearing the port change detect bit.
1	UEE	USB error interrupt enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host/Device Controller:**
		= 1	USBERRINT = 1	Issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USB error interrupt bit.
0	UE	USB interrupt enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host/Device Controller:**
		= 1	USBINT = 1	Issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USB interrupt bit.

4.11.20 USB Frame Index (FRINDEX)

Offset: 0x1B00014C
Access: Read/Write (host mode)
Read-Only (device mode)
Reset Value: Undefined (free-running counter)

Used by the host controller to index the periodic frame list. The register updates every 125 ms (once each micro-frame). Bits [*N*:3] are used to select a particular entry in the periodic frame list during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by system software in the frame list size field in the register "USB Command (USBCMD)" on page 135. This register must be written as a DWord. Byte writes produce-undefined results. This register cannot be written unless the Host Controller is in the halted state. A write to this register while the run/stop hit is set to a one produces undefined results. Writes to this register also affect the SOF value.

In device mode this register is read only and, the device controller updates the FRINDEX [13:3] register from the frame number indicated by the SOF marker. Whenever a SOF is received by the USB bus, FRINDEX [13:3] is checked against the SOF marker. If FRINDEX [13:3] is different from the SOF marker, FRINDEX [13:3] is set to the SOF value and FRINDEX [2:0] is set to 0 (i.e., SOF for 1 ms frame). If FRINDEX [13:3] is equal to the SOF value, FRINDEX [2:0] increments (i.e., SOF for 125-µs micro-frame.)

Bit	Name	Description
31:14	RES	Reserved. Must be written to 0.
13:0	FRINDEX	Frame index The value, in this register, increments at the end of each time frame (micro-frame). Bits [*N*:3] are used for the frame list current index, thus each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. In device mode the value is the current frame number of the last frame transmitted. It is not used as an index. In either mode bits 2:0 indicate the current micro-frame. The values of *N* are based on the value of the frame list size field in the register "USB Command (USBCMD)" when used in host mode:

USBCMD	[Frame Size List] Number	Elements *N*
000	1024	12
001	512	11
010	256	10
011	128	9
100	64	8
101	32	7
110	16	6
111	8	5

4.11.21 Frame List Base Address (PERIODICLISTBASE)

Offset: 0x1B000154
Access: Read/Write (writes must be DWord)
Reset Value: 0

Bit	Name	Description
31:12	PERBASE	Contains the beginning address of the periodic frame list in the system memory. HCD loads this register prior to starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kb aligned. The contents of this register are combined with the frame index register (FRINDEX) to enable the host controller to step through the periodic frame list in sequence. (Host mode only)
11:0	RES	Reserved. Must be written to zero.

4.11.22 USB Device Address (DEVICEADDR)

Access: Read/Write
Reset Value: 0

Bit	Name	Description
31:25	USBADR	USB device address After any controller reset or a USB reset, the device address is set to the default address (0). The default address will match all incoming addresses. Software shall reprogram the address after receiving a SET_ADDRESS descriptor.
24	USBADRA	Device address advance (default=0) When written to 0, any writes to USBADR are instantaneous. When this bit is written to 1 at the same time or before USBADR (bits [31:25]) is written, the write to the USBADR field is staged and held in a hidden register. After an IN occurs on endpoint 0 and is ACKed, USBADR is loaded from the holding register. Hardware will automatically clear this bit if: ■ IN is ACKed to endpoint 0 (USBADR is updated from staging register) ■ OUT/SETUP occur to endpoint 0 (USBADR is not updated) ■ Device reset occurs (USBADR is reset to 0) Note: After the status phase of the SET_ADDRESS descriptor, the DCD has 2 ms to program the USBADR field. This mechanism ensures this specification is met when the DCD can not write of the device address within 2ms from the SET_ADDRESS status phase. If the DCD writes the USBADR with USBADRA = 1 after the SET_ADDRESS data phase (before the prime of the status phase), the USBADR is programmed instantly at the correct time and meets the 2 ms USB requirement.
23:0	RES	Reserved. Must be written to zero.

4.11.23 Next Asynchronous List Address (ASYNCLISTADDR)

Offset: 0x1B000158
Access: Read/Write (writes must be DWord)
Reset Value: 0

Bit	Name	Description
31:5	ASYBASE	Link pointer low (LPL) (Host mode only) Correspond to memory address signals [31:5], respectively.
4:0	RES	Reserved. Must be written to zero.

4.11.24 Address at Endpointlist in Memory (ENEDPOINTLIST_ADDR)

Access: Read/Write
Reset Value: 0

Bit	Name	Description
31:11	EPBASE	Endpoint list pointer (low) These bits correspond to memory address signals [31:11], respectively. This field references a list of up to 32 queue heads, i.e., one queue head per endpoint and direction. In device mode, this register contains the address of the top of the endpoint list in system memory. Bits [10:0] of this register cannot be modified by the system software and will always return a zero when read.The memory structure referenced by this physical memory pointer is assumed 64-byte.
10:0	RES	Reserved. Must be written to zero.

4.11.25 TT Status and Control (TTCTRL)

Offset: 0x1B00015C
Access: Read/Write (writes must be DWord)
Reset Value: 0

Bit	Name	Description
31	RES	Reserved. Must be written to zero.
30:24	TTHA	Internal TT hub address representation Used to match against the hub address field in queue head and SITD to determine whether the packet is routed to the internal TT for directly attached FS/LS devices. If the hub address in the queue head or SITD does not match this address, the packet is broadcast on the high speed ports destined for a downstream high speed hub with the address in the queue head or SITD. This register contains parameters needed for internal TT operations. This register is not used in the device controller operation.
23:0	RES	Reserved. Must be written to zero.

4.11.26 Programmable Burst Size (BURSTSIZE)

Offset: 0x1B000160
Access: Read/Write (writes must be DWord)
Reset Value: 0

Bit	Name	Description
31:16	RES	Reserved. Must be written to zero.
15:8	TXPBURST	Programmable Tx burst length Represents the maximum length of the burst in 32-bit words while moving data from system memory to the USB bus. The default is the constant VUSB_HS_TX_BURST.
7:0	RXPBURST	Programmable Rx burst length Represents the maximum length of the burst in 32-bit words while moving data from the USB bus to system memory. The default is the constant VUSB_HS_RX_BURST.

4.11.27 Host Tx Pre-Buffer Packet Tuning (TXFILLTUNING)

Offset: 0x1B000164
Access: Read/Write (writes must be DWord)
Reset Value: See Field Descriptions

Definitions:
Table 4-13.

T_0	Standard packet overload
T_1	Time for send data payload
T_{FF}	Time to fetch a packet into Tx FIFO up to specified level
T_S	Total packet flight time (send-only) packet = $T_0 + T_1$
T_P	Total packet time (fetch-and-send) packet = $T_{FF} + T_0 + T_1$

Controls performance tuning associated with how the host controller posts data to the Tx latency FIFO before moving the data to the USB bus. The specific areas of performance include how much data to post into the FIFO and an estimate of how long the operation will take in the target system.

On discovery of a Tx packet (OUT/SETUP) in the data structures, the host controller checks whether T_P remains before the end of the (micro-)frame. If so, it pre-fills the Tx FIFO. If during the pre-fill operation the time remaining in the (micro-)frame is < T_S, the packet attempt ceases and the packet is tried at a later time. This condition is not an error and the host controller eventually recovers, but a note of a "back-off" occurrence is made on the scheduler health counter. When a back-off event is detected, the partial packet fetched may need to be discarded from the latency buffer to make room for periodic traffic that begins after the next SOF. Excessive back-off events can waste bandwidth and power on the system bus and thus should be minimized. Back-offs can be minimized with use of the TSCHHEALTH (T_{FF}).

Bit	Name	Description
31:22	RES	Reserved. Must be written to zero.
21:16	TXFIFOTHRES	FIFO burst threshold (Default = 0x2) Controls the number of data bursts posted to the Tx latency FIFO in host mode before the packet begins on to the bus. The minimum value is 2; this value should be a low as possible to maximize USB performance. A higher value can be used in systems with unpredictable latency and/or insufficient bandwidth where the FIFO may underrun because the data transferred from the latency FIFO to USB occurs before it can be replenished from system memory.
15:13	RES	Reserved. Must be written to zero.
12:8	TXSCHEALTH	Scheduler health counter (Default = 0x0) Increments when the host controller fails to fill the Tx latency FIFO to the level programmed by TXFIFOTHRES before running out of time to send the packet before the next SOF. This health counter measures how many times this occurs to aid in selecting a proper TXSCHOH. Writing to this register clears the counter and this counter maxes out at 31.
7	RES	Reserved. Must be written to zero.
6:0	TXSCHOH	Scheduler overload (Default = 0x0) This register adds an additional fixed offset to the schedule time estimator described above as T_{FF}. As an approximation, the value chosen for this register should limit the number of back-off events captured in the TXSCHHEALTH to less than 10 per second in a highly utilized bus. Choosing a value that is too high for this register is not desired as it can needlessly reduce USB utilization.

4.11.28 Endpoint NAK (ENDPTNAK)

Offset: 0x1B000178
Access: Read/Write-to-Clear
Reset Value: 0

Bit	Name	Description	
31:16	EPTN	Tx endpoint NAK Each Tx endpoint has 1 bit in this field. The bit is set when the device sends a NAK handshake on a received IN token for the corresponding endpoint.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0
15:0	EPRN	Rx endpoint NAK Each Rx endpoint has 1 bit in this field. The bit is set when the device sends a NAK handshake on a received OUT or PING token for the corresponding endpoint.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0

4.11.29 Endpoint NAK Enable (ENDPTNAKEN)

Offset: 0x1B00017C
Access: Read/Write
Reset Value: 0

Bit	Name	Description	
31:16	EPTNE	Tx endpoint NAK enable Each bit is an enable bit for the corresponding Tx endpoint NAK bit. If this bit is set and the corresponding Tx endpoint NAK bit is set, the NAK interrupt bit is set.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0
15:0	EPRNE	Rx endpoint NAK enable Each bit is an enable bit for the corresponding Rx endpoint NAK bit. If this bit is set and the corresponding Rx endpoint NAK bit is set, the NAK interrupt bit is set.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0

4.11.30 Port/Status Control (PORTSC0)

Offset: 0x1B000184
Access: See Field Descriptions
Reset Value: See Field Descriptions

Host Controller

A host controller must implement one to eight port registers; the number is implemented by a instantiation of a host controller (see the register "Host Control Structural Parameters (HCSPARAMS)" on page 133). Software uses this information as an input parameter to determine how many ports need service. This register is only reset when power is initially applied or in response to a controller reset. The initial conditions of a port are:

- No device connected
- Port disabled

If the port has port power control, this state remains until software applies power to the port by setting port power to one.

Device Controller

A device controller must implement only port register one and does not support power control. Port control in device mode is only used for status port reset, suspend, and current connect status. It also initiates test mode or forces signaling and allows software to place the PHY into low power suspend mode and disable the PHY clock.

Bit	Name	Access	Description
31:30	PTS	RW/RO	Parallel transceiver select This register bit pair is used in conjunction with the configuration constant VUSB_HS_PHY_TYPE to control which parallel transceiver interface is selected. ■ If VUSB_HS_PHY_TYPE is set for 0–3 then this bit is read only ■ If VUSB_HS_PHY_TYPE is set for 4–7, this bit is read/write This field resets to: 00 — UTMI/UTMI — If VUSB_HS_PHY_TYPE = 0, 4 01 — RES — Reserved 10 — ULPI — If VUSB_HS_PHY_TYPE = 2, 6 11 — Serial/1.1 PHY (FS Only) — If VUSB_HS_PHY_TYPE = 3, 7
29	RES	RO	Reserved
28	PTW	RW/RO	Parallel transceiver width Used in conjunction with the configuration constant VUSB_HS_PHY16_8 to control the data bus width of the UTMI transceiver interface. ■ If VUSB_HS_PHY16_8 is set for 0 or 1, this bit is read only ■ If VUSB_HS_PHY16_8 is 2 or 3, this bit is read/write This bit resets to 1 if VUSB_HS_PHY16_8 selects a default UTMI interface width of 16-bits else it is reset to 0. This bit has no effect if the serial interface is selected. 0 — Writing this bit to 0 selects the 8-bit [60MHz] UTMI interface 1 — Writing this bit to 1 selects the 16-bit [30MHz] UTMI interface
27:26	PSPD	RO	Port speed Indicates the speed at which the port is operating. For HS mode operation in the host controller and HS/FS operation in the device controller the port routing steers data to the protocol engine. For FS and LS mode operation in the host controller, the port routing steers data to the Protocol Engine with the embedded transaction translator. 00 — Full Speed 01 — Low Speed 10 — High Speed 11 — Not used
25	RES	RO	Reserved. Must be set to zero.

Bit	Name	Access	Description
24	PFSC	RW	Port force full speed connect; Default = 0 (debug mode only) Setting this bit to 1 forces the port to only connect at Full Speed and disables the chirp sequence, allowing the port to identify itself as High Speed (useful for testing FS configurations with a HS host, hub or device).
23	PHCD	RW	PHY low power suspend: clock disable (PLPSCD)
			0 — Disables the PHY clock (Default)
			1 — Enables the PHY clock
			Reading this bit indicates the status of the PHY clock. NOTE: The PHY clock cannot be disabled if it is being used as the system clock.
			Device Mode — The PHY can be put into Low Power Suspend – Clock Disable when the device is not running (USBCMD Run/Stop = 0) or the host has signaled suspend (PORTSC SUSPEND = 1). Low power suspend clears automatically when the host has signaled resume if using a circuit similar to that in 10. Before forcing a resume from the device, the device controller driver must clear this bit.
			Host Mode — The PHY can be put into Low Power Suspend – Clock Disable when the downstream device has been put into suspend mode or when no downstream device is connected. Low power suspend is completely under the control of software.
22	WKOC	RW	Wake on over-current enable (WKOC_E) (Host mode only)
			0 — This field is zero if Port Power (PP) is zero (Default)
			1 — Sensitizes the port to over-current conditions as wake-up events
21	WKDS	RW	Wake on Disconnect Enable (WKDSCNNT_E) (Host mode only)
			0 — This field is zero if Port Power (PP) is zero or in device mode (Default)
			1 — Sensitizes the port to device disconnects as wake-up events
20	WKCN	RW	Wake on connect enable (WKCNNT_E) (Host mode only)
			0 — This field is zero if Port Power (PP) is zero or in device mode (Default)
			1 — Sensitizes the port to device connects as wake-up events
19:16	PTC[3:0]	RW	Port test control The FORCE_ENABLE_FS and FORCE ENABLE_LS are extensions to the test mode support. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values forces the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. Note: Low speed operations are not supported as a peripheral device. Any other value than zero indicates that the port is operating in test mode.
			Value — **Specific Test**
			0000 — TEST_MODE_DISABLE (Default)
			0001 — J_ STATE
			0010 — K_STATE
			0011 — SE0 (host) / NAK (device)
			0100 — Packet
			0101 — FORCE_ENABLE_HS
			0110 — FORCE_ENABLE_FS
			0111 — FORCE_ENABLE_LS
			1111:1000 — Reserved

<table>
<tr><th>Bit</th><th>Name</th><th>Access</th><th>Description</th></tr>
<tr><td>15:14</td><td>PIC</td><td>RW</td><td>Port indicator control
Writes to this field have no effect if the P_INDICATOR bit in the HCSPARAMS register is a zero. If P_INDICATOR bit is a one, then the bit is:
Value | Specific Test
00 | Port indicators off (Default)
01 | Amber
10 | Green
11 | Undefined</td></tr>
<tr><td>13</td><td>PO</td><td>RO</td><td>Port owner; default = 0
Port owner hand-off is not implemented in this design, therefore this bit always reads back as 0. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device.</td></tr>
<tr><td>12</td><td>RES</td><td>RW</td><td>Reserved</td></tr>
<tr><td>11:10</td><td>LS</td><td>RO</td><td>Line status; bit encoding is:
Setting | Meaning
00 | SE0
01 | J_ STATE
10 | K_STATE
11 | Undefined
These bits reflect the current logical levels of the D+ (bit [11]) and D– (bit [10]) signal lines.
Device Mode | In device mode, the use of line-state by the device controller driver is not necessary.
Host Mode | In host mode, the use of line-state by the host controller driver is not necessary (unlike EHCI), because the port controller state machine and the port routing manage the connection of LS and FS.</td></tr>
<tr><td>9</td><td>HSP</td><td>RO</td><td>High-speed port; see also bits [27:26], PSPD
0 | Connected host/device is not in a high-speed mode (Default)
1 | The host/device connected to the port is in high-speed mode</td></tr>
<tr><td>8</td><td>PR</td><td>RW/ RO</td><td>Port reset
■ This field is zero if Port power (PP) is zero
■ When software writes a one to this bit, the bus-reset sequence as defined in USB2.0 is started. This bit automatically changes to zero after reset.
Device Mode: Read-Only
Device reset from the USB bus is also indicated in the register “USB Status (USBSTS)” on page 137.
Host Mode: Read/Write
0 | Port is not in reset (Default)
1 | Port is in reset</td></tr>
</table>

Bit	Name	Access	Description	
7	SUSP	RW/ RO	Suspend Port Enabled Bit and Suspend bit of this register define the port states:	
			Bits	**Port State**
			0*x*	Disable
			10	Enable
			11	Suspend
			This field is zero if Port Power (PP) is zero in host mode.	
			Device Mode	Read-Only ■ 0=Port not in suspend state (Default) ■ 1=Port in suspend state
			Host Mode	Read/Write ■ 0=Port not in suspend state (Default) ■ 1=Port in suspend state In suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. The host controller unconditionally sets this bit to zero when software sets the force port resume bit to zero. The host controller ignores a write of zero to this bit. If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined.
6	FPR	RW	Force port resume	
			0	No resume (K-state) detected/driven on port (Default)
			1	Resume detected/driven on port
			This field is zero if Port Power (PP) is zero in host mode.	
			Device Mode	After the device has been in suspend state for 5 ms or more, software must set this bit to 1 to drive resume signaling before clearing. The device controller sets this bit to one if a J-to-K transition is detected while the port is in the suspend state. The bit will be cleared when the device returns to normal operation. Also, when this bit transitions to a one because a J-to-K transition detected, the port change detect bit in the register"USB Status (USBSTS)" is also set to one.
			Host Mode	Software sets this bit to one to drive resume signaling. The host controller sets this bit to one if a J-to-K transition is detected while the port is in the suspend state. When this bit transitions to a one because a J-to-K transition is detected, the port change detect bit in the register "USB Status (USBSTS)" is also set to one. This bit automatically changes to zero after the resume sequence is complete. This behavior is different from EHCI where the host controller driver is required to set this bit to a zero after the resume duration is timed in the driver.
5	OCC	RWC	Over-current change. For device-only implementations this bit shall always be 0.	
			0	(Default)
			1	This bit is set to 1 when there is a change to over-current active. Software clears this bit by writing a one to this bit position.
4	OCA	RO	Over-current active. For device-only implementations this bit shall always be 0.	
			0	This port does not have an over-current condition. This bit automatically transitions from one to zero when the over-current condition is removed. (Default)
			1	This port currently has an over-current condition

Bit	Name	Access	Description	
3	PEC	RWC	Port enable/disable change	
			0	No change (Default)
			1	Port enabled/disabled status has changed
			This field is zero if Port Power (PP) is zero.	
			Device Mode	The device port is always enabled (this bit will be zero)
			Host Mode	For the root hub, this bit gets set to a one only when a port is disabled due to disconnect on the port or due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification). Software clears this by writing a one to it.
2	PE	RW	Port enabled/disabled	
			0	Disabled (Default)
			1	Enabled
			This field is zero if Port Power (PP) is zero in host mode.	
			Device Mode	The device port is always enabled (this bit will be one)
			Host Mode	Ports can only be enabled by the host controller as a part of reset and enable. Software cannot enable a port by writing a one to this field. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by the host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, (0b) downstream propagation of data is blocked except for reset.
1	CSC	RWC	Connect status change	
			0	No change (Default)
			1	Change in current connect status. Software clears this bit by writing a 1 to it.
			This field is zero if Port Power (PP) is zero in host mode.	
			Device Mode	This bit is undefined in device controller mode.
			Host Mode	Indicates a change has occurred in the port's Current Connect Status. The host/device controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set).
0	CCS	RO	Current connect status	
			Device Mode	■ 0 = Not attached (Default) A zero indicates that the device did not attach successfully or was forcibly disconnected by the software writing a zero to the Run bit in the register "USB Command (USBCMD)" on page 135. It does not state the device being disconnected or suspended. ■ 1 = Attached A 1 indicates that the device successfully attached and is operating in either high speed or full speed as indicated by the high speed port bit in this register.
			Host Mode	This value reflects the current state of the port, and may not correspond directly to the event that caused the connect status change bit to be set. ■ 0 = No device is present. (Default) ■ 1 = Device is present on port. This field is zero if Port Power (PP) is zero in host mode.

4.11.31 USB Mode (USBMODE)

Offset: 0x1B0001A8
Access: Read/Write
Reset Value: 0

Bit	Name	Description	
31:5	RES	Reserved. Must be written to zero.	
4	SDIS	Stream disable mode ■ 0 = Inactive (Default) ■ 1 = Active	
		Device Mode	Setting to a 1 disables double priming on both Rx and Tx for low bandwidth systems. This mode, when enabled, ensures that the Rx and Tx buffers are sufficient to contain an entire packet, so the usual double buffering scheme is disabled to prevent overruns/underruns in bandwidth limited systems.
		Host Mode	Setting to a 1 ensures that overruns/underruns of the latency FIFO are eliminated for low bandwidth systems where the Rx and Tx buffers are sufficient to contain the entire packet. Enabling stream disable also has the effect of ensuring the Tx latency is filled to capacity before the packet is launched onto the USB.
3	SLOM	Setup lockout mode In device mode, this bit controls behavior of the setup lock mechanism.	
		0	Setup lockouts on (Default)
		1	Setup lockouts off
2	ES	Endian select Can change the byte ordering of transfer buffers to match the host microprocessor bus architecture. The bit fields in the microprocessor interface and the DMA data structures (including the setup buffer within the device QH) are unaffected by the value of this bit, because they are based upon 32-bit words.	
		Bit	**Meaning**
		0	Little Endian (Default) First byte referenced in least significant byte of 32-bit word
		1	Big Endian First byte referenced in most significant byte of 32-bit word
1:0	CM	Controller mode Controller mode is defaulted to the proper mode for host only and device only implementations. For those designs that contain both host and device capability, the controller will default to an idle state and will need to be initialized to the desired operating mode after reset. For combination host/device controllers, this register can only be written once after reset. If it is necessary to switch modes, software must reset the controller by writing to the RESET bit in the register "USB Command (USBCMD)" on page 135 before reprogramming this register.	
		Bit	**Meaning**
		00	Idle (Default for combination host/device)
		01	Reserved
		10	Device Controller (Default for device-only controller)
		11	Host Controller (Default for host-only controller)

4.11.32 Endpoint Setup Status (ENDPTSETUPSTAT)

Offset: 0x1B0001AC
Access: Read/Write-One-to-Clear
Reset Value: 0x00000000

Bit	Name	Description
31:16	RES	Reserved
15:0	ENDPTSETUPSTAT	Setup endpoint status (Device mode only) For every setup transaction received, a corresponding bit in this register is set to 1. Software must clear or acknowledge the setup transfer by writing a one to a respective bit after it has read the setup data from Queue head. The response to a setup packet as in the order of operations and total response time is crucial to limit bus time outs while the setup lock our mechanism is engaged.

4.11.33 Endpoint Initialization (ENDPTPRIME)

Offset: 0x1B0001B0
Access: Read/Write-One-to-Clear
Reset Value: 0x00000000

Bit	Name	Description	
31:16	PETB	Prime endpoint Tx buffer (Device mode only) For each endpoint a corresponding bit is used to request that a buffer prepared for a Tx operation in order to respond to a USB IN/INTERRUPT transaction. Software should write a 1 to the corresponding bit when posting a new transfer descriptor to an endpoint. Hardware automatically uses this bit to begin parsing for a new transfer descriptor from the queue head and prepare a Tx buffer. Hardware clears this bit when the associated endpoint(s) are successfully primed.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0
15:0	PERB	Prime endpoint Rx buffer For each endpoint a corresponding bit is used to request that a buffer prepared for a Rx operation in order to respond to a USB IN/INTERRUPT transaction. Software should write a 1 to the corresponding bit when posting a new transfer descriptor to an endpoint. Hardware automatically uses this bit to begin parsing for a new transfer descriptor from the queue head and prepare a Rx buffer. Hardware clears this bit when the associated endpoint(s) are successfully primed.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0

4.11.34 Endpoint De-Initialization (ENDPTFLUSH)

Offset: 0x1B0001B4
Access: Writing a 1 to a bit in this register causes the associated endpoint(s) to clear any primed buffers.
Reset Value: 0

This register is for device mode only.

Bit	Name	Description	
31:16	FETB	Flush endpoint Tx buffer If a packet is in progress for one of the associated endpoints, that transfer continues until completion. Hardware clears this register after the endpoint flush operation.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0
15:0	FERB	Flush endpoint Rx buffer If a packet is in progress for one of the associated endpoints, that transfer continues until completion. Hardware clears this register after the endpoint flush operation.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0

4.11.35 Endpoint Status (ENDPTSTATUS)

Offset: 0x1B0001B8
Access: Read-Only
Reset Value: 0

This register is for device mode only.

Bit	Name	Description	
31:16	ETBR	Endpoint Tx buffer ready One bit for each endpoint indicates status of the respective endpoint buffer. This bit is set to a 1 by the hardware as a response to a command from a corresponding bit in the register "Endpoint Initialization (ENDPTPRIME)" on page 152. A delay always occurs between setting a bit in the ENDPTPRIME register and endpoint indicating ready. This delay time varies based upon the current USB traffic and the number of bits set in the ENDPTPRIME register. Buffer ready is cleared by USB reset, by the USB DMA system, or through the ENDPTFLUSH register.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0
15:0	ERBR	Endpoint Rx buffer ready One bit for each endpoint indicates status of the respective endpoint buffer. This bit is set to a 1 by the hardware as a response to a command from a corresponding bit in the register "Endpoint Initialization (ENDPTPRIME)". A delay always occurs between setting a bit in the ENDPTPRIME register and endpoint indicating ready. This delay time varies based upon the current USB traffic and the number of bits set in the ENDPTPRIME register. Buffer ready is cleared by USB reset, by the USB DMA system, or through the ENDPTFLUSH register.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0

4.11.36 Endpoint Complete (ENDPTCOMPLETE)

Offset: 0x1B0001BC
Access: Read/Write-One-to-Clear
Reset Value: 0

This register is for device mode only.

Bit	Name	Description	
31:16	ETCE	Endpoint Tx complete event Indicates a Tx event (IN/INTERRUPT) occurred and software should read the corresponding endpoint queue to determine the endpoint status. If the corresponding IOC bit is set in the transfer descriptor, this bit is set simultaneously with the register USBINTR.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0
15:0	ERCE	Endpoint Rx complete event Indicates a Rx event (IN/INTERRUPT) occurred and software should read the corresponding endpoint queue to determine the endpoint status. If the corresponding IOC bit is set in the transfer descriptor, this bit is set simultaneously with the register USBINTR.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0

4.11.37 Endpoint Control 0 (ENDPTCTRL0)

Offset: 0x1B0001C0
Access: Read/Write
Reset Value: 0x0080008

Every device implements Endpoint0 as a control endpoint.

Bit	Name	Description	
31:24	RES	Reserved. Must be written to zero.	
23	TXE	Tx endpoint enable. Endpoint 0 is always enabled; this bit is always 1.	
22:20	RES	Reserved. Must be written to zero.	
19:18	TXT	Tx endpoint type (0 = Control). Endpoint 0 is always 0; this bit is always 0.	
17	RES	Reserved. Must be written to zero.	
16	TXS	Tx endpoint stall	
		0	Endpoint OK (Default)
		1	Endpoint stalled
15:8	RES	Reserved. Must be written to zero.	
7	RXE	Rx endpoint enable. Endpoint 0 is always enabled; this bit is always 1.	
6:4	RES	Reserved. Must be written to zero.	
3:2	RXT	Rx endpoint type (0 = Control). Endpoint 0 is fixed as a control endpoint; this bit is always 0	
1	RES	Reserved. Must be written to zero.	
0	RXS	Rx endpoint stall	
		0	Endpoint OK (Default)
		1	Endpoint stalled

4.11.38 Endpoint Control 1 (ENDPTCTRL1)

Offset: 0x1B0001C4 (Endpoint Control 1)
0x1B0001C8 (Endpoint Control 2)
0x1B0001CC (Endpoint Control 3)
0x1B0001D0 (Endpoint Control 4)
0x1B0001D4 (Endpoint Control 5)

Access: Read/Write
Reset Value: 0

Bit	Name	Description	
31:24	RES	Reserved. Must be written to zero.	
23	TXE	Tx endpoint enable An Endpoint should be enabled only after it has been configured	
22	TXR	Tx data toggle reset When a configuration event is received for this Endpoint, software must write a 1 to this bit in order to synchronize the data PIDs between the host and device.	
21	TXI	Tx data toggle inhibit	
		0	PID sequencing enabled (Default)
		1	PID sequencing disabled
20	RES	Reserved. Must be written to zero.	
19:18	TXT	Tx endpoint type	
		00	Control
		01	Isochronous
		10	Bulk
		11	Interrupt
17	TXD	Tx endpoint data source; should always be written to zero	
16	TXS	Tx endpoint stall	
		0	Endpoint OK (Default)
		1	Endpoint stalled
15:8	RES	Reserved. Must be written to zero.	
7	RXE	Rx endpoint enable An Endpoint should be enabled only after it has been configured	
6	RXR	Rx data toggle reset When a configuration event is received for this Endpoint, software must write a 1 to this bit in order to synchronize the data PIDs between the host and device.	
5	RXI	Rx data toggle inhibit	
		0	PID sequencing enabled (Default)
		1	PID sequencing disabled
4:3	RES	Reserved. Must be written to zero.	
2	RXT	Rx endpoint type	
		00	Control
		01	Isochronous
		10	Bulk
		11	Interrupt
1	RXD	Rx endpoint data source; should always be written to zero	
0	RXS	Rx endpoint stall	
		0	Endpoint OK (Default)
		1	Endpoint stalled

4.12 Serial Flash Registers

Table 4-14 shows the serial flash registers for the AR7242.

Table 4-14. **Serial Flash Registers**

Offset	Name	Description	Page
0x1F000000	SPI_FUNCTION_SELECT	SPI Function Select Register	page 156
0x1F000004	SPI_CONTROL	SPI Control Register	page 156
0x1F000008	SPI_IO_CONTROL	SPI IO Control	page 157
0x1F00000C	SPI_READ_DATA	SPI Read Data	page 157

4.12.1 SPI Function Select (SPI_FUNC_SELECT)

Address: 0x1F000000
Access: Read/Write
Reset: 0x0

This register is used to enable or disable the SPI.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	FUNCTION_ SELECT	Setting this bit to 0 enables SPI. Setting this bit to 1 makes the rest of the registers visible

4.12.2 SPI Control (SPI_CONTROL)

Address: 0x1F000004
Access: Read/Write
Reset: See field description

This register is used to set the functions for the SPI control, and can be written only if the FUNCTION_SELECT bit is set to 1.

Bit	Bit Name	Reset	Description
31:7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
6	REMAP_ DISABLE	0x0	Remaps 4 MB space over unless explicitly disabled by setting this bit to 1. If set to 1, 16 MB is accessible.
5:0	CLOCK_ DIVIDER	0x8	Specifies the clock divider setting. Actual clock frequency would be (AHB_CLK/((CLOCK_DIVIDER+1) * 2)). Therefore by default, if the AHB_CLK is 200 MHz, this would give 200/18 = ~11 MHz.

4.12.3 SPI I/O Control (SPI_IO_CONTROL)

Address: 0x1F000008
Access: Read/Write
Reset: 0x0

This register is used to configure the in/out bits for the SPI.

Bit	Bit Name	Description
31:19	RES	Reserved. Must be written with zero. Contains zeros when read.
18	IO_CS_2	The chip select 2 bit to be output
17	IO_CS_1	The chip select 1 bit to be output
16	IO_CS_0	The chip select 0 bit to be output
8	IO_CLOCK	The clock bit to be output
7:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	IO_DO	The data bit to be output

4.12.4 SPI Read Data (SPI_READ_DATA)

Address: 0x1F00000C
Access: Read-Only
Reset: 0x0

This register is used to return the data read from the flash device with bits sampled after every clock.

Bit	Bit Name	Type	Reset	Description
31:0	READ_DATA	RO	0x0	The read data sampled in every clock

4.13 Ethernet MAC/PHY Port Registers

This section describes the internal registers of the Ethernet port. Table 4-15 summarizes the Ethernet MAC/PHY port registers for the AR7242.

Table 4-15. **Ethernet Port Registers Summary**

Address	Description	Page
0x0000–0x0098	Global Control Registers	page 159
0x0100–0x0120	Port0 Control Registers	page 170
0x0200–0x0220	Port1 Control Registers	page 170
0x20000–0x200A4	Port0 Statistics Counters	page 178
0x20100–0x201A4	Port1 Statistics Counters	page 178

These registers are accessed by the CPU through the GE0 "MII Address" and "MII Control" registers. GE0 has a MDIO master, while the Ethernet MAC/PHY port has a MDIO slave.

The MDC/MDIO interface allows users to access the Ethernet MAC/PHY port internal registers and the MII registers. The format required to access the MII registers in the embedded PHY for a PHY_ADDR from 0x00 to 0x04 is:

start	OP	2'b0	Phy_Addr [2:0]	Reg_Addr [4:0]	TA [1:0]	Data [15:0]

The Op code "10" indicates the read command and "01" is the write command.

The Ethernet MAC/PHY port internal registers are 32-bits wide, but the MDIO access is only 16-bits wide, so two access cycles are required to access all 32 bits of the internal registers. Moreover, address spacing is more than the 10 bits supported by MDIO, so the upper address bits must be written to internal registers, similar to the page mode access method.

For example, the register address bits [18:9] are treated as a page address and are written out first as High_Addr[9:0]:

start	OP	2'b11	8'b0	6'b0	High_Addr [9:0]

Then the register would be accessed via:

start	OP	2'b10	Low_Addr [7:0]	TA [1:0]	Data [15:0]

Where:

- Low_Addr[7:1] is the address bit [8:2] of the register AND Low_Addr[0] is 0 for Data[15:0]

or

- Low_Addr[0] is 1 for Data[31:16]

4.13.1 Global Control Registers

Table 4-16 summarizes the global control registers for the AR7242.

Table 4-16. **Global Control Registers Summary**

Offset	Register	Page
0x0000	Global Mask Control	page 159
0x0010	Global Interrupt	page 160
0x0014	Global Interrupt Mask	page 161
0x0020	Global MAC Address 0	page 162
0x0024	Global MAC Address 1	page 161
0x002C	Flood Mask	page 162
0x0030	Global Control	page 163
0x0040	VLAN Table Function 0	page 163
0x0044	VLAN Table Function 1	page 164
0x0050	Address Table Function 0	page 164
0x0054	Address Table Function 1	page 165
0x0058	Address Table Function 2	page 165
0x005C	Address Table Control	page 166
0x0060	IP Priority Mapping 0	page 166
0x0064	IP Priority Mapping 1	page 167
0x0068	IP Priority Mapping 2	page 167
0x006C	IP Priority Mapping 3	page 168
0x0070	Tag Priority Mapping	page 168
0x0074	Service Tag	page 169
0x0080	MIB Function0	page 169
0x0098	MDIO Control	page 170

4.13.1.1 Global Mask Control

This register is used for soft resets.

Address: 0x0000
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31	SOFT_RET	WO	0x0	Software reset. This bit is set by software to initialize the hardware, and should be self-cleared by hardware after the initialization is done.
30:0	RES	RO	0x0	Reserved.

4.13.1.2 Global Interrupt

Address: 0x0010
Access: Read/Write
Reset: 0x0

This register provides the status of various interrupts based global parameters. Interrupts are only generated when the corresponding bits of the following "Global Interrupt Mask" are set.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17	LOOKUP_ERR_INT	Generates an interrupt when there is an error detected during a lookup
16	QM_ERR_INT	This bit generates an interrupt when the QM detects an error
15	RES	Reserved. Must be written with zero. Contains zeros when read.
14	HARDWARE_ INI_DONE	This bit generates an interrupt when the hardware memory initialization has completed
13	MIB_INI_INT	This bit generates an interrupt when the MIB memory initialization has completed
12	MIB_DONE_ INT	This bit generates an interrupt when the CPU has completed accessing the MIB
11	RES	Reserved
10	VT_MISS_VIO_ INT	This bit generates an interrupt when a VID is not located in the VLAN table
9	VT_MEM_VIO_INT	This bit generates an interrupt when a VID is located in the VLAN table, yet the source port is not a member of the VID
8	VT_DONE_INT	This bit generates an interrupt after completing an access to the VLAN table by the CPU
7	QM_INI_INT	Generates an interrupt after the QM memory initialization is completed
6	AT_INI_INT	Generates an interrupt when the address table initialization has completed
5	ARL_FULL_INT	This bit generates an interrupt when there is an address attempting to be added to the address resolution table, yet the table is full
4	ARL_DONE_ INT	This bit generates and interrupt when the address resolution table was accessed and the process has completed
3	MDIO_DONE_ INT	Generates an interrupt when the MDIO access MAC/PHY register is done
2	PHY_INT	Generates an interrupt originating from the physical layer
1:0	RES	Reserved

4.13.1.3 Global Interrupt Mask

Address: 0x0014
Access: Read/Write
Reset: See field description

This register controls various interrupts based global parameters. Interrupts are only generated when the bits of this register are set.

Bit	Bit Name	Reset	Description
31:18	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
17	LOOKUP_ERR_INT_ EN	0x0	Enables an interrupt when there is an error detected during a lookup
16	QM_ERR_INT_EN	0x0	Enables an interrupt when the QM detects an error
15	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
14	HARDWARE_ INI_DONE_EN	0x0	Enables an interrupt when the hardware memory initialization has completed
13	MIB_INI_INT_ EN	0x0	Enables an interrupt when the MIB memory initialization has completed
12	MIB_DONE_ INT_EN	0x0	Enables an interrupt when the CPU is finished accessing the MIB
11	RES	0x0	Reserved
10	VT_MISS_VIO_ INT_EN	0x0	Enables an interrupt when a VID is not located in the VLAN table
9	VT_MEM_VIO_INT_ EN	0x0	Enables an interrupt when a VID is located in the VLAN table, yet the source port is not a member of the VID
8	VT_DONE_INT_EN	0x0	Enables an interrupt after completing an access to the VLAN table by the CPU
7	QM_INI_INT_ EN	0x0	Enables an interrupt after the QM memory initialization has been completed
6	AT_INI_INT_ EN	0x0	Enables an interrupt when the address table initialization has completed
5	ARL_FULL_INT_EN	0x0	Enables an interrupt when there is an address attempting to be added to the address resolution table, yet the table is full
4	ARL_DONE_ INT_EN	0x0	Enables interrupt when the address resolution table was accessed and the process has completed
3	MDIO_DONE_ INT_EN	0x0	Enables an interrupt when the MDIO access MAC/PHY register is done
2	PHY_INT_EN	0x0	Enables an interrupt originating from the physical layer
1:0	RES	0x0	Reserved

4.13.1.4 Global MAC Address 1

Address: 0x0020
Access: Read/Write
Reset: See field description

This register, along with the preceding "Global MAC Address 2", are used to identify the station address of the Ethernet port.

Bit	Bit Name	Reset	Description
31:16	RES	0x0	Reserved
15:8	MAC_ADDR_ BYTE4	0x0	These bits represent the station address of the MAC/PHY which is used as a source address in pause frames or other management frames
7:0	MAC_ADDR_ BYTE5	0x01	

4.13.1.5 Global MAC Address 2

Address: 0x0024
Access: Read/Write
Reset: 0x0

This register, along with the following "Global MAC Address 1", are used to identify the station address of the MAC/PHY.

Bit	Bit Name	Description
31:24	MAC_ADDR_ BYTE0	These bits represent the station address of the MAC/PHY, which is used as a source address in pause frames or other management frames
23:16	MAC_ADDR_ BYTE1	
15:8	MAC_ADDR_ BYTE2	
7:0	MAC_ADDR_ BYTE3	

4.13.1.6 Flood Mask

Address: 0x002C
Access: Read/Write
Reset: See field description

This register is used to allocate broadcast, multicast and unicast frames.

Bit	Bit Name	Reset		Description
31:27	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
26	BROAD_TO_ CPU_EN	0x0	0	Broadcast frames cannot be transmitted to the CPU port
			1	Broadcast frames can be transmitted to the CPU port
25	ARL_MULTI_ LEAKY_EN	0x0	0	Ignores the LEAKY_EN bit in the ARL table to control multicast frame leaky VLANs. Uses only port-base MULTI_LEAKY_EN to control the frame leaky VLAN.
			1	Uses the LEAKY_EN bit in the ARL table to control multicast frame leaky VLANs and ignore the MULTI_LEAKY_EN
24	ARL_UNI_ LEAKY_EN	0x0	0	Ignores the LEAKY_EN bit in the ARL table to control unicast frame leaky VLAN. Uses only port-base UNI_LEAKY_EN to control the unicast frame leaky VLAN.
			1	Uses the LEAKY_EN bit in the ARL table to control unicast frame leaky VLANs and ignore the UNI_LEAKY_EN
23:18	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
17:16	MULTI_FLOOD _DP	0x3	These bits are used to find a destination port for a unknown multicast frame received by the MAC, within which the destination address is not contained in the address resolution table (ARL)	
15:5	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
1:0	UNI_FLOOD_ DP	0x3	These bits are used to find a destination port for a unknown unicast frame received by the MAC, within which the destination address is not contained in the address resolution table (ARL)	

4.13.1.7 Global Control

Address: 0x0030
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31	WEIGHT_ PRIORITY	0x0	0	Use strict priority for egress
			1	If MIX_WEIGHT_PRIORITY = 0, use an 8, 4, 2, 1 weighted fair queueing scheme, otherwise use mix mode
30:29	RES	0x3	Reserved	
28	MIX_WEIGHT _PRIORITY	0x0	0	Use the 8, 4, 2, 1 weighted fair queueing scheme when the WEIGHT_PRIORITY bit is set to 1
			1	Strict priority and weight priority mix mode. The highest priority uses strict priority, other priorities use a 4, 2, 1 weighted fair queueing scheme when the WEIGHT_PRIORITY bit is set as 1.
27:24	RES	0xF	Reserved	
26:14	RES	0x0	Reserved	
13:0	MAX_FRAME _SIZE	0x5EE	Max frame size can be received and transmitted by the MAC. The MAC drops any packet sized larger than MAX_FRAME_SIZE. The value is for normal packets; the MAC adds 4 if it supports VLAN, it adds 8 for double VLAN, and adds 2 for some headers.	

4.13.1.8 VLAN Table Function 0

Address: 0x0040
Access: Read/Write
Reset: 0x0

This register is used to set the various functions of the VLAN table, such as priority and ports.

Bit	Bit Name	Description	
31	VT_PRI_EN	Represents the priority of a VLAN in the VLAN table. VTU [3]	
30:28	VT_PRI	Represents the priority of a VLAN in the VLAN table. VTU [2:0]	
27:16	VID	Represents the value of the VLAN ID (VID) to be added or purged	
15:12	RES	Reserved. Must be written with zero. Contains zeros when read.	
11:5	RES	Reserved	
4	VT_FULL_VIO	This bit is set when there is a violation of the VLAN table. Set to 1 if the VLAN table is full when the CPU wishes to add a new VID to the VLAN table	
3	VT_BUSY	The VLAN table is busy. This bit must be set to 1 to start a VLAN table operation and cleared to zero after the operation has completed. If this bit is set to 1, the CPU cannot request another operation.	
2:0	VT_FUNC	The VLAN table operating functions	
		000	No operation
		001	Flush all entries in the VLAN table
		010	The CPU wants to load an entry into other VLAN table
		011	Used to purge an entry from the VLAN table
		100	Reserved
		101	Used to get the next entry in the VLAN table
		If the VID is 0 and VT_BUSY is set by the software, the hardware should search for the first valid entry in the VLAN table. If the VID is 0 and the VT_BUSY is reset by the hardware, there is no valid entry from the VID set by the software.	

4.13.1.9 VLAN Table Function 1

Address: 0x0044
Access: Read/Write
Reset: 0x0

This register is used to identify VLAN entries in the VID table.

Bit	Bit Name	Type	Reset	Description
31:12	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
11	VT_VALID	RW	0x0	Represents a valid entry in the VLAN table. VTU [15]
10	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:0	VID_MEM	RW	0x0	Represents a VID member in the VLAN table. VTU [25:16]

4.13.1.10 Address Table Function 0

Address: 0x0050
Access: Read/Write
Reset: 0x0

This register is used to configure functions of the address resolution (ARL) table.

Bit	Bit Name	Description	
31:24	AT_ADDR_ BYTES4	The fifth byte of the address	
23:16	AT_ADDR_ BYTES5	The last byte of the address	
15:13	RES	Reserved. Must be written with zero. Contains zeros when read.	
12	AT_FULL _VIO	ARL table full violation. This bit is set to 1 if the ARL table is full when the CPU wishes to add a new entry into the ARL table, and if the ARL table is empty when the CPU wants to purge an entry from the ARL table.	
11:8	AT_PORT_ NUM	The port number to be flushed. If the AT_FUNC is set to 101, the lookup module must flush all unicast entries for the port (or flush the port form the ARL table).	
		0x0	port 0
		0x1	port 1
7:5	RES	Reserved. Must be written with zero. Contains zeros when read.	
4	FLUSH_STAT IC_EN	0	When the AT_FUNC is set to 101, only dynamic entries in the ARL table will be flushed
		1	When the AT_FUNC is set to 101, static entries in the ARL table can be flushed
3	AT_BUSY	The address table is busy. Setting this bit to 1 starts an ARL operation and it must be cleared to zero after the operation is complete. If set to 1, the CPU cannot request another operation	
2:0	AT_FUNC	The address table operation functions	
		000	No operation
		001	Flush all entries
		010	Used to load an entry. If these bits are set, the CPU wishes to load an entry into the ARL table
		011	If these bits are set, used by the CPU to purge an entry from the ARL table
		100	Flushes all unlocked entries from the ARL
		101	Flushes the entries of one port from the Address table
		110	Used to get the next valid or static entry in the ARL table
		111	Setting these bits enables a MAC address to be searched
		If the address and the AT_STATUS are both zero, the hardware will search the first valid entry from entry0. If the address is set to zero and the AT_STATUS is not zero, the hardware will discover the next valid entry which has an address of 0x0. If the hardware returns an address and the AT_STATUS is zero, there is no next valid entry in the address table.	

4.13.1.11 Address Table Function 1

Address: 0x0054
Access: Read/Write
Reset: 0x0

This register holds the address of the ARL table, along with bits [23:16] and [31:24] of the preceding "Address Table Function 0".

Bit	Bit Name	Description
31:24	AT_ADDR_ BYTE0	The first byte of the address to operate. This byte is the highest byte of the MAC address for the most significant bit (MSB).
23:16	AT_ADDR_ BYTE1	The second byte of the address
15:8	AT_ADDR_ BYTE2	The third byte of the address
7:0	AT_ADDR_ BYTE3	The fourth byte of the address

4.13.1.12 Address Table Function 2

Address: 0x0058
Access: Read/Write
Reset: 0x0

This register is used to set parameters for the address resolution table (ARL) such as destination and source address.

Bit	Bit Name	Description	
31:27	RES	Reserved. Must be written with zero. Contains zeros when read.	
26:25	RES	Reserved	
24	LEAKY_EN	Used to enable the leaky VLAN for this MAC address. This bit can be used for multicast frames, control by ARL_UNI_LEAKY_EN and ARL_MULTI_LEAKY_EN.	
23:20	RES	Reserved. Must be written with zero. Contains zeros when read.	
19:16	AT_STATUS	The destination address status. Associated with the "status" bits in the Address Table.	
		0x0000	Indicates the entry is empty
		0x01 to 0x07	Indicates the entry is dynamic and valid
		0x08 to 0x0E	Reserved
		0x0F	Indicates the entry is static and will not be aged out or changed by the hardware
15	RES	Reserved. Must be written with zero. Contains zeros when read.	
14	SA_DROP_EN	Source address (SA) drop enable. Drop packet enable when source address is in this entry. If this bit is set to 1, the packet with an SA of this entry will be dropped.	
13	RES	Reserved	
12	AT_PRIORITY_EN	Setting this bit to 1 enables the use of a DA priority. Can override any other priority determined by the frame's data.	
11:10	AT_PRIORITY	The destination address (DA) priority. These priority bits can be used as a frame's priority when AT_PRIORITY_EN is set to one.	
9:2	RES	Reserved. Must be written with zero. Contains zeros when read.	
1:0	DES_PORT	The destination port bits for address. These bits indicate which ports are associated with the MAC address when they are set to one. Bit 0 is assigned to port 0, bit 1 to port 1.	

4.13.1.13 Address Table Control

Address: 0x005C
Access: Read/Write
Reset: See field description

This register is used to set the parameters of the Address Table Control, including address age out time and MAC address changes.

Bit	Bit Name	Reset	Description
31:21	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
20	ARP_EN	0x0	ARP frame acknowledge enable. Setting this bit to 1 is an acknowledgement by the hardware of a received ARP frame and allows it to be copied to the CPU port.
19	RES	0x1	Reserved.
18	LEARN_ CHANGE_EN	0x0	MAC address change
		0	If a hash violation occurs during learning, no new address will be learned in the ARL
		1	Enables a new MAC address change if a hash violation occurs during learning
17	AGE_EN	0x1	Enables the age operation. Setting this bit to 1 allows the lookup module that can age the address in the address table.
16	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	AGE_TIME	0x2B	The address table age timer. This determines the time that each entry remains valid in the address table, since it was last accessed. The maximum age time is about 10,000 minutes. The default value of 0x2B is for 5 minutes. If the AGE_EN is set to 1, these bits should not be set to 0.

4.13.1.14 IP Priority Mapping 0

Address: 0x0060
Access: Read/Write
Reset: See field description

This register is used to configure the priority mapping value of IPv4 ToS or IPv6 TC field. Bit [7] to bit [2] are used to map queue priority, but bit [1] and bit [0] are ignored. If ToS [7:2] or TC [7:2] is equal to 0x3C, the queue priority should be mapped to the value of these bits.

Bit	Bit Name	Reset	Description
31:30	IP_MAP	0x0	IP_0x3C
29:28	IP_MAP	0x0	IP_0x38
27:26	IP_MAP	0x0	IP_0x34
25:24	IP_MAP	0x0	IP_0x30
23:22	IP_MAP	0x0	IP_0x2C
21:20	IP_MAP	0x0	IP_0x28
19:18	IP_MAP	0x0	IP_0x24
17:16	IP_MAP	0x0	IP_0x20
15:14	IP_MAP	0x0	IP_0x1C
13:12	IP_MAP	0x0	IP_0x18
11:10	IP_MAP	0x0	IP_0x14
9:8	IP_MAP	0x0	IP_0x10
7:6	IP_MAP	0x0	IP_0x0C
5:4	IP_MAP	0x0	IP_0x08
3:2	IP_MAP	0x0	IP_0x04
1:0	IP_MAP	0x0	IP_0x00

4.13.1.15 IP Priority Mapping 1

Address: 0x0064
Access: Read/Write
Reset: See field description

This register is used to configure the priority mapping value of IPv4 ToS or IPv6 TC field. Bit [7] to bit [2] are used to map queue priority, but bit [1] and bit [0] are ignored. If ToS [7:2] or TC [7:2] is equal to 0x3C, the queue priority should be mapped to the value of these bits.

Bit	Bit Name	Reset	Description
31:30	IP_MAP	0x1	IP_0x7C
29:28	IP_MAP	0x1	IP_0x78
27:26	IP_MAP	0x1	IP_0x74
25:24	IP_MAP	0x1	IP_0x70
23:22	IP_MAP	0x1	IP_0x6C
21:20	IP_MAP	0x1	IP_0x68
19:18	IP_MAP	0x1	IP_0x64
17:16	IP_MAP	0x1	IP_0x60
15:14	IP_MAP	0x1	IP_0x5C
13:12	IP_MAP	0x1	IP_0x58
11:10	IP_MAP	0x1	IP_0x54
9:8	IP_MAP	0x1	IP_0x50
7:6	IP_MAP	0x1	IP_0x4C
5:4	IP_MAP	0x1	IP_0x48
3:2	IP_MAP	0x1	IP_0x44
1:0	IP_MAP	0x1	IP_0x40

4.13.1.16 IP Priority Mapping 2

Address: 0x0068
Access: Read/Write
Reset: See field description

This register is used to configure the priority mapping value of IPv4 ToS or IPv6 TC field. Bit [7] to bit [2] are used to map queue priority, but bit [1] and bit [0] are ignored. If ToS [7:2] or TC [7:2] is equal to 0x3C, the queue priority should be mapped to the value of these bits.

Bit	Bit Name	Reset	Description
31:30	IP_MAP	0x2	IP_0xBC
29:28	IP_MAP	0x2	IP_0xB8
27:26	IP_MAP	0x2	IP_0xB4
25:24	IP_MAP	0x2	IP_0xB0
23:22	IP_MAP	0x2	IP_0xAC
21:20	IP_MAP	0x2	IP_0xA8
19:18	IP_MAP	0x2	IP_0xA4
17:16	IP_MAP	0x2	IP_0xA0
15:14	IP_MAP	0x2	IP_0x9C
13:12	IP_MAP	0x2	IP_0x98
11:10	IP_MAP	0x2	IP_0x94
9:8	IP_MAP	0x2	IP_0x90
7:6	IP_MAP	0x2	IP_0x8C
5:4	IP_MAP	0x2	IP_0x88
3:2	IP_MAP	0x2	IP_0x84
1:0	IP_MAP	0x2	IP_0x80

4.13.1.17 IP Priority Mapping 3

Address: 0x006C
Access: Read/Write
Reset: See field description

This register is used to configure the priority mapping value of IPv4 ToS or IPv6 TC field. Bit [7] to bit [2] are used to map queue priority, but bit [1] and bit [0] are ignored. If ToS [7:2] or TC [7:2] is equal to 0x3C, the queue priority should be mapped to the value of these bits.

Bit	Bit Name	Reset	Description
31:30	IP_MAP	0x3	IP_0xFC
29:28	IP_MAP	0x3	IP_0xF8
27:26	IP_MAP	0x3	IP_0xF4
25:24	IP_MAP	0x3	IP_0xF0
23:22	IP_MAP	0x3	IP_0xEC
21:20	IP_MAP	0x3	IP_0xE8
19:18	IP_MAP	0x3	IP_0xE4
17:16	IP_MAP	0x3	IP_0xE0
15:14	IP_MAP	0x3	IP_0xDC
13:12	IP_MAP	0x3	IP_0xD8
11:10	IP_MAP	0x3	IP_0xD4
9:8	IP_MAP	0x3	IP_0xD0
7:6	IP_MAP	0x3	IP_0xCC
5:4	IP_MAP	0x3	IP_0xC8
3:2	IP_MAP	0x3	IP_0xC4
1:0	IP_MAP	0x3	IP_0xC0

4.13.1.18 Tag Priority Mapping

Address: 0x0070
Access: Read/Write
Reset: See field description

This register is used to map the priority value of TAG. If the pri [2:0] in the tag is equal to 0x07, the queue priority should be mapped to the value of these bits.

Bit	Bit Name	Reset	Description
31:16	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:14	TAG7	0x3	The priority mapping value of TAG. TAG_0x07
13:12	TAG6	0x3	The priority mapping value of TAG. TAG_0x06
11:10	TAG5	0x2	The priority mapping value of TAG. TAG_0x05
9:8	TAG4	0x2	The priority mapping value of TAG. TAG_0x04
7:6	TAG3	0x1	The priority mapping value of TAG. TAG_0x03
5:4	TAG2	0x0	The priority mapping value of TAG. TAG_0x02
3:2	TAG1	0x0	The priority mapping value of TAG. TAG_0x01
1:0	TAG0	0x1	The priority mapping value of TAG. TAG_0x00

4.13.1.19 Service Tag

Address: 0x0074
Access: Read/Write
Reset: 0x0

This register is used to double tag egress packets and recognize double tagged packets at ingress.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	SERVICE_TAG	The service tag. These bits are used to recognize the double tag at ingress and insert the double tag at egress.

4.13.1.20 MIB Function0

Address: 0x0080
Access: Read/Write
Reset: 0x0

This register is used to set the MIB functions such as the auto-cast timer and MIB functions.

Bit	Bit Name	Description	
31:27	RES	Reserved. Must be written with zero. Contains zeros when read.	
26:24	MIB_FUNC	The current MIB function	
		000	No Operation
		001	Flush all counters on all ports
		010	Reserved
		011	Capture all counters for all ports and auto-cast to the CPU port
		1xx	Reserved
23:18	RES	Reserved. Must be written with zero. Contains zeros when read.	
17	MIB_BUSY	The MIB module status	
		0	The MIB module is currently empty and can access a new command
		1	The MIB module is busy and cannot access a new command
16	MIB_AT _HALFEN	The MIB auto-cast is enabled due to half flow. If set to one, the MIB will be auto-cast when the highest bit count for any counter is set as 1.	
15:0	MIB_TIMER	The MIB auto-cast timer. If set to 0, the MIB will not auto-cast because the timer timed out. This timer is set in periods of 8.4 ms. The recommended value is 0x100. (8.4 ms x 4)	

4.13.1.21 MDIO Control

Address: 0x0098
Access: Read/Write
Reset: 0x0

This register is used to control the functions of the MDIO interface.

Bit	Bit Name	Description	
31	MDIO_BUSY	Writing a one to this bit represents the internal MDIO interface as busy. This bit should be set when the CPU reads or writes to the PHY register through the internal MDIO interface, and should be cleared after the hardware finishes this command	
30	MDIO_ MASTER_EN	Writing a 1 to this bit enables the MDIO master which is used to configure the PHY register. MDC should change to the internal MDC to PHY	
29:28	RES	Reserved. Must be written with zero. Contains zeros when read.	
27	MDIO_CMD	This bit represents the commands given for the MDIO	
		0	Write
		1	Read
26	MDIO_SUP_ PRE	Writing a 1 to this bit enables the supposed preamble	
25:21	PHY_ADDR	These bits represent the PHY address	
20:16	REG_ADDR	These bits represent the PHY register address	
15:0	MDIO_DATA	When write, these bits are data written to the PHY register. When read, these bits are read out from the PHY register	

4.13.2 Port Control Registers

Table 4-22 summarizes the port control registers for the AR7242.

Table 4-22. **Port Control Registers Summary**

Port0	Port1	Register	Page
0x0100	0x0200	Port Status	page 171
0x0104	0x0204	Port Control	page 172
0x0108	0x0208	Port Base VLAN	page 173
0x010C	0x020C	Rate Limit 0	page 174
0x0110	0x0210	Priority Control	page 174
0x0114	0x0214	Storm Control	page 175
0x0118	0x0218	Queue Control	page 176
0x011C	0x021C	Rate Limit 1	page 178
0x0120	0x0220	Rate Limit 2	page 178

4.13.2.1Port Status

Address: 0x0100/0x0200
Access: See field description
Reset: 0x0

This register denotes the settings for the port including flow control and speed.

Bit	Bit Name	Type	Description	
31:12	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
11	LINK_ASYN_PAUSE_EN	RO	The link partner supports ASYN flow control	
10	LINK_PAUSE_ EN	RO	The link partner support flow control	
9	LINK_EN	RW	This bit is used to enable the PHY link mode	
			0	Allows the MAC to be configured by the software
			1	Enables the use of the PHY link status to configure the MAC
8	LINK	RO	The current link status	
			0	PHY link down
			1	PHY link up
7	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
6	DUPLEX_MODE	RW	The duplex mode	
			0	Half-duplex mode
			1	Full-duplex mode
5	RX_FLOW_EN	RW	Rx MAC flow control enable	
4	TX_FLOW_EN	RW	Tx MAC flow control enable	
3	RXMAC_EN	RW	Enables the Rx MAC	
2	TXMAC_EN	RW	Enables the Tx MAC	
1:0	SPEED	RW	The speed mode	
			00	10 Mbps
			01	100 Mbps
			10	Reserved
			11	Speed mode error

4.13.2.2 Port Control

Address: 0x0104/0x0204
Access: Read/Write
Reset: See field description

This register is used to configure port functions such as spanning tree.

Bit	Bit Name	Reset	Description
31:18	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
17:16	RES	0x0	Reserved
15	DOUBLE _TAG_VLAN	0x0	Setting this bit to 1 will enable the double tag where the MAC will check received frames for the service tag and if found, remove it.
14	LEARN_EN	0x1	Used to enable the learning operation. Setting this bit to 1 will allow the lookup module to learn new addresses to the address table
13	SINGLE _VLAN_EN	0x0	Setting this bit allows the MAC to transmit and receive packets with the single VLAN enabled
12	MAC_LOOP_ BACK	0x0	Setting this bit to 1 enables the MAC Loop back function on the MII interface
11	RES	0x0	Reserved.
10	IGMP_MLD _EN	0x0	Enables IGMP/MLD Snooping. Setting this bit to one allows the port to examine all received frames and copy or redirect them to the CPU port, based on the IGMP_COPY_EN bit setting.
9:8	EG_VLAN_ MODE	0x0	Egress VLAN mode based on the following
			00 Egress should transmit frames unmodified
			01 Egress should transmit without VLAN
			10 Egress should transmit frames with VLAN
			11 Double tagged. The MAC should add one tag after the source address. This tag will be set in the SERVICE_TAG register
7	LEARN_ONE _ LOCK	0x0	0 Normal learning mode
			1 This port should not learn source addresses except from the first packet which will be locked in as a static address
6	PORT_LOCK _EN	0x0	When this bit is set to 1, the port lock is enabled. All packets received with the source address not found in the ARL table, or the source address resides in the ARL table but the port member is not the source address, should be redirected to the CPU or dropped, which is controlled by the LOCK_DROP_EN bit.
5	LOCK_DROP _ EN	0x0	0 If the source address is not in the ARL table or the port member is not the source port, the packet should be re4directed to the CPU when the PORT_LOCK_EN bit is set to 1.
			1 If the source address is not in the ARL table or if it is there but the port member is not the source port, the packet should be dropped when the PORT_LOCK_EN bit is set to 1.
4:3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
2:0	PORT_STATE	0x4	Port state. These bits manage the port to determine what kind of frames may enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree.
			000 Disabled mode. This port cannot send or receive frames.
			001 Blocking mode. The port forwards received management frames to the designed port only. Other frames are not transmitted or received and do not learn source addresses.
			010 Listening mode. The port receives and transmits only management frames without learning the source address. Other frames are not transmitted or received.
			011 Learning mode. The port learns all source addresses and discards all frames except management frames, and management frames can only be transmitted.
			100 Forwarding mode. The port will learn all source addresses and transmit and receive frames normally.

4.13.2.3 Port Base VLAN

Address: 0x0108/0x0208
Access: Read/Write
Reset: 0x0

This register is used to configure the bits for the VLANs, including port VIDs and Leaky VLANs.

Bit	Bit Name	Description	
31:30	8021Q_MODE	Sets the 802.1Q mode for this port	
		00	Disables the 802.1Q VLAN function. Port-based VLAN used only.
		01	Enables 802.1Q for all received frames. If the VID for the received frame is not contained in the VLAN table, port VLANs will be used and ingress membership will not be discarded.
		10	Enables 802.1Q for all received frames. Frames will be discarded only if the VID of the frames are not contained in the VLAN table. Ingress membership will not be discarded.
		11	Enables 802.1Q for all received frames. Frames will be discarded if the VID of the frames are not contained in the VLAN table and ingress membership will be discarded.
29:27	ING_PORT_PRI	The port default priority for received frames.	
25:16	PORT_VID_ MEMBER	Port Base VLAN Member. Each bit restricts which port can send frames to port 0, bit 16 must be set to 1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they are received on.	
26	FORCE_PORT_ VLAN_EN	Setting this bit forces port-based VLANs to be enabled. This uses the port base VLAN and the VLAN table to determine the destination port.	
15	ARP_LEAKY_EN	Setting this bit to 1 allows received frames from this port on the MAC to cross all VLANs (both port-based and 802.1Q)	
14	UNI_LEAKY_EN	Used to enable Unicast frames for the leaky VLAN. If the MAC receives unicast frames on this port, it should forward them as leaky VLAN frames. These frames may be switched to the destination port defined in the ARL table and then across all VLANs (including port-based and 802.1Q). Users may enable the ARL_MULTI_LEAKY_EN bit and the LEAKY_EN bit the ARL table to control unicast frames for the leaky VLAN. When the ARL_MULTI_LEAKY_EN is set to 0, only the MULTI_LEAKY_EN controls multicast frames for the leaky VLAN. If the ARL_MULTI_LEAKY_VLAN bit is set to 1, only frames with the destination address in the ARL table and their LEAKY_EN bit is set to 1, can be forwarded as leaky VLAN frames. This will force the MULTI_LEAKY_EN bit to be ignored.	
13	MULTI_LEAKY_ EN	Used to enable Multicast frames for the leaky VLAN. If the MAC receives multicast frames on this port, it should forward them as leaky VLAN frames. These frames may be switched to the destination port defined in the ARL table and then across all VLANs (including port-based and 802.1Q). Users may enable the ARL_MULTI_LEAKY_EN bit and the LEAKY_EN bit the ARL table to control unicast frames for the leaky VLAN. When the ARL_MULTI_LEAKY_EN is set to 0, only the MULTI_LEAKY_EN controls multicast frames for the leaky VLAN. If the ARL_UNI_LEAKY_VLAN bit is set to 1, only frames with the destination address in the ARL table and their LEAKY_EN bit is set to 1 can be forwarded as leaky VLAN frames. This will force the UNI_LEAKY_EN bit to be ignored.	
12	FORCE_ DEFALUT_VID_ EN	0	Received frames will use only the tag set with the received frames for port default VID and priority
		1	When 802.1Q is enabled, the received frames must use the port default VID and priority issued to them by the MAC/PHY
11:0	PORT_VID	The port default VID. Untagged frames transmitted from this port will have the default VID tagged to them	

4.13.2.4 Rate Limit

Address: 0x010C/0x020C
Access: Read/Write
Reset: See field description

This register is used to set rate limits various frame types.

Bit	Bit Name	Reset	Description
31:24	ADD_RATE_BYTE	0x18	The byte number should be added to the frame when calculating the rate limit. The default is 24 bytes for IPG, preamble SFD and CRC.
23	EGRESS_RATE_EN	0x0	Enables the port base rate limit. The rate should be set using the EG_PRI3_RATE
22	EGRESS_MANAGE_RATE_EN	0x0	Enables management frames to be included in the calculations for the egress rate limit
21	INGRESS_MANAGE_RATE_EN	0x0	Enables management frames to be included in the calculations for the ingress rate limit
20	INGRESS_MULTI_RATE_EN	0x0	Enables multicast frames to be included in the calculations for the ingress rate limit, if the destination address of those multicast frames is found in the ARL table
19:15	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
14:0	ING_RATE	0x7FFF	The Ingress Rate Limit for all priorities. This rate is limited to multiples of 32kbps. The default of 0x7FFF disables the rate limit for ingress traffic. When these bits are set to 0x0, no frames should be received on the port.

4.13.2.5 Priority Control

Address: 0x0110/0x0210 (See Table 4-22)
Access: Read/Write
Reset: See field description

This register is used to set the priority for QoS based on priorities set for other functions like ToS and IP.

Bit	Bit Name	Reset	Description
31:20	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
19	PORT_PRI_EN	0x1	Setting this bit to 1 allows the port-based priority to be used for QoS
18	DA_PRI_EN	0x0	Setting this bit to 1 allows the destination address priority to be used for QoS
17	VLAN_PRI_EN	0x0	Setting this bit to 1 allows the VLAN priority to be used for QoS
16	IP_PRI_EN	0x0	Setting this bit to 1 allows the ToS/TC to be used for QoS
15:8	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:6	DA_PRI_SEL	0x0	The DA priority selected level for QoS, which has five levels. The highest priority is the one found in the packet header. The other four are selected by these bits. If these bits are set to 0, the destination address priority is selected after the header. If set to n, the destination address priority is selected after the priority is set to n-1.
5:4	VLAN_PRI_SEL	0x1	VLAN priority selected level for QoS
3:2	IP_PRI_SEL	0x2	IP priority selected level for QoS
1:0	PORT_PRI_SEL	0x3	Port-based priority selected level for QoS

4.13.2.6 Storm Control

Address: 0x0114/0x0214
Access: Read/Write
Reset: 0x0

This register sets the rate for the storm control based on incoming broadcast, unicast and multicast frames.

Bit	Bit Name	Type	Reset	Description	
31:11	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
10	MULTI_STORM_EN	RW	0x0	Setting this bit to 1 enables unknown multicast frames to be included in the calculations for storm control	
9	UNI_STORM_EN	RW	0x0	Setting this bit to 1 enables unknown unicast frames to be included in the calculations for storm control	
8	BROAD_STORM_EN	RW	0x0	Setting this bit to 1 enables broadcast frames to be included in the calculations for storm control	
7:4	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
3:0	STORM_RATE	RW	0x0	The storm control rate	
				0x0	Disables storm control
				0x1	Rate set at 1K frames per second
				0x2	Rate set at 2K frames per second
				0x3	Rate set at 4K frames per second
				0x4	Rate set at 8K frames per second
				0x5	Rate set at 16K frames per second
				0x6	Rate set at 32K frames per second
				0x7	Rate set at 64K frames per second
				0x8	Rate set at 128K frames per second
				0x9	Rate set at 256K frames per second
				0xA	Rate set at 512K frames per second
				0xB	Rate set at 1M frames per second

4.13.2.7 Queue Control

Address: 0x0118/0x0218
Access: Read/Write
Reset: See field description

This register is used to set the buffer controls for QoS queues.

Bit	Bit Name	Reset	Description	
31:26	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
25	PORT_QUEUE _CTRL_EN	0x1	Setting this bit to 1 enables the specified port to use the memory depth control feature	
24	PRI_QUEUE_ CTRL_EN	0x0	Setting this bit to 1 enables the memory depth control for this port based on priority	
23:21	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
20:16	PRI_QUEUE_ NUM	0x10	This field sets the limit of the buffer size for QoS priority queue. Each bit represents a block of memory x 4, where each block represents 256 bytes. Therefore the maximum amount of memory that this bit can hold in the queue is 1024 bytes. (4x 256 = 1024)	
			0x0	No memory for the queue
			0x1	A maximum of 4 blocks (1024 bytes)
			0x2	A maximum of 8 blocks (2048 bytes)
			0x3	A maximum of 12 blocks (3072 bytes)
			...	...
			0x1F	A maximum of 120 blocks (30720 bytes)
			Each successive hex value holds the same formula until 0x1F which will be a maximum of 120 blocks (30720 bytes)	
15:12	PRI3_QUEUE_ NUM	0x0	This field sets the limit of the buffer size for QoS priority queue 3. Each bit represents a block of memory x 4, where each block represents 256 bytes. Therefore the maximum amount of memory that this bit can hold in the queue is 1024 bytes. (4x 256 = 1024)	
			0x0	No memory for the queue
			0x1	A maximum of 4 blocks (1024 bytes)
			0x2	A maximum of 8 blocks (2048 bytes)
			0x3	A maximum of 12 blocks (3072 bytes)
			...	...
			0xF	A maximum of 60 blocks (15360 bytes)
			Each successive hex value holds the same formula until 0xF which will be a maximum of 60 blocks (15360 bytes)	

11:8	PRI2_QUEUE_ NUM	0x0	This field sets the limit of the buffer size for QoS priority queue 2. Each bit represents a block of memory x 4, where each block represents 256 bytes. Therefore the maximum amount of memory that this bit can hold in the queue is 1024 bytes. (4x 256 = 1024)	
			0x0	No memory for the queue
			0x1	A maximum of 4 blocks (1024 bytes)
			0x2	A maximum of 8 blocks (2048 bytes)
			0x3	A maximum of 12 blocks (3072 bytes)
			...	...
			0xF	A maximum of 60 blocks (15360 bytes)
			Each successive hex value holds the same formula until 0xF which will be a maximum of 60 blocks (15360 bytes)	
7:4	PRI1_QUEUE_ NUM	0x0	This field sets the limit of the buffer size for QoS priority queue 1. Each bit represents a block of memory x 4, where each block represents 256 bytes. Therefore the maximum amount of memory that this bit can hold in the queue is 1024 bytes. (4x 256 = 1024)	
			0x0	No memory for the queue
			0x1	A maximum of 4 blocks (1024 bytes)
			0x2	A maximum of 8 blocks (2048 bytes)
			0x3	A maximum of 12 blocks (3072 bytes)
			...	...
			0xF	A maximum of 60 blocks (15360 bytes)
			Each successive hex value holds the same formula until 0xF which will be a maximum of 60 blocks (15360 bytes)	
3:0	PRI0_QUEUE_ NUM	0x0	This field sets the limit of the buffer size for QoS priority queue 0. Each bit represents a block of memory x 4, where each block represents 256 bytes. Therefore the maximum amount of memory that this bit can hold in the queue is 1024 bytes. (4x 256 = 1024)	
			0x0	No memory for the queue
			0x1	A maximum of 4 blocks (1024 bytes)
			0x2	A maximum of 8 blocks (2048 bytes)
			0x3	A maximum of 12 blocks (3072 bytes)
			...	...
			0xF	A maximum of 60 blocks (15360 bytes)
			Each successive hex value holds the same formula until 0xF which will be a maximum of 60 blocks (15360 bytes)	

4.13.2.8 Rate Limit Register 1

Address: 0x011C/0x021C
Access: Read/Write
Reset: See field description

This register is used to set the rate limits for priority queues.

Bit	Bit Name	Reset	Description
31	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
30:16	EG_PRI1_RATE	0x7FFF	The egress rate limit for priority 1. The rate limit is calculated in increments of 32 Kbps. The reset value will disable the rate limit for egress priority 2. If these bits are set to 0 no priority 1 frame will be sent out from this port.
15	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
14:0	EG_PRI0_RATE	0x7FFF	The egress rate limit for priority 0. The rate limit is calculated in increments of 32 Kbps. The reset value will disable the rate limit for egress priority 2. If these bits are set to 0 no priority 0 frame will be sent out from this port.

4.13.2.9 Rate Limit Register 2

Address: 0x0120/0x0220
Access: Read/Write
Reset: See field description

This register used to set the rate limits for priority queues.

Bit	Bit Name	Reset	Description
31	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
30:16	EG_PRI3_RATE	0x7FFF	The egress rate limit for priority 3. The rate limit is calculated in increments of 32 Kbps. The reset value will disable the rate limit for egress priority 0. If these bits are set to 1 no priority 3 frame will be sent out from this port.
15	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
14:0	EG_PRI2_RATE	0x7FFF	The egress rate limit for priority 2. The rate limit is calculated in increments of 32 Kbps. The reset value will disable the rate limit for egress priority 2. If these bits are set to 0 no priority 2 frame will be sent out from this port.

4.13.3 Statistics Counters

Table 4-10 lists the AR7242 statistics counters.

Table 4-10. **Extensive RMON/Statistics Counters**

Name	Description	Port0	Port1
RxBroad	The number of good broadcast frames received	20000	20100
RxPause	The number of pause frames received	20004	20104
RxMulti	The number of good multicast frames received	20008	20108
RxFcsErr	Total frames received with a valid length that have an invalid FCS and an integral number of octets	2000C	2010C
RxAllignErr	Total frames received with a valid length that not have an integral number of octets and invalid FCS	20010	20110
RxRunt	The number of frames received that are less than 64 byte long and good FCS	20014	20114
RxFragment	The number of frames received that are less than 64 byte long and bad FCS	20018	20118
Rx64Byte	The number of frames received that are exactly 64 byte long, including those with errors	2001C	2011C

Table 4-10. **Extensive RMON/Statistics Counters (continued)**

Rx128Byte	The number of frames received whose length between 65 to 127, including those with errors	20020	20120
Rx256Byte	The number of frames received whose length between 128 to 255, including those with errors	20024	20124
Rx512Byte	The number of frames received whose length between 256 to 511, including those with errors	20028	20120
Rx1024Byte	The number of frames received whose length between 512 to 1023, including those with errors	2002C	2012C
Rx1518Byte	The number of frames received whose length between 1024 to 1518, including those with errors	20030	20130
RxMaxByte	The number of frames received whose length between 1519 to MaxLength, including those with errors (Jumbo)	20034	20134
RxTooLong	The number of frames received whose length exceed MaxLength, including those with FCS errors	20038	20138
RxGoodByte	Total data octets received in frame with a valid FCS; all size frames are included	2003C	2013C
RxBadByte	Total data octets received in frame with a invalid FCS alignment error; all size frames are included and pause frame is included with a valid FCS	20044	20144
RxOverFlow	Total valid frames received that are discarded due to lack of buffer space.	2004C	2014C
Filtered	Port disable and unknown VID	20050	20150
TxBroad	Total good frames transmitted with a broadcast destination address	20054	20154
TxPause	Total good PAUSE frames transmitted	20058	20150
TxMulti	Total good frames transmitted with a multicast destination address	2005C	2015C
TxUnderRun	Total valid frames discarded that were not transmitted due to Tx FIFO underflow	20060	20160
Tx64Byte	Total frames transmitted with a length of exactly 64 byte, including errors	20064	20164
Tx128Byte	Total frames transmitted with length between 65 to 127, including errors	20068	20138
Tx256Byte	Total frames transmitted with length between 128 to 255, including errors	2006C	2016C
Tx512Byte	Total frames transmitted with length between 256 to 511, including errors	20070	20170
Tx1024Byte	Total frames transmitted with length between 512 to 1023, including errors	20074	20174
Tx1518Byte	Total frames transmitted with length between 1024 to 1518, including errors	20078	20178
TxMaxByte	Total frames transmitted with length between 1519 to MaxLength, including errors (Jumbo)	2007C	2017C
TxOverSize	Total frames over MaxLength but transmitted truncated with bad FCS	20080	20180
TxByte	Total data octets transmitted from frames counted, included with bad FCS	20084	20184
TxCollision	Total collisions experienced by a port during packet transmissions	2008C	2018C
TxAbortCol	Total number of frames not transmitted because the frame experienced 16 transmission attempts and was discarded	20090	20190
TxMultiCol	Total number of successfully transmitted frames that experienced more than one collision	20094	20194
TxSingalCol	Total number of successfully transmitted frames that experienced exactly one collision	20098	20198
TxExcDefer	The number of frames that deferred for an excessive period of time	2009C	2019C
TxDefer	Total frames whose transmission was delayed on its first attempt because the medium was busy	200A0	201A0
TxLateCol	Total number of times a collision is detected later than 512 bit-times into the transmission of a frame	200A4	201A4

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5-1 summarizes the absolute maximum ratings and Table 5-2 lists the recommended operating conditions for the AR7242.

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 5-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max Rating	Unit
V_{DD33}	Supply Voltage	–0.3 to 4.0	V
V_{DD25}	Maximum I/O Supply Voltage	–0.3 to 3.0	V
V_{DD12}	Core Voltage	–0.3 to 1.8	V
T_{store}	Storage Temperature	–65 to 150	°C
T_j	Junction Temperature	125	°C
ESD	Electrostatic Discharge Tolerance	2000	V

5.2 Recommended Operating Conditions

Table 5-2. **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	Supply Voltage	±10%	2.97	3.3	3.63	V
V_{DD25}	I/O Supply Voltage[1]	±5%	2.49	2.62	2.75	V
V_{DD12}	Core Voltage[1]	±5%	1.14	1.2	1.26	V
V_{DD12CD}	Core Voltage for CPU/DDR[1]	±5%	1.216	1.28	1.34	V
AV_{DD20}	Voltage for Ethernet PHY[1]	—	1.9	2.0	2.15	V
V_{DD_DDR}	DDR1 I/O Voltage[1]	±5%	2.47	2.6	2.73	V
	DDR2 I/O Voltage[1]	±5%	1.71	1.8	1.89	V
D_{DR_VREF}	DDR1 Reference Level for SSTL Signals[2]	—	1.24	1.3	1.37	V
	DDR2 Reference Level for SSTL Signals[2]	—	0.86	0.9	0.95	V
T_{case}	Case Temperature	—	0	—	110	°C
Psi_{JT}	Thermal Parameter[3]	—	—	—	3.1	°C/W

[1]Voltage regulated internally by the AR7242
[2]Divide VDD_DDR voltage by two externally, see reference design schematic
[3]The thermal parameter is for the 14x14 mm LQFP package.

5.3 General DC Electrical Characteristics

Table 5-3 lists the general DC electrical characteristics.

These conditions apply to all DC characteristics unless otherwise specified:

T_{amb} = 25 °C, V_{dd25} = 2.62 V

Table 5-3. **General DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	2.0	—	2.8	V
V_{IL}	Low Level Input Voltage	—	–0.3	—	0.4	V
I_{IL}	Input Leakage Current	With pull down	—	26	—	µA
V_{OH}	High Level Output Voltage	I_o = 1 mA	2.2	—	2.8	V
V_{OL}	Low Level Output Voltage	I_o = 1 mA	0	—	0.4	V
I_O	Output Current	V_o = 0 to V_{dd}	—	1	—	mA
	GPO_13 when used as LED_0	V_o = 0 to V_{dd}	—	10	—	mA
C_{IN}	Input Capacitance	—	—	3	—	pF

Table 5-4 lists the DDR1 DC electrical characteristics:

T_{amb} = 25 °C, V_{DD_DDR} = 2.6 V

Table 5-4. **DDR1 Interface DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	1.48	—	2.9	V
V_{IL}	Low Level Input Voltage	—	–0.3	—	1.12	V
V_{OH}	High Level Output Voltage	I_o = 1 mA	2.2	—	2.8	V
V_{OL}	Low Level Output Voltage	I_o = 1 mA	–0.3	—	0.4	V

Table 5-5 lists the DDR2 DC electrical characteristics:

T_{amb} = 25 °C, V_{DD_DDR} = 1.8 V

Table 5-5. **DDR2 Interface DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	1.1	—	2.2	V
V_{IL}	Low Level Input Voltage	—	–0.3	—	0.8	V
V_{OH}	High Level Output Voltage	I_o = 1 mA	1.6	—	2.2	V
V_{OL}	Low Level Output Voltage	I_o = 1 mA	–0.3	—	0.4	V

Table 5-5 lists the RGMII DC electrical characteristics:

T_{amb} = 25 °C, V_{DD} = 2.62 V

Table 5-6. **RGMII Interface DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	1.7	—	3.5	V
V_{IL}	Low Level Input Voltage	—	—	—	0.7	V
V_{OH}	High Level Output Voltage	—	2.0	—	2.8	V
V_{OL}	Low Level Output Voltage	—	–0.3	—	0.4	V
I_{IH}	Input High Current	—	—	—	15	µA
I_{IL}	Input Low Current	—	–15	—	—	µA

Table 5-7 lists the EJTAG and LDO DC electrical characteristics:

T_{amb} = 25 °C, V_{DD} = 2.62 V

Table 5-7. **EJTAG and LDO DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage (EJTAG_SEL, TRST_L, TCK, LDO_DDR_SEL)	—	2	—	3.6	V
V_{IL}	Low Level Input Voltage (EJTAG_SEL, TRST_L, TCK, LDO_DDR_SEL)	—	–0.3	—	0.4	V
V_{IH}	High Level Input Voltage (TMS, TDI)	—	2	—	2.8	V
V_{IL}	Low Level Input Voltage (TMS, TDI)	—	–0.3	—	0.4	V
V_{OH}	High Level Output Voltage (TDO)	—	2.2	—	2.8	V
V_{OL}	Low Level Output Voltage (TDO)	—	0	—	0.4	V

5.4 40 MHz Clock Characteristics

The 40 MHz reference clock can be AC coupled sine wave or square wave. An external 100 pF capacitor should connect between REFCLKIN and the clock source. See Table 5-8 and Table 5-9 for more information.

Table 5-8. **40 MHz Clock Sine Wave Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{Ampl}	Peak-to-Peak Amplitude	—	0.6	—	1.4	V

Table 5-9. **40 MHz Clock Square Wave Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{Ampl}	Peak-to-Peak Amplitude	—	0.6	—	1.2	V
T_{DCycle}	Duty Cycle	—	40	50	60	%
T_{Rise}	Rise Time	—	—	—	3	ns
T_{Fall}	Fall Time	—	—	—	3	ns

5.5 Power Consumption

Primary voltage supply of the AR7242 is provided by the VDD33, pins 71 and 117. The VDD33 is regulated by the internal LDOs to supply power to the external DDR memory, and magnetics of the Ethernet ports.

Figure 5-1 depicts the output voltages regulated by the AR7242. Refer to the reference design schematics for details. Table 5-10 shows the typical power consumption for the AR7242, including Ethernet port, PCIE interface operating in 802.11n HT40 mode, with bidirectional TCP traffic.

Table 5-10. **Power Consumption**

Symbol	Voltage (V)	Current (mA)
V_{DD33}	3.3	852[1]

[1]Current consumption does not include external DDR memory and magnetics.

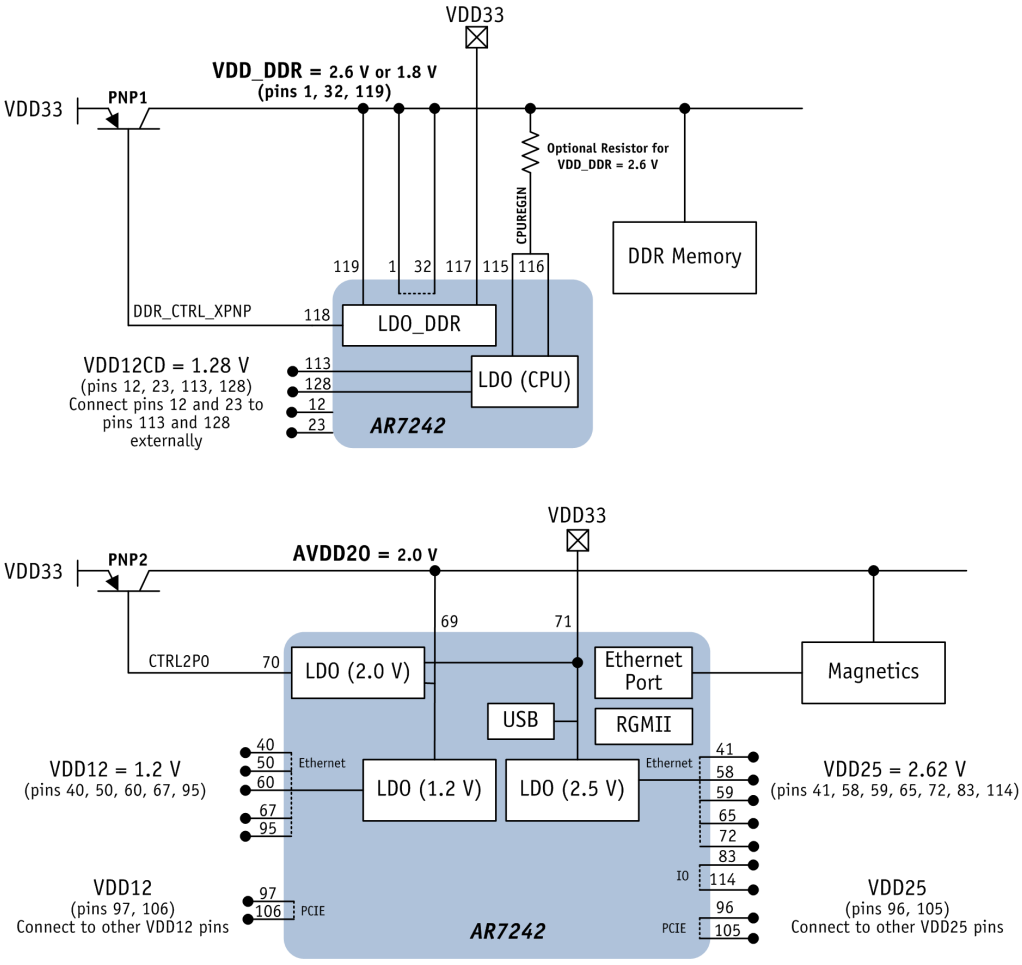

Figure 5-1. **Output Voltages Regulated by the AR7242**

5.6 External Voltage Regulator

External voltage regulator can be used to provide VDD12 and VDD12CD power to the AR7242 to reduce current consumption. Input to this regulator is 3.3 V and output should be 1.3 V ±2%. See Table 5-11.

Table 5-11. **Recommended External Voltage Regulator Operating Conditions**

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage	±10%	2.97	3.3	3.63	V
Output Voltage	±2%	1.274	1.3	1.326	V

Figure 5-2 depicts the voltages regulated by the AR7242 (except for VDD12CD and VDD12), and the external voltage regulator connection. Refer to the reference design schematics for details. Table 5-12 shows the typical power consumption for the AR7242 with Ethernet port, PCIE interface in 802.11n HT40 mode, with bidirectional TCP traffic..

Table 5-12. **Power Consumption with External Voltage Regulator**

Symbol	Voltage (V)	Current (mA)[1]
V_{DD33}	3.3	90
V_{DD12CD}[2]	1.28	519

[1]Current consumption without external DDR memory and magnetics
[2]Current consumption includes V_{DD12}

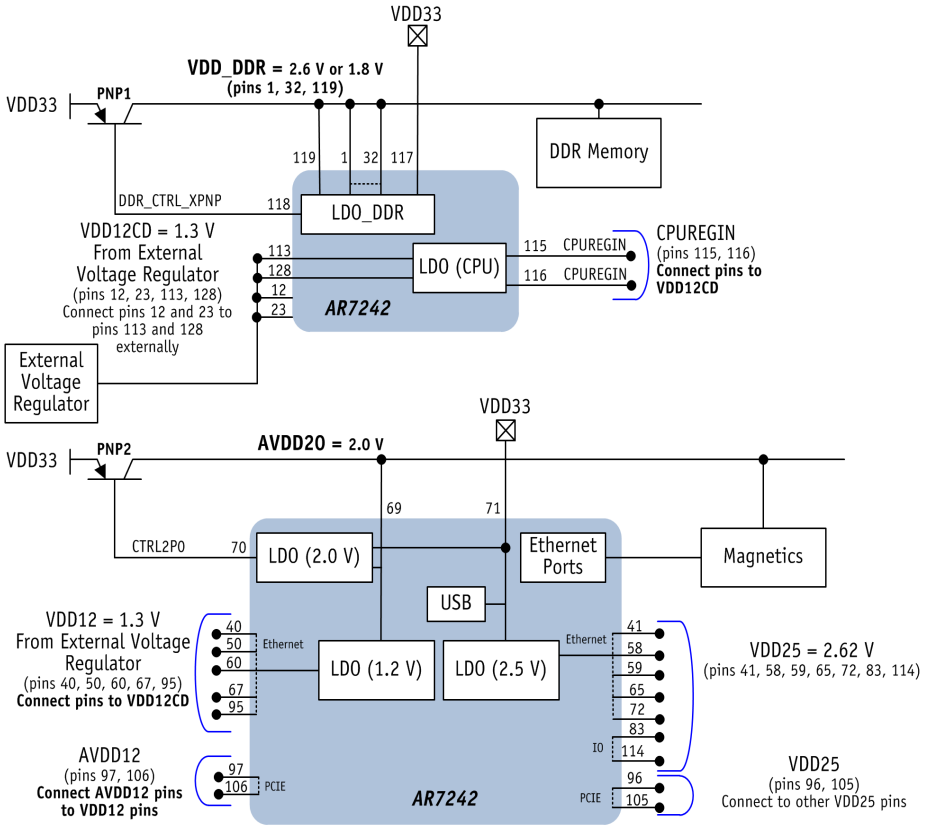

Figure 5-2. **Output Voltages Regulated by the AR7242 and External 1.3 V Voltage Regulator Connection**

6. AC Specifications

6.1 DDR Interface Timing

Figure 6-1 shows the DDR output timing. See Table 6-1 for timing values.

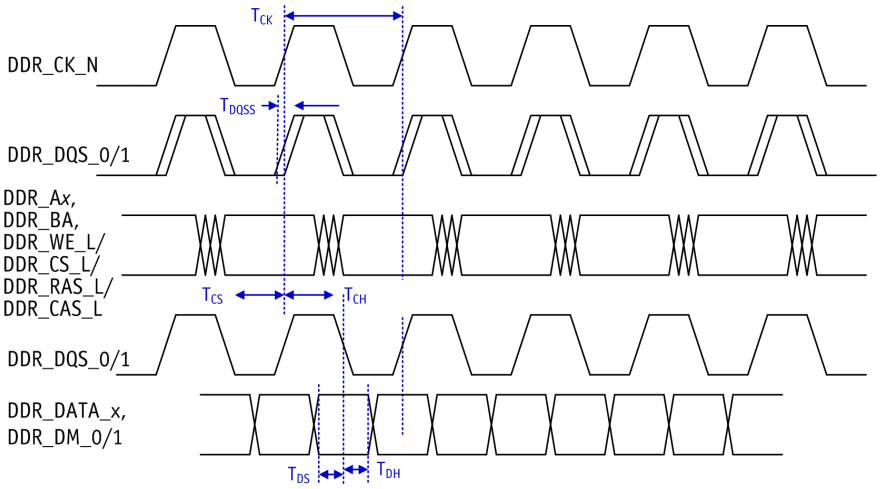

Figure 6-1. **DDR Output Timing**

Table 6-1. **DDR Output Timing Values[1]**

Parameter	Reference Signal	Min	Max	Comments
T_{CK}	—	—	5.0 ns	Normal period of CK_P clock output signal
T_{CS}	DDR_CK_P	2.0 ns	—	Control signals output setup time
T_{CH}	DDR_CK_P	2.0 ns	—	—
T_{DQSS}	DDR_CK_P	—	0.4 ns	Maximum skew between edge of CK_P and DQS with respect to either edge of CK_P
T_{DS}	DDR_DQS_0/1	1.0 ns	—	DDR data/mask signal setup time
T_{DH}	DDR_DQS_0/1	0.8 ns	—	DDR data/mask signal hold time

[1]These numbers assume a 400 MHz DDR_CLK frequency. Control signals include all address, bank address, RAS, CAS, CS_L, and CKE WE_L signals. Data signals include data and data mask signals.

Figure 6-2 shows the DDR input timing. See Table 6-2 for timing values.

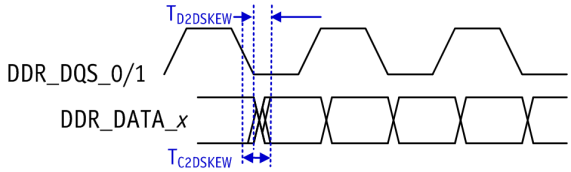

Figure 6-2. **DDR Controller Interface Input Timing**

Table 6-2. **DDR Controller Interface Input Timing Values**

Parameter	Reference Signal	Min	Max	Comments
$T_{C2DSKEW}$	DDR_DQS_0, DDR_DQS_1	—	0.4 ns	Maximum skew from DQS to DQ being stable from memory
$T_{D2DSKEW}$	—	—	0.2 ns	Maximum skew along data lines

6.2 Reset Timing

Internal reset of the AR7242 is held low until the VDD12 and VDD12CD voltages are up and RST_L pin (with internal pull-up) is deasserted. VDD12CD is generated from VDD_DDR, which is the last voltage domain to come up. The actual timing between the de-assertion of these signals is not critical. See Figure 6-3, the conceptual power up sequence.

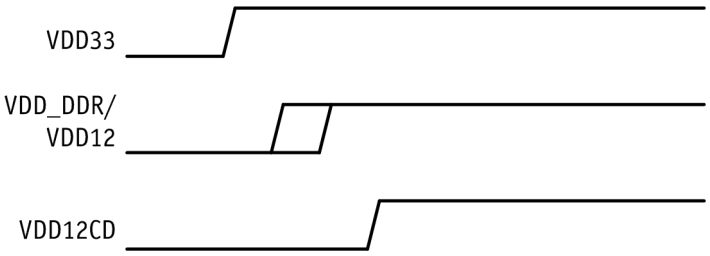

Figure 6-3. **Conceptual Power-Up Sequence**

Immediately after power on reset, the CPU boots up with the reference clock, then programs the PLL and releases all the interface resets, which causes the SYS_RST_OUT_L pin to be de-asserted. The time from internal reset de-asserted to the SYS_RST_OUT_L pin de-asserted is approximately 5 ms based on the 40 MHz reference clock. Figure 6-4 shows a conceptual reset timing diagram.

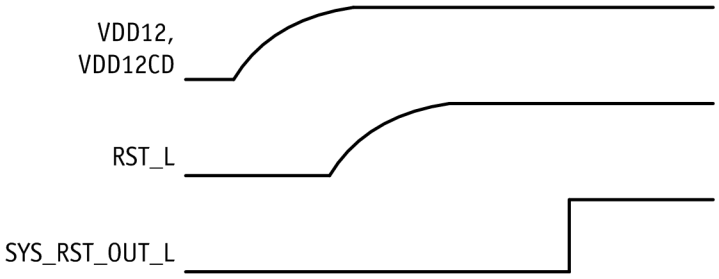

Figure 6-4. **Reset Timing**

6.3 SPI Serial Flash Interface Timing

Figure 6-5 shows the SPI serial flash interface timing.

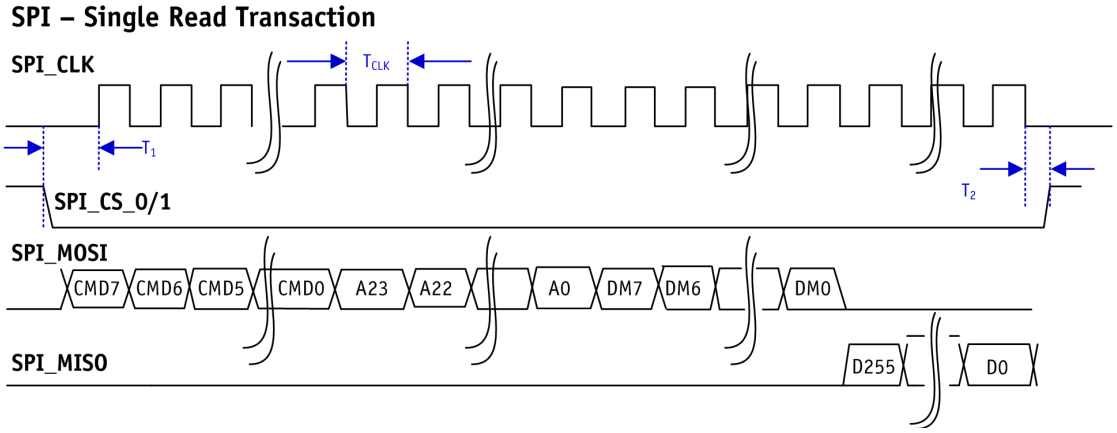

Figure 6-5. **SPI Serial Flash Interface Timing**

Table 6-3. **SPI Serial Flash Timing Values**

Symbol	Parameter
T_1	(3 + CLK_DIV) AHB_CLK Cycles
T_2	1 AHB_CLK
T_{CLK}	AHB_CLK/(CLK_DIV + 1) * 2

Figure 6-6 shows the SPI setup and hold timing.

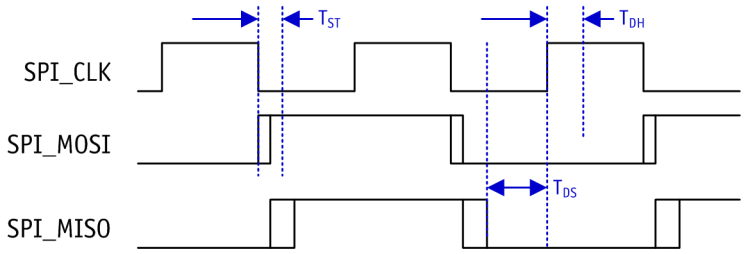

Figure 6-6. **SPI Setup and Hold Timing**

Table 6-4. **SPI Setup and Hold Timing Values**

Symbol	Minimum	Maximum	Comments
T_{DS}	3.0 ns	—	Minimum needed by the AR7242
T_{ST}	—	0.8 ns	Maximum time by which data is available
T_{DH}	0.5 ns	—	Minimum hold duration

6.4 RGMII Characteristics

Figure 6-7 shows the RGMII AC timing diagram.

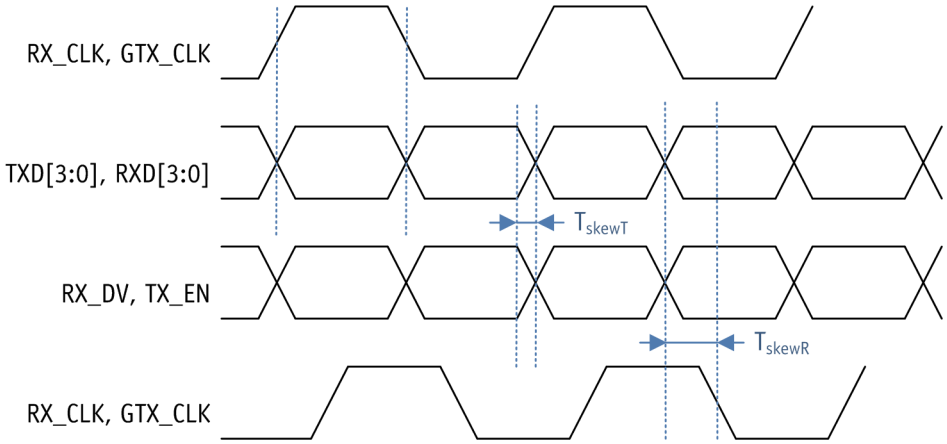

Figure 6-7. **RGMII AC Timing Diagram**

Table 6-5 shows the RGMII AC characteristics.

Table 6-5. **RGMII AC Characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
T_{skewT}	Data to clock output skew (at transmitter)	–500	0	500	ps
T_{skewR}	Data to clock output skew (at receiver)	1	—	—	ns
T_{cyc}	Clock cycle duration	7.2	8.0	8.8	ns
Duty_G	Duty cycle for Gigabit	45	50	55	%
Duty_T	Duty cycle for 10/100T	40	50	60	%
T_r/T_r	Rise/fall time	—	0.75	—	ns

7. Package Dimensions

The AR7242 14 mm x 14 mm LQFP-128 package drawings and dimensions are provided in Figure 7-1, Table 7-1, and Table 7-2.

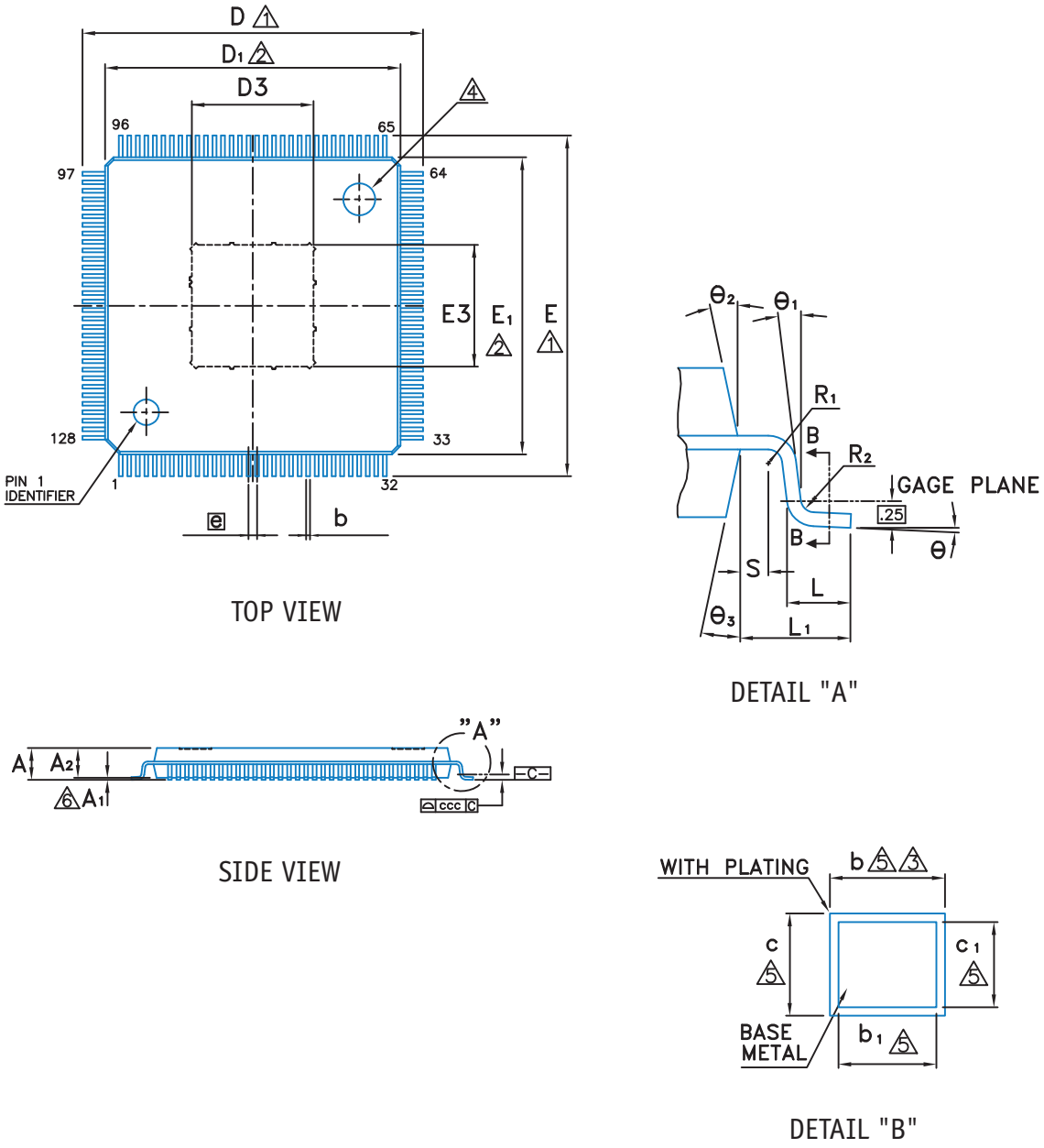

Figure 7-1. **Package Details**

Table 7-1. **Package Dimensions**

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	—	—	1.60	mm	—	—	0.063	inches
A1	0.05	—	—	mm	0.002	—	—	inches
A2	1.35	1.40	1.45	mm	0.053	0.055	0.057	inches
b	0.13	0.18	0.23	mm	0.005	0.007	0.009	inches
b1	0.13	0.16	0.19	mm	0.005	0.006	0.007	inches
c	0.09	—	0.20	mm	0.004	—	0.008	inches
c1	0.09	—	0.16	mm	0.004	—	0.006	inches
D	15.85	16.00	16.15	mm	0.624	0.630	0.636	inches
D1	13.90	14.00	14.10	mm	0.547	0.551	0.555	inches
E	15.85	16.00	16.15	mm	0.624	0.630	0.636	inches
E1	13.90	14.00	14.10	mm	0.547	0.551	0.555	inches
e		0.40 BSC		mm		0.016 BSC		inches
L	0.45	0.60	0.75	mm	0.018	0.024	0.030	inches
L1		1.00 REF		mm		0.039 REF		inches
R1	0.08	—	—	mm	0.003	—	—	inches
R2	0.08	—	0.20	mm	0.003	—	0.008	inches
S	0.20	—	—	mm	0.008	—	—	inches
θ	0	3.5	7	°	0	3.5	7	°
θ1	0	—	—	°	0	—	—	°
θ2/θ3		12° TYP				12° TYP		
ccc		0.08		mm		0.003		inches

[1] To be determined at seating plane C.
[2] Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
[3] Dimension b does not include dambar protrusion. Dambar cannot be located on the lower radius of the foot.
[4] Exact shape of each corner is optional.
[5] These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
[6] A1 is defined as the distance from the seating plane to the lowest point of the package body.
[7] Controlling dimension: Millimeters
[8] Reference document: JEDEC MS-026.
[9] Special characteristics C class: ccc.

Table 7-2. **Exposed Pad Size**

L/F	Dimension	Unit	Dimension	Unit
D3/E3	5.72/5.46 REF	mm	0.225/0.215 REF	inches

8. Ordering Information

The order number AR7242-AH1A specifies a LQFP halogen-free standard-temperature version of the AR7242.

Document Number: MKG-14829 Ver. 2.0

Atheros Communications, Incorporated
1700 Technology Drive
San Jose, CA 95110
tel: 408.773.5200
fax: 408.773.9940
www.atheros.com