December 2008

AR7100: A Scalable, High Performance And Cost-Effective Network Processor Family

General Description

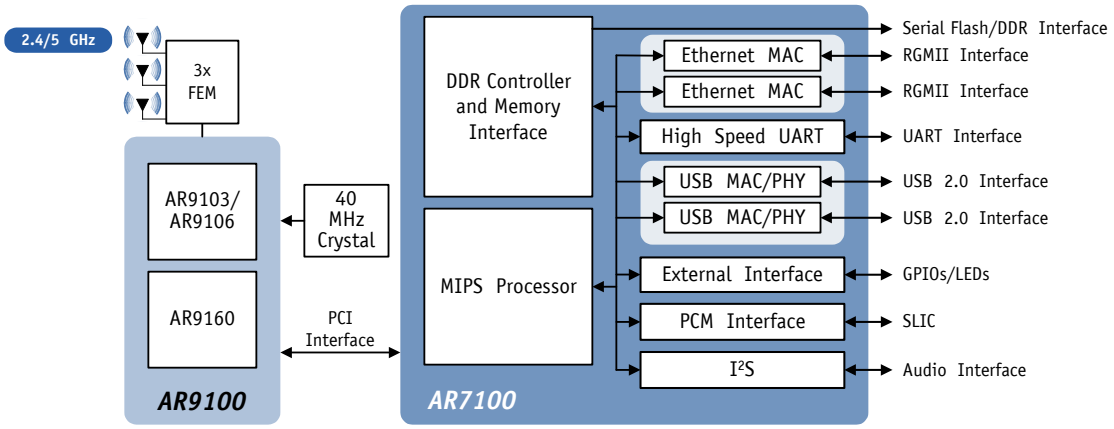
The Atheros AR7100 is a scalable, high performance and cost effective network processor family that allows efficient design of solutions addressing triple play services such as voice, video and data for home and enterprise access point, router and gateway applications. It includes a 32-bit MIPS processor, PCI host interface, two 802.3 Ethernet MACs with GMII/RGMII/RMII/MII interface, two USB 2.0 MAC/PHYs, a PCM interface for glueless SLIC support, external memory interface for serial Flash and DDR-SDRAM, a high-speed UART, I^2S interface, and GPIOs that can be used for LED controls.

The AR7100 network processor when paired with the AR9100 chipset family (AR9160 MAC/baseband processor and AR9106/AR9104/AR9103/AR9102/AR9101 radios) provides the best in class WLAN solution capable of supporting 802.11a/b/g/n standards.

Features

- Integrated MIPS 24K-family processor
- 300–680 MHz processor frequency:
  - AR7130, 300 MHz, Fast Ethernet version
  - AR7141, 400 MHz, supports Fast Ethernet and GB Ethernet
  - AR7161, 680 MHz, supports Fast Ethernet and GB Ethernet
- High Performance DDR memory controller (16- or 32-bit)
- Dual IEEE 802.3 Ethernet MAC supporting 10/100/1000 Mbps, full and half duplex and GMII/RGMII/RMII/MII interfaces
- Two-port USB 2.0 Host Controllers with built-in MAC/PHY
- UART for console support
- 32-bit, 33/66 MHz PCI 2.3 host interface supporting up to three client devices
- IEEE 1149.1 standard test access port and boundary scan architecture supported
- JTAG based debugging of the processor core supported
- 13 mm x 13 mm 384 TFBGA lead-free package
- Along with the Atheros AR9100 (MAC/BB and radio chips) family—Completes an all-CMOS solution for 802.11a/b/g/n WLANs, supporting extended range for worldwide operations

System Block Diagram



Revision History

Revision	Description of Changes
November 2008	Updated Section 5.3, DDR Register, offset address of PCI Window 0 to 7, DDR GE0, GE1, PCI and USB Flush registers.
June 2008	Updated registers section
February 2008	Added SPI registers, added pin direction and voltage information
January 2007	Updated RMII pin information
December 2006	Added register descriptions
November 2006	■ Updated the multiplexed Ethernet pin information ■ Updated the general description
September 2006	Preliminary information

Table of Contents

1. Pin Descriptions

This section contains both a package pinout (see Table 1-1 through Table 1-5) and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal

Table 1-1. **AR7100 Pin Assignments (1–12)**

	1	2	3	4	5	6	7	8	9	10	11	12
A	GND	VDD25	VDD25	DDR_DQ_27	DDR_DQ_25	DDR_DQS_3	DDR_DQM_2	DDR_DQ_23	DDR_DQ_22	DDR_DQ_21	DDR_DQ_19	DDR_DQ_17
B	GND	GND	GND	DDR_DQ_28	DDR_DQ_26	DDR_DQ_24	DDR_DQM_3	DDR_DQS_2	DDR_VREF	DDR_DQ_20	DDR_DQ_18	DDR_DQ_16
C	VDD25	VDD25	GND	VDD25	VDD25	VDD25	GND	GND	VDD12	VDD12	GND	VDD25
D	DDR_DQ_29	DDR_DQ_30	VDD25					VDD12	VDD12	VDD12	VDD12	
E	DDR_DQ_31	DDR_DQ_0	VDD25									
F	DDR_DQ_1	DDR_DQ_2	GND									
G	DDR_DQ_4	DDR_DQ_3	GND									
H	DDR_DQ_5	DDR_VREF	VDD25	VDD25				GND	GND	GND	GND	GND
J	DDR_DQ_7	DDR_DQ_6	VDD25	VDD25				GND	GND	GND	GND	GND
K	DDR_DQM_0	DDR_DQS_0	VDD25	VDD25				GND	GND	GND	GND	GND
L	DDR_DQS_1	DDR_DQM_1	VDD25	VDD25				GND	GND	GND	GND	GND
M	DDR_DQ_9	DDR_DQ_8	VDD25					GND	GND	GND	GND	GND
N	DDR_DQ_11	DDR_DQ_10	VDD25					GND	GND	GND	GND	GND
P	DDR_DQ_13	DDR_DQ_12	GND	VDD12				GND	GND	GND	GND	GND
R	DDR_CK_N	DDR_DQ_14	VDD12	VDD12				GND	GND	GND	GND	GND
T	DDR_CK_P	DDR_DQ_15	VDD12	VDD12				GND	GND	GND	GND	GND
U	DDR_A_12	DDR_VREF	DDR_CKE_L	VDD12				GND	GND	GND	GND	GND
V	DDR_A_11	DDR_BA_0	GND									
W	DDR_A_9	DDR_A_10	DDR_BA_1									
Y	DDR_A_8	DDR_A_0	DDR_WE_L									
AA	DDR_A_7	DDR_A_1	DDR_CAS_L					VDD33	VDD33	VDD33	VDD33	
AB	DDR_A_6	DDR_A_2	DDR_RAS_L	DDR_CS_L	UB0VSS33T	UBVDD33C	USB_ATEST	UB1VDD33T	VDD33	VDD33	ETH_27	ETH_24
AC	DDR_A_5	GND	DDR_A_3	UB0VSS33T	UB0VDD33T	UBVSS33C	UBXI	UB1VSS33T	UB1VSS33T	UB1VDD33T	ETH_26	ETH_23
AD	GND	DDR_A_4	UB0VDD33T	USB0_DP	USB0_DM	USB_REXT	UBXO	USB1_DM	USB1_DP	ETH_28	ETH_25	ETH_22

Table 1-2. **AR7100 Pin Assignments (13-24)**

	13	14	15	16	17	18	19	20	21	22	23	24
A	COLD_RST_L	SPI_MO_SI	SPI_CS_L	SYS_RST_L	TDO	GPIO_10[1]	GPIO_7[1]	GPIO_6[1]	GPIO_5[1]	GPIO_4[1]	GPIO_2[1]	GND
B	JTAG_ ENABLE	SPI_CLK	SPI_MI_SO	TRST_L	TDI	GPIO_11[1]	GPIO_8[1]	GPIO_3[1]	GPIO_1[1]	PCI_GNT1_L	GND	PCI_REQ1_ L
C	VDD25	VDD25	VDD25	VDD25	TMS	TCK	GPIO_9[1]	GPIO_0[1]	PCI_INT1_L	PCI_REQ2_L	PCI_AD_31	PCI_AD_30
D		VDD25	VDD25	VDD25	VDD25					PCI_GNT2_L	PCI_AD_29	PCI_AD_28
E										PCI_INT2_L	PCI_AD_27	PCI_AD_26
F										PCI_CBE3_L	PCI_AD_25	PCI_AD_24
G										PCI_SERR_L	PCI_REQ0_L	PCI_AD_23
H	GND	GND	GND	GND	GND				VDD12	PCI_RST_L	PCI_AD_21	PCI_AD_22
J	GND	GND	GND	GND	GND				VDD12	VDD12	PCI_AD_19	PCI_IDSEL
K	GND	GND	GND	GND	GND				VDD12	VDD12	PCI_AD_20	PCI_AD_18
L	GND	GND	GND	GND	GND				VDD12	PCI_CBE2_L	PCI_FRAME _L	PCI_AD_17
M	GND	GND	GND	GND	GND					PCI_TRDY_L	PCI_CLK_ OUT	PCI_IRDY_ L
N	GND	GND	GND	GND	GND					PCI_DEVSEL _L	PCI_INT0_L	PCI_CLK_I N
P	GND	GND	GND	GND	GND				VDD33	PCI_PERR_L	PCI_STOP_L	PCI_GNT0_ L
R	GND	GND	GND	GND	GND				VDD33	VDD33	PCI_AD_16	REF_CLK
T	GND	GND	GND	GND	GND				VDD33	VDD33	PCI_CBE1_L	PCI_PAR
U	GND	GND	GND	GND	GND				VDD33	NC	NC	PLL0_ VDD33
V										NC	PLL1_ VDD33	NC
W										PCI_AD_15	NC	NC
Y										PCI_AD_8	PCI_AD_13	PCI_AD_14
AA		VDD12	VDD12	VDD12	VDD12					PCI_AD_6	PCI_AD_10	PCI_AD_12
AB	ETH_21[1]	ETH_18[1]	VDD12	VDD12	ETH_11[1]	ETH_8[1]	ETH_5[1]	ETH_2[1]	PCI_AD_0	PCI_AD_3	PCI_CBE0_L	PCI_AD_11
AC	ETH_20[1]	ETH_17[1]	ETH_15[1]	ETH_13[1]	ETH_10[1]	ETH_7[1]	ETH_4[1]	ETH_1[1]	PCI_AD_2	PCI_AD_5	GND	PCI_AD_9
AD	ETH_19[1]	ETH_16[1]	ETH_14[1]	ETH_12[1]	ETH_9[1]	ETH_6[1]	ETH_3[1]	ETH_0[1]	PCI_AD_1	PCI_AD_4	PCI_AD_7	GND

[1]This pin is multiplexed. See Table 1-3

Table 1-3 shows the multiplexed Ethernet pins.

Table 1-3. **Multiplexed Ethernet Pins**

Ethernet	Pin	GMII	RGMII+RGMII	MII+RMII[1]	RMII+RMII[1]	Common Ethernet
ETH_0	AD20	GMII_COL	RGM1_TXCTL	MII_COL	—	—
ETH_1	AC20	GMII_CRS	RGM1_TXCLK	MII_CRS	—	—
ETH_2	AB20	GMII_RXDV	RGM0_RXCTL	MII_RXDV	RM0_RXCTL	—
ETH_3	AD19	GMII_RXERR	RGM1_RXCTL	MII_RXERR	—	—
ETH_4	AC19	GMII_TXDV	RGM0_TXCTL	MII_TXDV	RM0_TXCTL	—
ETH_5	AB19	GMII_TXERR	RGM1_RXCLK	MII_TXERR	—	—
ETH_6	AD18	GMII_RXCLK	RGM0_RXCLK	MII_RXCLK	RM0_CLK	—
ETH_7	AC18	GMII_TXCLK	RGM0_TXCLK	MII_TXCLK	—	—
ETH_8	AB18	MII_RXD_0	RGM0_RXD_0	MII_RXD_0	RM0_RXD_0	—
ETH_9	AD17	GMII_RXD_1	RGM0_RXD_1	MII_RXD_1	RM0_RXD_1	—
ETH_10	AC17	GMII_RXD_2	RGM0_RXD_2	MII_RXD_2	—	—
ETH_11	AB17	GMII_RXD_3	RGM0_RXD_3	MII_RXD_3	—	—
ETH_12	AD16	GMII_RXD_4	RGM1_RXD_0	RMII_RXD_0	RM1_RXD_0	—
ETH_13	AC16	GMII_RXD_5	RGM1_RXD_1	RMII_RXD_1	RM1_RXD_1	—
ETH_14	AD15	GMII_RXD_6	RGM1_RXD_2	RMII_RXC	RM1_RXCTL	—
ETH_15	AC15	GMII_RXD_7	RGM1_RXD_3	—	—	—
ETH_16	AD14	GMII_TXD_0	RGM0_TXD_0	MII_TXD_0	RM0_TXD_0	—
ETH_17	AC14	GMII_TXD_1	RGM0_TXD_1	MII_TXD_1	RM0_TXD_1	—
ETH_18	AB14	GMII_TXD_2	RGM0_TXD_2	MII_TXD_2	—	—
ETH_19	AD13	GMII_TXD_3	RGM0_TXD_3	MII_TXD_3	—	—
ETH_20	AC13	GMII_TXD_4	RGM1_TXD_0	RMII_TXD_0	RM1_TXD_0	—
ETH_21	AB13	GMII_TXD_5	RGM1_TXD_1	RMII_TXD_1	RM1_TXD_1	—
ETH_22	AD12	GMII_TXD_6	RGM1_TXD_2	RMII_TXC	RM1_TXCTL	—
ETH_23	AC12	GMII_TXD_7	RGM1_TXD_3	RMII_CLK	RM1_CLK	—
ETH_24	AB12	—	—	—	—	ETH_CLK
ETH_25	AD11	—	—	—	—	ETH_MDC
ETH_26	AC11	—	—	—	—	ETH_MDIO
ETH_27	AB11	—	—	—	—	ETH0_RESET_L
ETH_28	AD10	—	—	—	—	ETH1_RESET_L

[1]The AR7130 supports only MII+RMII and RMII+RMII modes. The AR7141 and AR7161 support all modes.

Table 1-4 shows the multiplexed GPIO pins.

Table 1-4. **Multiplexed GPIO Pins**

GPIO	Pin	UART/I^{2}S/Serial Interface
GPIO_0	C20	SI_CS1_L
GPIO_1	B21	SI_CS2_L
GPIO_2	A23	DRA
GPIO_3	B20	DXA
GPIO_4	A22	PCLK
GPIO_5	A21	FS

Table 1-4. **Multiplexed GPIO Pins (continued)**

GPIO	Pin	UART/I^{2}S/Serial Interface
GPIO_6	A20	I2S_SDO
GPIO_7	A19	I2S_WS
GPIO_8	B19	I2S_SCK
GPIO_9	C19	UART_SIN
GPIO_10	A18	UART_SOUT
GPIO_11	B18	I2S_SDI

Table 1-5 and Table 1-6 provide the signal-to-pin relationship information for the AR7100.

Table 1-5. **Signal-to-Pin Relationships**

Signal Name	Pin	Direction	Pull-Up/ Pull-Down	Voltage	Description
Reset and Reference Clock					
COLD_RST_L	A13	I	None	3.3 V	Reset entire chip
SYS_RST_L	A16	O	None	3.3 V	System reset for external devices
REF_CLK	R24	I	None	3.3 V	40 MHz reference clock
GPIO					
GPIO_0[1]	C20	I/O	None	3.3 V	General purpose I/O pins, 8 mA drive strength
GPIO_1[1]	B21	I/O	None	3.3 V	
GPIO_2[1]	A23	I/O	None	3.3 V	
GPIO_3[1]	B20	I/O	None	3.3 V	
GPIO_4[1]	A22	I/O	None	3.3 V	
GPIO_5[1]	A21	I/O	None	3.3 V	
GPIO_6[1]	A20	I/O	None	3.3 V	
GPIO_7[1]	A19	I/O	None	3.3 V	
GPIO_8[1]	B19	I/O	None	3.3 V	
GPIO_9[1]	C19	I/O	None	3.3 V	
GPIO_10[1]	A18	I/O	None	3.3 V	
GPIO_11[1]	B18	I/O	None	3.3 V	
I^2S					
I2S_SCK[1]	B19	O	None	3.3 V	Clock
I2S_SDI[1]	B18	I	None	3.3 V	Serial audio data in
I2S_SDO[1]	A20	O	None	3.3 V	Serial audio data out
I2S_WS[1]	A19	O	None	3.3 V	Word select for stereo
					0 Right
					1 Left
JTAG Interface					
JTAG_ENABLE	B13	I	None	3.3 V	JTAG interface enable
TDI	B17	I	None	3.3 V	JTAG data input
TDO	A17	O	None	3.3 V	JTAG data output
TMS	C17	I	None	3.3 V	JTAG mode select
TCK	C18	I	None	3.3 V	JTAG Clock
TRST_L	B16	I	None	3.3 V	JTAG reset
PCM					
DRA[1]	A23	O	None	3.3 V	Data transmitted from the AR7100 to the SLIC
DXA[1]	B20	I	None	3.3 V	Data transmitted from the SLIC to the AR7100
FS[1]	A21	O	None	3.3 V	Frame sync
PCLK[1]	A22	O	None	3.3 V	Clock

Table 1-5. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Pull-Up/ Pull-Down	Voltage	Description
UART					
UART_SIN[1]	C19	I	None	3.3 V	Serial data in
UART_SOUT[1]	A18	O	None	3.3 V	Serial data out
SPI Interface					
SPI_CLK	B14	O	None	3.3 V	Serial interface clock
SI_CS1_L[1]	C20	O	None	3.3 V	Optional serial interface chip select, for controlling external serial devices
SI_CS2_L[1]	B21	O	None	3.3 V	Optional serial interface chip select, for controlling external serial devices
SPI_CS_L	A15	O	None	3.3 V	SPI chip select
SPI_MI_SO	B15	I	None	3.3 V	Data transmitted from an external device to the AR7100
SPI_MO_SI	A14	O	None	3.3 V	Data transmitted from the AR7100 to an external device
DDR					
DDR_A_0	Y2	O	None	2.5 V	DDR address
DDR_A_1	AA2	O	None	2.5 V	
DDR_A_2	AB2	O	None	2.5 V	
DDR_A_3	AC3	O	None	2.5 V	
DDR_A_4	AD2	O	None	2.5 V	
DDR_A_5	AC1	O	None	2.5 V	
DDR_A_6	AB1	O	None	2.5 V	
DDR_A_7	AA1	O	None	2.5 V	
DDR_A_8	Y1	O	None	2.5 V	
DDR_A_9	W1	O	None	2.5 V	
DDR_A_10	W2	O	None	2.5 V	
DDR_A_11	V1	O	None	2.5 V	
DDR_A_12	U1	O	None	2.5 V	
DDR_BA_0	V2	O	None	2.5 V	DDR bank address
DDR_BA_1	W3	O	None	2.5 V	
DDR_CAS_L	AA3	O	None	2.5 V	DDR column address strobe
DDR_RAS_L	AB3	O	None	2.5 V	DDR row address strobe
DDR_CK_N	R1	O	None	2.5 V	DDR clock
DDR_CK_P	T1	O	None	2.5 V	
DDR_CKE_L	U3	O	None	2.5 V	DDR clock enable
DDR_CS_L	AB4	O	None	2.5 V	DDR chip select

Table 1-5. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Pull-Up/ Pull-Down	Voltage	Description
DDR_DQ_0	E2	I/O	None	2.5 V	DDR data bus
DDR_DQ_1	F1	I/O	None	2.5 V	
DDR_DQ_2	F2	I/O	None	2.5 V	
DDR_DQ_3	G2	I/O	None	2.5 V	
DDR_DQ_4	G1	I/O	None	2.5 V	
DDR_DQ_5	H1	I/O	None	2.5 V	
DDR_DQ_6	J2	I/O	None	2.5 V	
DDR_DQ_7	J1	I/O	None	2.5 V	
DDR_DQ_8	M2	I/O	None	2.5 V	
DDR_DQ_9	M1	I/O	None	2.5 V	
DDR_DQ_10	N2	I/O	None	2.5 V	
DDR_DQ_11	N1	I/O	None	2.5 V	
DDR_DQ_12	P2	I/O	None	2.5 V	
DDR_DQ_13	P1	I/O	None	2.5 V	
DDR_DQ_14	R2	I/O	None	2.5 V	
DDR_DQ_15	T2	I/O	None	2.5 V	
DDR_DQ_16	B12	I/O	None	2.5 V	
DDR_DQ_17	A12	I/O	None	2.5 V	
DDR_DQ_18	B11	I/O	None	2.5 V	
DDR_DQ_19	A11	I/O	None	2.5 V	
DDR_DQ_20	B10	I/O	None	2.5 V	
DDR_DQ_21	A10	I/O	None	2.5 V	
DDR_DQ_22	A9	I/O	None	2.5 V	
DDR_DQ_23	A8	I/O	None	2.5 V	
DDR_DQ_24	B6	I/O	None	2.5 V	
DDR_DQ_25	A5	I/O	None	2.5 V	
DDR_DQ_26	B5	I/O	None	2.5 V	
DDR_DQ_27	A4	I/O	None	2.5 V	
DDR_DQ_28	B4	I/O	None	2.5 V	
DDR_DQ_29	D1	I/O	None	2.5 V	
DDR_DQ_30	D2	I/O	None	2.5 V	
DDR_DQ_31	E1	I/O	None	2.5 V	
DDR_DQM_0	K1	O	None	2.5 V	DDR data mask
DDR_DQM_1	L2	O	None	2.5 V	
DDR_DQM_2	A7	O	None	2.5 V	
DDR_DQM_3	B7	O	None	2.5 V	
DDR_DQS_0	K2	I/O	None	2.5 V	DDR data strobe
DDR_DQS_1	L1	I/O	None	2.5 V	
DDR_DQS_2	B8	I/O	None	2.5 V	
DDR_DQS_3	A6	I/O	None	2.5 V	
DDR_VREF	B9, H2, U2		None	1.25 V	DDR voltage reference
DDR_WE_L	Y3	O	None	2.5 V	DDR write enable

Table 1-5. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Pull-Up/ Pull-Down	Voltage	Description
PCI					
PCI_AD_0	AB21	I/O	None	3.3 V	PCI address/data bus
PCI_AD_1	AD21	I/O	None	3.3 V	
PCI_AD_2	AC21	I/O	None	3.3 V	
PCI_AD_3	AB22	I/O	None	3.3 V	
PCI_AD_4	AD22	I/O	None	3.3 V	
PCI_AD_5	AC22	I/O	None	3.3 V	
PCI_AD_6	AA22	I/O	None	3.3 V	
PCI_AD_7	AD23	I/O	None	3.3 V	
PCI_AD_8	Y22	I/O	None	3.3 V	
PCI_AD_9	AC24	I/O	None	3.3 V	
PCI_AD_10	AA23	I/O	None	3.3 V	
PCI_AD_11	AB24	I/O	None	3.3 V	
PCI_AD_12	AA24	I/O	None	3.3 V	
PCI_AD_13	Y23	I/O	None	3.3 V	
PCI_AD_14	Y24	I/O	None	3.3 V	
PCI_AD_15	W22	I/O	None	3.3 V	
PCI_AD_16	R23	I/O	None	3.3 V	
PCI_AD_17	L24	I/O	None	3.3 V	
PCI_AD_18	K24	I/O	None	3.3 V	
PCI_AD_19	J23	I/O	None	3.3 V	
PCI_AD_20	K23	I/O	None	3.3 V	
PCI_AD_21	H23	I/O	None	3.3 V	
PCI_AD_22	H24	I/O	None	3.3 V	
PCI_AD_23	G24	I/O	None	3.3 V	
PCI_AD_24	F24	I/O	None	3.3 V	
PCI_AD_25	F23	I/O	None	3.3 V	
PCI_AD_26	E24	I/O	None	3.3 V	
PCI_AD_27	E23	I/O	None	3.3 V	
PCI_AD_28	D24	I/O	None	3.3 V	
PCI_AD_29	D23	I/O	None	3.3 V	
PCI_AD_30	C24	I/O	None	3.3 V	
PCI_AD_31	C23	I/O	None	3.3 V	
PCI_CBE0_L	AB23	I/O	None	3.3 V	PCI command/byte enable bus
PCI_CBE1_L	T23	I/O	None	3.3 V	
PCI_CBE2_L	L22	I/O	None	3.3 V	
PCI_CBE3_L	F22	I/O	None	3.3 V	
PCI_CLK_IN	N24	I	None	3.3 V	PCI clock input
PCI_CLK_OUT	M23	O	None	3.3 V	PCI clock output
PCI_DEVSEL_L	N22	I/O	None	3.3 V	PCI device select
PCI_IDSEL	J24	I	None	3.3 V	PCI ID select
PCI_FRAME_L	L23	I/O	None	3.3 V	PCI frame

Table 1-5. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Pull-Up/ Pull-Down	Voltage	Description
PCI_GNT0_L	P24	O	None	3.3 V	PCI arbitration grant
PCI_GNT1_L	B22	O	None	3.3 V	
PCI_GNT2_L	D22	O	None	3.3 V	
PCI_INT0_L	N23	I	None	3.3 V	PCI interrupts
PCI_INT1_L	C21	I	None	3.3 V	
PCI_INT2_L	E22	I	None	3.3 V	
PCI_IRDY_L	M24	I/O	None	3.3 V	PCI initiator ready
PCI_TRDY_L	M22	I/O	None	3.3 V	PCI target ready
PCI_PAR	T24	I/O	None	3.3 V	PCI address/data parity
PCI_PERR_L	P22	I/O	None	3.3 V	PCI parity error
PCI_SERR_L	G22	I/O	None	3.3 V	PCI sequence error
PCI_REQ0_L	G23	I	None	3.3 V	PCI arbitration request
PCI_REQ1_L	B24	I	None	3.3 V	
PCI_REQ2_L	C22	I	None	3.3 V	
PCI_RST_L	H22	O	None	3.3 V	PCI reset
PCI_STOP_L	P23	I/O	None	3.3 V	PCI stop
USB					
USB0_DM	AD5	I/O	None	3.3 V	USB0 port
USB0_DP	AD4	I/O	None	3.3 V	USB0 port
UB0VDD33T	AC5, AD3		None	3.3 V	USB0 port power
UB0VSS33T	AB5, AC4		None	3.3 V	USB0 port ground
USB1_DM	AD8	I/O	None	3.3 V	USB1 port
USB1_DP	AD9	I/O	None	3.3 V	USB1 port
UB1VDD33T	AB8, AC10		None	3.3 V	USB1 port power
UB1VSS33T	AC8, AC9		None	3.3 V	USB1 port ground
UBVDD33C	AB6		None	3.3 V	USB PLL common power
UBVSS33C	AC6		None	3.3 V	USB PLL common ground
UBXI	AC7	I	None	3.3 V	USB crystal in, 12 MHz
UBXO	AD7	O	None	3.3 V	USB crystal out
USB_REXT	AD6	IA	None	3.3 V	Bias resistor, connect a 3.4K ±1% resistor in series to ground
USB_ATEST	AB7	OA	None	3.3 V	Analog test output, should be left open

Table 1-5. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Pull-Up/ Pull-Down	Voltage	Description
Ethernet					
ETH_0[1]	AD20	I/O	None	3.3 V	Ethernet Interface signals. Can be configured to support 2xRGMII or 1xGMII, or 2xRMII or 1xMII+RMII.
ETH_1[1]	AC20	I/O	None	3.3 V	
ETH_2[1]	AB20	I	None	3.3 V	
ETH_3[1]	AD19	I	None	3.3 V	
ETH_4[1]	AC19	O	None	3.3 V	
ETH_5[1]	AB19	I/O	None	3.3 V	
ETH_6[1]	AD18	I	None	3.3 V	
ETH_7[1]	AC18	I/O	None	3.3 V	
ETH_8[1]	AB18	I	None	3.3 V	
ETH_9[1]	AD17	I	None	3.3 V	
ETH_10[1]	AC17	I	None	3.3 V	
ETH_11[1]	AB17	I	None	3.3 V	
ETH_12[1]	AD16	I	None	3.3 V	
ETH_13[1]	AC16	I	None	3.3 V	
ETH_14[1]	AD15	I	None	3.3 V	
ETH_15[1]	AC15	I	None	3.3 V	
ETH_16[1]	AD14	O	None	3.3 V	
ETH_17[1]	AC14	O	None	3.3 V	
ETH_18[1]	AB14	O	None	3.3 V	
ETH_19[1]	AD13	O	None	3.3 V	
ETH_20[1]	AC13	O	None	3.3 V	
ETH_21[1]	AB13	O	None	3.3 V	
ETH_22[1]	AD12	O	None	3.3 V	
ETH_23[1]	AC12	I/O	None	3.3 V	
ETH_24	AB12	O	None	3.3 V	
ETH_25	AD11	O	None	3.3 V	
ETH_26	AC11	I/O	None	3.3 V	
ETH_27	AB11	O	None	3.3 V	
ETH_28	AD10	O	None	3.3 V	

[1]This pin is multiplexed. See Table 1-3.

Table 1-6. **Signal-to-Pin Relationships (continued)**

Signal Name	ETH Pin	Pin	Direction	Pull-Up/ Pull-Down	Voltage	Description
GMII						
GMII_COL[1]	ETH_0	AD20	I	None	3.3 V	GMII collision
GMII_CRS[1]	ETH_1	AC20	I	None	3.3 V	GMII carrier sense
GMII_RXCLK[1]	ETH_6	AD18	I	None	3.3 V	GMII receive clock
GMII_RXD_0[1]	ETH_8	AB18	I	None	3.3 V	GMII receive data
GMII_RXD_1[1]	ETH_9	AD17	I	None	3.3 V	
GMII_RXD_2[1]	ETH_10	AC17	I	None	3.3 V	
GMII_RXD_3[1]	ETH_11	AB17	I	None	3.3 V	
GMII_RXD_4[1]	ETH_12	AD16	I	None	3.3 V	
GMII_RXD_5[1]	ETH_13	AC16	I	None	3.3 V	
GMII_RXD_6[1]	ETH_14	AD15	I	None	3.3 V	
GMII_RXD_7[1]	ETH_15	AC15	I	None	3.3 V	
GMII_RXDV[1]	ETH_2	AB20	I	None	3.3 V	GMII receive data valid
GMII_RXERR[1]	ETH_3	AD19	I	None	3.3 V	GMII receive error
GMII_TXCLK[1]	ETH_7	AC18	O	None	3.3 V	GMII transmit clock
GMII_TXD_0[1]	ETH_16	AD14	O	None	3.3 V	GMII transmit data
GMII_TXD_1[1]	ETH_17	AC14	O	None	3.3 V	
GMII_TXD_2[1]	ETH_18	AB14	O	None	3.3 V	
GMII_TXD_3[1]	ETH_19	AD13	O	None	3.3 V	
GMII_TXD_4[1]	ETH_20	AC13	O	None	3.3 V	
GMII_TXD_5[1]	ETH_21	AB13	O	None	3.3 V	
GMII_TXD_6[1]	ETH_22	AD12	O	None	3.3 V	
GMII_TXD_7[1]	ETH_23	AC12	O	None	3.3 V	
GMII_TXDV[1]	ETH_4	AC19	O	None	3.3 V	GMII transmit data valid
GMII_TXERR[1]	ETH_5	AB19	O	None	3.3 V	GMII transmit error

Table 1-6. **Signal-to-Pin Relationships (continued)**

Signal Name	ETH Pin	Pin	Direction	Pull-Up/ Pull-Down	Voltage	Description
MII+RMII						
MII_COL[1]	ETH_0	AD20	I	None	3.3 V	MII collision
MII_CRS[1]	ETH_1	AC20	I	None	3.3 V	MII carrier sense
MII_RXCLK[1]	ETH_6	AD18	I	None	3.3 V	MII receive clock
MII_RXD_0[1]	ETH_8	AB18	I	None	3.3 V	MII receive data
MII_RXD_1[1]	ETH_9	AD17	I	None	3.3 V	
MII_RXD_2[1]	ETH_10	AC17	I	None	3.3 V	
MII_RXD_3[1]	ETH_11	AB17	I	None	3.3 V	
MII_RXDV[1]	ETH_2	AB20	I	None	3.3 V	MII receive data valid
MII_RXERR[1]	ETH_3	AD19	I	None	3.3 V	MII receive error
MII_TXCLK[1]	ETH_7	AC18	I	None	3.3 V	MII transmit clock
MII_TXD_0[1]	ETH_16	AD14	O	None	3.3 V	MII transmit data
MII_TXD_1[1]	ETH_17	AC14	O	None	3.3 V	
MII_TXD_2[1]	ETH_18	AB14	O	None	3.3 V	
MII_TXD_3[1]	ETH_19	AD13	O	None	3.3 V	
MII_TXDV[1]	ETH_4	AC19	O	None	3.3 V	MII transmit data valid
MII_TXERR[1]	ETH_5	AB19	O	None	3.3 V	MII transmit error
RMII_RXC[1]	ETH_14	AD15	I	None	3.3 V	RMII receive control
RMII_RXD_0[1]	ETH_12	AD16	I	None	3.3 V	RMII receive data
RMII_RXD_1[1]	ETH_13	AC16	I	None	3.3 V	
RMII_CLK[1]	ETH_23	AC12	I	None	3.3 V	RMII clock
RMII_TXC[1]	ETH_22	AD12	O	None	3.3 V	RMII transmit control
RMII_TXD_0[1]	ETH_20	AC13	O	None	3.3 V	RMII transmit data
RMII_TXD_1[1]	ETH_21	AB13	O	None	3.3 V	

Table 1-6. **Signal-to-Pin Relationships (continued)**

Signal Name	ETH Pin	Pin	Direction	Pull-Up/ Pull-Down	Voltage	Description
RGMII+RGMII						
RGM0_RXCLK[1]	ETH_6	AD18	I	None	3.3 V	RGMII0 receive clock
RGM0_RXCTL[1]	ETH_2	AB20	I	None	3.3 V	RGMII0 receive control
RGM0_RXD_0[1]	ETH_8	AB18	I	None	3.3 V	RGMII0 receive data
RGM0_RXD_1[1]	ETH_9	AD17	I	None	3.3 V	
RGM0_RXD_2[1]	ETH_10	AC17	I	None	3.3 V	
RGM0_RXD_3[1]	ETH_11	AB17	I	None	3.3 V	
RGM0_TXCLK[1]	ETH_7	AC18	O	None	3.3 V	RGMII0 transmit clock
RGM0_TXCTL[1]	ETH_4	AC19	O	None	3.3 V	RGMII0 transmit control
RGM0_TXD_0[1]	ETH_16	AD14	O	None	3.3 V	RGMII0 transmit data
RGM0_TXD_1[1]	ETH_17	AC14	O	None	3.3 V	
RGM0_TXD_2[1]	ETH_18	AB14	O	None	3.3 V	
RGM0_TXD_3[1]	ETH_19	AD13	O	None	3.3 V	
RGM1_RXCLK[1]	ETH_5	AB19	I	None	3.3 V	RGMII1 receive clock
RGM1_RXCTL[1]	ETH_3	AD19	I	None	3.3 V	RGMII1 receive control
RGM1_RXD_0[1]	ETH_12	AD16	I	None	3.3 V	RGMII1 receive data
RGM1_RXD_1[1]	ETH_13	AC16	I	None	3.3 V	
RGM1_RXD_2[1]	ETH_14	AD15	I	None	3.3 V	
RGM1_RXD_3[1]	ETH_15	AC15	I	None	3.3 V	
RGM1_TXCLK[1]	ETH_1	AC20	O	None	3.3 V	RGMII1 transmit clock
RGM1_TXCTL[1]	ETH_0	AD20	O	None	3.3 V	RGMII1 transmit control
RGM1_TXD_0[1]	ETH_20	AC13	O	None	3.3 V	RGMII1 transmit data
RGM1_TXD_1[1]	ETH_21	AB13	O	None	3.3 V	
RGM1_TXD_2[1]	ETH_22	AD12	O	None	3.3 V	
RGM1_TXD_3[1]	ETH_23	AC12	O	None	3.3 V	

Table 1-6. **Signal-to-Pin Relationships (continued)**

Signal Name	ETH Pin	Pin	Direction	Pull-Up/ Pull-Down	Voltage	Description
RMII+RMII						
RM0_CLK[1]	ETH_6	AD18	I	None	3.3 V	RMII0 clock
RM0_RXCTL[1]	ETH_2	AB20	I	None	3.3 V	RMII0 receive control
RM0_RXD_0[1]	ETH_8	AB18	I	None	3.3 V	RMII0 receive data
RM0_RXD_1[1]	ETH_9	AD17	I	None	3.3 V	
RM0_TXD_0[1]	ETH_16	AD14	O	None	3.3 V	RMII0 transmit data
RM0_TXD_1[1]	ETH_17	AC14	O	None	3.3 V	
RM0_TXCTL[1]	ETH_4	AC19	O	None	3.3 V	RMII0 transmit control
RM1_CLK[1]	ETH_23	AC12	I	None	3.3 V	RMII1 clock
RM1_RXCTL[1]	ETH_14	AD15	I	None	3.3 V	RMII1 receive control
RM1_RXD_0[1]	ETH_12	AD16	I	None	3.3 V	RMII1 receive data
RM1_RXD_1[1]	ETH_13	AC16	I	None	3.3 V	
RM1_TXCTL[1]	ETH_22	AD12	O	None	3.3 V	RMII1 transmit control
RM1_TXD_0[1]	ETH_20	AC13	O	None	3.3 V	RMII1 transmit data
RM1_TXD_1[1]	ETH_21	AB13	O	None	3.3 V	
Common Ethernet						
ETH_CLK	ETH_24	AB12	O	None	3.3 V	Reference clock to Ethernet PHY chips
ETH_MDC	ETH_25	AD11	O	None	3.3 V	Management control interface clock
ETH_MDIO	ETH_26	AC11	I/O	None	3.3 V	Management control interface data
ETH0_RESET_L	ETH_27	AB11	O	None	3.3 V	ETH0 PHY chip reset
ETH1_RESET_L	ETH_28	AD10	O	None	3.3 V	ETH1 PHY chip reset

Table 1-7. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Description
Power		
GND	A1, A24, B1, B2, B3, B23, C3, C7, C8, C11, F3, G3, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, K8, K9, K10, K11, K12, K13, K14, K15, K16, K17, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, P3, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, V3, AC2, AC23, AD1, AD24	Digital ground
PLL0_VDD33	U24	3.3 V for PLL0
PLL1_VDD33	V23	3.3 V for PLL1
VDD12	C9, C10, D8, D9, D10, D11, H21, J21, J22, K21, K22, L21, P4, R3, R4, T3, T4, U4, AA14, AA15, AA16, AA17, AB15, AB16	1.2 V
VDD25	A2, A3, C1, C2, C4, C5, C6, C12, C13, C14, C15, C16, D3, D14, D15, D16, D17, E3, H3, H4, J3, J4, K3, K4, L3, L4, M3, N3	2.5 V
VDD33	P21, R21, R22, T21, T22, U21, AA8, AA9, AA10, AA11, AB9, AB10	3.3 V
NC	U22, U23, V22, V24, W23, W24	No connection

2. Functional Description

Figure 2-1 illustrates the AR7100 functional block diagram.

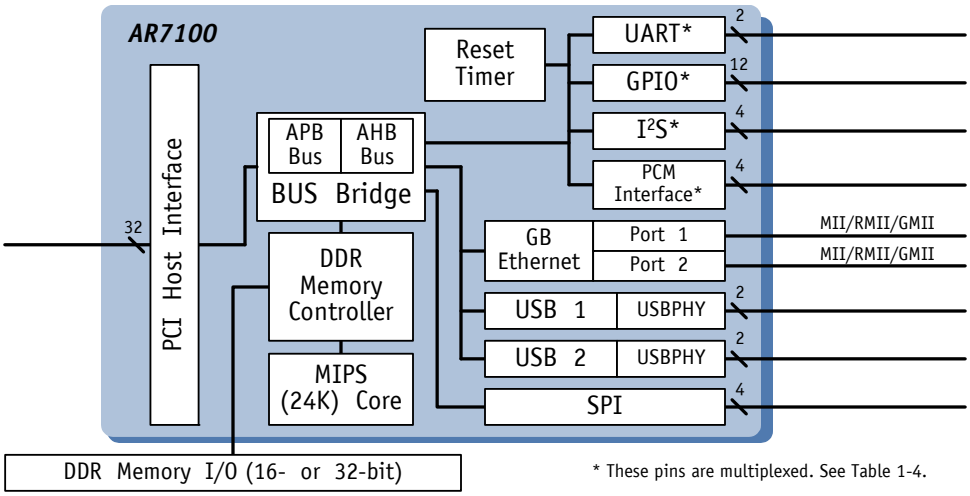


Figure 2-1. **Functional Block Diagram**

The AR7100 is comprised of several internal functional blocks. Table 2-1 summarizes these functional blocks.

Table 2-1. **Functional Blocks**

Block	Description	
32-bit PCI	Supports both 33 MHz and 66 MHz; the PCI is three devices with one interrupt line per device and supports PCI host only	
Bus Bridge	High-speed peripheral bus; the APB connects peripherals such as GPIO, PCM, and UART to the bus bridge. The AHB connects high-performance peripheral interfaces such as the GB Ethernet and USB interfaces to the bus bridge.	
CPU	An embedded 24 K MIPS processor with up to 400 MHz CPU speed. It has a 64 K four-way set associative instruction cache, 32 K four-way set associative data cache, single-cycle multiply-accumulate, and MIPS32 and MIPS16 instruction sets. It supports non-blocking cached reads.	
DDR Interface	16-bit or 32-bit DDR memory interface; up to 400 Mbps/pin The dedicated point-to-point interface for the CPU and dedicated point-to-point interfaces for each external master device control write buffering at each interface. The DDR interface separates arbitration by bank, allowing efficient pipelined RAS/CAS/precharge scheduling. It also allows multiple reads from the processor to issue at full bandwidth.	
Ethernet	Single port	Configured as a single port: can support GMII, MII, RGMII, and RMII
	Two ports	Configured as two ports: can support MII+RMII, RGMII+RGMII, RGMII+RMII, or RMII+RMII (the AR7130 supports only MII+RMII and RMII+RMII)
I^2S	FIFO-based four-wire interface for speaker output	
PCM	FIFO-based four-wire interface for audio input/output to an external SLIC	
Reset	The timers and interrupts necessary to keep the processor running; reset and clock control for each block in the design	
Serial	One SPI chip select dedicated to an external flash for boot; two configurable chip selects that can use GPIOs for configuration of external components	
UART	16550 equivalent UART for debug/console	
USB	Two USB host ports; both support high speed (480 Mbps), full speed (11 Mbps), and low speed (1 Mbps) operation	

2.1 Address MAP

Figure 2-2 shows the AR7100 address space.

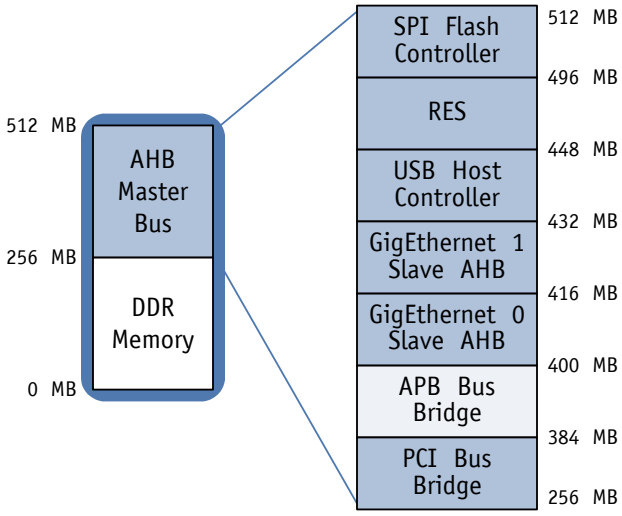


Figure 2-2. **Address Space**

Except for non-configuration accesses to DDR memory, all other devices on the AR7100 are accessed through the Atheros high-speed bus (AHB) bridge.

The address space is split into two 256-MB regions. The lower region maps to DDR memory and the upper region to the AHB bus bridge.

Table 2-2 describes the address space blocks.

Table 2-2. **Address Space**

Address Space	Description	
AHB Master Bus	The 256 MB region for AHB devices is divided into sixteen 16-MB windows.	
	PCI	The PCI range occupies a contiguous block of the lower eight windows. See the sections "PCI Address Space Offset for PCI Window 0 (PCI_WINDOW_0)" through "PCI Address Space Offset for PCI Window 7 (PCI_WINDOW_7)".
	APB Bridge	One 16-MB window of the AHB address space is devoted to an APB device mapper.
	The remaining windows are allocated to the slave ports of the two GB Ethernet MACs, the USB host controller, the SPI interface, and an APB bus bridge.	

2.2 Ethernet

The AR7100 supports up to two GB Ethernet ports as well as the MII, RMII, GMII, and RGMII interfaces. Table 2-3 shows the single- and dual-port configurations.

Table 2-3. **Port Configurations**

Number of Ports	Supported Interfaces
1	MII, RMII, GMII, and RGMII
2	MII+RMII, RGMII+RGMII, RGMII+RMII, or RMII+RMII

2.3 Ethernet Connection Diagrams

Figure 2-3 shows the RMII + RMII connection diagram.

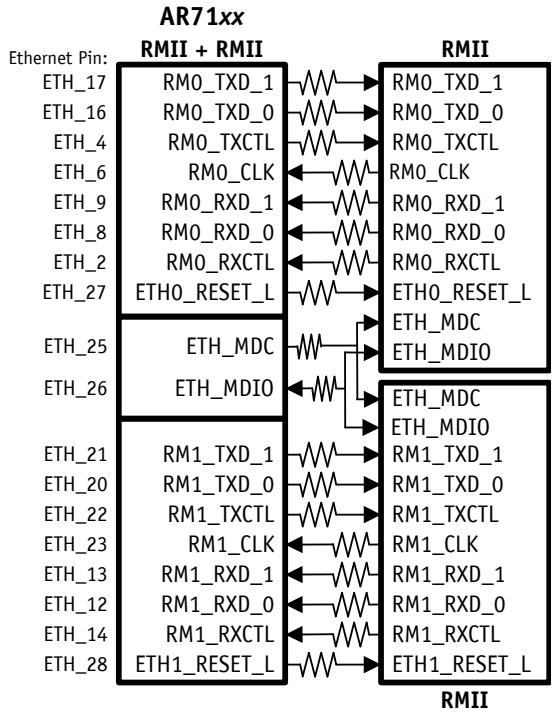


Figure 2-3. **RMII + RMII Connection Diagram**

Figure 2-4 shows the MII + RMII connection diagram.

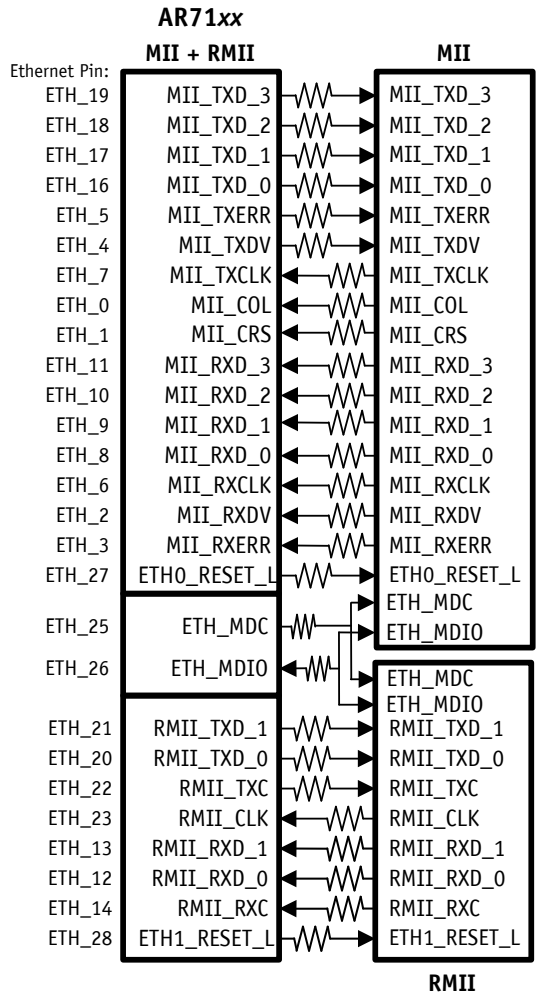


Figure 2-4. **MII + RMII Connection Diagram**

Figure 2-5 shows the RGMII + RGMII connection diagram.

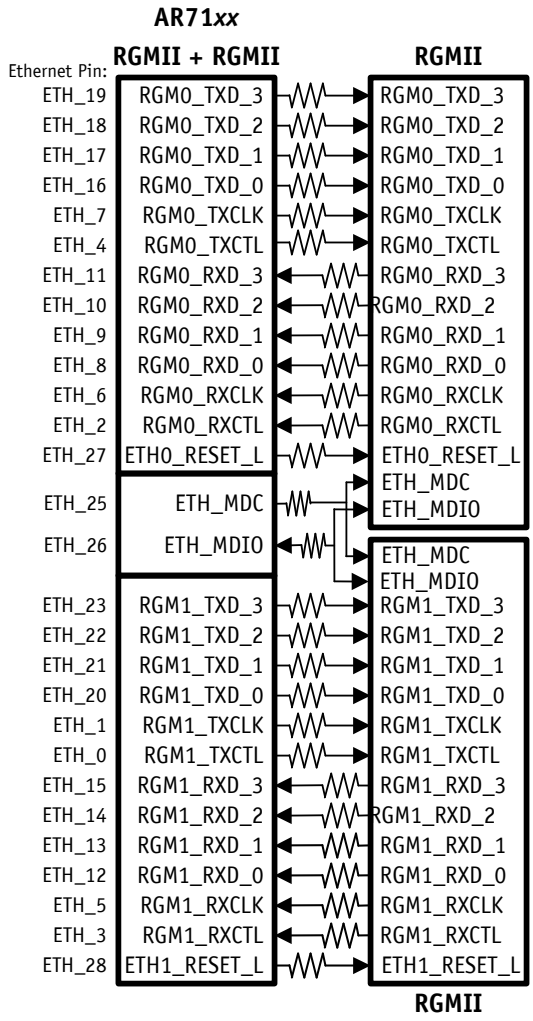


Figure 2-5. **RGMII + RGMII Connection Diagram**

Figure 2-6 shows the GMII PHY connections.

Note that due to ETH_7 re-use between the GMII and MII modes, the AR7100 cannot auto-negotiate between 10/100/1000 with many PHYs. RGMII is recommended for ports that require full 10/100/1000 functionality.

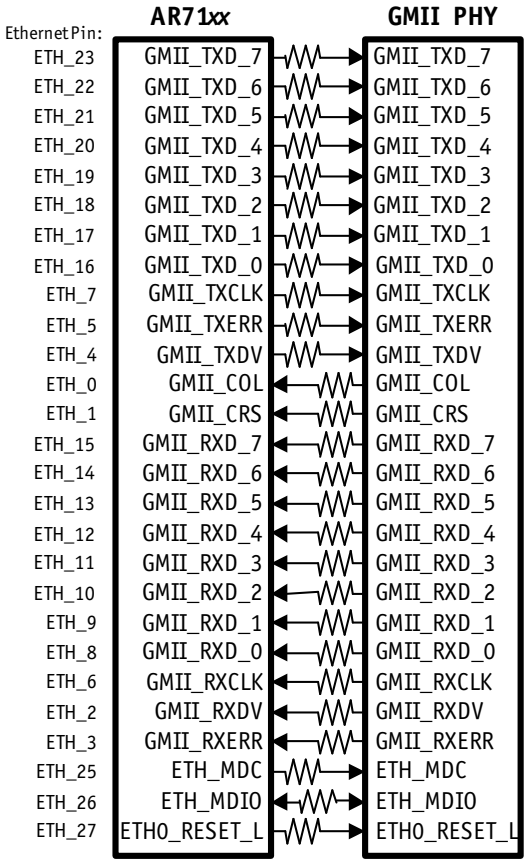


Figure 2-6. **GMII Connection Diagram**

Figure 2-7 shows the MII PHY connections.

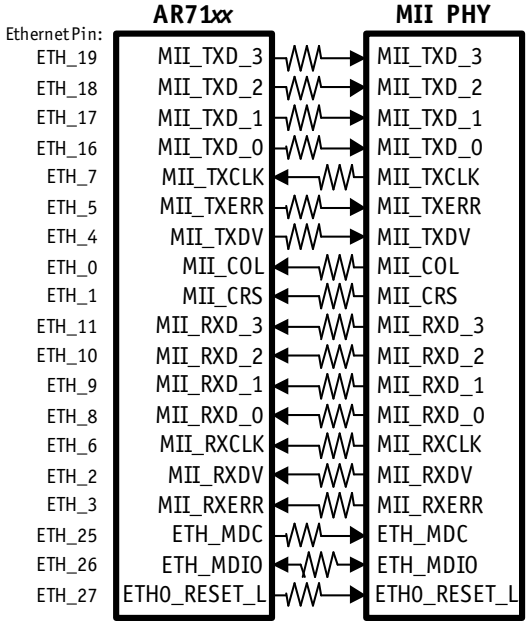


Figure 2-7. **MII Connection Diagram**

2.4 USB

USB is the Universal Serial Bus Interface for data exchange. The AR7100 supports an EHCI/OHCI USB 2.0 host interface with two high-speed ports. The USB UTMI PHY is also integrated into the chip. The USB Host controller registers are compliant with EHCI and OHCI specifications. All speeds (high-speed, full-speed, and low-speed) are supported on both ports.

2.5 Audio Interface

2.5.1 SLIC

SLIC is a four-wire interface for audio input/output to an external SLIC. The SLIC interface implements a PCM highway interface to an external SLIC device. The AR7100 can send and receive up to two channels of time-multiplexed PCM voice data over the PCM highway. The specific time slot can be programmed for each channel separately and can range from 0 to 128. The PCM highway includes a Framesync signal. A Framesync pulse is issued on this pin every 125 µs to give a basic voice sample rate of 8 KHz for each channel, and each channel can send or receive an 8-bit (compressed A law or µ law) sample during every frame period.

The voice sample clock PCLK ranges from 128 KHz for a 2 time slot interface to 8192 KHz for a 128 time slot PCM interface. The PCLK frequency is derived from an internal high frequency clock.

The reference device for the SLIC is a Silicon Laboratories Si3210/Si3050 ProSLIC® device. Other equivalent SLIC devices can also be supported. The AR7100 can connect up to two Si3210 devices, or 1 Si3050 + 1 Si3210 device (one device per voice channel). The SLIC Interface channel does not support transfer of 16-bit sample size.

2.5.2 I^2S

The AR7100 supports an I^2S interface to an external audio ADC/DAC, used to drive a speaker (or speakers) and/or a microphone. These features are supported:

- External clock input
  An external crystal or an ADC/DAC with an audio PLL is required to operate at standard audio frequencies. If the exact frequency is not important, the AR7100 can drive the clock and a low-cost ADC/DAC can be used without a PLL.
- Stereo and mono support
- Digital volume control (–84 dB to +42 dB)
- Sample sizes from 8-bits to 32-bits
- I^2S word sizes of 16-bits or 32-bits

A DMA engine is used to move data between the I^2S block and the DDR memory.

2.6 DDR Interface

The AR7100 supports a 16-bit or 32-bit DDR1 memory interface with up to 400 Mbps per pin, a dedicated point-to-point interface for the CPU, and dedicated point-to-point interfaces for each of the external master devices (USB, Ethernet(2) and PCI) and write buffering at each interface. Separate arbitration by bank allows efficient pipeline RAS/CAS/Precharge scheduling and multiple reads from the processor to issue at full bandwidth. Table 2-4 describes supported DDR configurations, with Table 2-5 on page 28 showing the address bits.

NOTE: The AR7100 does not support x4 DDR devices.

Table 2-4. **DDR Configurations**

Device Type	Device Count	Total Capacity
16-bit		
128 Mbx8	2	32 MB
128 Mbx16	1	16 MB
256Mbx8	2	64 MB
256Mbx16	1	32 MB
512Mbx8	2	128 MB
512Mbx16	1	64 MB
32-bit		
128 Mbx8	4	16 MB
128 Mbx16	2	32 MB
256Mbx8	4	128 MB
256Mbx16	2	64 MB
512Mbx8	4	256 MB
512Mbx16	2	128 MB

Table 2-5. **Address Mapping**

Bit	Use (16-Bit)	Use (32-Bit)
0	Unused (x16 DRAM)	Unused
1	CAS 0	Unused
2	CAS 1	CAS 0
3	CAS 2	CAS 1
4	CAS 3	CAS 2
5	BA 0	BA 0
6	BA 1	BA 1
7	CAS 4	CAS 3
8	CAS 5	CAS 4
9	CAS 6	CAS 5
10	CAS 7	CAS 6
11	CAS 8	CAS 7
12	RAS 0	CAS 8
13	RAS 1	RAS 0
14	RAS 2	RAS 1
15	RAS 3	RAS 2
16	RAS 4	RAS 3
17	RAS 5	RAS 4
18	RAS 6	RAS 5
19	RAS 7	RAS 6
20	RAS 8	RAS 7
21	RAS 9	RAS 8
22	RAS 10	RAS 9
23	RAS 11	RAS 10
24	RAS 12	RAS 11
25	CAS 9	RAS 12
26	CAS 11[1]	CAS 9
27	Unused	CAS 11[1]
31:28	Unused	Unused

[1]CAS 10 is used as the auto-precharge bit and cannot be used as an address

2.7 UART

The AR7100 has a single Tx/Rx UART port with 16550 equivalent debug/console.

2.8 CPU

The AR7100 uses an embedded 24Kc processor from MIPS Technology. For complete information on the 24Kc processor, visit: http://www.mips.com/products/processors/32-64-bit-cores/mips32-24k/index.cfm#resources.

2.9 Processor Frequency

The AR7100 has a built-in processor core that supports up to 300 MHz (AR7131), 400 MHz (AR7141), and 680 MHz (AR7161) with these features:

- 64-K four-way set associative instruction cache
- 32-K four- way set associative data cache
- Single cycle multiply-accumulate with MIPS32 and MIPS16 instruction sets
- Supports non-blocking cached reads

  Under Processor Cores-24K Family, refer to:

  MIPS32 24Kc Processor Core Datasheet v3.04

- MIPS32 4Kc Processor Core Family Software User's Manual v3.05

Under EJTAG, refer to:

- EJTAG Specification v2.60

The MIPS core processor can be configured in many ways to support different types of designs. Table 2-6 summarizes the configuration settings used by the AR7100.

Table 2-6. **Core Processor Configuration Settings**

Setting	Description
Cache Size	The AR7100 implements 64KB 4-way set associative instruction cache and 32KB 4-way set associative data cache. It supports the MIPS32 and MIPS16 instruction sets and non-blocking cached reads.
Scratch Pad	The AR7100 does not use scratch pad memory.
Endian	The AR7100 implements Big Endian addressing.
Write Buffer	The AR7100 uses a SysAD-style write buffer. Any sequential set of byte enables are allowed. Discontinuous byte enables are not allowed (byte 0 and byte 3 only, for example).
Block Addressing	The AR7100 implements sequential ordering.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the AR7100. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 3-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max. Rating	Unit
V_{DD33}	I/O Supply Voltage (3.3 V)	–0.3 to 4.6	V
T_{store}	Storage Temperature	–65 to 150	°C
T_J	Junction Temperature	120	°C
ESD	Electrostatic Discharge Tolerance	1.5	KV

3.1.1 Recommended Operating Conditions

Table 3-2. **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	I/O Supply Voltage	± 10%	3.0	3.3	3.6	V
V_{DD25}	DDR Supply Voltage	± 10%	2.25	2.5	2.75	V
V_{DDR_REF}	DDR Reference Supply Voltage	± 10%	1.125	1.25	1.375	V
V_{DD12}	Core Supply Voltage	± 3%	1.16	1.2	1.24	V
T_{case}	Commercial Case Temperature		0	25	95	°C
Ψ_{JT}	Junction-to-Top Center of the Package[1]				2.4	°C/W

[1]For the 13 mm x 13 mm TFBGA package

3.2 General DC Electrical Characteristics

Table 3-3 lists the general DC electrical characteristics. The following conditions apply to all DC characteristics unless otherwise specified:

V_{dd} = 3.3 V, T_{amb} = 25 °C

Table 3-3. **General DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	$V_{out} = V_{OH\ (min)}$	2.0	—	V_{dd} + 0.3	V
V_{IL}	Low Level Input Voltage	$V_{out} = V_{OL\ (min)}$	–0.3	—	0.8	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	—	± 5	—	µA
V_{OH}	High Level Output Voltage	No Load (I_o = 0)	V_{dd} –0.3	—	—	V
		I_o = 12 mA	V_{dd} –0.8	—	—	V
V_{OL}	Low Level Output Voltage	No Load (I_o = 0)	—	—	0.20	V
		I_o = 12 mA	—	—	0.27	V
I_O	Output Current	V_o = 0 to V_{dd}	—	—	8	mA
C_{IN}	Input Capacitance	—	—	6	—	pF

3.3 Power on Sequence Requirements

As long as the reset timing is met, the ordering of the AR7100 power supplies (VDD33 and VDD12) has no other requirements. See Figure 4-12, "Reset Timing," on page 38.

3.4 Typical Power Consumption Parameters

Table 3-4 shows the typical power drain on each of the on-chip power supply domains.

Table 3-4. **Typical Power Consumption**

Chip	1.2 V Supply	1.25 V Supply	2.5 V Supply	3.3 V Supply
AR7161	1 A	Negligible (<1 mA)	150 mA	50 mA
AR7141	800 mA	Negligible (<1 mA)	150 mA	50 mA
AR7130	700 mA	Negligible (<1 mA)	120 mA	50 mA

4. AC Specifications

4.1 GMII Timing (1000BASE-T)

4.1.1 GMII Transmit

Figure 4-1 shows the GMII Tx timing in 1000BASE-T mode.

See Table 4-1 on page 35 for timing values.

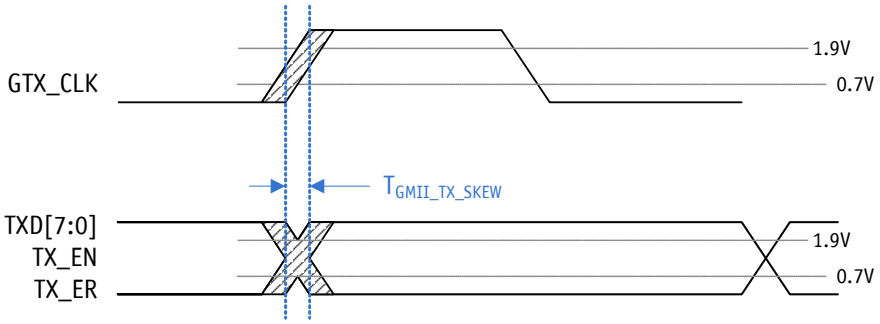


Figure 4-1. **GMII Tx Timing (1000BASE-T)**

4.1.2 GMII Receive

Figure 4-2 shows the GMII Rx timing in 1000BASE-T mode.

See Table 4-1 on page 35 for timing values.

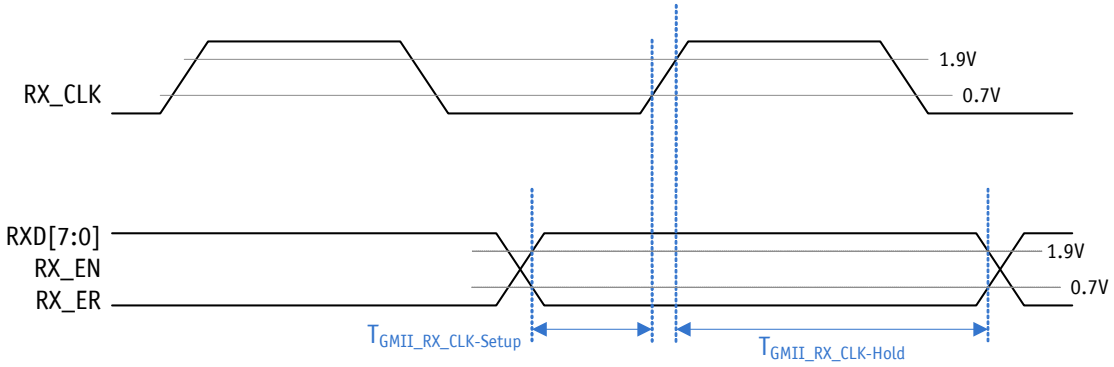


Figure 4-2. **GMII Rx Timing (1000BASE-T)**

4.2 RGMII Timing

4.2.1 RGMII Transmit

Figure 4-3 shows the RGMII Tx timing in 1000BASE-T mode.

See Table 4-1 on page 35 for timing values.

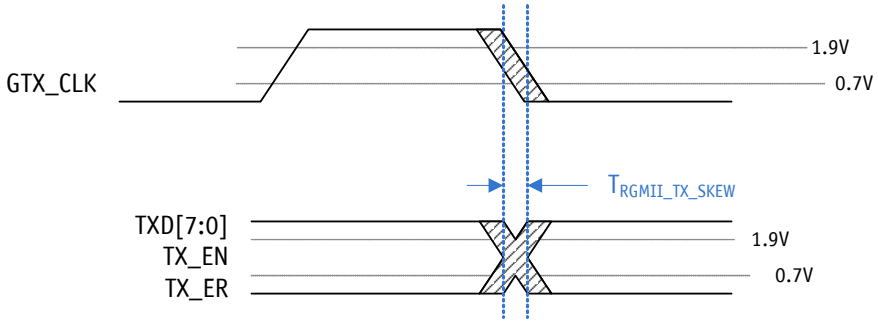


Figure 4-3. **RGMII Tx Timing (1000BASE-T)**

4.2.2 RGMII Receive

Figure 4-4 shows the RGMII Rx timing in 1000BASE-T mode.

See Table 4-1 on page 35 for timing values.

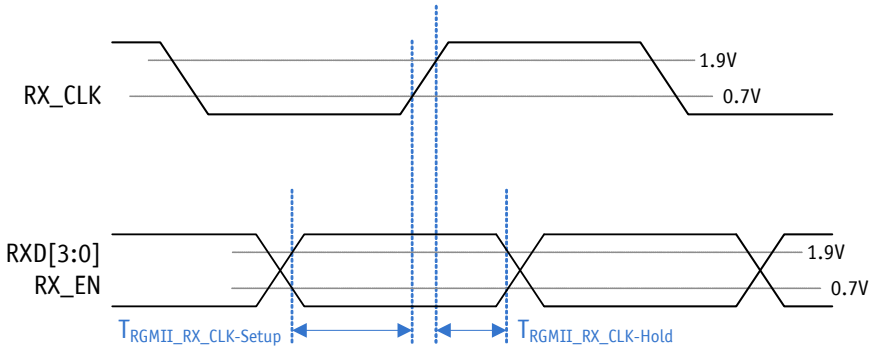


Figure 4-4. **RGMII Rx Timing (1000BASE-T)**

4.3 MII Timing (100 Mbps)

Figure 4-5 shows the MII Rx timing.
See Table 4-1 for timing values.

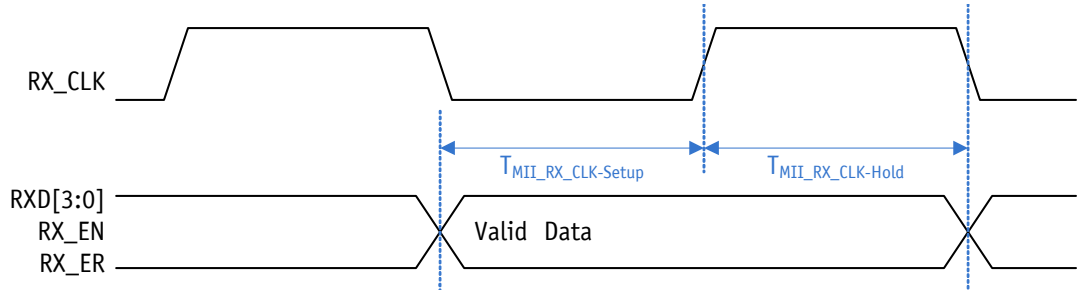


Figure 4-5. **MII Rx Timing (100 Mbps)**

4.4 RMII Timing (100 Mbps)

Figure 4-6 shows the RMII Rx timing.
See Table 4-1 for timing values.

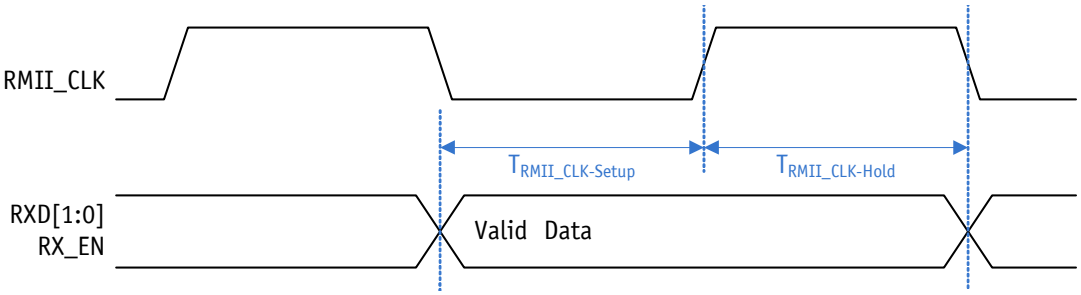


Figure 4-6. **RMII Rx Timing (100 Mbps)**

4.5 GMII, MII, RGMII, RMII Timing Values

Table 4-1 shows the timing values for
Figure 4-1 through Figure 4-6.

Table 4-1. **AR7100 GMII, MII, RGMII, RMII Timing Values**

Symbol	Parameter	Minimum	Maximum	Unit
$T_{GMII\_TX\_SKEW}$	GMII Tx skew value	—	0.5	ns
$T_{GMII\_RX\_CLK\text{-}Setup}$	GMII Rx setup time	1.6	—	ns
$T_{GMII\_RX\_CLK\text{-}Hold}$	GMII Rx hold time	0	—	ns
$T_{RGMII\_TX\_SKEW}$	RGMII Tx skew value	—	0.5	ns
$T_{RGMII\_RX\_CLK\text{-}Setup}$	RGMII Rx setup time	1.6	—	ns
$T_{RGMII\_RX\_CLK\text{-}Hold}$	RGMII Rx hold time	0	—	ns
$T_{MII\_RX\_CLK\text{-}Setup}$	MII Rx setup time	1.6	—	ns
$T_{MII\_RX\_CLK\text{-}Hold}$	MII Rx hold time	0	—	ns
$T_{RMII\_RX\_CLK\text{-}Setup}$	RMII Rx setup time	1.6	—	ns
$T_{RMII\_RX\_CLK\text{-}Hold}$	RMII Rx hold time	0	—	ns

4.6 PCI Timing

Figure 4-7 shows the PCI timing.

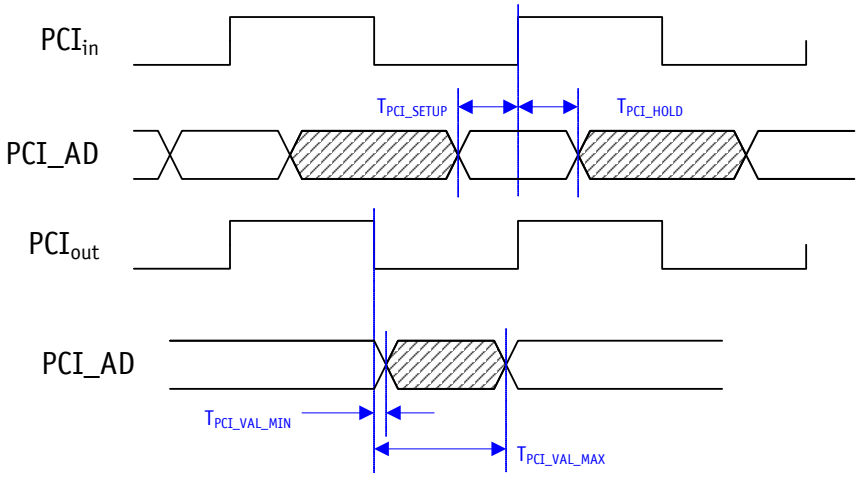


Figure 4-7. **PCI Timing**

Table 4-2 shows the timing values for Figure 4-7.

Table 4-2. **AR7100 PCI Timing Values**

Symbol	Parameter	Minimum	Maximum	Unit
T_{PCI_SETUP}	PCI setup time	3	—	ns
T_{PCI_HOLD}	PCI hold time	0	—	ns
T_{PCI_VAL}	PCI valid	2	6	ns

4.7 DDR Timing

4.7.1 DDR Address Bus

Figure 4-8 shows the DDR address bus timing.

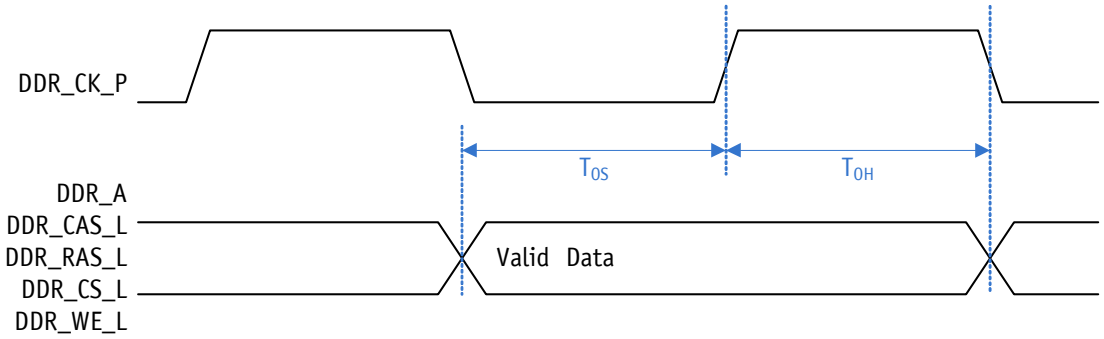


Figure 4-8. **DDR Address Bus**

4.7.2 DQ/DQM/DQS Bus Output

Figure 4-9 and Figure 4-10 show the DQ/DQS bus output timing.

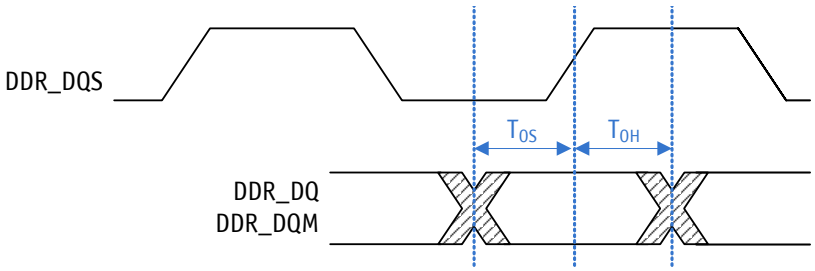


Figure 4-9. **DDR_DQ, DDR_DQM Bus Timing With Respect to DDR_DQS**

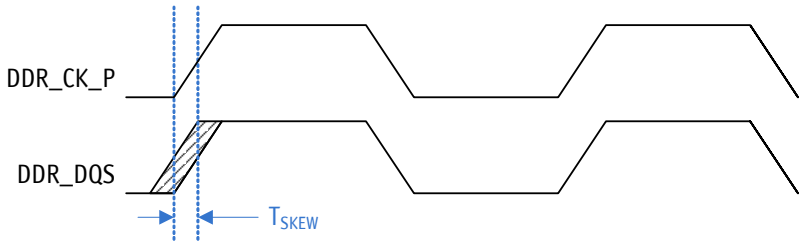


Figure 4-10. **DDR_DQS Timing With Respect to DDR_CK_P**

4.7.3 DQS/DQ Bus Input

Figure 4-11 shows the DQ/DQS bus input timing.

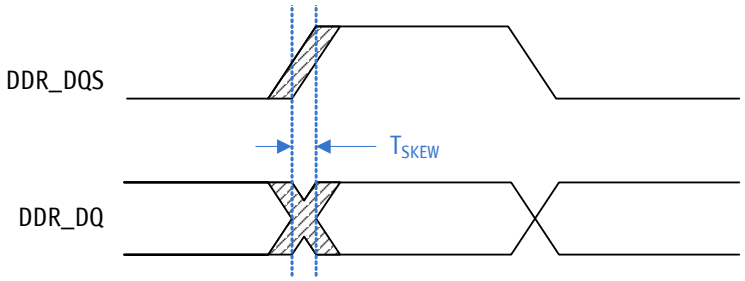


Figure 4-11. **DDR_DQ Timing With Respect to DDR_DQS**

Table 4-3 shows the timing values for Figure 4-8 through Figure 4-11.

Table 4-3. **AR7100 DDR Timing Values**

Symbol	Minimum	Maximum	Unit
DDR Address Bus			
T_{OS}	1.5	—	ns
T_{OH}	1.5	—	ns
DQ/DQM/DQS Bus Output			
T_{OS}	0.75	—	ns
T_{OH}	0.75	—	ns
T_{SKEW}	—	0.5	ns
DQS/DQ Bus Input			
T_{SKEW}	—	0.6	ns

4.8 Reset Timing

As shown in Figure 4-12, the COLD_RST_L pin must be asserted low (less than 1.6 V) for 1 ms after good power (3.0 V on VDD33 and 1.0 V on VDD12) has been supplied to the AR7100.

The drawing shows reset driven from an RC circuit connected to VDD33. If a reset timer is used instead, a delay of at least 1 ms should be used.

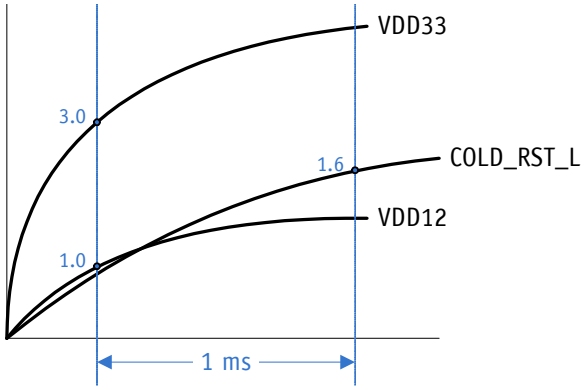


Figure 4-12. **Reset Timing**

5. Register Descriptions

This section describes the AR7100 registers.

Address	Registers	Page
0x17001000–0x17001028	PCI CSR	page 39
0x18000000–0x180000A0	DDR	page 46
0x18020000–0x18020014	UART	page 54
0x18030000–0x18030004	USB Control	page 58
0x18040000–0x18040028	GPIO	page 60
0x18050000–0x1805001C	PLL Control	page 63
0x18060000–0x18060090	Reset	page 68
0x18070000–0x18070004	MII	page 75
0x18090000–0x18090030	SLIC	page 76
0x180A0000–0x180A0048	SLIC/I^2S/ DMA	page 78
0x180B0000–0x180B004	Stereo	page 86
0x19000000–0x1900005C	Ethernet0	page 89
0x19000180–0x1900019C	Ethernet0 DMA	page 97
0x1A000000–0x1A00005C	Ethernet1	page 89
0x1A000180–0x1A00019C	Ethernet1 DMA	page 97
0x1F00000–0x1F0000C	SPI	page 102

5.1 PCI CSR Registers

Table 5-1 summarizes the PCI CSR registers for the AR7100. Note that to access the PCI CSR, make sure that the "PCI Address Space Offset for PCI Window 7 (PCI_WINDOW_7)" register on page 52 in the DDR space (at address 0x1800_0090) is equal to 0x0700_0000.

Table 5-1. **PCI CSR Register Summary**

Offset	Description	Page
0x17001000	Local Configuration Command	page 39
0x17001004	Local Configuration Write Data	page 40
0x17001008	Local Configuration Read Data	page 40
0x1700100C	Configuration I/O Address	page 40
0x17001010	Configuration I/O Command	page 40
0x17001014	Configuration I/O Write Data	page 41
0x17001018	Configuration I/O Read Data	page 41
0x1700101C	PCI Error	page 41
0x17001020	PCI Error Address	page 42
0x17001024	AHB Error	page 42
0x17001028	AHB Error Address	page 42

5.1.1 Local Configuration Command

Offset: 0x17001000
Access: Read/Write
Reset: 0

Bit	Name	Description
31:24	RES	Reserved
23:20	BYTE_ENABLE	PCI byte enable for configuration read or write
19:16	COMMAND	PCI command for configuration read or write
15:11	RES	Reserved
10:0	ADDRESS	PCI offset address; see "PCI Configuration Registers" on page 42

5.1.2 Local Configuration Write Data

Offset: 0x17001004
Access: Read/Write
Reset: 0

Bit	Description
31:0	Local configuration register write data A write to this register causes a write to the local config space, with the address and command specified by the register "Local Configuration Command".

5.1.3 Local Configuration Read Data

Offset: 0x17001008
Access: Read/Write
Reset: 0

Bit	Description
31:0	Local configuration register read data A read of this register causes a read of the local configuration space, with the address and command specified by the register "Local Configuration Command" on page 39.

5.1.4 Configuration I/O Address

Offset: 0x1700100C
Access: Read/Write
Reset: 0

Bit	Description
31:0	Address for configuration or I/O operation

5.1.5 Configuration I/O Command

Offset: 0x17001010
Access: Read/Write
Reset: 0

Bit	Description
31:8	Reserved
7:4	Byte enables for configuration or I/O operation
3:0	PCI command for configuration or I/O operation

5.1.6 Configuration I/O Write Data

Offset: 0x17001014
Access: Read/Write
Reset: 0

Bit	Description
31:0	Write data for a configuration or I/O operation A write of this register causes a PCI configuration or I/O write on the PCI bus, with the address specified by the register "Configuration I/O Address" on page 40 and the byte enables and command specified by the register "Configuration I/O Command" on page 40.

5.1.7 Configuration I/O Read Data

Offset: 0x17001018
Access: Read/Write
Reset: 0

Bit	Description
31:0	Read data for a configuration or I/O operation A read of this register causes a PCI configuration or I/O read on the PCI bus, with the address specified by the register "Configuration I/O Address" on page 40 and the byte enables and command specified by the register "Configuration I/O Command" on page 40. A master abort on the PCI bus causes a read of this register to return an error response and results in a CPU bus error, as is common during PCI discovery when the CPU attempts to read from non-existent PCI devices.

5.1.8 PCI Error

Offset: 0x1700101C
Access: Read/Write
Reset: 0

Bit		Description
31:2	Reserved	
1:0	PCI error message	
	01	Parity error On a parity error, the local configuration registers contains further information on the error.
	10	Fatal error A fatal error can be caused by a master or target abort or by exceeding the retry or TRDY timeout values in the local configuration registers.

5.1.9 PCI Error Address

Offset: 0x17001020
Access: Read/Write
Reset: 0

Bit	Names	Description
31:0	ADDRESS	Indicates the address of the PCI error.

5.1.10 AHB Error

Offset: 0x17001024
Access: Read/Write
Reset: 0

Bit	Names	Description
31:0	AHB_ERROR	Indicates an error response was received on an AHB transaction between the PCI controller and the DDR memory controller.

5.1.11 AHB Error Address

Offset: 0x17001028
Access: Read/Write
Reset: 0

Bit	Names	Description
31:0	ADDRESS	Indicates address of AHB error.

5.2 PCI Configuration Registers

Table 5-2 summarizes the PCI configuration registers for the AR7100. These registers are accessed through the "PCI CSR Registers". The offset refers to the address field in the register "Local Configuration Command" on page 39.

Table 5-2. **PCI Configuration Register Summary**

Offset	Name	Description	Page
0x04	COMMAND_STATUS	PCI Command Status	page 43
0x08	REVISION_ID	Device Revision ID	page 44
0x0C	CACHE_SZ	Cache Line Size	page 44
0x10	BASE_ADDR0	Memory Base Address	page 44
0x34	CAP_PTR	Capabilities Pointer	page 45
0x3C	INT_LINE	Interrupt Line	page 45
0x40	CFG_TIMER	TRDY Timeout Value	page 45

5.2.1 PCI Command Status (COMMAND_STATUS)

Offset: 0x04
Access: See field descriptions

The upper 16 bits provide access control of the PCI interface and are controlled by the host. The lower 16 bits provide the status of the functionality provided by the PCI interface and are mostly controlled by the AR7100.

Bit	Name	Access	Description			
31	DETECT_PAR_ERR	RO	Detect parity error			
30	SIG_SYS_ERR	RO	Signaled system error			
			On Read:		*On Write:*	
			0	No error	0	Do not clear bit
			1	Error	1	Clear error bit
29	RX_MAS_ABORT	RO	Received master abort			
28	RX_TARG_ABORT	RO	Received target abort			
27	SIG_TARG_ABORT	RO	Signaled target abort			
			On Read:		*On Write:*	
			0	No abort	0	Do not clear bit
			1	Abort	1	Clear error bit
26:25	DEVSEL_TIMING	RO	Device select timing			
			01	Medium		
24	MD_PAR_ERR	RO	Master data parity error			
			On Read:		*On Write:*	
			0	No error	0	Do not clear bit
			1	Error	1	Clear error bit
23	FAST_BB	RO	Fast back-to-back capable			
			0	Disabled		
			1	Enabled		
22	RES	RO	Reserved			
21	66MHZ_EN	RO	66 MHz capable			
20	CAP_LIST	RO	Capabilities list			
19	INT_STATUS	RO	Interrupt status			
18:16	RES	RO	Reserved			
15:11	RES	R/W	Reserved			
10	INT_EN	R/W	Interrupt disable			
9	FAST_BB_EN	R/W	Fast back-to-back enable			
8	SERR_EN	R/W	System error enable			
7	STEP_CNTL	RO	Stepping control			
6	PAR_ERR_RESP	R/W	Parity error response			
5	VGA_SNOOP	RO	VGA palette snoop			
4	MEM_WR_INV	R/W	Memory write and invalidate enable			
3	SPEC_CYCLES	RO	Special cycles			
2	BUS_MSTR	R/W	Bus master			
1	MEM_SPACE	R/W	Memory space			
0	IO_SPACE	R/W	I/O access enable			

5.2.2 Device Revision ID (REVISION_ID)

Offset: 0x08
Access: Read-Only
Reset Value: 0x01

Bit	Name	Description
31:8	CLASS_CODE	Class code identification value Contains the class code identification number that identifies the basic function of the device.
7:0	REVISION_ID	Revision identification Contains the device revision identification number. Value of this register can be loaded from the EEPROM when the EEPROM is attached.

5.2.3 Cache Line Size (CACHE_SZ)

Offset: 0x0C
Access: Read/Write
Reset Value: 0x00

Contains the size of the system cache line. This register is controlled by the host.

Bit	Name	Description	
31:24	RES	Reserved	
23:16	HDR_TYPE	Header type	
		0	Nonbridge PCI device
15:10	LATENCY_TMR	Latency timer Provides the minimum amount of time, in PCI clock cycles, that the bus master can retain ownership of the bus whenever it initiates a new transaction. This register is controlled by the host.	
9:8	RES	Reserved	
7:0	CACHE_SZ	Cache line size, in units of 32-bit words (4 bytes)	

5.2.4 Memory Base Address (BASE_ADDR0)

Offset: 0x10
Access: Read/Write
Reset Value: 0x000000C

Bit	Name	Description
31:0	BASE_ADDR0	Memory base address Contains the base address for accessing the WLAN memory mapped registers. This register is controlled by the host.

5.2.5 Capabilities Pointer (CAP_PTR)

Offset: 0x34
Access: Read-Only
Reset Value: 0x00

Bit	Name	Description
31:8	RES	Reserved
7:0	CAP_PTR	Capabilities pointer value Contains the value of the capabilities pointer, which provides an offset into the PCI configuration space.

5.2.6 Interrupt Line (INT_LINE)

Offset: 0x3C
Access: Read/Write
Reset Value: 0x00

Bit	Name	Description
31:24	MAX_LAT	Maximum latency value (in units of 0.25 µs) Contains the maximum latency value. Value can be loaded from the EEPROM.
23:16	MIN_GNT	Minimum grant value (in units of 0.25 µs) Contains a value that indicates how long the device (bus-master) retains PCI bus ownership. Value can be loaded from the EEPROM.
15:8	INT_PIN	Interrupt pin value Defines which of the four PCI interrupt request pins a PCI function is connected to. Value can be loaded from the EEPROM.
7:0	INT_LINE	Interrupt line value Contains the host interrupt controller interrupt line value that the device interrupt pin is connected to. This register is controlled by the host.

5.2.7 TRDY Timeout Value (CFG_TIMER)

Offset: 0x40
Access: Read/Write
Reset Value: 0x80

Bit	Name	Description
31:16	RES	Reserved
15:8	RETRY	Retry timeout value Contains the number of retires the controller will perform.
7:0	TRDY	TRDY timeout value (maximum is 0xFE) Contains the number of PCI clocks the controller waits for a TRDY signal from.

5.3 DDR Registers

Table 5-3 summarizes the AR7100 DDR registers.

Table 5-3. **DDR Register Summary**

Address	Name	Description	Page
0x18000000	DDR_CONFIG	DDR DRAM Configuration 1	page 47
0x18000004	DDR_CONFIG2	DDR DRAM Configuration 2	page 48
0x18000008	DDR_MODE_REGISTER	DDR Mode Value	page 48
0x1800000C	DDR_EXTENDED_MODE _REGISTER	DDR Extended Mode Value	page 49
0x18000010	DDR_CONTROL	DDR Control	page 49
0x18000014	DDR_REFRESH	DDR Refresh Control and Configuration	page 49
0x18000018	DDR_RD_DATA_THIS_CYCLE	DDR Read Data Capture Bit Mask	page 50
0x1800001C	TAP_CONTROL_0	DQS Delay Tap Control for Byte 0	page 50
0x18000020	TAP_CONTROL_1	DQS Delay Tap Control for Byte 1	page 50
0x18000024	TAP_CONTROL_2	DQS Delay Tap Control for Byte 2	page 51
0x18000028	TAP_CONTROL_3	DQS Delay Tap Control for Byte 3	page 51
0x1800007C	PCI_WINDOW_0	PCI Address Space Offset for PCI Window 0	page 51
0x18000080	PCI_WINDOW_1	PCI Address Space Offset for PCI Window 1	page 51
0x18000084	PCI_WINDOW_2	PCI Address Space Offset for PCI Window 2	page 51
0x18000088	PCI_WINDOW_3	PCI Address Space Offset for PCI Window 3	page 51
0x1800008C	PCI_WINDOW_4	PCI Address Space Offset for PCI Window 4	page 52
0x18000090	PCI_WINDOW_5	PCI Address Space Offset for PCI Window 5	page 52
0x18000094	PCI_WINDOW_6	PCI Address Space Offset for PCI Window 6	page 52
0x18000098	PCI_WINDOW_7	PCI Address Space Offset for PCI Window 7	page 52
0x1800009C	DDR_WB_FLUSH_GE0	Write Buffer Flush for GE0 Interface	page 53
0x180000A0	DDR_WB_FLUSH_GE1	Write Buffer Flush for GE1 Interface	page 53
0x180000A4	DDR_WB_FLUSH_USB	Write Buffer Flush for USB Interface	page 53
0x180000A8	DDR_WB_FLUSH_PCI	Write Buffer Flush for PCI Interface	page 53

5.3.1 DDR DRAM Configuration 1 (DDR_CONFIG)

Offset: 0x18000000
Access: Read/Write
Reset Value: See field descriptions

Bit	Name	Reset	Description	
31	HALF_WIDTH	0x0	Half width (16-bit) external DRAM memory system configuration. For half-width systems, the system uses DQ[15:0], DQS[1:0], and DM[1:0]. Bit [31] of "DDR DRAM Configuration 2 (DDR_CONFIG2)" can force a half-width system to use the upper data bits DQ[31:16], DQS[3:2], and DM[3:2].	
			0	32-bit
			1	16-bit
30	OPEN_PAGE	0x1	Controller open page policy. Open page policy increases bus efficiency if accesses are local to a page but increase random read/write latency.	
			0	Page open
			1	Page close
29:27	CAS_LATENCY	0x6	DRAM CAS latency parameter rounded up in memory core clock cycles. This setting is twice the setting used by the DRAM.	
			4	CAS latency 2 DRAM
			5	CAS latency 2.5 DRAM
			6	CAS latency 3 DRAM
26:23	TMRD	0xF	DRAM tMRD parameter rounded up in memory core clock cycles	
22:17	TRFC	0x1E	DRAM tRFC parameter rounded up in memory core clock cycles	
16:13	TRRD	0x4	DRAM tRRD parameter rounded up in memory core clock cycles	
12:9	TRP	0x6	DRAM tRP parameter rounded up in memory core clock cycles	
8:5	TRCD	0x6	DRAM tRCD parameter rounded up in memory core clock cycles	
4:0	TRAS	0x10	DRAM tRAS parameter rounded up in memory core clock cycles	

5.3.2 DDR DRAM Configuration 2 (DDR_CONFIG2)

Offset: 0x18000004
Access: Read/Write
Reset Value: See field descriptions

Sets up additional basic parameters for the DDR controller. Many settings are expressed in core memory cycles.

Bit	Name	Reset	Description	
31	HALF_WIDTH_LOW	0x1	Controls which part of the 32-bit DDR DQ bus is populated with DRAM in a 16-bit wide memory system	
			0	31:16
			1	15:0
30:26	RES	0x0	Reserved	
25:21	TWTR	0xE	DRAM tWTR parameter rounded up in memory core clock cycles. This number is the actual number of memory core clock cycles from the initial command of a 32-byte burst read.	
20:17	TRTP	0x8	DRAM read to precharge parameter rounded up in memory core clock cycles	
16:12	TRTW	0x10	DRAM tRTW parameter rounded up in memory core clock cycles. This number is the actual number of memory core clock cycles from the initial command of a 32-byte burst read to the initial command of a 32-byte burst write.	
11:8	TWR	0x6	DRAM tWR parameter rounded up in memory core clock cycles	
7	CKE	0x1	Directly controls the DDR_CKE_L pin	
6	PHASE_SELECT	0x0	Select output phase; must be set to 0x0	
5	CNTL_OE_EN	0x1	Control bit to allow the memory controller to tri-state the address/control output	
4	BURST_TYPE	0x0	DRAM burst type; must be set to 0x0	
3:0	BURST_LENGTH	0x8	DRAM burst length setting.	
			0x2	Half-width (16-bit) operation
			0x8	Full-width (32-bit) operation

5.3.3 DDR Mode (DDR_MODE_REGISTER)

Offset: 0x18000008
Access: Read/Write
Reset Value: 0x133

Contains the actual value written when bit 0 of the "DDR Control (DDR_CONTROL)" register is set to 1.

Bit	Name	Description
31:13	RES	Reserved
12:0	VALUE	Mode register value. Reset to CAS 3, BL=8, Sequential, DLL reset off.

5.3.4 DDR Extended Mode (DDR_EXTENDED_MODE_REGISTER)

Offset: 0x1800000C
Access: Read/Write
Reset Value: 0x2

Contains the actual value written when bit 1 of the "DDR Control (DDR_CONTROL)" register is set to 1.

Bit	Name	Description
31:13	RES	Reserved
12:0	VALUE	Extended mode register value. Reset to weak driver, DLL on.

5.3.5 DDR Control (DDR_CONTROL)

Offset: 0x18000010
Access: Read/Write
Reset Value: 0x0

Software can use this register to generate certain DDR memory operations that needed during the reset/initialization sequence.

Bit	Name	Description
31:4	RES	Reserved
3	PREA	Force a PRECHARGE ALL cycle
2	REF	Force an AUTO REFRESH cycle
1	EMRS	Force an EMRS update cycle
0	MRS	Force a MRS update cycle

5.3.6 DDR Refresh Control and Configuration (DDR_REFRESH)

Offset: 0x18000014
Access: Read/Write
Reset Value: See field descriptions

Controls when the DDR controller issues REFRESH commands to the DRAM. If the ENABLE bit is set, the controller issues a REFRESH every PERIOD cycles.

Bit	Name	Reset	Description
31:15	RES	0x0	Reserved
14	ENABLE	0x0	Refresh enable
13:0	PERIOD	0x2000	Refresh period

5.3.7 DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE)

Offset: 0x18000018
Access: Read/Write
Reset Value: See field descriptions

Bit	Name	Reset	Description	
31:24	RES	0x0	Reserved	
23:0	VEC	0xFF	Controls how many cycles of data are expected from the DRAM during a 32-byte burst.	
			0xFF	Full-width (32-bit) operation
			0xFFFF	Half-width (16-bit) operation

5.3.8 DQS Delay Tap Control for Byte 0 (TAP_CONTROL_0)

Offset: 0x1800001C
Access: Read/Write
Reset Value: See field descriptions

Controls the delay added to the DQS line to capture the data from the DRAM.

Bit	Name	Reset	Description
31:6	RES	0x0	Reserved
5	BYPASS_EN	0x0	Bypass enable. Short-circuits the first four taps directly to the output; only used in the slow corner where the absolute minimum delay is necessary
4:0	TAP	0x1	Tap setting for delay chain; up to 31 delay elements can be placed in the series. Standard value is 0x7.

5.3.9 DQS Delay Tap Control for Byte 1 (TAP_CONTROL_1)

Offset: 0x18000020
Access: Read/Write
Reset Value: 0x1

Bit	Name	Description	
31:6	RES	0x0	Reserved
5	BYPASS_EN	0x0	Bypass enable. Short-circuits the first four taps directly to the output; only used in the slow corner where the absolute minimum delay is necessary
4:0	TAP	0x1	Tap setting for delay chain; up to 31 delay elements can be placed in the series. Standard value is 0x7.

5.3.10 DQS Delay Tap Control for Byte 2 (TAP_CONTROL_2)

Offset: 0x18000024
Access: Read/Write
Reset Value: 0x1

Bit	Name	Description	
31:6	RES	0x0	Reserved
5	BYPASS_EN	0x0	Bypass enable. Short-circuits the first four taps directly to the output; only used in the slow corner where the absolute minimum delay is necessary
4:0	TAP	0x1	Tap setting for delay chain; up to 31 delay elements can be placed in the series. Standard value is 0x7.

5.3.11 DQS Delay Tap Control for Byte 3 (TAP_CONTROL_3)

Offset: 0x18000028
Access: Read/Write
Reset Value: 0x1

Bit	Name	Description	
31:6	RES	0x0	Reserved
5	BYPASS_EN	0x0	Bypass enable. Short-circuits the first four taps directly to the output; only used in the slow corner where the absolute minimum delay is necessary
4:0	TAP	0x1	Tap setting for delay chain; up to 31 delay elements can be placed in the series. Standard value is 0x7.

5.3.12 PCI Address Space Offset for PCI Window 0 (PCI_WINDOW_0)

Offset: 0x1800007C
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	OFFSET	Base address for PCI window 0 Accesses to PCI window 0 (0x1000_0000–0x1100_0000) are converted to the PCI bus address by taking bits [23:0] of the access and adding the contents of the PCI_WINDOW_0 register.

5.3.13 PCI Address Space Offset for PCI Window 1 (PCI_WINDOW_1)

Offset: 0x18000080
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	OFFSET	Base address for PCI window 1 Accesses to PCI window 1 (0x1100_0000–0x1200_0000) are converted to the PCI bus address by taking bits [23:0] of the access and adding the contents of the PCI_WINDOW_1 register.

5.3.14 PCI Address Space Offset for PCI Window 2 (PCI_WINDOW_2)

Offset: 0x18000084
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	OFFSET	Base address for PCI window 2 Accesses to PCI window 2 (0x1200_0000–0x1300_0000) are converted to the PCI bus address by taking bits [23:0] of the access and adding the contents of the PCI_WINDOW_2 register.

5.3.15 PCI Address Space Offset for PCI Window 3 (PCI_WINDOW_3)

Offset: 0x18000088
Access: Read/Write
Reset Value:0x0

Bit	Name	Description
31:0	OFFSET	Base address for PCI window 3 Accesses to PCI window 3 (0x1300_0000–0x1400_0000) are converted to the PCI bus address by taking bits [23:0] of the access and adding the contents of the PCI_WINDOW_3 register.

5.3.16 PCI Address Space Offset for PCI Window 4 (PCI_WINDOW_4)

Offset: 0x1800008C
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	OFFSET	Base address for PCI window 4 Accesses to PCI window 4 (0x1400_0000–0x1500_0000) are converted to the PCI bus address by taking bits [23:0] of the access and adding the contents of the PCI_WINDOW_5 register.

5.3.17 PCI Address Space Offset for PCI Window 5 (PCI_WINDOW_5)

Offset: 0x18000090
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	OFFSET	Base address for PCI window 5 Accesses to PCI window 5 (0x1500_0000–0x1600_0000) are converted to the PCI bus address by taking bits [23:0] of the access and adding the contents of the PCI_WINDOW_5 register.

5.3.18 PCI Address Space Offset for PCI Window 6 (PCI_WINDOW_6)

Offset: 0x18000094
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	OFFSET	Base address for PCI window 6 Accesses to PCI window 6 (0x1600_0000–0x1700_0000) are converted to the PCI bus address by taking bits [23:0] of the access and adding the contents of the PCI_WINDOW_6 register.

5.3.19 PCI Address Space Offset for PCI Window 7 (PCI_WINDOW_7)

Offset: 0x18000098
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	OFFSET	Base address for PCI window 7 Accesses to PCI window 7 (0x1700_0000–0x1800_0000) are converted to the PCI bus address by taking bits [23:0] of the access and adding the contents of the PCI_WINDOW_7 register. To access the PCI CSR registers, make sure that this register is equal to 0x0700_0000.

5.3.20 Write Buffer Flush for GE0 (DDR_WB_FLUSH_GE0)

Offset: 0x1800009C
Access: Read/Write
Reset Value: 0x0

Flushes any FIFOs between the GE0 interface and the DRAM. It should be run twice after any ISR read to ensure that any descriptor updates have completed to memory before being read by software

Bit	Name	Description
31:1	RES	Reserved
0	FLUSH	Set to 1 to flush; resets to 0 when the flush is complete

5.3.21 Write Buffer Flush for GE1 (DDR_WB_FLUSH_GE1)

Offset: 0x180000A0
Access: Read/Write
Reset Value: 0x0

Flushes any FIFOs between the GE1 interface and the DRAM. It should be run twice after any ISR read to ensure that any descriptor updates have completed to memory before being read by software

Bit	Name	Description
31:1	RES	Reserved
0	FLUSH	Set to 1 to flush; resets to 0 when the flush is complete

5.3.22 Write Buffer Flush for USB (DDR_WB_FLUSH_USB)

Offset: 0x180000A4
Access: Read/Write
Reset Value: 0x0

Flushes any FIFOs between the USB interface and the DRAM. It should be run twice after any ISR read to ensure that any descriptor updates have completed to memory before being read by software

Bit	Name	Description
31:1	RES	Reserved
0	FLUSH	Set to 1 to flush; resets to 0 when the flush is complete

5.3.23 Write Buffer Flush for PCI (DDR_WB_FLUSH_PCI)

Offset: 0x180000A8
Access: Read/Write
Reset Value: 0x0

Flushes any FIFOs between the PCI interface and the DRAM. It should be run twice after any ISR read to ensure that any descriptor updates have completed to memory before being read by software

Bit	Name	Description
31:1	RES	Reserved
0	FLUSH	Set to 1 to flush; resets to 0 when the flush is complete

5.4 UART Registers

Table 5-4 summarizes the UART registers for the AR7100. These registers use:

- Base address: 0x18020000

Table 5-4. **UART Register Summary**

Offset	Name	Description	Page
0x18020000	UART_RBR	Receive Buffer	page 54
	UART_THR	Transmit Holding	page 54
	UART_DLL	Divisor Latch Low	page 54
0x18020004	UART_IER	Interrupt Enable	page 55
	UART_DLH	Divisor Latch High	page 55
0x18020008	UART_IIR	Interrupt Identity	page 55
	UART_FCR	FIFO Control	page 55
0x1802000C	UART_LCR	Line Control	page 56
0x18020010	UART_MCR	Modem Control	page 56
0x18020014	UART_LSR	Line Status	page 57

5.4.1 Rx Buffer (UART_RBR); Tx Holding (UART_THR); Divisor Latch Low (UART_DLL)

Offset: 0x18020000
Access: (Varies)

- The read-only register UART_RBR contains the data byte received on the serial input port. Data in this register is only valid if the LSR data ready bit is set. In non-FIFO mode, RBR data must be read before more data arrives or it is overwritten. In FIFO mode, UART_RBR looks at the Rx FIFO head. If Rx FIFO is full and UART_RBR is not read before more data arrives, FIFO data is preserved but incoming data is lost and an overrun error occurs.
- The write-only register UART_THR contains data to transmit on the serial output port. Data can be written to THR if the LSR THR empty bit is set. If FIFOs are not enabled and THRE is set, writing to THR clears THRE. Other writes to THR before THRE is reset cause THR data to be overwritten. With FIFOs enabled and THRE set, characters may be written to THR before the FIFO is full.

Bit	Name	Description
31:8	RES	Reserved
7:0	DATA	Receive Data (UART_RBR) / Transmit Data (UART_THR) / See "Interrupt Enable (UART_IER); Divisor Latch High (UART_DLH)" on page 55 for description of how UART_DLL is used in parallel with UART_DLH.

5.4.2 Interrupt Enable (UART_IER); Divisor Latch High (UART_DLH)

Offset: 0x18020004
Access: (Varies)

Bit	Description
31:8	Reserved
7:0	The UART_DLH register with DLL forms a 16-bit, read/write, divisor latch register that contains the UART baud rate divisor. It is accessed by first setting DLAB bit [7] in the "Line Control (UART_LCR)". The output baud rate is: ■ baud = (clock frequency)/(16 * divisor) UART_IER is a read/write register containing bits that enable generation of interrupts: ■ Enable Received Data Available (ERBFI) ■ Enable Transmitter Holding Register Empty (ETBEI) ■ Enable Receive Line Status (ELSI) ■ Enable Modem Status (EDSSI)

5.4.3 Interrupt Identity (UART_IIR); FIFO Control (UART_FCR)

Offset: 0x18020008
Access: (Varies)

Bit	Description
31:8	Reserved
7:0	Identifies the source of an interrupt. Table 5-5 summarizes the interrupt operation.

Table 5-5. **UART Interrupt Control Functions**

Identification Register			Interrupt Set and Reset Function			
Bit [2]	Bit [1]	Bit [0]	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver line status	Overrun/parity/framing errors or break interrupt	Reading line status register
1	0	0	Second	Received data available	Receiver data available or read data FIFO trigger level reached	Reading receiver buffer register or the FIFO drops below the trigger level
0	1	0	Third	Transmitter holding register empty	Transmitter holding register empty	Reading IIR register (if source of interrupt) or writing into THR
0	0	0	Fourth	MODEM status	Clear to send, data set ready, ring indicator, or data center detect	Reading MODEM status register

5.4.4 Line Control (UART_LCR)

Offset: 0x1802000C
Access: Read/Write

Bit	Name	Description
31:8	RES	Reserved
7	DLAB	Divisor latch access Setting this bit enables reading and writing of the divisor latch registers DLL and DLH to set the baud rate of the UART. This bit must be cleared after initial baud rate setup to access other registers.
6	BREAK	Setting this bit sends a break signal by holding the sout line low (when not in loopback mode, as determined by "Modem Control (UART_MCR)" bit [4], until this bit clears. In loopback mode, the break condition is internally looped back to the receiver.
5	RES	Reserved
4	EPS	Even parity select If parity is enabled, this bit selects between even and odd parity. If set to a logic 1, an even number of logic 1s is transmitted or checked. If set to a logic 0, an odd number of logic 1s is transmitted or checked.
3	PEN	Parity enable When set, parity is enabled
2	STOP	Controls the number of stop bits in each transmitted or received serial character
1:0	CLS	Controls the number of bits per character in each transmitted or received serial character

5.4.5 Modem Control (UART_MCR)

Offset: 0x18020010
Access: Read/Write

Bit	Name	Description
31:8	RES	Reserved
7:5	RES	Must be filled with 0
4	LOOPBACK	When set, data on the sout line is held HIGH, while serial data output loops back to the S-in line, internally. In this mode all interrupts are fully functional.
3	RES	Reserved
2	RES	Reserved
1:0	RES	Reserved

5.4.6 Line Status (UART_LSR)

Offset: 0x18020014
Access: Read/Write

Bit	Name	Description
31:8	RES	Reserved
7	FERR	FIFO receiver error This bit is only active when FIFOs are enabled. It is set when there is at least one parity error, framing error, or break indication in the FIFO. This bit clears when the LSR is read, the character with the error is at the top of the receiver FIFO, and there are no subsequent errors in the FIFO. (Not supported)
6	TEMT	Transmitter empty This bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	THRE	Transmitter holding register empty When set, this bit indicates the UART can accept a new character for transmission. This bit is set whenever data is transferred from the THR to the transmitter shift register and no new data has been written to the THR. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled.
4	BI	Break interrupt This bit is set whenever the serial input (SIN) is held in a logic 0 state for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. A break condition on `sin` causes one and only one character, consisting of all zeros, to be received by the UART. Reading the Line Status register clears the BI bit.
3	FE	Framing error This bit is set whenever there is a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. The OE, PE and FE bits are reset when a read of this register is performed.
2	PE	Parity error This bit is set whenever there is a parity error in the receiver if the parity enable (PEN) bit in the "Line Control (UART_LCR)" is set.
1	OE	Overrun bit When set, this bit indicates an overrun error has occurred because a new data character was received before the previous data was read. The OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten.
0	DR	Data ready When set, this bit indicates the receiver contains at least one character in the RBR. This bit is cleared when the RBR is read.

5.5 USB Control Registers

Table 5-6 summarizes the AR7100 USB control registers.

Table 5-6. **USB Register Summary**

Address	Name	Description	Page
0x18030000	FLADJ_VAL	Frame Length Adjust	page 58
0x18030004	USB_CONFIG	USB Host Configuration	page 59

5.5.1 Frame Length Adjust (FLADJ_VAL)

Offset: 0x18030000
Access: Read/Write
Reset Value: 0x0

Sets the frame length adjust value for each port and for the host. The recommended value is 0x20 for both ports and the host. The two ports' values are interleaved:

- Port 0: {bit 10, bit 8, bit 6, bit 4, bit 2, bit 0}
- Port 1: {bit 11, bit 9, bit 7, bit 5, bit 3, bit 1}

Bit	Name	Description
31:18	RES	Reserved
17:12	HOST	Frame length adjust host
11:10	A5	Frame length adjust bit 5
9:8	A4	Frame length adjust bit 4
7:6	A3	Frame length adjust bit 3
5:4	A2	Frame length adjust bit 2
3:2	A1	Frame length adjust bit 1
1:0	A0	Frame length adjust bit 0

5.5.2 USB Host Configuration (USB_CONFIG)

Offset: 0x18030004
Access: Read/Write
Reset Value: See field descriptions

Bit	Name	Reset	Description	
31:20	RES	0x0	Reserved	
19	OHCI_DES_SWAP	0x0	Swap OHCI descriptor data	
18	OHCI_BUF_SWAP	0x1	Swap OHCI buffer data	
17	EHCI_DES_SWAP	0x0	Swap EHCI descriptor data	
16	EHCI_BUF_SWAP	0x1	Swap EHCI buffer data	
15:14	RES	0x0	Reserved	
13	DISABLE_XTL	0x0	Disable crystal and use GPIO as reference clock	
12	OVERRIDE_XTL	0x0	Overdrive XO input with a reference clock	
11:9	RES	0x0	Reserved	
8	OVER_CURRENT_AS_GPIO	0x0	0	Over-current detection is disabled
			1	Over-current input comes in on GPIO pins
7:6	RES	0x0	Reserved	
5:4	CLK_SEL	0x0	Select input clock frequency to USB PHY	
			00	12
			01	24
			10	48
3	RES	0x0	Reserved	
2	SS_SIMULATION_MODE	0x1	SS_SIMULATION_MODE_I strap value	
1	SS_RESUME_UTMI_PLS_DIS	0x0	SS_RESUME_UTMI_PLS_DIS_I strap value	
0	SS_UTMI_BACKWARD_ENB	0x0	SS_UTMI_BACKWARD_ENB_I strap value	

5.6 GPIO Registers

Table 5-7 summarizes the AR7100 GPIO control registers.

Table 5-7. **GPIO Register Summary**

Address	Name	Description	Page
0x18040000	GPIO_OE	GPIO Enable	page 60
0x18040004	GPIO_IN	GPIO Input Value	page 60
0x18040008	GPIO_OUT	GPIO Output Value	page 61
0x1804000C	GPIO_SET	GPIO Per-Bit Set	page 61
0x18040010	GPIO_CLEAR	GPIO Per-Bit Clear	page 61
0x18040014	GPIO_INT	GPIO Interrupt Enable	page 61
0x18040018	GPIO_INT_TYPE	GPIO Interrupt Type	page 62
0x1804001C	GPIO_INT_POLARITY	GPIO Interrupt Polarity	page 62
0x18040020	GPIO_INT_PENDING	GPIO Interrupt Pending	page 62
0x18040024	GPIO_INT_MASK	GPIO Interrupt Mask	page 62
0x18040028	GPIO_FUNCTION	GPIO Function	page 63

5.6.1 GPIO Enable (GPIO_OE)

Offset: 0x18040000
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:12	RES	Reserved	
11:0	OE	Per-bit output enable	
		0	Enables its use as an input
		1	Enables the output driver

5.6.2 GPIO Input Value (GPIO_IN)

Offset: 0x18040004
Access: Read-Only
Reset Value: 0x0

Bit	Name	Description
31:12	RES	Reserved
11:0	IN	The current values of each GPIO pin

5.6.3 GPIO Output Value (GPIO_OUT)

Offset: 0x18040008
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:12	RES	Reserved
11:0	OUT	Driver output value. If the corresponding bit in the "GPIO Enable (GPIO_OE)" register is set to 1, the GPIO pin drives the value in the corresponding bit of this register. Alternatively "GPIO Per-Bit Set (GPIO_SET)" or "GPIO Per-Bit Clear (GPIO_CLEAR)" may be used to control the output values.

5.6.4 GPIO Per-Bit Set (GPIO_SET)

Offset: 0x1804000C
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:12	RES	Reserved
11:0	SET	On a write, any bit that is set causes the corresponding GPIO bit to be set. Any bit that is not set has no effect.

5.6.5 GPIO Per-Bit Clear (GPIO_CLEAR)

Offset: 0x18040010
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:12	RES	Reserved
11:0	CLEAR	On a write, any bit that is set causes the corresponding GPIO bit to be cleared. Any bit that is not set has no effect.

5.6.6 GPIO Interrupt Enable (GPIO_INT)

Offset: 0x18040014
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:12	RES	Reserved
11:0	INT	For each bit that is set, that bit is considered an interrupt and OR'd into the GPIO interrupt line

5.6.7 GPIO Interrupt Type (GPIO_INT_TYPE)

Offset: 0x18040018
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:12	RES	Reserved	
11:0	TYPE	0	Indicates that the bit is an edge-sensitive interrupt
		1	Indicates that the bit is a level-sensitive interrupt

5.6.8 GPIO Interrupt Polarity (GPIO_INT_POLARITY)

Offset: 0x1804001C
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:12	RES	Reserved	
11:0	POLARITY	0	Indicates that the interrupt is active low (level) or falling edge (edge)
		1	Indicates that the interrupt is active high (level) or rising edge (edge)

5.6.9 GPIO Interrupt Pending (GPIO_INT_PENDING)

Offset: 0x18040020
Access: Read-Only
Reset Value: 0x0

Bit	Name	Description
31:12	RES	Reserved
11:0	PENDING	For each bit, indicates that an interrupt is currently pending. For edge sensitive interrupts, this register is read-with-clear.

5.6.10 GPIO Interrupt Mask (GPIO_INT_MASK)

Offset: 0x18040024
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:12	RES	Reserved
11:0	MASK	For each bit, if set, the corresponding interrupt in the "GPIO Interrupt Pending (GPIO_INT_PENDING)" register is passed on to the center interrupt controller

5.6.11 GPIO Function (GPIO_FUNCTION)

Offset: 0x18040028
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:18	RES	Reserved	
17	I2S_EN	Enable GPIO pins [11, 8:6] as I^2S interface pins	
		11	I2S_SDI
		8	I2S_SCK
		7	I2S_WS
		6	I2S_SDO
16	SLIC_EN	Enable GPIO pins [5:2] as SLIC interface pins	
		5	FS
		4	PCLK
		3	DXA
		2	DRA
15:14	RES	Reserved	
13	SI_CS2_L	Enable GPIO pin 1 as optional SPI chip select for controlling serial devices	
12	SI_CS1_L	Enable GPIO pin 0 as optional SPI chip select for controlling serial devices	
11:9	RES	Reserved	
8	UART_EN	Enable UART I/O on GPIO pins 9 (UART_SIN) and 10 (UART_SOUT)	
7:0	RES	Reserved	

5.7 PLL Control Registers

Table 5-8 summarizes the AR7100 PLL control registers.

Table 5-8. **PLL Control Register Summary**

Address	Name	Description	Page
0x18050000	CPU_PLL_CONFIG	CPU Phase Lock Loop Configuration	page 64
0x18050004	SEC_PLL_CONFIG	Secondary Phase Lock Loop Configuration	page 65
0x18050008	CPU_CLOCK_CONTROL	CPU Clock Control	page 65
0x18050010	ETH_INT0_CLK	Ethernet Internal Clock Control	page 66
0x18050014	ETH_INT1_CLK	Ethernet Internal Clock Control	page 66
0x18050018	ETH_EXT_CLK	Ethernet Clock Control	page 67
0x1805001C	PCI_CLK	PCI Clock Control	page 67

5.7.1 CPU Phase Lock Loop Configuration (CPU_PLL_CONFIG)

Offset: 0x18050000
Access: Read/Write
Reset Value: See field descriptions

Bit	Name	Reset	Description	
31	SW_UPDATE	0x0	When asserted, PLL control logic samples other values in this register	
30	LOCKED	0x0	PLL lock status	
29:23	RES	0x0	Reserved	
22:20	AHB_DIV	0x1	AHB clock divisor; AHB bus frequency is divided from the CPU clock by: 2 * (AHB_DIV + 1)	
19:18	DDR_DIV_SEL	0x0	Divider to generate the DDR clock from the PLL output; takes effect when the bit SW_UPDATE is set, then the bit CLOCK_SWITCH in the "CPU Clock Control (CPU_CLOCK_CONTROL)" register is set	
			00	Divide by 1
			01	Divide by 2
			10	Divide by 3
			11	Divide by 4
17:16	CPU_DIV_SEL	0x0	Divider to generate the CPU clock from the PLL output; takes effect when the bit SW_UPDATE is set, then the bit CLOCK_SWITCH in the CPU_CLOCK_CONTROL register is set	
			00	Divide by 1
			01	Divide by 2
			10	Divide by 3
			11	Divide by 4
15:12	PLL_LOOP_BW	0x4	PLL loop bandwidth setting; set to roundup: (total divider value/4) – 1	
11:10	PLL_DIV_IN	0x0	PLL input divider value Takes effect when SW_UPDATE bit is set	
			0	Divide by 1
			1	Divide by 2
			2	Divide by 4
9:8	PLL_DIV_OUT	0x0	PLL output divider value; takes effect when SW_UPDATE bit is set	
			0	Divide by 1
			1	Divide by 2
			2	Divide by 4
7:3	PLL_FB	0x14	PLL feedback divider value; the PLL implements a divide of this register value + 1; takes effect when SW_UPDATE bit is set	
2	RES	0x0	Reserved	
1	PLL_BYPASS	0x1	PLL bypass; takes effect when SW_UPDATE bit is set and then the CLOCK_SWITCH bit in the CPU_CLOCK_CONTROL register is set	
			0	Clock from PLL output
			1	Clock from PLL input
0	PLL_POWER_DOWN	0x1	PLL power down; takes effect when SW_UPDATE bit is set	
			0	Normal operation
			1	Power down

5.7.2 Secondary Phase Lock Loop Configuration (SEC_PLL_CONFIG)

Offset: 0x18050004
Access: Read/Write
Reset Value: See field descriptions

For standard configuration, the PLL should be set to run at 1 GHz.

Bit	Name	Reset	Description	
31	RES	0x0	Reserved	
30	LOCKED	0x0	PLL lock status	
29:23	RES	0x0	Reserved	
22:16	PLL_RESET	0x1	Reset the PLL dividers	
			0	PLL dividers
			1:2	GE0 dividers
			3:4	GE1 dividers
			5	PCI dividers
			6	ETH dividers
15:12	PLL_LOOP_BW	0x4	PLL loop bandwidth setting; set to roundup: (total divider value/4) – 1 Note, to run the PLL at 1 GHz, these bits must be set to 0x5.	
11:10	PLL_DIV_IN	0x0	PLL input divider value To run the PLL at 1 GHz, this bit must be set to 0.	
			0	Divide by 1
			1	Divide by 2
			2	Divide by 4
9:8	PLL_DIV_OUT	0x0	PLL output divider value To run the PLL at 1 GHz, this bit must be set to 0.	
			0	Divide by 1
			1	Divide by 2
			2	Divide by 4
7:3	PLL_FB	0x14	PLL feedback divider value; the PLL implements a divide of this register value + 1; takes effect when SW_UPDATE bit is set Note, to run the PLL at 1 GHz, these bits must be set to 0x18.	
2:1	RES	0x0	Reserved	
0	PLL_POWER_DOWN	0x1	PLL power down; takes effect when SW_UPDATE bit is set	
			0	Normal operation
			1	Power down

5.7.3 CPU Clock Control (CPU_CLOCK_CONTROL)

Offset: 0x18050008
Access: Read/Write
Reset Value: 0x0

Controls the CPU clock changes that require the clock to pause during changes, including any change to the PLL_BYPASS, CPU_CLK_DIV, and DDR_CLK_DIV values. If the ratio between CPU_CLK_DIV and DDR_CLK_DOV changes, the RESET_SWITCH bit must be set and the CLOCK_SWITCH causes a full CPU reset.

Bit	Name	Description
31:2	RES	Reserved
1	RESET_SWITCH	Reset during clock switch trigger; necessary if the ratio between CPU_CLK_DIV and DDR_CLK_DIV changes
0	CLOCK_SWITCH	Clock switch trigger; pauses the clock, changes the PLL_BYPASS, CPU_CLK_DIV, and DDR_CLK_DIV values, then restarts the clock

5.7.4 Ethernet Internal Clock Control (ETH_INT0_CLK)

Offset: 0x18050010
Access: Read/Write
Reset Value: See field descriptions

Controls the clock dividers needed to generate the 125 MHz clock for RGMII and GMII modes. Use these values when the PLL is running at 1 GHz:

- GMII (1000 Mbps): 0x1411_0000
- RGMII (10 Mbps): 0x0099_1099
- RGMII (100 Mbps): 0x0044_1011
- RGMII (1000 Mbps): 0x1311_0000

Bit	Name	Reset	Description
31:29	RES	0x0	Reserved
28	STAGE1_OFFSET_PHASE	0x0	Initial value of offset phase used for generating Ethernet Tx clock
27:24	STAGE1_OFFSET_COUNT	0x1	Initial value of offset counter used for generating Ethernet Tx clock
23:20	STAGE1_PHASE1_COUNT	0x1	Set this value to the number of internal divide clock cycles for the high phase of the Ethernet clock minus one
19:16	STAGE1_PHASE0_COUNT	0x1	Set this value to the number of internal divide clock cycles for the low phase of the Ethernet clock minus one
15:13	RES	0x0	Reserved
12	STAGE0_OFFSET_PHASE	0x1	Initial value of offset phase used for generating Ethernet Tx clock
11:8	STAGE0_OFFSET_COUNT	0x0	Initial value of offset counter used for generating Ethernet Tx clock
7:4	STAGE0_PHASE1_COUNT	0x0	Set this value to the number of PLL cycles for the high phase of the internal divide clock minus one
3:0	STAGE0_PHASE0_COUNT	0x0	Set this value to the number of PLL cycles for the low phase of the internal divide clock minus one

5.7.5 Ethernet Internal Clock Control (ETH_INT1_CLK)

Offset: 0x18050014
Access: Read/Write
Reset Value: See field descriptions

Controls the clock dividers needed to generate the 125 MHz clock for RGMII and GMII modes. Use these values when the PLL is running at 1 GHz:

- GMII (1000 Mbps): 0x1411_0000
- RGMII (10 Mbps): 0x0099_1099
- RGMII (100 Mbps): 0x0044_1011
- RGMII (1000 Mbps): 0x1311_0000

Bit	Name	Reset	Description
31:29	RES	0x0	Reserved
28	STAGE1_OFFSET_PHASE	0x0	Initial value of offset phase used for generating Ethernet Tx clock
27:24	STAGE1_OFFSET_COUNT	0x1	Initial value of offset counter used for generating Ethernet Tx clock
23:20	STAGE1_PHASE1_COUNT	0x1	Set this value to the number of internal divide clock cycles for the high phase of the Ethernet clock minus one
19:16	STAGE1_PHASE0_COUNT	0x1	Set this value to the number of internal divide clock cycles for the low phase of the Ethernet clock minus one
15:13	RES	0x0	Reserved
12	STAGE0_OFFSET_PHASE	0x1	Initial value of offset phase used for generating Ethernet Tx clock
11:8	STAGE0_OFFSET_COUNT	0x0	Initial value of offset counter used for generating Ethernet Tx clock
7:4	STAGE0_PHASE1_COUNT	0x0	Set this value to the number of PLL cycles for the high phase of the internal divide clock minus one
3:0	STAGE0_PHASE0_COUNT	0x0	Set this value to the number of PLL cycles for the low phase of the internal divide clock minus one

5.7.6 Ethernet Clock Control (ETH_EXT_CLK)

Offset: 0x18050018
Access: Read/Write
Reset Value: See field descriptions

Controls the clock dividers necessary to generate the 125- or 25-MHz clock driven off chip for the Ethernet PHY chip(s).

Bit	Name	Reset	Description
31:13	RES	0x0	Reserved
12:8	PHASE1_COUNT	0x2	Set this value to the number of PLL cycles for the high phase of the Ethernet clock minus one
7:5	RES	0x0	Reserved
4:0	PHASE0_COUNT	0x2	Set this value to the number of PLL cycles for the low phase of the Ethernet clock minus one

5.7.7 PCI Clock Control (PCI_CLK)

Offset: 0x1805001C
Access: Read/Write
Reset Value: See field descriptions

Bit	Name	Reset	Description
31:8	RES	0x0	Reserved
7:4	PHASE1_COUNT	0x4	Set this value to the number of PLL cycles for the high phase of the PCI clock minus one. Note: For 33 MHz, set these bits to 0xE. For 66 MHz, set these bits to 0x7 when the PLL is set to run at 1 GHz.
3:0	PHASE0_COUNT	0x4	Set this value to the number of PLL cycles for the low phase of the PCI clock minus one Note: For 33 MHz, set these bits to 0xE. For 66 MHz, set these bits to 0x6 when the PLL is set to run at 1 GHz.

5.8 Reset Registers

Table summarizes the AR7100 reset registers.

Table 5-9. **Reset Register Summary**

Address	Name	Description	Page
0x18060000	RST_GENERAL_TIMER	General Purpose Timer	page 68
0x18060004	RST_GENERAL_TIMER_RELOAD	General Purpose Timer Reload	page 68
0x18060008	RST_WATCHDOG_TIMER_CONTROL	Watchdog Timer Control	page 69
0x1806000C	RST_WATCHDOG_TIMER	Watchdog Timer	page 69
0x18060010	RST_MISC_INTERRUPT_STATUS	Misc. Interrupt Status	page 70
0x18060014	RST_MISC_INTERRUPT_MASK	Misc. Interrupt Mask	page 70
0x18060018	RST_PCI_INTERRUPT_STATUS	PCI Interrupt Status	page 71
0x1806001C	RST_PCI_INTERRUPT_MASK	PCI Interrupt Mask	page 71
0x18060020	RST_GLOBAL_INTERRUPT_STATUS	Global Interrupt Status	page 71
0x18060024	RST_RESET	Reset	page 72
0x1806002C	PERF_CONTROL	Performance Counter Control	page 73
0x18060030	PERF0_COUNTER	Performance Counter 0	page 74
0x18060034	PERF1_COUNTER	Performance Counter 1	page 74
0x18060090	RST_REVISION_ID	Chip Revision ID	page 74

5.8.1 General Purpose Timer (RST_GENERAL_TIMER)

Offset: 0x18060000
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	TIMER	Timer value This timer counts down to zero, sets an interrupt, then reloads from the "General Purpose Timer Reload (RST_GENERAL_TIMER_RELOAD)" register

5.8.2 General Purpose Timer Reload (RST_GENERAL_TIMER_RELOAD)

Offset: 0x18060004
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	RELOAD_VALUE	Timer reload value This timer contains the value that loads into the "General Purpose Timer (RST_GENERAL_TIMER)" register when decremented to zero

5.8.3 Watchdog Timer Control (RST_WATCHDOG_TIMER_CONTROL)

Offset: 0x18060008
Access: Read/Write
Reset Value: 0x0

Sets the action to take when the watchdog timer reaches zero.

Bit	Name	Description	
31	LAST	Indicates whether the last reset was caused by a watchdog timeout	
30:2	RES	Reserved	
1:0	ACTION	00	No action
		01	General purpose interrupt
		10	NMI
		11	Full chip reset

5.8.4 Watchdog Timer (RST_WATCHDOG_TIMER)

Offset: 0x1806000C
Access: Read/Write
Reset Value: 0x0

Counts down to zero then performs the action specified in the "Watchdog Timer Control (RST_WATCHDOG_TIMER_CONTROL)" register.

Bit	Name	Description
31:0	TIMER	Timer value This timer counts down to zero and remains at zero until set to another value by software; should be set to a nonzero value before updating the "Watchdog Timer Control (RST_WATCHDOG_TIMER_CONTROL)" register to a non-zero value

5.8.5 Misc. Interrupt Status (RST_MISC_INTERRUPT_STATUS)

Offset: 0x18060010
Access: See field descriptions
Reset Value: 0x0

The current state of the interrupt lines that combine to form the misc. interrupt to the processor.

Bit	Name	Access	Description
31:8	RES	—	Reserved
7	DMA_INT	RO	SLIC/I^2S DMA controller interrupt; must read the DMA controller to clear this interrupt
6	OHCI_INT	RO	USB OHCI controller interrupt; must read the OHCI controller to clear this interrupt
5	PC_INT	RO/RWC	CPU performance counter interrupt; generated whenever either of the internal CPU performance counters have bit 31 set; the relevant performance counter must be reset to clear this interrupt
4	WATCHDOG_INT	RO/RWC	Watchdog timer interrupt; generated when watchdog timer reaches zero and the register "Watchdog Timer Control (RST_WATCHDOG_TIMER_CONTROL)" is configured to generate a general purpose interrupt; cleared on a read of this register
3	UART_INT	RO	UART interrupt; must read the UART interrupt registers to clear this interrupt
2	GPIO_INT	RO	GPIO interrupt; must mask individual GPIO lines to clear this interrupt
1	ERROR_INT	RO	Interrupt caused by an address error on the internal PIO bus; must read and clear error logic registers to clear this interrupt
0	TIMER_INT	RO/RWC	Interrupt corresponding to the general purpose timer; cleared on a read of this register; the timer has already been reloaded from the "General Purpose Timer Reload (RST_GENERAL_TIMER_RELOAD)" register

5.8.6 Misc. Interrupt Mask (RST_MISC_INTERRUPT_MASK)

Offset: 0x18060014
Access: Read/Write
Reset Value: 0x0

Selectively enables or disables propagation of interrupts in the "Misc. Interrupt Status (RST_MISC_INTERRUPT_STATUS)" register.

Bit	Name	Description
31:8	RES	Reserved
7	DMA_MASK	Enables DMA interrupt if set to 1
6	OHCI_MASK	Enables OHCI interrupt if set to 1
5	PC_MASK	Enables CPU performance counter interrupt if set to 1
4	WATCHDOG_MASK	Enables a watchdog interrupt if set to 1
3	UART_MASK	Enables UART interrupt if set to 1
2	GPIO_MASK	Enables GPIO interrupt if set to 1
1	ERROR_MASK	Enables error interrupt if set to 1
0	TIMER_MASK	Enables timer interrupt if set to 1

5.8.7 PCI Interrupt Status (RST_PCI_INTERRUPT_STATUS)

Offset: 0x18060018
Access: Read-Only
Reset Value: See field descriptions

Contains the interrupt status for each of the three external PCI interrupt lines and for the PCI core.

Bit	Name	Reset	Description
31:5	RES	0x0	Reserved
4	PCI_CORE	0x0	Interrupt from the PCI core
3	RES	0x0	Reserved
2:0	PCI_INT	0x7	Shows the inverted raw signals from the external devices; active high

5.8.8 PCI Interrupt Mask (RST_PCI_INTERRUPT_MASK)

Offset: 0x1806001C
Access: Read/Write
Reset Value: 0x0

Selectively enables or disables propagation of interrupts in the "PCI Interrupt Status (RST_PCI_INTERRUPT_STATUS)" register.

Bit	Name	Description
31:5	RES	Reserved
4	PCI_CORE_MASK	Enables the PCI core interrupt
3	RES	Reserved
2:0	PCI_INT_MASK	Each bit enables interrupts from the corresponding PCI device

5.8.9 Global Interrupt Status (RST_GLOBAL_INTERRUPT_STATUS)

Offset: 0x18060020
Access: Read-Only
Reset Value: 0x0

A duplication of the cause register inside the CPU. During normal operation, it should not be used by software, but software can force an interrupt for testing by writing bits in this register.

Bit	Name	Description
31:6	RES	Reserved
5	TIMER_INT	Internal count/compare timer interrupt
4	MISC_INT	Misc. interrupt formed by the OR of all bits in the "Misc. Interrupt Status (RST_MISC_INTERRUPT_STATUS)" register enabled by the corresponding bit in the "Misc. Interrupt Mask (RST_MISC_INTERRUPT_MASK)" register
3	GE1_INT	Ethernet 1 interrupt; information available in the Ethernet 1 register space
2	GE0_INT	Ethernet 0 interrupt; information available in the Ethernet 0 register space
1	USB_INT	USB interrupt; information available in the USB register space
0	PCI_INT	PCI interrupt; information on which PCI device caused the interrupt is available in the "PCI Interrupt Status (RST_PCI_INTERRUPT_STATUS)" register

5.8.10 Reset (RST_RESET)

Offset: 0x18060024
Access: Read/Write
Reset Value: 0x0

Individually controls the reset to each of the chip's sub-modules.

Bit	Name	Description
31:29	RES	Reserved
28	EXTERNAL_RESET	External reset (SYS_RST_L pin); inverted before sent to the pin
27:25	RES	Reserved
24	FULL_CHIP_RESET	Software equivalent of pulling the reset pin; the system reboots with PLL disabled; always zero on read
23:22	RES	Reserved
21	CPU_NMI	Send an NMI to the CPU; always zero on read
20	CPU_COLD_RESET	CPU cold reset; always zero on read
19	DMA_RESET	Reset the I^2S/SLIC DMA controller
18	SLIC_RESET	Reset the SLIC controller
17	I2S_RESET	Reset the I^2S controller
16	DDR_RESET	Reset the DDR controller
15:14	RES	Reserved
13	GE1_MAC_RESET	Reset the Ethernet 1 MAC
12	GE1_PHY_RESET	Asserts the external ETH1_RESET_L pin
11:10	RES	Reserved
9	GE0_MAC_RESET	Reset the Ethernet 0 MAC
8	GE0_PHY_RESET	Assert the external ETH0_RESET_L pin
7	RES	Reserved
6	USB_OHCI_DLL_RESET	Reset the USB OHCI DLL
5	USB_HOST_RESET	Reset the USB host controller
4	USB_PHY_RESET	Reset the USB PHYs
3:2	RES	Reserved
1	PCI_BUS_RESET	Assert the external PCI_RST_L pin
0	PCI_CORE_RESET	Reset the PCI core; does not assert the external PCI_RST_L pin

5.8.11 Performance Counter Control (PERF_CONTROL)

Offset: 0x1806002C
Access: Read/Write
Reset Value: 0x0

Controls the data captured in the performance counters. A write to this register clears both performance counters.

The select options are:

Option	Description
4	GE0 Rx Packet Count Increments on every packet seen by GE0 before any filtering and before any packet drops.
6	GE1 Rx Packet Count Increments on every packet seen by GE1 before any filtering and before any packet drops.

Bit	Name	Description
31:13	RES	Reserved
12:8	PERF1	Control field for performance counter 1
7:5	RES	Reserved
4:0	PERF0	Control field for performance counter 0

5.8.12 Performance Counter 0 (PERF0_COUNTER)

Offset: 0x18060030
Access: Read/Write
Reset Value: 0x0

Increments when the signal selected by the "Performance Counter Control (PERF_CONTROL)" register is asserted.

Bit	Name	Description
31:0	COUNT	Performance counter; saturates when it reaches the maximum value

5.8.13 Performance Counter 1 (PERF1_COUNTER)

Offset: 0x18060034
Access: Read/Write
Reset Value: 0x0

Increments when the signal selected by the "Performance Counter Control (PERF_CONTROL)" register is asserted.

Bit	Name	Description
31:0	COUNT	Performance counter; saturates when it reaches the maximum value

5.8.14 Chip Revision ID (RST_REVISION_ID)

Offset: 0x18060090
Access: Read-Only
Reset Value: 0x0

Revision ID for the chip.

Bit	Name	Reset	Description	
31:8	RES	0x0	Reserved	
7:4	MAJOR	0xA	Major revision	
3:2	MINOR	0x1	Minor revision	
1:0	CHIP_ VERSION		Indicates the chip version:	
			00	AR7130
			01	AR7141
			10	AR7161

5.9 MII Registers

Table 5-10 summarizes the AR7100 MII registers.

Table 5-10. **MII Register Summary**

Address	Name	Description	Page
0x18070000	MII0_CNTL	MII0 Control	page 75
0x18070004	MII1_CNTL	MII1 Control	page 75

5.9.1 MII0 Control (MII0_CNTL)

Offset: 0x18070000
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:6	RES	Reserved	
5:4	SPEED	Interface speed:	
		00	10 Mbps
		01	100 Mbps
		10	1000 Mbps (not allowed with AR7130)
3:2	RES	Reserved	
1:0	SELECT	Select type of interface on GE0 port:	
		0	GMII (not allowed with AR7130)
		1	MII
		2	RGMII (not allowed with AR7130)
		3	RMII

5.9.2 MII1 Control (MII1_CNTL)

Offset: 0x18070004
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:6	RES	Reserved	
5:4	SPEED	Interface speed:	
		00	10 Mbps
		01	100 Mbps
		10	1000 Mbps (not allowed with AR7130)
3:1	RES	Reserved	
0	SELECT	Select type of interface on GE1 port:	
		0	RGMII (allowed with RGMII or RMII on port 0; not allowed with AR7130)
		1	RMII (allowed with MII, RGMII, or RMII on port 0)

5.10 SLIC Registers

Table 5-11 summarizes the AR7100 SLIC registers.

Table 5-11. **SLIC Register Summary**

Address	Name	Description	Page
0x18090000	SLIC_STATUS_REG	SLIC Status	page 76
0x18090004	SLIC_CNTRL_REG	SLIC Control	page 76
0x18090008	SLIC_SLOT0_NUM	Slot Number for SLIC Device 0	page 77
0x1809000C	SLIC_SLOT1_NUM	Slot Number for SLIC Device 1	page 77
0x1809002C	SLIC_SAM_POS	SLIC Sample Position	page 77
0x18090030	SLIC_FREQ_DIVIDER	SLIC Frequency Divider	page 77

5.10.1 SLIC Status (SLIC_STATUS_REG)

Offset: 0x18090000
Access: Read-Only
Reset Value: 0x0

Shows the status of the SLIC.

Bit	Name	Description	
31:3	RES	Reserved	
2	SLIC_STATUS_SLOT1_ENABLED	A value of 1 indicates SLOT 1 is enabled	
1	SLIC_STATUS_SLOT0_ENABLED	A value of 1 indicates SLOT 0 is enabled	
0	SLIC_STATUS_BLOCK_ENABLED	0	The SLIC block is disabled and no FS or PCM clock is generated
		1	The SLIC block is enabled and FS and PCM clock generation is enabled. Before this bit is enabled, SLIC frequency should be set.

5.10.2 SLIC Control (SLIC_CNTRL_REG)

Offset: 0x18090004
Access: Read/Write
Reset Value: 0x00x0

Bit	Name	Description	
31:3	RES	Reserved	
2	SLIC_STATUS_SLOT1_ENABLED	A value of 1 enables communications on SLOT 1	
1	SLIC_STATUS_SLOT0_ENABLED	A value of 1 enables communications on SLOT 0	
0	SLIC_STATUS_BLOCK_ENABLED	0	The SLIC block is disabled and no FS or PCM clock is generated
		1	The SLIC block is enabled and FS and PCM clock generation is enabled. Before this bit is enabled, SLIC frequency should be set.

5.10.3 Time Slice Assigned to Slot 0 (SLIC_SLOT0_NUM)

Offset: 0x18090008
Access: Write-Only
Reset Value: 0x0

Bit	Name	Description
31:8	RES	Reserved
7:0	SLIC_SLOT0_NUM	Slot number on which the SLIC device 0 will transmit and receive

5.10.4 Time Slice Assigned to Slot 1 (SLIC_SLOT1_NUM)

Offset: 0x1809000C
Access: Write-Only
Reset Value: 0x0

Bit	Name	Description
31:8	RES	Reserved
7:0	SLIC_SLOT1_NUM	Slot number on which the SLIC device 1 will transmit and receive

5.10.5 SLIC Sample Position (SLIC_SAM_POS)

Offset: 0x1809002C
Access: Write-Only
Reset Value: 0x0

Bit	Name	Description
31:8	RES	Reserved
7:0	SLIC_SAM_POS	Indicates SLIC data is sampled after the SLIC CLK edge in terms of the APB clock. This value should not be greater than SLIC_FREQ_DIVIDER.

5.10.6 SLIC Frequency Divider (SLIC_FREQ_DIVIDER)

Offset: 0x18090030
Access: Write-Only
Reset Value: 0x0

Bit	Name	Description
31:8	RES	Reserved
7:0	SLIC_FREQ_DIVIDER	Generates SLIC_CLK from the APB clock, which is divided by the value in the register to generate the SLCK clock. Per the SLIC specification, the frame sync (FS) should assert every 125 µs. SLIC_FREQ_DIVIDER and SLIC_SLOT_SEL should be programmed appropriately. The divider value should be one less than the actual divisor and min supported value is 2.

5.11 SLIC/I^{2}S DMA Registers

Table 5-12 summarizes the AR7100 SLIC/I^{2}S DMA control registers.

Table 5-12. **SLIC/I^{2}S DMA Register Summary**

Address	Name	Description	Page
0x180A0000	DMA_0_ADDRESS	DMA Base Address for SLIC Slot 0 Rx Channel	page 78
0x180A0004	DMA_0_CONFIG	DMA SLIC Slot 0 Rx Channel	page 79
0x180A0008	DMA_0_UPDATE	Buffer Queueing for SLIC Slot 0 Rx Channel	page 79
0x180A000C	DMA_1_ADDRESS	DMA Base Address for SLIC Slot 1 Rx Channel	page 79
0x180A0010	DMA_1_CONFIG	DMA SLIC Slot 1 Rx Channel	page 80
0x180A0014	DMA_1_UPDATE	Buffer Queueing for SLIC Slot 1 Rx Channel	page 80
0x180A0018	DMA_2_ADDRESS	DMA Base Address for the Stereo-to-Rx Channel	page 80
0x180A001C	DMA_2_CONFIG	DMA the Stereo-to-Rx Channel	page 81
0x180A0020	DMA_2_UPDATE	Buffer Queueing for the Stereo-to-Rx Channel	page 81
0x180A0024	DMA_3_ADDRESS	DMA Base Address for the SLIC Device 0 Tx Channel	page 82
0x180A0028	DMA_3_CONFIG	DMA for the SLIC Device 0 Tx Channel	page 82
0x180A002C	DMA_3_UPDATE	Buffer Queueing for the SLIC Device 0 Tx Channel	page 83
0x180A0030	DMA_4_ADDRESS	DMA Base Address for the SLIC Device 1 Tx Channel	page 83
0x180A0034	DMA_4_CONFIG	DMA for the SLIC Device 1 Tx Channel	page 83
0x180A0038	DMA_4_UPDATE	Buffer Queueing for the SLIC Device 1 Tx Channel	page 84
0x180A003C	DMA_5_ADDRESS	DMA Base Address for the Stereo Tx Channel	page 84
0x180A0040	DMA_5_CONFIG	DMA the Stereo Tx Channel	page 84
0x180A0044	DMA_5_UPDATE	Buffer Queueing for the Stereo Tx Channel	page 85
0x180A0048	DMA_INT	DMA Interrupt	page 85

5.11.1 DMA Base Address for SLIC Slot 0 Rx Channel (DMA_0_ADDRESS)

Offset: 0x180A0000
Access: Read/Write
Reset Value: 0x0

Contains the base address for the two DMA buffers associated with SLIC slot 0 Rx channel.

Bit	Name	Description
31:28	RES	Reserved
27:2	ADDRESS	Current DMA address
1:0	RES	Reserved

5.11.2 Configure DMA SLIC Slot 0 Rx Channel (DMA_0_CONFIG)

Offset: 0x180A0004
Access: See field descriptions
Reset Value: See field descriptions

Set the buffer size for SLIC slot 0 rx channel.

Bit	Name	Access	Reset	Description	
31:9	RES	—	0x0	Reserved	
8	ENABLE	RW	0x0	Enable this channel to access memory	
7	RES	—	0x0	Reserved	
6:4	SIZE	RW	0x0	Size of each buffer half	
				0	$2^2 = 4$
				1	$2^3 = 8$
				2	$2^4 = 16$
				3	$2^5 = 32$
				4	$2^6 = 64$
				5	$2^7 = 128$
				6	$2^8 = 256$
				7	$2^9 = 512$
3	RES	—	0x0	Reserved	
2	SIDE	RO	0x0	Current active side of the buffer	
1:0	SOFTWARE	RO	0x3	Software ownership of each half of the buffer	

5.11.3 Buffer Queueing for SLIC Slot 0 Rx Channel (DMA_0_UPDATE)

Offset: 0x180A0008
Access: Read/Write
Reset Value: 0x0

A write to this register clears the SOFTWARE bit in the corresponding "Configure DMA SLIC Slot 0 Rx Channel (DMA_0_CONFIG)" register.

Bit	Name	Description
31:2	RES	Reserved
1:0	SOFTWARE	Buffer queuing bits

5.11.4 DMA Base Address for SLIC Slot 1 Rx Channel (DMA_1_ADDRESS)

Offset: 0x180A000C
Access: Read/Write
Reset Value: 0x0

Contains the base address for the two DMA buffers associated with SLIC slot 1 Rx channel.

Bit	Name	Description
31:28	RES	Reserved
27:2	ADDRESS	Current DMA address
1:0	RES	Reserved

5.11.5 Configure DMA SLIC Slot 1 Rx Channel (DMA_1_CONFIG)

Offset: 0x180A0010
Access: Read/Write
Reset Value: 0x0

Set the buffer size for SLIC slot 1 Rx channel.

Bit	Name	Access	Reset	Description	
31:9	RES	—	0x0	Reserved	
8	ENABLE	RW	0x0	Enable this channel to access memory	
7	RES	—	0x0	Reserved	
6:4	SIZE	RW	0x0	Size of each buffer half	
				0	$2^2 = 4$
				1	$2^3 = 8$
				2	$2^4 = 16$
				3	$2^5 = 32$
				4	$2^6 = 64$
				5	$2^7 = 128$
				6	$2^8 = 256$
				7	$2^9 = 512$
3	RES	—	0x0	Reserved	
2	SIDE	RO	0x0	Current active side of the buffer	
1:0	SOFTWARE	RO	0x3	Software ownership of each half of the buffer	

5.11.6 Buffer Queueing for SLIC Slot 1 Rx Channel (DMA_1_UPDATE)

Offset: 0x180A0014
Access: Read/Write
Reset Value: 0x0

A write to this register clears the SOFTWARE bit in the corresponding "Configure DMA SLIC Slot 1 Rx Channel (DMA_1_CONFIG)" register.

Bit	Name	Description
31:2	RES	Reserved
1:0	SOFTWARE	Buffer queuing bits

5.11.7 DMA Base Address for the Stereo-to-Rx Channel (DMA_2_ADDRESS)

Offset: 0x180A0018
Access: Read/Write
Reset Value: 0x0

Contains the base address for the two DMA buffers associated with the stereo-to-Rx channel.

Bit	Name	Description
31:28	RES	Reserved
27:2	ADDRESS	Current DMA address
1:0	RES	Reserved

5.11.8 Configure DMA Stereo-to-Rx Channel (DMA_2_CONFIG)

Offset: 0x180A001C
Access: Read/Write
Reset Value: 0x0

Set the buffer size for the stereo-to-Rx channel.

Bit	Name	Access	Reset	Description	
31:9	RES	—	0x0	Reserved	
8	ENABLE	RW	0x0	Enable this channel to access memory	
7	RES	—	0x0	Reserved	
6:4	SIZE	RW	0x0	Size of each buffer half	
				0	$2^2 = 4$
				1	$2^3 = 8$
				2	$2^4 = 16$
				3	$2^5 = 32$
				4	$2^6 = 64$
				5	$2^7 = 128$
				6	$2^8 = 256$
				7	$2^9 = 512$
3	RES	—	0x0	Reserved	
2	SIDE	RO	0x0	Current active side of the buffer	
1:0	SOFTWARE	RO	0x3	Software ownership of each half of the buffer	

5.11.9 Buffer Queueing for the Stereo-to-Rx Channel (DMA_2_UPDATE)

Offset: 0x180A0020
Access: Read/Write
Reset Value: 0x0

A write to this register clears the SOFTWARE bit in the corresponding "Configure DMA Stereo-to-Rx Channel (DMA_2_CONFIG)" register.

Bit	Name	Description
31:2	RES	Reserved
1:0	SOFTWARE	Buffer queuing bits

5.11.10DMA Base Address for the SLIC Device 0 Tx Channel (DMA_3_ADDRESS)

Offset: 0x180A0024
Access: Read/Write
Reset Value: 0x0

Contains the base address for the two DMA buffers associated with the SLIC device 0 Tx channel.

Bit	Name	Description
31:28	RES	Reserved
27:2	ADDRESS	Current DMA address
1:0	RES	Reserved

5.11.11Configure DMA for the SLIC Device 0 Tx channel (DMA_3_CONFIG)

Offset: 0x180A0028
Access: Read/Write
Reset Value: 0x0

Set the buffer size for the SLIC device 0 Tx channel.

Bit	Name	Access	Reset	Description	
31:9	RES	—	0x0	Reserved	
8	ENABLE	RW	0x0	Enable this channel to access memory	
7	RES	—	0x0	Reserved	
6:4	SIZE	RW	0x0	Size of each buffer half	
				0	$2^2 = 4$
				1	$2^3 = 8$
				2	$2^4 = 16$
				3	$2^5 = 32$
				4	$2^6 = 64$
				5	$2^7 = 128$
				6	$2^8 = 256$
				7	$2^9 = 512$
3	RES	—	0x0	Reserved	
2	SIDE	RO	0x0	Current active side of the buffer	
1:0	SOFTWARE	RO	0x3	Software ownership of each half of the buffer	

5.11.12Buffer Queueing for the SLIC Device 0 Tx Channel (DMA_3_UPDATE)

Offset: 0x180A002C
Access: Read/Write
Reset Value: 0x0

A write to this register clears the SOFTWARE bit in the corresponding "Configure DMA for the SLIC Device 0 Tx channel (DMA_3_CONFIG)" register.

Bit	Name	Description
31:2	RES	Reserved
1:0	SOFTWARE	Buffer queuing bits

5.11.13DMA Base Address for the SLIC Device 1 Tx Channel (DMA_4_ADDRESS)

Offset: 0x180A0030
Access: Read/Write
Reset Value: 0x0

Contains the base address for the two DMA buffers associated with the SLIC device 1 Tx channel.

Bit	Name	Description
31:28	RES	Reserved
27:2	ADDRESS	Current DMA address
1:0	RES	Reserved

5.11.14Configure DMA for the SLIC Device 1 Tx Channel (DMA_4_CONFIG)

Offset: 0x180A0034
Access: Read/Write
Reset Value: 0x0

Set the buffer size for the SLIC device 1 Tx channel.

Bit	Name	Access	Reset	Description	
31:9	RES	—	0x0	Reserved	
8	ENABLE	RW	0x0	Enable this channel to access memory	
7	RES	—	0x0	Reserved	
6:4	SIZE	RW	0x0	Size of each buffer half	
				0	$2^2 = 4$
				1	$2^3 = 8$
				2	$2^4 = 16$
				3	$2^5 = 32$
				4	$2^6 = 64$
				5	$2^7 = 128$
				6	$2^8 = 256$
				7	$2^9 = 512$
3	RES	—	0x0	Reserved	
2	SIDE	RO	0x0	Current active side of the buffer	
1:0	SOFTWARE	RO	0x3	Software ownership of each half of the buffer	

5.11.15 Buffer Queueing for the SLIC Device 1 Tx Channel (DMA_4_UPDATE)

Offset: 0x180A0038
Access: Read/Write
Reset Value: 0x0

A write to this register clears the SOFTWARE bit in the corresponding "Configure DMA for the SLIC Device 1 Tx Channel (DMA_4_CONFIG)" register.

Bit	Name	Description
31:2	RES	Reserved
1:0	SOFTWARE	Buffer queuing bits

5.11.16 DMA Base Address for the Stereo Tx Channel (DMA_5_ADDRESS)

Offset: 0x180A003C
Access: Read/Write
Reset Value: 0x0

Contains the base address for the two DMA buffers associated with the stereo Tx channel.

Bit	Name	Description
31:28	RES	Reserved
27:2	ADDRESS	Current DMA address
1:0	RES	Reserved

5.11.17 Configure DMA for the Stereo Tx Channel (DMA_5_CONFIG)

Offset: 0x180A0040
Access: Read/Write
Reset Value: 0x0

Set the buffer size for the stereo Tx channel.

Bit	Name	Access	Reset	Description	
31:9	RES	—	0x0	Reserved	
8	ENABLE	RW	0x0	Enable this channel to access memory	
7	RES	—	0x0	Reserved	
6:4	SIZE	RW	0x0	Size of each buffer half	
				0	$2^2 = 4$
				1	$2^3 = 8$
				2	$2^4 = 16$
				3	$2^5 = 32$
				4	$2^6 = 64$
				5	$2^7 = 128$
				6	$2^8 = 256$
				7	$2^9 = 512$
3	RES	—	0x0	Reserved	
2	SIDE	RO	0x0	Current active side of the buffer	
1:0	SOFTWARE	RO	0x3	Software ownership of each half of the buffer	

5.11.18Buffer Queueing for the Stereo Tx Channel (DMA_5_UPDATE)

Offset: 0x180A0044
Access: Read/Write
Reset Value: 0x0

A write to this register clears the SOFTWARE bit in the corresponding "Configure DMA for the Stereo Tx Channel (DMA_5_CONFIG)" register.

Bit	Name	Description
31:2	RES	Reserved
1:0	SOFTWARE	Buffer queuing bits

5.11.19DMA Interrupt (DMA_INT)

Offset: 0x180A0048
Access: See field descriptions
Reset Value: 0x0

Contains the interrupt and mask information for the DMA channels.

Bit	Name	Access	Description
31:14	RES	—	Reserved
13:8	MASK	RW	Set to 1 to enable the corresponding interrupt
7:6	RES	—	Reserved
5:0	STATUS	RO, RWC	Current interrupt status per channel

5.12 Stereo Registers

Table 5-13 summarizes the AR7100 stereo control registers.

Table 5-13. **Stereo Register Summary**

Address	Name	Description	Page
0x180B0000	STEREO_CONFIG	Configure the Stereo Block	page 86
0x180B0004	STEREO_VOLUME	Set the Stereo Volume	page 88

5.12.1 Configure the Stereo Block (STEREO_CONFIG)

Offset: 0x180B0000
Access: Read/Write
Reset Value: See field descriptions

Controls the basic configuration of the stereo block.

Bit	Name	Reset	Description	
31:25	RES	0x0	Reserved	
24	ENABLE	0x0	Enables the stereo block for operation	
23	RESET	0x0	Resets the stereo buffers and I^2S state. Should be written to 1 when any of the data word sizes change, or if data synchronization is lost. Hardware will automatically clear to 0.	
22	I2S_DELAY	0x1	Determines whether I^2S uses a one-clock delay after WS changes but before data is sampled. Applies to MIC-in and stereo-out in master mode only. The one-clock delay is always present in slave mode.	
			0	No-delay slot, WS change is coincident with MSB
			1	One clock delay slot between WS and data MSB (I^2S standard)
21	RES	0x0	Reserved	
20	MIC_WORD_SIZE	0x0	Configures the microphone word size	
			0	16-bit PCM words
			1	32-bit PCM words
19:18	STEREO_MONO	0x0	Configures stereo/mono	
			0	Stereo
			1	Mono from channel 0
			2	Mono from channel 1
			3	Reserved

Bit	Name	Reset	Description	
17:16	DATA_WORD_SIZE	0x0	Controls the word size loaded into the PCM register from the DMA engine.	
			0	8 bits/word
			1	16 bits/word
			2	24 bits/word
			3	32 bits/word
15	I2S_WORD_SIZE	0x0	Controls the word size sent to the external I^2S DAC. When set to 32-bit words, the PCM data is left-justified in the I^2S word. I^2S word size:	
			0	16 bits per I^2S word
			1	32 bits per I^2S word
14:9	RES	0x0	Reserved	
8	MASTER	0x1	Controls I2S_CK and I2S_WS master	
			0	External DAC is the master and drives I2S_CK and I2S_WS
			1	AR7100 is the master and drives I2S_CK and I2S_WS
7:0	POSEDGE	0x27	Controls timing between positive clock edges when the chip is in master mode. This number counts in units of refclk, which is the high speed input to the chip before the PLL. The time between positive edges of the stereo data clock defines the sample rate of the data. This number can be calculated as: POSEDGE = REFCLK_FREQ/(SAMPLE_RATE * WORD_SIZE * 2) E.g., a 32 KSps sample rate with 16 bits/word and a 40 MHz refclk would yield: POSEDGE = 40 MHz/(32 KSps * 16 bits/word * 2) = 39.06 (round to 39)	

5.12.2 Set the Stereo Volume (STEREO_VOLUME)

Offset: 0x180B0004
Access: Read/Write
Reset Value: 0x0

Digitally attenuates or increases the volume level of the stereo output. Volume is adjusted in 3 dB steps. If the gain is set too high, PCM values saturate and waveform clipping occurs.

Bit	Name	Description	
31:13	RES	Reserved	
12:8	CHANNEL1	Channel 1 gain/attenuation. In this 5-bit number, the MSB is a sign bit, the others are magnitude. Setting the gain above +7 is not supported.	
		Binary (Decimal)	**Result**
		11111 (–16)	Maximum attenuation
		11110 (–14)	–84 dB
		...	...
		10001 (–1)	–6 dB
		10000 (0)	0 dB
		00000 (0)	0 dB
		00001 (+1)	+6 dB
		...	...
		00111 (+7)	+42 dB (maximum gain)
		01000 (+8)	Reserved
		...	...
		01111 (+15)	Reserved
7:5	RES	Reserved	
4:0	CHANNEL0	Channel 0 gain/attenuation. In this 5-bit number, the MSB is a sign bit, the others are magnitude. Setting the gain above +7 is not supported.	
		Binary (Decimal)	**Result**
		11111 (–16)	Maximum attenuation
		11110 (–14)	–84 dB
		...	...
		10000 (0)	0 dB
		00000 (0)	0 dB
		00000 (0)	0 dB
		00001 (+1)	+6 dB
		...	...
		00111 (+7)	+42 dB (maximum gain)
		01000 (+8)	Reserved
		...	...
		01111 (+15)	Reserved

5.13 Ethernet Registers

Table 5-14 summarizes the AR7100 Ethernet registers.

Table 5-14. **Ethernet Register Summary**

MAC 0 Address	MAC 1 Address	Description	Page
0x19000000	0x1A000000	MAC Configuration 1	page 90
0x19000004	0x1A000004	MAC Configuration 2	page 91
0x19000008	0x1A000008	IPG/IFG	page 91
0x1900000C	0x1A00000C	Half-Duplex	page 92
0x19000010	0x1A000010	Maximum Frame Length	page 92
0x19000014	0x1A000014	MII Configuration	page 93
0x19000018	0x1A000018	MII Command	page 93
0x1900001C	0x1A00001C	MII Address	page 94
0x19000020	0x1A000020	MII Control	page 94
0x19000024	0x1A000024	MII Status	page 94
0x19000028	0x1A000028	MII Indicators	page 94
0x19000040	0x1A000040	STA Address 1	page 95
0x19000044	0x1A000044	STA Address 2	page 95
0x19000054	0x1A000054	Transmit FIFO	page 95
0x19000058	0x1A000058	Dropped Frames	page 96
0x1900005C	0x1A00005C	Dropped Frames	page 96

5.13.1 MAC Configuration 1

MAC 0 Address: 0x19000000
MAC 1 Address: 0x1A000000
Access: Read/Write
Reset Value: 0x8000_0000

Bit	Name	Default	Description
31	SOFT_RESET	1	Resets all modules except for the host interface
30	SIMULATION_RESET	0	Resets the registers (e.g., the random backoff timer) that are not controlled using normal resets
29:20	RES	—	Reserved
19	RESET_RX_MAC_CONTROL	0	Resets the receive (Rx) MAC control block
18	RESET_TX_MAC_CONTROL	0	Resets the transmit (Tx) MAC control
17	RESET_RX_FUNCTION	0	Resets the Rx function
16	RESET_TX_FUNCTION	0	Resets the Tx function
15:9	RES	—	Reserved
8	LOOP_BACK	0	Causes the MAC Tx output to loop back to the MAC Rx inputs. Clearing this bit results in normal operation.
7:6	RES	—	Reserved
5	RX_FLOW_CONTROL	0	Causes Rx MAC control to ignore pause flow control frames
4	TX_FLOW_CONTROL	0	Causes Tx MAC control to send requested flow control frames. Clearing this bit prevents the MAC from sending flow control frames.
3	SYNCHRONIZED_RX	0	Synchronizes the Rx enable to the Rx stream
2	RX_ENABLE	0	Allows the MAC to receive frames from the PHY. Clearing this bit prevents frame reception.
1	SYNCHRONIZED_TX	0	Synchronizes the Tx enable to the Tx stream.
0	TX_ENABLE	0	Allows the MAC to transmit frames from the PHY. Clearing this bit prevents frame transmission.

5.13.2 MAC Configuration 2

MAC 0 Address: 0x19000004
MAC 1 Address: 0x1A000004
Access: Read/Write
Reset Value: 0x0000_7000

Bit	Name	Default	Description
31:16	RES	—	Reserved
15:12	PREAMBLE_LENGTH	0x7	Determines the length of the preamble field of the packet (in bytes).
11:10	RES	—	Reserved
9:8	INTERFACE_MODE	0x0	Determines the interface type the MAC connects to
5	HUGE_FRAME	0	Setting this bit allows frames longer than the maximum frame length to transmit and receive. Clear this bit to have the MAC limit the length of frames at the maximum frame length value as set in the "Maximum Frame Length"register.
4	LENGTH_FIELD	0	Length field checking. Setting this bit causes the MAC to check the frame's to ensure it matches the data field length. Clear this bit for no length field checking.
3	RES	—	Reserved
2	PAD/CRC ENABLE	0	Allows the MAC PAD all short frames and appends a CRC to every frame. Clear this bit if the frames for the MAC have a valid length and contain a CRC.
1	CRC_ENABLE	0	Configures the MAC to append a CRC to all frames. Clear this bit if the frames for the MAC have a valid length and contain a CRC.
0	FULL_DUPLEX	0	Configures the MAC to operate in full-duplex mode. Clear this bit to configure the mAC to operate in half-duplex mode only.

Interface Mode	Bit [9]	Bit [8]
RESERVED	0	0
Nibble Mode (10/100 Mbps MII/RMII/SMII...)	0	1
Byte mode (1000 Mbps GMII/TBI)	1	0
RESERVED	1	1

5.13.3 IPG/IFG

MAC 0 Address: 0x19000008
MAC 1 Address: 0x1A000008
Access: Read/Write
Reset Value: 0x4060_5060

Bit	Name	Default	Description
31	RES	—	Reserved
30:24	NON BACK-TO-BACK INTER-PACKET GAP 1	0x40	Represents the carrier sense window. If a carrier is detected, the MAC defers to the carrier. If, however, the carrier becomes active, the MAC continues timing and transmission. This action causes a collision and ensures media access.
23	RES	—	Reserved
22:16	NON BACK-TO-BACK INTER-PACKET GAP 2	0x60	Represents the non-back-to-back inter-packet gap in bit times
15:8	MINIMUM IFG ENFORCEMENT	0x50	Represents the minimum IFG size to enforce between frames (in bit times). Frames with less than the programmed IFG are dropped.
7	RES	—	Reserved
6:0	BACK-TO-BACK INTER-PACKET GAP	0x60	Represents the IPG between back-to-back packets (in bit times). This IPG parameter is used in full-duplex mode when two Tx packets are sent back-to-back. Set this field to the desired number of bits.

5.13.4 Half-Duplex

MAC 0 Address: 0x1900000C
MAC 1 Address: 0x1A00000C
Access: Read/Write
Reset Value: 0X00A1_F037

Bit	Name	Default	Description
31:24	RES	—	Reserved
23:20	ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION	0xA	Used when bit [19] is set. The value programmed is substituted for the Ethernet standard value of ten.
19	ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE	0	Setting this bit configures the Tx MAC to use the setting of bits [23:20] instead of the tenth collision. Clearing this bit causes the Tx MAC to follow the binary exponential backoff rule, which specifies that any collision after the tenth uses 210 – 1 as the maximum backoff time.
18	BACKPRESSURE NO BACKOFF	0	Configures the Tx MAC to immediately re-transmit following a collision during back pressure operation. Clearing this bit causes the Tx MAC to follow the binary exponential backoff rule.
17	NO BACKOFF	0	Configures the Tx MAC to immediately re-transmit following a collision. Clearing this bit causes the Tx MAC to follow the binary exponential backoff rule.
16	EXCESSIVE DEFER	1	Configures the Tx MAC to allow the transmission of a packet that has been excessively deferred. Clearing this bit causes the Tx MAC to abort transmission of a packet that has been excessively deferred.
15:12	RETRANSMISSION MAXIMUM	0xF	A programmable field that specifies the number of retransmit attempts following a collision before aborting the packet due to excessive collisions. 802.11 standards specify the maximum number of attempts as 0xF.
11:10	RES	—	Reserved
9:0	COLLISION WINDOW	0x37	Represents the slot time or collision window during which collisions might occur in a properly configured network. The preamble and SFD are included because the collision window begins at transmission start. Default is 0x37, which corresponds to the count of frame bytes at the end of the window. If the value is greater than 0x3F, the TPST signal will no longer work correctly.

5.13.5 Maximum Frame Length

MAC 0 Address: 0x19000010
MAC 1 Address: 0x1A000010
Access: Read/Write
Reset Value: 0x0000_0600

Bit	Name	Description
31:16	RES	Reserved
15:0	MAXIMUM FRAME LENGTH	Sets the maximum frame size in both Tx and Rx directions. Resets to 0x0600.

5.13.6 MII Configuration

MAC 0 Address: 0x19000014
MAC 1 Address: 0x1A000014
Access: Read/Write
Reset Value: 0X0000_0000

Bit	Name	Default	Description
31	RESET MII MGMT	0	Setting this bit resets MII management. Clearing this bit allows MII management to perform management read/write cycles as requested by the Host Interface.
30:6	RES	—	Reserved
5	SCAN AUTO INCREMENT	0	Setting this bit causes MII management to continually read from a set of contiguous PHYs. The PHY's starting address is specified by the PHY address field recorded in the "MII Address" register. The next read PHY is PHY Address + 1. The last queried PHY is the PHY at address 0x31, after which the read sequence returns to the PHY specified by the PHY address field.
4	PREAMBLE SUPPRESSION	0	Causes MII management to suppress preamble generation and reduce the management cycle from 64 clocks to 32 clocks. Clearing this bit causes MII management to perform management read/write cycles with the 64 clocks of preamble.
3	RES	—	Reserved
2:0	MGMT CLOCK SELECT	000	Determines the clock frequency of the management clock (MDC)

Management Clock Select	2	1	0
Source clock divided by 4	0	0	0
Source clock divided by 4	0	0	1
Source clock divided by 6	0	1	0
Source clock divided by 8	0	1	1
Source clock divided by 10	1	0	0
Source clock divided by 14	1	0	1
Source clock divided by 20	1	1	0
Source clock divided by 28	1	1	1

5.13.7 MII Command

MAC 0 Address: 0x19000018
MAC 1 Address: 0x1A000018
Access: Read/Write
Reset Value: 0X0000_0000

Bit	Name	Default	Description
31:2	RES	—	Reserved
1	SCAN_CYCLE	0	Causes MII management to perform read cycles continuously (e.g., to monitor link fail)
0	READ_CYCLE	0	Causes MII management to perform single read cycle

5.13.8 MII Address

MAC 0 Address: 0x1900001C
MAC 1 Address: 0x1A00001C
Access: Read/Write
Reset Value: 0X0000_0000

Bit	Name	Default	Description
31:13	RES	—	Reserved
12:8	PHY_ADDRESS	0x00	Represents the five-bit PHY address field used in management cycles. Up to 31 PHYs can be addressed (0 is reserved).
0	REGISTER_ADDRESS	0x00	Represents the five-bit register address field used in management cycles. Up to 32 register can be accessed.

5.13.9 MII Control

MAC 0 Address: 0x19000020
MAC 1 Address: 0x1A000020
Access: Write-Only
Reset Value: 0X0000_0000

Bit	Name	Default	Description
31:16	RES	—	Reserved
15:0	MII MGMT CONTROL (PHY Control)	0x0000	When written, an MII management write cycle is performed using the 16-bit data and the pre-configured PHY and Register addresses from "MII Address" (0x0A).

5.13.10MII Status

MAC 0 Address: 0x19000024
MAC 1 Address: 0x1A000024
Access: Read-Only
Reset Value: 0X0000_0000

Bit	Name	Description
31:16	RES	Reserved
15:0	MII MGMT STATUS (PHY Status)	Following an MII management read cycle, 16-bit data can be read from here.

5.13.11MII Indicators

MAC 0 Address: 0x19000028
MAC 1 Address: 0x1A000028
Access: Read-Only
Reset Value: 0X0000_0000

Bit	Name	Description
31:3	RES	Reserved
2	NOT_VALID	When a 1 is returned, this bit indicates that the MII management read cycle has not yet completed and that read data is not yet valid.
1	SCANNING	When a 1 is returned, this bit indicates that a scan operation (continuous MII management read cycles) is in progress,
0	BUSY	When a 1 is returned, this bit indicates that the MII management block is currently performing an MII management read or write cycle.

5.13.12STA Address 1

MAC 0 Address: 0x19000040
MAC 1 Address: 0x1A000040
Access: Read/Write
Reset Value: 0X0000_0000

Bit	Name	Default	Description
31:24	STATION_ADDRESS First octet	0x00	Holds the first octet of the STA address
23:16	STATION_ADDRESS Second octet	0x00	Holds the second octet of the STA address
15:8	STATION_ADDRESS Third octet	0x00	Holds the third octet of the STA address
7:0	STATION_ADDRESS Fourth octet	0x00	Holds the fourth octet of the STA address

5.13.13STA Address 2

MAC 0 Address: 0x19000044
MAC 1 Address: 0x1A000044
Access: Read/Write
Reset Value: 0X0000_0000

Bit	Name	Default	Description
15:8	STATION_ADDRESS Fifth octet	0x00	Holds the fifth octet of the STA address
7:0	STATION_ADDRESS Sixth octet	0x00	Holds the sixth octet of the STA address

5.13.14Transmit FIFO Threshold

MAC 0 Address: 0x19000054
MAC 1 Address: 0x1A000054
Access: Read/Write

Bit	Name	Description
31:25	RES	Reserved
24:16	Tx FIFO Full Threshold	Tx FIFO full threshold This value must be set to (2048 – x)/4, where x is the largest buffer that will queue up associated with a single Tx descriptor.
15:9	RES	Reserved
8:0	Tx FIFO Empty Threshold	Tx FIFO empty threshold For store and forward operations (safest), this value should be set to 0x1FF. For transmit to start once x bytes of data are in the Tx FIFO, set this value to x/4.

5.13.15Rx Filter Match

MAC 0 Address: 0x19000058
MAC 1 Address: 0x1A000058
Access: Read/Write

Bit	Description	
31:18	Reserved	
17	Unicast MAC address match	In combination with "Rx Filter Mask", bits [17:0] of this register control which frames are dropped and which are sent to the DMA engine. If the bit is set in "Rx Filter Mask" and it does not match the value in this bit, then the frame is dropped.
16	Truncated frame	
15	VLAN tag	
14	Unsupported op-code	
13	Pause frame	
12	Control frame	
11	Long event	
10	Dribble nibble	
9	Broadcast	
8	Multicast	
7	OK	
6	Out of range	
5	Length mismatch	
4	CRC error	
3	Code error	
2	False carrier	
1	RX_DV event	
0	Drop event	

5.13.16Rx Filter Mask

MAC 0 Address: 0x1900005C
MAC 1 Address: 0x1A00005C
Access: Read/Write

Bit	Name	Description
31:20	RES	Reserved
19	Byte/Nibble	Should be set to 1 in GMII mode and 1000 Mbps RGMII mode. Should be set to 0 in MII, RMII, or 10/100 Mbps RGMII mode.
18	Short Frame	If set to 1, all frames under 64 bytes are dropped.
17:0	Rx Filter	If set in this vector, the corresponding field must match exactly in "Rx Filter Match" for the packet to pass on to the DMA engine.

Table 5-15. **Rx Statistics Vector**

Bit	Description
15	Rx frame truncated
14	Rx long event
13	Rx VLAN tag detected
12	Rx unsupported op-code
11	Rx pause control frame
10	Rx control frame
9	Rx dribble
8	Rx broadcast: The packet's destination address contains a broadcast address
7	Rx multicast: The packet's destination address contains a multicast address
6	Rx OK: The frame contained a valid CRC and does not produce a code error

Table 5-15. **Rx Statistics Vector (continued)**

Bit	Description
5	Rx length out of range: The frame length was > 1518 bytes but < the max. frame length
4	Rx length check error: The packet's frame length does not match the actual data length.
3	Rx code error: One or more attempts were signalled as errors during packet reception.
2	Rx false carrier: After the last Rx statistics vector, a false carrier was detected, noted, and reported with these Rx statistics. False carrier activity (Rx channel activity that does not result in a packet receive attempt) is not associated with this packet.
1	Rx RX_DV event: The last Rx event was not long enough to be valid
0	Rx previous packet dropped

5.14 DMA Registers

Table 5-16 summarizes the AR7100 DMA registers.

Table 5-16. **DMA Register Summary**

MAC 0 Address	MAC 1 Address	Name	Description	Page
0x19000180	0x1A000180	DMA_TX_CTRL	Transmit Control	page 97
0x19000184	0x1A000184	DMA_TX_DESCRIPTOR	Pointer to Transmit Descriptor	page 97
0x19000188	0x1A000188	DMA_TX_STATUS	Transmit Status	page 98
0x1900018C	0x1A00018C	DMA_RX_CTRL	Receive Control	page 98
0x19000190	0x1A000190	DMA_RX_DESCRIPTOR	Pointer to Receive Descriptor	page 98
0x19000194	0x1A000194	DMA_RX_STATUS	Receive Status	page 99
0x19000198	0x1A000198	DMA_INTR_MASK	Interrupt Mask	page 99
0x1900019C	0x1A00019C	DMA_INTERRUPT	Interrupts	page 100

5.14.1 Transmit Control (DMA_TX_CTRL)

MAC 0 Address: 0x19000180
MAC 1 Address: 0x1A000180
Access: Read/Write
Reset Value: 0x0000_0000

Bit	Name	Default	Description
31:1	RES	—	Reserved
0	TX_ENABLE	0	Allows the DMA to transmit packets. The DMA controller clears this bit when it encounters a Tx underrun or bus error state.

5.14.2 Pointer-to-Tx Descriptor (DMA_TX_DESCRIPTOR)

MAC 0 Address: 0x19000184
MAC 1 Address: 0x1A000184
Access: Read/Write
Reset Value: 0x0000_0000

Bit	Name	Default	Description
31:16	DESCRIPTOR ADDRESS [31:16]	0	The descriptor address. When TX_ENABLE (bit [0] of the "Transmit Control (DMA_TX_CTRL)" register) is set by the host, the DMA controller reads this register to find the host memory location of the first Tx packet descriptor.
15:2	DESCRIPTOR ADDRESS [15:2]		
1:0	RES	0	Reserved

5.14.3 Tx Status (DMA_TX_STATUS)

MAC 0 Address: 0x19000188
MAC 1 Address: 0x1A000188
Access: Read/Write-one-to-clear
Reset Value: 0x0000_0000

Shows the status of Tx packet transfers.

Bit	Name	Default	Description
31:24	RES	—	Reserved
23:16	TX_PKT_COUNT	0	This 8-bit Tx packet counter increments when the DMA controller transfers a packet successfully, and decrements when the host writes a 1 to TX_PKT_SENT (bit [0]).
15:4	RES	—	Reserved
3	BUS_ERROR	0	Indicates that the DMA controller received a host/slave split, error, or retry response.
2	RES	—	Reserved
1	TX_UNDERRUN	0	This bit is set when the DMA controller reads a set empty flag in the descriptor it is processing.
0	TX_PKT_SENT	0	Indicates that one or more packets transferred successfully. This bit is cleared when TX_PKT_COUNT (bits [23:16]) is zero. Writing a 1 to this bit reduces TX_PKT_COUNT by one.

5.14.4 Rx Control (DMA_RX_CTRL)

MAC 0 Address: 0x1900018C
MAC 1 Address: 0x1A00018C
Access: Read/Write
Reset Value: 0x0000_0000

Bit	Name	Default	Description
31:1	RES	—	Reserved
0	RX_ENABLE	0	Allows the DMA to receive packets. When set, the built-in DMA controller begins receiving packets as the FIFO indicates they are available. The DMA controller clears this bit when it encounters an Rx overflow or bus error state.

5.14.5 Pointer-to-Rx Descriptor (DMA_RX_DESCRIPTOR)

MAC 0 Address: 0x19000190
MAC 1 Address: 0x1A000190
Access: Read/Write
Reset Value: 0x0000_0000

Bit	Name	Default	Description
31:16	DESCRIPTOR ADDRESS [31:16]	0	The descriptor address. When RX_ENABLE (bit [0] of the "Rx Control (DMA_RX_CTRL)" register) is set by the host, the DMA controller reads this register to find the host memory location of the first Rx packet descriptor.
15:2	DESCRIPTOR ADDRESS [15:2]		
1:0	RES	0	Reserved

5.14.6 Receive Status (DMA_RX_STATUS)

MAC 0 Address: 0x19000194
MAC 1 Address: 0x1A000194
Access: Read/Write-one-to-clear
Reset Value: 0x0000_0000

Shows the status of Tx packet transfers.

Bit	Name	Default	Description
31:24	RES	—	Reserved
23:16	RX_PKT_COUNT	0	This 8-bit Rx packet counter increments when the DMA controller transfers a packet successfully, and decrements when the host writes a 1 to RX_PKT_RECEIVED (bit [0]).
15:4	RES	—	Reserved
3	BUS_ERROR	0	Indicates that the DMA controller received a host/slave split, error, or retry response.
2	RES	—	Reserved
1	RX_OVERFLOW	0	This bit is set when the DMA controller reads a set empty flag in the descriptor it is processing.
0	RX_PKT_RECEIVED	0	Indicates that one or more packets transferred successfully. This bit is cleared when RX_PKT_COUNT (bits [23:16]) is zero. Writing a 1 to this bit reduces RX_PKT_COUNT by one.

5.14.7 Interrupt Mask (DMA_INTR_MASK)

MAC 0 Address: 0x19000198
MAC 1 Address: 0x1A000198
Access: Read/Write
Reset Value: 0x0000_0000

Setting a bit to 1 enables the corresponding status signal as an interrupt source. The register "Interrupts (DMA_INTERRUPT)" is the AND of DMA status bits with this register.

Bit	Name	Default	Description
31:8	RES	—	Reserved
7	BUS_ERROR_MASK	0	Enables BUS_ERROR (bit [3] in the "Receive Status (DMA_RX_STATUS)" register) as an interrupt source.
6	RX_OVERFLOW_MASK	0	Enables RX_OVERFLOW (bit [1] in the "Receive Status (DMA_RX_STATUS)" register) as an interrupt source.
5	RES	—	Reserved
4	RXPKT_RECEIVED_MASK	0	Enables RX_PKT_RECEIVED (bit [0] in the "Receive Status (DMA_RX_STATUS)" register) as an interrupt source.
3	BUS_ERROR_MASK	0	Enables BUS_ERROR (bit [3] in the "Tx Status (DMA_TX_STATUS)" register) as an interrupt source.
2	RES	—	Reserved
1	TX_UNDERRUN_MASK	0	Enables TX_UNDERRUN (bit [1] in the "Tx Status (DMA_TX_STATUS)" register) as an interrupt source.
0	TX_PKT_SENT_MASK	0	Enables TX_PKT_SENT (bit [0] in the "Tx Status (DMA_TX_STATUS)" register) as an interrupt source.

5.14.8 Interrupts (DMA_INTERRUPT)

MAC 0 Address: 0x1900019C
MAC 1 Address: 0x1A0009C
Access: Read-Only
Reset Value: 0x0000_0000

Flags in this register clear when their corresponding Status bit is cleared.

Bit	Name	Default	Description
31:8	RES	—	Reserved
7	BUS_ERROR_MASK	0	Records a Rx bus error interrupt when BUS_ERROR (bit [3] in the "Receive Status (DMA_RX_STATUS)" register) and BUS_ERROR_MASK (bit [7] of the "Interrupt Mask (DMA_INTR_MASK)" register) are both set.
6	RX_OVERFLOW_MASK	0	Records a Rx overflow error interrupt when RX_OVERFLOW (bit [1] in the "Receive Status (DMA_RX_STATUS)" register) and RX_OVERFLOW_MASK (bit [6] of the "Interrupt Mask (DMA_INTR_MASK)" register) are both set.
5	RES	—	Reserved
4	RXPKT_RECEIVED_MASK	0	Records a RX_PKT_RECEIVED error interrupt when RX_PKT_RECEIVED (bit [0] in the "Receive Status (DMA_RX_STATUS)" register) and RXPKT_RECEIVED_MASK (bit [4] of the "Interrupt Mask (DMA_INTR_MASK)" register) are both set.
3	BUS_ERROR_MASK	0	Records a BUS_ERROR (bit [3] in the "Tx Status (DMA_TX_STATUS)" register) and BUS_ERROR_MASK (bit [3] of the "Interrupt Mask (DMA_INTR_MASK)" register) are both set.
2	RES	—	Reserved
1	TX_UNDERRUN_MASK	0	Records a TX_UNDERRUN (bit [1] in the "Tx Status (DMA_TX_STATUS)" register) and TX_UNDERRUN_MASK (bit [1] of the "Interrupt Mask (DMA_INTR_MASK)" register) are both set.
0	TX_PKT_SENT_MASK	0	Records a TX_PKT_SENT (bit [0] in the "Tx Status (DMA_TX_STATUS)" register) and TX_PKT_SENT_MASK (bit [0] of the "Interrupt Mask (DMA_INTR_MASK)" register) are both set.

5.15 DMA Descriptor Definitions

Before DMA transfers can process, host memory must initialize two sets of descriptors: one for Tx and the other for Rx operations. Each descriptor set is a linked list that is typically closed to form a ring buffer. At the start of any transfer sequence, the DMA Tx/Rx descriptor register chooses the descriptor that provides the entry point into the buffer. Each descriptor is comprised of three 32-bit memory locations. See Table 5-17.

Table 5-17. **Descriptor Components**

Address	Name	Description	Page
0	PACKET_START_ADDR	Start Address for the Packet Data	page 101
4	PACKET_SIZE	Size of Packet, Overrides, and Empty Flag	page 101
8	NEXT_DESCRIPTOR	Next Descriptor Location	page 101

5.15.1 Packet Data Start Address (PACKET_START_ADDR)

Offset: 0
Access: Read/Write

Start addresses used in descriptor sequences must allow sufficient room in any location for a packet of the maximum size transferred.

Bit	Name	Description
31:16	PACKET START ADDRESS [31:16]	The DMA controller reads this field to find the host memory location of the first byte of data.
15:2	PACKET START ADDRESS [15:2]	
1:0	RES	Reserved. Default is 0.

5.15.2 Size of Packet, Overrides, and Empty Flag (PACKET_SIZE)

Offset: 4
Access: Read/Write

Bit	Name	Description		
31	EMPTY_FLAG	Validates the descriptors		
		Tx	Indicates the associated data's availability with the packet. On a successful Tx operation, the DMA controller writes a 1 to this location to indicate the associated data has transferred, ensuring that data cannot be transferred twice.	
		Rx	Indicates the specified location's availability to store the received packet. On a successful Rx operation, the DMA controller writes a 0 to this location to indicate the location was stored the received packet, ensuring that received data is not overwritten.	
30:25	RES	Reserved		
24	MORE	(Tx only) This more bit is set if the buffer is not the last fragment in a packet		
23:21	RES	Reserved		
20:16	FTPP_OVERRIDES	This five-bit field contains the per-packet override flags signaled to the FIFO during packet transmission. The bits are encoded as:		
		20	FTCFRM	FIFO Tx control frame
		19:18	FTPPPADMODE	FIFO Tx per-packet PAD mode
		17	FTPPGENFCS	FIFO Tx per-packet generate FCS
		16	FTPPEN	FIFO Tx per-packet enable
15:12	RES	Reserved		
11:0	PACKET_SIZE	Tx	Gives the size of packet to transfer in bytes	
		Rx	The DMA controller writes the number of received bytes to this field; the value of this field prior to the transfer is ignored	

5.15.3 Next Descriptor Location (NEXT_DESCRIPTOR)

Offset: 8
Access: Read/Write

Bit	Name	Default	Description
31:16	DESCRIPTOR ADDRESS [31:16]	—	The DMA controller reads this field to find the descriptor's host memory location for the next packet in the sequence. These descriptors should form a closed link list.
15:2	DESCRIPTOR ADDRESS [15:2]		
1:0	RES	0	Reserved

5.16 SPI Registers

Table 5-18 summarizes the SPI registers for the AR7100.

Table 5-18. **SPI Register Summary**

Offset	Description	Page
0x1F00000	Function Select	page 102
0x1F00004	SPI Control	page 102
0x1F00008	SPI I/O Control	page 103
0x1F0000C	SPI Read Data Shift	page 103

5.16.1 Function Select

Offset: 0x000
Access: Read/Write
Reset: 0

Bit	Description	
31:1	RES	Reserved, must be zero
0	0	When this bit is set to 0, reading from this register reads the contents of the serial flash. Writes to locations in other SPI registers have no effect if this bit is set to 0.
	1	Writing a one value to this bit selects GPIO mode for the SPI controller. In GPIO mode, other SPI registers are visible.

5.16.2 SPI Control

Offset: 0x004
Access: Read/Write
Reset: See field descriptions

Bit	Name	Reset	Description
31:7	RES	0	Reserved
6	REMAP_DISABLE	0	Disables the alias of the lower 4 MB of SPI space, thus enabling the ROM to boot from 1FC_0000 to alias 1F0_0000 until software disables aliasing.
5:0	CLOCK_DIVIDER	6	The clock divider setting is based on the AHB clock. The generated clock is AHB Clock / (2 << CLOCK DIVIDER).

5.16.3 SPI I/O Control

Offset: 0x008
Access: Read/Write
Reset: 0

Bit values of this register are mapped directly to the pins.

Bit	Name	Description
31:19	RES	Reserved
18	CS_2	SI_CS2_L (maps to GPIO 1)
17	CS_1	SI_CS1_L (maps to GPIO 0)
16	CS_0	SPI_CS_L
15:9	RES	Reserved
8	CLK	SPI_CLK
7:1	RES	Reserved
0	DO	SPI_MO_SI

5.16.4 SPI Read Data Shift

Offset: 0x00C
Access: Read/Write
Reset: 0

Bit	Name	Description
31:0	READ_DATA	Read data is shifted and sample every cycle

6. Package Dimensions

The AR7100 is packaged in a JEDEC M0-195 384LD TFBGA package. The body size is 13 mm by 13 mm. The package drawings and dimensions are provided in Figure 6-1, and Table 6-1.

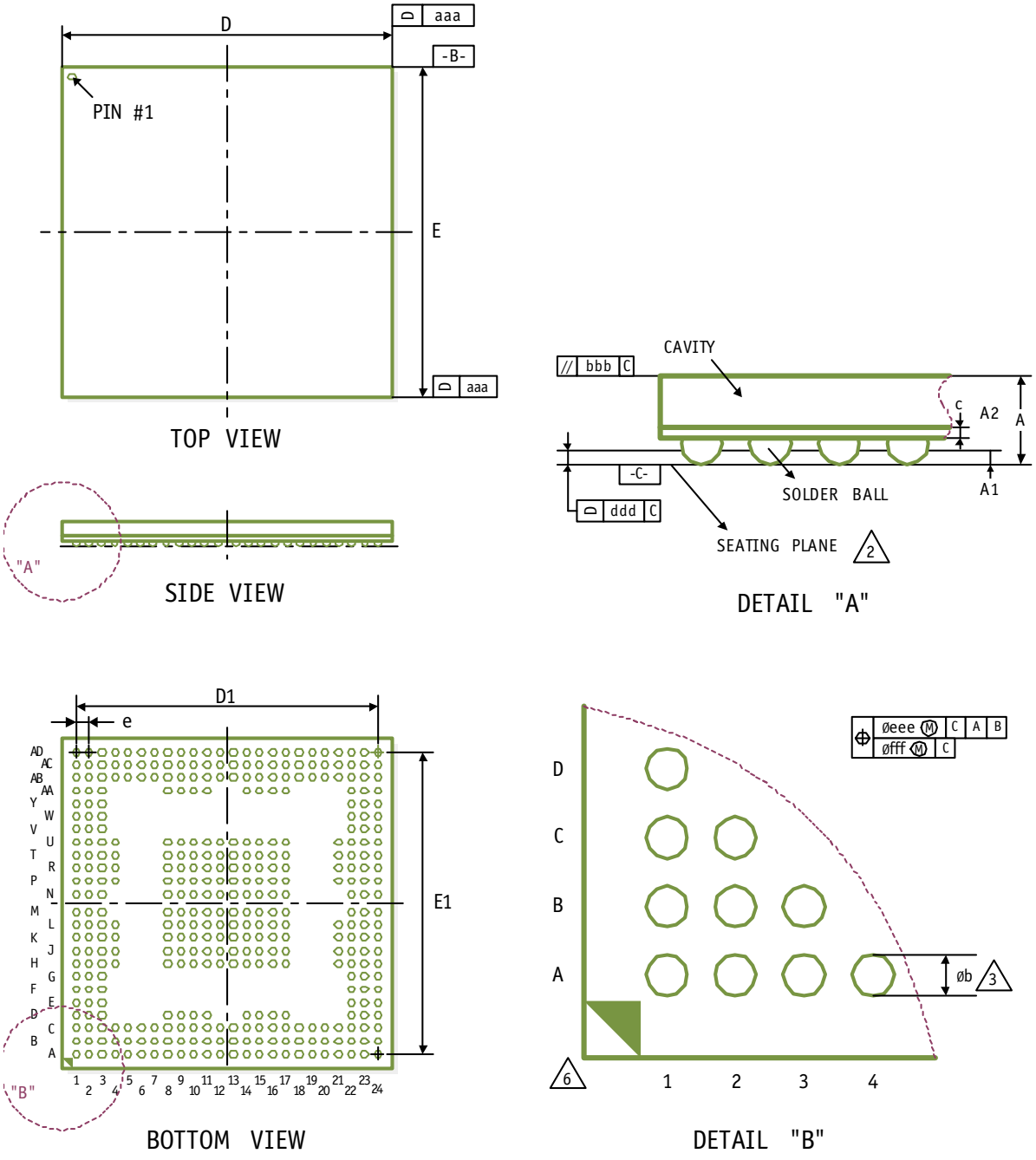


Figure 6-1. **Package Views**

Table 6-1. **Package Dimensions**

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	—	—	1.20	mm	—	—	0.047	inches
A1	0.16	0.21	0.26	mm	0.006	0.008	0.010	inches
A2	0.84	0.89	0.94	mm	0.033	0.035	0.037	inches
c	0.32	0.36	0.40	mm	0.013	0.014	0.016	inches
D	12.90	13.00	13.10	mm	0.508	0.512	0.516	inches
E	12.90	13.00	13.10	mm	0.508	0.512	0.516	inches
D1	—	11.50	—	mm	—	0.453	—	inches
E1	—	11.50	—	mm	—	0.453	—	inches
e	—	0.50	—	mm	—	0.020	—	inches
b	0.25	0.30	0.35	mm	0.010	0.012	0.014	inches
aaa		0.10		mm		0.004		inches
bbb		0.10		mm		0.004		inches
ddd		0.08		mm		0.003		inches
eee		0.15		mm		0.006		inches
fff		0.05		mm		0.002		inches
MD/ME		24/24				24/24		

Notes:
1. The controlling dimension is mm.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane C.
4. There shall be a minimum clearance of 0.25 mm between the edge of the solder ball and the body edge.
5. Reference document: JEDEC MO-195
6. The pattern of pin 1 fiducial is for reference only.
7. Special characteristics for C class: bbb, ddd.

7. Ordering Information

The following specifies BGA, lead-free, standard temperature range versions of the AR7100:

AR7130-BC1A, 300 MHz

AR7141-BC1A, 400 MHz

AR7161-BC1A, 680 MHz

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