JTAG Overview

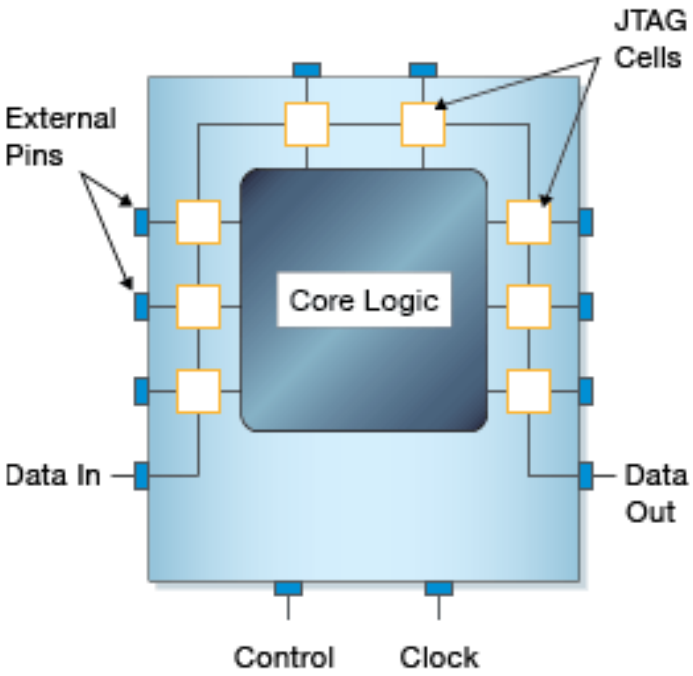
- JTAG Benefits
  - Low Cost
  - Ease of testing
- Physical Components
  - TAP, BSR
- JTAG Pins
  - TDI, TDO, TMS, TCK, TRST
- JTAG Modes
  - Bypass, ExTest, InTest

JTAG Introduction

- JTAG allows for the testing and programming of independent modules through a single, common, port.
- IEEE standard that gives a standard for how interconnected modules in a digital design can be tested.
- Has also been extended with the “Boundary-Scan-Based In-System Configuration of Programmable Devices” standard.
  - This extension includes on-board programming through the JTAG standard instead of just testing.
- IEEE Std. 1149.1, Standard Test Access Port and Boundary Scan Architecture
- IEEE Std. 1532, Boundary-Scan-Based In-System Configuration of Programmable Devices

Goals/Benefits of JTAG

- Low Cost
- Inter-circuit testing without need of physical test-probes
- Increased fault detection coverage
- Lower test time



- The image shows how a single JTAG enabled module may be designed.
  - Each pin on the module has a JTAG cell, these cells are then connected to the JTAG “Data-in” and “Data-Out” pins.
  - The input pins and output pins are loaded or read serially through that “Data-in” and “Data-out” pins.

Goals/Benefits of JTAG

- Allow access to individual modules directly.
- Gets rid of the need for physical connections in testing.
  - To test a specific module in a design, you would have to force inputs and read outputs by directly connecting to those input and output pins.
  - JTAG allows you use the standard JTAG port, target the module you want to test, and read back the responses form those tests without using physical probes.
- JTAG also increases fault detection in a circuit.
  - You can specify the module where a fault is occurring, and also allows you to test individual modules throughout the different steps in the lifecycle of the IC(Fabrication, Packaging, Integration, etc).

Goals/Benefits of JTAG

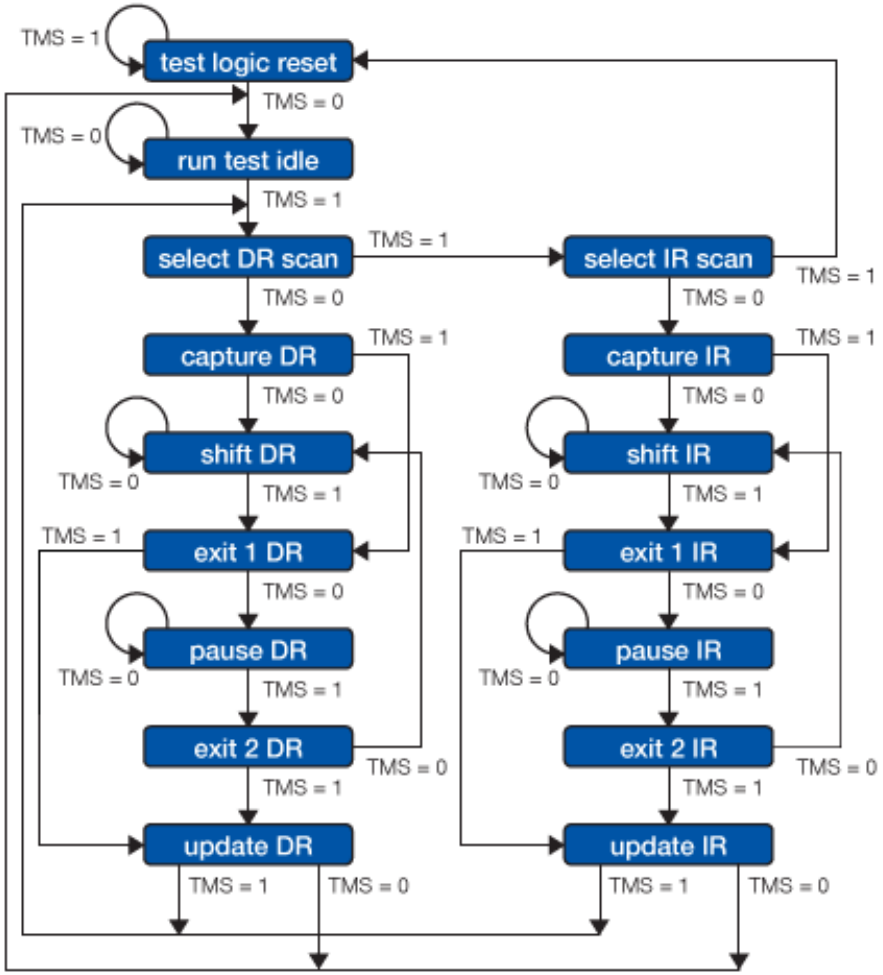
- JTAG can also help lower test times by allowing access to a specific module.
  - Instead of having many test vectors that achieve the function of a certain module, you can directly input that module with the test data you want.
  - This decreases the number of test-vectors needed to fully test a module, and the complexity in coming up with those test vectors.

Physical Components

- JTAG requires two added physical components. A TAP and BSR's
- The Tap of a JTAG system is used to control the operation of the JTAG. The tap includes an internal State machine that allows the control of necessary JTAG signals.
- The BSR's are registers added to the pins of the modules in the JTAG system. The registers allow for data to be loaded in and read out of the input and output pins on a module through a single, serial, JTAG connection.
- To go along with the physical setup of a JTAG system, JTAG modules are typically connected in series. There will be common signals between them, but typically data will have to move through each module to get from input to output.

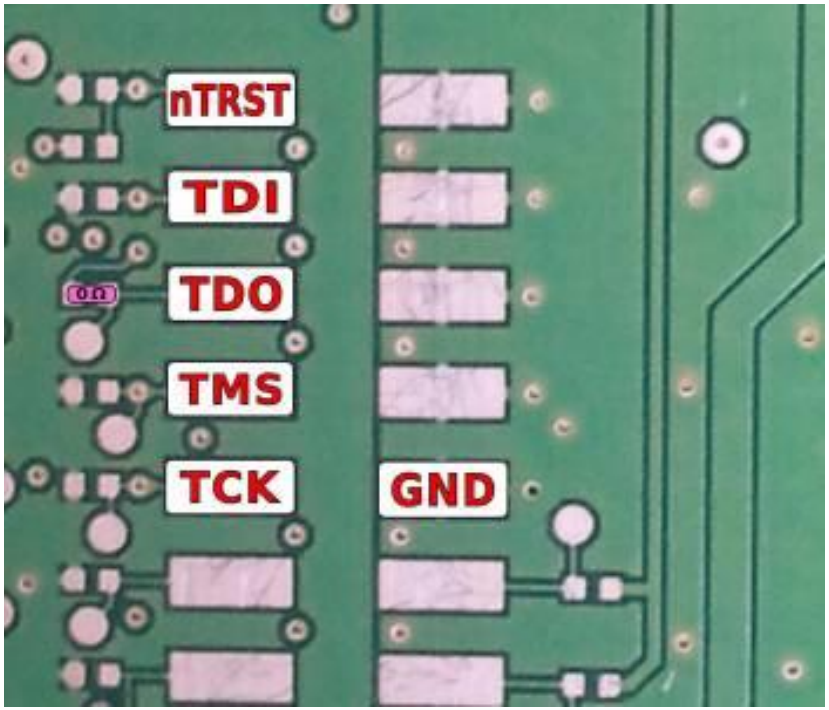
Physical Components

- TAP
  - Test Access Port
  - Interprets JTAG protocol
  - Controlled by TMS signal
- BSR
  - Boundary Scan Registers
  - Between module and TAP



JTAG Control

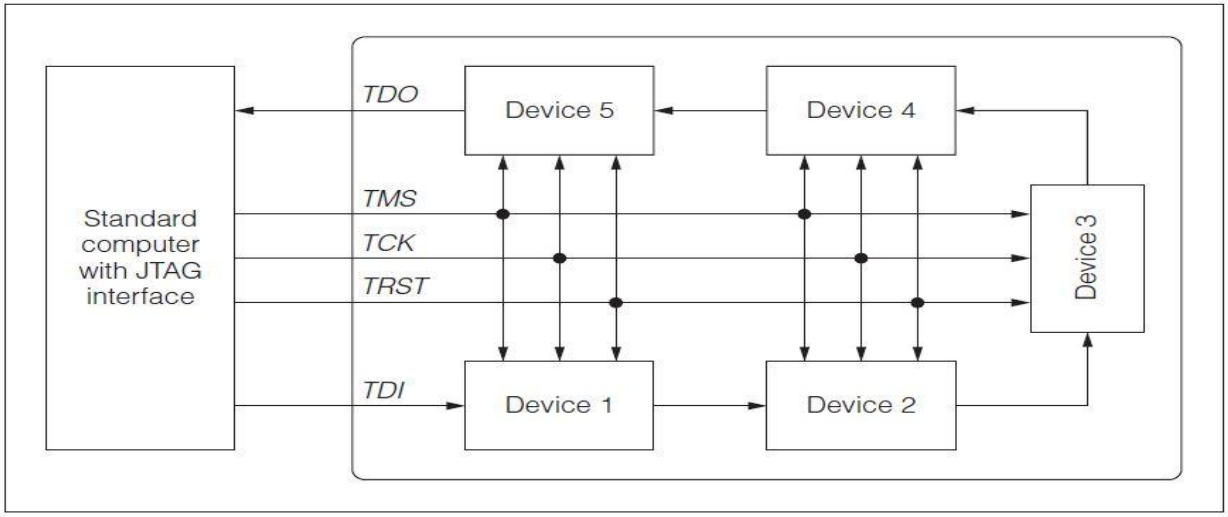
- The JTAG interface is run by five signals. These five pins allow the input of data, the reading of data, and the input of instruction/tests to be run.
  - TDO: Test Data Output
  - TDI: Test Data Input
  - TMS: Test Mode Select
  - TCK: Test Clock
  - TRST :Resets TAP Controller
- TDO and TDI are read serially based on the test clock.
- TMS controls the operation of the 16 state FSM inside the TAP.
- And TRST resets the TAP controller to known state.



JTAG Modes

- There are three required modes for all JTAG modules. Bypass allows a module to be ignored, and ExTest and InTest are ways of testing a module
- Each component in a JTAG system can be put into one of the three basic, JTAG modes.
  - The Bypass mode simply connects the TDI of a module to the TDO of a module. This allows a module in the JTAG chain to be bypassed so that a single module, or a group of modules can be targeted and tested.
  - ExTest mode takes data from the TDI pin and loads the output of a module serially. The inputs of that module are then read serially through the TDO pin.
  - InTest mode loads the input pins of a module, serially through the TDI pin, and reads the data from the output pins, serially through the TDO pin.
- A JTAG system is typically made up of JTAG components in series. This is why a bypass mode is necessary to isolate specific modules.

JTAG Modes



- Bypass
  - Connects TDI to TDO
  - One cycle delay
- ExTest
  - Asserts data on output pins
  - Reads data from input pins
- InTest
  - Asserts data on input pins
  - Reads data from output pins