ECCS-3241
Embedded Hardware-Software Codesign

Embedded Platform & Memory Interfacing

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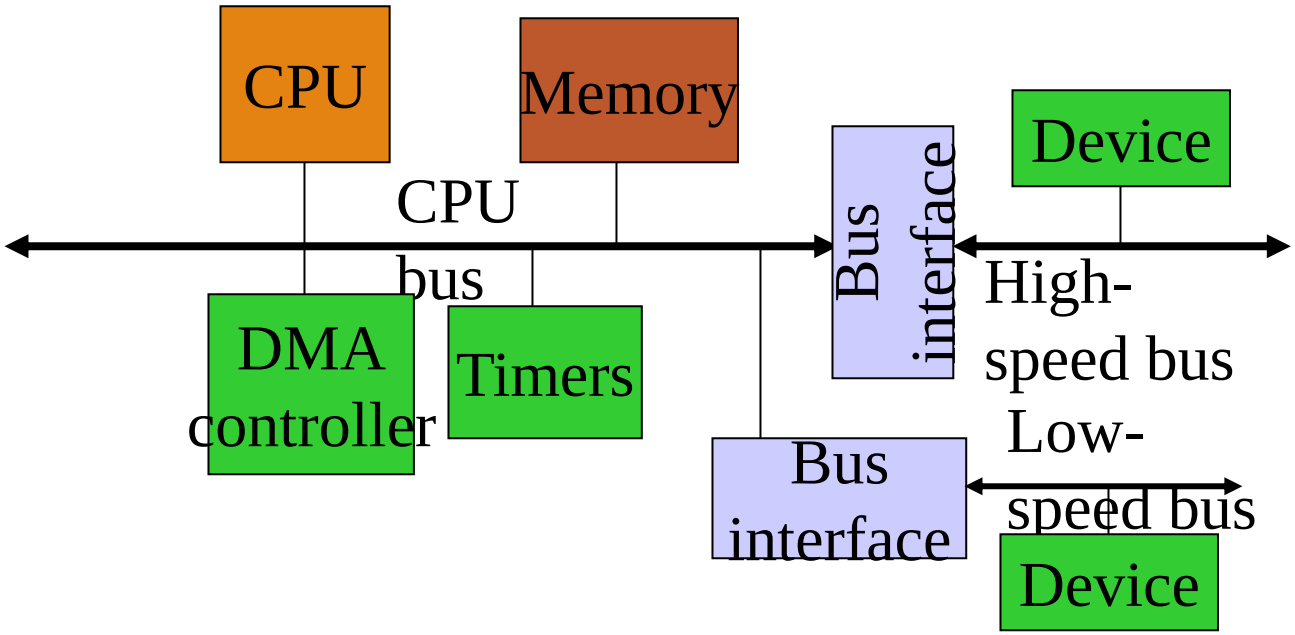
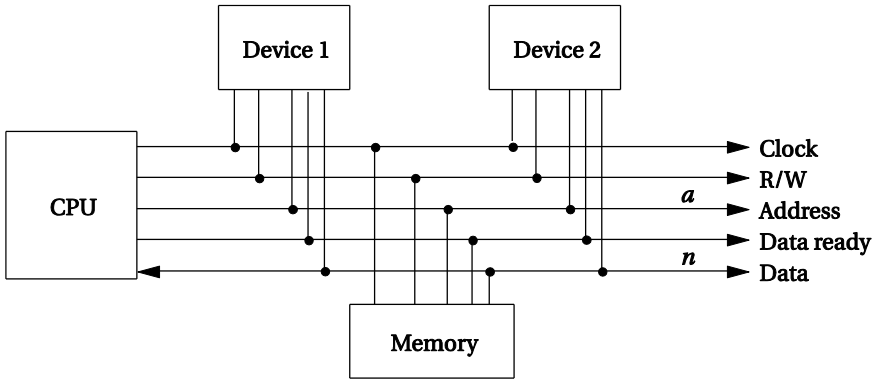
Embedded platform components



DMA: Direct Memory Access

Simpler representation of embedded platform

- Clock provides synchronization.
- R/W is true when reading (R/W' is false when writing).
- Address is a-bit bundle of address lines (bus).
- Data is n-bit bundle of data lines.
- Data ready signals when n-bit data is ready.



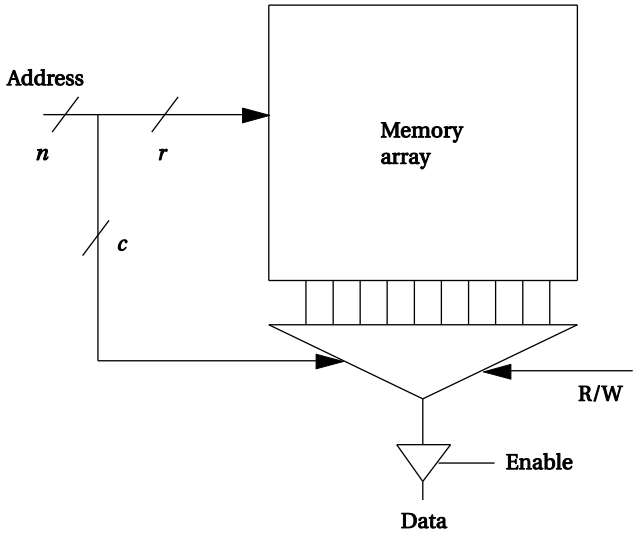
Memory Structure

Several different types of memory used in the system:

- DRAM.
- SRAM.
- Flash.
- EEPROM.

Each type of memory comes in varying:

- Capacities.
- Widths.

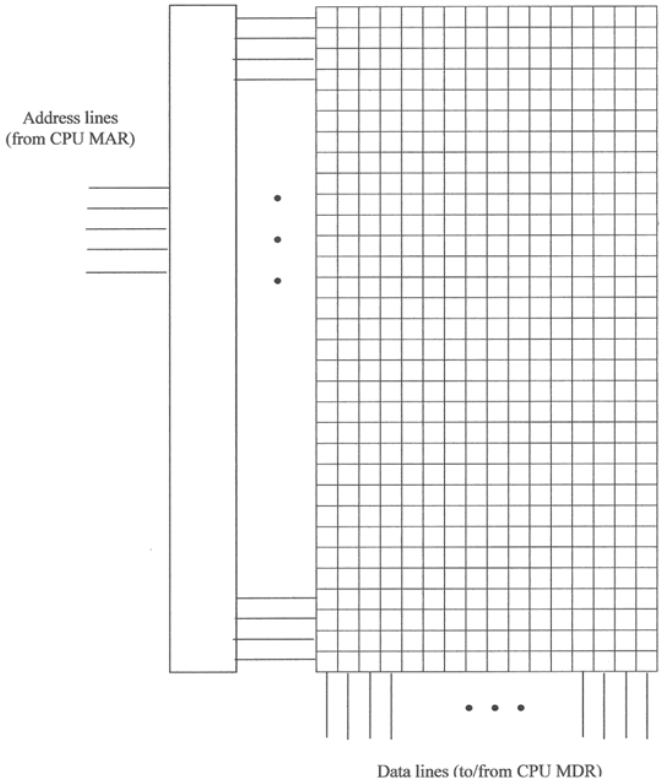


Memory Organization

- The memory of a computer consists of a large number of 1-bit storage devices organized into words.
- The number of bits in a word varies with the computer design.
- In modern computers, the memory word size is a power of two (8, 16, 32, or 64)
- The structure of memory can be described by specifying the number of bits in a word, and the number of words.
- The next slide shows the organization of a 16 x 32 memory.

16 x 32 memory

- The word length is 16, and the number of words is 32.
- For each bit position in the word, a data line connects the memory to the Memory Data Register in the CPU.
- The **data line** for a bit position carries data to or from one of the bits in the corresponding bit position.
- To specify a particular word in the memory, the *address* of the word is given in binary.
- In the example shown, the words are numbered 0 to 31, which in binary.
- Five lines, called *address lines*, carry the address from the CPU's Memory Address Register to the memory.



Memory Organization

In general:

- If a memory contains words that are *n* bits long, then *n* data lines are required.
- If a memory contains 2^k words, then *k* address lines are required.
- The following terminology is commonly used to refer to sizes of computer memories:
  - kilobyte (K) = 2^{10} = 1,024 bytes
  - megabyte (M) = 2^{20} = 1,048,576 bytes
  - gigabyte (G) = 2^{30} = 1,073,741,824 bytes

Memory Organization

How does the computer access a memory location corresponds to a particular address?

We observe that 4M can be expressed as $2^2 \times 2^{20} = 2^{22}$ words.

The memory locations for this memory are numbered 0 through $2^{22} - 1$.

Thus, the memory bus of this system requires at least 22 address lines.

- The address lines “count” from 0 to $2^{22} - 1$ in binary. Each line is either “on” or “off” indicating the location of the desired memory element.

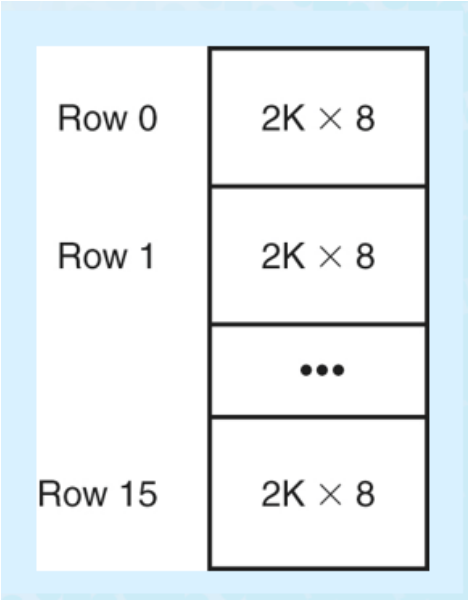
Memory Organization

- Physical memory usually consists of more than one RAM chip.
- Access is more efficient when memory is organized into banks of chips with the addresses interleaved across the chips
- With low-order interleaving, the low order bits of the address specify which memory bank contains the address of interest.
- Accordingly, in high-order interleaving, the high order address bits specify the memory bank.

Memory Organization

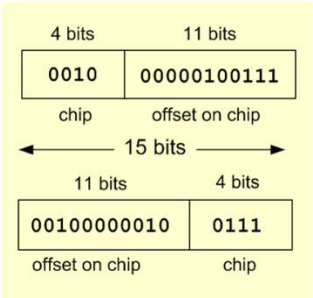
Example: Suppose we have a memory consisting of 16 2K x 8 bit chips.

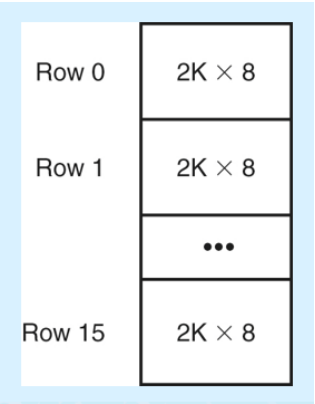
- Memory is 32K = $2^5 \times 2^{10} = 2^{15}$
- 15 bits are needed for each address.
- We need 4 bits to select the chip, and 11 bits for the offset into the chip that selects the byte.



Memory Organization

- In high-order interleaving the high-order 4 bits select the chip.
- In low-order interleaving the low-order 4 bits select the chip.





Random-access memory

Dynamic RAM is dense, requires refresh.

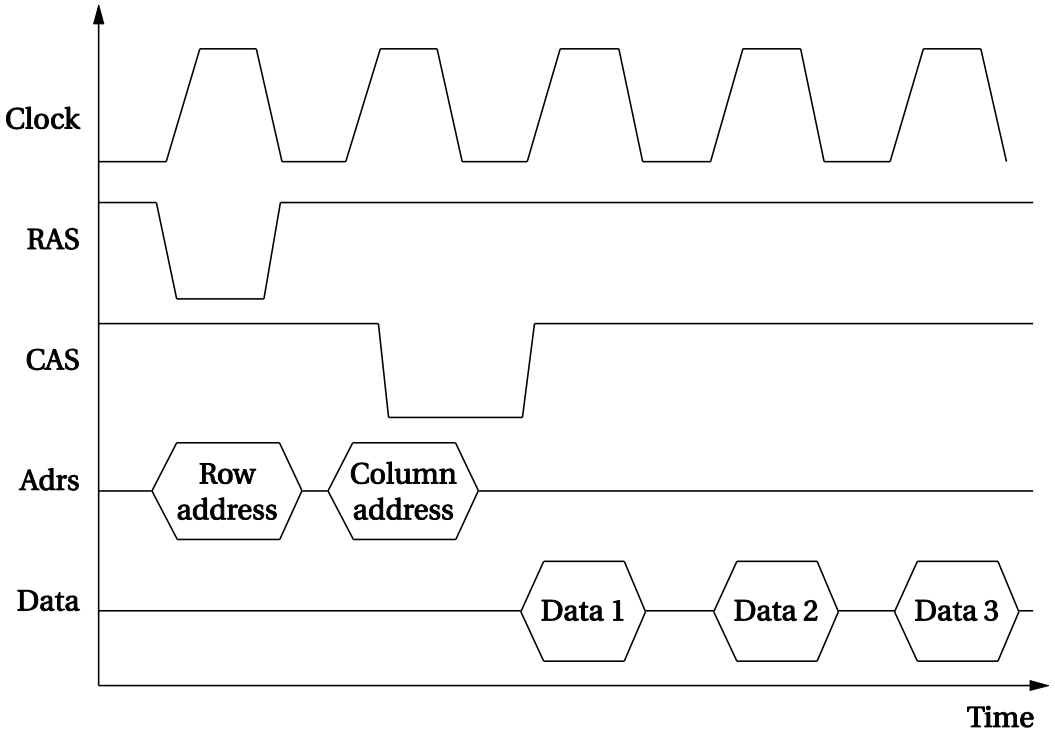
- SDRAM: synchronous DRAM.
- EDO DRAM: extended data out.
- FPM DRAM: fast page mode.
- DDR DRAM: double-data rate.

Static RAM is faster, less dense, consumes more power.

Flash memory

- Non-volatile memory
- Read operations are fast and byte/word addressable.
- Write operations takes time. Typically done in blocks.

SDRAM Read Operation



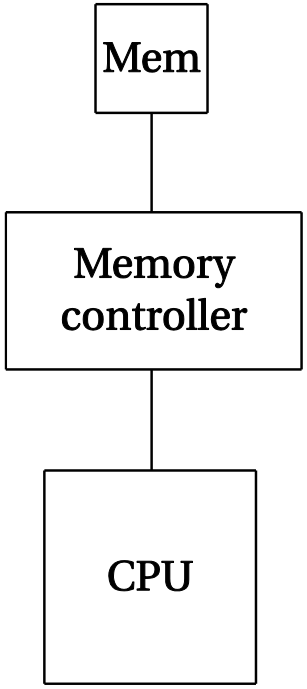
RAS&CAS: Row and Column Address strobes

Memory packaging

- SIMM: single in-line memory module.
- DIMM: dual in-line memory module.

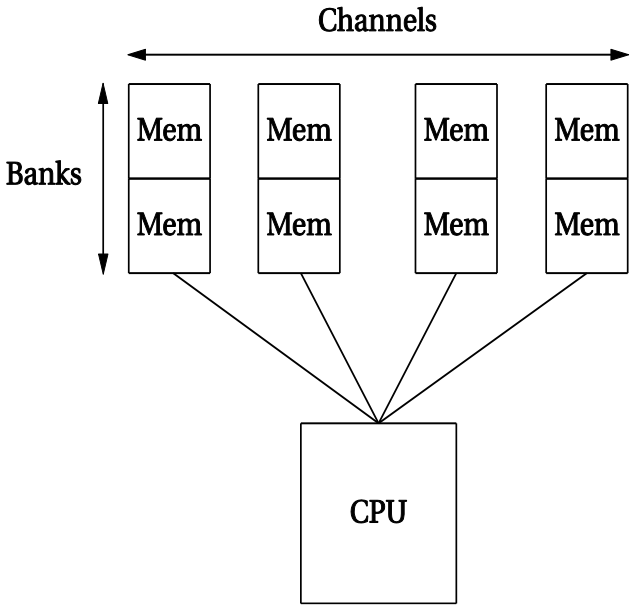
Memory systems and memory controllers

- Memory has complex internal organization.
- Memory controller hides details of memory interface, schedules transfers to maximize performance.



Channels and banks

- Channels provide separate connections to parts of memory.
- Banks are separate memory arrays.



512 Megabit SDRAM (Micron)

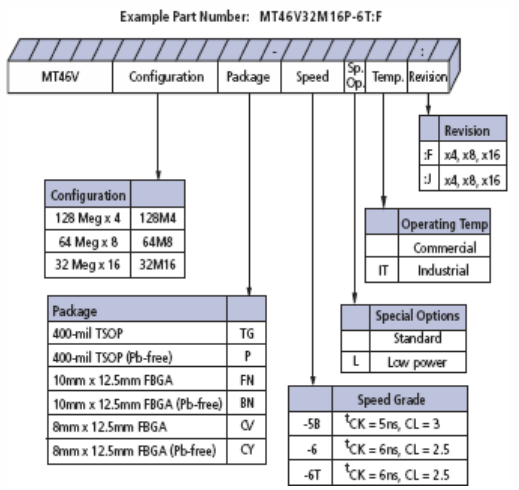
Table 2: Addressing

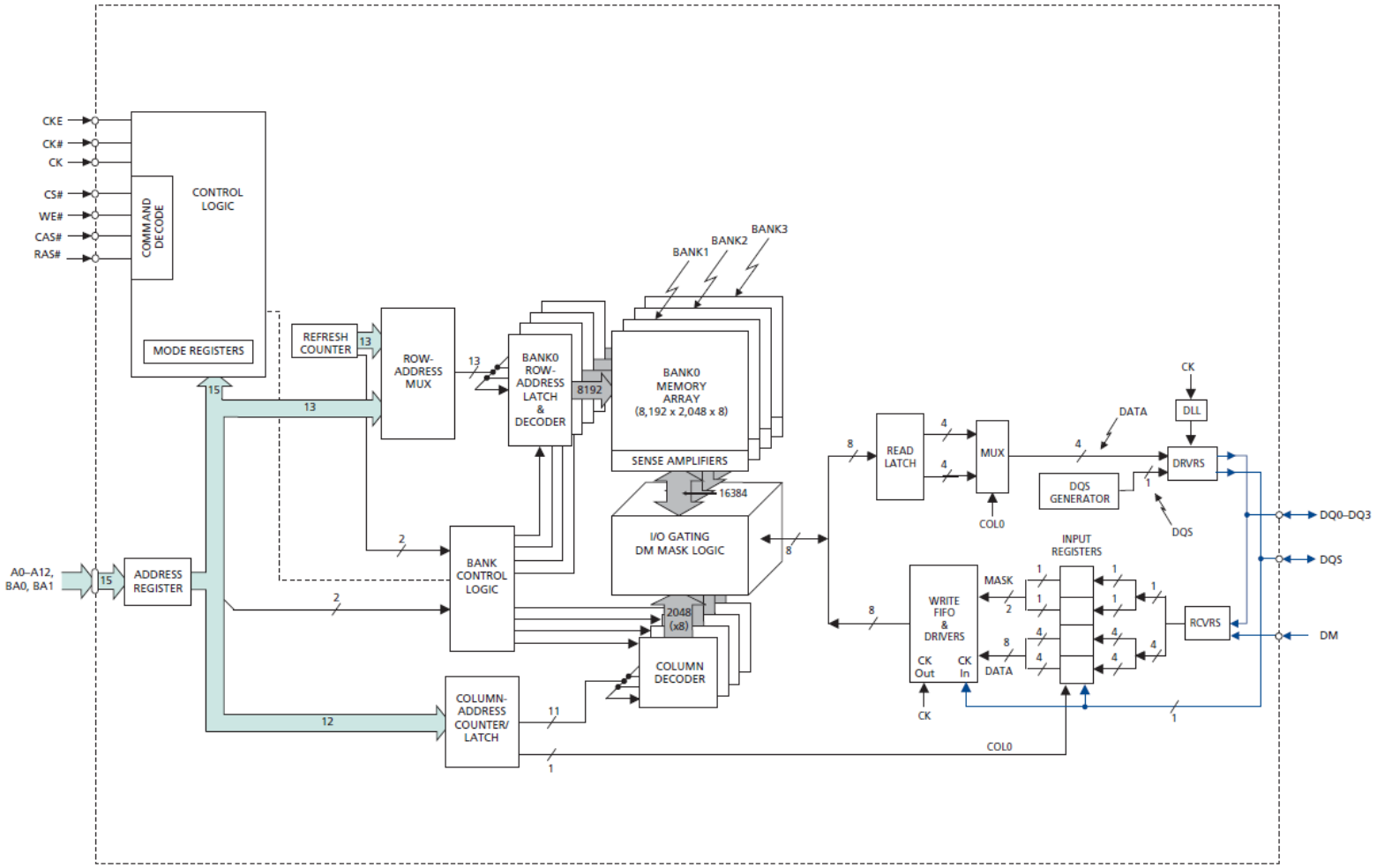
Parameter	128 Meg x 4	64 Meg x 8	32 Meg x 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row address	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)
Bank address	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column address	4K (A0–A9, A11, A12)	2K (A0-A9, A11)	1K (A0–A9)

Table 3: Speed Grade Compatibility

Marking	PC3200 (3-3-3)	PC2700 (2.5-3-3)	PC2100 (2-2-2)	PC2100 (2-3-3)	PC2100 (2.5-3-3)	PC1600 (2-2-2)
-5B[1]	Yes	Yes	Yes	Yes	Yes	Yes
-6	–	Yes	Yes	Yes	Yes	Yes
-6T	–	Yes	Yes	Yes	Yes	Yes
-75E	–	–	Yes	Yes	Yes	Yes
-75Z	–	–	–	Yes	Yes	Yes
-75	–	–	–	–	Yes	Yes
	-5B	-6/-6T	-75E	-75Z	-75	-75

Notes: 1. The -5B device is backward compatible with all slower speed grades. The voltage range of -5B device operating at slower speed grades is $V_{DD} = V_{DDQ} = 2.5V \pm 0.2V$.




CKE
CK#
CK
CS#
WE#
CAS#
RAS#
COMMAND DECODE
CONTROL LOGIC
MODE REGISTERS
REFRESH COUNTER
ROW-ADDRESS MUX
BANK0 ROW-ADDRESS LATCH & DECODER
BANK0 MEMORY ARRAY (8,192 x 2,048 x 8)
BANK1
BANK2
BANK3
SENSE AMPLIFIERS
I/O GATING DM MASK LOGIC
BANK CONTROL LOGIC
COLUMN DECODER
COLUMN-ADDRESS COUNTER/ LATCH
ADDRESS REGISTER
A0–A12, BA0, BA1
READ LATCH
MUX
COL0
DATA
DLL
DRVRS
DQS GENERATOR
DQS
DQ0–DQ3
INPUT REGISTERS
WRITE FIFO & DRIVERS
MASK
CK Out
CK In
RCVRS
DM

References

- W. WOLF – COMPUTERS AS COMPONENTS
- WWW.MICRON.COM