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Accurate Dynamic Voltage and Frequency Scaling Measurement for Low-Power Microcontrollors in Wireless Sensor Networks

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ABSTRACT

Wireless Sensor Networks (WSNs) began to permeate all facets of life thanks to low cost, inherent intelligent-processing capability, simple installation, flexible networking and low energy consumption characteristics. Also, the evaluation of real-world applications on different platforms can solve the implementation problems and contribute to broadening the spectrum of Internet of Things (IoT) applications. The purpose of this paper is to reduce the microcontroller's average consumption of a wireless sensor node through architectural and design processes using advanced technologies. This paper provides a state-of-the-art investigation on the most up-to date Dynamic Voltage and Frequency Scaling (DVFS) techniques. A benchmark is given to choose the appropriate DVFS technique according to the type of component, the time and resources constraints, the application requirements, the expected performance level, etc. An energy-saving design is implemented using an ultra-low power microcontroller MSP430 and is based on the DVFS strategy. To efficiently quantify the consumed energy and to ensure more accuracy, a new concept is introduced, which is the normalized power to offer more accuracy. Real voltage/frequency scaling measurement were conducted. We show that a high voltage/frequency can lead to up to 57% increase of the normalized-power.

1. Introduction

The advent of processors, low-power sensors, intelligent wireless networks and "Big Data" analysis tools has generated considerable interest in the Internet of Things (IoT) context [1]. Wireless Sensor Networks (WSNs), are merely a subset of the IoT topology to filter out irrelevant data and correlate data from multiple sensors. This massive data is processed in real time to allow potentially important decisions to be made [2,3]. With a large number of sensors deployed and ubiquitous in various applications, WSNs are becoming increasingly complex. They integrate many functionalities including image analytics and video streaming [4]. Meanwhile, the expansion of applications requires greater processing ability of such embedded system. The large volume of data, the complexity of applications and the necessary processing speed require increasingly sophisticated dedicated analysis tools and also a large amount of energy [5]. Many WSNs are battery-powered with limited energy resource [6,7]. In various critical applications, changing depleted nodes batteries becomes very costly and, in some cases, dangerous. This rising application requirements, coupled with battery autonomy challenges, puts even greater pressure on already constrained energy resources in WSNs. The power management strategies are the key to boosting efficiency in WSNs.

Various energy management techniques are implemented and developed to ensure the autonomy and the operability of these WSNs systems [8–12]. Different techniques are used to reduce the consumption of the node for example running the node in duty-cycle [13,14]. The node will run over a short period of activity and will be put into the lowest consumption mode the rest of the time. Although the most energy-consuming element in the node remains the radio that is why it is awakened only when necessary. The microcontroller (MCU) also consumes an important part of the total energy of a sensor node.

The challenge is also to generate very low voltages and very low currents during the idle phases and high currents during the active phases for the MCU, sensors and radios. To this end, well known approaches try to achieve this goal such as painstaking software optimization [15], parallel processing [10] or hardware acceleration [16]. One of the most effective techniques is the Dynamic Voltage and Frequency Scaling (DVFS) [17]. It allows not only to reduce the power consumption but

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also to generate less heat by the considered device which minimizes the cost per unit and average time to failure. Generally, the DVFS technique can be introduced as a framework that enable the change of the frequency and the operating voltage of the processor based on the system performance requirements at a pre-set point of time [18]. To control both hardware frequency and voltage, DFVS uses kernel drivers. While increased with frequency, the voltage boosts the performance and the stability to meet processing demands, but when decreased, it impacts the performance. The CPU processes fewer instructions in a given time. To overcome this drawbacks, the normalize power is defined. The basic idea is these normalized power enables clever characterization of high-performance microcontrollers and then it helps to choose the appropriate device in adequacy with the needs of the application and the users.

The main contributions of our paper are as follows.

1. We give an overview of the different DVFS techniques in order to propose a classification and a taxonomy of existing strategies which can be used as a reference in future discussions. The taxonomy recognizes eight different levels of processing techniques for rapid assessment of energy management requirement.
2. We introduce the normalized power to accurately and efficiently calculate the energy saving of the implemented DVFS
3. We implement the proposed DVFS policy using an ultra-low power microcontroller MSP430L5529 and we will highlight energy-saving measures based on Panstamp.

The reminder of the paper is as follows. Section 2 describes, deeply, the fundamental characteristics of the DVFS techniques. The purpose of that study is to carry out a critical survey and taxonomy of such work that will guide subsequent analysis of the energy models. Section 3, involves a description of how DVFS techniques are applied in WSN field. The impact of DVFS on the energy management viability in WSNs is evaluated through a comparison and a discussion. A key element of the proposed approach in section 4 is an energy-saving design for WSN systems is implemented using an ultra-low power microcontroller MSP430 and is based on the DVFS. Section 5 describes the energy efficiency design features of the prposed DVFS approach. Section 6 concludes the paper with discussion and directions for future work.

2. Classification of DVFS techniques

The principle of DVFS is to tune different frequencies and to provide the appropriate voltage. DVFS has proved very effective in both dynamic and static power consumption. In some applications the high performance is peaking only during a small fraction of the operating time, so a significant energy savings can be achieved [19]. Real-time applications potentially have variations in their actual execution time (AET) and, therefore, often end earlier than their estimated worst case execution time (WCET). When the length of the idle period is less than the best execution time (BET) of the first low-power state, DVFS could be used [20]. DVFS techniques exploit these variations in the actual workload to dynamically adjust the voltage and frequency of the processors. Their reduction inevitably results in a decrease in CPU power due to the nature of CMOS circuits introduced in equation (1).

$$P_{dynamic} = \alpha.C_L.V^2.f \quad (1)$$

According to this equation, a linear voltage reduction V implies a quadratic reduction of the power supplied by the component. However, a decrease in V implies also a reduction in the switching speed of the CMOS transistors. This inevitably leads to a decrease in the maximum processor frequency.

When the requested frequency is not available, the processor is then required to operate at a higher frequency. The frequency below which it is no longer possible to go is often referred to as the critical frequency. To choose the most efficient low-power state, the processor must know the size of the idle period, or at least have guarantees on its minimum size [20].

DVFS techniques may be classified based on eight factors as shown in Fig. 1. According to the scaling granularity, the DVFS can be classified into two categories which are “inter-task” where the speed of each task is fixed and cannot be modified among its different instances. For Intra-task processors, CPU speed is gradually increased to ensure timely completion of real-time tasks [21].

The network policy also has multiple forms, namely local DVFS and the global DVFS. The local DVFS can set the frequency of the clock signal and the voltage for each kernel separately. The global or chip-wide DVFS sets a main voltage/frequency of the entire chip based on the activity of the whole chip, as opposed to each core [22]. The global DVFS has many advantages, including lower cost, ease of implementation and operational flexibility, while energy performance and freedom of frequency choice prevail in the local DVFS [23].

Also, minimizing the overall energy consumption meanwhile avoiding the deadline violations is crucial to achieve high performances and to enhance the reliability of the network. Hence, time constraints become an influencing factor and then strict deadlines should be ensured. The time between the detection of an anomaly and the operator intervention would prevent the incident. A particularly significant example is the fall of a person that can quickly get critical. A deep study and several experiments to reduce the energy in WSNs were already conducted [4]. The modeling of real-time systems with time constraints can be divided into two categories, hard real-time systems and mixed criticality. It depends on whether it can tolerate time overruns for different types of applications.

Efficiency depends strongly on 2 factors: energy consumption and runtime. For this reason, many works combine scheduling [3,13,20,23–25] and energy management techniques [26–29]. Consequently, combining the DVFS energy optimization techniques and scheduling is one way to increase the energy efficiency. Moreover, offline or online approaches are used to integrate the scheduling policy with DVFS. The offline techniques calculate the optimized voltage/frequency for each task before it is performed and maintain these values during operation. The algorithm finds voltage/frequency settings at each interval to minimize the power while maintaining a specified performance constraint [24]. Nevertheless, these methods imply a pessimistic optimization because the execution time of tasks is often shorter than the WCET. For online methods, the voltage/frequency values are dynamically adjusted considering the execution time. If these approaches reduce lost time, they require a centralized control and lead to additional calculations (sequencer call during a task, more frequent context change …) [30].

The estimation technique is based on both profiling and monitoring-enabled techniques since the workload behavior change during the execution [7]. Processor workload estimation techniques determine the profile of the required workload and anticipate their value and behavior [31]. At the infrastructure level, the DVFS adjusts the operational voltage and frequency of the server according to the current workload to reduce energy waste and untimely server consolidation patterns. The DVFS takes advantage of the resulting workload behavior by exploiting profiling information. However, the monitoring method is based on an intelligent resource allocation technique that uses both DVFS and virtual machine (VM) migration methods. It defines the appropriate operating state and prevents aggressive migration of virtual machines [32]. Since the approximation of the CPU relative value allocations are reliable and error-prone in a distributed and heterogeneous system, the DVFS allocates exactly the necessary resources without relying on the percentage metric.

In the control level, the DVFS can be implemented on both chip, controller algorithms or OS-level. The operating systems rely on APIs to communicate with the underlying hardware and issue the most appropriate command to manage power consumption [33]. In the chip

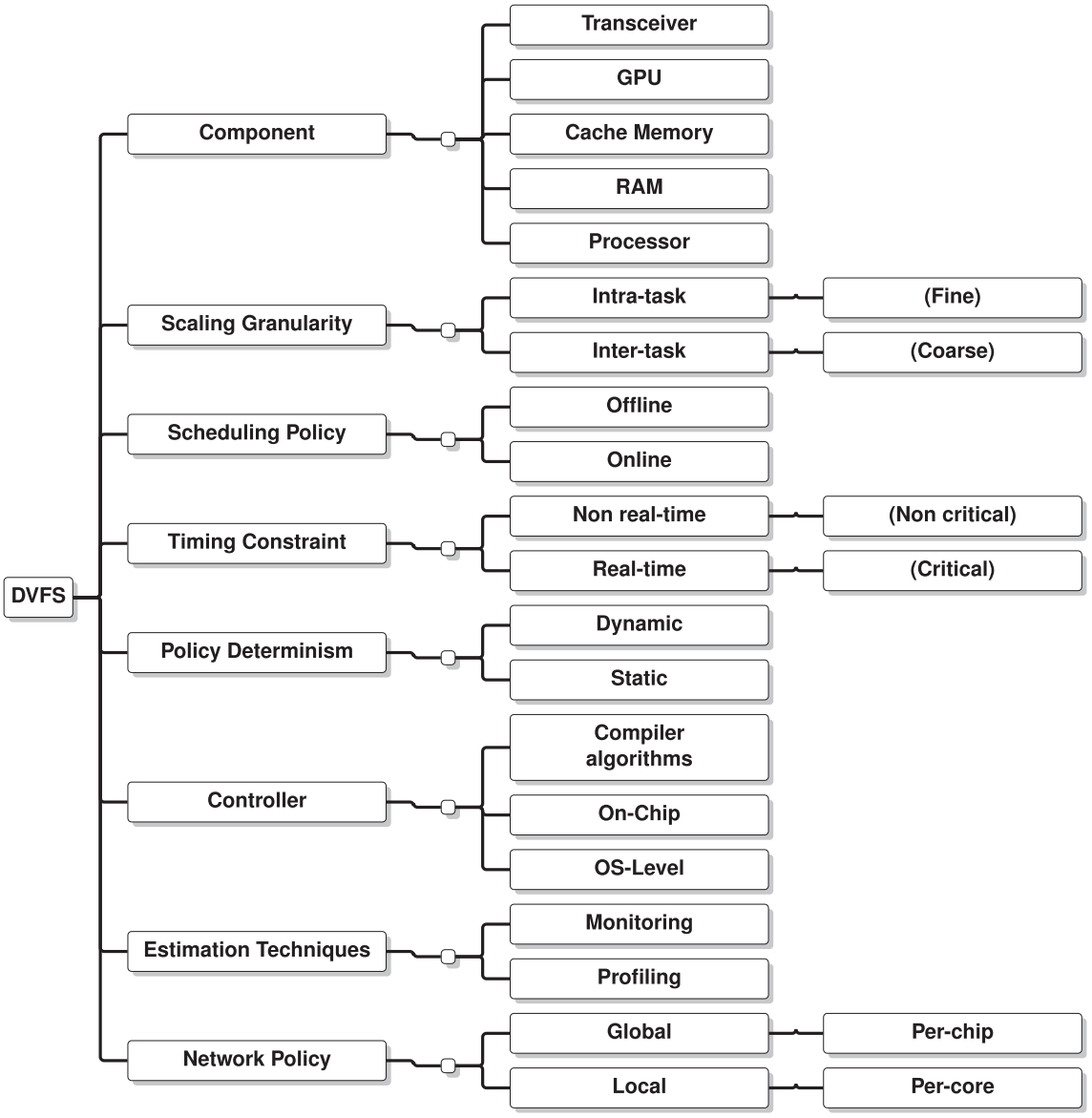

Fig. 1. DVFS taxonomy.

level-controller [25,30,34], the DVFS can be implemented on memory accesses using on-chip regulators.

DVFS has been gradually incorporated into most smart handheld devices and it has been widely adopted by laptop computers, server processor, and mobile devices to conserve energy. Moreover, DVFS is exploited for processor, GPU, RAM, radio transceiver and cache memory components [31]. The integration of GPU voltage and frequency settings on current NVIDIA boards has allowed the authors of [33] to calibrate both the GPU core voltage/frequency and memory frequency of the Fermi and Maxwell GPUs. The GPU DVFS induced a 20% gain in power consumption with a mere 4% loss in the GPU's performance. Testing a set of a real GPU platform with 37 GPU reference applications shows that the effect of the DVFS GPU is highly dependent on the characteristics of the application.

Memory power-down states during periods of inactivity between memory requests can be leveraged to further lower power consumption. Operating at well balanced speeds with peak computing power, leads to optimized memory-intensive workloads [34]. Also, the evaluation of multicore architectures and VMs has multiplied the number of RAMs, resulting in significant power consumption [35].

DVFS can also be applied in the radio transceiver unit [36]. Since the maximum energy consumed by the transceiver is in idle mode, it is preferable to avoid this state and instead keep the transceiver in a sleep mode. The transient activity state (ON/OFF) of the radio is another influencing factor that consumes a significant amount of energy.

To bridge the gap between application complexity and low hardware abstraction for WSNs, several middleware alternatives were designed. The virtualization of wireless sensor nodes has the potential to expand and unlock progress on many other fronts such as scalability, cooperation, low-power solutions, trends convergence and data analysis. This will pave the way for a paradigm shift offering more flexibility, viability and performance [37].

3. Related works to implementation of DVFS in WSNs

Currently, several variable-voltage microprocessors [26] were developed and many DVS algorithms [27,38] were proposed. Some algorithms are implemented in systems with real-time requirements [39,40].

Authors in Ref. [17] combined both hard-deadline scheduling with DVFS and energy harvesting for an heterogeneous multi-core WSN node. To enhance the real-time aspect and the varied power budget

of the proposed solution, the workload of tasks is adjusted jointly with the hardware power-mode. The workload and the quality of service are used to quantify and measure the work achieved on light-weight platforms.

DVFS decisions in Ref. [18] are made based on real-time task execution characteristics through a machine-learning method in single-core processors. A learning-based approach selects the best and most appropriate DVFS technique in real time from a set of techniques. It provides a framework with the selection of various scheduling policies and optimized real-time DVFS techniques. It is applied in multi-core processors and for synthetic tasks for real application.

[41] showed that applying DVFS on the ARM-based Commercial Off-the-shelf (COTS) microcontroller is better in terms of energy saving when compared to a DVFS exploited only for the CPU. They present their proper hardware platform to experiment both DPM and DVFS including an experimental set-up to measure the consumption of every unit of the MCU.

The authors in Ref. [25] used the DVFS technique in applications with tight deadlines. For specific application, the algorithm selects a server that runs between (F_{min}, F_{max}) and guarantees at the same time the performance of the application while ensuring that the task does not overload the resources.

Authors in Ref. [36] studied the impact on energy consumption at the radio transceiver level in tandem with the variation of hardware parameters such as clock voltage, frequency, data rate, communication time, frequency band and modulation scheme in WSNs [42]. proposed a power model using body bias control in order to improve the energy efficiency. The model is based on real-chip measurements of leakage current, switching current, and maximum operational frequency. It offers a DVFS energy optimization method that determines the optimal combination of supply and body bias voltages from on an approximated power model for a given frequency. Authors in Ref. [43] defined a Dynamic Frequency Controlling (DFC) strategy. It connects an external circuit to the PIC16F877A MCU to estimate the power. They propose a generic approach allowing the change of frequency through a clock generator based on the throughput information of the MCU. The power consumption was measured with a shunt resistor.

Authors in Ref. [44], set up a COTS-DVFS dedicated to a body area application implemented on a MSP430 to increase processing energy efficiency when timing and computational requirements are relaxed. They tested the behavior of the circuit under dynamic voltage shifting conditions on both transient and steady state. However, the authors do not consider the leakage current of the voltage converter.

In [45], an accurate macromodel is presented, which takes into account the energy and delay for DVFS transitions of the DC-DC modern converter based on datasheet component values. They divide this overhead delay into phase-locked loop (PLL) induced and underlocking-related delay. The same applies to the energy overhead which is the sum of the energy induced by the converter and by the CPU.

When investigating the current status of DVFS in the WSN, we come across different techniques that are used to backbone DVFS. For better energy saving, Table 1 summarizes the main features of the DVFS techniques. The use of processors decreases online as well as energy consumption because it is possible to activate low-power states for longer periods of time. The scheduling algorithm must then use this slack time online to reduce the energy consumption by increasing the size of idle periods. The inactivity/idle intervals of the WSNs are mainly due to sensor sampling time varying according to the process requirements and the WCET of the application. These decisions can only be made online because the actual execution time of each job (i.e. AET) cannot be known before execution. Real-time tasks rarely use all of their WCETs at runtime [20]. Thus, while guaranteeing the deadlines for all tasks at high criticality, it is possible to be aggressive on low critical tasks by proposing a scheduling where tasks will only use a portion of their WCET.

Memory management often draws a power disproportionate to its load, which hinders its scalability [16,35]. Thus, significant challenges remain unresolved. The usual methods of controlling the memory's power creates memory idleness through scheduling, batching and layout transformations [34]. Server consolidation in virtualized datacenter environment leveraged DVS technique to optimize energy consumption [32]. However, the aggressive migration of virtual machines and server consolidation executions are not optimal in terms of power consumption and node performance. Previous efforts and many widely used COTS processors do not have DVFS or apply DVFS only to processor cores [45]. In the case of data flow oriented applications, offline power management techniques are generally considered in the literature [2,5,35].

4. Proposed DVFS approach

The DVFS power saving technique is applied in order to stretch the processing time of the tasks and reduce the energy consumption by decreasing the CPU frequencies of the active power states. DVFS is used in high-computing nodes not only to decrease the power of the nodes but also to save more energy and to cool down the nodes. The decision for a particular voltage or frequency is based on several factors, including the application latency and the task arrival rate. Ideally, these two parameters are adjusted so that a task is completed "just in time". This dynamic adaptation is made by setting the values of the couple of (voltage/frequency) known as Operating Performance Points (OPPs). The values are determined in part by the processor's hardware architecture and in part by its functional behavior. Under these conditions, the DVFS controller affects the dynamic power consumption as well as the static power while meeting the requirements of the application. A mixed approach using DPM and DVFS is considered in Ref. [46]. All these techniques attempt to adapt traditional single or multiprocessor scheduling techniques to incorporate the criterion of minimizing power consumption. Synchronizing the dynamic change of DVFS states will have an impact on system stability. The impact of these DVFS transition overheads is variable and depends on how often we change the DVFS parameters. We will use the inter-task, local, mixed-criticity, dynamic method where the processor speed and voltage are selected before the task is reactivated. To yield high efficient-energy, the proposed DVFS is applied for the whole microcontroller including the CPU, PLL, memory, and input/output. The approach is portable and can be applied to other types of systems.

4.1. Normalized power

The power consumed during active mode are often identified and characterized as multiplication of supply voltage and average current of the microcontroller's active mode. This argument is correct when the microcontroller operates in active mode for indefinite time. This can be inaccurate, however, when a microcontroller operates in a duty cycle. Instead, total active power during a duty cycle is decidedly affected by performance of the microcontrollers [14]. It is more important to calculate the normalized power that is defined as a measure of power per throughput (mW/MIPS). It is critical to understand that the lower normalized power, the lower energy that microcontroller will consume.

4.2. Software implementation and validation

MSP430F5529 micro-controller is used in this paper [48]. A benchmarking study compared several platforms (PIC, STM32, MSP, etc) according to their architecture, their datasheet, and by real measurements in different power-modes. The MSP430 proved to be the most optimal in terms of energy consumption [49]. The measurement instrument used is a Keysight Technologies E5270 8-channel Pre-

Table 1
Comparison of existing DVFS strategies in WSN.

		[25]	[32]	[33]	[34]	[35]	[36]	[38]	[46]	[47]
Method		Scheduling	VM [a]		Control Algorithm	CREW [b] UD [c]		Machine learning	HEEPS [d]	AVS [e]
Application		Data-Center		CUDA Rodinia	Data-Center	Cloud Computing	Modulation Scheme		WSN	RT [f]
Components	CPU	x				x		x	x	x
	GPU			x		x				
	RAM			x	X					
	Radio						x			
Network Policy	Local	x		x		x	x		x	x
	Global									
Estimation Techniques	Profiling			No	No	x	No		No	x
	Monitoring	x	x	No	No		No		No	
Controller	OS-level		x			–			x	
	OnChip	x		x	x	–	x			
	Compiler					–				x
	Algorithms									
Policy Determinism	Static			x	x		x			
	Dynamic	x				x			x	x
Timing Constraint	Hard	x				x		x	x	x
	Not real time			x	x		x			
Scheduling Policy	Online			No			No	x	x	
	Offline	x		No	x	x	No			x
Scaling Granularity	Inter-task			x	x	–	–		x	
	Intra-task	x				–	–			x

[a] Virtual Machine.
[b] CPU and RAM Energy-aWare.
[c] Underload Detection.
[d] Hybrid Energy-Efficient Power Management for Wireless Sensor Networks.
[e] Automatic Voltage Scaler.
[f] Real-Time applications.

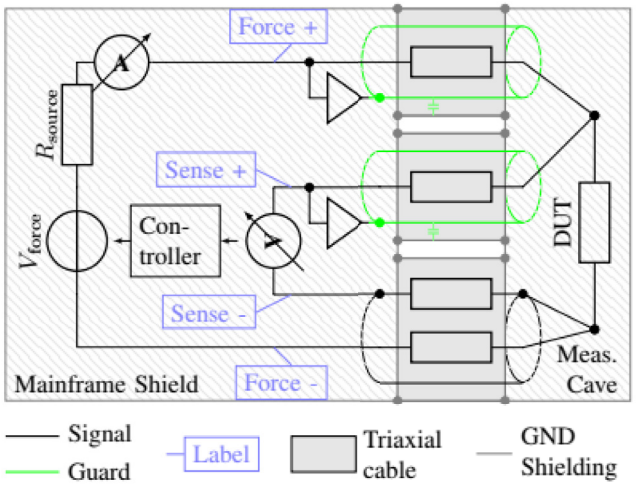

Fig. 2. Four-wire measurement setup involving a Keysight Technologies E5270 8-channel precision measurement mainframe guarding and shielding using SMU.

cision Measurement Mainframe [50] that supports a high-resolution Source/Measure Unit (SMU). The SMU applies a voltage to the force connection and measures it over the Device Under Test (DUT) with a sense interface. The controller automatically adjusts the supply voltage to match the voltage drop that is caused by the parasitic resistances of the force wires. The current profile is measured using the integrated amperemeter in series with the force connection. The thereby introduced voltage drop is eliminated by the feedback-controlled 4 wire-setup. The measurement device supports averaging of samples to reduce noise influences. The maximum sampling frequency is limited by around 300 Hz. To support different microcontrollers and make the measurements comparable to future measurements, a supply voltage of $\simeq$ 3.3 V, which most MCUs can support, is chosen for all measurements with constant supply voltage.

The measurement setup consists of the system under test setup, interfaced with an E5270B Precision IV Analyzer from Keysight technologies for power supply and sensing purposes as shown in Fig. 2. A mainframe computer controls of the supply voltage provided by the E5270B device to the system under test and collates the measured data for further analysis. The measurement interface is implemented as a LabVIEW virtual instrument.

5. Performance evaluation

To evaluate the impact of DVFS on the microcontroller's energy consumption, a control variance method is applied. Indeed, we set one of the variables whether it is frequency or voltage while measuring the normalized power, the virtual resistance, etc. and varying the other metric.

5.1. Simulation setup

To test the DVFS in MSP430, and because the frequency is limited by the supply voltage, the test was performed backwards from 18 MHz to 2 MHz with a 1 MHz step between frequencies. The presented results were obtained with the application, with static maximum supply voltage versus dynamic voltage. The opportunity for an accurate CPU-DVFS power model is presented under voltage, frequency, resistance and current scaling. We evaluate this model through real-hardware and on application performance in the next section.

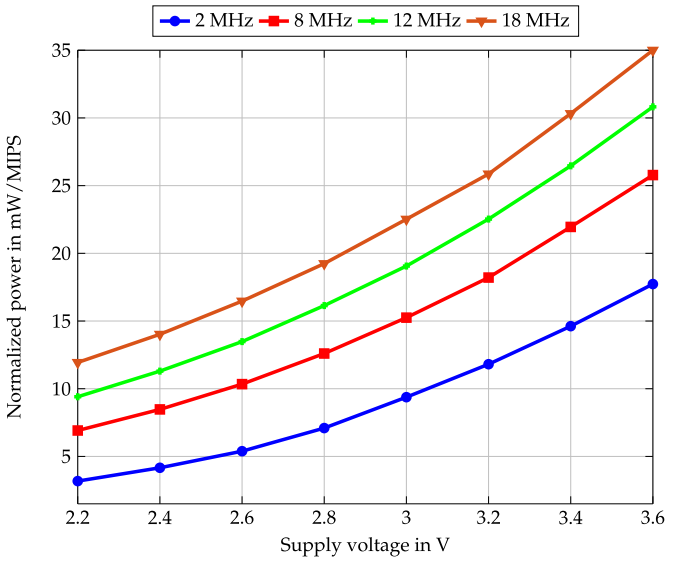

Fig. 3. Normalized power versus the supply voltage and frequency of the main clock using NOP instruction.

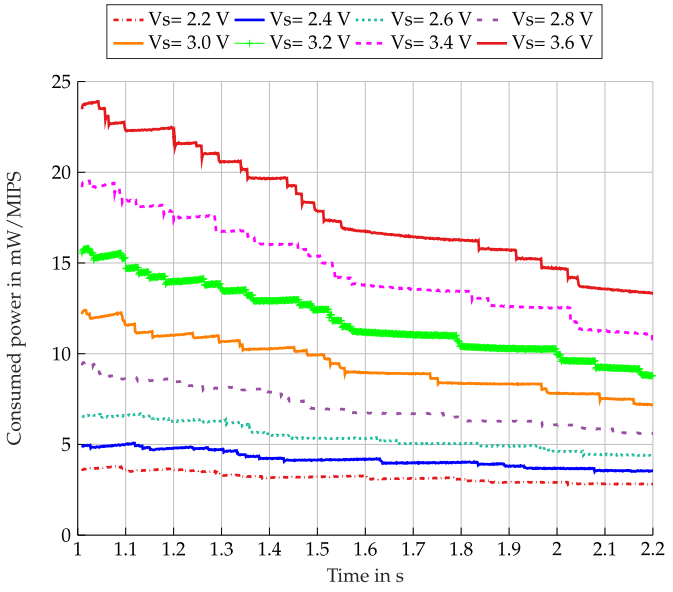

Fig. 4. Consumed power during time for different supply voltages at 2 MHz.

5.2. Simulation results

We performed DVFS measurement experiments on MSP430F529 platforms. Our experimental results can serve as DVFS CPU benchmarks and reveal the experimental results of DVFS effects on CPU energy consumption. As an example, we consider the frequency 18 MHz, when the voltage is fixed, we notice that when the voltage is gradually increased from 2.2 V to 3.6 V, the normalized power goes from 12 MIPS/W to 35 MIPS/W resulting in an increase of 57% as shown in Fig. 3.CPU normalized power is 35 mW/MIPS in the highest case (18 MHz, 3.6 V), and 22 mW/MIPS on average. We set the frequency at 2 MHz and vary the voltage as shown in Fig. 4. This experiment confirms that the highest voltage 3.6 V initially corresponds to the highest normalized power of 24 mW/MIPS although this value decreases over time. The variation

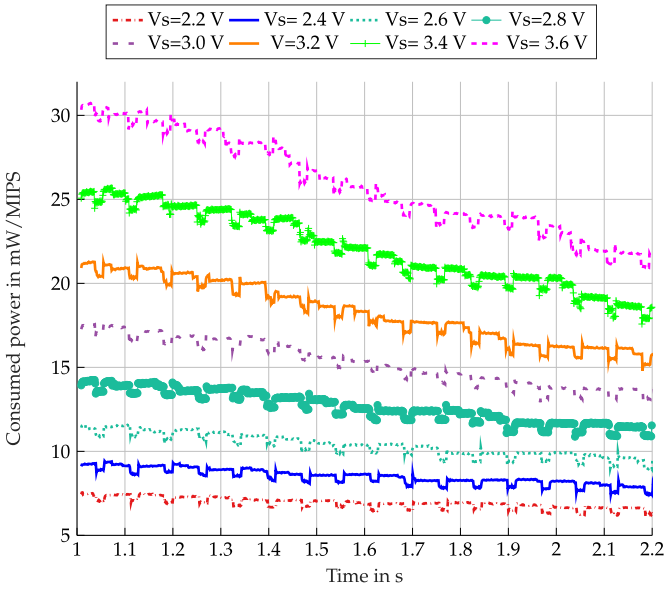

Fig. 5. Consumed power during time for different supply voltages at 8 MHz.

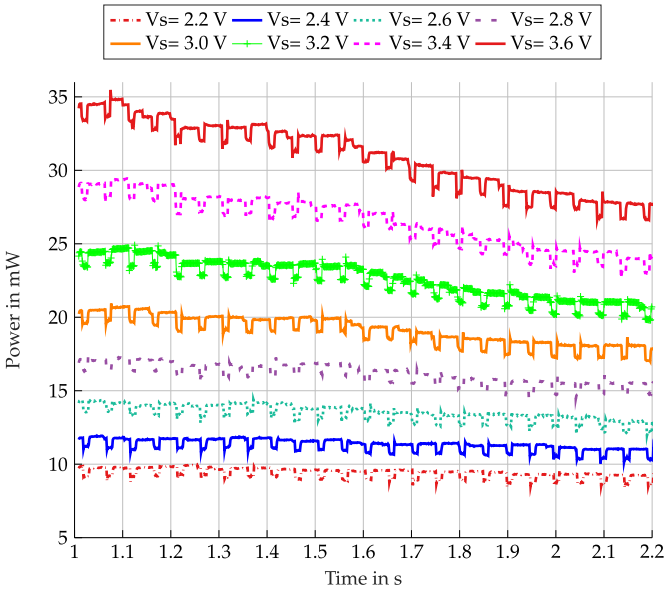

Fig. 6. Consumed power during time for different supply voltages at 12 MHz.

over time of the normalized power for V = 2.2 V remains approximately constant. Total average system power for each run is shown for comparison as demonstrated in the following Figs. 4–7. For the voltage V = 3.6 V, the power consumption increases by 37% when we go from 2 MHz to 18 Mhz.

Using high processor frequencies as demonstrated in Fig. 7 decreased the total energy since it enables shorter execution time (AET). Therefore, reducing the core voltage of the CPU is an efficient way to minimize the energy consumption in the idle power-mode and in the active power-mode when working at an appropriate core frequency.

Indeed, reducing the voltage slows down most of the applications, which results in an excess of energy consumption. The optimal setting of OPP depends on the application characteristics if real-time requirements are hard or with mixed criticicity. Since the best level of energy efficiency can be achieved via (F_{min}, V_{min}), these low-power operating points heavily affect the performance that is degraded resulting in an increase in execution time that induces an increase in energy itself

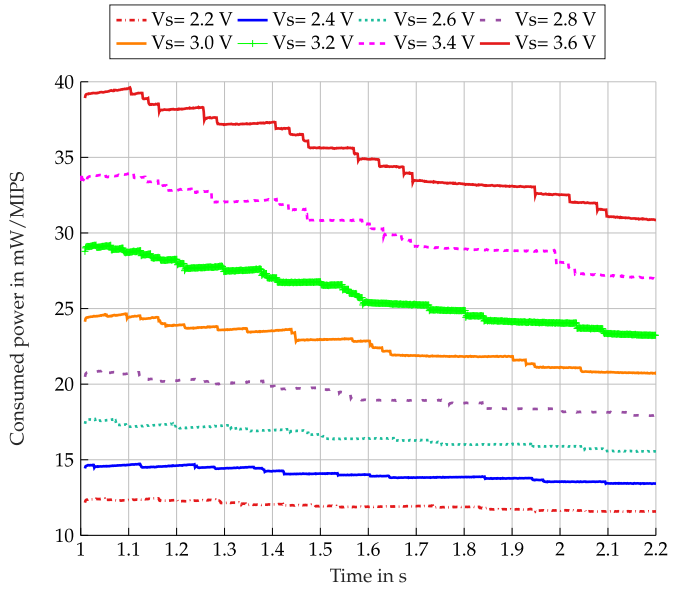

Fig. 7. Consumed power during time for different supply voltages at 18 MHz.

(Fig. 3. Therefore, it is wise to find a balance and a compromise between these 2 constraints.

Finally, our results demonstrate that system energy consumption is reduced significantly, compared to prior approaches, while respecting the user-specified performance constraints.

6. Conclusion

Dynamic voltage and frequency scaling (DVFS) has been widely used in many mobiles and embedded devices mainly for time-constrained applications to save energy consumption. We take into account the slack time when the tasks finish before their deadlines to ensure a maximum use of the processor. This paper summarizes the most important DVFS studies, the performance and power modeling techniques in WSN. The impact of DVFS on the performance or power consumption, especially for microcontrollers is also evaluated while introducing an advanced energy metric which is the normalized power.

The computational results show that DVFS reduces significantly the total energy consumption. A high voltage/frequency can leads up to 57% increase of the normalized-power when, the power consumption increases by 37% when we increased the frequency. As future works, we are intending in considering the impact of the DVFS timescale and scaling overhead on overall energy efficiency.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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