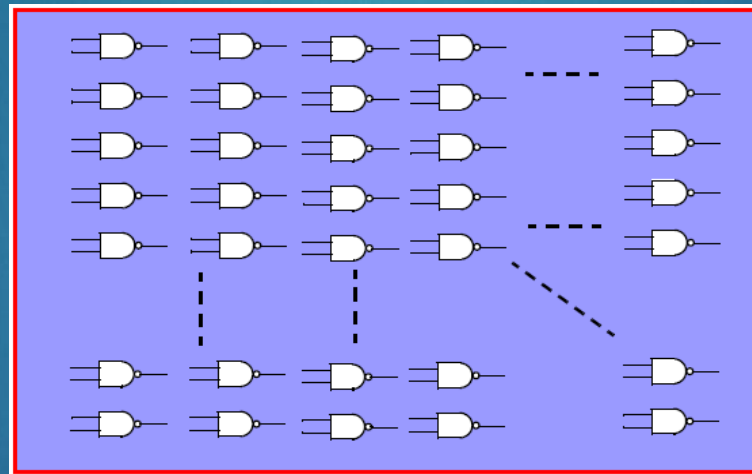


Introduction to FPGAs

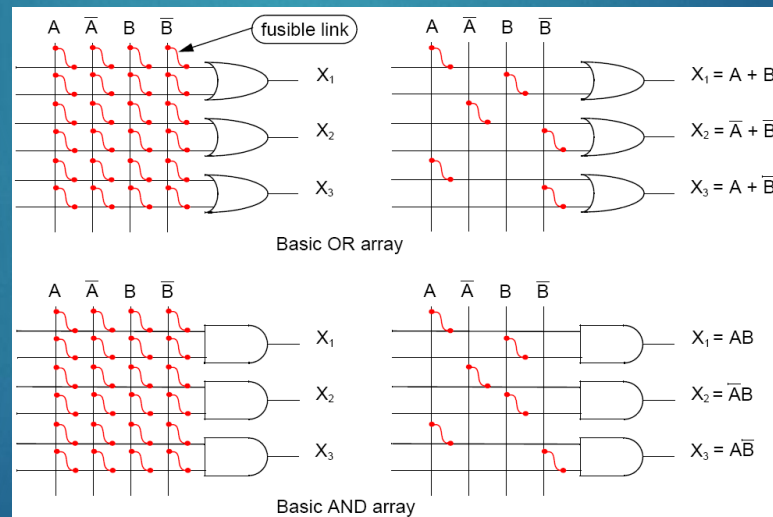
Historical Introduction

- ▶ In the beginning, digital design was done with the '74 series of chips.
- ▶ Some people would design their own chips based on Gate Arrays, which were nothing else than an array of NAND gates:



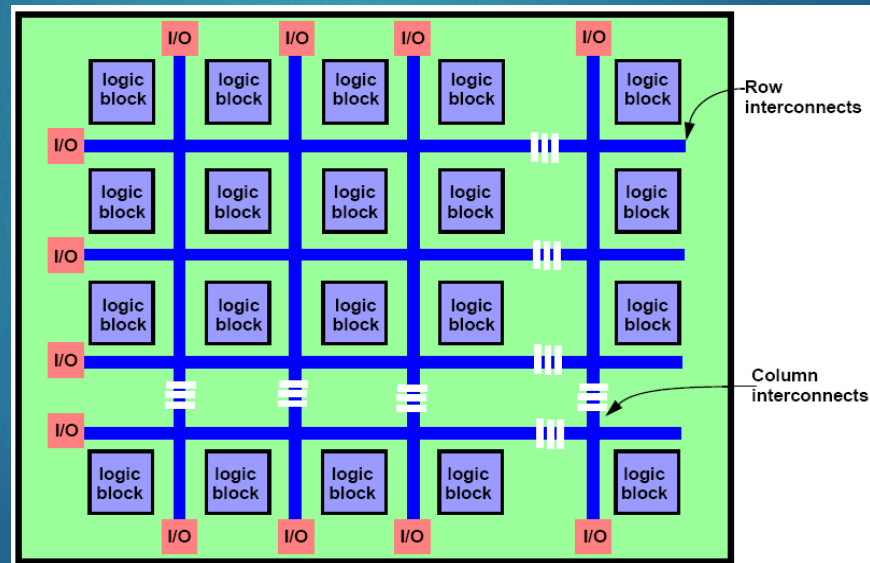
Historical Introduction

- ▶ The first programmable chips were PLAs (Programmable Logic Arrays): two level structures of AND and OR gates with user programmable connections.
- ▶ Programmable Array Logic devices were an improvement in structure and cost over PLAs. Today such devices are generically called Programmable Logic Devices (PLDs).



Historical introduction

- ▶ A complex PLD (CPLD) is nothing else than a collection of multiple PLDs and an interconnection structure.
- ▶ Compared to a CPLD, a Field Programmable Gate Array (FPGA) contains a much larger number of smaller individual blocks + large interconnection structure that dominates the entire chip.



Programmable logic

- ▶ An integrated circuit that can be programmed/reprogrammed with a digital logic of a certain level.
- ▶ Started at late 70s and constantly growing
- ▶ Now available of up to approximately 700K Flip-Flops in a single chip.

What are FPGAs

Field-Programmable Gate Array

Keywords

Field-Programmable-
Programmable on Site

Gate Arrays- Array like structure



What are the advantages?

- ❖ **Can be configured to act like any circuit**
 - Rapid Prototyping
- ❖ **Reconfigurable**
 - Can be programmed many times
- ❖ **Saves Product to Market Time**
 - Short Development time
 - Flexible to changes
 - No need for ASIC expensive design and production
 - Fast time to market
 - Of the shelf solutions are available



FPGAs Come In Many Forms



PCIe-Attached



CPU Integrated



In-Network

Image Source: <https://itpeernetwork.intel.com/intel-processors-fpga-better-together/>
<https://www.compsource.com/buy/AU50P00GPQG/Xilinx-6217>



In-Storage

Manufacturers

- ▶ Xilinx
- ▶ Altera
- ▶ Lattice
- ▶ Actel



XILINX FPGAs

45nm	28nm	20nm	16nm
SPARTAN ⁶	VIRTEX ⁷	VIRTEX ⁷ UltraSCALE	VIRTEX ⁷ UltraSCALE+
	KINTEX ⁷	KINTEX ⁷ UltraSCALE	KINTEX ⁷ UltraSCALE+
	ARTIX ⁷		ARTIX ⁷ UltraSCALE+
	SPARTAN ⁷		

<https://www.xilinx.com/products/silicon-devices/fpga.html>

Xilinx FPGAs

Zynq-7000 SoC



Zynq UltraScale+ MPSoC



Zynq UltraScale+ RFSoc



Versal ACAP

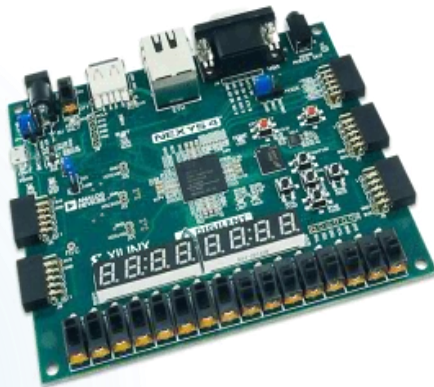


<https://www.xilinx.com/products/silicon-devices/soc.html>

FPGAs in Lab



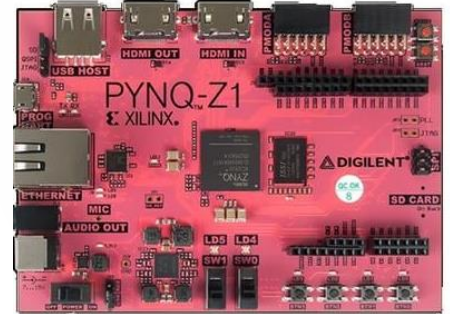
Zynq Ultrascale



Artix 7



Zynq/Xilinx Zynq-7000



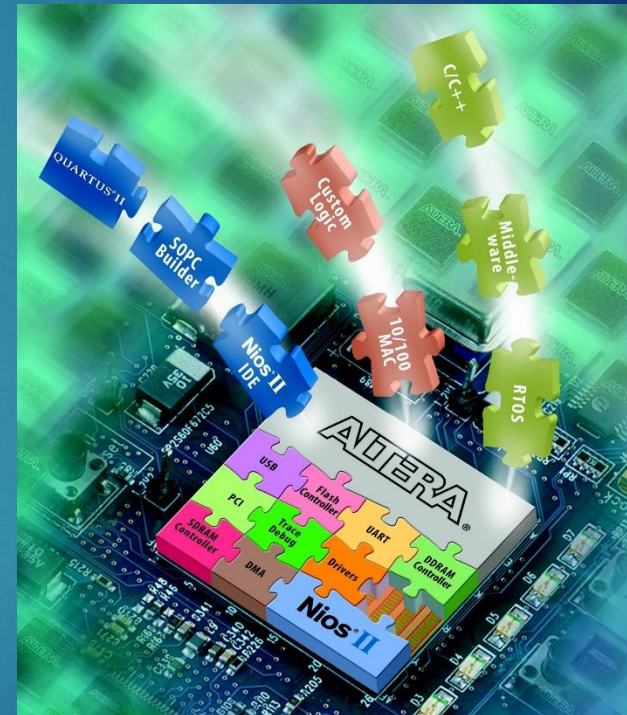
Zynq

Common FPGA Applications

- ▶ High Performance Computing
- ▶ Medical Equipment
- ▶ Data Servers
- ▶ Consumer Electronics
- ▶ Computer Networking
- ▶ Aerospace and Defense
- ▶ Etc.

Special FPGA functions

- ▶ Internal SRAM
- ▶ Embedded Multipliers and DSP blocks
- ▶ Embedded logic analyzer
- ▶ Embedded CPUs
- ▶ High speed I/O (~10GHz)
- ▶ DDR/DDRII/DDRIII SDRAM interfaces



How Is It Different From ASICs

- ▶ ASIC (Application-Specific Integrated Circuit)
 - ▶ Special chip purpose-built for an application
 - ▶ E.g., ASIC bitcoin miner, Intel neural network accelerator
 - ▶ Function cannot be changed once expensively built
- ▶ + FPGAs can be **field-programmed**
 - ▶ Function can be changed completely whenever
 - ▶ FPGA fabric **emulates** custom circuits
- ▶ - Emulated circuits are not as efficient as bare-metal
 - ▶ ~10x performance (larger circuits, faster clock)
 - ▶ ~10x power efficiency



FPGA vs ICs

Single FPGA may replace several ICs

No wire-wrapping

Less power consumption, faster speed

Increased Reliability

FPGA vs ASIC

FPGAs are
programmable
on site

ASICs have
considerable
design cost
and time

ASICs have to
be fabricated,
mistakes are
costly

FPGA - Field Programmable Gate Array

● Programmable logic blocks (Logic Element “LE”)

Implement combinational and sequential logic. Based on LUT and DFF.

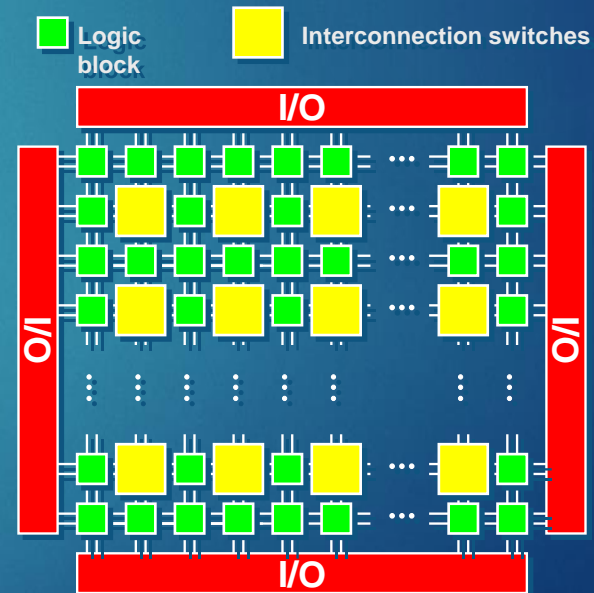
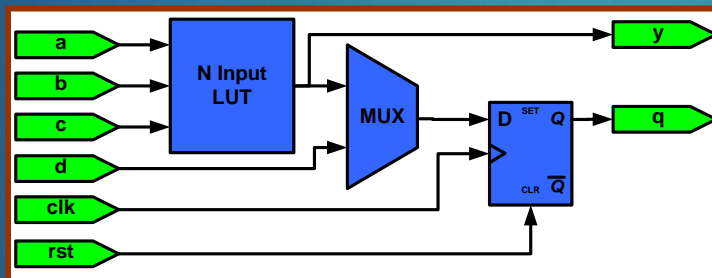
● Programmable I/O blocks

Configurable I/Os for external connections supports various voltages and tri-states.

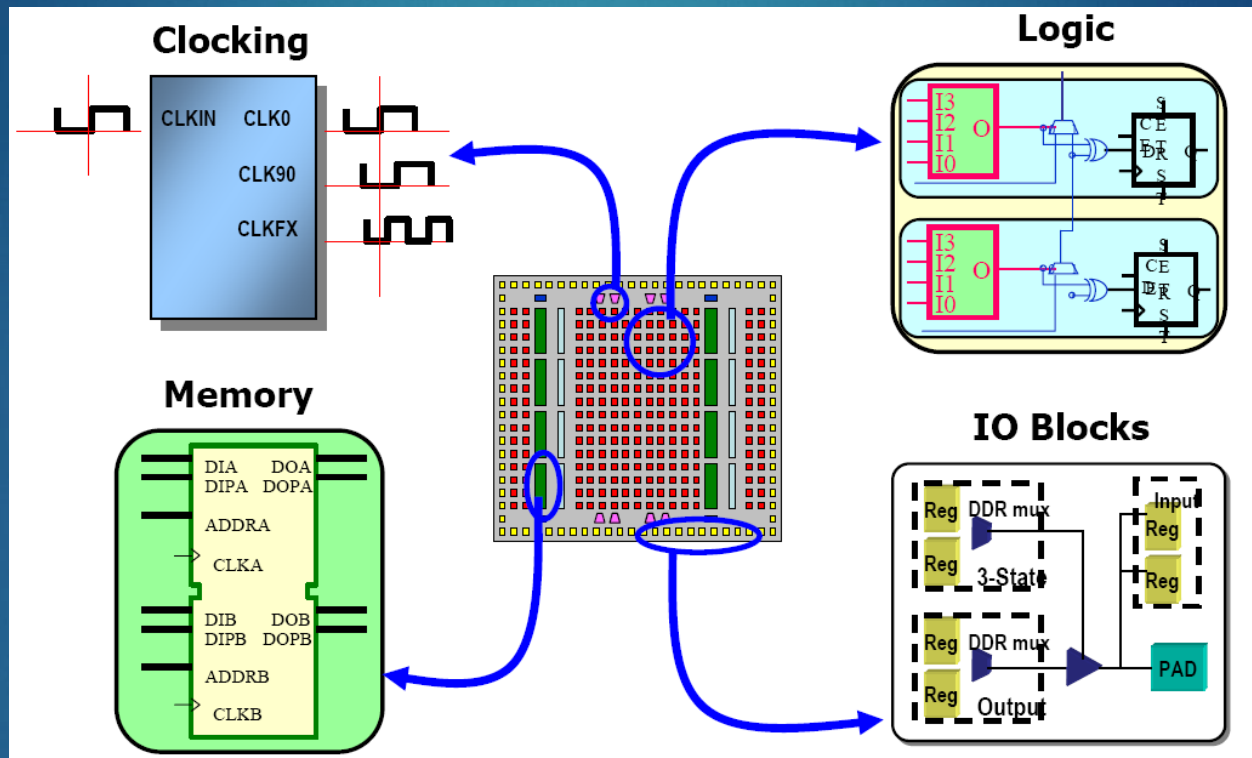
● Programmable interconnect

Wires to connect inputs, outputs and logic blocks.

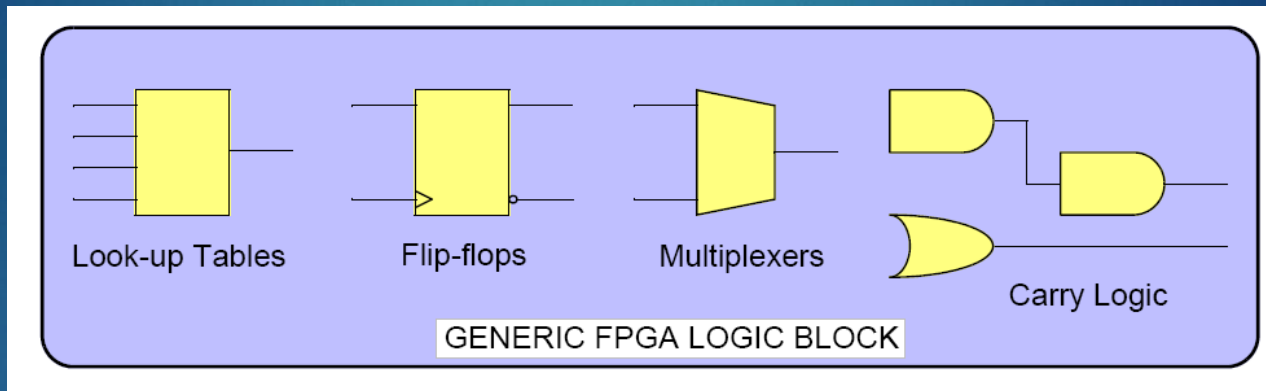
- clocks
- short distance local connections
- long distance connections across chip



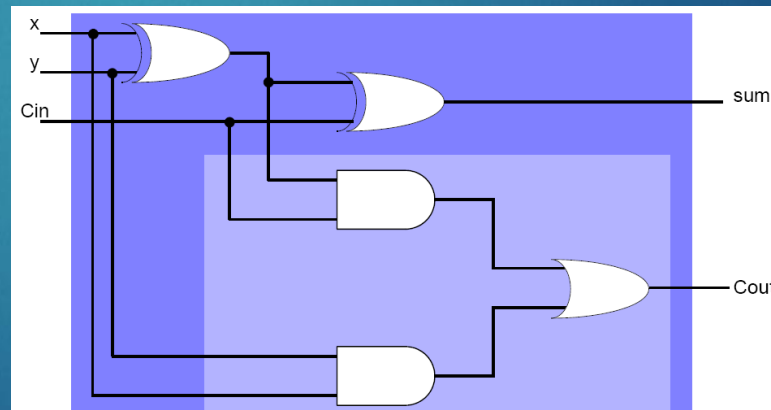
Basic FPGA architecture



The logic block: a summary view



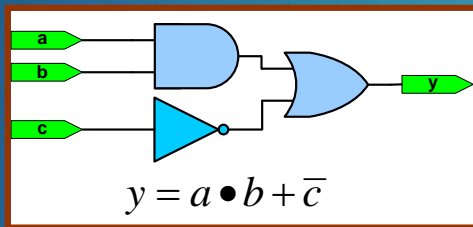
Example: using a LUT as a full adder.



Configuring LUT

- LUT is a RAM with data width of 1bit.
- The contents are programmed at power up

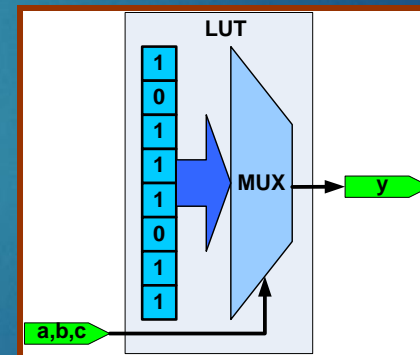
Required Function



Truth Table

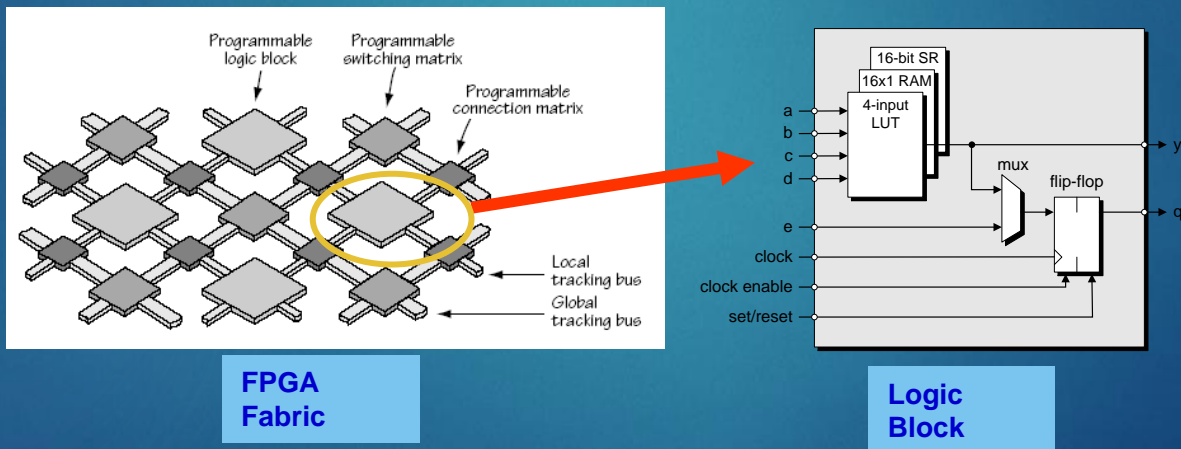
a	b	c	y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Programmed LUT



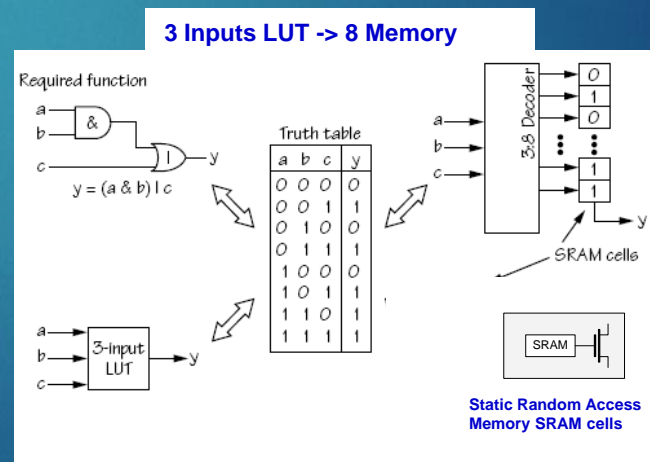
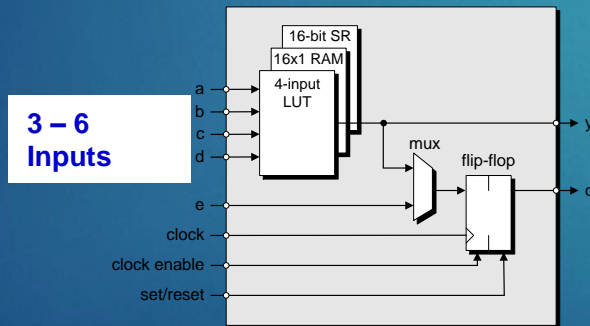
Logic Blocks

- ▶ Logic Functions implemented in Look Up Table **LUTs**.
- ▶ Flip-Flops. **Registers**. Clocked Storage elements.
- ▶ Multiplexers (select 1 of N inputs)



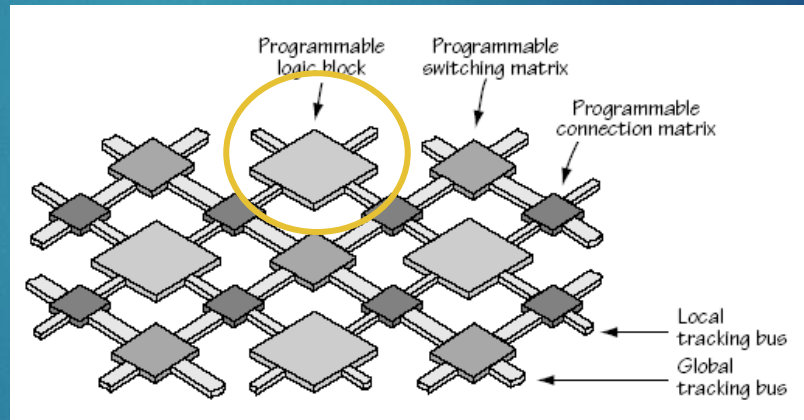
Look Up Tables LUTs

- ▶ LUT contains Memory Cells to implement small logic functions
- ▶ Each cell holds '0' or '1' .
- ▶ Programmed with outputs of Truth Table
- ▶ Inputs select content of one of the cells as output
- ▶ Configured by re-programmable **SRAM** memory cells



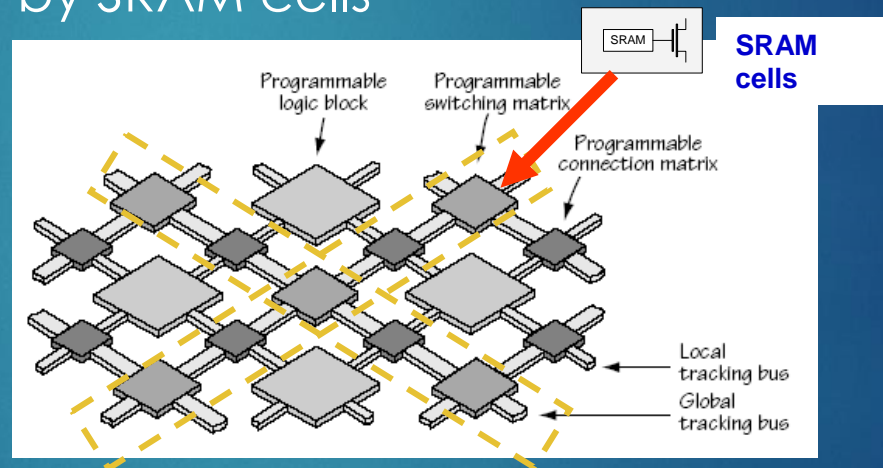
Logic Blocks

- Larger Logic Functions built up by connecting many Logic Blocks together

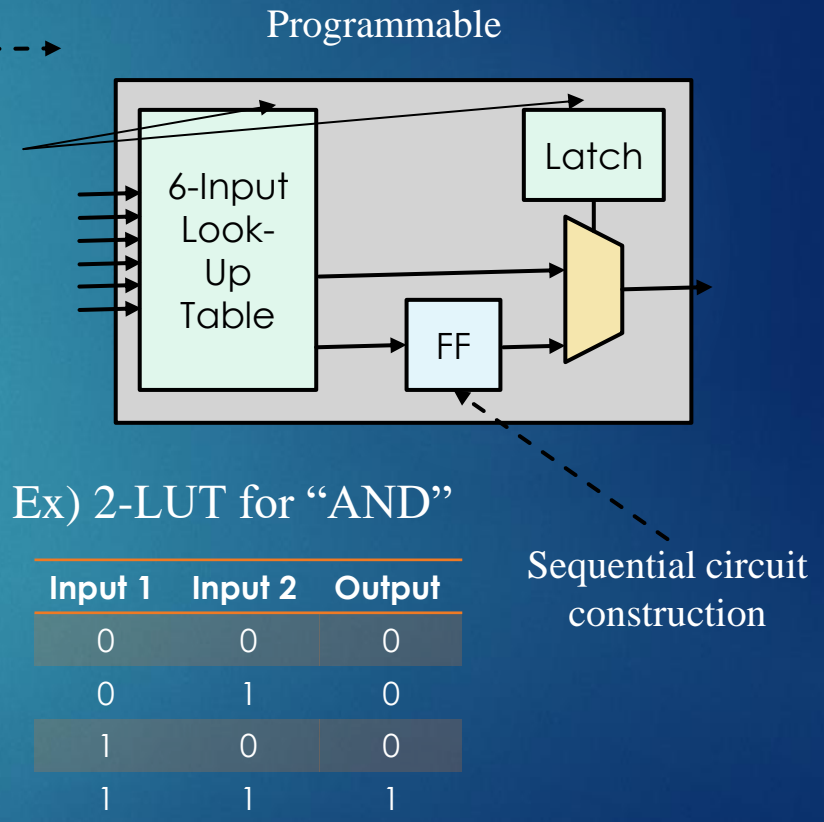
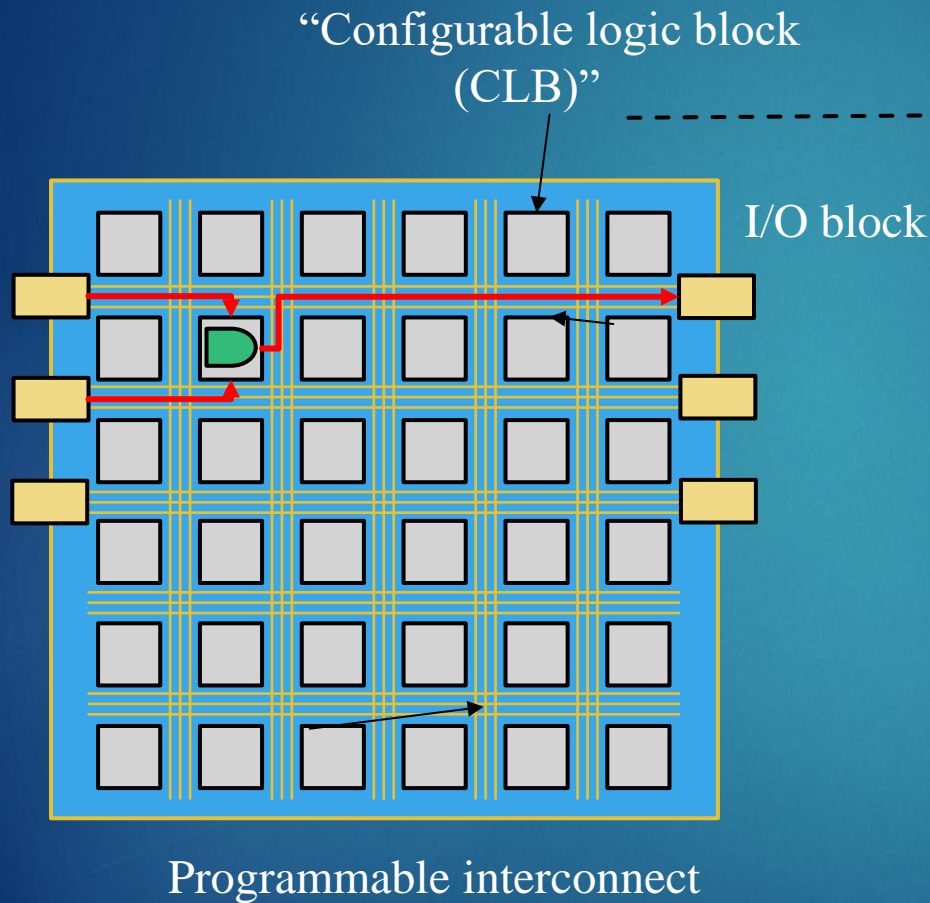


Logic Blocks

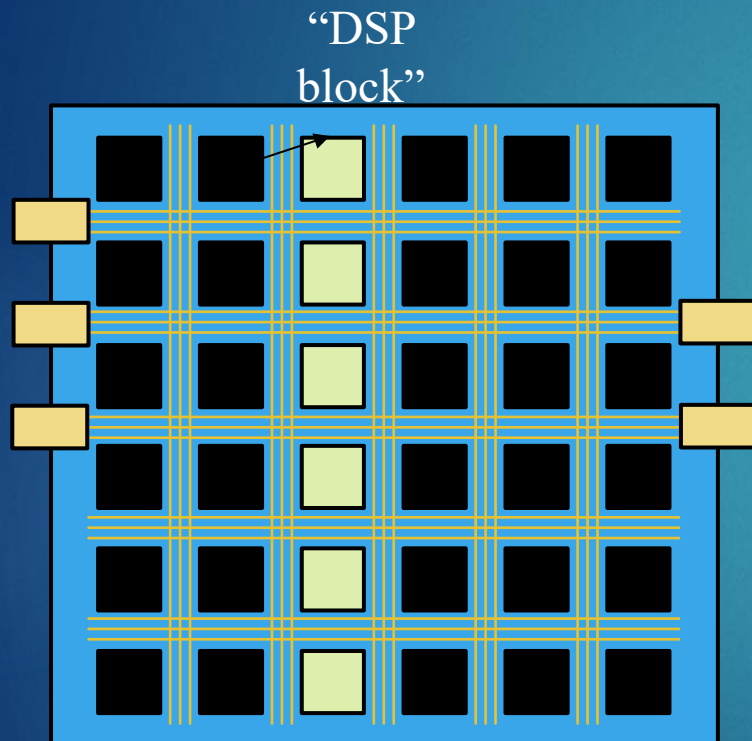
- ▶ Larger Logic Functions built up by connecting many Logic Blocks together
- ▶ Determined by SRAM cells



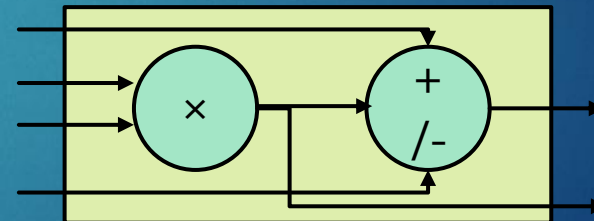
Basic FPGA Architecture



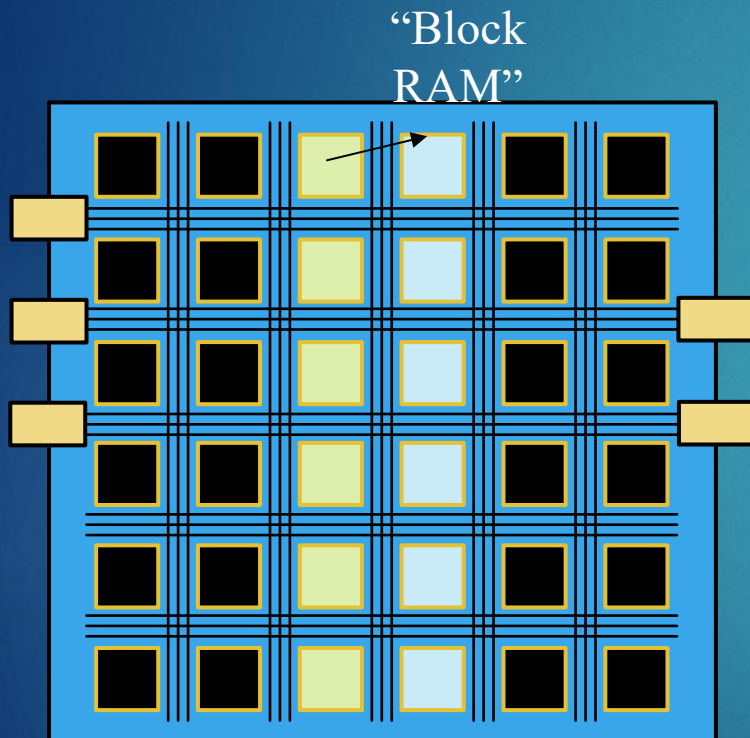
Basic FPGA Architecture – DSP Blocks



- ▶ CLBs act as gates – Many needed to implement high-level logic
- ▶ Arithmetic operation provided as efficient ALU blocks
 - ▶ “Digital Signal Processing (DSP) blocks”
 - ▶ Each block provides an adder + multiplier



Basic FPGA Architecture – Block RAM

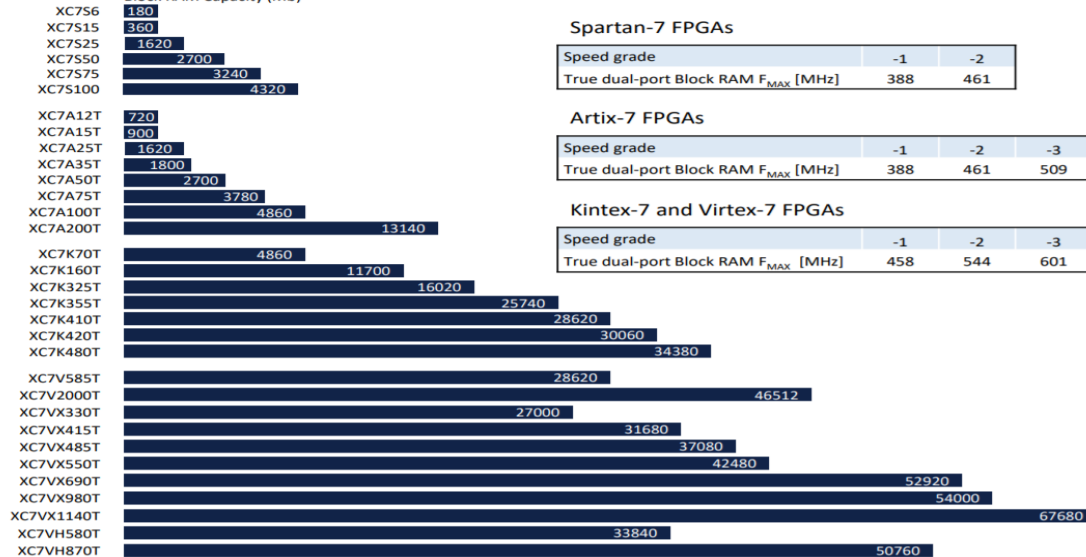


- ▶ CLB can act as flip-flops
 - ▶ (~1 bit/block) – tiny!
- ▶ Some on-chip SRAM provided as blocks
 - ▶ ~18/36 Kbit/block, MBs per chip
 - ▶ Massively parallel access to data → multi-TB/s bandwidth

Block RAM Capacity in different Xilinx FPGAs

Block RAM Metrics

Block RAM Capacity (Mb)



Spartan-7 FPGAs

Speed grade	-1	-2
True dual-port Block RAM F _{MAX} [MHz]	388	461

Artix-7 FPGAs

Speed grade	-1	-2	-3
True dual-port Block RAM F _{MAX} [MHz]	388	461	509

Kintex-7 and Virtex-7 FPGAs

Speed grade	-1	-2	-3
True dual-port Block RAM F _{MAX} [MHz]	458	544	601

<https://www.xilinx.com/content/dam/xilinx/support/documentation/selection-guides/7-series-product-selection-guide.pdf>