Chapter 7: Microarchitecture

# Single-Cycle Control

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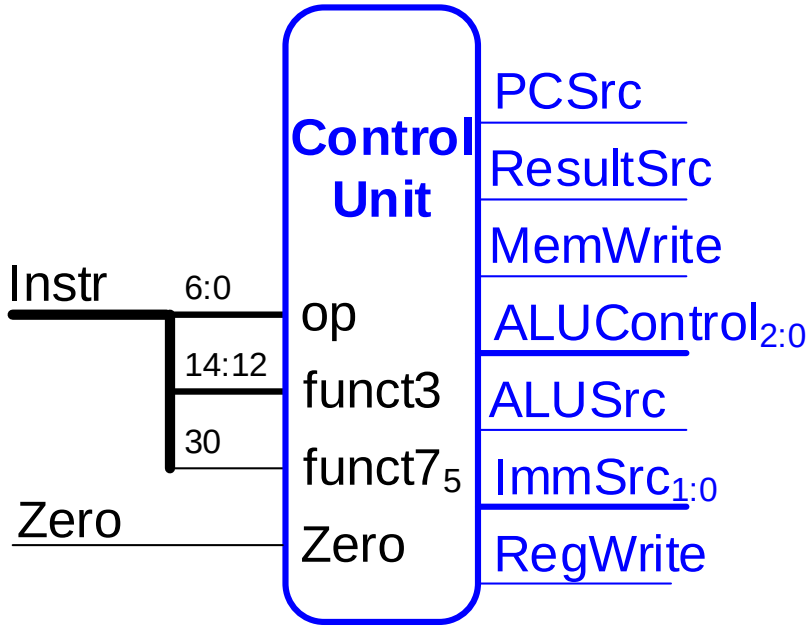
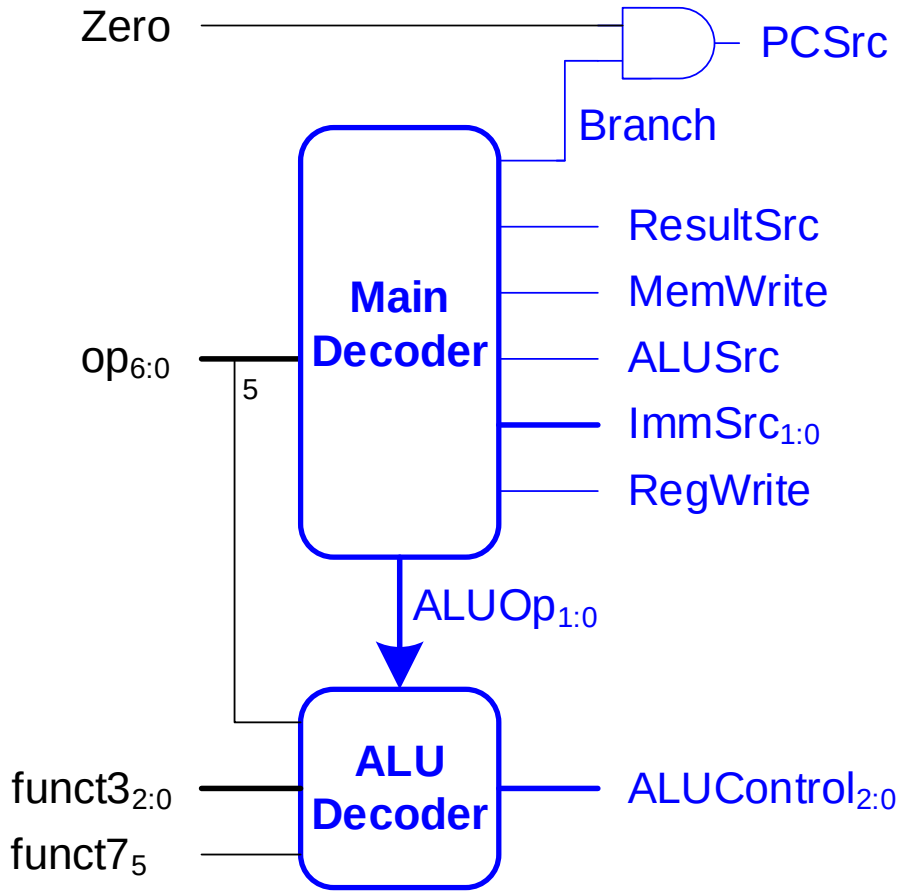
## High-Level View

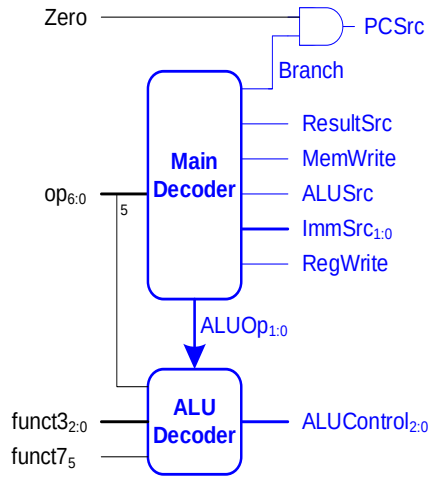



## Low-Level View



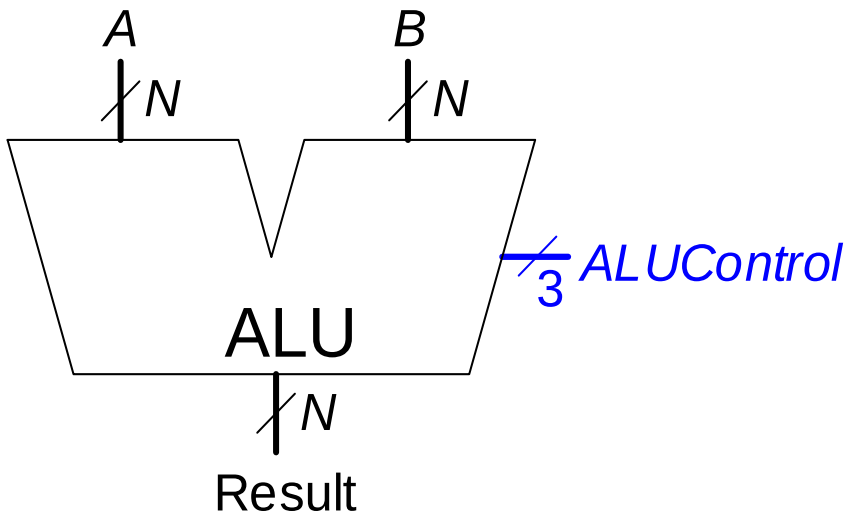
# Single-Cycle Control: Main Decoder

| op | Instr. | RegWrite | ImmSrc | ALUSrc | MemWrite | ResultSrc | Branch | ALUOp |
|---|---|---|---|---|---|---|---|---|
| 3 | `lw` | | | | | | | |
| 35 | `sw` | | | | | | | |
| 51 | R-type | | | | | | | |
| 99 | `beq` | | | | | | | |



# Review: ALU

| $ALUControl_{2:0}$ | Function |
|---|---|
| 000 | add |
| 001 | subtract |
| 010 | and |
| 011 | or |
| 101 | SLT |



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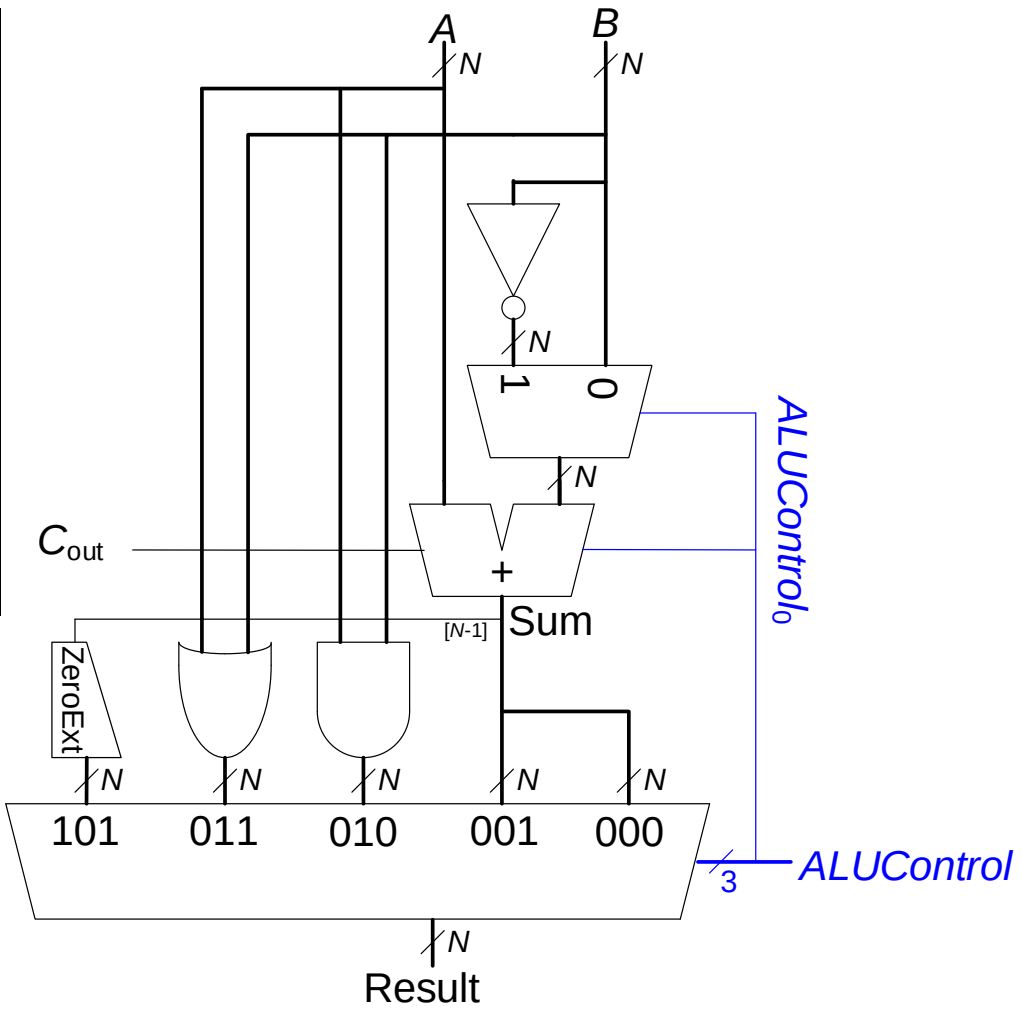
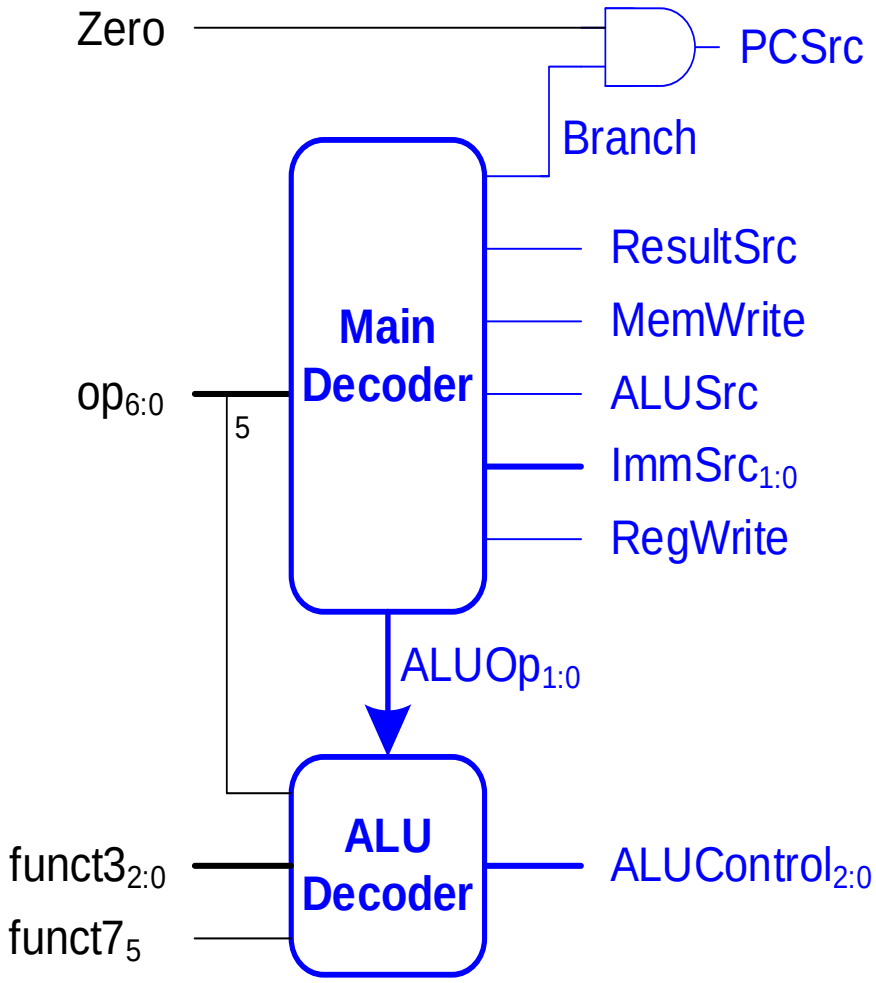
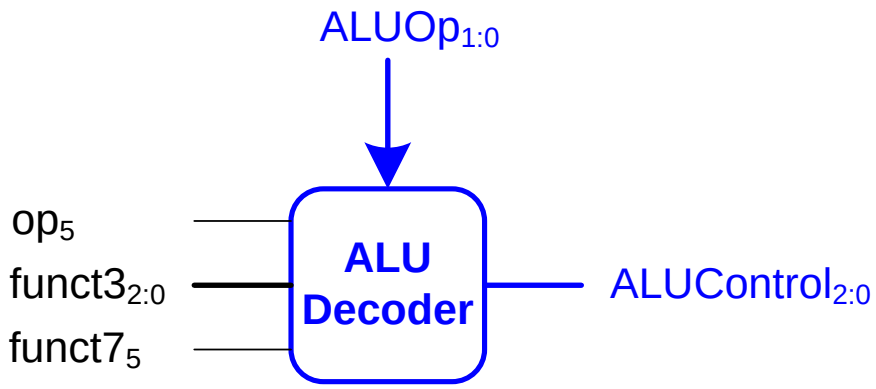


# Single-Cycle Control: ALU Decoder



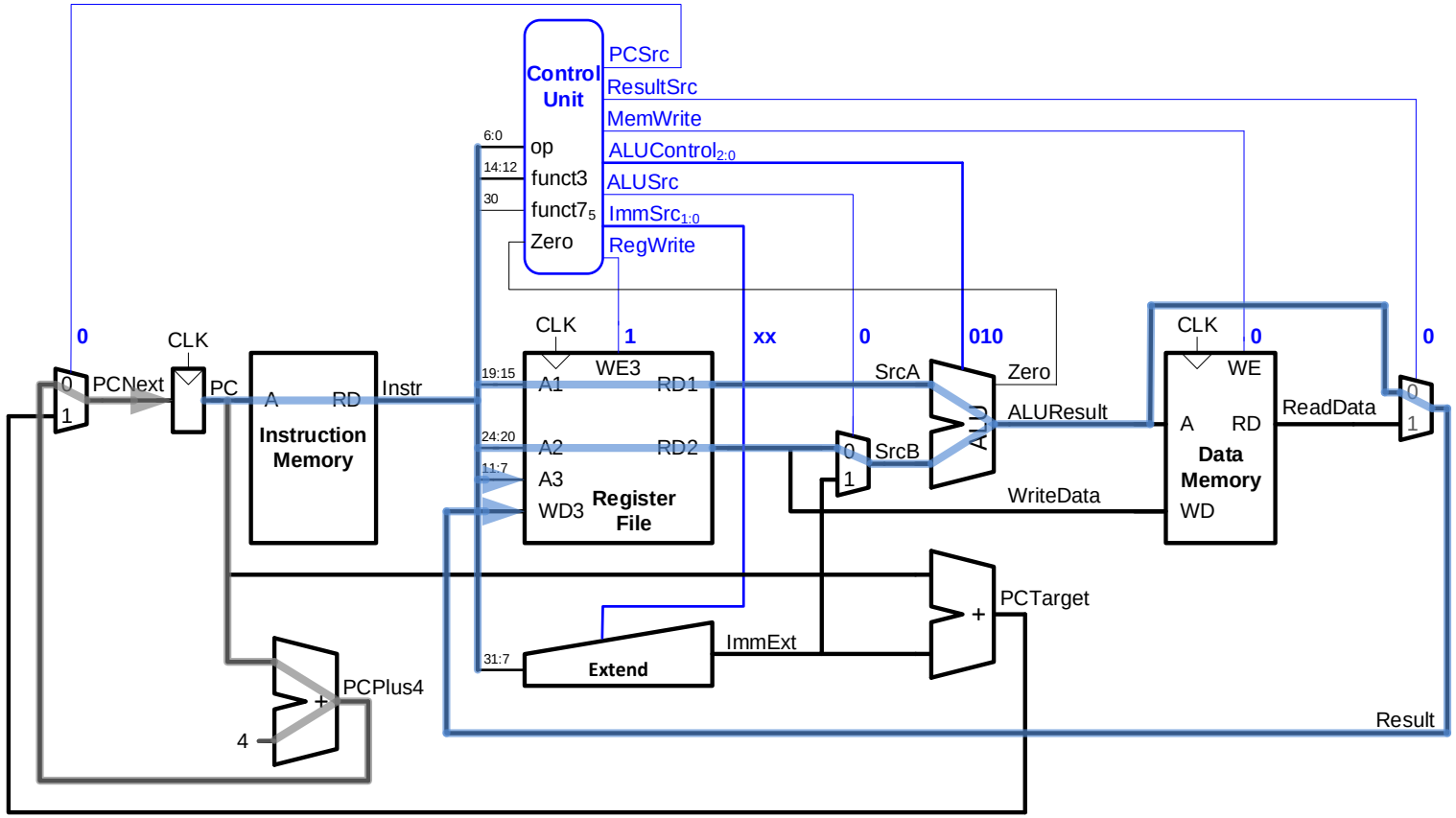
# Single-Cycle Control: ALU Decoder

| *ALUOp* | funct3 | $op_5$, $funct7_5$ | Instruction | $ALUControl_{2:0}$ |
|---|---|---|---|---|
| 00 | x | x | **lw, sw** | 000 (add) |
| 01 | x | x | **beq** | 001 (subtract) |
| 10 | 000 | 00, 01, 10 | **add** | 000 (add) |
| | 000 | 11 | **sub** | 001 (subtract) |
| | 010 | x | **slt** | 101 (set less than) |
| | 110 | x | **or** | 011 (or) |
| | 111 | x | **and** | 010 (and) |



# Example: and

| op | Instruct | RegWrite | ImmSrc | ALUSrc | MemWrite | ResultSrc | Branch | ALUOp |
|---|---|---|---|---|---|---|---|---|
| 51 | R-type | 1 | XX | 0 | 0 | 0 | 0 | 10 |




and x5, x6, x7