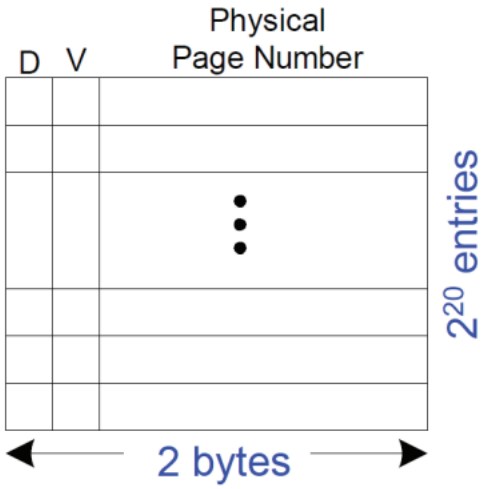
Examples from problem section and homework hints

Exercise 8.20

(a) **23 bits**
(b) $2^{32}/2^{12} = \mathbf{2^{20}}$ **virtual pages**
(c) 8 MB / 4 KB = $2^{23}/2^{12} = \mathbf{2^{11}}$ **physical pages**
(d) virtual page number: **20 bits**; physical page number = **11 bits**
(e) # virtual pages / # physical pages = $\mathbf{2^{9}}$ virtual pages mapped to each physical page.

Imagine a program around memory address 0x01000000 operating on data around address 0x00000000. Physical page 0 would constantly be swapped between these two virtual pages, causing severe thrashing.
(f) $\mathbf{2^{20}}$ page table entries (one for each virtual page).
(g) Each entry uses 11 bits of physical page number and 2 bits of status information.
Thus, **2 bytes** are needed for each entry (rounding 13 bits up to the nearest number of bytes).
(h) The total table size is $\mathbf{2^{21}}$ **bytes**.



Exercise 8.22

(a) From Equation 8.2, $AMAT = t_{cache} + MR_{cache}\,(t_{MM} + MR_{MM}\,t_{VM})$.
However, each data access now requires an address translation (page table or TLB lookup).
Thus,

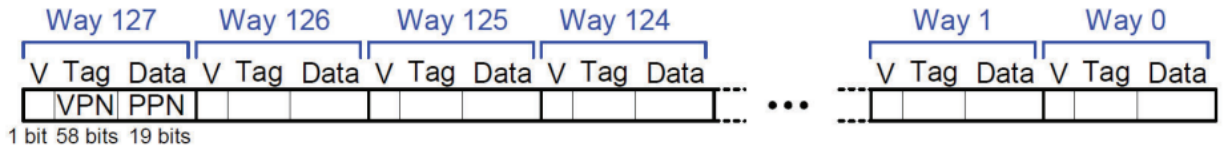
Without the TLB:
$AMAT = t_{MM} + [t_{cache} + MR_{cache}\,(t_{MM} + MR_{MM}\,t_{VM})]$
$AMAT = 100 + [1 + 0.02(100 + 0.000003(1{,}000{,}000))]$ cycles = **103.06 cycles**

With the TLB:
$AMAT = [t_{TLB} + MR_{TLB}(t_{MM})] + [t_{cache} + MR_{cache}\,(t_{MM} + MR_{MM}\,t_{VM})]$
$AMAT = [1 + 0.0005(100)] + [1 + 0.02(100 + 0.000003 \times 1{,}000{,}000)]$ cycles
= **4.11 cycles**

(b) # bits per entry = valid bit + tag bits + physical page number
1 valid bit
tag bits = virtual page number = 20 bits
physical page number = 11 bits

Thus, # bits per entry = 1 + 20 + 11 = **32 bits**
Total size of the TLB = 64 × 32 bits = **2048 bits**

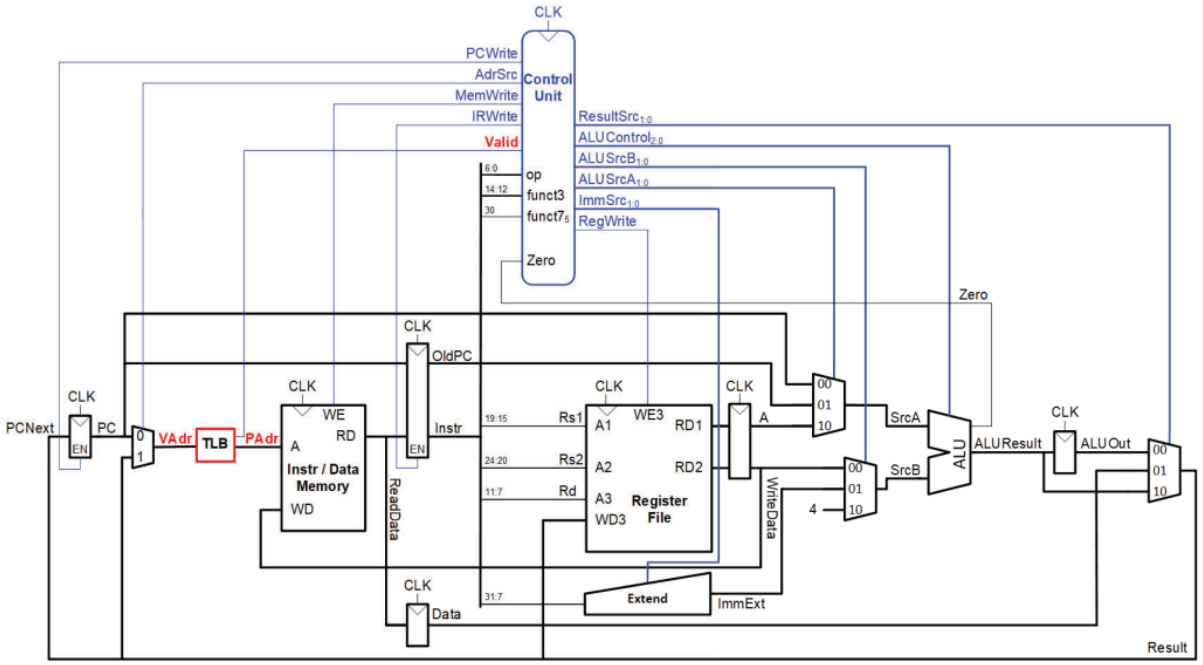
(c)



(d) **1 × 2048 bit SRAM**

Exercise 8.24

(a)



(b) Each instruction and data access now takes at least one additional clock cycle. On each access, the virtual address (*VAdr* in Figure 8.3) needs to be translated to a physical address (*PAdr*). Upon a TLB miss, the page table in main memory must be accessed.

Hints on the assignment:

- 8.21 similar to 8.20

- 8.23 similar and easier than 8.20
- 8.25: tests your understanding of the whole chapter: decision making