Materials Today: Proceedings 28 (2020) 1695–1700

Contents lists available at ScienceDirect

Materials Today: Proceedings

journal homepage: www.elsevier.com/locate/matpr

Design and analysis of CMOS based 6T SRAM cell at different technology nodes

Meenakshi Devi, Charu Madhu *, Nidhi Garg

Electronics and Communication Department, University Institute of Engineering and Technology (UIET), Panjab University, Chandigarh 160025, India

ARTICLE INFO

Article history:
Received 26 March 2020
Received in revised form 28 April 2020
Accepted 6 May 2020
Available online 5 June 2020

Keywords:
Static random access memory (SRAM)
Static noise margin (SNM)
Write static noise margin (WSNM)
Read static noise margin (RSNM)
Predictive technology model (PTM)

ABSTRACT

The CMOS technology is rapidly growing towards large scale integration on a single chip leading to smaller size consuming smaller area. The demand for speed and efficiency are also increasing day by day. With continues down scaling of technologies, the integral density of the chip increases. Stability and reliability of any memory device such as SRAM, DRAM in different environments, is a critical issue. In this paper, the design and analysis of CMOS based 6T SRAM cell at different technology nodes is demonstrated. The main purpose of this paper is to simulate 6T SRAM to evaluate the performance at different CMOS technology nodes (180 nm, 90 nm, 65 nm, 45 nm) with the help of predictive technology model (PTM) file. The constancy of the SRAM bit cell in terms of static noise margin (SNM) is analysed by butterfly curve method. Simulations are done using BSIM3 model PTM files on HSPICE tool. The results shown in this paper clearly indicate that as we proceed from 180 nm to 45 nm delay reduces and stability improves i.e. read static noise margin (RSNM) is improved by 7.72% while write static noise margin (WSNM) is improved by 5.94% of the 6T SRAM cell.

Selection and peer-review under responsibility of the scientific committee of the International Conference on Aspects of Materials Science and Engineering.

1. Introduction

The trend now a days, demand the devices which are more stable and have high processing speed. Static random access memory (SRAM) is being used in cache memory because of its certain requirements like high speed and less area [1]. The international roadmap for semiconductor (ITRS) report shows that the transistor count is increasing day by day [2] which lead to increase in the delay. Considerable attention is being paid by the researchers to achieve the optimum delay and stability of the cell. The performance of transistor gets degraded for the lower value of the threshold voltage. However, increase in the threshold voltage of the transistor, leads to increase in the cell leakage and also affects the stability of the cell [3]. The objective of the research is to enhance static noise margin (SNM) and reduce the delay of existing SRAM structures by keeping performance under control. The 6T SRAM cell is designed and analysis is carried out considering various parameters like temperature, voltage and power consumption [4–6]. Herein, 6T SRAM cell analysis based on CMOS is done to discover the impact on its parameter performance i.e. SNM, read static noise margin (RSNM), write static noise margin (WSNM), delay. SRAM cell is designed and simulated with various CMOS based technologies in HSPICE tool at same supply voltage. The conventional SRAM is designed and scaled by using the model file from Predictive Technology Model (PTM) Beta Version. Its disseminating improvement as compared with already existing work is shown in Tables 1–4) in terms of stability of the cell i.e. SNM and delay [7]. The paper is organized as follows: Section II describes the working and operations performed by SRAM cell. Section III demonstrates the experimental results achieved and Section IV summarizes the paper.

1.1. SRAM cell

SRAM cell is a type of semiconductor memory having two stable states (0, 1) in logic circuitry for data storage. The working of the SRAM memory cell is quite simple because all the operations are performed by the single bit line. The memory cells in SRAM are organized in the matrix form and each cell can be addressed individually. The data stored in the SRAM cells can read all the content at once with the help of column decoder. As the single bit line is

* Corresponding author.
E-mail address: charu_uiet@pu.ac.in (C. Madhu).

https://doi.org/10.1016/j.matpr.2020.05.130
2214-7853/
Selection and peer-review under responsibility of the scientific committee of the International Conference on Aspects of Materials Science and Engineering.

Table 1
Comparison of the HSNM between the different CMOS technologies.

6T SRAM	Previous HSNM data (mV)	Hold SNM (mV)
180 nm	869.75 [13]	350
90 nm	721[9]	300
65 nm	465 [15]	275
45 nm	261 [21]	200

Table 2
Comparison of the RSNM between the different CMOS technologies.

6T SRAM	Previous RSNM data (V)	Read SNM (V)
180 nm	0.2 [21]	0.12
90 nm	0.1 [9]	0.07
65 nm	0.09 [15]	0.065
45 nm	0.04 [21]	0.05

Table 3
Comparison of the WSNM between the different CMOS technologies.

6T SRAM	Previous WSNM data (V)	Write SNM(V)
180 nm	1.09 [21]	1.5
90 nm	0.63 [9]	1.2
65 nm	0.83 [15]	1
45 nm	0.4 [21]	0.8

Table 4
Comparison of the delay between the different CMOS technologies.

6T SRAM	Previous delay data(Ps)	Write delay (Ps)
180 nm	75 [13]	52
90 nm	83.57 [15]	42
65 nm	89.99 [15]	30
45 nm	81.82 [15]	12

connected to drain terminal of pass transistors, the tolerance capacity of noise margin gets improved. The bit lines will pass through 2 input nodes of access transistors, which control the cell stability during operations [8]. Word line present in the circuit is responsible to enable both the access transistors. The two bit lines are used to transfer the data for read and write operation. The refreshing circuit is not required in the SRAM. There are two key features of SRAM which makes it extraordinary: First, the data is held statically (the stored data in the SRAM memory works without refreshing unlike dynamic random access memory) [9]. Secondly, SRAM is basically random access memory which means the memory can access the data in any order for read and write operation, until the previous address is mentioned in the memory location. Earlier, the operations performed by the asynchronous SRAM chip follow sequence patterns. However, SRAM serves as cache memory in commercial applications which requires faster SRAM to provide direct interface with CPU. SRAM cells are used in many more applications such as portable device like digital camera, automatic electronics, cell phones, industries and scientific subsystem etc.

2. Operations of 6T SRAM cell.

The basic circuit of SRAM cell requires six transistors, two NMOS and two PMOS which behave as cross-coupled inverters with two driver transistors. In this format, the circuit has bi-stable states i.e. logic 0 & logic 1. The 6T SRAM cell offers better electrical performance parameters such as speed, SNM, low power and read current in comparison to its lower versions like 4T SRAM cell [10]. SRAM is mostly used embedded memory for CMOS ICs and it uses "Bi-stable inverter circuitry" to store a bit. During read operation, bit line and bit bar line are pre-charged after that word line is activated. The differential voltage is set among bit line and bit bar line because one of the bit-line gets discharged. The potential difference is created between nodes and can be detected by using sense amplifier. During write operation, both the bit line and bit bar line are given complementary values and then voltage is given to word line. The node which stored zero value will be discharged through pass transistor. In ideal or standby state, there is no connection established between internal nodes and bit lines. The inverters are the storage element and reinforce the data bit within the cell as long as the power is supplied [11,12].

2.1. Hold operation in SRAM

If the WL is not connected to V_{dd} as shown in Fig. 1, the driver transistors M_5 and M_6 gets disconnected from the BL and BLB of the cell. The circuitry inside the cell formed by M_1–M_4 will continue to keep the stored value as long as it is connected by electric supply. Initially the BL and BLB are not charged by column pre-charged circuit. If M3 is holding '0', then M1 would be off and M4 would be ON. Hence it will turn up the access transistor M_5. In this return M2 will be off and it will cut node Qfrom V_{dd}. Hence, zero is maintained at node Q [13].

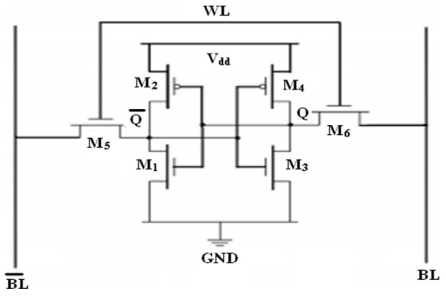

Fig. 1. Schematic diagram of 6T SRAM Cell.

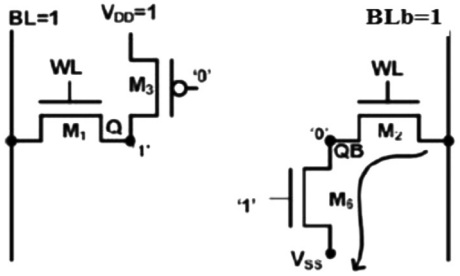

Fig. 2. Read '0' operation.

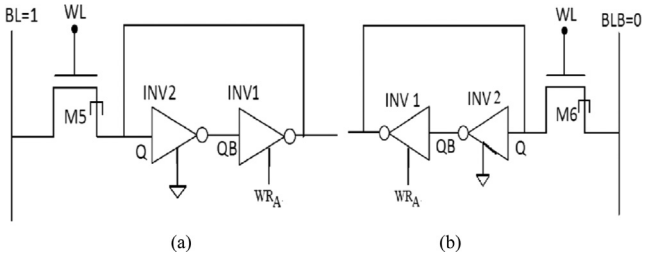

Fig 3. (a) Write '1' operation (b) Write '0' operation [12]

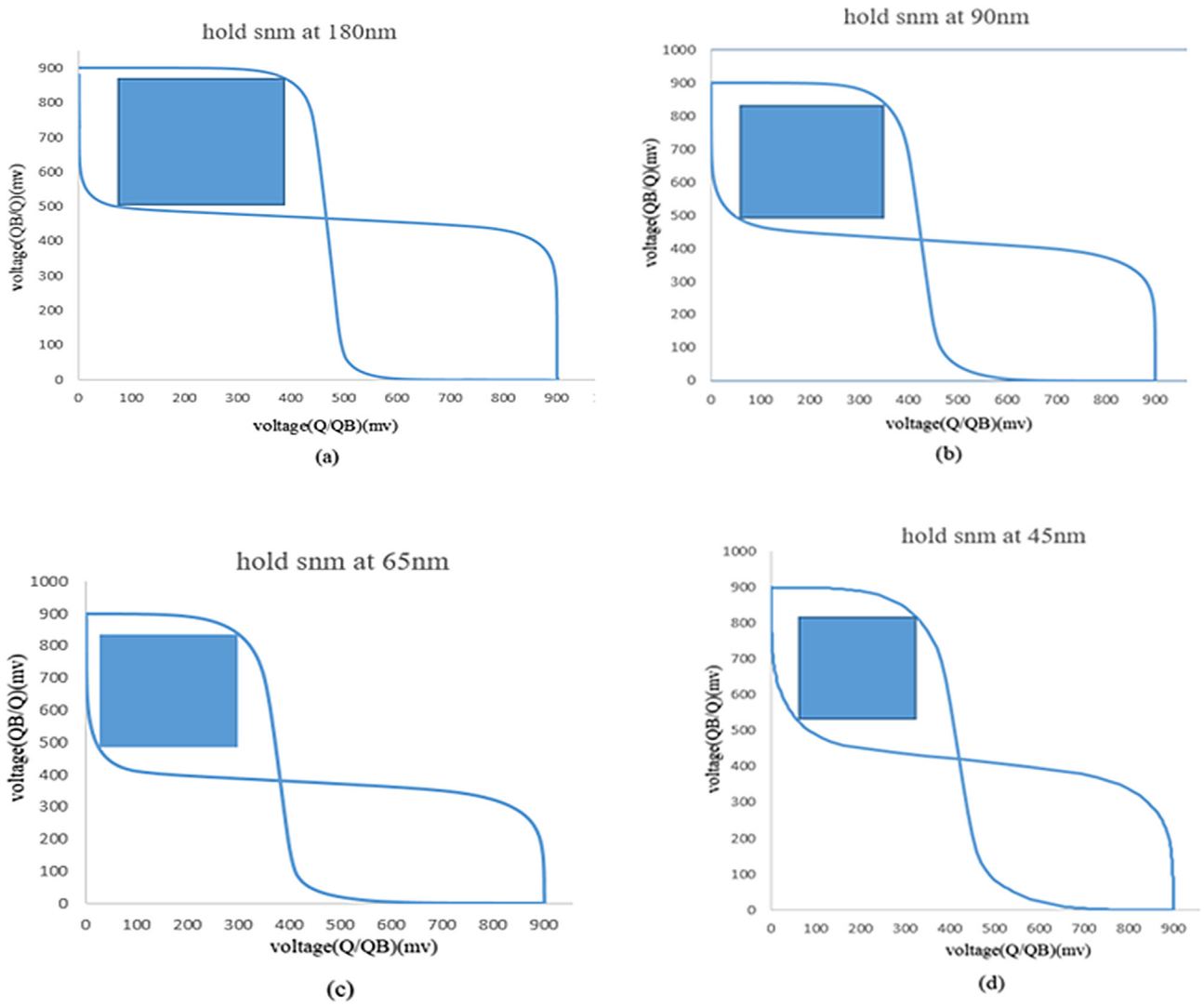

Fig. 4. Experiment results of HSNM at (a) 180 nm (b) 90 nm (c) 65 nm (d) 45 nm.

2.2. Read operation in SRAM

This operation is started by pre-charging both lines (BL, BLB) and then WL is activated. Let '1' is stored at Q, read current will not find path to discharge. Thus, the value stored at node Q will remain same. If Q is stored '0', then the path will be created between PMOS and ground and it will immediately proceed to intermediate voltage. But undesired bump will be created due to voltage differences. The reason behind the unwanted bump is voltage generated at node Q (by the voltage divider between access transistor and NMOS). This voltage does cross the threshold value [14,15]. The best way to explain the read operation is by taking the example as shown in Fig. 2. Suppose '1' is given to left side node Q and '0' is given to right side node QB. This will turn on the cell M_2 and cell M_1 will be in off mode. When the word line goes high, then the current will flow through M_2 to V_{ss} via M_6. The circuit will start discharging the corresponding bit line capacitance. On the other hand the voltage on the BLB remains high since there is no way to discharge [16].

2.3. Write operation in SRAM

Fig. 3 illustrate write '1' and write '0' operation in SRAM. Primarily, word line is charged by supply voltage V_{dd}. Let us assume that the node QB and Q store values '1'& '0'respectively. The access transistor 'M5' is connected to bit-line (initially at '0') is turned ON. This creates potential difference across 'M5' transistor and current flows through 'M2 to 'M5'. This shows that the current flows towards the lower potential and node QB is set at low voltage level for successful write '0' operation. It happens so because the bit line access transistors (NMOS) are created stronger than the PMOS transistors in the cell itself. They can easily overrule, no problem is incurred [17].

3. Performance parameters and comparison

The cell stability level is measured by the extent of its durability against noise and DC disturbances. SNM is one of dominant way to analyse and negotiate the stability. The factors affecting the stability of SRAM cell are mainly DC noise and offset. Basically SNM tells the noise tolerance capacity of the single bit cell without toggling their present state. The disturbance occurs mainly when the operating condition changes during environmental variations. There are two methods to calculate SNM. One method is to add some noise intentionally and then to find out where the stored data over turn. The other way is the graphical approach. The best way to measures SNM is butterfly curve method. It is calculated with the help of perfect square fit between the butterfly curve loops [18]. The given 6T SRAM cell is simulated at scaled technologies

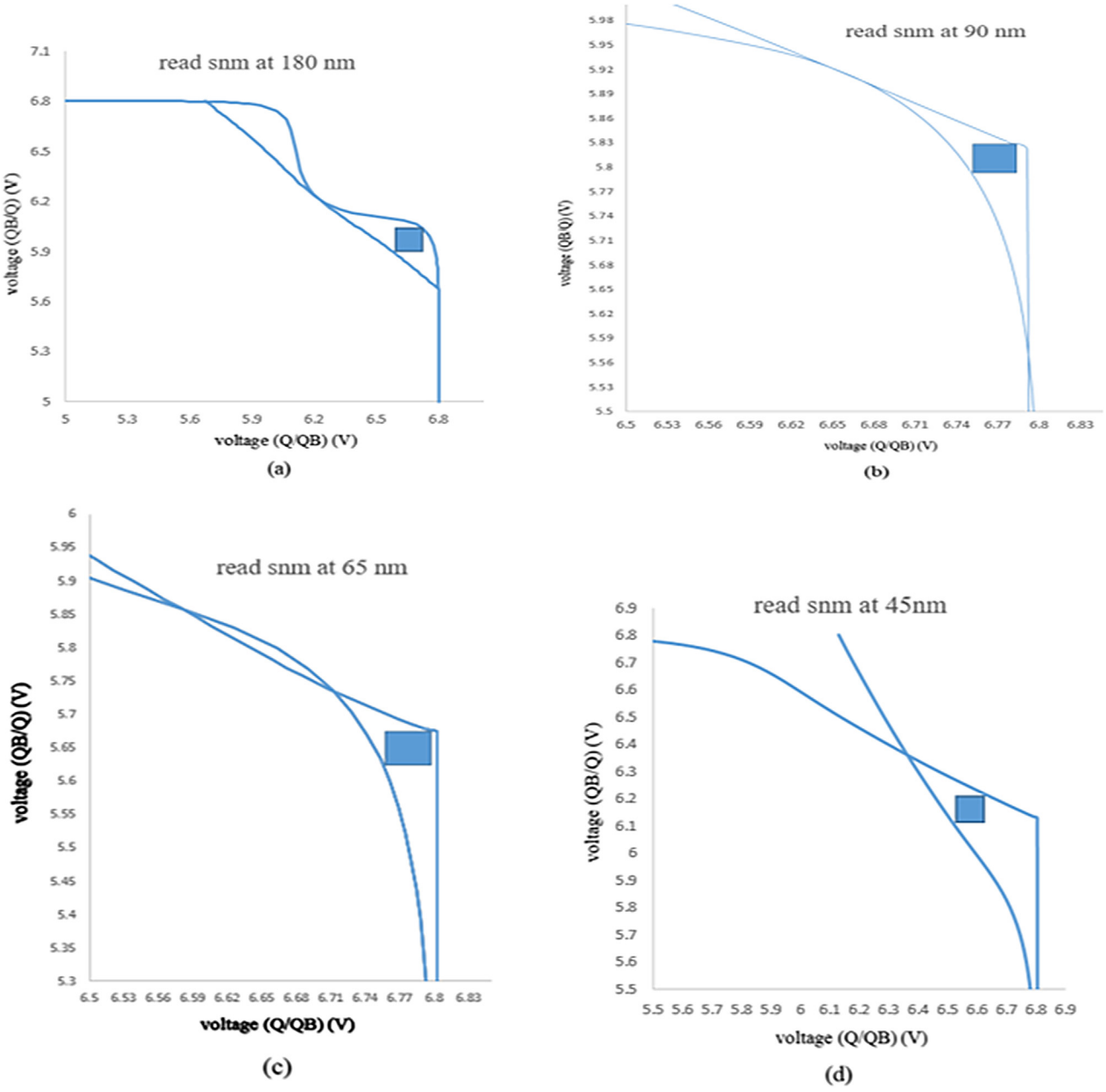

Fig. 5. Experimental results of RSNM at (a) 180 nm (b) 90 nm (c) 65 nm (d) 45 nm.

mainly 180 nm, 90 nm, 65 nm, 45 nm keeping the parameters same. The effect of the SRAM cell is mostly compared on the basis of performance parameters namely noise margin, RSNM, WSNM and delay.

3.1. Static noise margin

SNM specifies the maximum value of DC voltage that can be tolerated by SRAM cell by adding noise free input values without altering the output voltages. With the lower technologies, the size of the memory cell is small. There is exponential relation between sub threshold voltage and channel length of the transistors in the SRAM cell. The threshold voltage reduces in correspondence with the reduction in the channel length to maintain the cell stability at scaled technologies [18,19]. Fig. 4 shows Hold static Noise Margin (HSNM) of the 6T SRAM cell at V_{dd} of 0.9 V leading to the enhancement of HSNM (24.85% average improvement is observed).

3.2. Read static noise margin

Read static noise margin (RSNM) is the measure of the ability of the cell to read the stored data. In scaled technology nodes, the read current mainly gets disturbed when the stored data changes frequently due to the scaling of critical current. This increases the voltage strictly and improves the SNM during read operation i.e. RSNM [19]. Fig. 5 shows the read static noise margin of the 6T SRAM cell at different CMOS technologies at V_{dd} 0.9 V. The 6T SRAM cell at scaled technologies exhibits edgy transition in the voltage transfer curve (VTC) which demonstrates enhancement in the RSNM of the cell on an average of 7.72%.

3.3. Write static noise margin

This figure of merit defines the write ability (i.e. how easily the bit line stores the data). Max disturbance or noise that a cell can

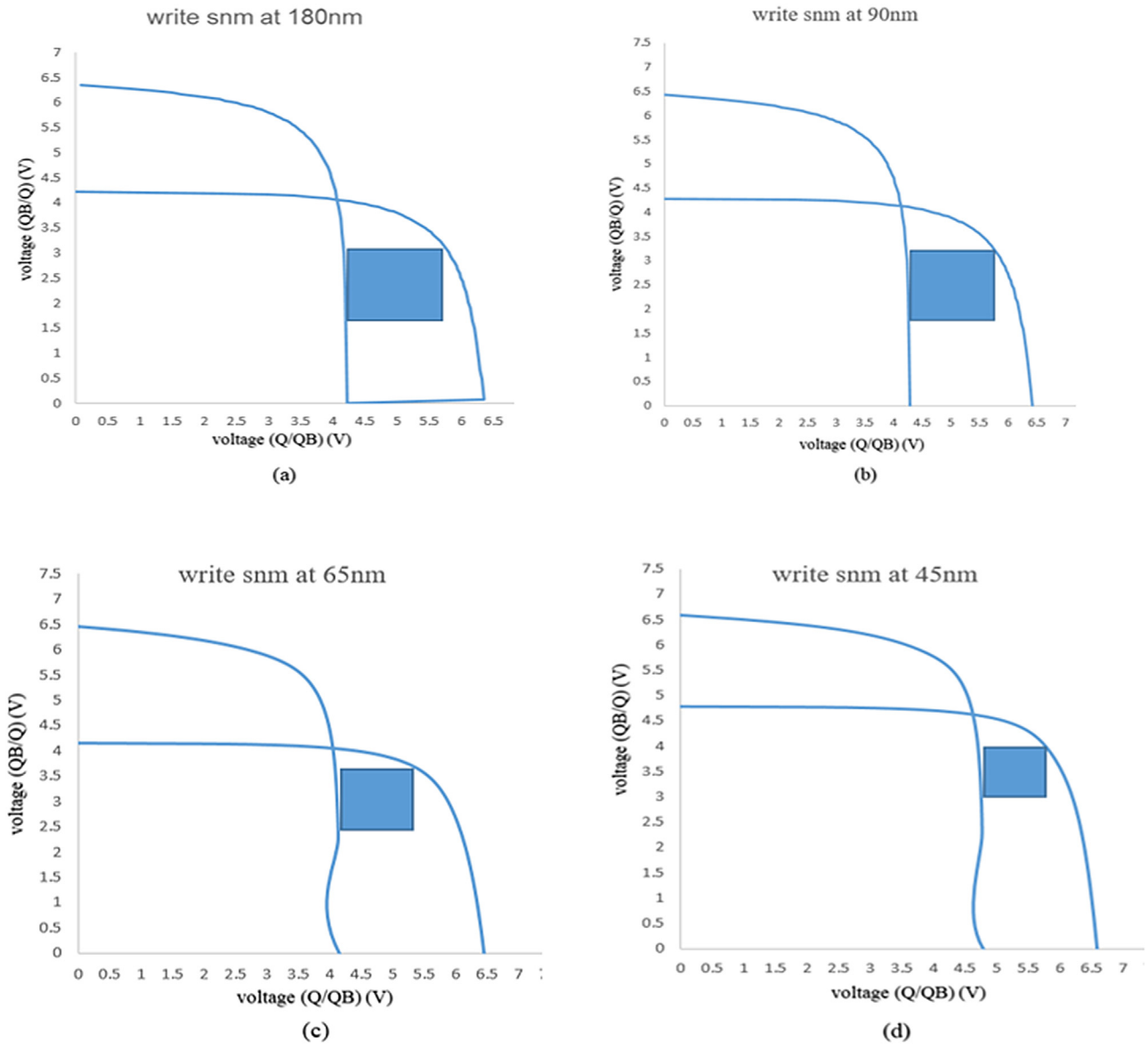

Fig. 6. Experimental results of WSNM at (a) 180 nm (b) 90 nm (c) 65 nm (d) 45 nm.

tolerate is known as write margin. The intention of this analysis is to portray minimum demand of voltages at scaled technology nodes [19,20]. During write cycle, stronger access transistor and weaker pull up transistor are used which improves write static noise margin (WSNM) at scaled technologies. Fig. 6 shows the WSNM of the 6T SRAM cell at different CMOS technologies at V_{dd} of 0.9 V. The 6T SRAM cell at scaled technologies exhibits edgy transition in the VTC which enhances the WSNM of the cell on an average of 5.94%.

3.4. Delay

A comparison of the write delay between various technologies of CMOS based 6T SRAM cell at V_{dd} of 0.9 V is presented in table 4. It is observed that write delay is reduced with technology scaling by keeping supply voltage same. The delay of the 6T SRAM cell is reduced by 14% when compared for various scaled technologies [15,20].

4. Conclusion

This paper demonstrated CMOS based 6T SRAM cell design and the results are compared for different technology nodes (180 nm, 90 nm, 65 nm, 45 nm). It is demonstrated that BSIM3 CMOS based 6T SRAM offers less delay, less read margin and less write margin resulting in improved stability of the cell as compared to previously reported data. BSIM3 CMOS based 6T SRAM cell demonstrates delay of 12 ps at 45 nm being 14% lesser than the reference data. The CMOS based SRAM cell has shown 24.85% improvement in SNM. The improved SNM achieved by the circuit makes it more stable than the earlier SRAM reported in the literature. The 6T SRAM cell has shown 5.94% improvement in WSNM. The device thus can be used at higher speed. 7.72% improvement

in RSNM is also observed. The study resulted in reduction in delay making CMOS based 6T SRAM cell at 45 nm appropriate for its use for high speed application like aircrafts and satellites.

CRediT authorship contribution statement

Meenakshi Devi: Data Curation, Formal Analysis, Investigations, Software, Visualization, Writing- Original draft. **Charu Madhu:** Conceptualization, Formal Analysis, Methodology, Resources, Supervision, Visualization, Writing- review and editing. **Nidhi Garg:** Conceptualization, Methodology, Supervision, Visualization, Writing- review and editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

The authors acknowledges support from the Electronics and Communication Department, UIET, Panjab University for providing the lab facilities to carry out this research work.

References

[1] A. Agal, Pardeep, B. Krishan, 6T SRAM Cell: Design And Analysis, Int. J. Eng. Res. Appl. 4 (2014) 574–577.
[2] A. Bhaskar, Design and analysis of low power SRAM cells, in: 2017 Innovations in Power and Advanced Computing Technologies (I-PACT), IEEE, 2017: pp. 1–5. doi:10.1109/IPACT.2017.8244888.
[3] Y. Cao, A. Balijepalli, S. Sinha, C.-C. Wang, W. Wang, W. Zhao, The Predictive Technology Model in the Late Silicon Era and Beyond, Foundations and Trends® in Electronic Design Automation. 3 (2009) 305–401. doi:10.1561/1000000012.
[4] M. Jagasivamani, Dong Sam Ha, "Development of a low-power SRAM compiler," ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196), Sydney, NSW, 2001, pp. 498-501 vol. 4.
[5] P.S. Kanhaiya, C. Lau, G. Hills, M. Bishop, M.M. Shulaker, 1 Kbit 6T SRAM Arrays in Carbon Nanotube FET CMOS, in: 2019 Symposium on VLSI Technology, IEEE, 2019: pp. T54–T55. doi:10.23919/VLSIT.2019.8776563.
[6] R. Kolhal, V. Agarwal, A Power and Static Noise Margin Analysis of different SRAM cells at 180nm Technology, in: 2019 3rd International Conference on Electronics, Communication and Aerospace Technology (ICECA), IEEE, 2019: pp. 6–12. doi:10.1109/ICECA.2019.8821868.
[7] A.A. Kumar, A. Chalil, Performance Analysis of 6T SRAM Cell on Planar and FinFET Technology, in: 2019 International Conference on Communication and Signal Processing (ICCSP), IEEE, 2019, pp. 0375–0379, https://doi.org/10.1109/ICCSP.2019.8697928.
[8] C.A. Kumar, B.K. Madhavi, K. Lalkishore, Performance analysis of low power 6T SRAM cell in 180nm and 90nm, in: 2016 2nd International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), IEEE, 2016, pp. 351–357, https://doi.org/10.1109/AEEICB.2016.7538307.
[9] R. Kataria, Priya, Neeharika, Design And Performance Analysis of 6T SRAM cell at 90nm Technology, Int. J. Adv. Res. Electron. Commun. Eng. 5 (2016) 984–987.
[10] S. Banu, S. Yogesh, R. Kamalam, Design of Low Power 6T SRAM 8 * 8 Array Using Gateway Transistor, International Journal of Advanced Research in Education & Technology (IJARET) 2 (2015) 125–128.
[11] A. Pathak, D. Sachan, H. Peta, M. Goswami, A Modified SRAM Based Low Power Memory Design, in: 2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID), IEEE, 2016, pp. 122–127, https://doi.org/10.1109/VLSID.2016.80.
[12] P. Raikwal, V. Neema, A. Verma, Design and analysis of low power single ended 8T, in: SRAM ARRAY (4×4) at 180nm technology, in: 2016 International Conference on Signal Processing, Communication, Power and Embedded System (SCOPES), IEEE, 2016, pp. 312–316, https://doi.org/10.1109/SCOPES.2016.7955841.
[13] I. Rizvi, R. Nidhi, M.S. Hashmi Mishra, Design and analysis of a noise induced 6T SRAM cell, in: 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), IEEE, 2016, pp. 4209–4213, https://doi.org/10.1109/ICEEOT.2016.7755510.
[14] A. Singh, M. Khosla, B. Raj, CNTFET modeling and low power SRAM cell design, in: 2016 IEEE 5th Global Conference on Consumer Electronics, IEEE, 2016: pp. 1–4. doi:10.1109/GCCE.2016.7800437.
[15] S. Poonam, M. Soni Taleja, Study and simulate the 6t sram cell & analysis the parameters delay & power with the variation of vdd & temperature at 45nm, 65nm & 90nm technologies, Int. J. Tech. Res. (IJTR) 2 (2013) 1–5.
[16] K. Verma, S.K. Jaiswal, D. Jain, V. Maurya, Design and Analysis of 1-Kb 6T SRAM Using Different Architecture, in: 2012 Fourth International Conference on Computational Intelligence and Communication Networks, IEEE, 2012, pp. 450–454, https://doi.org/10.1109/CICN.2012.81.
[17] K. Verma, S.K. Jaiswal, M.A. Khan, Design of a high performance and low power 1Kb 6T SRAM using bank partitioning method, in: 2011 International Conference on Multimedia, Signal Processing and Communication Technologies, IMPACT , 2011. (2011), pp. 56–59, https://doi.org/10.1109/MSPCT.2011.6150519.
[18] J. Zhang, Z. Wang, N. Verma, In-memory computation of a machine-learning classifier in a standard 6T SRAM Array, IEEE J. Solid-State Circ. 52 (2017) 915–924, https://doi.org/10.1109/JSSC.2016.2642198.
[19] S. Bala, M. Khosla, Design and performance analysis of low-power SRAM based on electrostatically doped tunnel CNTFETs, J. Comput. Electron. 18 (2019) 856–863, https://doi.org/10.1007/s10825-019-01345-z.
[20] S.K. Kingra, C. Madhu, A. Sharma, N. Priya, 3D device simulation of 6T SRAM cell with voltage scaling in 90nm CMOS, in: 2015 International Conference on Signal Processing, Computing and Control (ISPCC), IEEE, 2015, pp. 241–246, https://doi.org/10.1109/ISPCC.2015.7375033.
[21] T. Mohita, T. Newar, J. Chowdhury Roy, J.K. Das, "Design and stability analysis of CNTFET based SRAM Cell', 2016 IEEE Students' Conf. Electr. Electron. Comput. Sci. SCEECS 2016, 2016, 1–5.