A 256 × 256 CMOS Imaging Array with Wide Dynamic Range Pixels and Column-Parallel Digital Output

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***Abstract*—A stepped reset-gate voltage technique is applied to a CMOS active pixel sensor array to increase dynamic range by 26 dB. A frame rate of 390 frames/s is achieved using column-parallel output circuits. Switched-capacitor correlated double-sampling circuits reduce fixed-pattern noise to 4.0 mV (dark). Cyclic analog-to-digital converters achieve approximately 9-b accuracy. At 30 frames/s, random noise is 0.56 mV (dark), optical dynamic range is 96 dB, and power is 52 mW.**

***Index Terms*— Active pixel sensor (APS), analog–digital conversion, CMOS analog integrated circuits, image sensors, smart pixels.**

I. Introduction

ACTIVE pixel sensor (APS) arrays are under extensive investigation as a possible alternative to conventional charge-coupled device (CCD) imagers. Potential benefits include increased system integration, reduced power consumption, and flexible pixel addressing. The CMOS image sensor described in this paper is intended for an automotive stereo vision system, where the scene dynamic range may be as much as five orders of magnitude [1]. If the scene dynamic range exceeds the sensor dynamic range, portions of the image will be clipped in the dark and/or bright regions. The dynamic range of typical CMOS image sensors is around 70 dB, which is well below the application requirement.

Previous techniques for extending dynamic range usually employ a nonlinear imaging element, often the gate-source voltage of a subthreshold MOSFET or the voltage across a forward-biased diode [1]–[8]. Depending on the specific technique, these schemes may suffer from image lag, large pixel size, inflexible compression characteristic, or long integration time.

This paper describes the design and evaluation of a 256 × 256 CMOS pixel array, which uses a dynamic range expansion technique providing flexible digital control of the compression characteristic. This allows the user to change the compression based on the lighting conditions or system requirements and allows simple data processing to invert the compression and obtain the original image. The pixel does not require any components beyond those normally present in a standard CMOS pixel. Pixel readout is column-parallel for high frame rate, with one correlated double-sampling (CDS) circuit per column and one analog-to-digital converter (ADC) per two columns.

The theory behind the wide dynamic range algorithm is described in Section I. The imager design is discussed in Section II. Measured test results from a prototype imager are presented in Section III. Conclusions are provided in Section IV.

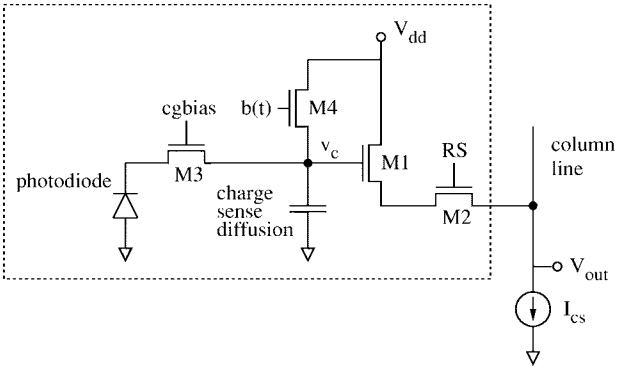

Fig. 1. Equivalent schematic of pixel.

II. Theory

The technique used to increase dynamic range was originally described in terms of a CCD pixel [9], [10] but can be readily adapted to a CMOS pixel. The equivalent circuit and cross section for the CMOS pixel are shown in Figs. 1 and 2, respectively. The structure is essentially identical to a standard APS pixel design. A charge spill gate $M3$ is added to increase the sensitivity but is not necessary to implement the wide dynamic range algorithm. $M3$'s gate is held at a constant potential of approximately 1 V. Charge generated in the photodiode flows into $M3$'s source and is discharged through $M3$'s drain into the charge sense diffusion. This allows charge generated over a large n^+ diffusion area to be

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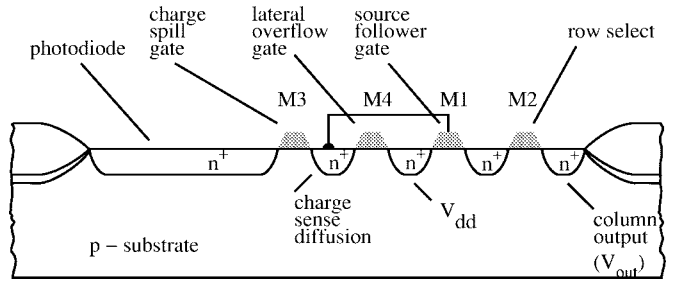


Fig. 2. Cross section of wide dynamic range pixel.

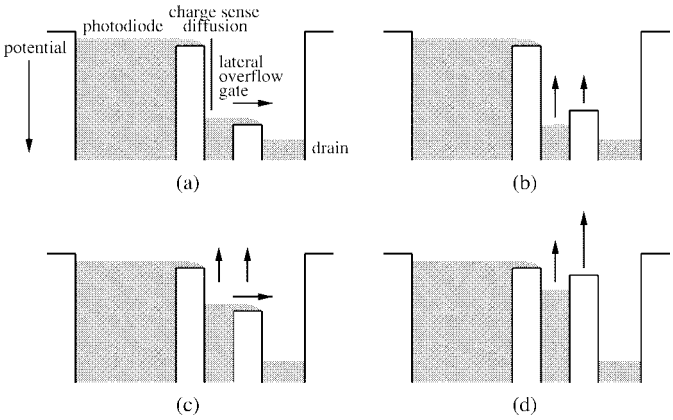


Fig. 3. Integration and reset sequence for wide dynamic range. (a) Pixel reset; previously integrated charge is dumped to drain. (b) Start of integration period; charge freely accumulates in photodiode. (c) Photodiode charge limited by lateral overflow gate. (d) Near end of integration period; charge freely accumulates in photodiode.

sensed using a small capacitance. Since the photodiode is not reset between frames, the charge spill gate is likely to increase image lag.

Fig. 3 shows the operating sequence for the wide dynamic range (compressive) pixel. In Fig. 3(a), the pixel is first reset by pulling the lateral overflow gate voltage $B(t)$ high. This lowers the potential barrier between the charge sense node and drain diffusion and allows excess charge to flow into the drain. In (b), after reset, the lateral overflow gate is abruptly raised a small amount. Charge begins to accumulate in the photodiode at a rate proportional to the illumination. Over the integration period, the lateral overflow gate rises at a rate that increases with time. In (c), if the illumination is sufficiently high, there will be a period of time in the integration interval during which the photodiode charge is limited by the lateral overflow gate. In (d), eventually, the lateral overflow gate rises fast enough to retain all of the photocurrent entering the integration well. At the end of the integration period, the row select is turned on and the output voltage is sensed on the column output line.

Compared to the standard pixel, the compressive pixel has significantly different properties in three areas. The main difference is the intentional change in the transfer characteristic relating input illumination to output voltage, described in Section II-A. However, the random and fixed-pattern noise (FPN) as functions of illumination also change. These differences are explained in Sections II-B and II-C.

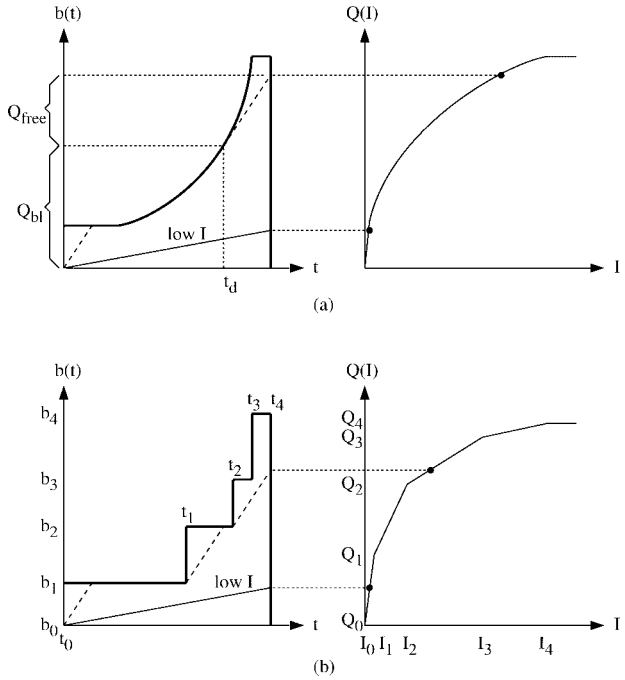


Fig. 4. Example barrier and charge integration curves. The barrier curves are shown in bold. Charge integration curves for high and low illumination are shown by dashed and solid lines, respectively. (a) Continuous barrier and (b) stepped barrier.

A. Relationship Between Barrier Curve and Compression Curve

The barrier height as a function of time is referred to as the barrier curve $b(t)$, and the resultant integrated charge as a function of illumination is referred to as the compression curve $Q(I)$. Example barrier curves and their corresponding compression curves are shown in Fig. 4. The barrier height $b(t)$ represents the charge capacity of the sense node and is the product of the sense-node capacitance and barrier potential voltage, which is a function of the lateral overflow gate voltage $B(t)$.

The continuous-time case is shown in Fig. 4(a). The charge integration curve (integrated charge as a function of time) is shown for two illumination levels. For low illumination, the charge integration curve stays below the barrier, and all photogenerated charge is retained for the entire integration period. For high illumination, the charge integration curve starts below the barrier curve and rises linearly. At some point, the charge integration curve intersects the barrier curve. The charge integration curve cannot go above the barrier curve, since that excess charge would immediately flow to the drain node. The charge integration curve therefore follows the barrier curve until the slope of the barrier curve equals the initial slope of the charge integration curve. This time is the "departure time" t_d. From t_d until the end of the integration period, the barrier curve lies above the charge integration curve, and all photocharge falling on the pixel during this interval is retained.

The integrated charge at time t_d is referred to as the barrier-limited charge Q_{bl} because the integrated charge is continuously limited by the barrier curve until time t_d. The

charge integrated between t_d and the end of the integration period is referred to as the freely integrated charge Q_{free} because no photogenerated carriers flow into the drain during this period.

For convenience, the barrier curve is approximated by a stepped waveform as shown in Fig. 4(b). Charge integration curves corresponding to low and high illumination levels are again shown. The resultant compression curve is now piecewise linear, and the number of segments is equal to the number of steps in the barrier function. The departure time must be one of the t_i; in this example, it is t_2.

A relationship between $b(t)$ and $Q(I)$ can be determined assuming that the photocurrent is constant over the integration period. The barrier curve is defined by the N corners (t_i, b_i), and the compression curve by the N breakpoints $(I_k, Q(I_k))$. Levels should be chosen so that the piecewise linear curve connecting the points $(t_i, b(t_i))$ is convex upward. Otherwise, the compression curve will have fewer than N segments

$$\frac{b_1}{t_1} < \frac{b_i - b_{i-1}}{t_i - t_{i-1}} < \frac{b_{i+1} - b_i}{t_{i+1} - t_i}, \quad 2 \le i \le N-1. \tag{1}$$

The compression curve is piecewise linear, with positive but decreasing slopes. The compression curve always starts at zero, and limits at the saturation charge $Q_{\max}$ for $I \ge I_N$.

If the barrier levels b_k and departure times t_k are known, the compression curve breakpoints $(I_i, Q(I_i))$ can be calculated. Breakpoints occur when the charge integration curve departure point switches from $t_d = t_k$ to $t_d = t_{k+1}$. At this point, both t_k and t_{k+1} are departure points. The charge integration curve passes through (t_k, b_k) and (t_{k+1}, b_{k+1})

$$I_i = \frac{b_i - b_{i-1}}{t_i - t_{i-1}}, \quad 1 \le i \le N \tag{2}$$

$$Q(I_i) = b_{i-1} + I_i(T - t_{i-1}), \quad 1 \le i \le N. \tag{3}$$

Similarly, for almost any piecewise-linear compression curve, barrier levels b_k and departure times t_k can be found to obtain that compression curve. The departure times are uniquely determined by the slopes of the segments of the compression curve; once these are known, the barrier levels can be found by rearranging (3)

$$t_k = T - \frac{Q(I_{k+1}) - Q(I_k)}{I_{k+1} - I_k}, \quad 0 \le k \le N-1 \tag{4}$$

$$b_k = Q(I_{k+1}) - I_{k+1}(T - t_k), \quad 0 \le k \le N-1. \tag{5}$$

B. Random Noise

The main contributions to pixel random noise are shot noise from the current flowing over the barrier, the dark current, and the photogenerated current.

Subthreshold current flows through the charge spill device and lateral overflow gate during reset, and during a portion of the integration period if the illumination is high enough. It is assumed that the shot noises on the currents through $M3$ and $M4$ are independent but have the same magnitude (since the average currents are the same). The voltage noise at the sense node is calculated by integrating the product of the current noise spectral density and the sense node impedance

$$v_{n,bar}^2 = 2\int_0^\infty \frac{2qI}{|g_s + j2\pi f C_{\text{sense}}|^2}\, df \tag{6}$$

$$= (4qI)\frac{g_s}{C_{\text{sense}}}\frac{1}{2\pi}\frac{\pi}{2}\left(\frac{1}{g_s}\right)^2 \tag{7}$$

$$= \frac{qI}{g_s C_{\text{sense}}} \tag{8}$$

$$= \frac{kT}{C_{\text{sense}}} \tag{9}$$

where the conductance looking into the source of the lateral overflow transistor is

$$g_s = \frac{I}{kT/q} \tag{10}$$

and C_{sense} is the total capacitance on the charge sense node. This number is doubled by the CDS operation, since the shot noise is uncorrelated between the intervals when charge flows over the barrier. This noise component is not a function of illumination. Although this result is identical to the well-known result for reset noise of a (CCD) output diffusion [11], that was not immediately obvious since the noise mechanisms are different.

The total random noise is the sum of the random noise at the departure time, given by the expression above, and the random noise due to charge accumulated between the departure time and the end of the integration period. The charge accumulated during this interval is simply Q_{free}, and the associated number of noise electrons is equal to the square root of the number of integrated electrons. This, in turn, is a function of the photocurrent, dark current, and chosen compression function. The associated random noise voltage on the sense node is

$$v_{n,phot}^2 = \frac{qQ_{\text{free}}}{C_{\text{sense}}^2} \tag{11}$$

and the total random noise with CDS is therefore

$$v_{n,tot}^2 = 2\frac{kT}{C_{\text{sense}}} + \frac{qQ_{\text{free}}}{C_{\text{sense}}^2}. \tag{12}$$

C. FPN

FPN is caused by mismatches in the optical aperture A_{opt}, the sense node source/drain capacitance C_{sd}, pixel dark current I_{dark}, $M1$'s width and length W_1 and L_1, $M1$'s effective threshold voltage $V_{te,1}$, $M3$'s drain overlap capacitance $C_{ol,3}$, $M4$'s effective threshold voltage $V_{te,4}$, column bias current I_{cs}, row select "on" resistance $r_{ds,2}$, $M1$'s back-gate parameter γ_{M1}, and $M4$'s overlap capacitance $C_{ol,4}$. FPN associated with a mismatch source is determined by comparing the output voltages of two pixels that differ in that one parameter but are otherwise identical [12].

Table I lists the sources of FPN and the sensitivity of the pixel output voltage to each mismatch. These sensitivities are shown qualitatively in Fig. 5. Mismatches in I_{cs}, $r_{ds,2}$ $V_{te,M1}$, and $\Delta V_{te,M4}$ produce the same output offset voltage

TABLE I
FPN SOURCES IN WIDE DYNAMIC RANGE PIXEL

Parameter	Sensitivity
C_{sd}, $C_{ol,3}$	$\frac{G_{sf}}{C_{sense}^2}Q'$
A_{opt}	$-G_{sf}\frac{Q_{free}}{A_{opt}C_{sense}}\frac{I}{I+I_{dark}}$
I_{dark}	$-G_{sf}\frac{Q_{free}/C_{sense}}{I+I_{dark}}$
$V_{te,1}$	-1
$V_{te,4}$	-1
$C_{ol,4}$	$\frac{G_{sf}}{C_{sense}^2}\left(Q_{free}-\frac{C_{ol,4}}{C_{sense}}(Q_{max}-Q_{bl})\right)$
I_{cs}	$-\frac{G_{sf}}{g_{m1}}$
W_1	$\frac{2}{3}L_1C_{ox}(1-G_{sf})\frac{G_{sf}Q'}{C_{sense}^2}+\frac{G_{sf}I_{cs}}{g_{m1}W_1}$
L_1	$\frac{2}{3}W_1C_{ox}(1-G_{sf})\frac{G_{sf}Q'}{C_{sense}^2}-\frac{G_{sf}I_{cs}}{g_{m1}L_1}$
$r_{ds,2}$	$-I_{cs}$
γ_1	$-\frac{1}{2}\frac{g_{m1}}{g_{mb1}}\gamma_1$

$$Q' = Q_{free} + \frac{C_{ol,4}}{C_{sense}}(Q_{max} - Q_{bl})$$

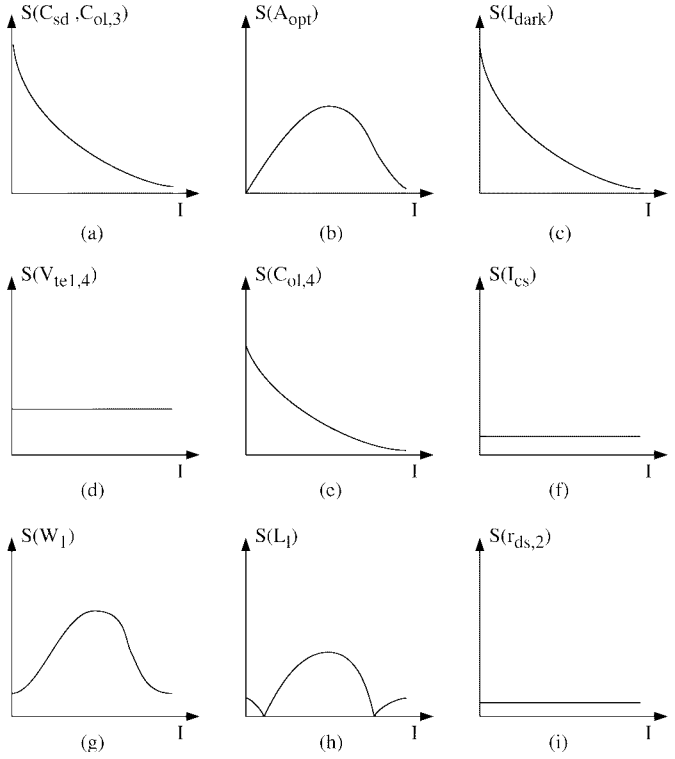


Fig. 5. Qualitative FPN sensitivities for various mismatch sources in wide dynamic range pixel.

at all illuminations. Mismatch in A_{opt} affects only the freely accumulated charge Q_{free}. It does not affect Q_{bl} because there are a limited number of barrier level values b_k that Q_{bl} can have, and it requires a large change in illumination or FPN to switch between barrier levels. Mismatch in A_{opt} does not

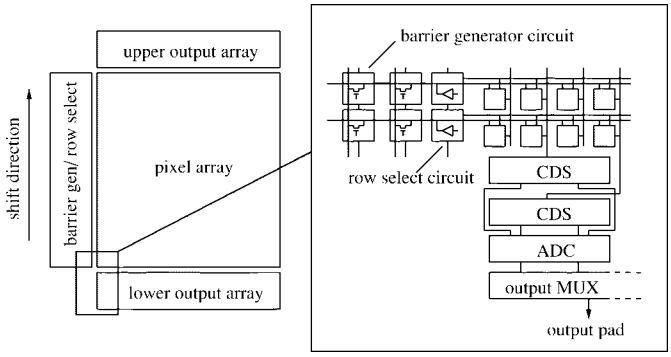


Fig. 6. Block diagram of test chip.

contribute to dark FPN because there is no photogeneration in the dark. At high illumination, the FPN sensitivity depends on the barrier curve; the plots in Fig. 5 assume that the free charge component tends toward zero as the pixel saturates. The most important FPN sources are those that cause dark offset errors that cannot be removed by CDS. This includes mismatches in I_{dark} and any component of C_{sense}. The FPN due to dark current mismatch is

$$\text{FPN}_{I_{\text{dark}}} = G_{sf}\frac{I_{\text{dark}}T_{\text{int}}}{C_{\text{sense}}}\frac{\Delta I_{\text{dark}}}{I_{\text{dark}}} \tag{13}$$

where G_{sf} is the source-follower gain. Using the measured value of I_{dark} and a 33-ms integration time, and assuming a I_{dark} mismatch of 20%, $\text{FPN}_{I_{\text{dark}}}$ would be about 1.2 mV. The FPN due to sense capacitance mismatch is

$$\text{FPN}_{C_{\text{sense}}} = G_{sf}\frac{C_{ol,4}}{C_{\text{sense}}}\frac{(b(0)-b(T_{\text{int}}))}{C_{\text{sense}}}\frac{\Delta C_{\text{sense}}}{C_{\text{sense}}} \tag{14}$$

where $b(0)$ is the barrier curve value at reset and $b(T_{\text{int}})$ is the barrier curve value at the end of the integration period. Assuming a 2% C_{sense} mismatch, $\text{FPN}_{C_{\text{sense}}}$ would be about 2.8 mV. These are rough estimates based on assumed mismatches, which could be significantly larger or smaller.

III. IMAGE DESIGN

A block diagram of the imager is shown in Fig. 6. The imager includes a 256 × 256 array of wide dynamic range pixels and a 256-stage, 9-bit shift register for barrier generation and row select. Each column has a dedicated CDS circuit, and every two columns share a cyclic ADC. The barrier generation shift register is described first, then the CDS and ADC circuits.

A. Barrier Generation

The barrier voltage waveform is generated by an 8-bit wide, 256-stage digital shift register. Three bits are entered from off-chip and decoded to produce an 8-bit word containing exactly one "1" bit. Once every row readout time, the shift register is advanced by one row and the new word is entered at the front. In each row, the corresponding word selects one of eight analog bias lines to connect to the lateral overflow gate line common to all pixels in the row.

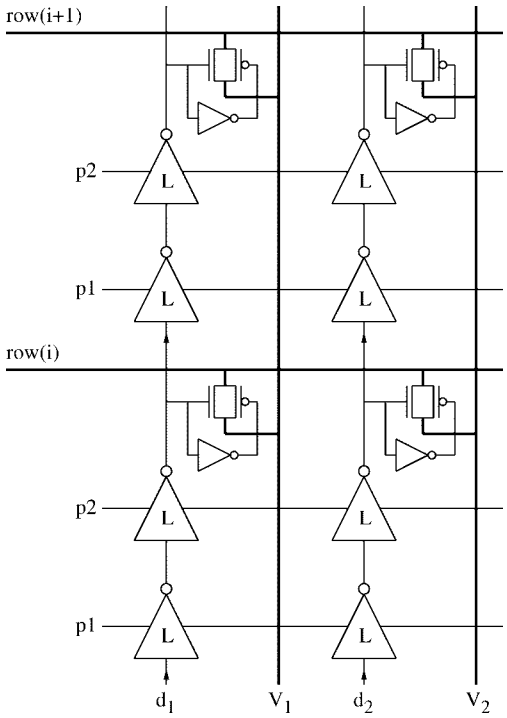


Fig. 7. Barrier waveform generator circuit for two rows. Only two barrier generation shift registers are shown.

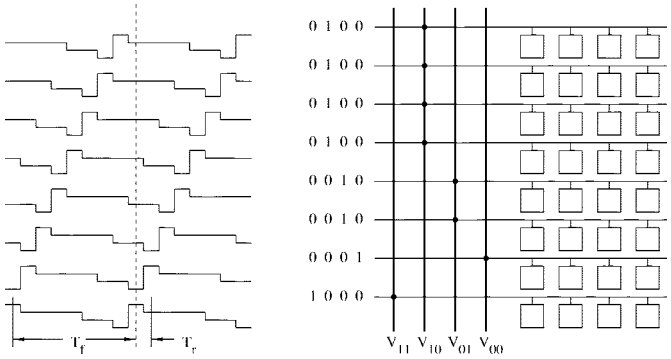


Fig. 8. Staggered readout example for an eight-row, four-step barrier function imager. T_r is the row time and T_f is the frame time. The digital word next to each row specifies which analog level V_{ij} is connected to the barrier in that row.

Fig. 7 shows two bits of the barrier generation shift register for one row. The analog voltages are V_1 and V_2. The two-phase nonoverlapping clock is **p1** and **p2**, which is generated on-chip from an external clock. If d_i is one, row (i) is connected to V_i when **p2** goes high. If d_i is zero, no connection is made between row(i) and V_i. In each row, exactly one of the digital bits d_i will be a one, so the row is connected to exactly one of the analog levels V_i. The bit travels to the output unchanged (since the two inversions cancel), where it is passed on to the next row.

Fig. 8 shows the barrier waveforms for each row and the switch connections at the instant of time indicated by the dashed line. The figure is drawn for an eight-row, four-step barrier function imager, but this example scales to the actual 256-row, eight-step barrier function test chip. Each time the barrier shift register advances, the dashed line moves to the left by the row time T_r. After eight row times, all rows have been read out and the cycle repeats, so for this example, the frame time $T_f = 8T_r$. The actual test chip has 256 rows, so $T_f = 256T_r$. The dynamic range enhancement technique is very flexible since not only the analog voltage levels but also the step timing is user adjustable.

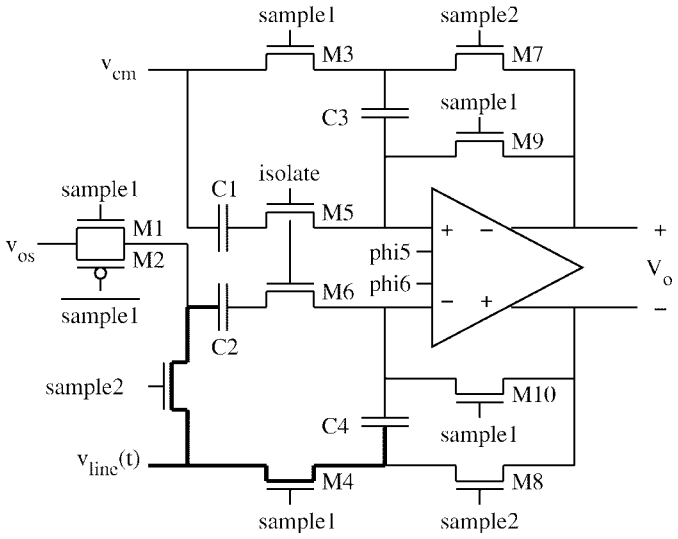


Fig. 9. Complete CDS circuit schematic. Input signal path is shown in bold. On sample phase, signal is passed onto $C4$. On reset phase, signal is passed onto $C2$.

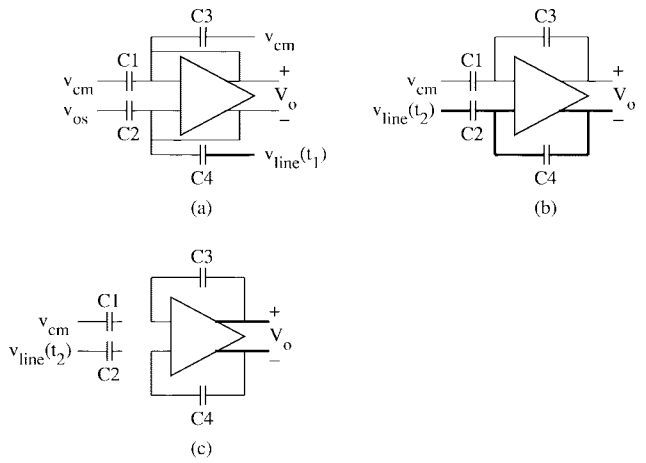


Fig. 10. CDS clocking sequence. The signal path is shown in bold.

B. CDS

Fig. 9 shows a complete schematic diagram of the CDS circuit. The CDS circuit reduces FPN by subtracting the pixel output at the end of the integration period from the pixel output at reset. It also converts the single-ended output from the pixel to a fully differential voltage. When a pixel reaches the end of its integration period, its row select turns on. At the same time, **sample1** goes high. The CDS circuit configuration during this interval is shown in Fig. 10(a). After the column line voltage $v_{\text{line}}(t_1)$ and op-amp output V_o have settled to the required accuracy, **sample1** goes low. Feedback switches

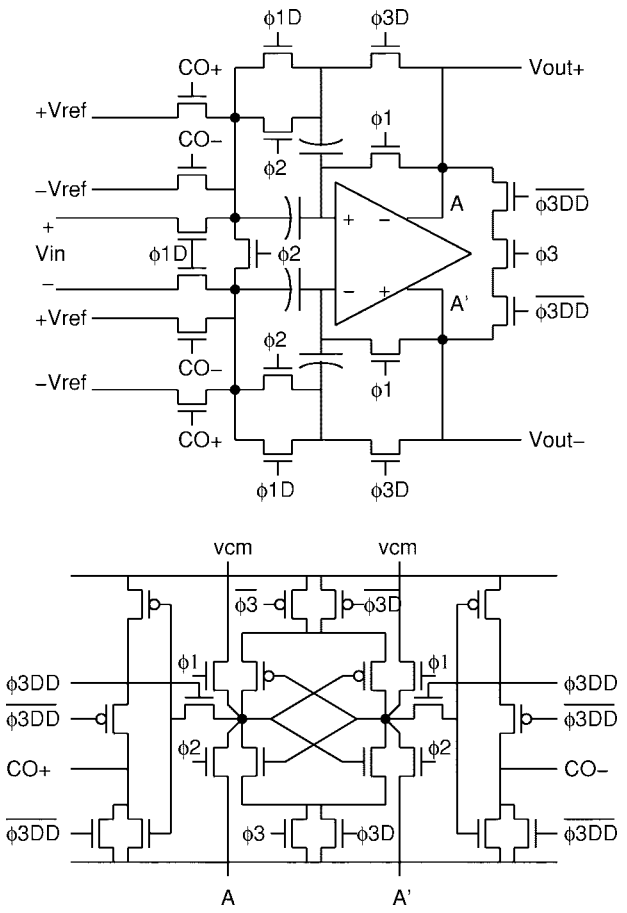


Fig. 11. Schematic diagram for one stage of cyclic ADC.

$M9$ and $M10$ are timed to open slightly before the other switches clocked on **sample1** to avoid voltage-dependent clock feedthrough. Next, **sample2** goes high and **p2** goes high. There is no specific delay required between the falling edge of **sample1** and the rising edge of **sample2**, but the two clocks must not overlap. The rising edge of **p2** advances the barrier generation shift register so that the lateral overflow gate voltage rises to the reset level. The CDS configuration during this period is shown in Fig. 10(b). After the column line voltage $v_{\text{line}}(t_2)$ and the op-amp output have settled, **isolate** goes low, isolating the CDS circuit from any change in potential on the column line. This configuration is shown in Fig. 10(c).

C. Cyclic ADC

Several approaches have been taken to focal-plane data conversion, including sigma–delta, successive approximation, and single-slope architectures [13]–[15]. A cyclic architecture was chosen for this chip as a reasonable approach for 8–10-bit accuracy at several hundred frames per second. The converter is similar to a previous design [16], but with a simplified clocking scheme that does not compensate for capacitor ratio mismatch. The converter has two stages, each of which contains an op-amp, four capacitors, a dynamic latch, and several NMOS switches. A four-phase nonoverlapping clock is used. The schematic diagram for one stage is shown in Fig. 11,

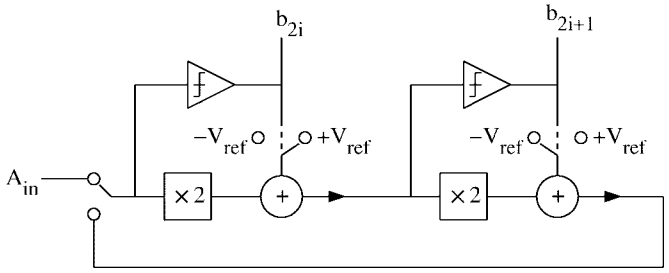


Fig. 12. Cyclic ADC algorithm.

and a block diagram of the algorithm is shown in Fig. 12. At the start of a conversion cycle, the first stage samples the input to the ADC on $\phi 1$. In the second stage, the dynamic latch is activated, producing the least significant bit from the previous sample. Simultaneously, the second stage calculates the residue from this bit. On $\phi 2$, the first stage compares the sampled input to zero. The first-stage op-amp acts as an open-loop preamp for the dynamic latch. As the op-amp outputs diverge, their difference eventually exceeds the dynamic latch offset voltage. During this phase, the second stage is reset by shorting the op-amp outputs together. On $\phi 3$, the first-stage latch is disconnected from the op-amp and activated, producing the most significant bit (MSB). The residue of the first stage is calculated by multiplying the sampled input by two and either adding or subtracting twice the reference voltage, depending on whether the MSB was one or zero. The second stage is sampling the residue produced by the first stage. On $\phi 4$, the first stage is reset by shorting the op-amp outputs together. The second-stage op-amp acts as a preamp for the second-stage dynamic latch. Subsequent clock phases repeat the cycle, except that on $\phi 1$, the first stage samples the residue from the second stage instead of the ADC input. Bits are produced on $\phi 1$ and $\phi 3$, so a 10-b conversion requires five complete clock periods.

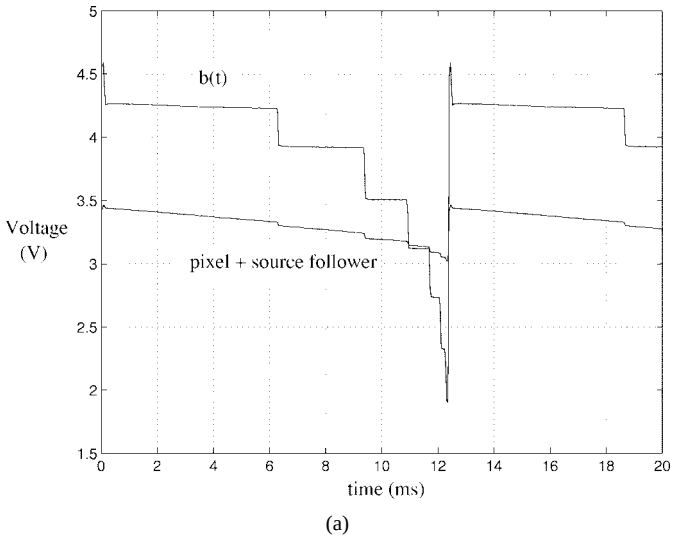
IV. Experimental Results

A. Pixel Response

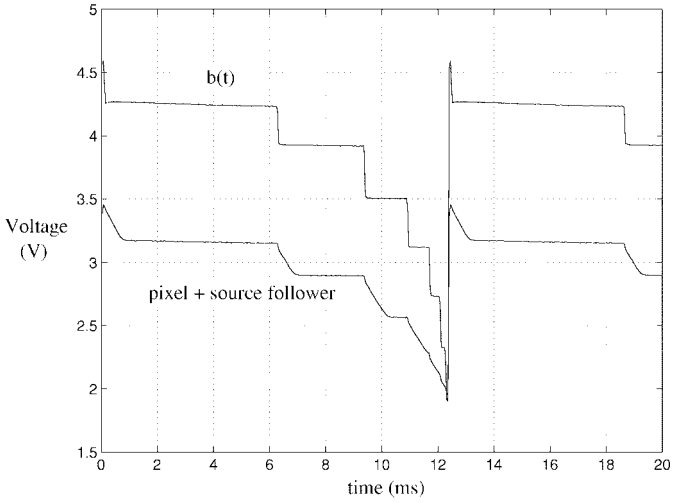
Basic operation of the wide dynamic range pixel was confirmed using an individual test pixel structure. The test pixel is identical to an array pixel but is buffered by a PMOS source follower, which adds approximately 1 V to the output voltage. The pixel output and barrier curve are shown in Fig. 13 for low, medium, and high illumination. The barrier curve and charge integration curve decrease with time since a *reduction* in lateral overflow gate voltage corresponds to an *increase* in barrier height.

B. Responsivity and Conversion Gain

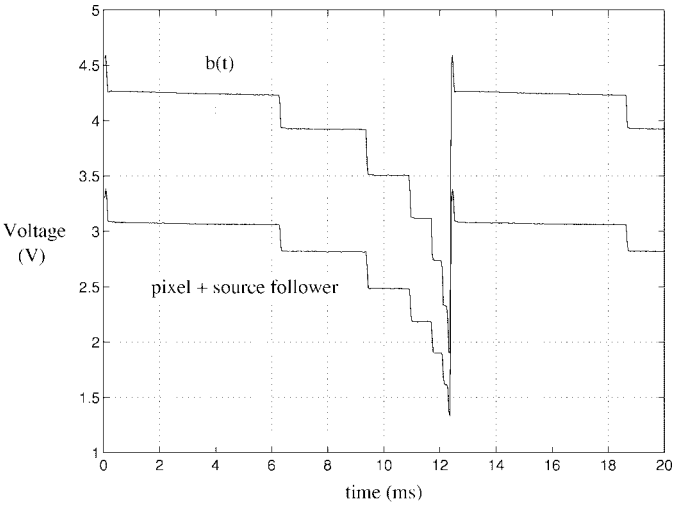
Responsivity and conversion gain were measured using a 10 $\times$ 10 array of test pixels. These pixels are identical to array pixels, except that their sense nodes are connected together and brought to a pin. Responsivity is found by illuminating the test pixel array with monochromatic light. The light power per unit area is measured with a calibrated photodiode, and



(a)



(b)

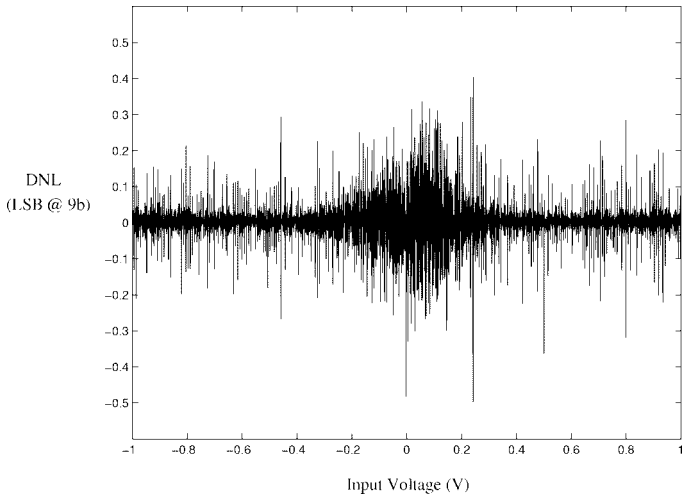


(c)

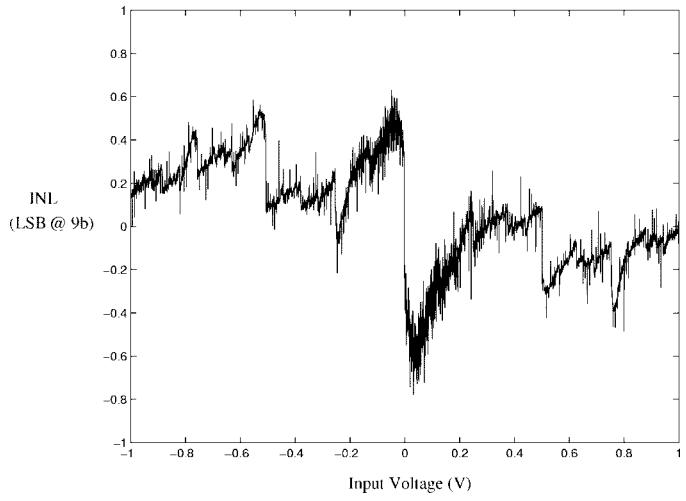
Fig. 13. Pixel output and barrier curve: (a) low illumination, (b) medium illumination, and (c) high illumination.

TABLE II
PERFORMANCE SUMMARY

Process	0.8 μm 5V CMOS single poly, triple metal
Pixel fill factor	49 %
Dark response	174 mV/s
Conversion gain	13.1 μV / e$^-$
Responsivity	16 mA/W @ 450 nm 23 mA/W @ 550 nm 29 mA/W @ 650 nm
Saturation	1.69 V
Power dissipation	52 mW @ 30 fps 400 mW @ 390 fps
optical dynamic range	70 dB (linear mode) 96 dB (compressive mode)
Random noise	0.56 mV (dark, 1σ)
Fixed-pattern noise	0.24% saturation (dark, 1σ)
Max conversion rate	200 KSPS (10 bits)
ADC accuracy, typical	9b



(a)



(b)

Fig. 14. On-chip converter linearity plots: (a) differential nonlinearity and (b) integral nonlinearity.

the total test array current is measured with a picoammeter; the ratio of these quantities is defined as the responsivity. The photodiode and test pixel array were illuminated two ways: through a small aperture and using flood exposure. These

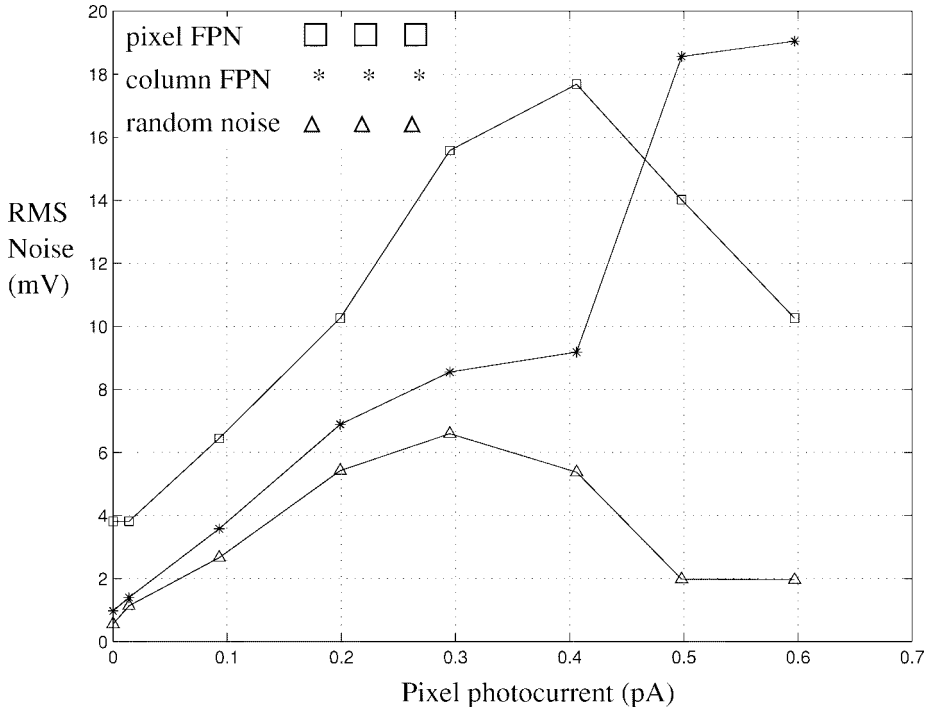


Fig. 15. Measured random and fixed-pattern noise for imager operating in linear mode. One pA is equivalent to 61 lux.

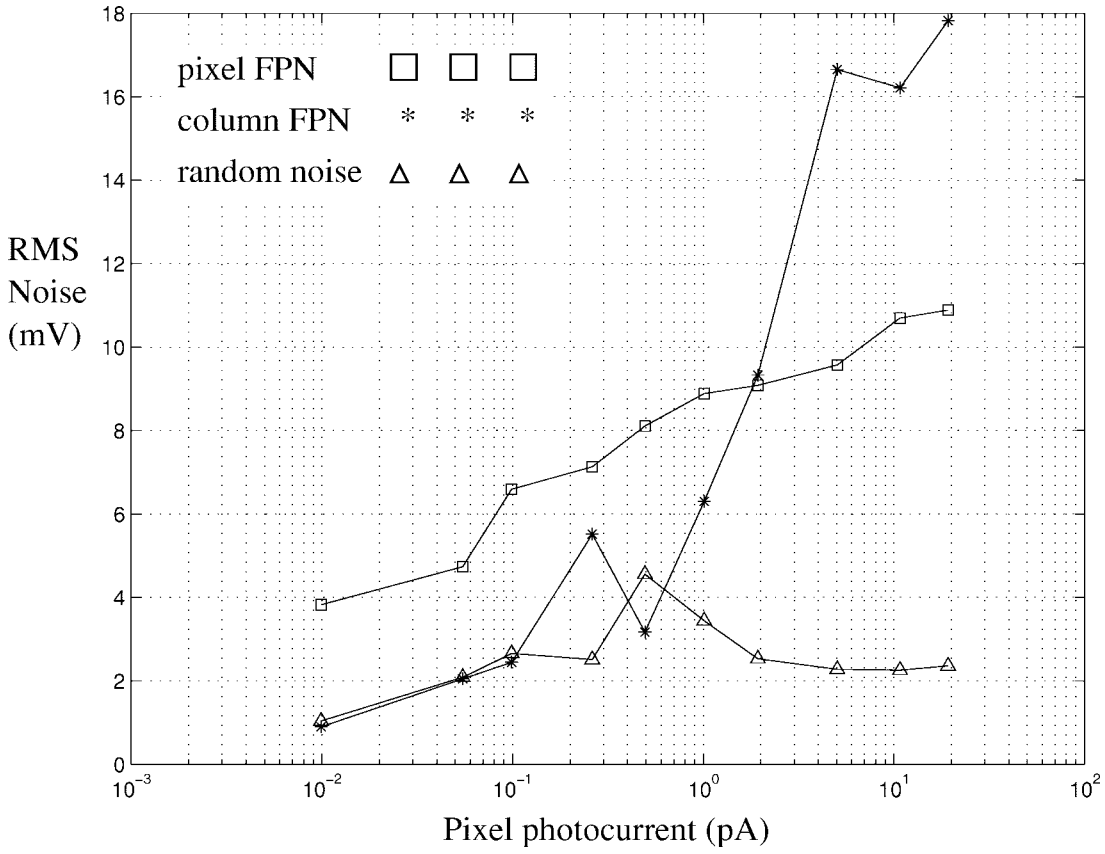


Fig. 16. Measured random and fixed-pattern noise for imager operating in compressive imaging mode. One pA is equivalent to 61 lux.

techniques gave similar results; their averages at 450, 550, and 650 nm are shown in Table II. No infrared cut filter or on-chip color filter was used.

Conversion gain is the change in pixel output voltage divided by the change in integrated charge. Conversion gain is a weak function of bias point, since the quantum efficiency, sense node capacitance, and pixel source follower gain are functions of output voltage. An average value was measured by finding the photocurrent that moves the test pixel output voltage over its output range. This technique produced a conversion gain of 13.1 μV/e$^-$, close to the estimated value of 16.8 μV/e$^-$.

C. ADC

The differential nonlinearity (DNL) and integral nonlinearity (INL) plots for the ADC are shown in Fig. 14. The tested sampling rate is 12.8 kS/s, and the sample is digitized to 12 bits. The DNL and INL indicate 9-b accuracy. The INL plot has a large shift at the major carry point and smaller shifts at the next most significant carry points, characteristic of capacitor mismatch or signal-dependent charge feedthrough. Nonlinearity plots obtained from three chips produced very similar results.

D. Random and Fixed-Pattern Noise

FPN and random noise are determined by uniformly illuminating the pixel array at several different irradiances. At each irradiance, 16 frames are captured. FPN is calculated from the measured data using the following equations:

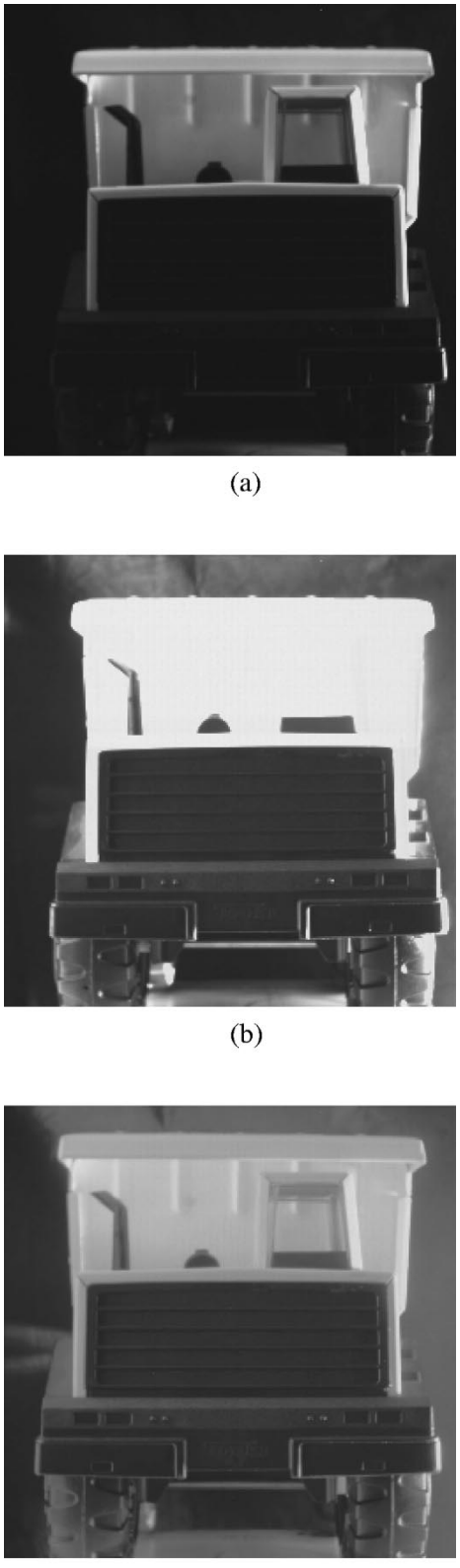
$$\text{FPN (column)} = \sqrt{\frac{\sum_j (\overline{P}_j - \overline{P})^2}{j-1}} \tag{15}$$

$$\text{FPN (pixel)} = \sqrt{\frac{\sum_{i,j} (P_{i,j} - \overline{P}_j)^2}{i \cdot j - 1}}. \tag{16}$$

Random noise is determined by averaging all 16 frames and subtracting that average from each frame. The rms pixel value of the difference frames represents random noise

$$v_{n,rms} = \sqrt{\frac{\sum_f (P_f(i,j) - \overline{P}(i,j))^2}{f-1}}. \tag{17}$$

The FPN and random noise for the linear imaging mode is shown in Fig. 15. Pixel FPN initially rises from its value in the dark due to gain FPN sources but falls when the pixels saturate. This is expected, since sense capacitance and optical aperture do not affect the output voltage when the pixel saturates. Random noise also initially increases from its value in the dark, presumably due to photonic noise. It falls when the pixel saturates, since photonic shot noise goes away, leaving only barrier shot noise.



(a) (b) (c)

Fig. 17. Sample frames from imager: (a) linear imaging mode, low illumination; (b) linear imaging mode, high illumination; and (c) compressive imaging mode, same illumination as (b).

The FPN and random noise for the compressive imaging mode are shown in Fig. 16. These curves depend on the barrier

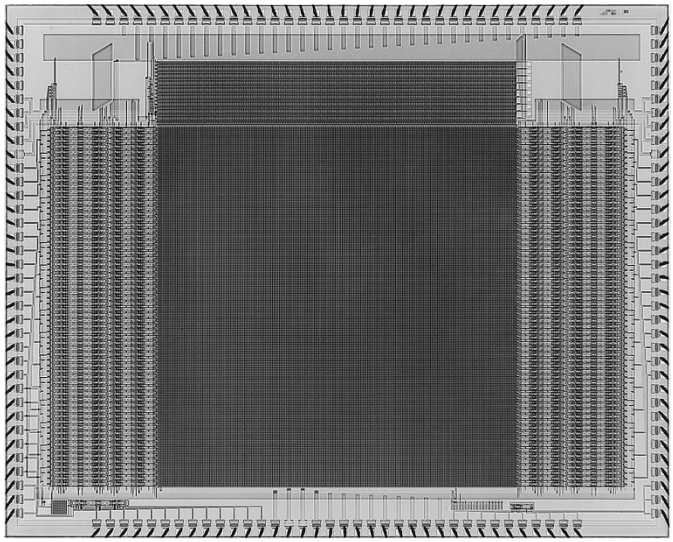


Fig. 18. Die photo of prototype imager.

curve; the lateral overflow gate voltage used here is

$$b(t) = \begin{cases} 4.7V & 0 \le t \le \frac{1}{2}T \\ 4.4V & \frac{1}{2}T \le t \le \frac{3}{4}T \\ 4.1V & \frac{3}{4}T \le t \le \frac{7}{8}T \\ 3.8V & \frac{7}{8}T \le t \le \frac{15}{16}T \\ 3.5V & \frac{15}{16}T \le t \le \frac{31}{32}T \\ 3.2V & \frac{31}{32}T \le t \le \frac{63}{64}T \\ 2.9V & \frac{63}{64}T \le t \le \frac{127}{128}T \\ 5.0V & \frac{127}{128}T \le t \le T. \end{cases} \tag{18}$$

Column FPN approximately follows the shape of the transfer characteristic, implying that column-to-column mismatch is mostly a gain error on the pixel output voltage. FPN and random noise for the linear and compressive imaging modes are the same at the high and low limits.

E. Sample Frames

Fig. 17 shows representative imager output. Fig. 17(a) shows a toy truck imaged using the conventional linear imaging mode. Details of the truck bottom are lost due to the low light level. In Fig. 17(b), the lighting is increased sufficiently to make out details in the lower half, but now the upper half of the truck is saturated. Fig. 17(c) is taken using the same illumination as in (b), but now compressive imaging with approximately 20× increase in dynamic range is used. Details in both halves of the image are clearly visible. Image lag was not characterized.

A die photo of the prototype wide dynamic range imager is shown in Fig. 18.

V. Summary

A technique has been demonstrated for increasing dynamic range in a CMOS imager by a factor of approximately 20. The technique, based on a previously described technique for CCD imagers, requires no additional circuitry in the pixel and therefore no reduction in fill factor. The piecewise-linear compression curve is digitally controlled by the user.

The column-parallel switched-capacitor CDS circuit reduces many forms of offset FPN. Offset FPN sources that are not removed include lateral overflow gate overlap capacitance and dark current mismatch. The CDS amplifier offset voltage is nulled, but mismatch in the CDS capacitors contributes to gain FPN. The switched-capacitor cyclic ADC achieves approximately 9-b accuracy, limited by capacitor matching.

Table II gives measured performance statistics for the prototype imager.

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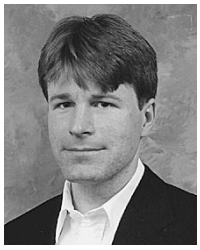

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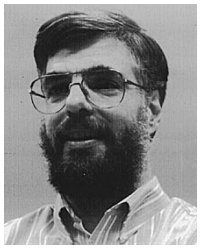

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