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The chip manufacturing industry: Environmental impacts and eco-efficiency analysis

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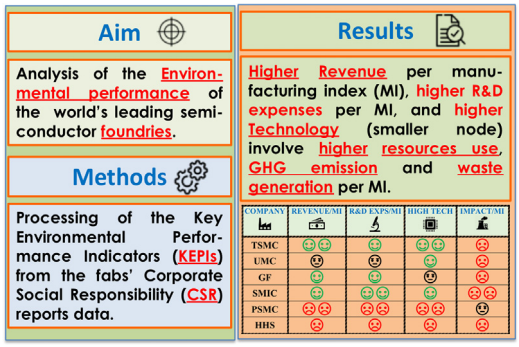
HIGHLIGHTS

- Chip fabrication firms have the most advanced manufacturing processes in the world.
- Chip production is highly input-intensive with huge environmental impact.
- This is the first paper on the eco-performance assessment of the chip sector.
- Higher revenue per wafer produced seems to imply higher resource use.
- Higher R&D expenses seems to imply more GHG emissions and waste generation.

GRAPHICAL ABSTRACT



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ABSTRACT

Semiconductor manufacturing has followed the fate of a large part of industrial production: many companies, around the world, have maintained higher functions (design and engineering) and outsourced other production stages to third-party manufacturers, located mostly in Asia. Some chip companies have thus become "fabless" firms, commissioning the "fabrication" of their product to wafer "foundries" or "fabs". For the first time, in this paper, by calculating and subsequently analyzing various key environmental performance indicators (KEPIs) from the data of the fabs Corporate Social Responsibility (CSR) reports, the environmental impacts and the eco-efficiency of the world's leading semiconductor foundries are analyzed and assessed. The aim is to highlight the relations between company size, technological capacity and environmental impact. A preliminary homogenization was necessary to process the company original data and indicators, often related to different units of production, and to obtain raw data in absolute value. Subsequently, adopting a single common manufacturing index (MI), it was possible to obtain and use new comparable performance indicators and KEPIs. The consequent comparative assessment allowed to give a reliable overall picture of the current resource consumption and pollution of this highly strategic sector, highlighting its next heavy environmental challenges. The result, in fact, is that, differently to what happens in many other sectors, in the semiconductor industry, larger company size (higher revenue), higher value added per wafer produced (higher revenue/MI), and higher technological capacity (higher R&D expenses and smaller technology node) are not always related to lower quantities (per unit of production) of water, energy, waste, wastewater and GHG emissions. It is hoped that, for the future, foundry firms, especially those with the most advanced technologies, will invest much more to optimize their resource use and to further reduce GHGs emissions and waste generation.

1. Introduction

Semiconductors or semiconductor devices are also known as chips, microchips or integrated circuits (ICs). They are not only the beating heart of

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the digital age in which we live but also the key strategic tools of the current and future global geopolitical assets and digital and energy transition policies (US 116th Congress, 2020; US 117th Congress, 2020; European Commission, 2022), being critical components in many different fields (consumer and industrial electronics, telecommunications, automotive, military equipment, etc.).

According to the World Semiconductor Trade Statistics (WSTS, 2022), the global semiconductor market, in 2021, reached a total revenue of over US $ 550 billion, up 26.2 % compared to the previous year; nearly one fifth of this revenue (i.e., US $ 107.5 billion) is attributable to the wafer fabrication sector only (TrendForce, 2022).

Semiconductor manufacturing is one of the most complex, globalized and interlinked industrial supply chains in the world (Varas et al., 2021). It basically consists of three major steps or phases, each of them with high know-how intensity levels (core intellectual property, IP): 1) design; 2) "fabrication"; 3) "assembly, testing and packaging" (ATP). All these three phases can be carried out: a) in-house, by a single company ("integrated device manufacturer" or IDM), as for Intel; although this happens in very few cases now; b) or, as it is much more common, by different agents. In fact, a company ("design-only firm" or "fabless firm"), such as AMD, Qualcomm, Broadcom, Texas Instruments (TI), ST Microelectronics, and so on, could simply design its ICs and outsource some other phases: e.g., the wafer fabrication to a specific facility ("pure play foundry" or "fab"), that usually manufactures designs for others, and the ATP stage to an "outsourced semiconductor assembly and testing (OSAT) firm" (Khan et al., 2021; US DOE, 2022).

1.1. Manufacturing technologies overview

Chip manufacturing requires highly specialized and very expensive plants, based on advanced processes, equipment and tools.

Below, the fabrication phases and the most used technologies (among the myriads of those possible and/or in the testing phase) are briefly described, starting from polycrystalline EG (electronic grade) silicon (or gallium arsenide, germanium, gallium nitride, aluminum oxide, etc.) to get the final device (Liu, 2021). From EG silicon, cylindrical ingots (boules) of monocrystalline silicon, in an extremely pure form and of various diameters, are obtained by float zone (FZ) or Czochralski (CZ) methods (Anttila, 2020). The ingots are then sectioned into wafers of different thickness and subjected to a preliminary planarization (Kao and Chung, 2021). The subsequent processes are substantially the following macro-phases: doping, thin-film deposition, removal process, and lithography; not necessarily according to this sequence (Adak, 2021). During the doping step, dopant atoms are introduced into semiconductors by ion implantation, gas-source doping, solid-source doping, and drive-in diffusion (Duffy et al., 2020). By deposition, material is transferred on the wafer surface. It can take place by various techniques of different complexity depending on the wafer features; those most commonly used are the following: physical vapor deposition (PVD), chemical vapor deposition (CVD), electrochemical deposition (ECD), molecular beam epitaxy (MBE), and atomic layer deposition (ALD) (Wang et al., 2016; Devaray et al., 2022). By various lithographic techniques (e.g., optical or UV lithography or photolithography, extreme ultraviolet lithography or EUVL, wet lithography, electron-beam lithography, nanoimprint) (Singh et al., 2017; Saifullah et al., 2022), an ionic beam or UV radiation selectively remove parts of the wafer, previously coated with a chemical substance (photoresist), using quartz photoplates (photomasks), containing the patterns to be produced, and specific equipment (stepper or mask-aligner) (Lee, 2021; Fang and He, 2022). During deposition and lithography, removal processes (wet or dry etching), collectively or selectively, subtract material from the wafer surface by plasma corrosion techniques (e.g., RIE, reactive-ion etching), chemical substances (hydrofluoric acid or other developer solutions) or chemical-mechanical planarization (CMP) (Shen et al., 2018; Huff, 2021). The remaining photoresist is removed in another step (resist strip process) by solvents, oxygen plasma etching or UV-ozone ashing (Kohli, 2019). Each of these fabrication steps involves high environmental impact related to the use of huge quantities of ultrapure water (UPW), energy, and hazardous substances, and to pollutants emissions and waste generation.

After the fabrication processes, each ICs gets tested to verify its correct operation (ATP phase). ATP processes are many and very different from each other, depending on the packaging type and material, wafer type and material and packaging technology. They are characterized by constant and fast innovations and labor-intensive phases, carried out by many companies, some of which are also very small because ATP segment has the lowest entry barriers (Andrae and Andersen, 2011; Khan et al., 2021). For these reasons, it is not possible to investigate the environmental impacts of the companies of ATP sector.

1.2. Background, aim and scope

As stated above, wafer fabrication step is one of the most profitable phases of the entire semiconductor value chain. It has also the manufacturing phase with the highest environmental impact, since it involves the use of huge quantities of raw material, water, energy, and the generation of waste and emissions. For the first time, in this paper, by the calculation and subsequent comparative analysis of the processed Key Environmental Performance Indicators (KEPIs), the environmental impacts and eco-efficiency of the world's leading semiconductor "foundries" or "fabs" (i.e., of those firms that deal exclusively with the fabrication phase, turning raw silicon into ICs) are analyzed and assessed.

Semiconductor production is moving, more and more, towards the centralization of production to achieve important and vital economies of scale which, in turn, require very high investments in plants, equipment and R&D. Over the past few years, the required technology (in particular, that related to semiconductor manufacturing equipment, SME) has become increasingly advanced and the correlated investments increasingly higher (many billions of US $ per plant) (McKinsey & Co., 2020). Due to this huge amount of money, many foundries were no longer able to invest in R&D and went out of business; in addition, there were difficulties, for some big brands (AMD, Qualcomm, TI, etc.), to re-shoring many steps of their production (Kamakura, 2022). Therefore, there has been a progressive, strong concentration, in particular, of the fabrication step in the hands of few foundries (SIA, 2021), of which only one is the absolute dominant: the Taiwanese Semiconductor Manufacturing Company (TSMC), which holds, in 2021, over 50 % of the global foundry revenue (TrendForce, 2022).

About that, fabrication firms that, in 2021, recorded the largest market shares of the global foundry revenue (equal to US $ 107.5 billion) were the following: TSMC Ltd. (53 % revenue share), Samsung Semiconductor Global (18 % share), United Microelectronic Corporation (UMC, 7 % share), GlobalFoundries (GF) Inc. (6 % share), Semiconductor Manufacturing International Co. (SMIC, 5 % share), Hua Hong Semiconductor Ltd. (HHS Group, 2 % share), and Powerchip Semiconductor Manufacturing Corp (PSMC, 2 % share).

By going to back, along the semiconductor global supply chain and adopting a Life Cycle Assessment (LCA) approach, the contribution, to the overall environmental impact, of the equipment suppliers should also be assessed. The world market of this other sector is currently dominated – especially for the latest generation semiconductors, which manufacturing requires the most advanced technologies, e.g., EUVL and micro-diffraction-based focus (mDBF) equipment (Lakcher et al., 2020) – by the Dutch company ASML (Advanced Semiconductor Materials Lithography) Holding N.V., founded in 1984 by a joint-venture between Philips and ASMI (Advanced Semiconductor Materials International). ASML has become a colossal multinational corporate in few years: in 2021, it has achieved a revenue of 18.6 billion euros with almost 30,000 employees (Boerse Group AG, 2022); it claims to hold between 80 % and 85 % of the total market share of semiconductor manufacturing equipment and 100 % of the EUVL systems' world supply (ASML, 2022). However, this research will not analyze the environmental performance of ASML, which belonging to a different industrial segment, has very different processes and output, not comparable with those of the foundries. Furthermore, to date, excluding the recent restrictions imposed by the US on its sales to China, ASML sells its advanced equipment

indifferently to all foundries, and, therefore, its contribution is not an influencing factor to be investigated for the fabs' environmental analysis and assessment.

Over the years, some researchers have analyzed the applicability of LCA to this particular industry. LCA is a powerful method to give a global vision of the impacts generated by products and would be very useful also for this sector, but if it were easily applicable to this context. Krishnan et al. (2004) were the first who developed a schematic model of a bottom-up LCA approach for semiconductor production, recognizing the related limits and difficulties of this implementation. Other authors (Huang et al., 2012) set alternative methodologies to reduce time and costs of a traditional LCA for the calculation of the carbon footprint of these products (CFPs), identifying and isolating specific key process factors. In this context, a valuable and extensive contribution, concerning the characterization and quantification of the environmental impacts of semiconductor industry, was provided by Boyd (2012), who described different analytical techniques useful for applying LCA methodology to different types of semiconductors: complementary metal-oxide semiconductor (CMOS), flash memory, and dynamic random-access memory (DRAM).

By the survey of the available literature, it was found that there were very few scientific case studies and researches about the assessment of the environmental impacts of semiconductor industry, investigating in particular one or more phases of wafer fabrication, namely: Ahmad, 2007; Higgs et al., 2009; Liu et al., 2010, Boyd et al., 2010; Wang, 2014; Huang et al., 2016; Kuo et al., 2022.

The common limit of these studies, deeply analyzed in the discussion section of this paper, was their restricted research scope: the related authors, in fact, dealt only with the impact assessment of single fabrication processes or production phases. So far, no study has focused on the overall impacts of this sector or, at least, of a whole company. And this, for many reasons, mainly: technological and trade secrets, hard availability of reliable data for LCA, intrinsic complexity of the industrial sector, complexity and variability of the related production technologies and methods, very fast innovations, different feature of the products and different manufacturing technologies (Kuo et al., 2022). For the same reasons, for scholars, it is not easy identifying and setting sector standards as reference to compare environmental performance and impacts of different companies, plants or processes (Mullen and Morris, 2021; Kuo et al., 2022).

To fill this research gap, the author of this paper aims to give his contribution for an overview of the environmental impacts and eco-efficiency of this complex and high-risk industry by investigating, among other things, the connections between the size of a company (revenue, production), its technological capacity (process technology node, R&D annual expenses) and its environmental impacts, (water use and energy consumption, pollutants emissions and waste generation).

The subject analyzed by this paper is extremely topical, considering that this sector is assuming worldwide an increasing political and economic prominence. Indirect examples of its global strategic importance are the recent crisis about the availability of microprocessors (“chip crunch”) and the political disputes between China and Taiwan, mainly founded on the worldwide role assumed by the latter country in the production of semiconductor devices.

2. Materials and methods

This study was focused on the calculation and subsequent analysis of the environmental data and indicators of the Corporate Social Responsibility (CSR) reports of the foundries only, i.e., excluding the IDM companies, the fabless firms and the OSAT companies; this to avoid the risk of invalidating the consequent comparative analysis taking into account substantially different manufacturing processes and environmental impacts. In fact, at the moment, it is not possible, analyzing the respective CSR reports or other available official documents, to identify and isolate data of resource consumption, waste generation and pollutant emissions of the portion of IDM production process concerning the chip fabrication step only. This exclusion, however, does not invalidate this study, because, as stated, it concerns the analysis and assessment comparison of the performances of the foundries only.

The preliminary data collection and processing, basically, consisted of the following alternative operations: or 1) collection of a series of KEPIs for common items, both identifying them in the CSR reports and reporting them as they are, if available in an appropriate format (for example, in the case of UMC); or 2) KEPIs calculation starting from data available in absolute value (e.g., for TSMC); or, as more often it happened, 3) conversion of the KEPIs already available in the foundries reports by suitable factors. These preliminary steps were fundamental to normalize, homogenize and, subsequently, compare the environmental performance data of the various companies.

Data sources were, almost exclusively, unless otherwise indicated (e.g., in some cases, the information was found into the same companies' websites), the company CSR reports and, precisely, the specific part of each report reserved to the environmental, social and governance (ESG) Performance Summary section, if present, or into other non-specific sections of the same reports.

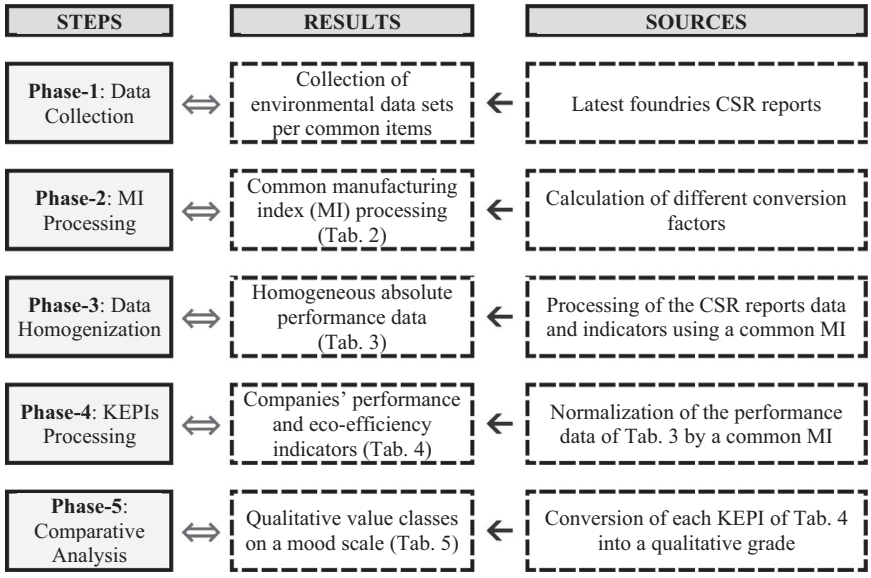
In order to make the logic and the contents of this study clearer to the readers' understanding, it was considered appropriate giving an overview of the research framework of this paper. The related research activities were subdivided into several procedural steps, namely: Phase-1 (Data collection); Phase-2 (MI processing); Phase-3 (Data homogenization); Phase-4 (KEPIs processing); Phase-5 (Comparative analysis). By each of these phases, it was obtained an output which was used as input for the immediately following phase. For shortness and more intelligibility, it was also considered suitable the following summary table:

The data of CRS reports, about the company output and environmental impacts, were the basis for the processing of the eco-efficiency key-indicators, that, subsequently, allowed to compare different company performance situations. The choice of these indicators, referred to a common production unit (i.e., manufacturing index, MI), was obviously in part conditioned by the data availability in the CSR reports. A selection was made to choose only those items and data that were available in all the examined company reports. For these reasons, the items considered and used for the subsequent calculation of KEPIs and for the eco-efficiency analysis, were the following: a) revenue; b) R&D expenses; c) production; d) GHG scope 1 emissions; e) GHG scope 2 emissions; f) fluorinated or F- GHG emissions; g) energy consumption; h) water withdrawal; i) wastewater discharge; l) general waste generated; m) hazardous waste generated.It was necessary to overcome some difficulties to obtain the necessary data for this analysis, because not all the foundry KEPIs are available in a standard common format. For example, many companies did not disclose their annual production (e.g., in terms of number of wafers produced or total area of wafers); besides, the analyzed firms used different manufacturing parameters (i.e., units of production) to normalize their performance data (Table 1). In this way, an immediate comparative assessment was not possible. For these reasons, a preliminary data homogenization was necessary to do.

Due to the above, and for the purpose to obtain comparable KEPIs, starting from the data and indicators available in the CSR reports, it was chosen to adopt a common divider or industry standard: i.e., a unique MI, equivalent to the total area of the wafers annually produced (wafer-m^2 or wfr-m^2) by a specific foundry, taking into account the number of wafers annually manufactured and the number of masking steps or layers required to wafer fabrication (AMD, 2022). This MI is directly related to the complexity of production process and to the quantities of inputs (raw material, energy), waste and to production costs. In fact, MI and the technological complexity of the wafer fabrication processes are mainly a function of the wafer size (maximum diameter that can be processed), process technology node (or technology node, or process node or process feature size) and the number of wafer mask layers, proportional to the number of steps required to produce a wafer (Den et al., 2018).

The calculation of this MI – then, as common production unit to which referring the various economic and environmental performances of the analyzed foundries – was a fundamental step in order to proceed to the subsequent phase of inter-company comparison of the various performance

Table 1
Research framework.



indicators. In fact, within the CSR reports, numerical data, in absolute value, of economic and environmental aspects were rarely available: indeed, there were, almost always, data normalized to different production units (i.e., different MI), as reported in Table 2. This would have made impossible an immediate performance comparison between different companies. For the calculation of a common MI, it was considered that a wafer has, on average, e.g. 45 Mo—Si mask layers (Semiconductor Engineering, 2022) and that a round wafer size of 11.8 in. (usually referred as 12") and another of 7.9 inch (usually referred as 8") have, respectively, a diameter of 300 mm (and then, an area of 0.070686 m^2) and 200 mm (and then, an area of 0.031416 m^2). For example, in the case of TSMC, to transform its MI (i.e., 12-inch wfr-layer), it was necessary to multiply it by the following conversion factor (as indicated in Table 2): 0.0015708 (wfr-m^2). This adjusted MI was obtained dividing the wafer area (0.070686 m^2) by the average number (45) of the mask-layers of each wafer. In any case, in Table 2, the conversion factors of all the companies and, in the related legend, the calculation procedure, used to obtain them, are shown.For the final assessment of performance comparison between the examined companies, it was considered useful to summarize the different data and indicators in a graphical framework (Table 5), following the subsequent steps and assumptions: 1) the indicators considered for this purpose were: a) Smallest technology node, b) Revenue per unit of production (Revenue/MI), c) Scope 1&2 GHG emissions intensity (1&2-GHG/MI), d) F-GHG emissions intensity (F-GHG/MI), e) Energy intensity (Energy/MI), f) Water withdrawn per MI (Water/MI), g) Wastewater discharge per MI (Wastewater/MI); h) Waste generated for MI (Waste/MI), i) Hazardous waste for MI (H-waste/MI); 2) the highest value of each indicator of the above items was set equal to 1 (e.g., in Table 4, the TSMC value of 48,970 was considered equivalent to 1); 3) the other values of the same indicator of the remaining companies were compared to this highest value (e.g., for UMC, 26,510/48,970 = 0.54); 4) for each of these new derived indicators (e.g., the above 0.54), thus calculated, a value judgment was indicated using the following classes (on a scale ranging from 0 to 1): 0 ÷ 0.20: "Very Good" (VG); 0.21 ÷ 0.40: "Good" (G); 0.41 ÷ 0.60: "Neutral" (N); 0.61 ÷ 0.80: "Bad" (B); 0.81 ÷ 1.00: "Very Bad" (VB) (Table 5); 5) then, since this is a scale with different efficiency grades, it implies that, with the exception of Revenue/MI only, a

Table 2
World major wafer production companies (2020).
Sources: Information and elaboration of data of Trendforce (2022), TSMC (2020), UMC (2020), GF (2021), SMIC (2020), PSMC (2020), HHS (2020).

Company	Headquarters (*a*)	Fabs in operation (country codes) (*b*)	Wafer size (*c*)	Smallest technology node (*d*)	Manufacturing Indexes (MIs) (*e*)	MI Conversion factor° to wfr-m^2(*f*)
TSMC	Hsinchu (TW)	TW (10 fabs), CN (2 fabs), US (1 fab) and SG (1 fab)	150 mm (1 fab), 200 mm (7 fabs), 300 mm (6 fabs)	5 nm	12-inch equivalent wafer mask layer	0.0015708[a]
Samsung Semiconductor Global	Suwon (KOR)	KOR (4 fabs), CN (1 fab) and US (1 fab)	200 mm (1 fab), 300 mm (5 fabs)	7 nm	N/A	–
UMC	Hsinchu (TW)	TW (8 fabs), CN (2 fabs), JP (1 fab), SG (1 fab)	150 mm (1 fab), 200 mm (7 fabs), 300 mm (4 fabs)	14 nm	wafer-m^2 (wfr-m^2)	1
GF	Malta (US)	SG (4 fabs), DE (3 fabs), US (3 fabs)	200 mm (4 fabs), 300 mm (6 fabs)	12 nm	*12-inch equivalent wafer mask layer	0.0015708[a]
SMIC	Shanghai (CN)	CN (9 fabs)	200 mm (3 fabs), 300 mm (6 fabs)	8 nm	8-inch equivalent wafer mask layer	0.0006981333[b]
PSMC	Hsinchu (TW)	TW (3 fabs)	300 mm (3 fabs)	22 nm	wafer-cm^2 (wfr-cm^2)	0.0001[c]
HHS	Shanghai (CN)	CN (2 fabs)	300 mm (2 fabs)	14 nm	8-inch wafer	0.031416[d]

° from (e) to a common MI (wfr-m^2).
[a] (0.070686 m^2) / (45 mask-layers) = 0.0015708 (wfr-m^2).
[b] (0.031416 m^2) / 45 (mask layers) = 0.0006981333 (wfr-m^2).
[c] (1 m^2) • (10^{-3} cm^2) = 0.0001 (wfr-m^2).
[d] (31,416 mm^2) • (10^{-6} m^2) = 0.031416 (wfr-m^2).
* arbitrary.

Table 3
World major wafer foundries performance data (2020).
Sources: Elaboration of data of TSMC (2020), UMC (2020), GF (2021), SMIC (2020), PSMC (2020), HHS (2020).

	TSMC	UMC	GF	SMIC	PSMC	HHS	Total
a) Revenue (Million USD)	45,969	5959	5959	4256	851	851	63,859
b) R&D Investments (Million USD)	3464	438	477	677	104	108	5268
c) Production - Wafer-m^2 (in 000)	938.7	224.8	194.6	123.9	122.7	64.2	1669
d) GHG Emissions - Scope 1 (000 tCO_2e)	2450.3	717.0	423.5	550.1	107.9	18.1	4267
e) GHG Emissions - Scope 2 (000 tCO_2e)	7460.2	1852.4	214.8	1579.2	565.1	430.5	12,102
f) GHG Emissions - Scope 1&2 (000 tCO_2e)	9910.5	2569.4	638.3	2129.3	673.0	448.6	16,369
g) F-GHG Emissions (000 tCO_2e)	1311.5	461.4	318.0	416.9	459.5	223.6	3191
h) Total Energy Consumption[a] (GWh)	16,919.1	3761.6	3215.0	1775.1	1265.9	831.1	27,768
i) Water Withdrawal (000 t)	129,110	22,748	27,258	26,629	6114	15,938	227,797
l) Wastewater Discharge (000 t)	51,810	4308	23,786	13,170	4013	6030	103,117
m) General Waste Generated (t)	277,340	25,107	20,401	33,878	10,934	6143	373,803
n) Hazardous Waste Generated (t)	298,400	31,634	41,503	28,706	6247	9262	415,752
o) Total Waste Generated (t)	575,740	56,741	61,904	62,584	17,181	15,405	789,555

[a] Electricity and natural gas.

high value of a specific indicator means a low company performance (e.g., low technological capacity, low efficiency in resource use and high environmental impact); 6) the above scale was the basis of the Graphical Abstract, converting the value of each class into a suitable pictogram (mood scale); 7) the overall average value for each fab was entered in the last row of Table 5 and converted, also in this case, into an unitary format setting the highest value (89) equal to 1, thus giving an immediate idea of the overall environmental impact of each company.

It would have been of undoubted importance and usefulness to differentiate the productions of the various companies by type of chip and/or specific technological process; in fact, if that were possible, this would have helped to make a more accurate analysis. However, this was impossible for the following reasons: a) currently, data and information sources of such high detail (i.e., differentiated by type of chip and/or by type of technology) are not made available by the analyzed foundries, probably for reasons of trade secrets and know-how protection; b) chip features, and the related production technology, of the analyzed manufacturers are many and very different: as it can be seen in Table 2, in which it was specified, for example, that the same company produces wafers of different sizes (from 150 to 300 mm); a wafer size is related to a particular type of process (in fact, for this reason, plants are located in different territories on the basis of wafer size and feature) and, obviously, to different environmental impacts; unfortunately, this information is not available for the public: in fact, e.g., the environmental data and the KEPIs of the CSR reports concern the entire organization and are not differentiated on the basis of each particular process; c) moreover, due to lack of data, it is impossible to relate the environmental performance, on the basis of each process node, because each company had different nodes output: e.g., in 2021, TSMC has produced chips at 350, 250, 220, 180, 160, 150, 28, 20, 16, 5, 3 nm; UMC at 4000, 1000, 500, 350, 250, 180, 150, 130, 110, 90, 55, 40, 28, 14 nm; GF at 600, 350, 180, 110, 90, 65, 45, 40, 28, 22, 14, 12 nm; SMIC at 350, 180, 90, 55, 45, 40, 32, 28, 14, 12, 8 nm; PSMC at 90, 70, 22 nm; and HHS at 65, 55, 28, 22, 14 nm.

3. Results

In Table 2, summary information of the analyzed companies was reported: headquarters, fabs in operation, wafer size, smallest technology node (or process transistor gate length, i.e., the size of the nanometric features that can be etched onto the wafers) and the different MIs, used by the companies to normalize the data of their own several environmental performances declared in their respective environmental reports. In the same table, the conversion factors of the different MIs for the examined companies are also indicated.

The 2020 data of all the companies listed above were used, with the exception of Samsung Group because, from the annual Samsung Electronics Sustainability reports, it was not possible to find the performance information about its Semiconductor Division alone.After the calculation of data and indicators of all the analyzed companies (TSMC, UMC, GF, SMIC, PSMC and HHS), Table 3 was obtained, in which the raw data of each company have been indicated for each single item, as stated above.

By the consequent processing of the data contained in the above table, eco-efficiency indicators (KEPIs) were obtained. The most significant related results of these operations are shown in Table 4 and in the related figures below. Table 4, in which the performance indicators and KEPIs of the six companies are shown, was later used as reference basis for the final comparative analysis.

TSMC, SMIC, GF and UMC, having the highest technological capacity (high R&D expenses per MI and smaller technology node) (Table 4), are also the foundries with the highest unitary values of revenue (Fig. 1).

Semiconductor fabrication involves, as it can be seen from Table 4, the production of a considerable amount of GHG emissions (estimated

Table 4
Company performance and eco-efficiency indicators (KEPIs) (2020).
Sources: Elaboration of data of TSMC (2020), UMC (2020), GF (2021), SMIC (2020), PSMC (2020), HHS (2020).

	TSMC	UMC	GF	SMIC	PSMC	HHS	Total
a) Revenue/MI (USD/wfr-m^2)	48,970	26,510	30,622	34,350	6936	13,255	38,261
b) R&D Investments/MI (USD/wfr-m^2)	3690	1948	2451	5464	848	1682	3156
c) GHG_1/MI (kg CO_2e/wfr-m^2)	2610	3190	2176	4440	879	282	2557
d) GHG_2/MI (kg CO_2e/wfr-m^2)	7947	8241	1104	12,746	4606	6706	7252
e) $GHG_{1\&2}$/MI (kg CO_2e/wfr-m^2)	10,558	11,431	3280	17,186	5485	6988	9808
f) F-GHG/MI (kg CO_2e/wfr-m^2)	1397	2053	1634	3365	3745	3483	1912
g) Energy Intensity (MWh/wfr-m^2)	18.024	16.734	16.521	14.327	10.317	12.945	16.638
h) Energy Efficiency (MWh/Million USD)	368.1	631.2	539.5	417.1	1487.5	976.6	434.9
i) Water Withdrawal/MI (tons/wfr-m^2)	137.5	101.2	140.1	214.9	49.8	248.3	136.5
l) Wastewater Discharge/MI (tons/wfr-m^2)	55.2	19.2	122.2	106.3	32.7	93.9	61.8
m) General Waste Generated (kg/wfr-m^2)	295	112	105	273	89	96	224
n) Hazardous Waste Generated (kg/wfr-m^2)	318	141	213	232	51	144	249
o) Total Waste Generated (kg/wfr-m^2)	613	252	318	505	140	240	473

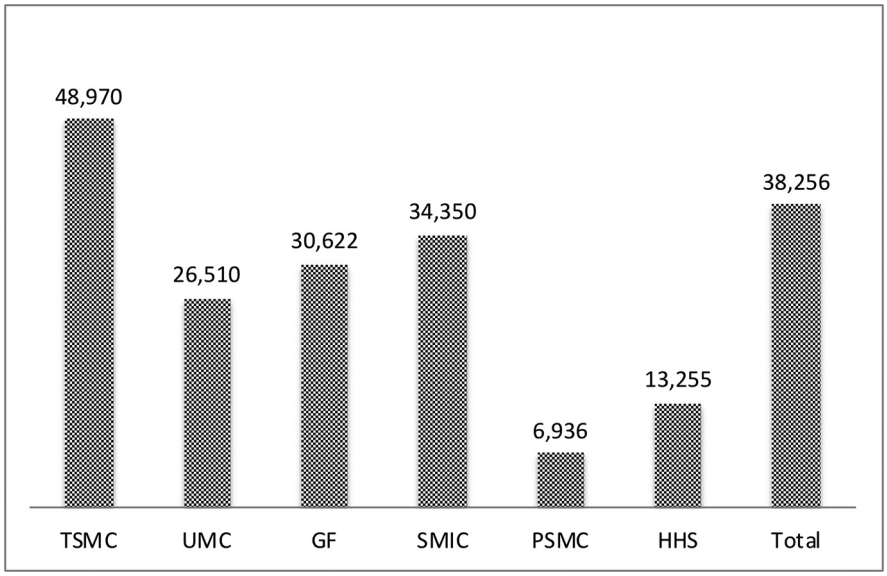


Fig. 1. Revenue per Unit of Production (USD/wfr-m^2).

according to the GHG Protocol and the ISO 14064-1 Standard). Only two companies (TSMC and UMC) disclose the data of their own GHG Scope 3 emissions; for this reason, it was decided to exclude them from this study.

Indirect emissions (Scope 2), generally, are much higher than direct emissions (Scope 1), related, as it is known, to the activities controlled by an organization. Between them, the corresponding emission average ratio is approximately 3:1 (Table 4). There are cases, however, in which this ratio has very higher values (e.g., almost 24:1 for HHS); this probably occurs when most of the production processes are carried out by third parties.

The GHG emission (Scope 1 and Scope 2) intensity is, on average, 9800 kg CO_2e/wfr-m^2 (Fig. 2). Those foundries, that significantly have values below this average (GF, PSMC and HHS), probably use more renewable energy sources (like photovoltaic one) or outsource some upstream and downstream phases of their wafer manufacturing. Obviously, the complexity of wafer architecture affects production costs, energy consumption and the related GHG emissions; TSMC, UMC and SMIC are examples of this situation.

Huge quantities of different fluorinated compounds (i.e., CH_3F, CHF_3, CH_2F_2, CF_4, C_2F_6, C_3F_8, NF_3, SF_6, etc.) with high Global Warming Potential (GWP) are used by the semiconductor fabs to print circuits on wafers, to clean the CVD chambers and as fluorinated heat transfer fluids (FHTFs) (US EPA, 2018; IPCC, 2022). The highest quantities of F-GHG emissions per unit of production are related to the processes of PSMC (3.75 t CO_2e/wfr-m^2), HHS (3.48 t CO_2e/wfr-m^2) and SMIC (3.37 t CO_2e/wfr-m^2) (Fig. 3). The company with the most advanced recovery systems of these gases, directly in the chambers of production tools is TSMC (1397 kg CO_2e/wfr-m^2) (TSMC, 2020).

Energy, in the semiconductor industry, almost entirely as electricity, is mainly used to power production equipment and tools and to constantly guarantee the high critical cleanroom standards (PG&E, 2011). The highest overall energy intensity values per unit of production (Fig. 4) are related to the fabrication processes of those firms having the highest production volumes and the best energy efficiency performances compared to the revenue (Tabb. 3 and 4): TSMC (18.02 MWh/wfr-m^2), UMC (16.73 MWh/wfr-m^2), GF (16.52 MWh/wfr-m^2), and SMIC (14.33 MWh/wfr-m^2).

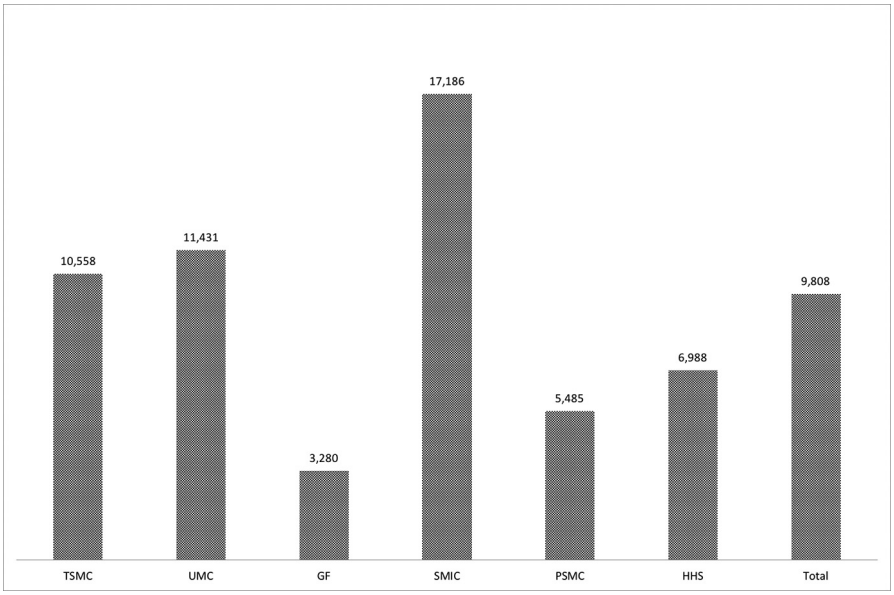


Fig. 2. GHG Emission Intensity - Scope 1&2 (kg CO_2e/wfr-m^2).

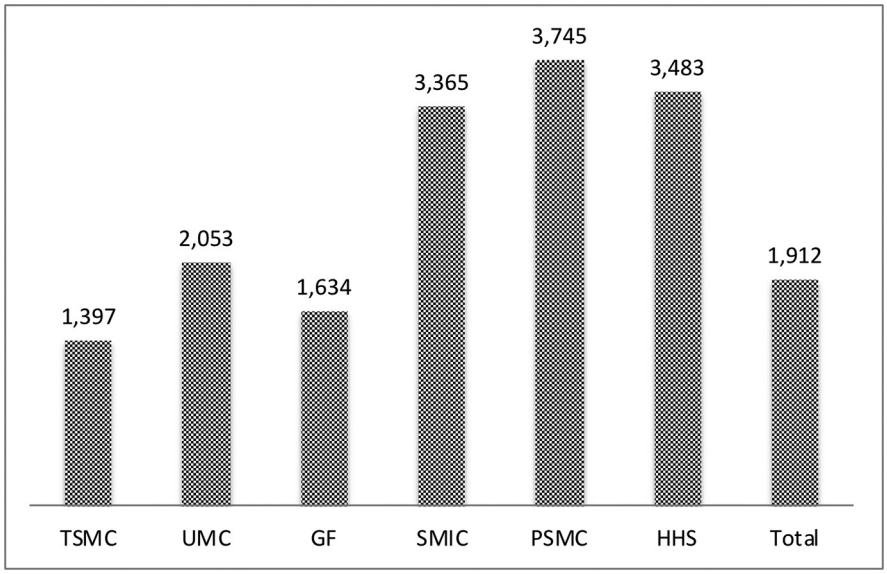


Fig. 3. F-GHG Emission Intensity (kg CO_2e/wfr-m^2).

The component of electricity and energy consumption from non-renewable sources – in all production cycles that are responsible for direct and indirect GHG emissions, as it is also in this one – must be considered to have a double burden for the overall environmental impact of a company: in fact, in addition to the impact on the environment due to the consumption of energy from fossil sources (i.e., depletion of natural resources), it also correspondingly causes another type of impact, related to the generation of GHG (Scope 1, 2, 3) and other pollutants emissions by own or others' combustion processes.

Many thousands of tons of ultrapure water (UPW) are also required for the production of a single square meter of wafer. UPW, which must be absolutely free of dissolved particles, ions and gases, is used in the wafer cleaning processes. Smaller and more complex wafers require more UPW. Generally, almost all the water intake becomes UPW (Hoo et al., 2009; TSMC, 2020; UMC, 2020).

The water used per unit of production varies widely: ranging from 50 t/wfr-m^2 of PSMC to almost 250 t/wfr-m^2 of HHS (Fig. 5). The TSMC indicator is on the average. HHS has the highest water intensity and high volumes of wastewater discharge (94 t/wfr-m^2).

Conversely, from the examination of Fig. 6, in which the volumes of wastewater discharge for MI are shown, the companies that, among all, have the related low volumes of wastewater discharge, are the following: UMC, PSMC and TSMC.

Many different wastes are produced during the semiconductor fabrication processes. The flows of waste generated can be divided into general or non-hazardous waste (e.g., processing waste, waste solvents, waste ammonium sulfate, sludge from water treatment, containers, waste mixed hardware, domestic waste, and others) and hazardous waste (e.g., waste acids, waste solvents, waste copper sulfate, containers and others) (UMC, 2020). The foundries that have the highest values of total waste per wfr-m^2 (Fig. 7) and hazardous waste per wfr-m^2 (Fig. 8) are also those (TSMC and SMIC) that have the highest revenue per unit of production and produce the wafers with the most advanced and complex architecture.

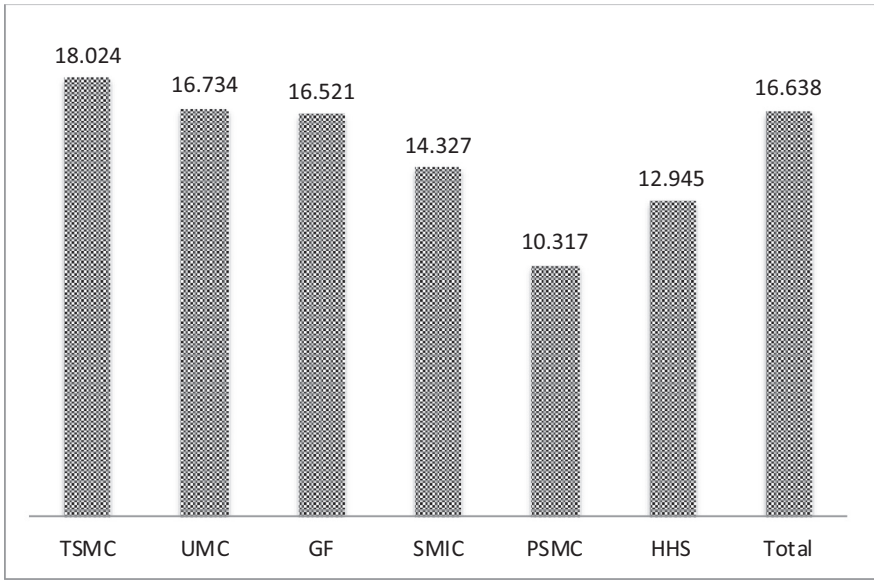


Fig. 4. Energy Intensity (MWh/wfr-m^2).

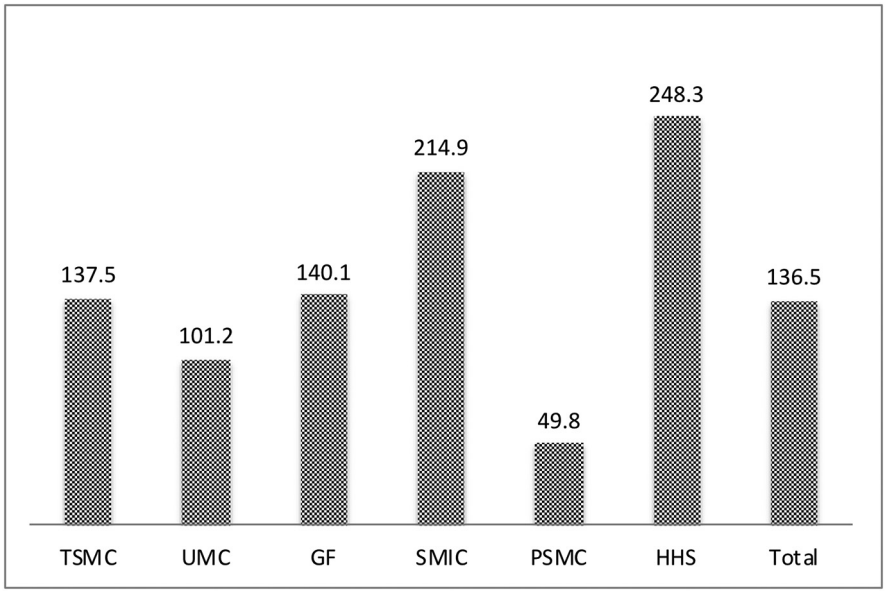


Fig. 5. Tons of Water Withdrawn per wfr-m^2.

In order to better summarize and understand the overall situation, it was considered useful, as above stated, to group the values of the calculated KEPIs in a summary dashboard (Table 5).

By the above Table 5, it was possible to get a schematic picture of the comparative assessment of the various companies regarding their respective environmental impacts and eco-efficiency performance. In fact, it was possible to easily compare these indices, not only, each other for the same item of the table, but also with those indices of other items for the same and/or other company. SMIC and TSMC were the foundries with the highest overall average impact: (as resource use, GHG emission and waste generation) respectively, 0.89 and 0.70. These same companies, as stated above, were also those that had the highest technology capacity, the highest revenues and the most advanced semiconductors production.

PSMC had the best environmental performance compared to the others (0.38 as average value).

It is clear that advanced products (higher revenue/MI), bigger company size (higher annual revenue), and higher technological capacity (R&D investments, technology process node) are not always directly related to lower eco-efficiency indicators.

4. Discussion

The first attempt to assess the environmental impact of chip manufacturing was made by Ahmad in his 2007 thesis dissertation concerning the application of LCA methodology to a CMOS wafer production. In the conclusions of his study, he stated that – in accordance with what was highlighted above in this paper, about the double burden of energy consumption from non-renewable sources for the overall environmental impact of a company – the energy consumption of manufacturing equipment and tools are preponderant (75 %), compared to other components, for the overall environmental effects associated with CMOS production.

These considerations were also confirmed by the results of the subsequent research of Liu et al. (2010) and Wang (2014). The formers dealt with the LCA of DRAM (dynamic random-access memory) in Taiwan's

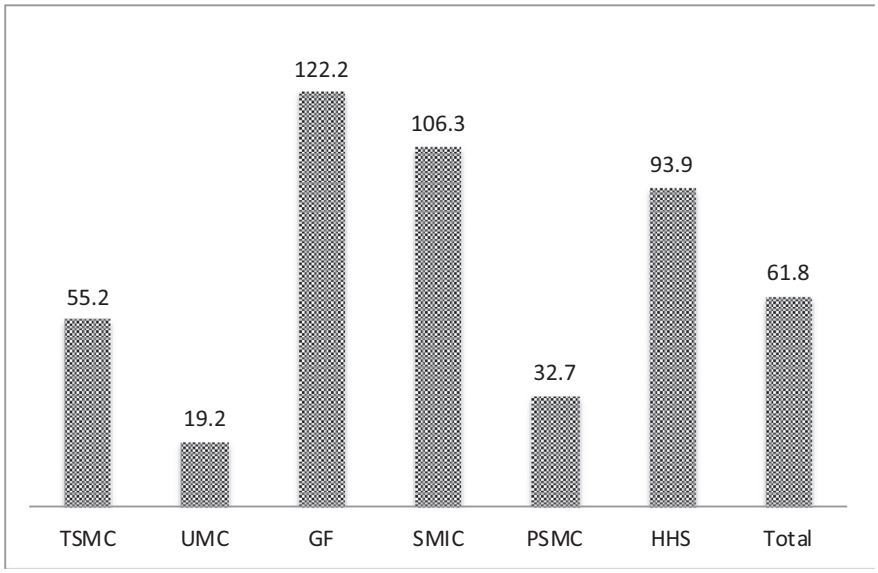


Fig. 6. Tons of Wastewater Discharge per wfr-m^2.

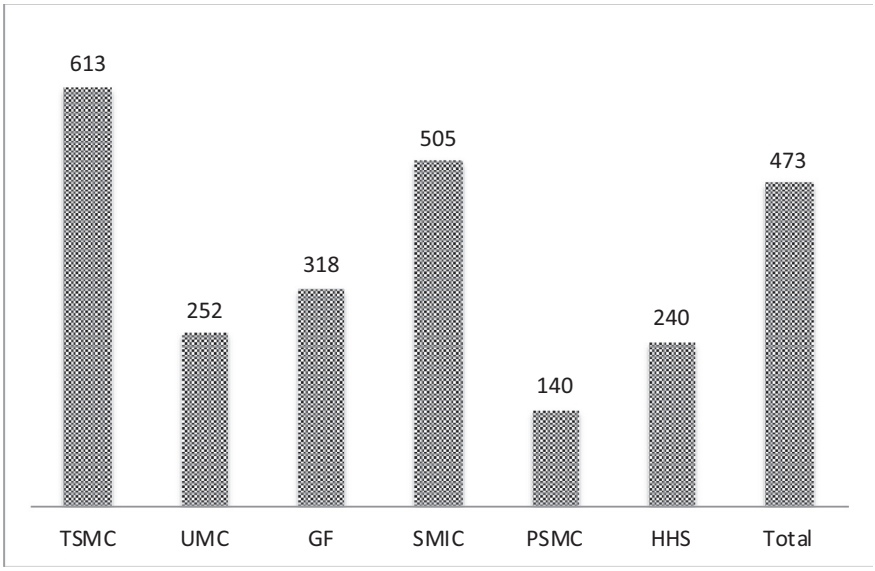


Fig. 7. Kilograms of General Waste Generated per wfr-m^2.

semiconductor manufacturers. Their conclusions were that the use of non-renewable sources of energy and the global warming potential were the primarily responsible of the environmental impacts of this industry. In particular, according them, the following processes had, in descending order, the bigger contribution to pollution: etching, diffusion, and photolithography. Wang also stated that most of the energy consumed in the production phase (64 %), principally used to assure high air purity standards into cleanrooms, contributed to the carbon footprint of ICs.

Reducing the use of energy from non-renewable sources – to better manage, within acceptable and sustainable limits, the environmental impacts of the semiconductor manufacturing industry, especially to achieve high standards of energy efficiency and significant reduction of global warming potential – was also recognized as a primary need by Boyd et al. (2010).

Kuo et al. (2022) – in addition to further reiterating that electricity consumption, during the manufacturing phase, was the main responsible of the environmental impacts of the semiconductor sector – stated that the nanoscale parameter of the wafer feature heavily affected the overall environmental impact of the process: in particular, according to these authors, the impact of 20 nm technology was less than that of 30 nm or 40 nm ones. This conclusion confirms the considerations of this paper about the technology process node as a key parameter of the valuation of the technological capacity grade and the assessment of environmental impacts of a company. Huang et al. (2016) also stated, in fact, that the technology node and the number of mask layers were the main parameters of the regression models for predicting the CFP (carbon footprint of a product) of a wafer. This result considerably simplified the LCA calculation reducing the amount of information, time and costs.

Regards to the GHG emissions, above cited for their Scope 1 and Scope 2 related components, it should be specified that, for the purposes of the overall assessment of the contribution given by a production process or a company to the generation of GHG emissions, it would be appropriate, from a LCA point of view, taking also into account that component (i.e., Scope 3) of GHG emissions related to the activities of a company that are not included in Scope 1 and Scope 2 categories: i.e. those emissions that are

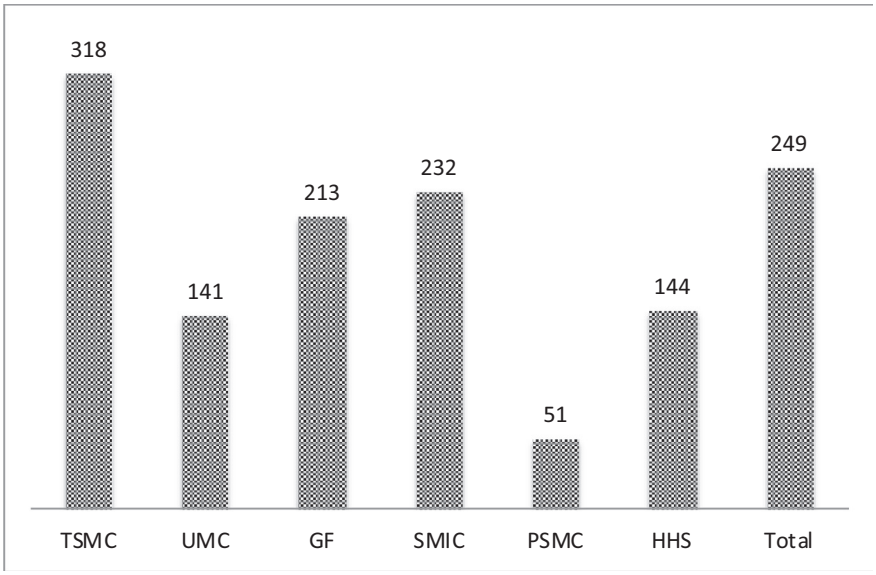


Fig. 8. Kilograms of Hazardous Waste Generated per wfr-m^2.

Table 5
Summary dashboard and value classes on the mood scale.
Sources: Elaboration of data of TSMC (2020), UMC (2020), GF (2021), SMIC (2020), PSMC (2020), HHS (2020).

	TSMC	UMC	GF	SMIC	PSMC	HHS
a) Smallest Technology Node (nm)[a]	5 [VG]	14 [N]	12 [N]	8 [VG]	22 [VB]	14 [N]
b) Revenue/MI	1.00 [VG]	0.54 [N]	0.63 [G]	0.70 [G]	0.14 [VB]	0.27 [B]
c) R&D Investments/MI	0.68 [G]	0.35 [B]	0.45 [N]	1.00 [VG]	0.16 [VB]	0.31 [B]
d) GHG_1/MI	0.59 [N]	0.72 [B]	0.49 [N]	1.00 [VB]	0.20 [VG]	0.06 [VG]
e) GHG_2/MI	0.62 [B]	0.65 [B]	0.09 [VG]	1.00 [VB]	0.36 [G]	0.53 [N]
f) F-GHG/MI	0.37 [G]	0.55 [N]	0.43 [N]	0.89 [VB]	1.00 [VB]	0.93 [VB]
g Energy/MI	1.00 [VB]	0.93 [VB]	0.92 [VB]	0.79 [B]	0.57 [N]	0.72 [B]
h) Water Withdrawal/MI	0.55 [N]	0.41 [N]	0.56 [N]	0.87 [VB]	0.20 [VG]	1.00 [VB]
i) Wastewater Discharge/MI	0.45 [N]	0.16 [VG]	1.00 [VB]	0.87 [VB]	0.27 [G]	0.77 [B]
l) General Waste Generated/MI	1.00 [VB]	0.38 [G]	0.36 [G]	0.93 [VB]	0.30 [G]	0.32 [G]
m) Hazardous Waste Generated/MI	1.00 [VB]	0.44 [N]	0.67 [B]	0.73 [B]	0.16 [VG]	0.45 [N]
n) Average [n = Σ(d÷m)/8]	0.70 (0.79) [B]	0.54 (0.61) [B]	0.57 (0.64) [B]	0.89 (1.00) [VB]	0.38 (0.43) [N]	0.60 (0.67) [B]

Legend: VB: very bad; B: bad; N: neutral; G: good; VG: very good.
[a] According to a scale with the following classes: 5 ÷ 8.4: VG; 8.5 ÷ 11.8: G; 11.9 ÷ 15.2: N; 15.3 ÷ 18.6: B; 18.7 ÷ 22: VB.

generated by the remaining large fraction of the value chain of a company (e.g., related to the mobility of employees, to supply chain, logistics, the use of the products, etc.). Unfortunately, this GHG category is difficult to calculate for this sector and only two companies (TSMC and UMC) published these data in their CSR reports; for this reason, this GHG component was excluded from this research. Indeed, the importance of this category, for the assessment of the overall CO_2 footprint of this specific industry, was also recognized by Higgs et al. (2009), who further highlighted the computational difficulties due to a lack of standardization boundaries and standard methodologies for several components of the semiconductor manufacturing footprint.

In conclusion of this overview, it can be deduced, by the survey of the available scientific literature, that no research, to date, has focused on the environmental impacts of the chip manufacturing or fabrication sector in its entirety or, in any case, of its single whole company.

5. Conclusions

Analyzing the entire value chain of manufacturing of these electronic components, the fabrication processes are undoubtedly those with the highest environmental impact, due to the huge quantities of raw materials and waste produced.

In conclusion, it can be stated that, differently to what happens in many other industrial sectors, in the semiconductor fabrication phase, larger company size and advanced products are not always related to lower quantities, per unit of production, of energy, waste and GHG emissions. In fact, those foundry firms that have the highest revenue per unit of production (TSMC, SMIC, GF, UMC), producing the most advanced semiconductors, are the same ones that have the highest GHG emission intensity indicators – excluding, in this case, the situation of GF, which stated, in its CSR report, values of indirect GHG emissions much lower than the direct ones – the highest energy intensity of their products, and the highest waste generation per unit of production.

The comparative analysis and assessment of the performance and eco-efficiency of the analyzed companies allowed to give an overall reliable picture of the current resource consumption and pollution of this industrial sector, highly strategic for the development and sustainability of the entire world economy.

Furthermore, the results of this study contribute both to provide elements of investigation or reflection for further scientific research on the environmental issues of the semiconductor industry.

It is hoped that, for the future, especially those foundry firms with the highest revenue and the most advanced technologies will invest much more to optimize their energy and water use and to adopt more efficient recovery and recycling systems, in order to further reduce the amount of their GHG emissions and waste, especially of hazardous ones.

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Data availability

Data will be made available on request.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could havse appeared to influence the work reported in this paper.

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