CNN projects for Spring 2015

Members

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~~2~~ 1 Groups

- **FPGA implementation group**
  - **step1 : Write a simple CNN using matlab or C source code**
  - **step 2: Naïve CNN on FPGA**
  - **step 3: KAIST_CNN on FPGA**
  - **step 4: SP_CNN on FPGA**
  - **step 5: Bigger scales on FPGA**
- CNN algorithm developments
  - Functional simulator
  - Test out other inputs

future work

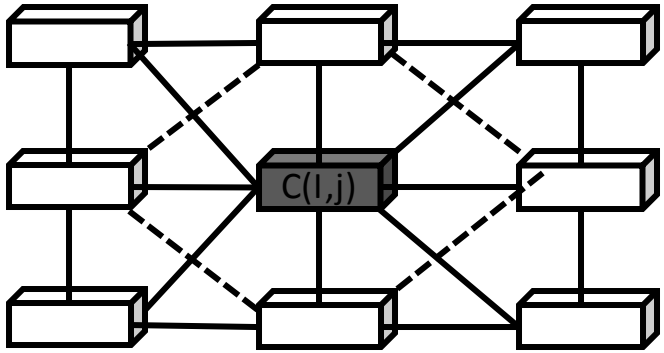
  - Other neural networks
  - Convolutional neuron network

CNN Simulator

- https://dmanatunga@bitbucket.org/dmanatunga/cnn-simulator.git

- author: Dilan Manatunga manatunga@gmail.com
- Look at matlab directory, look at the holefiling example

Naïve CNN



$$x_{ij}(t+1) = \sum_{C(k,l)\in N_r(i,j)} A(i,j;k,l) * y_{kl}(t) + \sum_{C(k,l)\in N_r(i,j)} B(i,j;k,l) * u_{kl}(t) + I$$

$$y_{ij}(t+1) = \frac{1}{2}\left[|x_{ij}(t)+1| - |x_{ij}(t)-1|\right]$$

8-bit operations

input comes from a memory

Registers for A,B templates

y function is fixed

Put a ALU for functional units

First CNN Design

- 6x6 CNN
- input image 8 bits. (6x6 image cells)
- MAC: Multiply + Adder
- Each cell has 9 MAC units to compute with outputs, 9 MAC units to compute with neighbor input values, 1 final adder to sum constant
- A,B, I value registers

MAC Sharing CNN

- Naïve CNN: All 9 inputs are summed together
- MAC sharing CNN: use only 1 MAC unit to sum all 9 inputs
- → A basic model for KAIST_CNN

KAIST_CNN

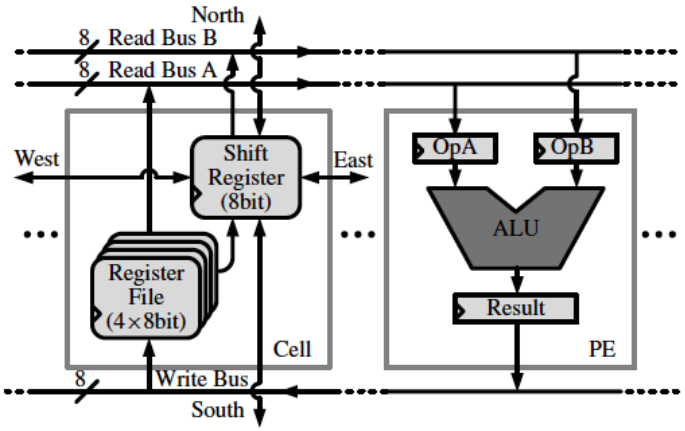


Fig. 6. Cell-PE interconnection. Each PE can access 40 cells through two read buses and one write bus.

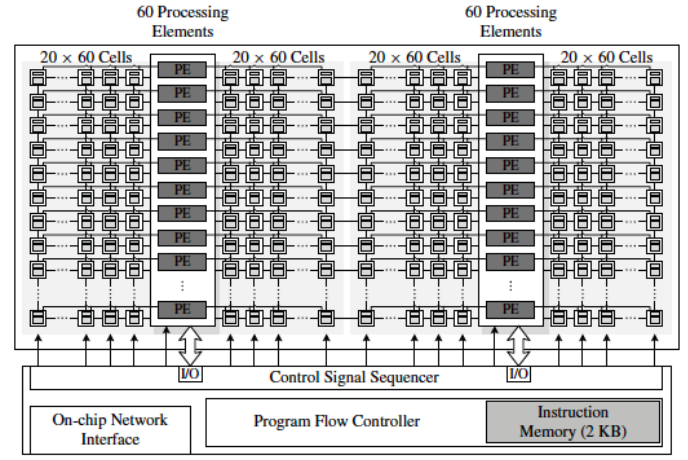
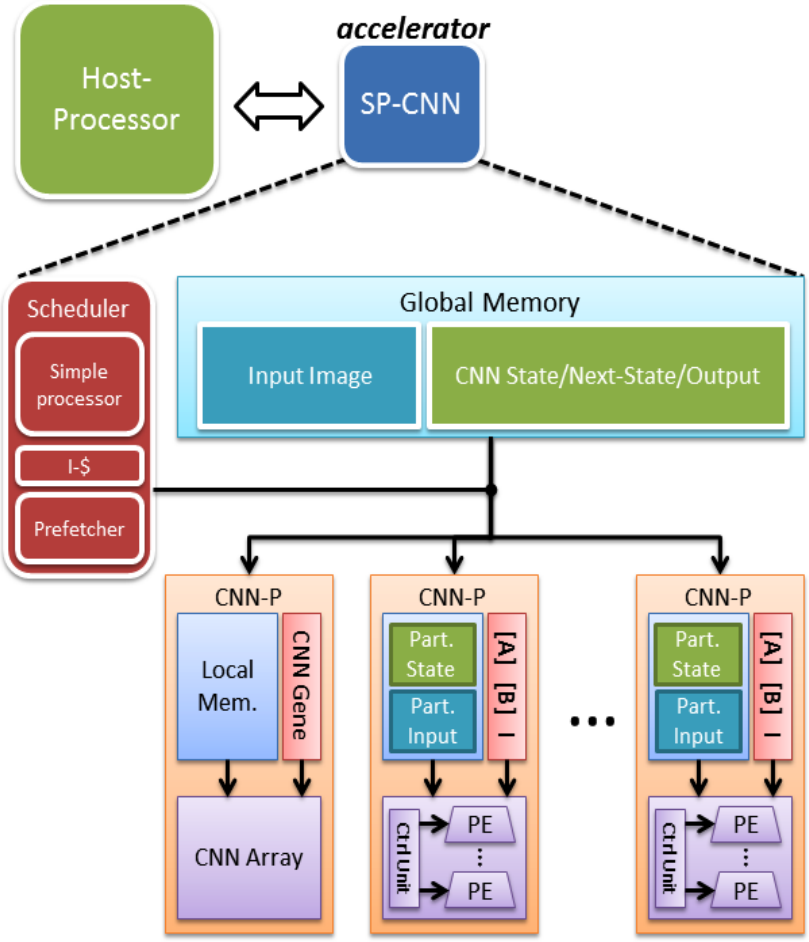


Fig. 5. Block diagram of the VAE. A total of 120 PEs are shared by 4800 cells.

ALUs are shared

Required a shift register

SP-CNN



Start from CNN-P ,
Connect with a SRAM memory
2 CNN-Ps
Connect with a SRAM memory