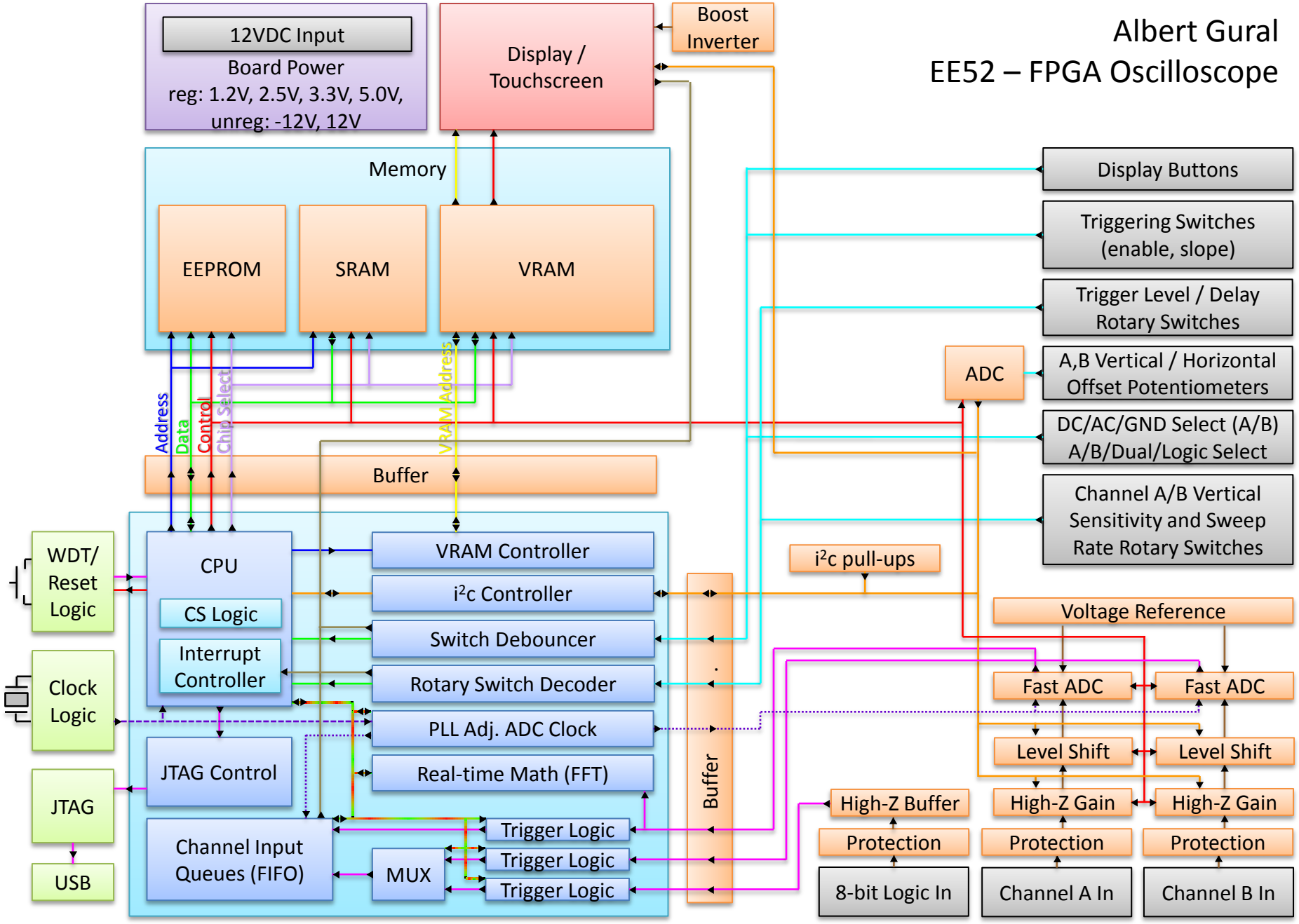
Albert Gural
EE52 – FPGA Oscilloscope
12VDC Input
Board Power
reg: 1.2V, 2.5V, 3.3V, 5.0V,
unreg: -12V, 12V
Display / Touchscreen
Boost Inverter
Memory
EEPROM
SRAM
VRAM
Address
Data
Control
Chip Select
VRAM Address
Buffer
Display Buttons
Triggering Switches (enable, slope)
Trigger Level / Delay Rotary Switches
ADC
A,B Vertical / Horizontal Offset Potentiometers
DC/AC/GND Select (A/B)
A/B/Dual/Logic Select
Channel A/B Vertical Sensitivity and Sweep Rate Rotary Switches
WDT/ Reset Logic
Clock Logic
JTAG
USB
CPU
CS Logic
Interrupt Controller
JTAG Control
Channel Input Queues (FIFO)
VRAM Controller
i²c Controller
Switch Debouncer
Rotary Switch Decoder
PLL Adj. ADC Clock
Real-time Math (FFT)
Trigger Logic
Trigger Logic
Trigger Logic
MUX
Buffer
i²c pull-ups
Voltage Reference
Fast ADC
Fast ADC
Level Shift
Level Shift
High-Z Gain
High-Z Gain
High-Z Buffer
Protection
Protection
Protection
8-bit Logic In
Channel A In
Channel B In

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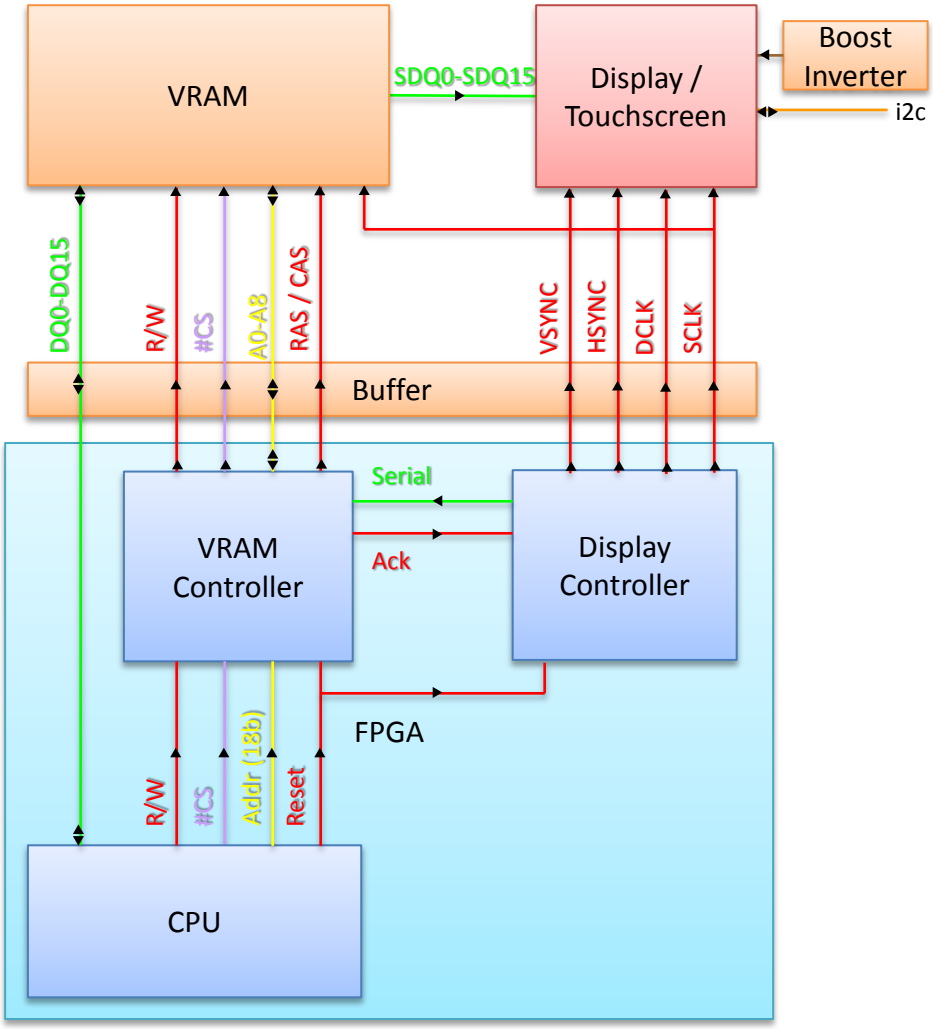
EE52 – FPGA Oscilloscope
Video Display Block Diagram