AVR - HW8

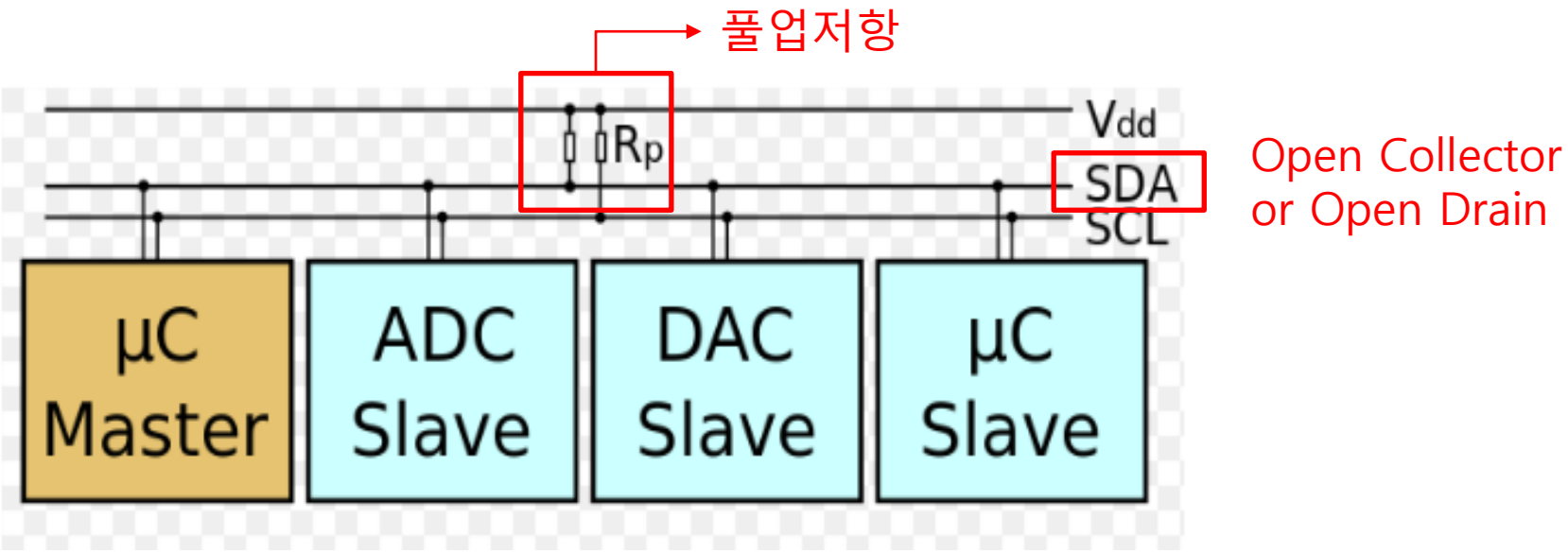
임베디드스쿨1기
Lv1과정
2020. 11. 06
손표훈

1. I2C통신

(1) I2C통신? I2C버스방식을 사용한 직렬 동기통신이고 반이중(Half-Duplex)다.

- I2C버스란? 장치들간 연결을 위한 필립스에서 개발한 직렬 컴퓨터 버스
- I2C버스는 양방향 오픈 드레인(또는 오픈 컬렉터)방식이며, SCL(Serial Clock)과 SDA(Serial Data) 두 선을 이용한다.
- H/W적으로 포트를 줄일 수 있어 경제적이고 하나의 버스에 여러 개의 장치를 연결할 수 있다.

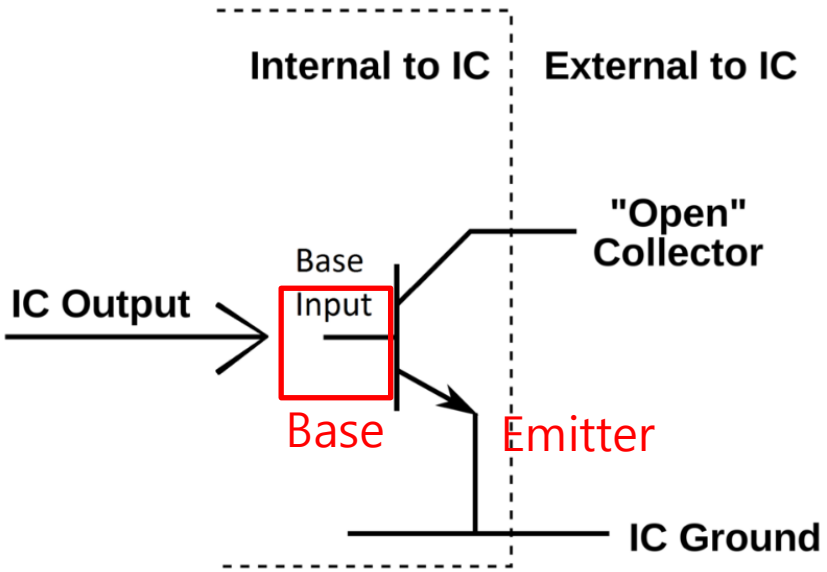
(2) I2C통신의 구조



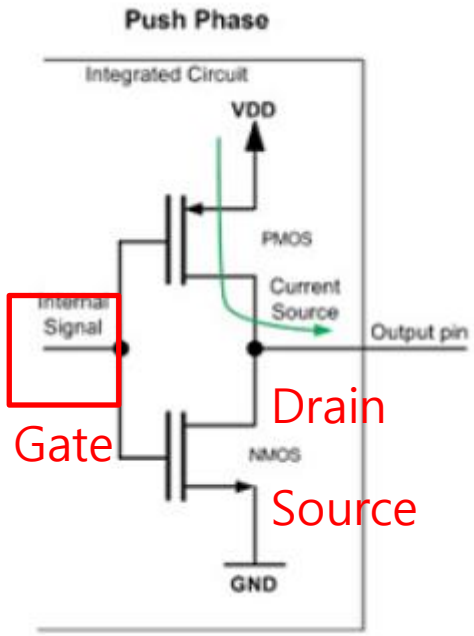
1. I2C통신

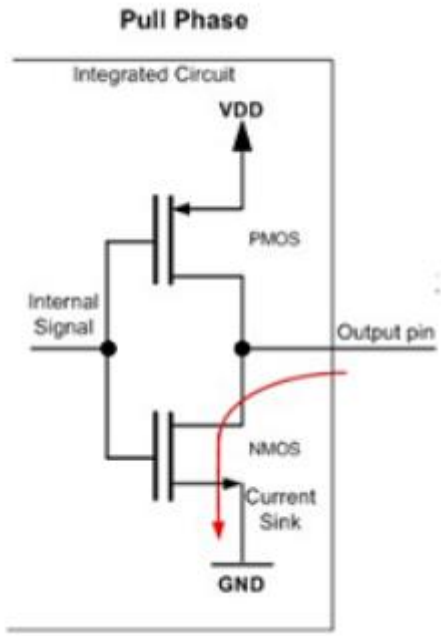
※ Open Collector(Open Drain)?
- BJT(NPN)의 경우 Open Collector, FET(N-ch)의 경우 Open Drain이라 한다.

Open Collector



Open Drain





- 왜 이 구조를 사용할까?

우선 BJT와 FET는 간단히 말해 "가변저항"이라 볼 수 있다.
둘의 차이는 "전류제어"냐 "전압제어"냐의 차이(실제로 FET도 게이트 최소 전류가 있음..)
NPN BJT의 경우 Base에서 Emitter로 전류가 흐르면 Collector와 Emitter사이에 저항 값이 낮아진다.
N-ch FET의 경우 Gate의 전위보다 Source의 전위가 낮으면 Drain과 Source사이의 저항 값이 낮아진다.

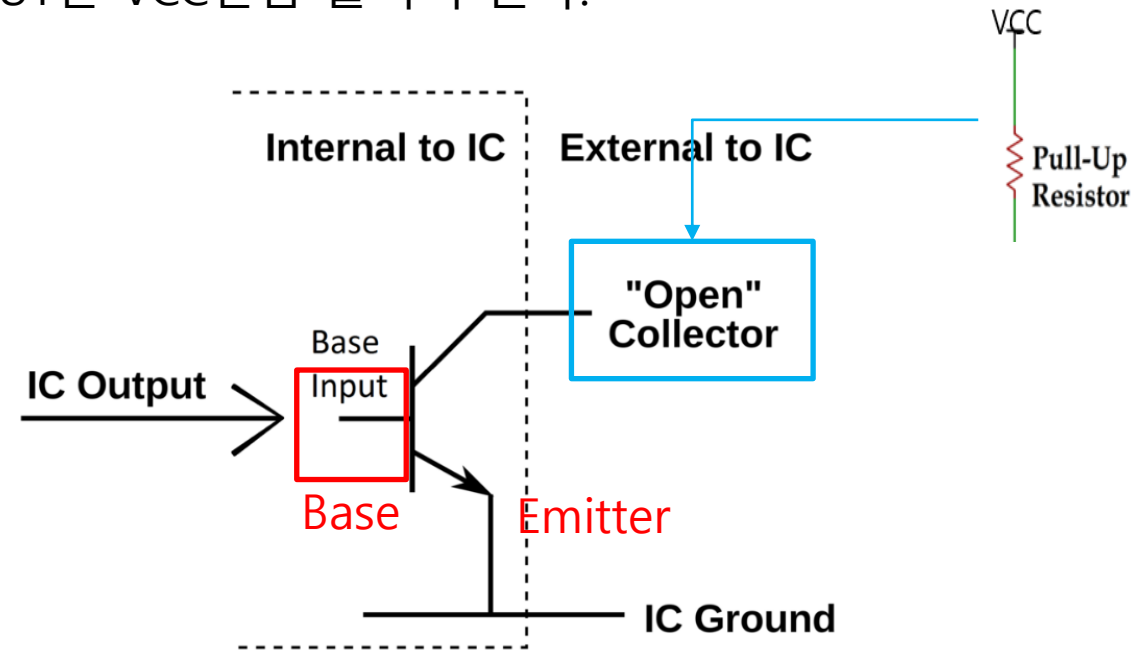
1. I2C통신

- 왜 이 구조를 사용할까?
- 주로 디지털에서 스위칭 용도로 사용됨

BJT를 예로들면
ON동작 : Base에 전압이 가해져서(High) B -> E로 전류가 흐르면(대략 1mA 이상) C-E의 저항이 낮아지면서(포화) 전위가 GND에 가까워진다.

OFF 동작 : 반대로 Base전압이 끊기면(Low) B->E로 전류가 흐르지 않아 C-E 저항 값이 높아진다..

만약 Open Collector로 명시된 곳(OUTPUT)에 Pull-Up저항으로 원하는 전압의 레벨과 연결한다면 BJT가 OFF가 되면 OUTPUT은 VCC만큼 출력이 된다.



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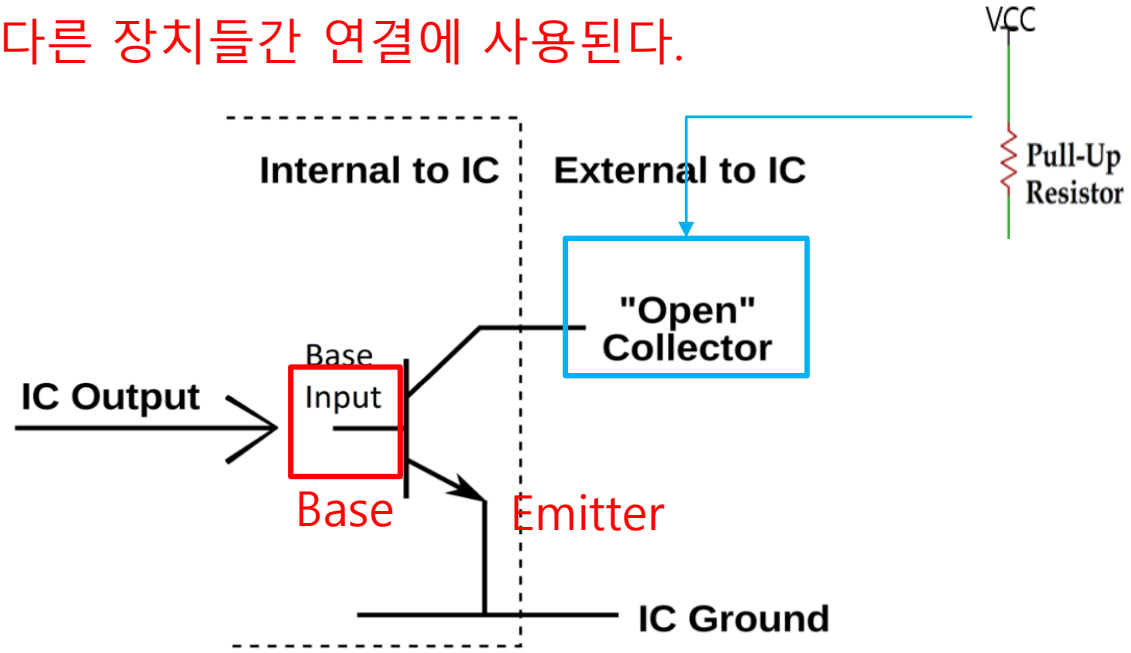
이 때 Open Collector로 명시된 곳(OUTPUT)에 Pull-Up저항으로 원하는 전압의 레벨과 연결한다면 BJT가 OFF가 되면 OUTPUT은 VCC만큼 출력이 된다.

따라서 동작전압이 서로 다른 장치들간 연결에 사용된다.

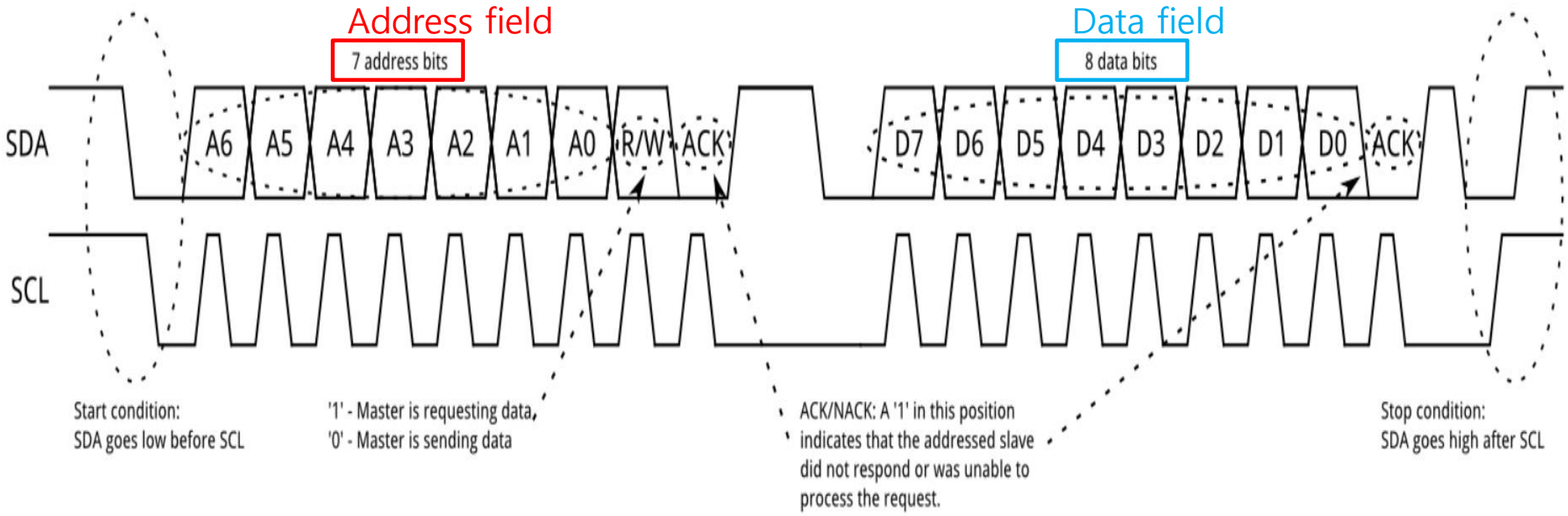


1. I2C통신

(3) I2C 통신 프로토콜

- Master에서 통신을 제어한다.
- Start, Stop : SCL이 'H'일 때 SDA가 'L'면 Start, 반대로 'L'일 때 'H'이면 Stop을 의미한다.
  만약 Stop에서 바로 'L'가 이어지면 다음 데이터의 시작을 의미한다.
- 데이터 패킷은 아래와 같다.

- 프레임의 ACK Bit자리는 '1'이면 Slave가 Master의 데이터 수신이 정상임을 뜻하고 '0'(NACK)는
- 수신오류를 의미한다.



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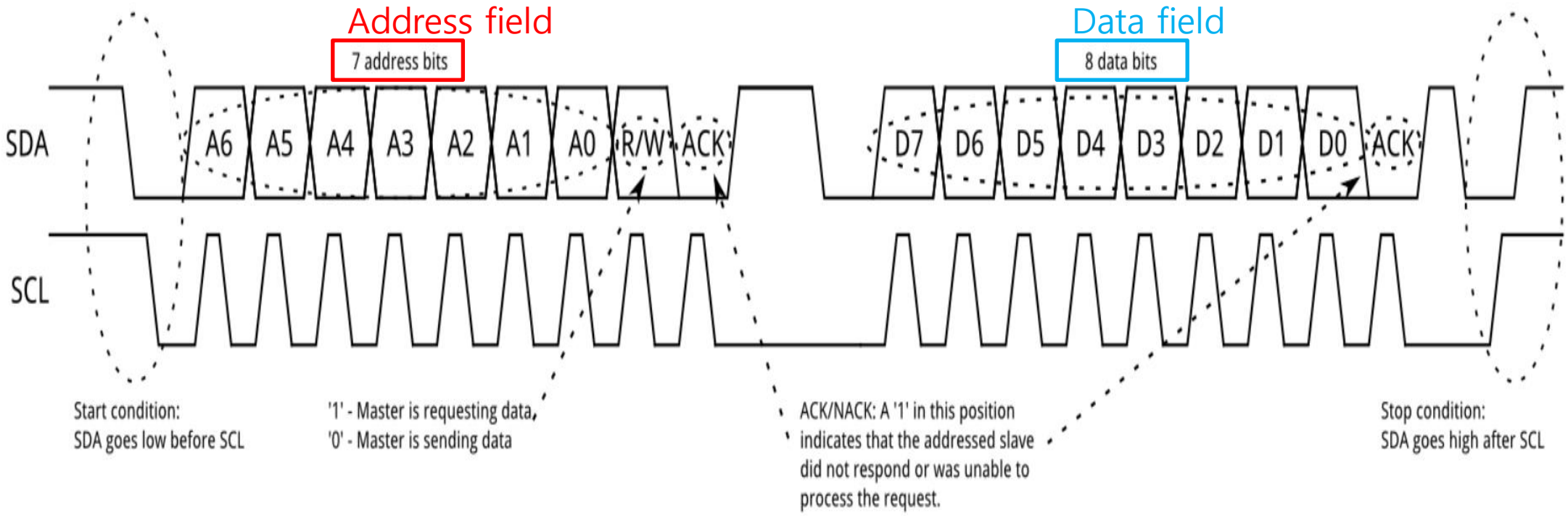
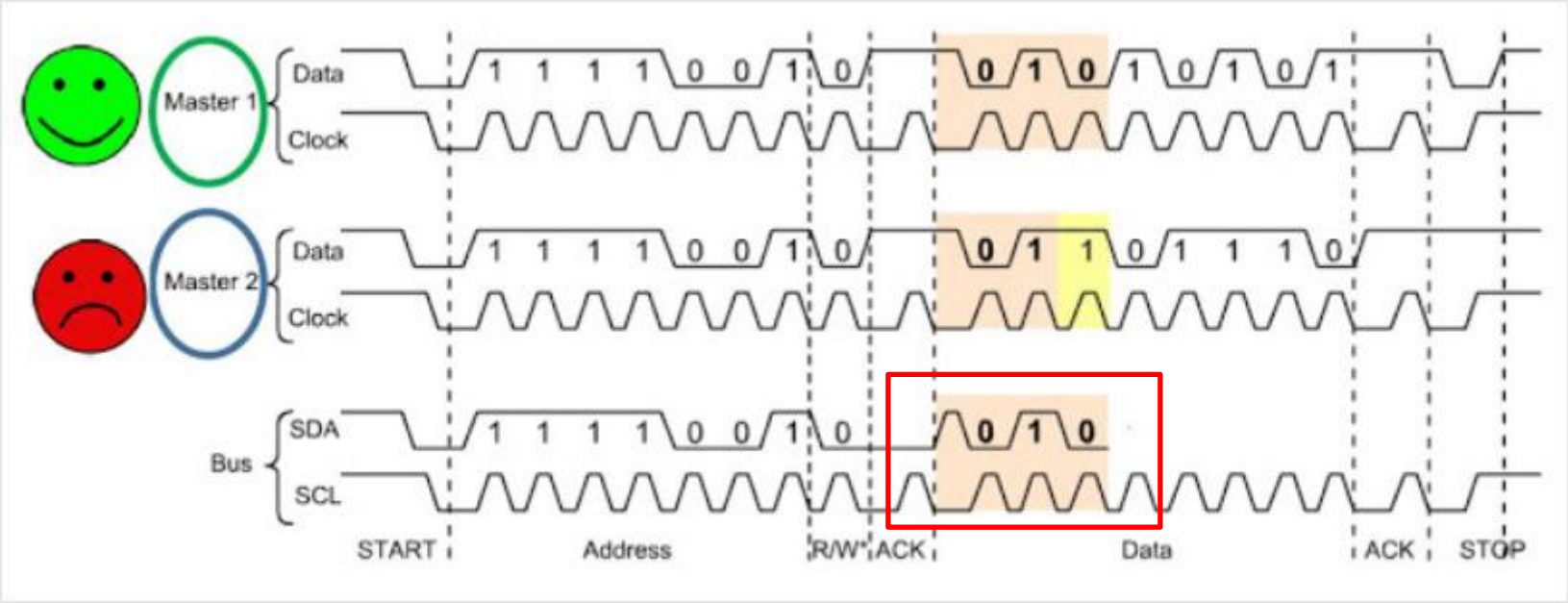


1. I2C통신

(3) I2C 통신 프로토콜
- I2C는 여러 개의 Master를 버스에 연결할 수 있다.
- 만약 여러 개의 Master가 동시에 데이터 전송을 한다면
  Open Collector 특성상 'L'가 우위를 점한다.

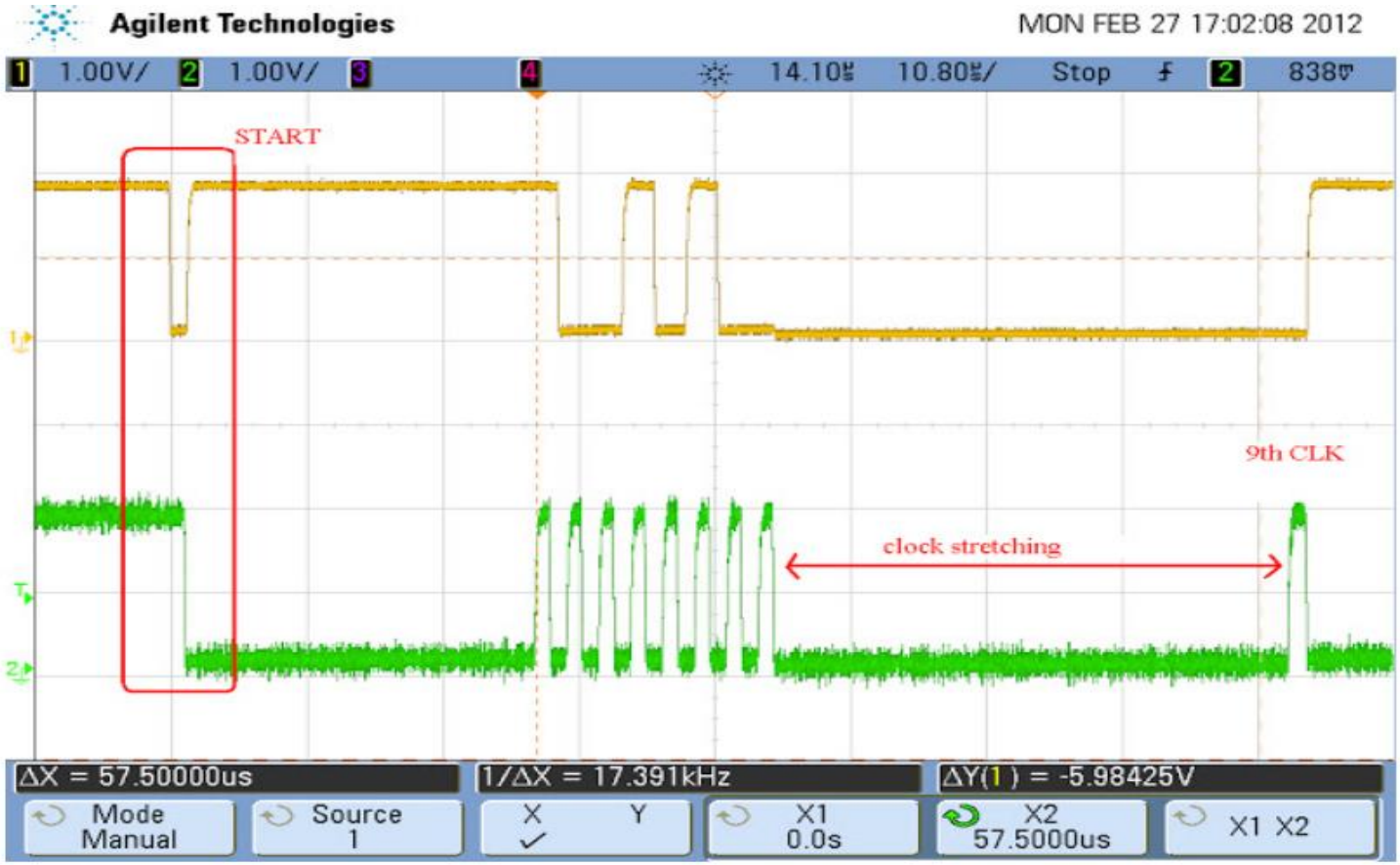
Master1과 Master2가 있을 때
Master1 : 0101010
Master2 : 0110111이라면..
버스는 아래 그림과 같이 된다... 이 와 같은 상황을 I2C Arbitration이라 한다.



1. I2C통신

(3) I2C 통신 프로토콜

- Slave의 데이터 처리가 지연이 생길 때 Clock Stretching이 Slave로 부터 발생한다..
  Slave가 강제로 SCL라인을 'L'로 내려버린다.



1. I2C통신

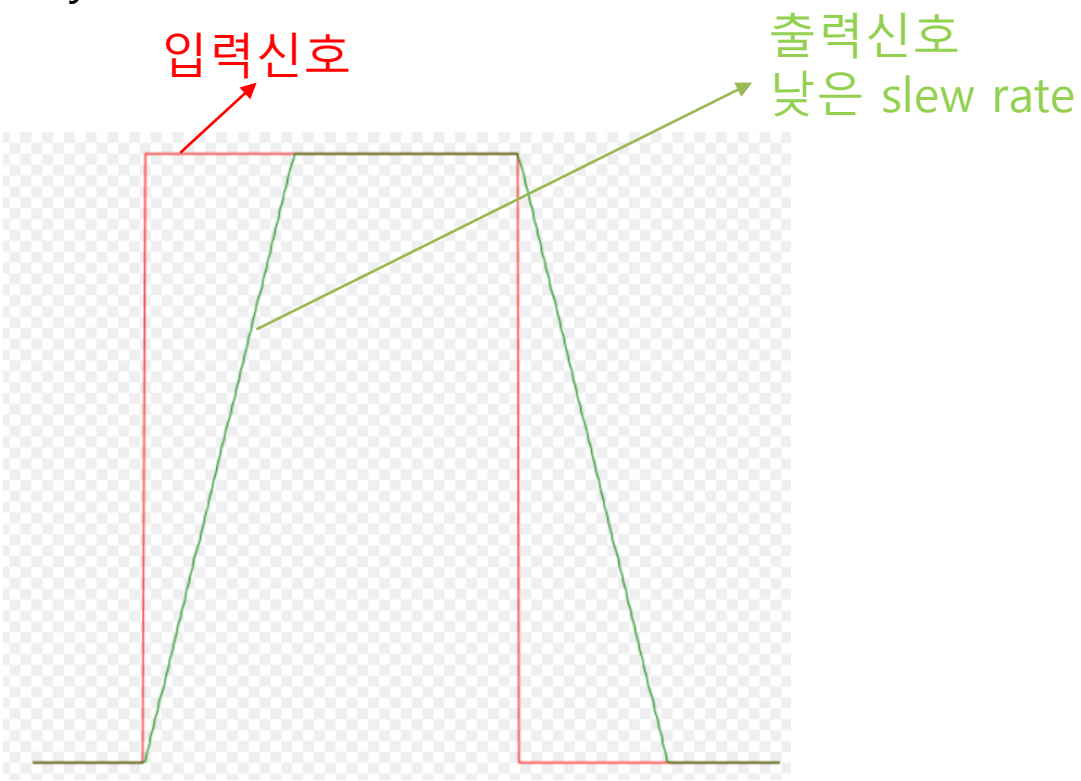
(4) ATmega328P의 I2C통신

Features

- Simple yet powerful and flexible communication interface, only two bus lines needed
- Both master and slave operation supported
- Device can operate as transmitter or receiver
- 7-bit address space allows up to 128 different slave addresses
- Multi-master arbitration support
- Up to 400kHz data transfer speed
- Slew-rate limited output drivers
- Noise suppression circuitry rejects spikes on bus lines
- Fully programmable slave address with general call support
- Address recognition causes wake-up when AVR® is in sleep mode
- Compatible with Phillips' I²C protocol

일반적인 i2c프로토콜을 사용 할 수 있다

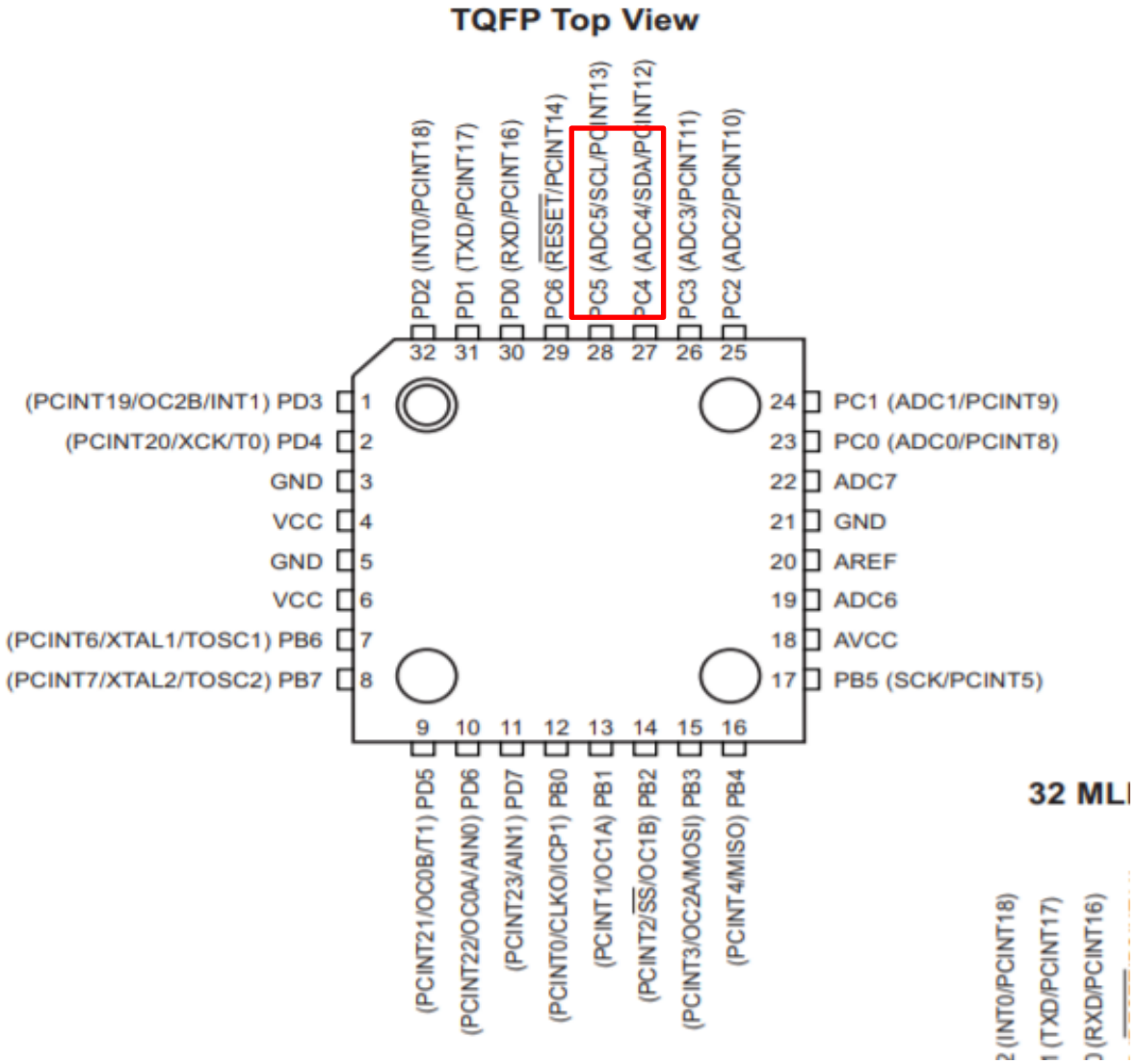
Slew Rate?
최대 출력 변화율로 보통 V/us단위로 많이 사용한다
Delay가 아님!



Slew Rate를 제한하는이유?
Slew Rate가 높을수록 전압 변화폭이 커서 EMI에 악영향이 생김(스위칭 노이즈)
그 외 다른이유가 있는지 궁금합니다!

1. I2C통신

(4) ATmega328P의 I2C통신
- 핀맵

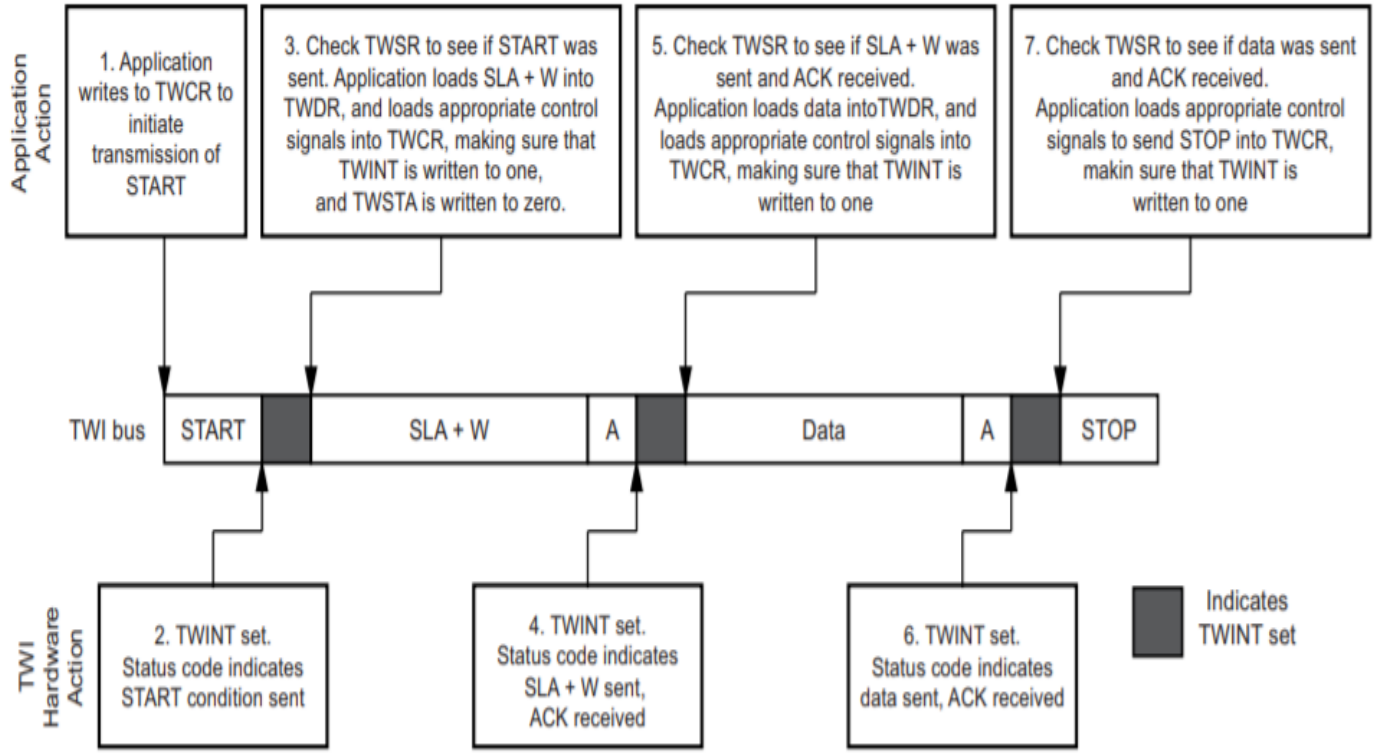


포기하면 얻는 건 아무것도 없다.

1. I2C통신

(4) ATmega328P의 I2C통신
- 데이터 패킷

Figure 21-10. Interfacing the Application to the TWI in a Typical Transmission



S:	START condition
Rs:	REPEATED START condition
R:	Read bit (high level at SDA)
W:	Write bit (low level at SDA)
A:	Acknowledge bit (low level at SDA)
$\overline{A}$:	Not acknowledge bit (high level at SDA)
Data:	8-bit data byte
P:	STOP condition
SLA:	Slave address

1. I2C통신

(4) ATmega328P의 I2C통신

- Master Transmitter에 따른 TWCR(I2C Control Register) 설정
  다음 페이지의 TWSR의 상태를 보고 TWCR 레지스터를 설정해야함

A START condition is sent by writing the following value to TWCR:

TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE
value	1	X	1	0	X	1	0	X

TWEN must be set to enable the 2-wire serial interface, TWSTA must be written to one to transmit a START condition and TWINT must be written to one to clear the TWINT flag. The TWI will then test the 2-wire serial bus and generate a START condition as soon as the bus becomes free. After a START condition has been transmitted, the TWINT flag is set by hardware, and the status code in TWSR will be 0x08 (see Table 21-3). In order to enter MT mode, SLA+W must be transmitted. This is done by writing SLA+W to TWDR. Thereafter the TWINT bit should be cleared (by writing it to one) to continue the transfer. This is accomplished by writing the following value to TWCR:

TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE
value	1	X	0	0	X	1	0	X

When SLA+W have been transmitted and an acknowledgement bit has been received, TWINT is set again and a number of status codes in TWSR are possible. Possible status codes in master mode are 0x18, 0x20, or 0x38. The appropriate action to be taken for each of these status codes is detailed in Table 21-3.

When SLA+W has been successfully transmitted, a data packet should be transmitted. This is done by writing the data byte to TWDR. TWDR must only be written when TWINT is high. If not, the access will be discarded, and the write collision bit (TWWC) will be set in the TWCR register. After updating TWDR, the TWINT bit should be cleared (by writing it to one) to continue the transfer. This is accomplished by writing the following value to TWCR:

TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE
value	1	X	0	0	X	1	0	X

This scheme is repeated until the last byte has been sent and the transfer is ended by generating a STOP condition or a repeated START condition. A STOP condition is generated by writing the following value to TWCR:

TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE
value	1	X	0	1	X	1	0	X

A REPEATED START condition is generated by writing the following value to TWCR:

TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE
value	1	X	1	0	X	1	0	X

After a repeated START condition (state 0x10) the 2-wire serial interface can access the same slave again, or a new slave without transmitting a STOP condition. Repeated START enables the master to switch between slaves, master transmitter mode and master receiver mode without losing control of the bus.

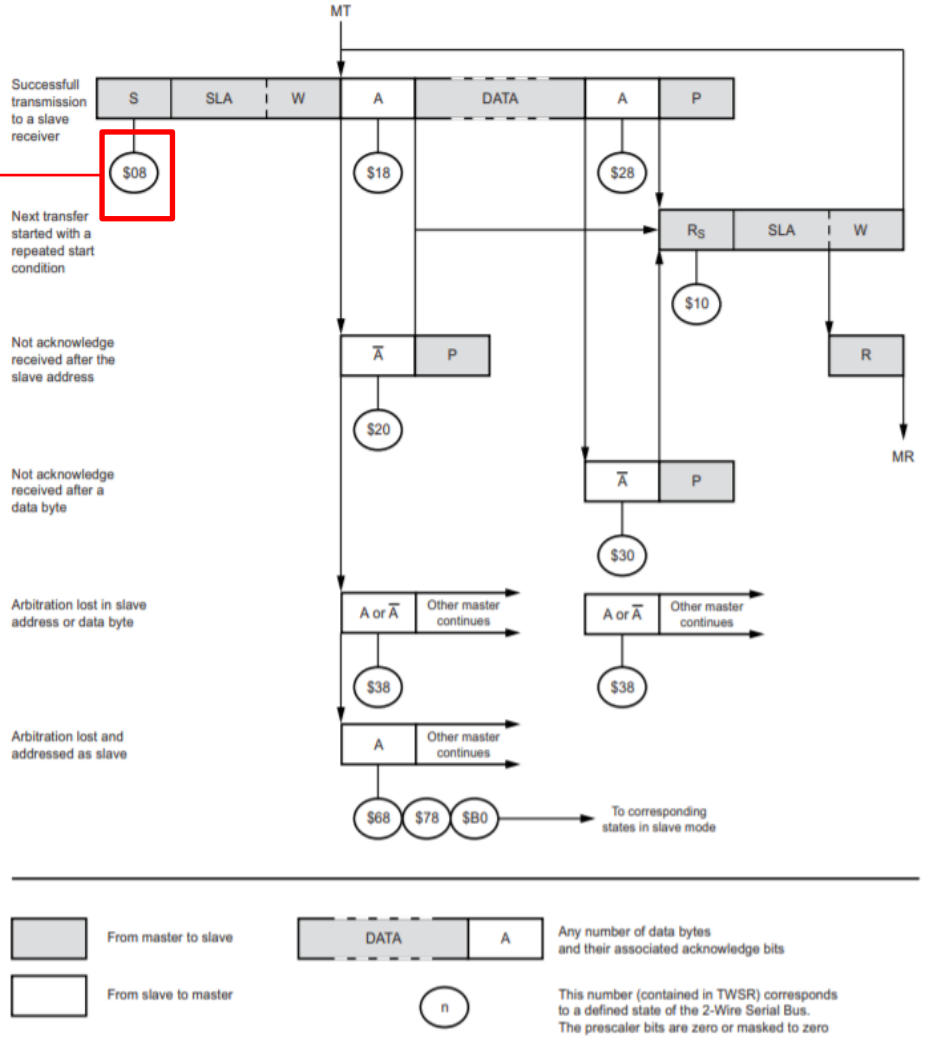
1. I2C통신

(4) ATmega328P의 I2C통신

Table 21-3. Status Codes for Master Transmitter Mode

Status Code (TWSR) Prescaler Bits are 0	Status of the 2-wire Serial Bus and 2-wire Serial Interface Hardware	Application Software Response: To/from TWDR	To TWCR: STA	STO	TWINT	TWEA	Next Action Taken by TWI Hardware
0x08	A START condition has been transmitted	Load SLA+W	0	0	1	X	SLA+W will be transmitted; ACK or NOT ACK will be received
0x10	A repeated START condition has been transmitted	Load SLA+W or	0	0	1	X	SLA+W will be transmitted; ACK or NOT ACK will be received
		Load SLA+R	0	0	1	X	SLA+R will be transmitted; Logic will switch to master receiver mode
0x18	SLA+W has been transmitted; ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO Flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO flag will be reset
0x20	SLA+W has been transmitted; NOT ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO flag will be reset
0x28	Data byte has been transmitted; ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO flag will be reset
0x30	Data byte has been transmitted; NOT ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO flag will be reset
0x38	Arbitration lost in SLA+W or data bytes	No TWDR action or	0	0	1	X	2-wire Serial Bus will be released and not addressed Slave mode entered
		No TWDR action	1	0	1	X	A START condition will be transmitted when the bus becomes free

re 21-12. Formats and States in the Master Transmitter Mode



데이터 프레임의 전송상태를 TWSR(I2C Status Register)를 통해 알 수 있다.

1. I2C통신

(4) ATmega328P의 I2C통신
- Slave Receiver모드

To initiate the slave receiver mode, TWAR and TWCR must be initialized as follows:

TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE
value	Device's own slave address							

The upper 7 bits are the address to which the 2-wire serial interface will respond when addressed by a master. If the LSB is set, the TWI will respond to the general call address (0x00), otherwise it will ignore the general call address.

TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE
value	0	1	0	0	0	1	0	X

TWEN must be written to one to enable the TWI. The TWEA bit must be written to one to enable the acknowledgement of the device's own slave address or the general call address. TWSTA and TWSTO must be written to zero.

When TWAR and TWCR have been initialized, the TWI waits until it is addressed by its own slave address (or the general call address if enabled) followed by the data direction bit. If the direction bit is "0" (write), the TWI will operate in SR mode, otherwise ST mode is entered. After its own slave address and the write bit have been received, the TWINT flag is set and a valid status code can be read from TWSR. The status code is used to determine the appropriate software action. The appropriate action to be taken for each status code is detailed in Table 21-5. The slave receiver mode may also be entered if arbitration is lost while the TWI is in the master mode (see states 0x68 and 0x78).

If the TWEA bit is reset during a transfer, the TWI will return a "not acknowledge" ("1") to SDA after the next received data byte. This can be used to indicate that the slave is not able to receive any more bytes. While TWEA is zero, the TWI does not acknowledge its own slave address. However, the 2-wire serial bus is still monitored and address recognition may resume at any time by setting TWEA. This implies that the TWEA bit may be used to temporarily isolate the TWI from the 2-wire serial bus.

In all sleep modes other than Idle mode, the clock system to the TWI is turned off. If the TWEA bit is set, the interface can still acknowledge its own slave address or the general call address by using the 2-wire serial bus clock as a clock source. The part will then wake up from sleep and the TWI will hold the SCL clock low during the wake up and until the TWINT flag is cleared (by writing it to one). Further data reception will be carried out as normal, with the AVR® clocks running as normal. Observe that if the AVR is set up with a long start-up time, the SCL line may be held low for a long time, blocking other data transmissions.

Note that the 2-wire serial interface data register – TWDR does not reflect the last byte present on the bus when waking up from these sleep modes.

TWAR(I2C Address Register)를 통해 어드레스 값을 설정한다(초기값 : 0xFF)

1. I2C통신

(4) ATmega328P의 I2C통신
- Slave Receiver모드

Table 21-5. Status Codes for Slave Receiver Mode

Status Code (TWSR) Prescaler Bits are 0	Status of the 2-wire Serial Bus and 2-wire Serial Interface Hardware	Application Software Response					Next Action Taken by TWI Hardware
		To/from TWDR	To TWCR				
			STA	STO	TWINT	TWEA	
0x60	Own SLA+W has been received; ACK has been returned	No TWDR action or	X	0	1	0	Data byte will be received and NOT ACK will be returned
		No TWDR action	X	0	1	1	Data byte will be received and ACK will be returned
0x68	Arbitration lost in SLA+R/W as Master; own SLA+W has been received; ACK has been returned	No TWDR action or	X	0	1	0	Data byte will be received and NOT ACK will be returned
		No TWDR action	X	0	1	1	Data byte will be received and ACK will be returned
0x70	General call address has been received; ACK has been returned	No TWDR action or	X	0	1	0	Data byte will be received and NOT ACK will be returned
		No TWDR action	X	0	1	1	Data byte will be received and ACK will be returned
0x78	Arbitration lost in SLA+R/W as Master; General call address has been received; ACK has been returned	No TWDR action or	X	0	1	0	Data byte will be received and NOT ACK will be returned
		No TWDR action	X	0	1	1	Data byte will be received and ACK will be returned
0x80	Previously addressed with own SLA+W; data has been received; ACK has been returned	Read data byte or	X	0	1	0	Data byte will be received and NOT ACK will be returned
		Read data byte	X	0	1	1	Data byte will be received and ACK will be returned

Table 21-5. Status Codes for Slave Receiver Mode (Continued)

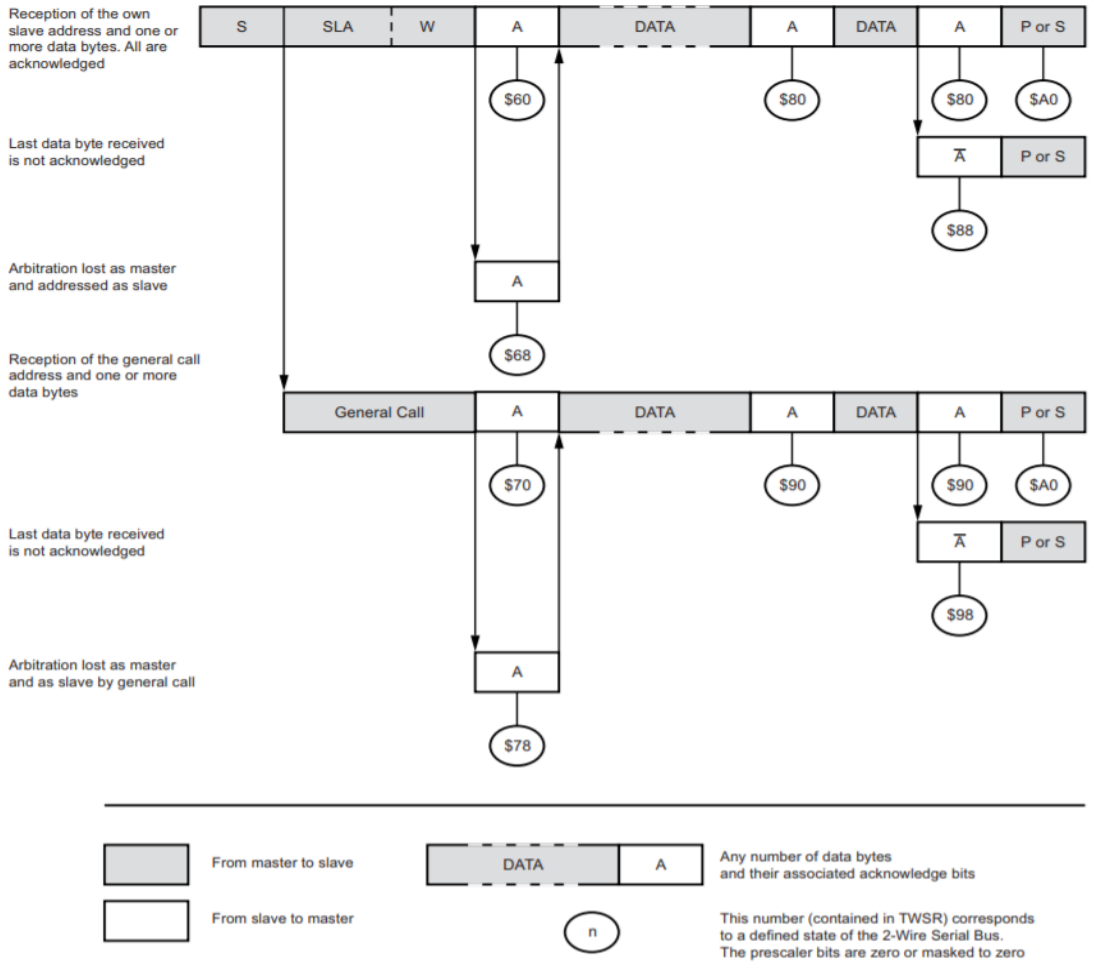
Status Code (TWSR) Prescaler Bits are 0	Status of the 2-wire Serial Bus and 2-wire Serial Interface Hardware	Application Software Response					Next Action Taken by TWI Hardware
		To/from TWDR	To TWCR				
			STA	STO	TWINT	TWEA	
0x88	Previously addressed with own SLA+W; data has been received; NOT ACK has been returned	Read data byte or	0	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA
		Read data byte or	0	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if TWGCE = "1"
		Read data byte or	1	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA; a START condition will be transmitted when the bus becomes free
		Read data byte	1	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if TWGCE = "1"; a START condition will be transmitted when the bus becomes free
0x90	Previously addressed with general call; data has been received; ACK has been returned	Read data byte or	X	0	1	0	Data byte will be received and NOT ACK will be returned
		Read data byte	X	0	1	1	Data byte will be received and ACK will be returned
0x98	Previously addressed with general call; data has been received; NOT ACK has been returned	Read data byte or	0	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA
		Read data byte or	0	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if TWGCE = "1"
		Read data byte or	1	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA; a START condition will be transmitted when the bus becomes free
		Read data byte	1	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if TWGCE = "1"; a START condition will be transmitted when the bus becomes free
0xA0	A STOP condition or repeated START condition has been received while still addressed as slave	No action	0	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA
			0	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if TWGCE = "1"
			1	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA; a START condition will be transmitted when the bus becomes free
			1	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if TWGCE = "1"; a START condition will be transmitted when the bus becomes free

TWAR(I2C Address Register)를 통해 어드레스 값을 설정한다(초기값 : 0xFF)

1. I2C통신

(4) ATmega328P의 I2C통신
- Slave Receiver모드

Figure 21-16. Formats and States in the Slave Receiver Mode



Master모드처럼 TWSR로 데이터 수신 상태를 확인하고 TWCR을 설정한다.
차이점은 어드레스값 설정을 해야함!!

1. I2C통신

(4) ATmega328P의 I2C통신
- 통신 속도 설정

Bit Rate Generator Unit

This unit controls the period of SCL when operating in a master mode. The SCL period is controlled by settings in the TWI bit rate register (TWBR) and the prescaler bits in the TWI status register (TWSR). Slave operation does not depend on bit rate or prescaler settings, but the CPU clock frequency in the slave must be at least 16 times higher than the SCL frequency. Note that slaves may prolong the SCL low period, thereby reducing the average TWI bus clock period. The SCL frequency is generated according to the following equation:

$$\text{SCL frequency} = \frac{\text{CPU Clock frequency}}{16 + 2(\text{TWBR}) \times (\text{PrescalerValue})}$$

2를 곱하라는건지?

- TWBR = Value of the TWI Bit rate register.
- PrescalerValue = Value of the prescaler, see Table 21-8 on page 200.

Note: Pull-up resistor values should be selected according to the SCL frequency and the capacitive bus line load. See Table 28-7 on page 264 for value of pull-up resistor.

TWBR – TWI Bit Rate Register

Bit	7	6	5	4	3	2	1	0	
(0xB8)	TWBR7	TWBR6	TWBR5	TWBR4	TWBR3	TWBR2	TWBR1	TWBR0	TWBR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7..0 – TWI Bit Rate Register**

TWBR selects the division factor for the bit rate generator. The bit rate generator is a frequency divider which generates the SCL clock frequency in the master modes. See Section 21.5.2 “Bit Rate Generator Unit” on page 180 for calculating bit rates.

Table 21-8. TWI Bit Rate Prescaler

TWPS1	TWPS0	Prescaler Value
0	0	1
0	1	4
1	0	16
1	1	64

1. I2C통신

(4) ATmega328P의 I2C통신
- Pull-up저항 계산

통신 속도를 고려하여 풀업저항 선정!!

Table 28-7. 2-wire Serial Bus Requirements

Parameter	Condition	Symbol	Min	Max	Units
Input low-voltage		V_{IL}	–0.5	$0.3\ V_{CC}$	V
Input high-voltage		V_{IH}	$0.7\ V_{CC}$	$V_{CC} + 0.5$	V
Hysteresis of schmitt trigger inputs		$V_{hys}^{(1)}$	$0.05\ V_{CC}^{(2)}$	–	V
Output low-voltage	3mA sink current	$V_{OL}^{(1)}$	0	0.4	V
Rise time for both SDA and SCL		$t_r^{(1)}$	$20 + 0.1C_b^{(3)(2)}$	300	ns
Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF^{(3)}$	$t_{of}^{(1)}$	$20 + 0.1C_b^{(3)(2)}$	250	ns
Spikes suppressed by input filter		$t_{SP}^{(1)}$	0	$50^{(2)}$	ns
Input current each I/O pin	$0.1V_{CC} < V_i < 0.9V_{CC}$	I_i	–10	10	µA
Capacitance for each I/O pin		$C_i^{(1)}$	–	10	pF
SCL clock frequency	$f_{CK}^{(4)} > max(16f_{SCL}, 250kHz)^{(5)}$	f_{SCL}	0	400	kHz
Value of pull-up resistor	$f_{SCL} \le 100kHz$	R_P	$\frac{V_{CC} - 0.4V}{3mA}$	$\frac{1000ns}{C_b}$	Ω
	$f_{SCL} > 100kHz$		$\frac{V_{CC} - 0.4V}{3mA}$	$\frac{300ns}{C_b}$	Ω
Hold time (repeated) START condition	$f_{SCL} \le 100kHz$	$t_{HD;STA}$	4.0	–	µs
	$f_{SCL} > 100kHz$		0.6	–	µs
Low period of the SCL clock	$f_{SCL} \le 100kHz$	t_{LOW}	4.7	–	µs
	$f_{SCL} > 100kHz$		1.3	–	µs
High period of the SCL clock	$f_{SCL} \le 100kHz$	t_{HIGH}	4.0	–	µs
	$f_{SCL} > 100kHz$		0.6	–	µs
Set-up time for a repeated START condition	$f_{SCL} \le 100kHz$	$t_{SU;STA}$	4.7	–	µs
	$f_{SCL} > 100kHz$		0.6	–	µs
Data hold time	$f_{SCL} \le 100kHz$	$t_{HD;DAT}$	0	3.45	µs
	$f_{SCL} > 100kHz$		0	0.9	µs
Data setup time	$f_{SCL} \le 100kHz$	$t_{SU;DAT}$	250	–	ns
	$f_{SCL} > 100kHz$		100	–	ns
Setup time for STOP condition	$f_{SCL} \le 100kHz$	$t_{SU;STO}$	4.0	–	µs
	$f_{SCL} > 100kHz$		0.6	–	µs
Bus free time between a STOP and START condition	$f_{SCL} \le 100kHz$	t_{BUF}	4.7	–	µs
	$f_{SCL} > 100kHz$		1.3	–	µs

Notes:
1. In Atmel ATmega328P, this parameter is characterized and not 100% tested.
2. Required only for $f_{SCL} > 100kHz$.
3. C_b = capacitance of one bus line in pF.
4. f_{CK} = CPU clock frequency
5. This requirement applies to all Atmel ATmega328P 2-wire serial interface operation. Other devices connected to the 2-wire serial bus need only obey the general f_{SCL} requirement.

SCL이 100KHz 이하일 때

SCL이 100KHz 이상일 때

*Transistor 특성에 의해 Vcc전압
스위칭 속도에 영향을 줌
따라서 저항의 최소값은
Vcc를 고려하여 설정