Mobile DDR Controller for BeMicro SDK

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ARROW ELECTRONICS

1 Overview

The BeMicro SDK development board employs a low-power MDDR memory device for code and/or data storage. The component mounted is a Micron MT46H32M16LFBF-5 device, thus, a 512Mbit Mobile Low-Power DDR memory device in BGA60 package. An IP module inside the FPGA is needed to make the memory device work.

Several IP vendors offer ready-to-run modules for dynamic memory devices. The example designs used during the BeMicro SDK workshop series make use of the versatile Microtronix DRAM controller core. This controller features several access ports that can run at different clock frequencies and, because of that, is suitable for lots of different applications. Furthermore, it can be configured for different devices and device settings.

However, because of license restrictions, professional IP modules may not always the best choice for some simple handcrafted FPGA designs that are produced in very low quantities. The same applies to test designs made for BeMicro SDK. For such designs, the Arrow MDDR Controller for BeMicro SDK may be helpful.

The usage of the Arrow MDDR Controller for BeMicro SDK is free of charge or any royalties. However, it is bound to a license agreement that is part of this manual. In short form, it is allowed to use the MDDR controller core only with Altera devices and only if they have been purchased or obtained in any other legal way from Arrow or one of its subsidiary companies.

2 System description

2.1 Memory Component

The Arrow MDDR Controller for BeMicro SDK only supports the Micron MT46H32M16 device. This is the device that is mounted on the BeMicro SDK.

2.2 Internal Interface

The Arrow MDDR Controller for BeMicro SDK features one single Avalon MM slave interface.

3 Installation

The steps listed below are necessary to make the controller and therefore the memory device work.

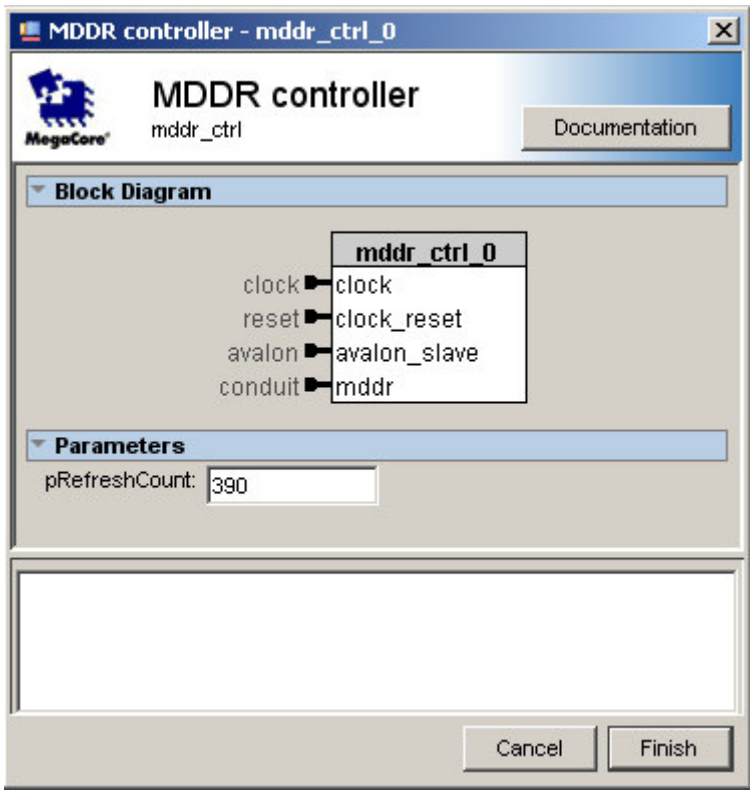
- Create a folder named ip in the Altera Quartus working folder of your FPGA design if the folder not already exists.
- Create a folder named arrow_mddr_ctrl in the folder ip.
- Copy the ZIP archive arrow_mddr_ctrl.zip to the folder arrow_mddr_ctrl and extract the archive there. You should get five files.

File name	Content
mddr_ctrl.v	Verilog source code
top_level_example.v	Verilog sample instantiation
mddr_ctrl_hw.tcl	TCL file for SOPC builder
mddr_ctrl.sdc	Timing constraint file
BeMicro_SDK_MDDR_ctrl.pdf	User manual and license agreement

Now, the controller is ready for use.

4 Instantiation using SOPC builder

After installation, the MDDR controller appears in the project part of the component library of the SOPC builder. It can be added to a SOPC system in the same way as other components. When adding it, a parameterization window pops-up.



4.1 Parameterization

The parameter pRefreshCount defines the refresh period of the controller. According to the specification, the memory device used requires an average periodic refresh interval (t_{REFI}) of 7.8 us maximum. You have to calculate the value of the parameter pRefreshCount based on the frequency of the clock that drives the clock input of the MDDR controller.

pRefreshCount = clock frequency * average periodic refresh interval

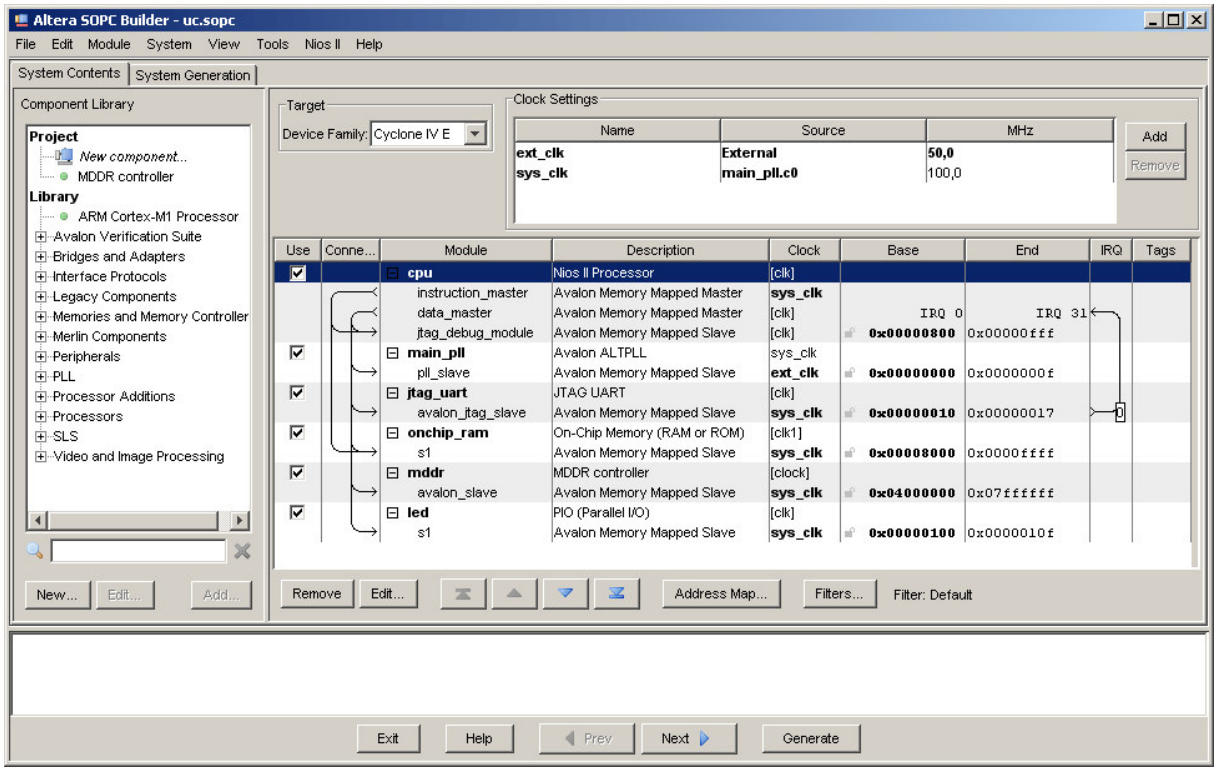
Examples:

```
clock frequency = 50 MHz
pRefreshCount = 50 * 1E6 * 1/s * 7.8 * 1E-6 s = 390

clock frequency = 100 MHz
pRefreshCount = 100 * 1E6 * 1/s * 7.8 * 1E-6 s = 780
```

If the parameter pRefreshCount is set to a value lower than the required value then the refresh cycles occur more often than necessary. This consumes some memory bandwidth and increases the power consumption, but the device will work properly. Setting the parameter to a value higher than required may lead to memory content loss. This must be avoided, so be sure not to set the parameter to a value higher than calculated. In case the frequency changes during runtime use the lowest frequency for the calculation of the parameter pRefreshCount.

At the end, your SOPC might look like this:



4.2 Timing requirements

After the controller has been added to an SOPC system the system must be generated. Then, before compiling the FPGA, the SDC file containing the timing constraints has to be adjusted. First, add the SDC file to the list of SDC files to be processed. Then use an editor to modify the data in the first section of the SDC file according to your needs. Detailed information about that can be found in the comment lines of the SDC file.

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6 Document history

2011-09-06: Initial release.