Lab 9

Using LTspice Simulation Software to Simulate a Digital Circuit

Introduction:

In this laboratory exercise you will use software to simulate the circuit action of the furnace controller you designed and built in an earlier laboratory exercise. This lab is written assuming that you will use the LTspice IV (Linear Technology SPICE) program for "schematic capture" and circuit simulation. Linear Technology is an integrated circuit manufacturer that developed an easy-to-use version of the SPICE circuit-simulation program. The first version of SPICE (Simulation Program with Integrated Circuit Emphasis) was introduced in 1973.

Schematic capture is the process of using a computer aided design (CAD) program to draw the electronic schematic on the display of a computer and then save the schematic as a file. The circuit simulation feature will be used to show the output signals of the circuit in relation to the input signals using a timing diagram format. CAD programs that are designed specifically for electronic circuits are known as EDA (electronic design automation) programs.

Procedure:

1. To perform schematic capture and simulation of your furnace controller (or any other design) you will proceed through the following steps (see page 8 of this lab for an example schematic created using LTspice):

    1. The appropriate electronic parts must be "placed" onto the schematic
    2. Wires must be drawn to interconnect the parts
       (parts placement and interconnection can be done in an iterative manner)
    3. A "stimulus" for the circuit must be created (e.g., a clock signal)
    4. The wires in the schematic whose voltage (or current) are to be reported in the simulation results (e.g., a timing diagram) must be selected for viewing
    5. The parameters for the simulation must be established (e.g., the amount of time for which the circuit is to be simulated)
    6. The circuit is simulated and the results analyzed

2. Begin this process by executing the LTspice program so that you can perform “schematic capture” of your furnace controller design:

    Click **Start > Programs > LTspice IV**

    To create a **new** schematic, **click the left-most button (icon) on the toolbar** (the icon is a sheet of paper with a red circular symbol (when the pointer is on the button/icon, the button hint is “New Schematic”)).

    To open an **existing** schematic, **click the ‘open-folder’ button on the toolbar** (the button hint is “Open”). The schematic file must have an extension of ‘**asc**’ and can be stored in the “LTspiceIV” folder.

To give a new schematic a file name (or create a new file name for an existing schematic):

Click **File > Save As**

And then enter the desired file name (e.g., **Lab9** (with an extension of **asc**)) into the 'File name' box – and then click 'Save'.

As you create your schematic you should periodically **click the 'Save' button on the toolbar** (the icon is a floppy disk).

After you click the "New Schematic" button on the toolbar, or open an existing schematic, the main window of the LTspice program will change from dark gray to light gray – the light gray indicates the program is ready to operate.

One-by-one you will need to 'place' and 'interconnect' the counter (74193) and the gates that create the signals **Gas** and **Fan**. The techniques to select, place, and interconnect parts are given below.

The furnace controller laboratory exercise shows either a 555 timer circuit or a function generator driving the clock input of the 74193 counter. Although you can simulate the 555 timer circuit, it will be easier to drive the clock input of the counter with a clock signal generated within the simulation program (i.e., a voltage source with a 'pulse' specification).

Important notes:

1. If the 74193 counter is not available within the simulation program then use the **74HCT161 four-bit counter with its input signals ENT (or CET), ENP (or CEP), LOAD! (or PE!), and CLR! (or R!) (! = NOT) all wired to logic '1' (use a voltage source set to 5v to create a logic '1')**
2. The clock signal will be created by a **voltage source set to 'pulse' mode** (the details of how to select a voltage source and set its mode will be given shortly)
3. Any digital input that is to be at a **logic '0'** should have a **ground connection** wired to that input
4. Any digital input that is to be at a **logic '1'** should have a **voltage source set to 5v** wired to that input
5. The simulator program assumes that any logic part that requires power is wired to an appropriate power source (i.e., you do **not** need to show power being wired to any logic IC).

To create a schematic you will need to "add" and then "place" (i.e., position) "parts". As you add and place parts you will also draw wires so as to interconnect the pins of the parts as dictated by your design. Each time you attempt to add a part to your schematic, you must search for your desired part within the "parts libraries" that are available for your use.

You will use digital ICs (gates and the 74HCT161 counter) from the "**74HCT**" digital IC library. To do so requires that the 74HCT library files must be loaded into the appropriate folders for use by LTspice.

Using your schematic from Lab 6, begin the schematic capture process by placing the counter, and then the gates, onto a schematic using LTspice. Directions for selecting a part, creating wires, moving parts, deleting parts, etc. are given below.

To add a part (e.g., a gate/counter/voltage source/etc.) to your schematic:

+Click the **'AND gate' button** on the toolbar (button hint: 'Component') to bring-up the 'Select Component Symbol' window
+Every name that appears within square brackets (e.g., **[74HCT]**) is a 'library' of parts (components) within that group – the library names are followed by the names of non-IC generic parts (including the **'voltage'** source (near the end of the listing))
+If you want a part from the 74HCT digital library, then double-click **[74HCT]** and then click (to select) the IC you desire
(many of the ICs have a regular version and a second 'i' version – which use the IEEE Std. 91-1984 'dependency notation' symbology, which is not commonly used (e.g., gates are drawn as square boxes with a symbol used to indicate the type of gate (an AND gate uses a '&' within the box, an OR gate uses a '≥' within the box))
-OR-
If you want a voltage source (or other non-IC generic part) click (to select) the name of the part you desire (e.g., click 'voltage')
+Click **'OK'** (to finalize your part selection)
+Position the part where desired
+**Left click** to place part and then:
*If two or more of these parts are desired then repeat the part positioning/left click process as needed
*When done, **right click to end**

To delete an object:

+Click the **'Scissor' button** on the toolbar (button hint: 'Cut')
+Position the pointer on the object to be deleted and **left click** to delete (and repeat as desired)
+Right click to end

To move an object:

+Click the **'Open Hand' button** on the toolbar (button hint: 'Move')
+Click the item to be moved
+Move the pointer to reposition the item as desired
+When item is in the desired position, **left click** to place item
+Right click to end

To make a connection to logic '0' or logic '1':

For a logic '0':
+Click the **'Ground' button** on the toolbar (button hint: 'Ground') and then place the ground as desired (left click to place/right click to end)

For a logic '1':
+Click the **'And' gate button** on the toolbar to bring up the 'Select Component Symbol' window
+Click the **'voltage'** component / Click **'OK'**
+Place the voltage source where desired then left click/right click
+With the pointer on the voltage source, right click to bring up the 'Voltage Source' specification window
+Enter 5.0 into the 'DC value(V):' field (you can leave the 'Series Resistance(Ω):' field blank)
+Click **'OK'**

To draw a wire between parts:

+Click the **'Pencil' button** on the toolbar (button hint: 'Wire')
+Position the pointer where a wire is to start and then **left click**
+Move pointer to where the wire should end (or make a 90-degree turn) and **left click** (repeat as needed to get to where the wire should end)
+Right click to end

Note: If a wire is drawn into a midpoint of an existing wire, a "connection dot" (or "junction") is automatically created

To create a clock signal:

+Click the **'AND gate' button** on the toolbar and select the **'voltage'** component, position the voltage source as desired, left click/right click
+With the pointer on the voltage source, right click to bring up the 'Voltage Source' specification window
+Click **'Advanced'** (to bring-up the 'Independent Voltage Source' window)
+Select **'PULSE'** and then enter the values as follows:

Vinitial(V):	**0**	('Low' voltage will be 0 volts)
Von(V):	**5**	('High' voltage will be 5 volts)
Tdelay(s):	**0**	
Trise(s):	**1n**	(Trise = 'Rise time' and Tfall = 'Fall time',
Tfall(s):	**1n**	1n = 1 nanosecond (do not enter 0 for Trise or Tfall, as it will cause a very slow rise/fall))
Ton(s):	**0.5m**	(The 'high' time during each cycle is 0.5 milliseconds = 0.5 msec)
Tperiod(s):	**1m**	(The time for each cycle is 1 msec) (which results in a frequency of 1 kHz))
Ncycles:	**18**	(Number of clock cycles to create – the furnace controller's output signals repeat after every 8 clock cycles, so it would seem that we need to simulate just 8 clock cycles – however, we might desire to view the counter's QD output and there is a slight undesirable aspect to LTspice's timing diagram presentation that necessitates one or two extra clock cycle)

+Click **'OK'**

The above specifications will create a clock signal alternating between 0 volts and 5 volts with a period of 1 millisecond (resulting in a frequency of 1,000 Hz = 1 kHz), a 'high' time of 0.5 milliseconds per cycle, for 18 clock cycles.

To give a wire a "signal name":

+ Click the '**A**' **button** on the toolbar (button hint: 'Label Net')
+Enter the desired signal name into the net name field
+Click **'OK'**
+Position the signal name such that it is touching the appropriate wire in the schematic and then **left click** (you can repeat if you desire this signal name at multiple places along the wire)
+Right click to end

Note: Naming important wires in a schematic clarifies the schematic and also clarifies the signals presented in the simulation results (i.e., timing diagrams)

To prepare for simulating the circuit:

LTspice was designed for simulating analog circuits where timing diagrams often have all the signals superimposed on the same voltage scale (y axis). However, timing diagrams for digital circuits need to have the signals separated (along the y axis) since all the signals are alternating between the same voltages (0v and 5 volts) and if the signals were superimposed, it would be very difficult to differentiate one signal from another. LTspice has two components that allow signals that alternate between the same voltages to be separated (vertically) so that it is visually easy to see how a given signal changes relative to one or more other signals. Signals that are to be separated vertically on the timing diagram must be connected to the inputs of either of these parts and it is the corresponding outputs of these parts that should be displayed for the simulation results. The 'DVIEW5' part allows for up to 5 signals to be displayed and the 'DVIEW10' part allows for up to 10 signals to be displayed.

+Click the **'AND gate' button** on the toolbar and then double-click the **[Digital]** library
+Click the **'DVIEW10'** part name (to select) and then click **'OK'**
+Position the part as desired then left click/right click

Now create an individual wire between each of the following signals, in your schematic, and the indicated input of the 'DVIEW10' part as follows:

1. **CLOCK to DVIEW input 1**
2. **QC (Q2) of 74HCT161 to DVIEW input 2**
3. **QB (Q1) of 74HCT161 to DVIEW input 3**
4. **QA (Q0) of 74HCT161 to DVIEW input 4**
5. **Gas output of your logic to DVIEW input 5**
6. **Fan output of your logic to DVIEW input 6**

Note: The order of the connections to the DVIEW part determines the order of the displayed signals in the timing diagram

Now create individual short **wires from DVIEW outputs 1 – 6 where each wire goes from a DVIEW output for a short distance to the right** (where it will not be connected to anything). Now create a meaningful **'signal name'** for each of these wires where each signal name **touches** its wire (e.g., use the following signal names: **CLOCKx**, **Hx**, **Wx**, **Tx**, **Gasx**, and **Fanx**). (Note: The **x**'s have been added since two different wires cannot have the same signal name and you have likely already used CLOCK/H/W/T/... to the left of DVIEW)

Next, you need to tell the simulation portion of LTspice where to find the 'models' for the internal operation of the 74HCT ICs that you have used.

+Click the **'.op' button** on the toolbar (button hint: 'SPICE Directive')
+Type **.lib 74hct.lib** then press control-M (while holding down the Control key, press the 'M' key (to make a new line)) then type **.lib dview.lib** (note that both directives start with a period (.))
+Click **'OK'**

Your two directives should now appear somewhere on the schematic.

To simulate the circuit:

+Click 'Simulate' on the menu bar
+Click 'Edit Simulation Cmd' in the drop-down menu
+Enter **16m** (for 16 msec) into the '**Stop Time:**' field
+Enter **7m** (for 7 msec) into the '**Time to Start Saving Data:**' field
+Click **'OK'**

You should now see a .tran (i.e., transient) directive somewhere on your schematic.

The goal is to simulate the furnace controller logic for 8 clock cycles. One might think that 0 should be entered into the 'Time to Start Saving Data:' field and 8m should be entered into the 'Stop Time:' field as this would simulate 8 milliseconds which equates to 8 clock cycles (since there is 1 millisecond per clock cycle, as entered into the voltage source specification for the clock signal). However, with these values, LTspice will start the counter in state 1 (not state 0, as desired). As such, we 'delay' the start time for recording data until the counter rolls over to state 0 (in terms of counter outputs QA/QB/QC), which occurs at 7 milliseconds – and we continue recording simulation data until 16 milliseconds (for 9 milliseconds of simulation data – which allows us to see the counter go from state 0 to state 7 and then back to state 0).

To perform the simulation and get a timing diagram of the results:

+Click the **'Runner' button** on the toolbar (button hint: 'Run')
(or click 'Simulate' on the menu bar then click 'Run')

You should now see the LTspice window divided into two sub-windows – one sub-window shows your schematic and the other sub-window shows a timing diagram (with no signals being displayed).

To display signals onto the timing diagram, you need to place **'voltage probes' (also known as 'voltage markers')** on the wires in the schematic that you want reported on the timing diagram. To do so:

+Position the pointer on the **wire** connected to **DVIEW output 1 (CLOCKx)** (**the pointer will change to a red voltage probe when the pointer is on a wire**) **and click**
+One-by one, do the same operation for the wires connected to DVIEW outputs 2 - 6

As you click signals (creating 'voltage probes'), the signals will be added to the timing diagram in the order they occur on the outputs of the DVIEW part. Note that the voltage scale on the left side of the timing diagram is meaningless. Also, if you had not used the DVIEW10 part, and directly displayed the above signals, they would all be on top of each other in the timing diagram – a virtually useless presentation.

Special note: After simulating, if you position the pointer **on** a **pin** of a device (not a wire), the pointer will change to a **black current probe (it will have a circular clamp instead of a needle at the end (as voltage probes have))**. In this lab there is no need for any current probes as we are interested in voltages, not currents.

You should carefully examine the timing diagram to verify that the displayed results for the signals **Gas** and **Fan** are correct in relation to the counter signals **QC, QB, and QA**. Also, carefully note the signals QC/QB/QA in relation to each other. You should see that they begin by displaying the counter being in **state 0** (for one clock cycle) – followed by **state 1** (for one clock cycle) – **...** followed by **state 7** (for one clock cycle) which is then followed by **state 0**. You may wish to have your lab instructor verify that your simulation is correct.

If any of the signals are not correct, you must determine, and correct, whatever is causing the discrepancy.

To save your schematic in a file:

+Click the toolbar item that resembles a floppy disk

The last step is to make the 'unit numbers' (the 'U' number at the top of each device) of your devices consistent. That is, the unit numbers should progress from U1 to the highest numbered unit without skipping any numbers (e.g., if your design requires three ICs then three units are required – U1, U2, and U3).

Note that if you are using 2-input NAND gates (7400 (or **74HCT00**)), there are four 2-input NAND gates per 7400 IC. As such, each 7400 IC has **subunits A, B, C, and D** (subunit A has input pins 1 and 2 and the output is pin 3, subunit B has input pins 4 and 5 and the output is pin 6, etc.). Assume a schematic requires three 2-input NAND gates – they would all have the same unit number (since only one IC is needed), but with different subunit designations (e.g., **U2A**, **U2B**, and **U2C**). In most schematic capture programs, when you change the subunit designation for a device (that belongs to an IC with subunits), the pin numbers on the schematic symbol for the device change to the appropriate pin numbers for that subunit. However, LTspice does not show pin numbers.

Make sure the unit numbers on your schematic meet the desired characteristics stated above.

To change the unit designation (or add/change a subunit designation) of a part:

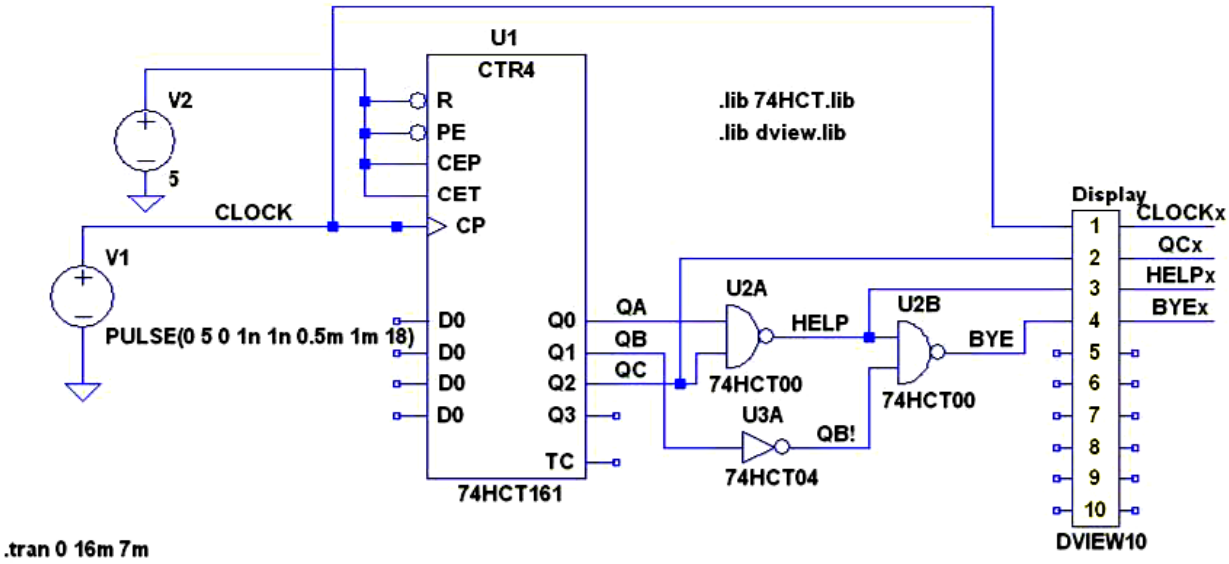
+Position the pointer on top of the unit designator of a part
+Right click
+Enter the desired unit/subunit designation
+Click **'OK'**

Note: Voltage sources should have unit designators of V1, V2, etc.

Make sure your schematic and simulation results conform to the following:

1. All signals appearing in the timing diagram must have meaningful names
2. Each IC in the schematic should have a unique "unit number" (e.g., U1, U2, etc.) and the unit numbers should progress from U1 to the highest numbered unit without skipping any numbers (e.g., if your design requires three ICs then three units are required - U1, U2, and U3)
   (gate-type ICs (e.g., 7400, 7404, etc.) identify the individual gates within the unit as subunit 'A', subunit 'B', etc. (e.g., if your design requires three two-input NAND gates then use subunits A, B, and C within one 7400 IC (e.g., U2A, U2B, and U2C) instead of using the first sub-unit within three different units (e.g., U2A, U3A, and U4A)))
3. The timing diagram should have the **CLOCK signal** on top, then the **input signals** (to the furnace controller – **QC (H), QB (W),** and **QA (T)**), and finally the **output signals** (**Gas** and **Fan** below the input signals)

Example schematic created using LTspice (this schematic illustrates the use of several parts that you will need to use in your schematic):



The schematic file that corresponds to the above schematic can be downloaded from www.spot.pcc.edu/~ghecht (search for a link to the file Lab9Example.asc). After downloading the file, it can be opened in LTspice and simulated (assuming the 74HCT library has been loaded into LTspice).