FPGA Based Digital Pulse Width Modulation Using Xilinx DCM For Motor Controlling

Rijo Baby
Electronics And Communication Engineering (B.E)
St.Anne's College of Engineering And Technology
Panruti India

Abstract: - **PWM signal have a major role in digital electronics. It generates variable-width pulses to represent the amplitude of an analog input signal. .Although it consider as ON OFF stages. In this paper specified for controllingPWM signal by a fast and reliable new method and also its reduce the area, complexity and power consumption with low cost .FPGA based Xilinx digital clock manager (DCM) synchronized clock pulses can effectively control the DPWMsignals, and from the implementation of this method we can control the motors used in industrial level applications like in robotics fast movement motors, solar control tracker, industrial motors, hydraulic valve etc. This proposed hybrid module uses a synchronous counter-based comparator block and a DCM based fine-resolution block implementing a synchronous delay line using delay flip flop. The design was successfully implemented on a low-cost Xilinx Spartan-3E FPGA kit.**

Keywords: *DCM, FPGA, DPWM*

1 INTRODUCTION

Pulse width modulation is a modulation technique in which the pulse width is changes with respect to the time.[1] Digital device can easily work with inputs and outputs that have only two states, on and off. So it easily uses to control a LED's state i.e. ON or OFF. In the same way use it to control any electrical device ON/OFF by using proper drivers (transistor, triac, relays etc.). But sometimes you need more than just "ON" & "OFF" control over the device if control the brightness of a LED or the speed of DC motor then digital (ON/OFF) signals simply can't do it. This situation is very smartly handled by a technique called PWM or Pulse Width Modulation. In this paper proposing architecture that makes fast and reliably control the pwm signal. And it implements into the low cost and simplest FPGA Spartan family.by this module we can easily control the motor or switchconditions .The rapid rising and falling edges ensure that devices are turned on or off as fast as practically possible to minimize the switching transition time[2].Although other considerations, such as parasitic ringing and electromagnetic interference (EMI) emission to be avoided.[3]The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero[4]. PWM also works well with digital controls, which, because of their ON/OFF nature, can easily set the needed duty cycle.a DCM Fig.1 like digital frequency synthesis (multiplier/divider), duty-cycle correction, programmable phase shifter, programmable duty-cycle synthesizer and coarse phase shifter[5].Several FPGA-based solutions have also been proposed in the literature. One common solution is to use a coarse resolution counter-based stage plus one or several on-chip digital clock manager (DCM) blocks. The coarse phase shifter provides the outputs as CLK0, CLK90, CLK180 and CLK270. The output also depends on the duty_cycle_correction input. The PWM signal is set at the beginning of the counter period, and it is reset after a given number of clock cycles plus a certain fraction of the clock period established by the DCM[6].

Several FPGA-based configuration scenarios are studied. A series of tests including design and timing-precision analysis were conducted to discuss and validate the obtained hardware architectures[7].While FPGAs used to be selected for lower speed/complexity/volume designs in the past, today's FPGAs easily push the 500MHz performance barrier. Implemented using Field Programmable Gate Array (FPGA) controller, Better performance and cost reduction and it madeSuitable for power supply applications. The digital realization of the control circuits improves the efficiency and reduces the cost.The FPGA design flow eliminates the complex and time-consuming floor planning, place and route, timing analysis, and mask / re-spins stages of the project since the design logic is already synthesized to be placed onto an already verified, characterized FPGA device[8]. The Spartan 3E Starter Board provides a powerful and highly advanced self-contained development platform for designs targeting the Spartan 3E FPGA from Xilinx. The Spartan®-3 Generation of FPGAs offers a choice of five platforms, each delivering a unique cost-optimized balance of programmable logic, connectivity, and dedicated hard IP for your low-cost applications.it have 500K gate Spartan 3E FPGA with a 32 bit RISC processor and DDR interfaces. Xilinx software can perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.The core generator will have a much importance in generation of DCM.

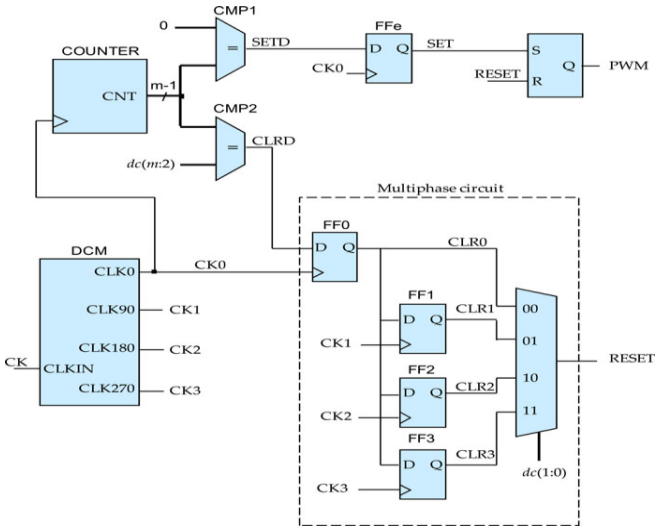

Fig.2 proposed module

I. DEVELOPING PROCESS:

Proposed module showing in the Fig.2 this architecture is called DMC based DPWM controller. The DCM generated by a core generator. Feature of phase shifting it produce four different types of phase different CLK pulses .clk0, clk90, clk180, clk270. The CLK 0 taken as a major CLK signal and the positive edge counter starts the counting. The first edge consider as reset. The m-1 counter value compared with the external giving pulse dc(m:0). "CNT" has $m-1$ bits. "CLRD" signal is set when the $m-1$ most-significant bits (MSBs), dc(m:2), are equal to CNT; and SETD signal is set when CNT is equal to zero and dc(m:2) is different from zero. Fig. 4 shows how the circuit works with m = 4, and dc = "1001". Basically, when the counter CNT is equal to the $m-1$ MSBs of the duty command dc, signal CLRD activates. The resulting pulse is captured in the next clock cycle by FF0, and phase shifted 90◦, 180◦, and 270◦ by flip-flops FF1, FF2,and FF3, respectively. These four FFs implement a multiphase synchronous circuit [9]. The two least-significant bits (LSBs) of the duty command are used by the multiplexer to select the phase-shifted signal that clears the SR latch. The advantage of this proposal in relation to others is that the digital circuit that generates the reset of the SR latch is synchronous. The use of asynchronous circuits to reset the latch makes harder to calculate timing using static timing analysis and can result in glitching since controlling the logic and routing delays in an FPGA is more difficult than in ASIC implementations.

A. SoftwareImplementation:

Starting with generation of DCM using core generator in Xilinx, to write individual coding for every component and write top module which calling all components include DCM module written with Verilog coding then simulate both behavioral and ISE simulator using Xilinx simulation tool. The simulatedresults show that PWM controlled output wave form.For getting wave form needs to force values. Theentries architecture there is four inputs and one output. Other CLK are generated by DCM. So forcing the input values. First reset must be in HIGH because to starting of the device reset function is in needed. When reset =HIGH PWM =0 reset =low get the PWM controlled output wave form here showing fig. dc ='11001'.Fig .3 shows the simulated wave form.

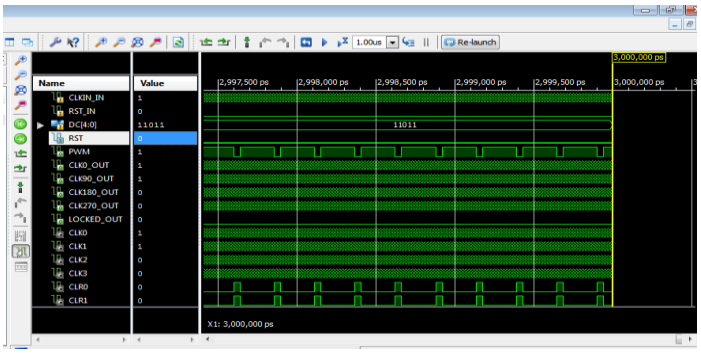

Fig.3 controlled PWM(simulated output)

B. Hardware implementation:

For hard ware implementation needs to download the Verilog coding to the FPGA kitthrough Xilinx ISE simulator tool. Spartan 3e is the FPGA kit which is used for implementation in this paper showing the controlled PWM can use for motor control. To connect 5v DC motor to the I/O ports of kit and through the control channels give inputs and analyzing the variation of the speed of motor.Fig.4 shows hard ware implementation.

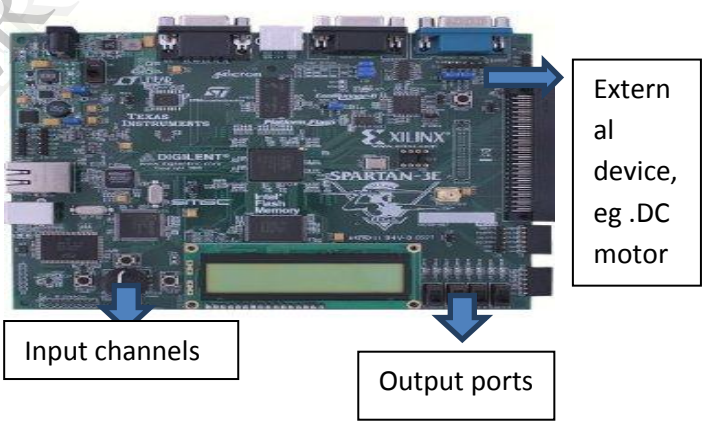

Fig.4 hardware implementation in FPGA kit

C. Application and advantages:

Controlling PWM architectures are many more in industry. This module leads more categories like using synchronous CKL we can reduce the glitching effect so the switching power loss reduced. FPGA Spartan 3e kit reduces the complexity, cost, and power conception. And this method giving high resolution, and switching frequency, up to 625 ps speed of motor. Major thing is easy to control the PWM signal. So these advantages are helps to implement the module into lots of practical applications. Like industrial motor speed controlling, power convertors[9], robotics in robotics the DC motors wants high controlling .another attractive area is solar tracking control .solar tracking control like MMPT we can implement PWM. Major draw backs of

MMPT is high cost, complex circuit, with the high controlling with constant frequency can choose PWM method for the solar cell tracking controlled and the another one use is to control the hydraulic valve control the major working is to controlled valve we can control the flow of liquid .so the controlling of PWM we can implement lot of applications.

II. CONCLUSION:

Advances in power electronics and digital control have made necessary the development of high-resolution DPWM.The DCM-based architecture can be implemented using the resources present in low-cost FPGAs, and the maximum clock frequency is determined by the DCMs instead of the multiphase circuit. The experimental results show a resolution of 625 PSfor the DCM-based architecture and it shows more efficiency in avoiding glitching and power loss. The controlled output can use in many of the industrial applications. The future enhancements are going on research.

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