Instruction	RegSource	RegWr	Extender_Op	ALU_Src	Mem_Rd	Mem Wr	
R_Type		0	1	x	0	0	0
SLLI		0	1	x	1	0	0
SRLI		0	1	x	1	0	0
SRAI		0	1	x	1	0	0
RORI		0	1	x	1	0	0
ADDI		0	1	1	1	0	0
SLTI		0	1	1	1	0	0
SLTIU		0	1	0	1	0	0
SEQI		0	1	1	1	0	0
XORI		0	1	0	1	0	0
ORI		0	1	0	1	0	0
ANDI		0	1	0	1	0	0
NORI		0	1	0	1	0	0
SET		x	1	1	1	0	0
SSET		x	1	x	1	0	0
JALR		0	1	1	1	0	0
LW		0	1	1	1	1	0
SW		0	0	1	1	0	1
BEQ		0	0	1	0	0	0
BNE		0	0	1	0	0	0
BLT		0	0	1	0	0	0
BGE		0	0	1	0	0	0
BLTU		0	0	1	0	0	0
BGEU		0	0	1	0	0	0

Mem_to_Reg	PC_Src	Branch	Jump	imm_select
00	11	0	0	x
00	11	0	0	x
00	11	0	0	x
00	11	0	0	x
00	11	0	0	x
00	11	0	0	0
00	11	0	0	0
00	11	0	0	0
00	11	0	0	0
00	11	0	0	0
00	11	0	0	0
00	11	0	0	0
00	11	0	0	0
00	11	0	0	0
00	11	0	0	0
10	10	0	1	0
01	11	0	0	0
x	11	0	0	1
x	01	1	0	1
x	01	1	0	1
x	01	1	0	1
x	01	1	0	1
x	01	1	0	1
x	01	1	0	1