The NEORV32 Processor

by Dipl.-Ing. Stephan Nolting

A customizable, lightweight and open-source
32-bit RISC-V soft-core microcontroller.

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The **NEORV32 Processor** Project
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1. Overview

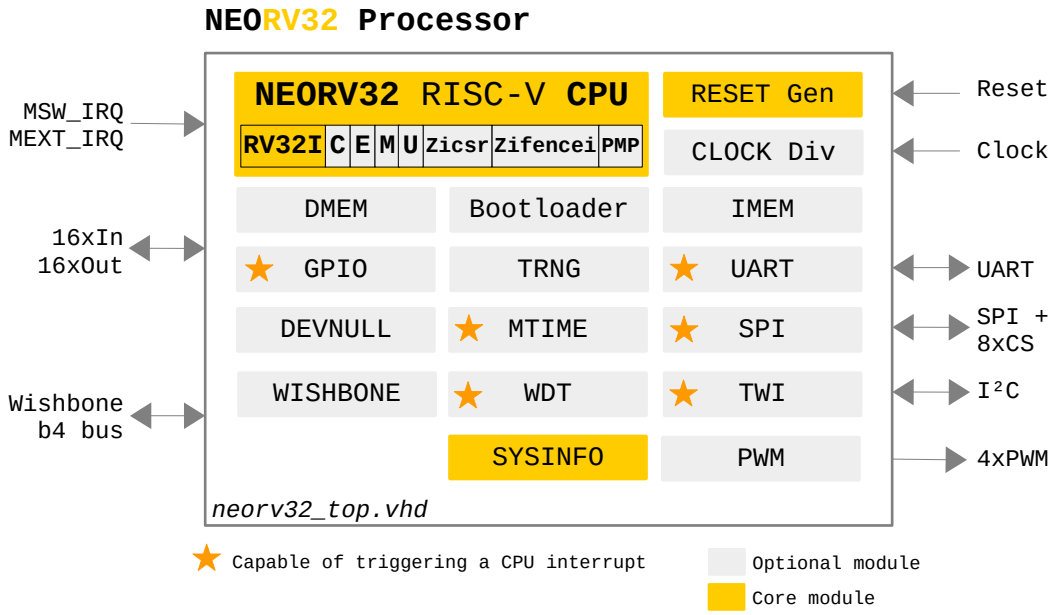

Figure 1: NEORV32 processor block diagram

The **NEORV32**[1] **processor** a customizable full-scale mikrocontroller-like processor system based on the RISC-V-compliant `rv32i` **NEORV32 CPU** with optional `M`, `E`, `C` and `U`, `Zicsr`, `Zifencei` and PMP (physical memory protection) extensions. The CPU was built from scratch and is compliant to the *Unprivileged ISA Specification Version 2.2* and a subset of the *Privileged Architecture Specification Version 1.12-draft*. The non-compliant issues can be found in chapter 1.4.1 RISC-V Non-Compliance Issues.

The **processor** is intended as auxiliary processor within a larger SoC designs or as stand-alone custom microcontroller. Its top entity can be directly synthesized for any FPGA without modifications and provides a full-scale RISC-V based microcontroller with common peripherals like GPIO, serial interfaces for UART, I²C and SPI, timers, external bus interface and embedded memories. All optional features beyond the base CPU can be enabled and configured via VHDL generics.

Alternatively, you can use the **NEORV32 CPU** as stand-alone central processing unit and build your own microcontroller or processor system around it.

This project comes with a complete software ecosystem that features core libraries for high-level usage of the provided functions and peripherals, application makefiles, a runtime environment and several example programs. All software source files provide a doxygen-based documentary.

The project is intended to work "out of the box". Just synthesize the test setup from this project, upload it to your FPGA board of choice and start playing with the NEORV32. If you do not want to compile the GCC toolchain by yourself, you can also download pre-compiled binaries for Linux.

Quickstart: Jump directly to the **5. Let's Get It Started!** chapter to get started.

1 Pronounced "*neo-R-V-thirty-two*" or "*neo-risc-five-thirty-two*" in its long form.

1.1. Design Principles

I've worked on and with several soft-core architecture. And I have studied even more of them. There are so many good projects on GitHub: Great processor designs and projects with the best of intentions. Unfortunately, many of them lack a good documentation, that covers everything down from the rtl level to the software library and how all the parts get together.

➔ **From zero to main(): Completely open source and documented.**

Everyone uses different FPGAs and evaluations boards. This variety is a good thing. Though, it can be quite frustrating if you have to dig into the deepest corners of a HDL project if you just want to do a quick test synthesis for your FPGA board.. This project comes in a technology-independent form. Nevertheless, it also provides *optional alternative* components, that are tailored to specific FPGAs.

➔ **Plain VHDL without technology-specific parts like attributes, macros or primitives.**

I just talked about it. Sometimes you just want to check out a project. This project also tries to be useful for beginners, too.

➔ **Easy to use – working out of the box.**

Some of the open-source processors out there have nice CPI and benchmark parameters. But at least some of these architectures have quite unrealistic memory interfaces (read response within the same cycle) most memories cannot provide. Also, I do not like asynchronous interfaces (some of them even require latches) and clock gating to halt certain parts of a circuit.

➔ **Clean synchronous design, no wacky combinatorial interfaces.**

Probably we all are fanboys/girls/you-name-it of a specific FPGA architectures, toolchains or manufacturers. All FPGA vendors out there have their individual benefits, but I really like the Lattice iCE40 FPGAs. They are so tiny and have a very clean and simple architecture (no fancy multiplexers and stuff like that). The large embedded memory blocks are a nice extra.

➔ **The processor has to fit in a Lattice iCE40 UltraPlus 5k FPGA running at 20+ MHz.**

1.2. Citing

If you are using the NEORV32 in some kind of publication, please cite it as follows:

```
S. Nolting, "The NEORV32 Processor", github.com/stnolting/neorv32
```

1.3. Processor Key Features

- 32-bit `rv32i` RISC-V-compliant base CPU (→ p.28)
  - Optional `C` extension for compressed instructions
  - Optional `E` extensions for embedded CPU version
  - Optional `M` extension for multiplication and division instructions
  - Optional `U` extension for user mode privilege level
  - Optional `Zicsr` extension for control and status register access and exception/interrupt system
  - Optional `Zifencei` extension for instruction stream synchronization
  - Optional Physical Memory Protection (PMP)
- Toolchain based on free RISC-V GCC port; prebuilt toolchains available (→ p.69)
- Application compilation based on GNU makefiles (→ p.71)
- Doxygen-based documentation of the software framework (→ p.87); the automatically deployed version is available at https://stnolting.github.io/neorv32/files.html
- Completely described in behavioral, platform-independent VHDL – no primitives, macros, etc. used
- Fully synchronous design, no latches, no gated clocks
- Small hardware footprint and high operating frequency (→ p.23)
- Highly customizable processor configuration (→ p.16)
- Optional processor-internal data and instruction memories (**DMEM/IMEM** → p.Fehler: Verweis nicht gefunden)
- Optional internal **bootloader** with UART console and automatic SPI flash boot option (→ p.74)
- Optional machine system timer (**MTIME** → p.55), RISC-V-compliant
- Optional universal asynchronous receiver and transmitter (**UART** → p.56)
- Optional 8/16/24/32-bit serial peripheral interface controller (**SPI** → p.58) with 8 dedicated CS lines
- Optional two wire serial interface controller (**TWI** → p.60), compatible to the I²C standard
- Optional general purpose parallel IO port (**GPIO** → p.52), 16xOut, 16xIn
- Optional 32-bit external bus interface, Wishbone b4 compliant (**WISHBONE** → p.50)
- Optional watchdog timer (**WDT** → p.53)
- Optional PWM controller with 4 channels and 8-bit duty cycle resolution (**PWM** → p.62)
- Optional GARO-based true random number generator (**TRNG** → p.64)
- Optional dummy device; provides advanced simulation console output (**DEVNULL** → p.66)
- System configuration information memory to check HW config. by software (**SYSINFO** → p.67)

1.4. RISC-V Compliance

The processor passes the official RISC-V compliance test. The port of this test suite for the NEORV32 can be found in the neorv32_compliance_test GitHub repository.

RISC-V `rv32i` Tests

```
Check                 I-ADD-01 ... OK
Check                I-ADDI-01 ... OK
Check                 I-AND-01 ... OK
Check                I-ANDI-01 ... OK
Check               I-AUIPC-01 ... OK
Check                 I-BEQ-01 ... OK
Check                 I-BGE-01 ... OK
Check                I-BGEU-01 ... OK
Check                 I-BLT-01 ... OK
Check                I-BLTU-01 ... OK
Check                 I-BNE-01 ... OK
Check          I-DELAY_SLOTS-01 ... OK
Check               I-EBREAK-01 ... OK
Check                I-ECALL-01 ... OK
Check            I-ENDIANESS-01 ... OK
Check                   I-IO-01 ... OK
Check                 I-JAL-01 ... OK
Check                I-JALR-01 ... OK
Check                 I-LB-01 ... OK
Check                I-LBU-01 ... OK
Check                 I-LH-01 ... OK
Check                I-LHU-01 ... OK
Check                I-LUI-01 ... OK
Check                 I-LW-01 ... OK
Check         I-MISALIGN_JMP-01 ... OK
Check        I-MISALIGN_LDST-01 ... OK
Check                I-NOP-01 ... OK
Check                 I-OR-01 ... OK
Check                I-ORI-01 ... OK
Check             I-RF_size-01 ... OK
Check            I-RF_width-01 ... OK
Check               I-RF_x0-01 ... OK
Check                  I-SB-01 ... OK
Check                  I-SH-01 ... OK
Check                I-SLL-01 ... OK
Check               I-SLLI-01 ... OK
Check                I-SLT-01 ... OK
Check               I-SLTI-01 ... OK
Check              I-SLTIU-01 ... OK
Check               I-SLTU-01 ... OK
Check                I-SRA-01 ... OK
Check               I-SRAI-01 ... OK
Check                I-SRL-01 ... OK
Check               I-SRLI-01 ... OK
Check                I-SUB-01 ... OK
Check                 I-SW-01 ... OK
Check                I-XOR-01 ... OK
Check               I-XORI-01 ... OK
--------------------------------
OK: 48/48 RISCV_TARGET=neorv32 RISCV_DEVICE=rv32i RISCV_ISA=rv32i
```

RISC-V `rv32im` Tests

```
Check                      DIV ... OK
Check                     DIVU ... OK
Check                      MUL ... OK
Check                     MULH ... OK
Check                   MULHSU ... OK
Check                    MULHU ... OK
Check                      REM ... OK
Check                     REMU ... OK
--------------------------------
OK: 8/8 RISCV_TARGET=neorv32 RISCV_DEVICE=rv32im RISCV_ISA=rv32im
```

RISC-V `rv32imc` Tests

```
Check                    C-ADD ... OK
Check                   C-ADDI ... OK
Check                C-ADDI16SP ... OK
Check                C-ADDI4SPN ... OK
Check                    C-AND ... OK
Check                   C-ANDI ... OK
Check                   C-BEQZ ... OK
Check                   C-BNEZ ... OK
Check                      C-J ... OK
Check                    C-JAL ... OK
Check                   C-JALR ... OK
Check                     C-JR ... OK
Check                     C-LI ... OK
Check                    C-LUI ... OK
Check                     C-LW ... OK
Check                   C-LWSP ... OK
Check                     C-MV ... OK
Check                     C-OR ... OK
Check                   C-SLLI ... OK
Check                   C-SRAI ... OK
Check                   C-SRLI ... OK
Check                    C-SUB ... OK
Check                     C-SW ... OK
Check                   C-SWSP ... OK
Check                    C-XOR ... OK
--------------------------------
OK: 25/25 RISCV_TARGET=neorv32 RISCV_DEVICE=rv32imc RISCV_ISA=rv32imc
```

RISC-V `rv32Zicsr` Tests

```
Check                 I-CSRRC-01 ... OK
Check                I-CSRRCI-01 ... OK
Check                 I-CSRRS-01 ... OK
Check                I-CSRRSI-01 ... OK
Check                 I-CSRRW-01 ... OK
Check                I-CSRRWI-01 ... OK
--------------------------------
OK: 6/6 RISCV_TARGET=neorv32 RISCV_DEVICE=rv32Zicsr RISCV_ISA=rv32Zicsr
```

RISC-V `rv32Zifencei` Tests

```
Check             I-FENCE.I-01 ... OK
--------------------------------
OK: 1/1 RISCV_TARGET=neorv32 RISCV_DEVICE=rv32Zifencei RISCV_ISA=rv32Zifencei
```

1.4.1 RISC-V Non-Compliance Issues

This list shows the *currently known* issues regarding full RISC-V-compliance.

Not exception is triggered yet when using registers above `x15` in embedded mode (CPU `E` extension enabled via the `CPU_EXTENSION_RISCV_E` generic).

The `misa` CSR is read-only. It reflects the *synthesized* CPU extensions. Hence, all implemented CPU extensions are always active and cannot be enabled/disabled dynamically during runtime. Any write access to it is ignored and will not cause any exception or side-effects.

The performance counter CSRs `[m]cycleh` and `[m]instreth` are only 20-bit wide (in contrast to the original 32-bit).

The `mcause` CSR is read-only for the application code. Any write access to this CSR is simply ignored.

The *Physical Memory Protection* (PMP) only supports the modes `OFF` and `NAPOT` yet. Also, the CPU only supports up to 8 regions.

1.4.2 Custom Extensions

The custom extensions are always enabled and are indicated by the `X` bit in the `misa` CSR.

The CPU provides four “fast interrupt” interrupts, which are controlled via custom bit in the `mie` and `mip` CSR. This extension is mapped to bits, that are available for custom use (according to the RISC-V specs). Also, custom trap codes for `mcause` are provided.

1.5. Project Folder Structure

```
neorv32                 Project home folder.
|
├─.ci                   Scripts for continuous integration.
|
├─docs                  Project documentary: RISC-V specifications implemented in this
| |                     project, Wishbone bus specification, NEORV32 data sheet, doxygen
| |                     makefiles.
| |
| ├─doxygen_build       Software documentary HTML files (generated by doxygen).
| |
| └─figures             Images mainly for the GitHub front page.
|
├─rtl                   Processor's VHDL source files.
| |
| ├─core                This folder contains all the rtl (VHDL) core files of the NEORV32.
| |                     Make sure to add ALL of them to your FPGA EDA project.
| |
| ├─top_templates       Here you can find alternative top entities of the NEORV32.
| |
| └─fpga_specific       This folder provides FPGA technology-specific optimized HW modules.
|
├─sim                   The sim folder contains the default VHDL testbench and additional
| |                     simulation files.
| |
| ├─ghdl                Simulation script for GHDL.
| |
| └─Vivado              Default Xilinx Vivado simulation waveform configuration.
|
└─sw                    The software folder contains the processor's core libraries,
  |                     makefiles, linker scripts, start-up codes and example programs.
  |
  ├─bootloader          Source and compilation script of the NEORV32-internal bootloader.
  |
  ├─common              Application & bootloader linker scripts and startup codes.
  |
  ├─example             Here you can find several example programs. Each project folder
  | |                   includes the program's C sources and a makefile. Add your own
  | └─...               projects to this folder.
  |
  ├─image_gen           Helper program to generate executables for the NEORV32.
  |
  └─lib                 This folder contains the processor's core libraries.
    |
    ├─include           NEORV32 hardware driver library C source files and the according
    └─source            header/include files.
```

There are further files and folders starting with a dot which – for example – contain data/configurations only relevant for `git` or for the continuous integration framework (`.ci`). These files and folders are not relevant for the actual checked-out NEORV32 project.

1.6. VHDL File Hierarchy

All necessary VHDL hardware description files are located in the project's `rtl/core` folder. The top entity of the entire processor including all the required configuration generics is **neorv32_top.vhd**.

All processor core VHDL files have to be assigned to a new **library** called **neorv32**.

```
neorv32_top.vhd                  Processor core top entity
|
├─neorv32_boot_rom.vhd            Bootloader ROM
| └─neorv32_bootloader_image.vhd  Boot ROM initialization image for the bootloader
├─neorv32_busswitch.vhd           Bus switch to mux CPU's I & D interfaces to
|                                 processor bus
├─neorv32_cpu.vhd                NEORV32 CPU top entity
| ├─neorv32_package.vhd           Processor/CPU main VHDL package file
| ├─neorv32_cpu_alu.vhd           Arithmetic/logic unit
| ├─neorv32_cpu_bus.vhd           Bus interface unit + physical memory protection
| ├─neorv32_cpu_control.vhd       CPU control, exception/IRQ system and CSRs
| | └─neorv32_cpu_decompressor.vhd Compressed instructions decoder
| ├─neorv32_cpu_cp_muldiv.vhd     Multiplication/division co-processor
| └─neorv32_cpu_regfile.vhd       Data register file
├─neorv32_devnull.vhd             Dummy device
├─neorv32_dmem.vhd                Processor-internal data memory
├─neorv32_gpio.vhd                General purpose input/output port unit
├─neorv32_imem.vhd                Processor-internal instruction memory
| └─neor32_application_image.vhd  IMEM application initialization image
├─neorv32_mtime.vhd               Machine system timer
├─neorv32_pwm.vhd                 Pulse-width modulation controller
├─neorv32_spi.vhd                 Serial peripheral interface controller
├─neorv32_sysinfo.vhd             System configuration information memory
├─neorv32_trng.vhd                True random number generator
├─neorv32_twi.vhd                 Two wire serial interface controller
├─neorv32_uart.vhd                Universal asynchronous receiver/transmitter
├─neorv32_wdt.vhd                 Watchdog timer
└─neorv32_wb_interface.vhd        External Wishbone bus gateway
```

1.7. Processor Top Entity – Signals

The following table shows all interface ports of the processor top entity (`rtl/core/neorv32_top.vhd`). The type of all signals is **`std_ulogic`** or **`std_ulogic_vector`**, respectively – except for the TWI signals, which are of type **`std_logic`**.

Signal Name	Width	Direction	Function	HW Module
Global Control				
clk_i	1	Input	Global clock line, all registers triggering on rising edge	global
rstn_i	1	Input	Global reset, low-active	
External bus interface (Wishbone-compatible)				
wb_adr_o	32	Output	Destination address	WISHBONE
wb_dat_i	32	Input	Write data	
wb_dat_o	32	Output	Read data	
wb_we_o	1	Output	Write enable ('0' = read transfer)	
wb_sel_o	4	Output	Byte enable	
wb_stb_o	1	Output	Strobe	
wb_cyc_o	1	Output	Valid cycle	
wb_ack_i	1	Input	Transfer acknowledge	
wb_err_i	1	Input	Transfer error	
Advanced memory control signals				
fence_o	1	Output	Indicates an executed `fence` instruction	CPU
fencei_o	1	Output	Indicates an executed `fencei` instruction	
General Purpose Inputs & Outputs (GPIO)				
gpio_o	16	Output	General purpose parallel output[2]	GPIO
gpio_i	16	Input	General purpose parallel input	
Universal Asynchronous Receiver/Transmitter (UART)				
uart_txd_o	1	Output	UART serial transmitter	UART
uart_rxd_i	1	Input	UART serial receiver	
Serial Peripheral Interface Controller (SPI)				
spi_sck_o	1	Output	SPI controller clock line	SPI
spi_sdo_o	1	Output	SPI serial data output	
spi_sdi_i	1	Input	SPI serial data input	
spi_csn_o	8	Output	SPI dedicated chip select lines 0..7[3] (low-active)	
Two-Wire Interface Controller (TWI)				
twi_sda_io	1	InOut	TWI serial data line	TWI
twi_scl_io	1	InOut	TWI serial clock line	
Pulse-Width Modulation Channels (PWM)				
pwm_o	4	Output	Pulse-width modulated channels	PWM
Interrupts				
msw_irq_i	1	Input	Machine software interrupt (RISC-V)	CPU
mext_ack_o	1	Input	Machine external interrupt (RISC-V)	

Table 1: neorv32_top.vhd – processor's top entity interface ports

2 Bit #0 is used by the bootloader to drive a high-active status LED.
3 Chip select #0 is used by the bootloader to access the external boot SPI flash.

1.8. Processor Top Entity – Configuration Generics

This is a list of all configuration generics of the NEORV32 processor top entity `rtl/neorv32_top.vhd`. The generic name is shown in **orange**, the type in **black** and the default value in light gray. Most of the configured settings can be determined by the software via the SYSINFO IO module (3.14. System Configuration Information Memory (SYSINFO)).

1.8.1 General

`CLOCK_FREQUENCY` **natural** `0`
The clock frequency of the processor's `clk_i` input port in Hertz (Hz).

`BOOTLOADER_USE` **boolean** `true`
Implement the boot ROM, pre-initialized with the bootloader image when `true`. This will also change the processor's boot address from `MEM_ISPACE_BASE` to the base address of the boot ROM. See chapter 4.5. Bootloader for more information.

`CSR_COUNTERS_USE_USE` **boolean** `true`
Implement the standard RISC-V (performance) counter CSRs `[m]cyle[h]`, `[m]instret[h]` and `time[h]`. The counters can only be accessed when `CPU_EXTENSION_RISCV_Zicsr` is `true`. If this generic is disabled, any access to one of those CSRs will cause an exception. The `time[h]` CSRs require an input from the MTIME unit.

`USER_CODE` **std_ulogic_vector(31 downto 0)** `0x"00000000"`
Custom user code that can be read by software via the SYSINFO module.

1.8.2. RISC-V CPU Extensions

See chapter 2. Central Processing Unit (CPU) for more information.

`CPU_EXTENSION_RISCV_C` **boolean** `false`
Implement the CPU extension for compressed instructions when `true`.

`CPU_EXTENSION_RISCV_E` **boolean** `false`
Implement the embedded CPU extension (only implement the first 16 data registers) when `true`.

`CPU_EXTENSION_RISCV_M` **boolean** `false`
Implement integer multiplication and division instruction when `true`.

`CPU_EXTENSION_RISCV_U` **boolean** `false`
Implement user privilege level when `true`.

`CPU_EXTENSION_RISCV_Zicsr` **boolean** `true`
Implement the control and status register (CSR) access instructions when `true`. Note: When this option is disabled, the complete exception system will be excluded from synthesis. Hence, no interrupts and no exceptions can be detected.

The `CPU_EXTENSION_RISCV_Zicsr` should be **always enabled**. The bootloader and also the default application start-up code (`crt0.S`) rely on system information provided by (custom) CSRs.

`CPU_EXTENSION_RISCV_Zifencei` boolean `true`
Implement the instruction fetch synchronization instruction `ifetch.i`. For example, this option is required for self-modifying code.

1.8.3. Physical Memory Protection

`PMP_USE` boolean `false`
Implement physical memory protection (PMP) when `true`.

`PMP_NUM_REGIONS` natural `4`
Defines the number of PMP regions. Allowed configurations: 1 to 8. With each additional region the according `pmpcfgx` and `pmpaddrx` CSR / CSR bits become available.

`PMP_GRANULARITY` natural `14`
The PMP only supports the `NATOP` mode. This generic defines the minimal granularity. Allowed values: 1 (8-byte region), 1 (16-byte region), …, 30 (4GB region). Default is 14 (64kB region).

1.8.4. Memory Configuration – Instruction Memory

See chapter Fehler: Verweis nicht gefunden for more information.

`MEM_ISPACE_BASE` std_ulogic_vector(31 downto 0) `x"00000000"`
Base address of the instruction memory space. This is also the default boot address, if the bootloader is not implemented.

`MEM_ISPACE_SIZE` natural `16*1024`
Size of the instruction memory space in bytes. Starts at `MEM_ISPACE_BASE`.

`MEM_INT_IMEM_USE` boolean `true`
Implement processor internal instruction memory (IMEM) when `true`.

`MEM_INT_IMEM_SIZE` natural `16*1024`
Size in bytes of the processor internal instruction memory (IMEM) when `true`. Has no effect when `MEM_INT_IMEM_USE` is `false`. Must no be greater than `MEM_ISPACE_SIZE`.

`MEM_INT_IMEM_ROM` boolean `false`
Implement processor-internal instruction memory as read-only memory, which will be initialized with the application image at synthesis time. Has no effect when `MEM_INT_IMEM_USE` is `false`.

1.8.5. Memory Configuration – Data Memory

See chapter 3.2. Processor-Internal Data Memory (DMEM) for more information.

MEM_DSPACE_BASE **std_ulogic_vector(31 downto 0)** x"80000000"
Base address of the data memory space.

MEM_DSPACE_SIZE **natural** 8*1024
Size of the data memory space in bytes. Starts at MEM_DSPACE_BASE.

MEM_INT_DMEM_USE **boolean** true
Implement processor internal data memory (DMEM) when true.

MEM_INT_DMEM_SIZE **natural** 8*1024
Size in bytes of the processor internal data memory (DMEM) when true. Has no effect when MEM_INT_DMEM_USE is false. Must no be greater than MEM_DSPACE_SIZE.

1.8.6. Memory Configuration – External Memory Interface

See chapter 3.4. Processor-External Memory Interface (WISHBONE) for more information.

MEM_EXT_USE **boolean** false
Implement external bus interface (WISHBONE) when true.

MEM_EXT_REG_STAGES **natural** 2
Defines the number of register stages inside the external bus gateway. Allowed configurations: 0, 1 or 2. Adding register stages increases the bus access latency but will also improve timing.

MEM_EXT_TIMEOUT **natural** 15
Maximum length of bus access in main clock cycles. If a bus access is not acknowledged within the specified time, the access is aborted and a load/store/instruction access fault is triggered.

1.8.7. Processor Peripherals

See chapter Fehler: Verweis nicht gefunden for more information.

IO_GPIO_USE **boolean** true
Implement general purpose input/output port unit (GPIO) when true. When disabled, the gpio_i signal is unconnected and the gpio_o signal is always low. See chapter 3.5. General Purpose Input and Output Port (GPIO) for more information.

IO_MTIME_USE **boolean** true
Implement machine system timer (MTIME) when true. When disabled, the CPU's machine timer interrupt is not available. The CPU_EXTENSION_RISCV_Zicsr has to be enabled if you want to use the machine system timer's interrupt. See chapter 3.7. Machine System Timer (MTIME) for more information.

IO_UART_USE **boolean** true
Implement universal asynchronous receiver/transmitter (UART) when true. When disabled, the uart_rxd_i signal is unconnected and the uart_txd_o signal is always low. See chapter 3.8. Universal Asynchronous Receiver and Transmitter (UART) for more information.

IO_SPI_USE **boolean** true
Implement serial peripheral interface controller (SPI) when true. When disabled, the spi_miso_i signal is unconnected, the spi_sclk_o and spi_mosi_o signals are always low and the spi_csn_o signal is always high. See chapter 3.9. Serial Peripheral Interface Controller (SPI) for more information.

IO_TWI_USE **boolean** true
Implement two-wire interface controller (TWI) when true. When disabled, the twi_sda_io and twi_scl_io signals are unconnected. See chapter 3.10. Two Wire Serial Interface Controller (TWI) for more information.

IO_PWM_USE **boolean** true
Implement pulse-width modulation controller (PWM) when true. When disabled, the pwm_o signal is always low. See chapter 3.11. Pulse Width Modulation Controller (PWM) for more information.

IO_WDT_USE **boolean** true
Implement watchdog timer (WDT) when true. See chapter 3.6. Watchdog Timer (WDT) for more information.

IO_TRNG_USE **boolean** false
Implement true-random number generator (TRNG) when true. See chapter 3.12. True Random Number Generator (TRNG) for more information.

IO_DEVNULL_USE **boolean** true
Implement dummy device (DEVNULL) when true. This device can also be used for fast simulation console out. See chapter 3.13. Dummy Device (DEVNULL) and 5.12. Simulating the Processor for more information.

1.9. CPU Top Entity – Signals

The following table shows all interface ports of the CPU top entity (`rtl/core/neorv32_cpu.vhd`). The type of all signals is **`std_ulogic`** or **`std_ulogic_vector`**, respectively.

Signal Name	Width	Direction	Function	HW Module
Global Control				
clk_i	1	Input	Global clock line, all registers triggering on rising edge	global
rstn_i	1	Input	Global reset, low-active	
Instruction Bus Interface				
i_bus_addr_o	32	Output	Destination address	BUS_UNI
i_bus_rdata_i	32	Input	Write data	
i_bus_wdata_o	32	Output	Read data	
i_bus_ben_o	4	Output	Byte enable	
i_bus_we_o	1	Output	Write transaction	
i_bus_re_o	1	Output	Read transaction	
i_bus_cancel_o	1	Output	Cancel current transfer	
i_bus_ack_i	1	Input	Bus transfer acknowledge from accessed peripheral	
i_bus_err_i	1	Input	Bus transfer terminate from accessed peripheral	
i_bus_fence_o	1	Output	Indicates an executed FENCEI instruction	
Data Bus Interface				
i_bus_addr_o	32	Output	Destination address	BUS_UNIT
i_bus_rdata_i	32	Input	Write data	
i_bus_wdata_o	32	Output	Read data	
i_bus_ben_o	4	Output	Byte enable	
i_bus_we_o	1	Output	Write transaction	
i_bus_re_o	1	Output	Read transaction	
i_bus_cancel_o	1	Output	Cancel current transfer	
i_bus_ack_i	1	Input	Bus transfer acknowledge from accessed peripheral	
i_bus_err_i	1	Input	Bus transfer terminate from accessed peripheral	
i_bus_fence_o	1	Output	Indicates an executed FENCE instruction	
System Time				
time_i	64	Input	System time input (from MTIME)	CSR
Interrupts (RISC-V-compliant)				
msw_irq_i	1	Input	RISC-V machine software interrupt	CONTROL
mext_irq_i	1	Input	RISC-V external software interrupt	
mtime_irq_i	1	Input	RISC-V timer software interrupt	
Fast Interrupts (custom extension)				
firq_i	4	Input	Fast interrupt request signals	CONTROL

Table 2: neorv32_cpu.vhd – CPU top entity interface ports

1.10. CPU Top Entity – Configuration Generics

This is a list of all configuration generics of the NEORV32 processor top entity `rtl/neorv32_cpu.vhd`. The generic name is shown in **orange**, the type in **black** and the default value in light gray.

1.10.1 General

`CSR_COUNTERS_USE_USE` **boolean** `true`
Implement the standard RISC-V (performance) counter CSRs `[m]cyle[h]`, `[m]instret[h]` and `time[h]`. The counters can only be accessed when `CPU_EXTENSION_RISCV_Zicsr` is `true`. If this generic is disabled, any access to one of those CSRs will cause an exception. The `time[h]` CSRs require an input from an MTIME unit via the `time_i` input signal.

`HW_THREAD_ID` **std_ulogic_vector(31 downto 0)** `x"00000000"`
The hart ID of the CPU. Can be read via the `mhartid` CSR. Hart IDs must be unique within a system.

`CPU_BOOT_ADDR` **std_ulogic_vector(31 downto 0)** `x"00000000"`
Defines the boot address of the CPU after reset.

1.10.2. RISC-V CPU Extensions

`CPU_EXTENSION_RISCV_C` **boolean** `false`
Implement the CPU extension for compressed instructions when `true`.

`CPU_EXTENSION_RISCV_E` **boolean** `false`
Implement the embedded CPU extension (only implement the first 16 data registers) when `true`.

`CPU_EXTENSION_RISCV_M` **boolean** `false`
Implement integer multiplication and division instruction when `true`.

`CPU_EXTENSION_RISCV_U` **boolean** `false`
Implement user privilege level when `true`.

`CPU_EXTENSION_RISCV_Zicsr` **boolean** `true`
Implement the control and status register (CSR) access instructions when `true`. Note: When this option is disabled, the complete exception system will be excluded from synthesis. Hence, no interrupts and no exceptions can be detected.

The `CPU_EXTENSION_RISCV_Zicsr` should be **always enabled**. The bootloader and also the default application start-up code (`crt0.S`) rely on system information provided by (custom) CSRs.

`CPU_EXTENSION_RISCV_Zifencei` **boolean** `true`
Implement the instruction fetch synchronization instruction `ifetch.i`. For example, this option is required for self-modifying code.

1.10.3. Physical Memory Protection

PMP_USE **boolean** false
Implement physical memory protection (PMP) when true.

PMP_NUM_REGIONS **natural** 4
Defines the number of PMP regions. Allowed configurations: 1 to 8. With each additional region the according pmpcfgx and pmpaddrx CSR / CSR bits become available.

PMP_GRANULARITY **natural** 14
The PMP only supports the NATOP mode. This generic defines the minimal granularity. Allowed values: 1 (8-byte region), 1 (16-byte region), …, 30 (4GB region). Default is 14 (64kB region).

1.10.4. Bus Interface

BUS_TIMEOUT **natural** 15
Maximum length of bus access in main clock cycles. If a bus access is not acknowledged within the specified time, the access is aborted and a load/store/instruction access fault is triggered.

1.11. FPGA Implementation Results

This chapter shows exemplary implementation results of the NEORV32 processor for an **Intel Cyclone IV EP4CE22F17C6N** FPGA on a *Terasic © DE0-Nano* board. The design was synthesized using **Intel Quartus Prime Lite 19.1** ("balanced implementation"). The timing information is derived from the Timing Analyzer / Slow 1200mV 0C Model. If not other specified, the default configuration of the processor's generics is assumed. No constraints were used.

The first chapter shows the implementation results for different CPU configurations (via the `CPU_EXTENSION_*` generics only) while the second chapter shows the implementation results for each of the available peripherals. The results were taken from the fitter report (Resource Section / Resource Utilization by Entity) and reflect the resource utilization by the CPU only.

Please note, that the provided results are just a relative measure as logic functions of different modules might be merged between entity boundaries, so the actual utilization results might vary a bit.

1.11.1. CPU

```
Hardware Version:    1.3.0.0
```

CPU	CPU Configuration Generics	LEs	FFs	MEM bits	DSPs	F_{max}

`rv32i`	`CPU_EXTENSION_RISCV_C = false`
	`CPU_EXTENSION_RISCV_E = false`
	`CPU_EXTENSION_RISCV_M = false`
	`CPU_EXTENSION_RISCV_Zicsr = false`
	`CPU_EXTENSION_RISCV_Zifencei = false`
		1122	481	2048	0	112 MHz

`rv32i` + `Zicsr` + `Zifencei`	`CPU_EXTENSION_RISCV_C = false`
	`CPU_EXTENSION_RISCV_E = false`
	`CPU_EXTENSION_RISCV_M = false`
	`CPU_EXTENSION_RISCV_Zicsr = true`
	`CPU_EXTENSION_RISCV_Zifencei = true`
		1891	819	2048	0	100 MHz

`rv32im` + `Zicsr` + `Zifencei`	`CPU_EXTENSION_RISCV_C = false`
	`CPU_EXTENSION_RISCV_E = false`
	`CPU_EXTENSION_RISCV_M = true`
	`CPU_EXTENSION_RISCV_Zicsr = true`
	`CPU_EXTENSION_RISCV_Zifencei = true`
		2496	1067	2048	0	100 MHz

`rv32imc` + `Zicsr` + `Zifencei`	`CPU_EXTENSION_RISCV_C = true`
	`CPU_EXTENSION_RISCV_E = false`
	`CPU_EXTENSION_RISCV_M = true`
	`CPU_EXTENSION_RISCV_Zicsr = true`
	`CPU_EXTENSION_RISCV_Zifencei = true`
		2734	1066	2048	0	100 MHz

`rv32emc` + `Zicsr` + `Zifencei`	`CPU_EXTENSION_RISCV_C = true`
	`CPU_EXTENSION_RISCV_E = true`
	`CPU_EXTENSION_RISCV_M = true`
	`CPU_EXTENSION_RISCV_Zicsr = true`
	`CPU_EXTENSION_RISCV_Zifencei = true`
		2722	1066	1024	0	100 MHz

Table 3: Hardware utilization for different CPU configurations

1.11.2. Processor Modules

Hardware Version: **1.3.0.0**

Module	Description	LEs	FFs	MEM bits	DSPs
Boot ROM	Bootloader ROM (4kB)	4	1	32 768	0
BUSSWITCH	Mux for CPU I & D interfaces	62	8	0	0
DEVNULL	Dummy device	3	1	0	0
DMEM	Processor-internal data memory (8kB)	12	2	65 536	0
GPIO	General purpose input/output ports	40	33	0	0
IMEM	Processor-internal instruction memory (16kB)	7	2	131 072	0
MTIME	Machine system timer	266	166	0	0
PWM	Pulse_width modulation controller	72	69	0	0
SPI	Serial peripheral interface	198	125	0	0
SYSINFO	System configuration information memory	10	7	0	0
TRNG	True random number generator	105	93	0	0
TWI	Two-wire interface	75	44	0	0
UART	Universal asynchronous receiver/transmitter	153	108	0	0
WDT	Watchdog timer	59	45	0	0

Table 4: Hardware utilization by the different peripheral modules

1.11.3. Exemplary FPGA Results

The following table shows exemplary *NEORV32 processor implementation results* for different FPGA platforms. The processor setup uses **all provided peripherals**, all CPU extensions (but not the `E` extension), no external memory interface and only internal instruction and data memories. IMEM uses 16kB and DMEM uses 8kB memory space. The setup top entity connects most of the processor's top entity signals to FPGA pins – except for the Wishbone bus and the external interrupt signals.

```
Hardware Version:   1.3.0.0
CPU Configuration:  rv32i(m)c + Zicsr + Zifencei
```

Vendor	FPGA	Board	Toolchain	Impl. strategy	LUT / LE	FF / REG	DSP	Embedded memory	*f* [MHz]
Intel	Cyclone IV EP4CE22F17C6N	Terasic DE0-Nano	Quartus Prime Lite 19.1	balanced	3934 (18%)	1799 (8%)	0 (0%)	Memory bits: 231424 (38%)	100
Lattice	iCE40 UltraPlus iCE40UP5K-SG48I	Upduino v2.0	Radiant 2.1 (LSE)	timing	4895 (92%)	1636 (31%)	0 (0%)	EBR: 12 (40%) SPRAM: 4 (100%)	22.875*
Xilinx	Artix-7 XC7A35TICSG324 -1L	Arty A7-35T	Vivado 2019.2	default	2432 (12%)	1852 (4%)	0 (0%)	BRAM: 8 (16%)	100*

Table 5: Hardware utilization for different FPGA platforms

Notes

The Lattice iCE40 UltraPlus setup uses the FPGA's SPRAM memory primitives for the internal IMEM and DEMEM (each 64kb). The according FPGA-specific memory components for the IMEM and DMEM can be found in the `rtl/fpga_specific` folder. Also, the Lattice setup does not implement the `M` extension.

The clock frequencies marked with an asterisk (*) are constrained clocks. The remaining ones are "f_max" results from the place and route timing reports.

The Upduino and the Arty board have on-board SPI flash memories for storing the FPGA configuration. These device can also be used by the default NEORV32 bootloader to store and automatically boot an application program after reset (both tested successfully).

1.12. CPU Performance

Hardware Version:	**1.3.0.0**

1.12.1. CoreMark Benchmark

Configuration

Hardware:	32kB IMEM, 16kB DMEM, 100MHz clock
CoreMark:	**2000** iteration, MEM_METHOD is **MEM_STACK**
Compiler:	**RISCV32-GCC 10.1.0**
Peripherals:	**UART** for printing the results

The performance of the NEORV32 was tested and evaluated using the CoreMark CPU benchmark. This benchmark focuses on testing the capabilities of the CPU core itself rather than the performance of the whole system. The according source code and the SW project can be found in the `sw/example/coremark` folder. All NEORV32-specific modifications were done in the port-me files - "outside" of the time-critical benchmark core.

The resulting CoreMark score is defined as CoreMark iterations per second:

$$\text{CoreMark Score} = \frac{\text{CoreMark iterations}}{\text{Time in seconds}}$$

The execution time is determined via the RISC-V-compliant `[m]cycle[h]` CSRs. The relative CoreMark score is defined as CoreMark score divided by the clock frequency [MHz]:

$$\text{Relative CoreMark Score} = \frac{\text{CoreMark Score}}{\text{Clock frequency [MHz]}}$$

Results

CPU	Executable Size	Optimization	CoreMark Score	CoreMarks/ Mhz
`rv32i + Zicsr + Zifencei`	21600 bytes	`-O2`	**27.02**	**0.2702**
`rv32imc + Zicsr + Zifencei`	20976 bytes	`-O2`	**57.14**	**0.5714**
`rv32im + Zicsr + Zifencei`	16348 bytes	`-O2`	**57.14**	**0.5714**

Table 6: NEORV32 CoreMark results

1.12.2. Instruction Timing

The NEORV32 CPU is based on a multi-cycle architecture. Each instruction is executed in a sequence of several consecutive micro operations. Hence, each instruction requires several clock cycles to execute. The average CPI (cycles per instruction) depends on the instruction mix of a specific applications and also on the available CPU extensions. The following table shows the performance results for successfully (!) running 2000 CoreMark iterations. The average CPI is computed by dividing the total number of required clock cycles (only the timed core to avoid distortion due to IO wait cycles) by the number of executed instructions (`[m]instret[h]` CSRs). The executables were generated using optimization `-O2`.

CPU	Required Clock Cycles	Executed Instructions	Average CPI
`rv32i + Zicsr + Zifencei`	7 433 933 906	1 494 298 800	**4.97**
`rv32im + Zicsr + Zifencei`	3 589 861 906	628 281 454	**5.71**
`rv32imc + Zicsr + Zifencei`	3 587 131 226	628 282 016	**5.70**

More information regarding the execution time of each implemented instruction can be found in chapter 2.2. Instruction Timing2.2. Instruction Timing.

2. Central Processing Unit (CPU)

The NEORV32 CPU is the heart of the NEORV32 processor. You can use it as part of the processor or you can just the CPU and build your very own processor system. The CPU itself consists of the following VHDL files from the project's `rtl/core` folder:

`neorv32_cpu.vhd`	**CPU top entity**
`neorv32_cpu_alu.vhd`	Arithmetic/logic unit
`neorv32_cpu_bus.vhd`	Bus interface unit
`neorv32_cpu_control.vhd`	CPU control and CSRs
`neorv32_cpu_cp_muldiv.vhd`	MULDIV co-processor (for CPU `M` extension)
`neorv32_cpu_decompressor.vhd`	Compressed instructions decoder (for CPU `C` extension)
`neorv32_cpu_regfile.vhd`	Data register file
`neorv32_package.vhd`	Processor/CPU package files

CPU Key Features

- 32-bit RISC-V CPU: `rv32[i/e][c][m]` + `[U][Zicsr][Zifencei]`
- Compliant to the RISC-V user specifications – passes the RISC-V compliance tests
- Mostly compliant to the RISC-V privileged specifications
- Optional privileged architecture (`Zicsr`) extension supporting RISC-V-compliant control and status registers (CSRs), access instructions, exceptions and interrupts
- Optional `Zifencei` extension for instruction stream synchronization via the `fence.i` instruction
- Privilege levels: Machine level (`M-mode`), User level (`U-mode`, when `U` extension is enabled)
- Optional Physical Memory Configuration (PMP), compliant to the RISCV-specs., only supports `NAPOT` mode and up to 8 regions yet
- Von-Neumann architecture, separated interfaces for instruction fetch and data access (merged into single bus via a bus switch for the NEORV32 processor)
- Little-endian byte order
- No hardware support of unaligned data/instructions accesses – they will trigger an exception. When the `C` extension is enabled, instructions can also be 16-bit aligned and a misaligned instruction address exception is not possible anymore
- Two-stage pipelined multi-cycle in-order instruction execution
- NEORV32-specific custom CSRs are mapped to the official RISC-V custom address spaces

Architecture

The NEORV32 CPU was designed from scratch based only on the official ISA and privileged architecture specifications. The following figure shows the simplified architecture of the CPU.

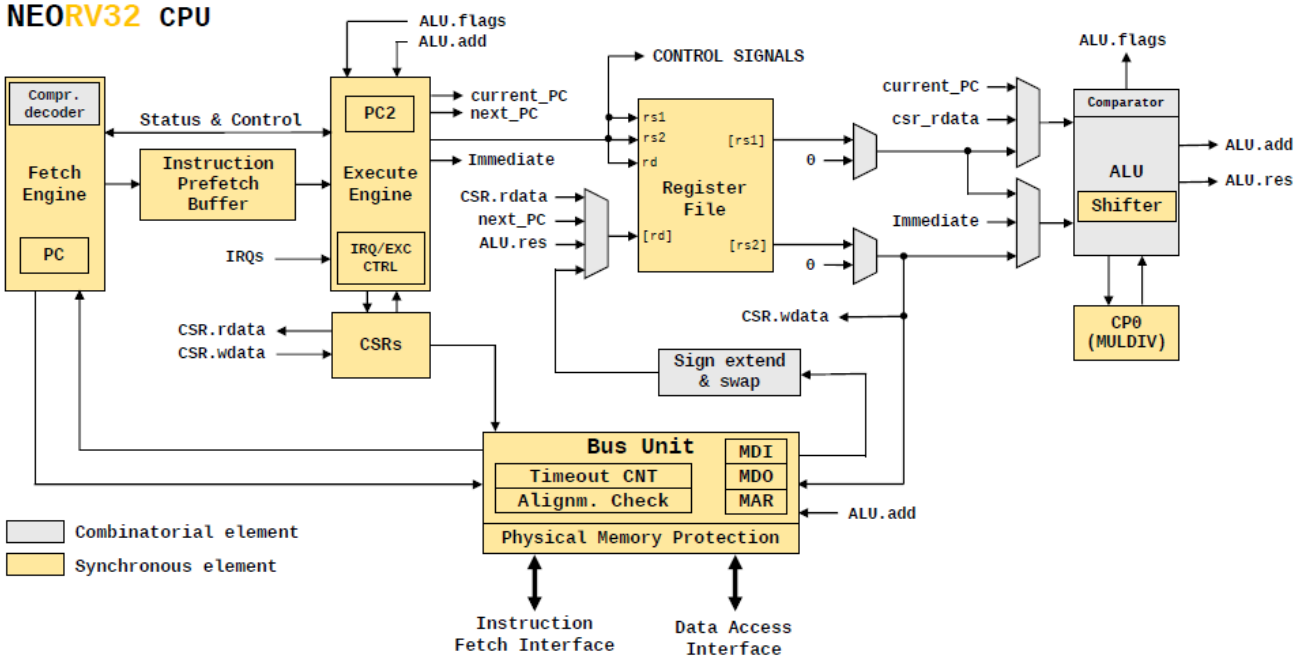

Figure 2: Simplified architecture of the NEORV32 CPU

The CPU uses a 2 stages pipelined architecture. The first stage (IF) is responsible for fetching new instructions from memory via the *fetch engine*. Compressed instructions – if enabled – are decompressed in this stage. The second stage (EX) is responsible for actually executing the fetched instructions via the *execute engine*. Both stages are connected via an instruction prefetch buffer.

These two pipeline stages are based on a multi-cycle processing engine. So the processing of each stage for a certain operations can take several cycles. Since the IF and EX stages are decoupled via the instruction prefetch buffer, both stages can operate in parallel and with overlapping operations. Hence, the optimal CPI (cycles per instructions) is 2, but it can be significantly higher: For instance when executing loads/stores, multi-cycle operations like shifts and multiplications or when the instruction fetch engine has to reload the prefetch buffers due to a taken branch.

Basically, the NEORV32 CPU is somewhere between a classical pipelined architecture, where each stage requires exactly one processing cycle (if not stalled) and a classical multi-cycle architecture, which executes every single instruction in a series of consecutive micro-operations.

The combination of these two classical design paradigms allows an increased instruction execution in contrast to a pure multi-cycle approach (due to the pipelined approach) at a reduced hardware footprint (due to the multi-cycle approach). This seems to be a quite good trade-off – at least for me.

The CPU provides independent interfaces for instruction fetch and data access. These two bus interfaces are merged into a single processor-internal bus via a bus switch. Hence, memory locations including peripheral devices are mapped to a single 32-bit address space making the architecture a modified Von-Neumann Architecture.

2.1. Instruction Set and CPU Extensions

32-bit Base ISA (`I` extension)

The CPU supports the complete RV32I base integer instruction set:

- `Immediates:` `LUI` `AUIPC`
- `Jumps:` `JAL` `JALR`
- `Branches:` `BEQ` `BNE` `BLT` `BGE` `BLTU` `BGEU`
- `Memory:` `LB` `LH` `LW` `LBU` `LHU` `SB` `SH` `SW`
- `ALU:` `ADDI` `SLTI` `SLTIU` `XORI` `ORI` `ANDI` `SLLI` `SRLI` `SRAI` `ADD` `SUB` `SLL` `SLT` `SLTU` `XOR` `SRL` `SRA` `OR` `AND`
- `Environment:` `ECALL` `EBREAK` `FENCE`

In order to keep the hardware footprint low, the CPU's shift unit uses a bit-serial approach. Shift operations are split in coarse shifts (multiples of 4) and a final fine shift (0 to 3). The total execution time depends on the shift amount.

The `FENCE` instruction does not perform any CPU-internal operation at all and behaves like a NOP. However, the top's `fence_o` signal is set high for one cycle to inform the memory system.

Embedded CPU Architecture (`E` extension)

This extensions does not feature additional instructions. However, the embedded CPU version only implements the lower 16 registers and uses a specific ABI (`ilp32e`).

Compressed Instructions (`C` extension)

Compressed 16-bit instructions are available when the `CPU_EXTENSION_C` configuration generic is `true`. In this case the following instructions are available:

- `C.ADDI4SPN` `C.LW` `C.SW` `C.NOP` `C.ADDI` `C.JAL` `C.LI` `C.ADDI16SP` `C.LUI` `C.SRLI` `C.SRAI` `C.ANDI` `C.SUB` `C.XOR` `C.OR` `C.AND` `C.J` `C.BEQZ` `C.BNEZ` `C.SLLI` `C.LWSP` `C.JR` `C.MV` `C.EBREAK` `C.JALR` `C.ADD` `C.SWSP`

Integer Multiplication and Division (`M` extension)

Hardware-accelerated multiplication and division instructions are available when the `CPU_EXTENSION_M` configuration generic is `true`. In this case the following instructions are available:

- `Multiplication:` `MUL` `MULH` `MULHSU` `MULHU`
- `Division:` `DIV` `DIVU` `REM` `REMU`

Multiplication and division operations are executed in a bit-serial approach. The execution time is fixed and not affected by the actual operation values.

User Privilege Level (`U` extension)

Add the less-privileged *user mode* when the `CPU_EXTENSION_U` configuration generic is `true`.

Control and Status Register Access (`Zicsr` extension)

The CSR access instructions as well as the exception and interrupt system are implemented when the `CPU_EXTENSION_RISCV_Zicsr` configuration generic is `true`. In this case the following instructions are available:

- `CSR access:` `CSRRW` `CSRRS` `CSRRC` `CSRRWI` `CSRRSI` `CSRRCI`
- `Environment:` `MRET` `WFI`

The "wait for interrupt instruction" `WFI` works like a *sleep* command. When executed, the CPU is halted until a valid interrupt request occurs (fast interrupt or machine software/external/timer interrupt).

Instruction Coherency Operation (`Zifencei` extension)

The `Zifencei` CPU extension is implemented if the `CPU_EXTENSION_RISCV_Zifencei` configuration generic is `true`. It allows manual synchronization of the instruction stream.

- `FENCE.I`

The `FENCE.I` instruction resets the CPU's instruction fetch engine and flushes all prefetch buffers. This allows a clean re-fetch of modified data from memory. Also, the top's `fencei_o` signal is set high for one cycle to inform the memory system.

Physical Memory Protection (`PMP` extension)

The NEORV32 physical memory protection is compliant to the PPM specified by the RISC-V specs. The circuitry is implemented when the `PMP_USE` configuration generic is `true`. The actual number of available PMP configuration registers (`pmpcfgx`) and PMP address registers (`pmpaddrx`) is defined by the configured number of regions (`PMP_NUM_REGIONS`).

The NEORV32 PMP only supports the NAPOT mode. The minimal available region granulartiy can be configured via the `PMP_GRANULARITY` generic.

- `CSRs:` `pmpcfg0` `pmpcfg1` `pmpaddr0` `pmpaddr1` `pmpaddr2` `pmpaddr3` `pmpaddr4` `pmpaddr5` `pmpaddr6` `pmpaddr7`

An illegal access to a protected region will trigger the according instruction/load/store *access fault* exception.

2.2. Instruction Timing

The following table shows the required clock cycles for executing a certain instruction. The execution cycles assume a bus access without additional wait states (like bus accesses to processor-internal memories or peripherals) and a filled pipelined.

Class	Instructions	Execution Cycles
ALU	ADDI SLTI SLTIU XORI ORI ANDI ADD SUB SLT SLTU XOR OR AND LUI AUIPC C.ADDI4SPN C.NOP C.ADDI C.LI C.ADDI16SP C.LUI C.ANDI C.SUB C.XOR C.OR C.AND C.ADD C.MV	2
ALU – Shifts	SLLI SRLI SRAI SLL SRL SRA C.SRLI C.SRAI C.SLLI	2 + *sha*[4]/4 + 1
Branches	BEQ BNE BLT BGE BLTU BGEU C.BEQZ C.BNEZ	Taken: 4 + 6 Not taken: 3
Jumps	JAL JALR C.JAL C.J C.JR C.JALR	4 + 6
Memory	LB LH LW LBU LHU SB SH SW C.LW C.SW C.LWSP C.SWSP	5
Multiplication	MUL MULH MULHSU MULHU	2 + 32 + 4
Division	DIV DIVU REM REMU	2 + 32 + 6
CSR Access	CSRRW CSRRS CSRRC CSRRWI CSRRSI CSRRCI	3
System	ECALL EBREAK MRET WFI FENCE FENCE.I C.EBREAK	3

Table 7: Required clock cycles per instruction (optimal)

Branches and Jumps

Jumps and taken branches are quite painful due to the pipelined architecture and the prefetch buffers, which require flushing and reloading after every jump or taken branch. However, this architecture highly accelerates the execution of all other instruction types. In summary, this acceleration overcomes the high branch penalty cycles.

Average CPI for "Real" Applications

The average CPI (cycles per instructions) for executing the CoreMark benchmark for different CPU configurations is presented in chapter 1.12.2. Instruction Timing.

4 Shift amount: 0..31

2.3. Control and Status Registers (CSRs)

The CSRs, the CSR-related instructions as well as the complete exception and interrupt processing system are only available when the `CPU_EXTENSION_RISCV_Zicsr` generic is `true`.

The following table shows a summary of all available CSRs. The address defines the CSR address for the CSR access instructions. The [ASM] name can be used for (inline) assembly code and is directly understood by the assembler/compiler. The [C] names are defined by the NEORV32 core library and can be used as immediates in plain C code. The "R/W" column shows whether the CSR can be read and/or written.

According to the RISC-V specs writing an implemented read-only CSR does not trigger an exception. When accessing a CSR that is not available or that is not implemented due to the actual processor/CPU configuration, the CSR access will trigger an invalid instruction exception.

If not otherwise mentioned, all CSRs are `0x0000_0000` after reset.

The NEORV32-specific CSRs (if available at all) are mapped to the official "*custom CSRs*" CSR address space.

Notes for the following Table

- **C** CSRs with this note have or are a custom CPU extension (that is allowed by the RISC-V specs)
- **R** This note indicates that a CSR is read-only (in contrast to the originally specified r/w capability)
- **S** CSRs with this node have a constrained compatibility; for example not all specified bits are available

Address	Name [ASM]	Name [C]	R/W	Function	Note
Machine Trap Setup (RISC-V compliant)					
0x300	mstatus	CSR_MSTATUS	r/w	Machine status register	
0x301	misa	CSR_MISA	r/-	Machine CPU ISA and extensions	R
0x304	mie	CSR_MIE	r/w	Machine interrupt enable register	C
0x305	mtvec	CSR_MTVEC	r/w	Machine trap-handler base address (for ALL traps)	
Machine Trap Handling (RISC-V compliant)					
0x340	mscratch	SCR_MSCRATCH	r/w	Machine scratch register	
0x341	mepc	CSR_MEPC	r/w	Machine exception program counter	
0x342	mcause	CSR_MCAUSE	r/-	Machine trap cause	R
0x343	mtval	CSR_MTVAL	r/w	Machine bad address or instruction	
0x344	mip	CSR_MIP	r/w	Machine interrupt pending register	C
Physical Memory Protection (RISC-V compliant)					
0x3a0	pmpcfg0	CSR_PMPCFG0	r/w	Physical memory protection configuration for region 0..3	S
0x3a1	pmpcfg1	CSR_PMPCFG1	r/w	Physical memory protection configuration for region 4..7	S
0x3b0	pmpaddr0	CSR_PMPADDR0	r/w	Physical memory protection address register region 0	
0x3b1	pmpaddr1	CSR_PMPADDR1	r/w	Physical memory protection address register region 1	
0x3b2	pmpaddr2	CSR_PMPADDR2	r/w	Physical memory protection address register region 2	
0x3b3	pmpaddr3	CSR_PMPADDR3	r/w	Physical memory protection address register region 3	
0x3b4	pmpaddr4	CSR_PMPADDR4	r/w	Physical memory protection address register region 4	
0x3b5	pmpaddr5	CSR_PMPADDR5	r/w	Physical memory protection address register region 5	
0x3b6	pmpaddr6	CSR_PMPADDR6	r/w	Physical memory protection address register region 6	
0x3b7	pmpaddr7	CSR_PMPADDR7	r/w	Physical memory protection address register region 7	
Counters and Timers (RISC-V compliant)					
0xb00	mcycle	CSR_MCYCLE	r/w	Machine cycle counter low word	
0xb02	minstret	CSR_MINSTRET	r/w	Machine instructions-retired counter low word	
0xb80	mcycleh	CSR_MCYCLEH	r/w	Machine cycle counter low word	S
0xb82	minstreth	CSR_MINSTRETH	r/w	Machine instructions-retired counter high word	S
0xc00	cycle	CSR_CYCLE	r/-	Cycle counter low word	
0xc01	time	CSR_TIME	r/-	System time (from MTIME) low word	
0xc02	instret	CSR_INSTRET	r/-	Instructions-retired counter low word	
0xc80	cycleh	CSR_CYCLEH	r/-	Cycle counter high word	S
0xc81	timeh	CSR_TIMEH	r/-	System time (from MTIME) high word	
0xc82	instreth	CSR_INSTRETH	r/-	Instructions-retired counter high word	S
Machine Information Registers, read-only (RISC-V compliant)					
0xf11	mvendorid	CSR_MVENDORID	r/-	Vendor ID	
0xf12	marchid	CSR_MARCHID	r/-	Architecture ID	
0xf13	mimpid	CSR_MIMPID	r/-	Machine implementation ID / version	
0xf14	mhartid	CSR_MHARTID	r/-	Machine thread ID	

Table 8: NEORV32 Control and Status Registers (CSRs)

2.3.1. Machine Trap Setup

Machine Status Register (mstatus)

The `mstatus` CSR is compliant to the RISC-V specs. The following bits are implemented (all remaining bits are always zero and are read-only):

Bit#	Name	R/W	Function
12:11	MPP	r/w	Previous machine privilege level, 11= machine (M) mode, 00= user (U) level
7	MPIE	r/w	Previous machine interrupt enable flag
3	MIE	r/w	Machine interrupt enable flag

When entering an exception/interrupt, the `MIE` flag is copied to `MPIE` and cleared afterwards. When leaving the exception/interrupt (via the `MRET` instruction), `MPIE` is copied back to `MIE`.

ISA and Extensions (misa)

This CSR is not fully RISC-V-compliant as it is read-only. Hence, implemented CPU extensions cannot be switch on/off during runtime.

The `MISA` CSR is compliant to the RISC-V `misa` CSR. The first 26 bits show the implemented CPU extensions. The following bits are implemented (all remaining bits are always zero and are read-only):

Bit#	R/W	Function
31:30	r/-	32-bit indicator (always “01”)
23	r/-	The **X** extension bit is always set to indicate custom non-standard extensions
20	r/-	**U** CPU extensions (user mode), wet when `CPU_EXTENSION_RISCV_U` enabled
12	r/-	**M** CPU extension (muld/div HW), set when `CPU_EXTENSION_RISCV_M` enabled
8	r/-	**I** CPU extension, always set, cleared when `CPU_EXTENSION_RISCV_E` enabled
4	r/-	**E** CPU extension (embedded), set when `CPU_EXTENSION_RISCV_E` enabled
2	r/-	**C** CPU extension (compressed instructions), set when `CPU_EXTENSION_RISCV_C` enabled

Machine Interrupt-Enable Register (mie)

The `mie` CSR is compliant to the RISC-V specs. The following bits are implemented (all remaining bits are always zero and are read-only):

Bit#	Name	R/W	Function
19	CPU_MIE_FIRQ3E	r/w	Fast interrupt channel 3 enable
18	CPU_MIE_FIRQ2E	r/w	Fast interrupt channel 2 enable
17	CPU_MIE_FIRQ1E	r/w	Fast interrupt channel 1 enable
16	CPU_MIE_FIRQ0E	r/w	Fast interrupt channel 0 enable
11	MEIE	r/w	Machine external interrupt enable
7	MTIE	r/w	Machine timer interrupt enable (from MTIME)
3	MSIE	r/w	Machine software interrupt enable

Machine Trap-Handler Base Address (mtvec)

The `mtvec` CSR is compliant to the RISC-V specs. This register stores the base address for the machine trap handler. The CPU jumps to this address, regardless of the trap source. The lowest two bits of this register are always zero and cannot be altered.

Bit#	Name	R/W	Function
31:2	-	r/w	4-byte aligned base address of trap base handler
1:0	-	r/-	Always zero

2.3.2. Machine Trap Handling

Scratch Register for Machine Trap Handlers (mscratch)

The `mscratch` CSR is compliant to the RISC-V specs. It is a general purpose scratch register that can be used by the exception/interrupt handler.

Machine Exception Program Counter (mepc)

The `mepc` CSR is compliant to the RISC-V specs. For exceptions (like an illegal instruction) this register provides the address of the exception-causing instruction. For Interrupt (like a machine timer interrupt) this register provides the address of the next not-yet-executed instruction.

Machine Trap Cause (mcause)

This CSR is not fully RISC-V-compliant since the `mcause` is read-only. Only the CPU's trap controller can write to this CSR. Any write access from the application program is ignored.

The `mcause` CSR is compliant to the RISC-V specs. It shows the cause of the current exception / interrupt (see chapter 2.4. Exceptions and Interrupts).

Bit#	Name	R/W	Function
31	-	r/w	1: Indicates an interrupt; 0: Indicates an exception
30:5	-	r/-	Always zero
4:0	-	r/w	Exception ID code

Machine Bad Address or Instruction (mtval)

The `mtval` CSR is compliant to the RISC-V specs. When a trap is triggered, the CSR shows either the faulting address (for misaligned/faulting load/stores/fetch) or the faulting instruction itself (for illegal instructions). For interrupts the CSR is set to zero.

Machine Interrupt Pending (mip)

The `mip` CSR is compliant to the RISC-V specs but hast custom extension. The following bits are implemented (all remaining bits are always zero and are read-only):

Bit#	Name	Note	R/W	Function
19	CPU_MIP_FIRQ3P	*custom*	r/-	Fast interrupt channel 3 pending
18	CPU_MIP_FIRQ2P	*custom*	r/-	Fast interrupt channel 2 pending
17	CPU_MIP_FIRQ1P	*custom*	r/-	Fast interrupt channel 1 pending
16	CPU_MIP_FIRQ0P	*custom*	r/-	Fast interrupt channel 0 pending
11	MEIP	RISC-V	r/-	Machine external interrupt pending
7	MTIP	RISC-V	r/-	Machine timer interrupt pending (from MTIME)
3	MSIP	RISC-V	r/-	Machine software interrupt pending

2.3.3. Physical Memory Protection

Physical Memory Protection Configuration Register 0 & 1 (pmpcfg0 & pmpcfg1)

The `pmpcfg0` and `pmpcfg1` CSRs are compliant to the RISC-V specs. They are used to configure up to 8 protection regions. The following bits (for the first PMP configuration entry) are implemented (all remaining bits are always zero and are read-only):

Bit#	RISC-V Name	R/W	Function
7	L	r/w	Lock bit
6:5	-	r/-	Reserved, always read as zero
4:3	A	r/w	Mode configuration; only **OFF** ("00") and **NAPOT** ("11") are supported
2	X	r/w	Execute permission
1	W	r/w	Write permission
0	R	r/w	Read permission

Physical Memory Protection Address Registers 0 to 7 (pmaddrg0 ... pmpaddr7)

The `pmpaddr0` to `pmpaddr7` CSRs are compliant to the RISC-V specs. They are used to configure the base address and the region size for up to 8 regions.

2.3.4. Counters and Timers

These timers and counter can be used for performance evaluation of an application. The `[m]instret[h]` counters increment when an instruction enters the *execute* stage in the CPU's execute engine. The `[m]cycle[h]` counters increment with the CPU clock when the CPU is not in sleep mode.

Cycle Counter for RDCYCLE Instruction – Low (cycle)

The `cycle` CSR is compliant to the RISC-V specs. It shows the lower 32-bit of the cycle counter. The `cycle` CSR is read-only and is a shadowed copy from the `mcycle` CSR.

Cycle Counter for RDCYCLEH Instruction – High (cycleh)

The `cycleh` CSR is not fully RISC-V-compliant since only the lowest 20-bit (in contrast to the original RISC-V-specified 32-bit) are implemented. The remaining bits are always zero.

The `cycleh` CSR is compliant to the RISC-V specs. It shows the upper **20-bit** of the cycle counter. The `cycleh` CSR is read-only and is a shadowed copy from the `mcycleh` CSR.

System Time for RDTIME Instruction – Low (time)

The `time` CSR is compliant to the RISC-V specs. It shows the lower 32-bit of the current system time. The system time is generated by the MTIME system timer unit via the CPU `time_i` signal. The `time` CSR is read-only. Change the system time via the MTIME unit.

System Time for RDTIMEH Instruction – High (timeh)

The `timeh` CSR is compliant to the RISC-V specs. It shows the upper 32-bit of the current system time. The system time is generated by the MTIME system timer unit via the CPU `time_i` signal. The `timeh` CSR is read-only. Change the system time via the MTIME unit.

Instructions-Retired Counter for RDINSTRET Instruction – Low (instret)

The `instret` CSR is compliant to the RISC-V specs. It shows the lower 32-bit of the number of retired instruction. The `instret` CSR is read-only and is a shadowed copy from the `minstret` CSR.

Instructions-Retired Counter for RDINSTRETH Instruction – High (instreth)

The `instreth` CSR is not fully RISC-V-compliant since only the lowest 20-bit (in contrast to the original RISC-V-specified 32-bit) are implemented. The remaining bits are always zero.

The `instreth` CSR is compliant to the RISC-V specs. It shows the upper **20-bit** of the number of retired instruction. The `instreth` CSR is read-only and is a shadowed copy from the `minstreth` CSR.

Machine Cycle Counter – Low (mcycle)

The `mcycle` CSR is compliant to the RISC-V specs. It shows the lower 32-bit of the cycle counter. The `mcycle` CSR can also be written and is copied to the `cycle` CSR.

Machine Cycle Counter – High (mcycleh)

The `mcycleh` CSR is not fully RISC-V-compliant since only the lowest 20-bit (in contrast to the original RISC-V-specified 32-bit) are implemented. The remaining bits are always zero.

The `mcycleh` CSR is compliant to the RISC-V specs. It shows the upper **20-bit** of the cycle counter. The `mcycleh` CSR can also be written and is copied to the `cycleh` CSR.

Machine Instruction-Retired Counter – Low (mcycle)

The `minstret` CSR is compliant to the RISC-V specs. It shows the lower 32-bit of the retired instructions counter. The `minstret` CSR can also be written and is copied to the `instret` CSR.

Machine Instruction-Retired Counter – High (mcycleh)

The `minstreth` CSR is not fully RISC-V-compliant since only the lowest 20-bit (in contrast to the original RISC-V-specified 32-bit) are implemented. The remaining bits are always zero.

The `minstreth` CSR is compliant to the RISC-V specs. It shows the upper **20-bit** of the retired instructions counter. The `minstreth` CSR can also be written and is copied to the `instreth` CSR.

2.3.5. Machine Information Registers

Vendor ID (mvendorid)

The `mvendorid` CSR is compliant to the RISC-V specs. It is read-only and always reads zero.

Architecture ID (marchid)

The `marchid` CSR is compliant to the RISC-V specs. It is read-only and always reads zero.

Implementation ID (mimpid)

The `mimpid` CSR is compliant to the RISC-V specs. It is read-only and shows the version of the NEORV32 as BCD-coded number.

Hardware Thread ID (mhartid)

The `mhartid` CSR is compliant to the RISC-V specs. It is read-only and shows the core's hart ID, which is assigned via the CPU's `HW_THREAD_ID` generic.

2.4. Exceptions and Interrupts

The NEORV32 supports the following exceptions and instructions (traps).Whenever an exception or interrupt is triggered, the CPU transfers control to the address stored in the `mtvec` CSR. The cause of the according interrupt or exception can be determined via the content of the `mcause` CSR

The traps are prioritized. If several exceptions occur at once only the one with highest priority is triggered. If several interrupts trigger at once, the one with highest priority is triggered while the remaining ones are queued. After completing the interrupt handler the interrupt with the second highest priority will issues and so on.

Custom Fast Interrupts
As a custom extension, the NEORV32 CPU features 4 fast interrupt request lines via the `firq_i(3 :0)` CPU top entity signals. These four interrupts have unique configuration and status flags in the `mie` and `mip` CSRs and also provide custom trap codes (see below).

Notes
The lines marked with an "**C**" are custom user extensions.

Priority	mcause	ID [C]	Function	Note
1	0x8000000B	TRAP_CODE_MEI	Machine external interrupt	
2	0x80000007	TRAP_CODE_MTI	Machine timer interrupt (via MTIME)	
3	0x80000003	TRAP_CODE_MSI	Machine software interrupt	
4	0x80000010	TRAP_CODE_FIRQ_0	Fast interrupt request channel 0	**C**
5	0x80000011	TRAP_CODE_FIRQ_1	Fast interrupt request channel 1	**C**
6	0x80000012	TRAP_CODE_FIRQ_2	Fast interrupt request channel 2	**C**
7	0x80000013	TRAP_CODE_FIRQ_3	Fast interrupt request channel 3	**C**
8	0x00000001	TRAP_CODE_I_ACCESS	Instruction access fault	
9	0x00000002	TRAP_CODE_I_ILLEGAL	Illegal instruction	
10	0x00000000	TRAP_CODE_I_MISALIGNED	Instruction address misaligned	
11	0x0000000B	TRAP_CODE_MENV_CALL	Environment call from M-mode (`ECALL`)	
12	0x00000003	TRAP_CODE_BREAKPOINT	Breakpoint (`EBREAK`)	
13	0x00000006	TRAP_CODE_S_MISALIGNED	Store address misaligned	
14	0x00000004	TRAP_CODE_L_MISALIGNED	Load address misaligned	
15	0x00000007	TRAP_CODE_S_ACCESS	Store access fault	
16	0x00000005	TRAP_CODE_L_ACCESS	Load access fault	

The [C] names are defined by the NEORV32 core library and can be used as immediates in plain C code.

2.5. Address Space

The CPU is a 32-bit architecture with separated instruction and data interfaces making it a *Harvard Architecture*. Each of this interfaces can access an address space of up to 2^{32} bytes (4GB). For the **NEORV32 processor**, these two interfaces are multiplexed to a single processor-internal bus making it a *modified von-Neumann* architecture.

NEORV32 Processor

For the NEORV32 processor, the address space is divided into 4 main region: The instruction memory space for instructions, the data memory space for application runtime data, the bootloader address space for the processor-internal bootloader and the IO address space for the processor-internal peripheral/IO devices.

The beginning of the memory space for instructions is defined via the `MEM_MISPACEBASE` generic. This generic must be 4-byte aligned. The complete size of the instruction memory space is defined via the `MEM_MISPACESIZE` generic (in bytes). Analogous, the beginning of the memory space for data is defined via the `MEM_MDSPACEBASE` generic. This generic must be 4-byte aligned, too. The complete size of the data memory space is defined via the `MEM_MDSPACESIZE` generic (in bytes). The instruction and data memory address spaces can also overlap or can also be completely identical.

The base address of the bootloader and the IO region for the peripheral devices are fixed. These address regions cannot be used for other applications – even if the bootloader or all IO devices are not implemented.

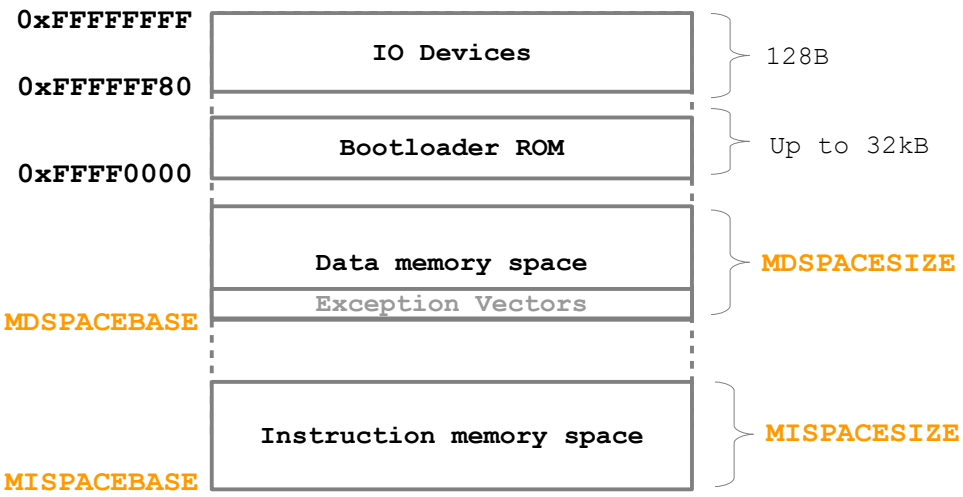

Figure 3: General NEORV32 address space layout

The processor can implement internal memories for instructions (IMEM) and data (DMEM), which will be mapped to FPGA block RAMs. The implementation of these memories is controlled via the boolean `MEM_INT_IMEM_USE` and `MEM_INT_DMEM_USE` generics. The size of these memories are configured via the `MEM_INT_IMEM_SIZE` and `MEM_INT_DMEM_SIZE` generics (in bytes). The processor-internal instruction memory (IMEM) can be implemented as ROM (`MEM_INT_IMEM_ROM`), which is initialized with the application code during synthesis. If the processor-internal IMEM is implemented, it is located at the base address of the instruction address space. Also, the processor-internal data memory is located at the beginning of the data address space if implemented. If the configured instruction/data memory space is greater than the size of the IMEM/DMEM, the accesses to the according addresses are forwarded to the external bus interface to interface processor-external memories and peripheral devices (when `MEM_EXT_USE` generic is `true`).

2.6. Bus Interface

The CPU provides two independent bus interfaces: One for fetching instructions (`i_bus_*`) and one for accessing data (`d_bus_*`) via load and store operations. Both interfaces use the same interface protocol. The two CPU busses are multiplexed by a bus switch (`rtl/core/neorv32_busswitch.vhd`) in the processor so both can access the processor-internal bus. Again, the processor-internal bus provides the same interface protocol as the original CPU interfaces.

The bus switch allows data accesses to have higher priority than instruction fetch accesses. The CPU's fetch provides prefetch buffers so there is no big deal it has to wait for bus access.

All processor-internal peripherals and memories are connected to the processor-bus driven by the bus switch. Also, the Wishbone-based external memory interface is connected to this bus. Hence, the processor uses a von-Neumann approach since data and instructions are accessed via the same bus and address space.

2.6.1. Interface Signals

The following table shows the signals of the interfaces seen from the CPU (a `*_o` signal is driven by the CPU and a `*_i` signal is read by the CPU).

Signal	Size	Function
`bus_addr_o`	32	The access address
`bus_rdata_i`	32	Data input for read operations
`bus_wdata_o`	32	Data output for write operations
`bus_ben_o`	4	Byte enable signal for write operations
`bus_we_o`	1	Bus write access
`bus_re_o`	1	Bus read access
`bus_cancel_o`	1	Indicates that the current bus access is terminated by the controller (the CPU)
`bus_ack_i`	1	Accessed peripheral indicates a successful completion of the bus transaction
`bus_err_i`	1	Accessed peripheral indicates an error during the bus transaction
`bus_fence_o`	1	This signal is set for one cycle when the CPU executes a data/instruction fence operation

Currently, there a no pipelined operation implemented. So only a single transfer request can be "on the fly". This also means that there can only be an exclusive active read transaction or an active write transactions – read and write transactions in parallel are not yet implemented.

2.6.2. Protocol

A bus request is triggered either by the `bus_re_o` signal (for reading data) or by the `bus_we_o` signal (for writing data). These signals are active for one cycle and initiate a new bus transaction. The transaction is completed when the accessed peripheral either sets the `bus_ack_i` signal (→ successful completion) or the `bus_err_i` signal to indicate an error during the transaction. All these control signals are only active (= high) for one single cycle.

An error during a transfer will trigger the according ***instruction bus access fault*** or ***load/store bus access fault*** exception. The CPU can also terminate a transfer (when an error during transfer is encountered) via the `bus_cancel_o` signal.

The transfer can be completed directly in the next cycle after it was initiated (via the `bus_re_o` or `bus_we_o` signal) if the peripheral sets `bus_ack_i` or `bus_err_i` high for one cycle.

There is no problem if the accessed peripheral takes longer to process the request. However, the bus transaction **has to be completed** within the number of cycles specified via the top entity `MEM_EXT_TIMEOUT` generic (for example within 15 cycles). If not, the according *instruction bus access fault* or *load/store bus access fault* exception is triggered and the CPU cancels the transaction via the `bus_cancel_o` signal.

Read Access

For a read access, the accessed address (`bus_addr_o`) is set when `bus_re_o` goes high. The address is kept stable until the transaction is completed. In the example below the accessed peripheral cannot answer directly in the next cycle after issuing. The peripheral hast to apply the read data right in the same cycle as the bus transaction is completed (here, the transaction is successful and the peripheral sets the `bus_ack_i` signal).

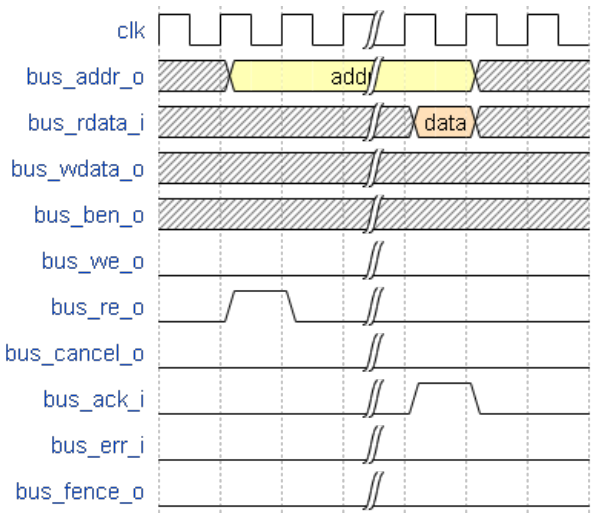

Figure 4: CPU interface read access

Write Access

For a write access, the accessed address (`bus_addr_o`), the data to be written (`bus_wdata_o`) and the byte enable signals (`bus_ben_o`) are set when `bus_we_o` goes high. These three signals are kept stable until the transaction is completed. In the example below the accessed peripheral cannot answer directly in the next cycle after issuing. Here, the transaction is successful and the peripheral sets the `bus_ack_i` signal several cycles after issuing.

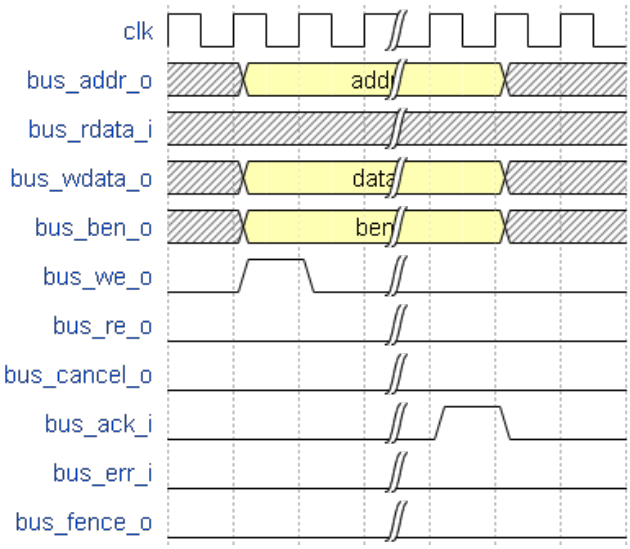

Figure 5: CPU interface write access

Memory Barriers

Whenever the CPU executes a fence instruction, the according interface signal is set high for one cycle (`d_bus_fence_o` for a `fence` instruction; `i_bus_fence_o` for a `fencei` instruction). It is the task of the memory system to perform the necessary operations (like a cache flush and refill).

3. Processor

The NEORV32 processor implements the NEORV32 CPU together with common processor modules to provide a RISC-V-based microcontroller-like platform.

The processor-internal peripheral/IO devices are located at the end of the 32-bit address space at base address `0xFFFFFF80`. A region of `128 bytes` is reserved for this devices. Hence, all peripheral are accessed using a memory-mapped scheme. A special linker script as well as the NEORV32 core software library abstract the specific memory layout for the user.

The peripheral/IO address space should not be used for other applications even when all of the devices are not implemented.

When accessing an IO device, that hast not been implemented (e.g., via the `IO_xxx_USE` generics), a load/store access fault is triggered.

Internal Reset Generator

Most processor-internal modules – except for the CPU and the watchdog timer – do not require a dedicated reset signal. However, all devices can be reset by software by clearing the corresponding unit's control register. The automatically included application start-up code will perform such a software-reset of all modules to ensure a clean system reset state.

The hardware reset signal of the processor can either be triggered via the external reset pin (`rstn_i`, **low-active**) or by the internal watchdog timer (if implemented). Before the external reset signal is applied to the system, it is filtered (so no spike can generate a reset, a minimum active reset period of one clock cycle is required) and extended to have a minimal duration of four clock cycles.

Internal Clock Divider

An internal clock divider generates 8 clock signals derived from the processor's main clock input `clk_i`. These derived clock signals are not actual *clock signals*. Instead, they are derived from a simple counter and are used as "clock enable" signal by the different processor modules. Thus, the whole design operates using only the main clock signal (single clock domain). Some of the processor peripherals like the Watchdog or the UART can select one of the derived clock enabled signals for their internal operation. If none of the connected modules require a clock signal from the divider, it is automatically deactivated to reduce dynamic power.

The peripheral devices, which provide a time-based configuration, provide a 3 bit prescaler select in their according control register to select 1 out of the 8 available clocks. The mapping of the prescaler select bits to the actually obtained clock are shown in the table below. Here, *f* represents the processor main clock from the top entity `clk_i` signal.

Prescaler bits:	000	001	010	011	100	101	110	111
Resulting clock:	f/2	f/4	f/8	f/64	f/128	f/1024	f/2048	f/4096

Notes

You should use the provided core software library to interact with the peripheral devices. This prevents incompatibilities with future versions, since the hardware driver functions handle all the register and register bit accesses.

Most of the IO devices do not have a hardware reset. Instead, the devices are reset via software by writing zero to the unit's control register. A general software-based reset of all devices is done by the application start-up code `crt0.asm`.

Nomenclature

Each peripheral device chapter features a register map showing accessible control and data registers of the according device including the implemented control and status bits. You can directly interact with these registers/bits via the provided C-code defines. These defines are defined in the main main processor core library file `sw/lib/include/neorv32.h`. The registers and/or register bits, which can be directly accessed using plain C-code, are marked with a **`[C]`**.

Not all registers or register bits can be arbitrarily read/written. The following read/write access types are available:

`r/w` Registers / register bits can be read and written.

`r/-` Registers / register bits are read-only. Any write access to them has no effect.

`0/w` These registers / register bits are write-only. They auto-clear in the next cycle and are always read as zero.

Bits / registers that are not listed in the register map tables are not (yet) implemented. These registers / register bits are always read as zero. A write access to them has no effect, but user programs should only write zero to them to keep compatible with future extension.

When writing to read-only registers, the access is nevertheless acknowledged, but no actual data is written. When reading data from a write-only register the result is undefined.

3.1. Processor-Internal Instruction Memory (IMEM)

Overview

Hardware source file(s):	`neorv32_imem.vhd`	
Software driver file(s):	`none`	Implicitly used
Top entity ports:	`none`	

Configuration generics:	`MEM_INT_IMEM_USE`
	`MEM_INT_IMEM_SIZE`
	`MEM_INT_IMEM_ROM`
		Implement processor-internal IMEM when `true`
		IMEM size in bytes
		Implement IMEM as ROM

A processor-internal instruction memory can be enabled via the processor's `MEM_INT_IMEM_USE` generic. The size in bytes is defined via the `MEM_INT_IMEM_SIZE` generic. If the IMEM is implemented, the memory is mapped into the instruction memory space (defined via the `MEM_MISPACESIZE` generic) and located at the beginning of the instruction memory space (defined via the `MEM_MISPACEBASE` generic).

By default, the IMEM is implemented as RAM, so the content can be modified during run time. This is required when using a bootloader that can update the content of the IMEM at any time. If you do not need the bootloader anymore – since your application development is done and you want the program to permanently reside in the internal instruction memory – the IMEM can also be implemented as true read-only memory. In this case set the `MEM_INT_IMEM_ROM` generic of the processor's top entity to `true`.

When the IMEM is implemented as ROM, it will be initialized during synthesis with the actual application program image. Based on your application the toolchain will automatically generate a VHDL initialization file `rtl/core/neorv32_application_image.vhd`, which is automatically inserted into the IMEM. If the IMEM is implemented as RAM, the memory will not be initialized at all.

3.2. Processor-Internal Data Memory (DMEM)

Overview

Hardware source file(s):	`neorv32_dmem.vhd`	
Software driver file(s):	`none`	Implicitly used
Top entity ports:	`none`	
Configuration generics:	`MEM_INT_DMEM_USE` `MEM_INT_DMEM_SIZE`	Implement processor-internal DMEM when `true` DMEM size in bytes

A processor-internal data memory can be enabled via the processor's `MEM_INT_DMEM_USE` generic. The size in bytes is defined via the `MEM_INT_DMEM_SIZE` generic. If the DMEM is implemented, the memory is mapped into the data memory space (defined via the `MEM_MDSPACESIZE` generic) and located at the beginning of the data memory space (defined via the `MEM_MDSPACEBASE` generic). The DMEM is always implemented as RAM.

3.3. Processor-Internal Bootloader ROM (BOOTROM)

Overview

Hardware source file(s):	`neorv32_boot_rom.vhd`	
Software driver file(s):	`none`	Implicitly used
Top entity ports:	`none`	
Configuration generics:	`BOOTLOADER_USE`	Implement bootloader when `true`

As the name already suggests, the boot ROM contains the read-only bootloader image. When the bootloader is enabled via the `BOOTLOADER_USE` generic it is directly executed after system reset.

The bootloader ROM is located at address `0xFFFF0000`. This location is fixed and the bootloader ROM size must not exceed 32kB. The bootloader read-only memory is automatically initialized during synthesis via the `rtl/core/neorv32_bootloader_image.vhd` file, which is generated when compiling and installing the bootloader sources.

The bootloader ROM address space cannot be used for other applications even when the bootloader is not implemented.

Boot Configuration

When the bootloader is implemented, the CPU starts execution after reset right at the beginning of the boot ROM. If the bootloader is not implemented, the CPU starts execution at the beginning of the instruction memory space defined via `MEM_MISPACEBASE` generic. In this case, the instruction memory has to contain a valid executable – either by using the internal IMEM with an initialization during synthesis or by a user-defined initialization process.

3.4. Processor-External Memory Interface (WISHBONE)

Overview

Hardware source file(s):	`neorv32_wishbone.vhd`	
Software driver file(s):	`none`	Implicitly used
Top entity ports:	`wb_adr_o`	Address output (32-bit)
	`wb_dat_i`	Data input (32-bit)
	`wb_dat_o`	Data output (32-bit)
	`wb_we_o`	Write enable
	`wb_sel_o`	Byte enable (4-bit)
	`wb_stb_o`	Strobe
	`wb_cyc_o`	Valid cycle
	`wb_ack_i`	Acknowledge
	`wb_err_i`	Bus error
	`fence_o`	Indicates an executed `fence` instruction
	`fencei_o`	Indicates an executed `fencei` instruction
Configuration generics:	`MEM_EXT_USE`	Enable external memory interface when `true`
	`MEM_EXT_REG_STAGES`	Number of interface register stages
	`MEM_EXT_TIMEOUT`	Maximum length of bus accesses

The external memory interface uses the Wishbone interface protocol. The external interface port is available when the `MEM_EXT_USE` generic is `true`. This interface can be used to attach external memories, custom hardware accelerators additional IO devices or all other kinds of IP blocks.

All memory accesses from the CPU, that do not target the internal bootloader ROM, the internal IO region or the internal data/instruction memories (if implemented at all) are forwarded to the Wishbone gateway and thus to the external memory interface.

Latency

The Wishbone gateway can be configured to provide additional register stages to ease timing closure. The `MEM_EXT_REG_STAGES` generic defines the number of register stages:

- 0: No register stages; no additional latency
- 1: Processor-outgoing signals are buffered; 1 cycle additional latency
- 2: Processor-outgoing and -incoming signals are buffered; 2 cycles additional latency

Bus Access Timeout

Whenever the CPU starts a memory access, an internal timer is started. If the accessed address (the memory or peripheral device) does not acknowledge the transfer within a certain time, the bus access is canceled and a load/store/instruction fetch bus access fault exception is raised – depending on the bus access type.

The processor-internal memories and peripherals will always acknowledge the transfers within two cycles. Of course, a bus timeout will occur if accessing unused address locations. For example, a bus timeout and thus, a load/store bus access fault, will occur when trying to access an IO device, that has not been implemented.

The maximum bus cycle time, after which an exception will be raised, is defined via the `MEM_EXT_TIMEOUT` generic of the NEORV32 processor.

Bus accesses via the external memory interface are acknowledged via the Wishbone-compliant `wb_ack_i` signal. The external bus accesses can be terminated/aborted at any time by an accessed device/memory via the Wishbone-compliant `wb_err_i` signal.

The bus timeout value is defined for the external memory interface but also applies when accessing processor-internal modules like memories or IO device. Hence, this parameter must not be less than one cycle.

Wishbone Bus Protocol

The external memory interface uses Classic Pipelined Wishbone Transactions. There is always a delay of at least one clock cycle between issuing a bus access and read-back / acknowledge. The transactions are always in order and cannot overlap.

A detailed description of the implemented Wishbone bus protocol and the according interface signals can be found in the data sheet "*Wishbone B4 – WISHBONE System-on-Chip (SoC) Interconnection Architecture for Portable IP Cores*". A copy of this document can be found in the `docs` folder of this project.

3.5. General Purpose Input and Output Port (GPIO)

Overview

Hardware source file(s):	`neorv32_gpio.vhd`	
Software driver file(s):	`neorv32_gpio.c` `neorv32_gpio.h`	
Top entity ports:	`gpio_o` `gpio_i`	16-bit parallel output port 16-bit parallel input port
Configuration generics:	`IO_GPIO_USE`	Implement GPIO port unit when `true`
CPU interrupts:	`Fast IRQ channel 1`	Pin-change interrupt

Theory of Operation

The general purpose parallel IO port unit provides a simple 16-bit parallel input port and a 16-bit parallel output port. These ports can be used chip-externally (for example to drive status LEDs, connect buttons, etc.) or system-internally to provide control signals for other IP modules. When the modules is disabled for implementation, the GPIO output port is tied to zero.

The parallel input port features a single pin-change interrupt. Whenever an input pin has a low-to-high or high-to-low transition, the interrupt is triggered. When the modules is disabled for implementation, the pin-change interrupt is permanently disabled.

Register Map

Address	Name [C]	Bit(s) (Name) [C]	R/W	Function
0xFFFFFF80	GPIO_INPUT	0..15	r/-	Parallel input port
0xFFFFFF84	GPIO_OUTPUT	0..15	r/w	Parallel output port

Table 9: GPIO port unit register map

3.6. Watchdog Timer (WDT)

Overview

Hardware source file(s):	`neorv32_wdt.vhd`	
Software driver file(s):	`neorv32_wdt.c` `neorv32_wdt.h`	
Top entity ports:	`none`	
Configuration generics:	`IO_WDT_USE`	Implement Watchdog timer when `true`
CPU interrupts:	`Fast IRQ channel 0`	Watchdog timer overflow

Theory of Operation

The watchdog (WDT) provides a last resort for safety-critical applications. The WDT has a free running 20-bit counter, that needs to be reset every now and then by the user program. If the counter overflows, either a system reset or an interrupt is generated.

The watchdog is enabled by setting the `WDT_CT_EN` bit. The clock used to increment the internal counter is selected via the 3-bit `WDT_CT_CLK_SWLx` prescaler:

`WDT_CT_CLK_SWLx`	`000`	`001`	`010`	`011`	`100`	`101`	`110`	`111`
Main clock prescaler:	2	4	8	64	128	1024	2048	4096
Timeout period in clock cycles:	2 097 152	4 194 304	8 388 608	67 108 864	134 217 728	1 073 741 824	2 147 483 648	4 294 967 296

Whenever the internal timer overflow, the watchdog executes one of two possible actions: Either a hard processor reset or an interrupt request to the CPU's fast interrupt channel #0. The `WDT_CT_MODE` bit defines the action to take on overflow: When cleared, the Watchdog will trigger an IRQ, when set the WDT will cause a system reset.

The cause of the last action of the Watchdog can be determined via the `WDT_CT_CAUSE` flag. If this flag I zero, the processor has been reset via the external reset pin. If this flag is set, the last action (reset or interrupt) was caused by a Watchdog timer overflow. The `WDT_CT_PWFAIL` flag is set, when the last Watchdog action was triggered by an illegal access to the Watchdog control register.

The Watchdog control register can only be accessed when the access password is present in bits 15:8 of the written data. The default Watchdog password is: **`0x47`**
The watchdog is reset whenever a valid write access to the unit's control register is performed.

Register Map

Address	Name [C]	Bit(s)	(Name) [C]	R/W	Function
0xFFFFFF8C	WDT_CT	0	WDT_CT_CLK_SEL0	r/w	Clock prescaler select bit 0
		1	WDT_CT_CLK_SEL1	r/w	Clock prescaler select bit 1
		2	WDT_CT_CLK_SEL2	r/w	Clock prescaler select bit 2
		3	WDT_CT_EN	r/w	Watchdog enable
		4	WDT_CT_MODE	r/w	Overflow action: 1: reset, 0: IRQ
		5	WDT_CT_CAUSE	r/-	Cause of last WDT action
		6	WDT_CT_PWFAIL	r/-	Last WDT action caused by wrong pwd
		15:8	WDT_CT_PASSWORD	0/w	Watchdog access password

Table 10: WDT register map

3.7. Machine System Timer (MTIME)

Overview

Hardware source file(s):	`neorv32_mtime.vhd`	
Software driver file(s):	`neorv32_mtime.c` `neorv32_mtime.h`	
Top entity ports:	`none`	
Configuration generics:	`IO_MTIME_USE`	Implement MTIME when `true`
CPU interrupts:	`MTI`	Machine timer interrupt

Theory of Operation

The MTIME machine system timer implements the memory-mapped `mtime` timer from the official RISC-V specifications. This unit features a 64-bit system timer incremented with the primary processor clock.

The 64-bit system time can be accessed via the `MTIME_LO` and `MTIME_HI` registers. A 64-bit time compare register – accessible via `MTIMECMP_LO` and `MTIMECMP_HI` – can be used to trigger an interrupt to the CPU whenever `MTIME >= MTIMECMP`. This interrupt is directly forwarded to the CPU's `MTI` interrupt. The time and compare registers can also be accessed as single 64-bit registers via the `MTIME` and `MTIMECMP` defines.

There is no need to acknowledge the MTIME interrupt. The interrupt request is a single-shot signal, so the CPU is triggered once if the system time is greater than or equal to the compare time. Hence, another MTIME IRQ is only possible when increasing the compare time.

The 64-bit counter and the 64-bit comparator are implemented as 2×32-bit counters and comparators with a registered carry to prevent a 64-bit carry chain ad thus, to simplify timing closure.

Register Map

Address	Name [C]	R/W	Function
0xFFFFFF90	MTIME_LO	r/w	Machine system time, low word
0xFFFFFF94	MTIME_HI	r/w	Machine system time, high word
0xFFFFFF98	MTIMECMP_LO	r/w	Time compare, low word
0xFFFFFF9C	MTIMECMP_HI	r/w	Time compare, high word

Table 11: MTIME register map

All registers of the MTIME system timer can only be written in full word mode (using `sw` instruction). All other write accesses will have no effect.

3.8. Universal Asynchronous Receiver and Transmitter (UART)

Overview

Hardware source file(s):	`neorv32_uart.vhd`	
Software driver file(s):	`neorv32_uart.c` `neorv32_uart.h`	
Top entity ports:	`uart_txd_o` `uart_rxd_o`	Serial transmitter output Serial receiver input
Configuration generics:	`IO_UART_USE`	Implement UART when `true`
CPU interrupts:	`Fast IRQ channel 2`	TX done or RX done

Theory of Operation

In most cases, the UART is a standard interface used to establish a communication channel between the computer/user and an application running on the processor platform. The NEORV32 UART features a standard configuration frame configuration: 8 data bits, 1 stop bit and no parity bit. These values are fixed. The actual Baudrate is configurable by software.

The UART is enabled when the `UART_CT_EN` bit in the UART control register is set. The actual transmission Baudrate (like “19200”) is configured via the 20-bit `UART_CT_BAUDxx` value and the 3-bit `UART_CT_PRSCx` clock prescaler.

`UART_CT_PRSCx`	`000`	`001`	`010`	`011`	`100`	`101`	`110`	`111`
Resulting prescaler:	2	4	8	64	128	1024	2048	4096

$$Baudrate = \frac{f_{main}\,[Hz]}{\text{Prescaler} \cdot \text{UART\_CT\_BAUD}}$$

A new transmission is started by writing the data byte to the lowest byte of the `UART_DATA` register. The transfer is completed when the `UART_CT_TX_BUSY` control register flag returns to zero. A new received byte is available when the `UART_DATA_AVAIL` flag of the `UART_DATA` register is set. If a new byte is received before the previous one has been read by the CPU, the receiver overrun flag `UART_CT_RXOR` is set.

The UART has a single interrupt, which can be trigger by two sources: The interrupt is triggered when a transmission has finished and the `UART_CT_TX_IRQ` flag is set. Additionally, the interrupt can also be triggered when a data byte has been received and the `UART_CT_RX_IRQ` flag is set.

If the UART is not implemented, the UART’s serial output port is tied to zero and the UART’s interrupt is unavailable.

Register Map

Address	Name [C]	Bit(s) (Name) [C]		R/W	Function
0xFFFFFFA0	UART_CT	11:0	UART_CT_BAUDxx	r/w	20-bit BAUD configuration value
		24	UART_CT_PRSC0	r/w	Baudrate clock prescaler select bit 0
		25	UART_CT_PRSC1	r/w	Baudrate clock prescaler select bit 1
		26	UART_CT_PRSC2	r/w	Baudrate clock prescaler select bit 2
		27	UART_CT_RXOR	r/-	UART receiver overrun
		28	UART_CT_EN	r/w	UART enable
		29	UART_CT_RX_IRQ	r/w	RX complete IRQ enable
		30	UART_CT_TX_IRQ	r/w	TX done IRQ enable
		31	UART_CT_TX_BUSY	r/-	Transceiver busy flag
0xFFFFFFA4	UART_DATA	7:0	UART_DATA_LSB/MSB	r/w	Receive/transmit data (8-bit)
		31	UART_DATA_AVAIL	r/-	RX data available when set

Table 12: UART register map

3.9. Serial Peripheral Interface Controller (SPI)

Overview

Hardware source file(s):	`neorv32_spi.vhd`	
Software driver file(s):	`neorv32_spi.c` `neorv32_spi.h`	

Top entity ports:	`spi_sck_o`
	`spi_sdo_o`
	`spi_dsi_i`
	`spi_csn_o`
		1-bit serial controller clock output
		1-bit serial controller data output
		1-bit serial controller data input
		8-bit chip select port (low-active)

Configuration generics:	`IO_SPI_USE`	Implement SPI when `true`
CPU interrupts:	`Fast IRQ channel 3`	Transmission done interrupt

Theory of Operation

SPI is a synchronous serial transmission protocol. The NEORV32 SPI transceiver allows 8-, 16-, 24- and 32-bit wide transmissions. The unit provides 8 dedicated chip select signals via the top entity's `spi_csn_o` signal.

The SPI unit is enabled via the `SPI_CT_EN` bit. The idle clock polarity is configured via the `SPI_CT_CPHA` bit and can be low (0) or high (1) during idle. Data is shifted in/out with MSB first when the `SPI_CT_DIR` bit is cleared; data is sifted in/out LSB-first when the flag is set. The data quantity to be transferred within a single transmission is defined via the `SPI_CT_SIZEx` bits. The unit supports 8-bit ("00"), 16-bit ("01"), 24-bit ("10") and 32-bit ("11") transfers. Whenever a transfer is completed, an interrupt is triggered when the `SPI_CT_IRQ_EN` bit is set. A transmission is still in progress as long as the `SPI_CT_BUSY` flag is set. T he SPI controller features 8 dedicated chip-select lines. These lines are controlled via the control register's `SPI_CT_CSx` bits. When the CSx bit is set, the according chip select line `spi_csn_o(x)` goes low (low-active chip select lines)

The SPI clock frequency is defined via the 3 `SPI_CT_PRSCx` clock prescaler bits. The following prescalers are available:

`SPI_CT_PRSCx`	`000`	`001`	`010`	`011`	`100`	`101`	`110`	`111`
Resulting prescaler:	2	4	8	64	128	1024	2048	4096

Based on the `SPI_CT_PRSCx` configuration, the actual SPI clock frequency f_{SPI} is determined by:

$$f_{SPI} = \frac{f_{main}[Hz]}{2 \cdot Prescaler}$$

A transmission is started when writing data to the `SPI_DATA` register. The data must be LSB-aligned. So if the SPI transceiver is configured for less than 32-bit transfers data quantity, the transmit data must be placed into the lowest 8/16/24 bit of `SPI_DATA`. Vice versa, the received data is also always LSB-aligned.

Register Map

Address	Name [C]	Bit(s) (Name) [C]		R/W	Function
0xFFFFFFA8	SPI_CT	0	SPI_CT_CS0	r/w	Direct chip select 0, csn(0) is low when set
		1	SPI_CT_CS1	r/w	Direct chip select 1, csn(1) is low when set
		2	SPI_CT_CS2	r/w	Direct chip select 2, csn(2) is low when set
		3	SPI_CT_CS3	r/w	Direct chip select 3, csn(3) is low when set
		4	SPI_CT_CS4	r/w	Direct chip select 4, csn(4) is low when set
		5	SPI_CT_CS5	r/w	Direct chip select 5, csn(5) is low when set
		6	SPI_CT_CS6	r/w	Direct chip select 6, csn(6) is low when set
		7	SPI_CT_CS7	r/w	Direct chip select 7, csn(7) is low when set
		8	SPI_CT_EN	r/w	SPI enable
		9	SPI_CT_CPHA	r/w	Idle clock polarity
		10	SPI_CT_PRSC0	r/w	Clock prescaler select bit 0
		11	SPI_CT_PRSC1	r/w	Clock prescaler select bit 1
		12	SPI_CT_PRSC2	r/w	Clock prescaler select bit 2
		13	SPI_CT_DIR	r/w	Shift direction (0: MSB first, 1: LSB first)
		14	SPI_CT_SIZE0	r/w	Transfer size (00: 8.bit, 01: 16-bit, 10: 24-bit, 11: 32-bit)
		15	SPI_CT_SIZE1	r/w	
		16	SPI_CT_IRQ_EN	r/w	Transfer done interrupt enable
		31	SPI_CT_BUSY	r/-	Ongoing transfer when set
0xFFFFFFAC	SPI_DATA	31:0		r/w	Receive/transmit data, LSS-aligned

Table 13: SPI transceiver register map

3.10. Two Wire Serial Interface Controller (TWI)

Overview

Hardware source file(s):	`neorv32_twi.vhd`	
Software driver file(s):	`neorv32_twi.c` `neorv32_twi.h`	
Top entity ports:	`twi_sda_io` `twi_scl_io`	Bi-directional serial data line Bi-directional serial clock line
Configuration generics:	`IO_TWI_USE`	Implement TWI when `true`
CPU interrupts:	`Fast IRQ channel 3`	Transmission done interrupt

Theory of Operation

The two wire interface – actually called I²C – is a quite famous interface for connecting several on-board components. Since this interface only needs two signals (the serial data line SDA and the serial clock line SCL) – despite of the number of connected devices – it allows easy interconnections of several peripheral nodes. The NEORV32 TWI implements a TWI **controller**. It features "**clock stretching**", so a slow peripheral can halt the transmission by pulling the SCL line low. **Currently no multi-controller support is available. Also, the TWI unit cannot operate in peripheral mode.**

The TWI is enabled via the control register `TWI_CT_EN` bit. The user program can start / terminate a transmission by issuing a START or STOP condition. These conditions are generated by setting the according bit (`TWI_CT_START` or `TWI_CT_STOP`) in the control register.

Data is send by writing a byte to the `TWI_DATA` register. Received data can also be obtained from this register. The TWI controller is busy (transmitting or performing a START or STOP condition) as long as the `TWI_CT_BUSY` bit in the control register is set.

An accessed peripheral has to acknowledge each transferred byte. When the `TWI_CT_ACK` bit is set after a completed transmission, the accessed peripheral has send an acknowledge. If it is cleared after a transmission, the peripheral has send a not-acknowledge (NACK). The NEORV32 TWI controller can also send an ACK (→ controller acknowledge "MACK") after a transmission by pulling SDA low during the ACK time slot. Set the `TWI_CT_MACK` bit to activate this feature. If this bit is cleared, the ACK/NACK of the peripheral is sampled in this time slot (normal mode).

In summary, the following independent TWI operations can be triggered by the application program:

- send START condition (also as REPEATED START condition)
- send STOP condition
- send (at least) one byte while also sampling one byte from the bus

The serial clock (SCL) and the serial data (SDA) lines can only be actively driven low by the controller. Hence, external pull-up resistors are required for the SDA and SCL lines.

The TWI clock frequency is defined via the 3 TWI_CT_PRSCx clock prescaler bits. The following prescalers are available:

TWI_CT_PRSCx	000	001	010	011	100	101	110	111
Resulting prescaler:	2	4	8	64	128	1024	2048	4096

Based on the TWI_CT_PRSCx configuration, the actual TWI clock frequency f_{SCL} is determined by:

$$f_{SCL} = \frac{f_{main}[Hz]}{4 \cdot Prescaler}$$

Register Map

Address	Name [C]	Bit(s) (Name) [C]		R/W	Function
0xFFFFFFB0	TWI_CT	0	TWI_CT_EN	r/w	TWI enable
		1	TWI_CT_STAT	0/w	Generate START condition
		2	TWI_CT_STOP	0/w	Generate STOP condition
		3	TWI_CT_IRQ_EN	r/w	Transmission-done interrupt enable
		4	TWI_CT_PRSC0	r/w	Clock prescaler select bit 0
		5	TWI_CT_PRSC1	r/w	Clock prescaler select bit 1
		6	TWI_CT_PRSC2	r/w	Clock prescaler select bit 2
		7	TWI_CT_MACK	r/w	Generate controller ACK for each transmission
		30	TWI_CT_ACK	r/-	ACK received when set
		31	TWI_CT_BUSY	r/-	Transfer in progress when set
0xFFFFFFB4	TWI_DATA	7:0	TWI_DATA	r/-	Receive/transmit data

Table 14: TWI register map

3.11. Pulse Width Modulation Controller (PWM)

Overview

Hardware source file(s):	`neorv32_pwm.vhd`	
Software driver file(s):	`neorv32_pwm.c` `neorv32_pwm.h`	
Top entity ports:	`pwm_o`	4-channel PWM output
Configuration generics:	`IO_PWM_USE`	Implement PWM controller when `true`
CPU interrupts:	`none`	

Theory of Operation

The PWM controller implements a pulse-width modulation controller with four independent channels and 8-bit resolution per channel. It is based on an 8-bit counter with four programmable threshold comparators that control the actual duty cycle of each channel. The controller can be used to drive a fancy RGB-LED with 24-bit true color, to dim LCD backlights or even for motor control. An external integrator (RC low-pass filter) can be used to smooth the generated “analog” signals.

The PWM controller is activated by setting the `PWM_CT_EN` bit in the module’s control register. When this flag is cleared, the unit is reset and all PWM output channels are set to zero. The base clock for the PWM generation is defined via the 3 `PWM_CT_PRSCx` bits. The 8-bit duty cycle for each channel, which represents the channel’s “intensity", is defined via the according 8-bit `PWM_DUTY_CHx` byte in the `PWM_DUTY` register.

Based on the duty cycle `PWM_DUTY_CHx` the according analog output voltage (relative to the IO supply voltage) of each channel can be computed by the following formula:

$$Intensity_{xx} = \frac{\text{PWM\_DUTY\_CHx}}{2^8}\,\%$$

The frequency of the generated PWM signals is defined by the PWM operating clock. This clock is derived from the main processor clock and divided by a prescaler via the 3 `PWM_CT_PRSCx` bits in the unit’s control register. The following prescalers are available:

`PWM_CT_PRSCx`	`000`	`001`	`010`	`011`	`100`	`101`	`110`	`111`
Resulting prescaler:	2	4	8	64	128	1024	2048	4096

The resulting PWM frequency is defined by:

$$f_{PWM} = \frac{f_{main}}{2^8 \cdot Prescaler}$$

Register Map

Address	Name [C]	Bit(s) (Name) [C]		R/W	Function
0xFFFFFFB8	PWM_CT	0	PWM_CT_EN	r/w	PWM controller enable
		1	PWM_CT_PRSC0	r/w	Clock prescaler select bit 0
		2	PWM_CT_PRSC1	r/w	Clock prescaler select bit 1
		3	PWM_CT_PRSC2	r/w	Clock prescaler select bit 2
0xFFFFFFBC	PWM_DUTY	7:0	PWM_DUTY_CH0	r/w	8-bit duty cycle for channel 0
		15:8	PWM_DUTY_CH1	r/w	8-bit duty cycle for channel 1
		23:16	PWM_DUTY_CH2	r/w	8-bit duty cycle for channel 2
		31:24	PWM_DUTY_CH3	r/w	8-bit duty cycle for channel 3

Table 15: PWM controller register map

3.12. True Random Number Generator (TRNG)

Overview

Hardware source file(s):	`neorv32_trng.vhd`	
Software driver file(s):	`neorv32_trng.c` `neorv32_trng.h`	
Top entity ports:	`none`	
Configuration generics:	`IO_TRNG_USE`	Implement TRNG when `true`
CPU interrupts:	`none`	

This device is still highly experimental!

Theory of Operation

The NEORV32 true random number generator provides true random numbers for your application. Instead of using a pseudo RNG like a LFSR, the TRNG of the processor uses a simple, straight-forward ring oscillator as physical entropy source. Hence, voltage and thermal fluctuations are used to provide true physical random data. It features a platform independent architecture based on two papers which are cited at the bottom of the following pages.

When the `TRNG_CT_EN` bit is set, the TRNG starts operation. Make sure to configure the GARO taps using the `TRNG_CT_TAPx` bits in advance. As soon as the `TRNG_DATA_VALID` bit in the `TRNG_DATA` register is set, the current sampled 16-bit random data can be obtained from the lowest 16 bits of the `TRNG_DATA` register. Note, that the TRNG needs at least 16 clock cycles to generate a new random byte. During this sampling time the current output random data is kept in the output register until a valid sampling of the new byte has completed.

Architecture

The NEORV32 TRNG is based on the *GARO **Ga**lois **R**ing **O**scillator TRNG*[5]. Basically, this architecture is an asynchronous LFSR constructed from a chain of inverters. Before the output signal of one oscillator is passed to the input of the next one, the signal can be XORed with the final output signal of the inverter chain (see image below) using a switching mask (f).

The default setup of the TRNG uses a total of 16 inverters and a software configurable GARO tap maks. To prevent the synthesis tool from doing logic optimization and thus, removing all but one inverter, the TRNG uses simple latches to decouple an inverter and its actual output. The latches are reset when the TRNG is disabled and are enabled one by one by a simple shift register when the TRNG is activated. By this, the TRNG provides a platform independent architecture[6] since no specific VHDL attributes are required.
The single-bit output signal of the GARO array is fed through flip flops to eliminate any metastability beyond this point. Afterwards, a Von-Neuman de-biasing is applied to get rid of any any bias introduced by the GARO array. If the de-biasing fails, an additional cycle is required to obtain a now random sample. This process might replicate depending on the quality of the GARo oscillation.

5 "Enhancing the Randomness of a Combined True Random Number Generator Based on the Ring Oscillator Sampling Method" by Mieczyslaw Jessa and Lukasz Matuszewski
6 "Extended Abstract: The Butterfly PUF Protecting IP on every FPGA" by Sandeep S. Kumar, Jorge Guajardo, Roel

The single-bit output signal of the GARO array is fed through flip flops to eliminate any metastability beyond this point. Afterwards, a Von-Neuman de-biasing is applied to get rid of any any bias introduced by the GARO array. If the de-biasing fails, an additional cycle is required to obtain a now random sample. This process might replicate depending on the quality of the GARO oscillation.

This de-biased signal is used as input for a simple chaos machine post-processing to provide a 'better' uniform distribution. This chaos machine is implemented as a 16-bit LFSR. As soon as 16 valid bits (so no errors during the de-biasing) have bin sampled, the resulting data is moved to the output register and is available for fetching by the CPU bus.

Register Map

Address	Name [C]	Bit(s) (Name) [C]		R/W	Function
0xFFFFFFC0	TRNG_CT	15:0	TRNG_CT_TAP	r/w	16-bit GARo tap mask configuration
		31	TRNG_CT_EN	r/w	TRNG enable
0xFFFFFFC4	TRNG_DATA	15:0	TRNG_DATA	r/-	Random data output
		31	TRNG_DATA_VALID	r/-	Random data valid when set

Table 16: TRNG register map

3.13. Dummy Device (DEVNULL)

Overview

Hardware source file(s):	`neorv32_devnull.vhd`	
Software driver file(s):	`none`	
Top entity ports:	`none`	
Configuration generics:	`IO_DEVNULL_USE`	Implement DEVNULL when `true`
CPU interrupts:	`none`	

Theory of Operation

Just like the device file `/dev/null`, the DEVNULL unit discards any data written to it as always returns zero when reading from it. The bus access to this unit always succeeds (when the unit is implemented). It is primarily meant for testing or if you need to make a data read access (e.g., from a peripheral device), where the read access itself triggers some action and you do not actually need the return data.

```
// not so good:
volatile uint32_t dst = SOME_IO_REG;

// better:
DEVNULL_DATA = SOME_IO_REG;
```

Register Map

Address	Name [C]	Bit(s)	R/W	Function
0xFFFFFFC8	DEVNULL_DATA	31:0	r/w	Write has no effect, read always return 0; the bus access always succeeds
		7:0	-/w	Write ASCII data to simulator console and logging filde

Table 17: DEVNULL register map

Simulation Usage

When writing data to `DEVNULL_DATA` in a simulation, the lowest 8 bit of the written data will be printed as ASCII char to the simulator's console. Additionally, this ASCII data will be written to a file called `neorv32.devnull.out` in the simulation home folder. All written data is also dumped as 32-bit hexadecimal value into a file called `neorv32.devnull.data.out` also in the simulation home folder.

More information regarding the simulation-only usage of the DEVNULL device can be found in chapter 5.12. Simulating the Processor.

3.14. System Configuration Information Memory (SYSINFO)

Overview

Hardware source file(s):	neorv32_sysinfo.vhd	
Software driver file(s):	none	
Top entity ports:	none	
Configuration generics:	*	Shows the settings of most config. generics
CPU interrupts:	none	

Theory of Operation

The SYSINFO allows the application software to determine the settings of most of the processor's top entity generics. All registers of this unit are read-only.

This devices is always implemented – regardless of the actual hardware configuration. The bootloader as well as the NEORV32 software runtime environment require information (like memory layout) for correct operation.

Register Map

Address	Name [C]	R/W	Function
0xFFFFFFE0	SYSINFO_CLK	r/-	Clock speed in Hz (via CLOCK_FREQUENCY generic)
0xFFFFFFE4	SYSINFO_USER_CODE	r/-	Custom user code, assigned via the USER_CODE generic
0xFFFFFFE8	SYSINFO_FEATURES	r/-	Implemented hardware (see next table)
0xFFFFFFEC	-	r/-	*reserved*
0xFFFFFFF0	SYSINFO_ISPACE_BASE	r/-	Instruction address space base (via MEM_ISPACE_BASE generic)
0xFFFFFFF4	SYSINFO_ISPACE_SIZE	r/-	Instruction address space size in bytes (via MEM_ISPACE_SIZE generic)
0xFFFFFFF8	SYSINFO_DSPACE_BASE	r/-	Data address space base (via MEM_DSPACE_BASE generic)
0xFFFFFFFC	SYSINFO_DSPACE_SIZE	r/-	Data address space size in bytes (via MEM_ISPACE_SIZE generic)

Table 18: SYSINFO register map

SYSINFO_FEATURES

Bit#	Name [C]	Function
25	SYSINFO_FEATURES_IO_DEVNULL	Set when DEVNULL is implemented (via the IO_DEVNULL_USE generic)
24	SYSINFO_FEATURES_IO_TRNG	Set when the TRNG is implemented (via the IO_TRNG_USE generic)
23	-	-
22	SYSINFO_FEATURES_IO_WDT	Set when the WDT is implemented (via the IO_WDT_USE generic)
21	SYSINFO_FEATURES_IO_PWM	Set when the PWM is implemented (via the IO_PWM_USE generic)
20	SYSINFO_FEATURES_IO_TWI	Set when the TWI is implemented (via the IO_TWI_USE generic)
19	SYSINFO_FEATURES_IO_SPI	Set when the SPI is implemented (via the IO_SPI_USE generic)
18	SYSINFO_FEATURES_IO_UART	Set when the UART is implemented (via the IO_UART_USE generic)
17	SYSINFO_FEATURES_IO_MTIME	Set when the MTIME is implemented (via the IO_MTIME_USE generic)
16	SYSINFO_FEATURES_IO_GPIO	Set when the GPIO is implemented (via the IO_GPIO_USE generic)
4	SYSINFO_FEATURES_MEM_INT_DMEM	Set when the processor-internal IMEM is implemented (via the MEM_INT_IMEM_USE generic)
3	SYSINFO_FEATURES_MEM_INT_IMEM_ROM	Set when the processor-internal IMEM is read-only (via the MEM_INT_IMEM_ROM generic)
2	SYSINFO_FEATURES_MEM_INT_IMEM	Set when the processor-internal DMEM implemented (via the MEM_INT_DMEM_USE generic)
1	SYSINFO_FEATURES_MEM_EXT	Set when the external Wishbone bus interface is implemented (via the MEM_EXT_USE generic)
0	SYSINFO_FEATURES_BOOTLOADER	Set when the processor-internal bootloader is implemented (via the BOOTLOADER_USE generic)

4. Software Architecture

To make actual use of the processor, the NEORV32 project comes with a complete software ecosystem. This ecosystem consists of the following elementary parts.

Application and bootloader start-up codes	`sw/common/bootloader_crt0.S` `sw/common/crt0.S`
Application and bootloader linker scripts	`sw/common/bootloader_neorv32.ld` `sw/common/neorv32.ld`
Core hardware driver libraries	`sw/lib/include/` `sw/lib/source/`
Makefiles	E.g. `sw/example/blink_led/makefile`
Auxiliary tool for generating NEORV32 executables	`sw/image_gen/`
Default booloader	`sw/bootloader/bootloader.c`

The complete software ecosystem is based on the RISC-V port of the GCC GNU Compiler Collection.

Last but not least, the NEORV32 ecosystem provides some example programs for testing the hardware, for illustrating the usage of peripherals and for general getting in touch with the project.

4.1. Toolchain

The toolchain for this project is based on the free RISC-V GCC-port. You can find the compiler sources and build instructions on the official RISC-V GNU toolchain GitHub page: https://github.com/riscv/riscv-gnu-toolchain. The NEORV32 uses a 32-bit base integer architecture (`rv32i`) and a 32-bit integer and soft-float ABI (`ilp32`), so make sure you build an according toolchain.

Alternatively, you can download a prebuilt `rv32i/e` toolchain for 64-bit x86 Linux from: github.com/stnolting/riscv_gcc_prebuilt

More information regarding the toolchain (building from scratch or downloading the prebuilt ones) can be found in chapter 5.1. Toolchain Setup.

4.2. Core Software Libraries

The NEORV32 project provides a set of C libraries that allow an easy usage of all of the core's peripheral and CPU features. All you need to do is to include the main NEORV32 library file in your application's source file(s):

```
#include <neorv32.h>
```

Together with the makefile, this will automatically include all the processor's header files located in `sw/lib/include` into your application. The actual source files of the core libraries are located in `sw/lib/source` and are automatically included into the source list of your software project. The following files are currently part of the NEORV32 core library:

C source file	C header file	Function
-	`neorv32.h`	Main NEORV32 definitions and library file.
`neorv32_cpu.c`	`neorv32_cpu.h`	HW driver functions for the NEORV32 CPU.
`neorv32_gpio.c`	`neorv32_gpio.h`	HW driver functions for the GPIO.
`neorv32_mtime.c`	`neorv32_mtime.h`	HW driver functions for the MTIME.
`neorv32_pwm.c`	`neorv32_pwm.h`	HW driver functions for the PWM.
`neorv32_rte.c`	`neorv32_rte.h`	NEORV32 runtime environment helper functions.
`neorv32_spi.c`	`neorv32_spi.h`	HW driver functions for the SPI.
`neorv32_trng.c`	`neorv32_trng.h`	HW driver functions for the TRNG.
`neorv32_twi.c`	`neorv32_twi.h`	HW driver functions for the TWI.
`neorv32_uart.c`	`neorv32_uart.h`	HW driver functions for the UART.
`neorv32_wdt.c`	`neorv32_wdt.h`	HW driver functions for the WDT.

Documentation

All core library functions are highly documented using doxygen. To generate the HTML-based documentation, navigate to the project's `docs` folder and execute doxygen using the provided doxygen makefile:

```
neorv32/docs$ doxygen doxygen_makefile_sw
```

This will generate (or update) the `docs/doxygen_build` folder. To view the documentation, open the `docs/doxygen_build/html/index.html` file with your browser of choice. Click on the "files" tab to see a list of all documented files.

The SW documentation is automatically built and deployed to GitHub pages by Travis CI. The online documentation is available at: https://stnolting.github.io/neorv32/files.html

4.3. Application Makefile

Application compilation is based on a single GNU makefile. Each project in the `sw/example` folder features a makefile. All these makefiles are identical. When creating a new project, copy an existing project folder or at least the makefile to your new project folder. I suggest to create new projects also in `sw/example` to keep the file dependencies. Of course, these dependencies can be manually configured via makefiles varibales when your project is located somewhere else.

Before you can use the makefiles, you need to install the RISC-V GCC toolchain. Also, you have to add the installation folder of the compiler to your system's PATH variable. More information can be found in chapter 5. Let's Get It Started!.

The makefile is invoked by simply executing `make` in your console:

```
neorv32/sw/example/blink_led$ make
```

4.3.1. Makefile Targets

Just executing `make` will show the help menu showing all available targets. The following targets are available:

`help`	Show a short help text explaining all available targets.
`check`	Check the toolchain. You should run this target at least once after installation.
`info`	Show the makefile configuration (see next chapter).
`compile`	Compile all sources and generate `compile` executable for upload via bootloader
`install`	Compile all sources, generate executable (via `compile` target) for upload via bootloader and generate and install IMEM VHDL initialization image file `rtl/core/neorv32_application_image.vhd`.
`all`	Execute `compile` and `install`.
`clean`	Remove all generated files in the current folder.
`clean_all`	Remove all generated files in the current folder and also removes the compiled core libraries and the compiled image generator tool.
`bootloader`	Compile all sources, generate executable and generate and install BOOTROM VHDL initialization image file `rtl/core/neorv32_bootloader_image.vhd`. This target uses the bootloader-specific start-up code (`sw/common/bootloader_crt0.S`) and linker script (`sw/common/bootloader_neorv32.ld`) instead.

4.3.2. Makefile Configuration

The compilation flow is configured via variables right at the beginning of the makefile:

```
# ################################################################################
# USER CONFIGURATION
# ################################################################################
# Compiler effort
EFFORT = -Os

# User's application sources (add additional files here)
APP_SRC = $(wildcard *.c)

# User's application include folders (don't forget the '-I' before each entry)
APP_INC = -I .

# Compiler toolchain (use default if not set by user)
RISCV_TOOLCHAIN ?= riscv32-unknown-elf

# CPU architecture and ABI
MARCH = -march=rv32i
MABI  = -mabi=ilp32

# Path to runtime c library (use default if not set by user)
LIBC_PATH   ?= $(dir $(shell which $(CC)))../$(RISCV_TOOLCHAIN)/lib/libc.a
LIBGCC_PATH ?= $(dir $(shell which $(CC)))../lib/gcc/$(RISCV_TOOLCHAIN)/*/libgcc.a

# Relative or absolute path to the NEORV32 home folder (use default if not set by user)
NEORV32_HOME ?= ../../..
# ################################################################################
```

Description of Makefile Configuration Variables

`EFFORT`	Optimization level, optimize for size (`-Os`) is default; legal values: `-O0` `-O1` `-O2` `-O3` `-Os`
`APP_SRC`	The *.c source files of the application. *.c-files in the current folder are automatically added via wildcard. Additional files can be added; separated by white spaces
`APP_INC`	Include file folders; separated by white spaces; must be defined with `-I` prefix
`RISCV_TOOLCHAIN`	The toolchain to be used; follows the naming convention architecture-vendor-output
`MARCH`	The architecture of the RISC-V CPU. Only RV32 is supported by the NEORV32. Enable compiler support of optional CPU extension by adding the according extension letter (e.g. `rv32im` for `M` CPU extension).
`MABI`	The default 32-bit integer ABI. Do not change.
`LIBC_PATH`	Location of the standard C library.
`LIBGCC_PATH`	Locations of the standard GCC C-library.
`NEORV32_HOME`	Relative or absolute path to the NEORV32 project home folder. Adapt this if the makefile/project is not in the project's `sw/example` folder.

The makefile configuration variable can be re-defined directly when invoking the makefile:
`$ make MARCH=-march=rv32ic clean_all compile`

4.4. Executable Image Format

When all the application sources have been compiled and linked, a final executable file has to be generated. For this purpose, the makefile uses the NEORV32-specific linker script `sw/common/neorv32.ld` to map all the sections into only four final sections: `.text`, `.rodata`, `.data` and `.bss`. These four section contain everything required for the application to run:

`.text`	Executable instructions generated from the start-up code and all application sources
`.rodata`	Constants (like strings) from the application; also the initial data for initialized variables
`.data`	This section is required for the address generation of fixed (= global) variables only
`.bss`	This section is required for the address generation of dynamic memory constructs only

The `.text` and `.rodata` sections are mapped to processor's instruction memory space and the `.data` and `.bss` sections are mapped to the processor's data memory space.

Finally, the `.text`, `.rodata` and `.data` sections are extracted and concatenated into a single file `main.bin`. This file is parsed by the NEORV32 image generator (`sw/image_gen`) to generate the final executable. The image generator can generate three types of executables, selected by a flag when calling the generator:

`-app_bin`	Generates an executable binary file `neorv32_exe.bin` (for UART uploading via the bootloader)
`-app_img`	Generates an executable VHDL memory initialization image for the processor-internal IMEM. This option generates the `rtl/core/neorv32_application_image.vhd` file.
`-bld_img`	Generates an executable VHDL memory initialization image for the processor-internal BOOT ROM. This option generates the `rtl/core/neorv32_bootloader_image.vhd` file.

All these options are managed by the makefile – so you don't actually have to think about them. The normal application compilation flow will generate the `neorv32_exe.bin` file in the current software project folder ready for upload via the UART to NEORV32 bootloader.

This executable version has a very small header consisting of three 32-bit words located right at the beginning of the file. This header is generated by the image generator (`sw/image_gen`). The image generator is automatically compiled when invoking the makefile.

The first word of the executable is the signature word and is always `0x4788CAFE`. Based on this word, the bootloader can identify a valid image file. The next word represents the size in bytes of the actual program image. A simple "complement" checksum of the actual program image is given by the third word. This provides a simple protection against data transmission or storage errors.

4.5. Bootloader

The default bootloader (`sw/bootloader/bootloader.c`) of the NEORV32 processor allows you to upload new program executable at every time. If you have an external SPI flash connected to the processor (for example the FPGA configuration memory), you can store the program executable to it and the system can directly boot it after reset without any user interaction.

The bootloader is only implemented when the `BOOTLOADER_USE` generic is `true` and requires the CSR access CPU extension (`CPU_EXTENSION_RISCV_Zicsr` generic is `true`).

The bootloader requires the UART for manual executable upload or SPI flash programming (`IO_UART_USE` generic is `true`).

For the automatic boot from an SPI flash, the SPI controller has to be implemented (`IO_SPI_USE` generic is `true`) and the machine system timer MTIME has to be implemented (`IO_MTIME_USE` generic is `true`), too.

To interact with the bootloader, attach the UART signals (`uart_txd_o` and `uart_rxd_o`) of the processor's top entity via a COM port (-adapter) to a computer, configure your terminal program using the following settings and perform a reset of the processor.

Terminal console settings (19200-8-N-1):

- `19200 Baud`
- `8 data bits`
- `No parity bit`
- `1 stop bit`
- `Newline on \r\n (carriage return, newline)`
- `No transfer protocol for sending data, just the raw byte stuff`

The bootloader uses the LSB of the top entity's `gpio_o` output port as high-active status LED (all other output pin are set to low level by the bootloader). After reset, this LED will start blinking at ~2Hz and the following intro screen should show up in your terminal:

```
<< NEORV32 Bootloader >>

BLDV: Jul  2 2020
HWV:  0.1.0.1
CLK:  0x05F5E100 Hz
USER: 0x00000000
MISA: 0x42801104
CONF: 0x01FF0015
IMEM: 0x00008000 bytes @ 0x00000000
DMEM: 0x00002000 bytes @ 0x80000000

Autoboot in 8s. Press key to abort.
```

The uploaded executables are always stored to the instruction space starting at the base address of the instruction space.

This start-up screen also gives some brief information about the bootloader version and several system parameters:

`BLDV`	Bootloader version (built time).
`HWV`	Processor hardware version (from the `mimpid` CSR).
`USER`	Custom user code (from the `USER_CODE` generic).
`CLK`	Processor clock speed in Hz (via the `mclock` CSR from the `CLOCK_FREQUENCY` generic).
`MISA`	CPU extensions (from the `misa` CSR).
`CONF`	Processor configuration (via the `mfeatures` CSR from the IO and MEM config. generics).
`IMEM`	Instructions memory base address and size in byte (via the `mispacebase` & `mispacesize` CSRs from the `MEM_ISPACE_BASE` & `MEM_ISPACE_SIZE` generics).
`DMEM`	Data memory base address and size in byte (via the `mdspacebase` & `mdspacesize` CSRs from the `MEM_DSPACE_BASE` & `MEM_DSPACE_SIZE` generics).

Now you have 8 seconds to press any key. Otherwise, the bootloader starts the auto boot sequence. When you press any key within the 8 seconds, the actual bootloader user console starts:

```
<< NEORV32 Bootloader >>

BLDV: Jul  2 2020
HWV:  0.1.0.1
CLK:  0x05F5E100 Hz
USER: 0x00000000
MISA: 0x42801104
CONF: 0x01FF0015
IMEM: 0x00008000 bytes @ 0x00000000
DMEM: 0x00002000 bytes @ 0x80000000

Autoboot in 8s. Press key to abort.
Aborted.

Available commands:
 h: Help
 r: Restart
 u: Upload
 s: Store to flash
 l: Load from flash
 e: Execute
CMD:>
```

The auto-boot countdown is stopped and now you can enter a command from the list to perform the corresponding operation:

- **`h`**: Show the help text (again)
- **`r`**: Restart the bootloader and the auto-boot sequence
- **`u`**: Upload new program executable (`neorv32_exe.bin`) via UART into the instruction memory
- **`s`**: Store executable to SPI flash at `spi_csn_o(0)`
- **`l`**: Load executable from SPI flash at `spi_csn_o(0)`
- **`e`**: Start the application, which is currently stored in the instruction memory

A new executable can be uploaded via UART by executing the `u` command. The executable can be directly executed via the `e` command. To store the recently uploaded executable to an attached SPI flash press `s`. To directly load an executable from the SPI flash press `l`. The bootloader and the auto-boot sequence can be manually restarted via the `r` command.

4.5.1. Auto Boot Sequence

When you reset the NEORV32processor, the bootloader waits 8 seconds for a user console input before it starts the automatic boot sequence. This sequence tries to fetch a valid boot image from the external SPI flash, connected to SPI chip select `spi_csn_o(0)`. If a valid boot image is found and can be successfully transferred into the instruction memory, it is automatically started. If no SPI flash was detected or if there was no valid boot image found, the bootloader stalls and the status LED is permanently activated.

4.5.2. External SPI Flash for Booting

If you want the NEORV32 bootloader to automatically fetch and execute an application at system start, you can store it to an external SPI flash. The advantage of the external memory is to have a non-volatile program storage, which can be re-programmed at any time just by executing some bootloader commands. Thus, no FPGA bitstream recompilation is required at all.

SPI Flash Requirements

The bootloader can access an SPI compatible flash via the processor top entity's SPI port and connected to chip select `spi_csn_o(0)`. The flash must be capable of operating at least at 1/8 of the processor's main clock. Only single read and write byte operations are used. The address has to be 24 bit long. Furthermore, the SPI flash has to support at least the following commands:

- `READ (0x03)`
- `READ STATUS (0x05)`
- `WRITE ENABLE (0x06)`
- `PAGE PROGRAM (0x02)`
- `SECTOR ERASE (0xD8)`
- `READ ID (0x9E)`

Compatible (FGPA configuration) SPI flash memories are for example the **Winbond W25Q64FV** or the **Micron N25Q032A**.

SPI Flash Configuration

The base address `SPI_FLASH_BOOT_ADR` for the executable image inside the SPI flash is defined in the "user configuration" section of the bootloader source code (`sw/bootloader/bootloader.c`). Most FPGAs, that use an external configuration flash, store the golden configuration bitstream at base address 0. Make sure there is no address collision between the FPGA bitstream and the application image. You need to change the default sector size if your Flash has a sector size greater or less than 64kB:

```
/** SPI flash boot image base address */
#define SPI_FLASH_BOOT_ADR     0x00800000

/** SPI flash sector size in bytes */
#define SPI_FLASH_SECTOR_SIZE  (64*1024)
```

For any change you made inside the bootloader, you have to recompile the bootloader (5.10. Re-Building the Internal Bootloader) and do a new synthesis of the processor.

4.5.3. Bootloader Error Codes

If something goes wrong during the bootloader operation, an error code is shown. In this case, the processor stalls, a bell command and one of the following error codes is send to the terminal, the status LED is permanently activated and the system must be manually reset.

`ERR_0`	If you try to transfer an invalid executable (via UART or from the external SPI flash), this error message shows up. Also, if no SPI flash was found during a boot attempt, this message will be displayed.
`ERR_1`	Your program is way too big for the internal processor's instructions memory. Increase the memory size or reduce (optimize!) your application code.
`ERR_2`	This indicates a checksum error. Something went wrong during the transfer of the program image (upload via UART or loading from the external SPI flash). If the error was caused by a UART upload, just try it again. When the error was generated during a flash access, the stored image might be corrupted.
`ERR_3`	This error occurs if the attached SPI flash cannot be accessed. Make sure you have the right type of flash and that it is properly connected to the NEORV32 SPI port using chip select #0.
`ERR_4`	The instruction memory is marked as read-only. Set the `MEM_INT_IMEM_ROM` generic to `false` to allow write accesses.
`ERR_5`	This error pops up when an exception was triggered. Such an error with exception code "0x00000002" will be generated when you try to boot from the instruction memory, but no valid executable has been loaded yet.

4.5.4. Final Notes

The bootloader is intended to work independently of the actual hardware (-configuration). Hence, it should be compiled with the minimal base ISA only. The current version of the bootloader uses the `rv32i` ISA – so it will not work on `rv32e` architectures. To make the bootloader work on embedded CPU, recompile it using the `rv32e` ISA (see chapter 5.10. Re-Building the Internal Bootloader).

4.6. NEORV32 Runtime Environment

The software architecture of the NEORV32 comes with a minimal runtime environment that takes care of clean application start and also of all interrupts and exceptions during execution.

The initial part of the runtime environment is the `sw/common/crt0.asm` application start-up code. This piece of code is automatically linked with every application program and represents the starting point for every application. Hence, it is directly executed after reset. The start-up code performs the following operations:

- Initialize all data registers `x1` – `x31` (`x1` – `x15` only for embedded CPU mode) with zero.
- Setup stack-pointer (`sp`): The stack always starts at the very end of the data address space (`DSPACEBASE` + `DSPACESIZE` – 4).
- Initialize the global pointer (`gp`) according to the `.data` segment layout provided by the linker script.
- Clear IO area: Write zero to all memory-mapped registers in the IO region. If certain devices have not been implemented, a bus access fault exception will occur. This exception is also processed by the start-up code.
- Clear the `.bss` section defined by the linker script.
- Copy read-only data from the `.text` section to the `.data` section to initialize initialized variables.
- Call the application's `main` function (with no arguments).
- If the main function return, the processor goes to an endless sleep mode (using a simple loop or the `WFI` instruction if implemented).

Using the NEORV32 Runtime Environment (RTE)

After system start-up, the runtime environment is responsible for catching all implemented exceptions and interrupts. To install and activate the NEORV32 RTE, execute the following function:

```
void neorv32_rte_setup(void);
```

This setup initializes the RISC-V-compliant `mtvec` CSR, which provides the base address for all instruction and exception handlers. The address stored to this register reflects the *first-level exception handler* provided by the NEORV32 RTE. Whenever an exception or interrupt is triggered, this *first-level handler* is called.

The *first-level handler* performs a complete context save, analyzes the source of the exception/interrupt and calls the according *second-level exception* handler, which actually takes care of the exception/interrupt. For this, the RTE manages a private look-up table to store the according trap handlers.

After the initial setup of the RTE, each entry in the trap handler look-up table is initialized with a debug handler, that outputs detailed hardware information via UART when triggered. This is intended as a fall-back for debugging or accidentally triggered exceptions/interrupts.

For instance, an illegal instruction exception catched by the RTE might look like this:

```
<RTE> Illegal instruction @0x000002d6, MTVAL=0x00001537 </RTE>
```

To install the **actual application's trap handlers**, the NEORV32 RTE provides function for installing and uninstalling trap handler for each implemented exception/interrupt.

```
int neorv32_rte_exception_install(uint8_t id, void (*handler)(void));
```

The following `id` exception IDs are available:

ID name [C]	Description / exception or interrupt causing event
`RTE_TRAP_I_MISALIGNED`	Instruction address misaligned
`RTE_TRAP_I_ACCESS`	Instruction (bus) access fault
`RTE_TRAP_I_ILLEGAL`	Illegal instruction
`RTE_TRAP_BREAKPOINT`	Breakpoint (EBREAK instruction)
`RTE_TRAP_L_MISALIGNED`	Load address misaligned
`RTE_TRAP_L_ACCESS`	Load (bus) access fault
`RTE_TRAP_S_MISALIGNED`	Store address misaligned
`RTE_TRAP_S_ACCESS`	Store (bus) access fault
`RTE_TRAP_MENV_CALL`	Environment call from machine mode (ECALL instruction)
`RTE_TRAP_MTI`	Machine timer interrupt (via MTIME)
`RTE_TRAP_MEI`	Machine external interrupt
`RTE_TRAP_MSI`	Machine software interrupt
`RTE_TRAP_FIRQ_0`	Fast interrupt channel 0
`RTE_TRAP_FIRQ_1`	Fast interrupt channel 1
`RTE_TRAP_FIRQ_2`	Fast interrupt channel 2
`RTE_TRAP_FIRQ_03`	Fast interrupt channel 3

When installing a custom handler function for any of these exception/interrupts, make sure the function uses no attributes (especially no *interrupt* attribute!), has no arguments and no return value like in the following example:

```
void handler_xyz(void) {

  // handle exception/interrupt...
}
```

Do **NOT** use the `((interrupt))` attribute for the application exception handler functions! This will place an `mret` instruction to the end of it making it impossible to return to the first-level exception handler, which will cause stack corruption.

Example: Installation of the MTIME interrupt handler:

```
neorv32_rte_exception_install(EXC_MTI, handler_xyz);
```

To remove a previously installed exception handler, call the according uninstall function from the NEORV32 runtime environment. This will replace the previously installed handler by the initial debug handler, so even uninstalled exceptions and interrupts are further captured.

```
int neorv32_rte_exception_uninstall(uint8_t id);
```

Example: Removing the MTIME interrupt handler:

```
neorv32_rte_exception_uninstall(EXC_MTI);
```

More information regarding the NEORV32 runtime environment can be found in the `doxygen` software documentation (also available online).

5. Let's Get It Started!

To make your NEORV32 project run, follow the guides from the upcoming sections. Follow these guides step by step and in the presented order.

Keep in mind that – for instance – a `rv32imc` toolchain only provides library code compiled with compressed and mul/div instructions! Hence, this code cannot be executed (without emulation) on an architecture without these extensions!

5.1. Toolchain Setup

At first, we need to get the RISC-V GCC toolchain. There are two possibilities to do this:

- Download and compile the official RISC-V GNU toolchain
- Download and install a prebuilt version of the toolchain

Compilation of the toolchain is done using the guide from the official https://github.com/riscv/riscv-gnu-toolchain GitHub page. I have done that on my computer and you can download my prebuilt version from https://github.com/stnolting/riscv_gcc_prebuilt.

The default toolchain for this project is `riscv32-unknown-elf`.
Of course you can use any other RISC-V toolchain. Just change the `RISCV_TOOLCHAIN` variable in the application makefile(s) according to your needs.

Besides of the RISC-V GCC, you will need a native GCC to compile the NEORV32 image generator.

5.1.1. Making the Toolchain from Scratch

The official RISC-V repository uses submodules. You need the --recursive option to fetch the submodules automatically:

```
$ git clone --recursive https://github.com/riscv/riscv-gnu-toolchain
```

Download and install the prerequisite standard packages:

```
$ sudo apt-get install autoconf automake autotools-dev curl python3 libmpc-dev libmpfr-dev libgmp-dev gawk build-essential bison flex texinfo gperf libtool patchutils bc zlib1g-dev libexpat-dev
```

To build the Linux cross-compiler, pick an install path. If you choose, say, `/opt/riscv`, then add `/opt/riscv/bin` to your `PATH` now.

```
$ export PATH:$PATH:/opt/riscv/bin
```

Then, simply run the following commands in the RISC-V GNU toolchain source folder (for `rv32gc`):

```
riscv-gnu-toolchain$ ./configure --prefix=/opt/riscv --with-arch=rv32gc –with-abi=ilp32
riscv-gnu-toolchain$ make
```

After a while (hours!) you will get `riscv32-unknown-elf-gcc` and all of its friends in your `/opt/riscv/bin` folder.

5.1.2. Downloading and Installing the Prebuilt Toolchain

Alternatively, you can download a prebuilt version of the toolchain. I have compiled the toolchain on a 64-bit x86 Ubuntu (Ubuntu on Windows, actually):

```
$ git clone https://github.com/stnolting/riscv_gcc_prebuilt.git
```

Alternatively, you can directly download the according toolchain archive from:
https://github.com/stnolting/riscv_gcc_prebuilt

Unpack the archive and copy the content to a location in your file system (e.g. `/opt/riscv`).

Of course, you can also use any other prebuilt version of the toolchain. Make sure it supports the `rv32i/e` architecture and uses the `ilp32` or `ilp32e` ABI.

5.1.3. Installation

Now you have the binaries. The last step is to add them to your `PATH` environment variable (if you have not already done so). Make sure to add the binaries folder (`bin`) of your toolchain.

```
$ export PATH:$PATH:/opt/riscv/bin
```

You should add this command to your `.bashrc` (if you are using bash) to automatically add the RISC-V toolchain at every console start.

5.1.4. Testing the Installation

To make sure everything works fine, navigate to an example project in the NEORV32 example folder and execute the following command:

```
neorv32/sw/example/blink_led$ make check
```

This will test all the tools required for the NEORV32. Everything is working fine if `Toolchain check OK` appears at the end.

5.2. General Hardware Setup

The following steps are required to generate a bitstream for your FPGA board. If you want to run the **NEORV32 processor** in simulation only, the following steps might also apply.

In this tutorial we will use a test implementation of the **processor** – using most of the processor's optional modules but just propagating the minimal signals to the outer world. Hence, this guide is intended as evaluation or "hello world" project to check out the NEORV32. A little note: The order of the following steps might be a little different for your specific EDA tool.

1. Create a new project with your FPGA EDA tool of choice.

2. Add all VHDL files from the project's `rtl/core` folder to your project. Make sure to *reference* the files only – do not copy them.

3. Make sure to add all the rtl files to a new **library** called `neorv32`. If your FPGA tools does not provide a field to enter the library name, check out the "properties" menu of the rtl files.

4. The `rtl/core/neorv32_top.vhd` VHDL file is the top entity of the NEORV32 processor. If you already have a design, instantiate this unit into your design and proceed. If you do not have a design yet and just want to check out the NEORV32 – no problem! In this guide we will use a simplified top entity: Add the `rtl/core/top_templates/neorv32_test_setup.vhd` VHDL file to your project too, and select it as top entity. This test setup provides a minimal test hardware setup:

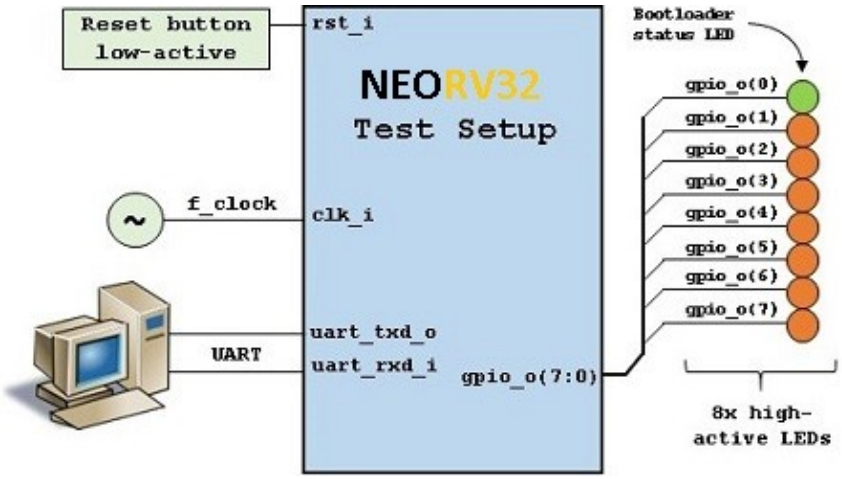

Figure 6: Hardware configuration of the NEORV32 test setup

5. This test setup only implements some very basic processor and CPU features. Also, only the minimum number of signals is propagated to the outer world.

6. The configuration of the NEORV32 processor is done using the generics of the instantiated processor top entity. Let's keep things simple at first and use the default configuration (see below). But there is one generic, that has to be set according to your FPGA / board: The clock frequency of the top's clock input signal (`clk_i`). Use the `CLOCK_FREQUENCY` generic to specify your clock source's frequency in Hertz (Hz) (→ the default value, that you need to adapt, is marked in **orange**).

```
neorv32_top_inst: neorv32_top
generic map (
  -- General --
  CLOCK_FREQUENCY              => 100000000, -- in Hz
  BOOTLOADER_USE               => true,
  CSR_COUNTERS_USE             => true,
  USER_CODE                    => x"00000000",
  -- RISC-V CPU Extensions --
  CPU_EXTENSION_RISCV_C        => false,
  CPU_EXTENSION_RISCV_E        => false,
  CPU_EXTENSION_RISCV_M        => false,
  CPU_EXTENSION_RISCV_Zicsr    => true,
  CPU_EXTENSION_RISCV_Zifencei => true,
  -- Physical Memory Protection (PMP) --
  PMP_USE                      => false,
  PMP_NUM_REGIONS              => 4,
  PMP_GRANULARITY              => 15,
  -- Memory configuration: Instruction memory --
  MEM_ISPACE_BASE              => x"00000000",
  MEM_ISPACE_SIZE              => 16*1024, -- in BYTES
  MEM_INT_IMEM_USE             => true,
  MEM_INT_IMEM_SIZE            => 16*1024, -- in BYTES
  MEM_INT_IMEM_ROM             => false,
  -- Memory configuration: Data memory --
  MEM_DSPACE_BASE              => x"80000000",
  MEM_DSPACE_SIZE              => 8*1024, -- in BYTES
  MEM_INT_DMEM_USE             => true,
  MEM_INT_DMEM_SIZE            => 8*1024, -- in BYTES
  -- Memory configuration: External memory interface --
  MEM_EXT_USE                  => false,
  MEM_EXT_REG_STAGES           => 2,
  MEM_EXT_TIMEOUT              => 15,
  -- Processor peripherals --
  IO_GPIO_USE                  => true,
  IO_MTIME_USE                 => true,
  IO_UART_USE                  => true,
  IO_SPI_USE                   => false,
  IO_TWI_USE                   => false,
  IO_PWM_USE                   => false,
  IO_WDT_USE                   => true,
  IO_TRNG_USE                  => false,
  IO_DEVNULL_USE               => true
)
```

7. If you feel like it – or if your FPGA does not provide enough resources – you can modify the memory sizes (`MEM_INT_IMEM_SIZE` and `MEM_INT_DMEM_SIZE`, marked in **red** and **blue**) or exclude certain peripheral modules from implementation. But as mentioned above, let's keep things simple and use the standard configuration for now. We will use the processor-internal data and instruction memories for the test setup. So make sure, the instruction and data space sizes are always equal to the sizes of the internal memories (i.e. `MEM_INT_IMEM_SIZE` == `MEM_ISPACESIZE` and `MEM_INT_DMEM_SIZE` == `MEM_DSPACESIZE`).

Keep the internal instruction and data memory sizes in mind – these values are required for setting up the software framework in the next chapter.

8. Depending on your FPGA tool of choice, it is time to assign the signals of the test setup top entity to the according pins of your FPGA board. All the signals can be found in the entity declaration:

```
entity neorv32_test_setup is
  port (
    -- Global control --
    clk_i      : in  std_ulogic := '0'; -- global clock, rising edge
    rstn_i     : in  std_ulogic := '0'; -- global reset, low-active, async
    -- GPIO --
    gpio_o     : out std_ulogic_vector(7 downto 0); -- parallel output
    -- UART --
    uart_txd_o : out std_ulogic; -- UART send data
    uart_rxd_i : in  std_ulogic := '0' -- UART receive data
  );
end neorv32_test_setup;
```

9. Attach the clock input `clk_i` to your clock source and connect the reset line `rstn_i` to a button of your FPGA board. Check whether it is low-active or high-active – the reset signal of the processor must be **low-active**, so maybe you need to invert the input signal. If possible, connected at least bit #0 of the GPIO output port `gpio_o` to a high-active LED (invert the signal when your LEDs are low-active). Finally, connect the UART signals `uart_txd_o` and `uart_rxd_i` to your serial host interface (dedicated pins, USB-to-serial converter, etc.).

10. Perform the project HDL compilation (synthesis, mapping, bitstream generation).

11. Download the generated bitstream into your FPGA ("program" it) and press the reset button (just to make sure everything is sync).

12. Done! If you have assigned the bootloader status LED (bit #0 of the GPIO output port), it should be flashing now and you should receive the bootloader start prompt via the UART.

5.3. General Software Framework Configuration

While your synthesis tool is crunching the NEORV32 HDL files, it is time to configure the project's software framework for your processor hardware.

1. You need to tell the linker the size of the processor's instruction and data memories. We have just configured the test setup – so you should remember the memory configuration.

2. Open the application linker script `sw/common/neorv32.ld` with a text editor. Right at the beginning of the linker script you will find the memory configuration:

```
MEMORY
{
  rom  (rx) : ORIGIN = 0x00000000, LENGTH = 16*1024
  ram (rwx) : ORIGIN = 0x80000000, LENGTH =  8*1024
}
```

3. There are four parameters that are relevant here: The origin and the length of the instruction memory (named `rom`) and the origin and the length of the data memory (named `ram`). These four parameters have to be always sync to your hardware memory configuration:

The `rom` `ORIGIN` parameter has to be equal to the configuration of the `MEM_ISPACE_BASE` generic.
The `rom` `LENGTH` parameter has to be equal to the configuration of the `MEM_ISPACE_SIZE` generic.

The `ram` `ORIGIN` parameter has to be equal to the configuration of the `MEM_DSPACE_BASE` generic.
The `ram` `LENGTH` parameter has to be equal to the configuration of the `MEM_DSPACE_SIZE` generic.

5.4. Building the Software Documentation

If you wish, you can generate the documentation of the NEORV32 software framework. This doxygen-based documentation illustrates the core libraries as well as all the example programs. A deployed version of the documentation can be found online at **GitHub pages**.

1. Make sure `doxygen` is installed. Navigate to the `docs` folder and generate the documentation files using the provided doxygen makefile:

```
neorv32/docs$ doxygen doxygen_makefile_sw
```

2. Doxygen will generate a HTML-based documentary. The output files are placed in (a new folder) `docs/doxygen_build/html`. Move to this folder and open `index.html` with your browser. Click on the "files" tab to see an overview of all documented files.

5.5. Application Program Compilation

1. Open a terminal console and navigate to one of the project's example programs. For example the simple `sw/example_blink_led` program. This program uses the NEORV32 `GPIO` unit to display an 8-bit counter on the lowest eight bit of the `gpio_o` port.

2. To compile the project, execute:

```
neorv32/sw/example/blink_led$ make compile
```

3. This will compile and link the application sources together with all the included libraries. At the end, your application is put into an ELF file (main.elf). The image generator process takes this file and creates a final executable. The makefile will show the resulting memory utilization and the executable size in the console:

```
neorv32/sw/example/blink_led$ make compile
Memory utilization:
   text    data     bss     dec     hex filename
    852       0       0     852     354 main.elf
Executable (neorv32_exe.bin) size in bytes:
864
```

4. That's it. The compile target has created the actual executable (`neorv32_exe.bin`) in the current folder, which is ready to be uploaded to the processor via the bootloader and a UART interface.

5.6. Uploading and Starting of a Binary Executable Image via UART

We have just created the executable. Now it is time to upload it to the processor. In this tutorial, we will use **TeraTerm** as an exemplary serial terminal program for **Windows**, but the general procedure is the same for other terminal programs, build environments or operating systems.

Make sure your terminal program can transfer the executable in raw byte mode without any protocol stuff around it.

1. Connect the UART interface of your FPGA (board) to a COM port of your computer or use an USB-to-serial adapter.

2. Start a terminal program. In this tutorial, I am using TeraTerm for Windows. You can download it from **https://ttssh2.osdn.jp/index.html.en**

3. Open a connection to the corresponding COM port. Configure the terminal according to the following parameters:

   - `19200 Baud`
   - `8 data bits`
   - `1 stop bit`
   - `No parity bits`
   - `No transmission/flow control protocol (just raw byte mode)`
   - `Newline on \r\n = carriage return & newline (if configurable at all)`

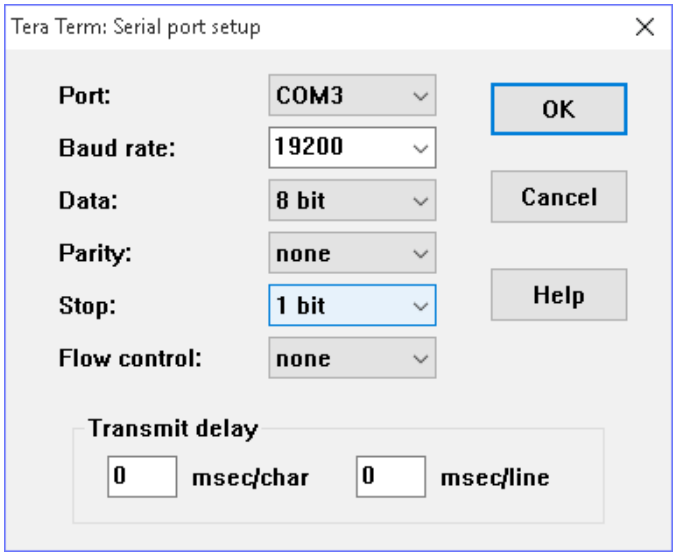

Figure 7: Serial configuration of TeraTerm

4. Also make sure, that single chars are transmitted without any consecutive “new line” or “carriage return” commands (this is highly dependent on your terminal application of choice, TeraTerm only sends the raw chars by default).

5. Press the NEORV32 reset button to restart the bootloader. The status LED starts blinking and the bootloader intro screen appears in your console. Hurry up and press any key (hit space!) to abort the automatic boot sequence and to start the actual bootloader user interface console.

```
<< NEORV32 Bootloader >>

BLDV: Jul  2 2020
HWV:  0.1.0.1
CLK:  0x05F5E100 Hz
USER: 0x00000000
MISA: 0x42801104
CONF: 0x01FF0015
IMEM: 0x00008000 bytes @ 0x00000000
DMEM: 0x00002000 bytes @ 0x80000000

Autoboot in 8s. Press key to abort.
Aborted.

Available commands:
 h: Help
 r: Restart
 u: Upload
 s: Store to flash
 l: Load from flash
 e: Execute
CMD:>
```

6. Execute the “Upload” command by typing `u`. Now the bootloader is waiting for a binary executable to be send.

```
CMD:> u
Awaiting neorv32_exe.bin...
```

7. Use the “send file” option of your terminal program to transmit the previously generated binary executable `neorv32_exe.bin`.

8. Again, make sure to transmit the executable in **raw binary mode** (no transfer protocol, no additional header stuff). When using TeraTerm, select the “binary” option in the send file dialog:

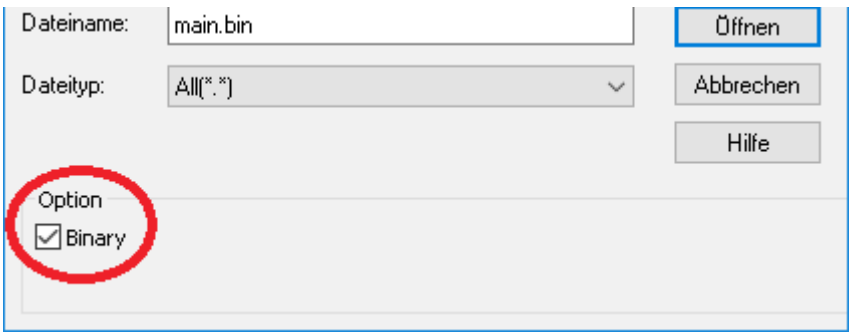

Figure 8: Transfer executable in binary mode (German version of TeraTerm)

9. If everything went fine, **`OK`** will appear in your terminal:

```
CMD:> u
Awaiting neorv32_exe.bin... OK
```

10. The executable now resides in the instruction memory of the processor. To execute the program right now execute the "Execute" command by typing `e`.

```
CMD:> u
Awaiting neorv32_exe.bin... OK
CMD:> e
Booting…

Blinking LED demo program
```

11. Now you should see the LEDs counting.

5.7. Setup of a New Application Program Project

Done with all the introduction tutorials and those example programs? Then it is time to start your own application project!

1. The easiest way of creating a new project is to make a copy of an existing project (like the `blink_led` project) inside the `example` folder. By this, all file dependencies are kept and you can start coding and compiling.

2. If you want to have he project folder somewhere else, you need to adapt the project's makefile. In the makefile you will find a variable that keeps the relative or absolute path to the NEORV32 home folder. Just modify this variable according to your project's location:

```
# Relative or absolute path to the NEORV32 home folder (use default if not set by user)
NEORV32_HOME ?= ../../..
```

3. If your project contains additional source files outside of the project folder, you can add them to the `APP_SRC` variable:

```
# User's application sources (add additional files here)
APP_SRC = $(wildcard *.c) ../somewhere/some_file.c
```

4. You also need to add the folder containing the include files of your new project to the `APP_INC` variable (do not forget the `-I` prefix):

```
# User's application include folders (don't forget the '-I' before each entry)
APP_INC = -I . -I ../somewhere/include_stuff_folder
```

5. If you feel like it, you can change the default optimization level:

```
# Compiler effort
EFFORT = -Os
```

5.8. Enabling RISC-V CPU Extensions

Whenever you enable a RISC-V compliant CPU extensions via the `CPU_EXTENSION_RISCV_*` generics, you need to adapt the toolchain configuration so the compiler actually can make use of the extension.

To do so, open the makefile of your project (e.g., `sw/example/blink_led/makefile`) and scroll to the "USER CONFIGURATION" section right at the beginning of the file. You need to modify the `MARCH` and `MABI` variables according to your CPU hardware configuration.

```
# CPU architecture and ABI
MARCH = -march=rv32i
MABI  = -mabi=ilp32
```

The following table shows the different combinations of CPU extensions and the according configuration for the `MARCH` and `MABI` variables. Of course you can also just use a subset of the available extensions (e.g. `march=rv32im` for a `rv32imc` CPU).

Enabled CPU Extension(s)	Toolchain MARCH	Toolchain MABI
none	`MARCH=-march=rv32i`	`MABI = -mabi=ilp32`
`CPU_EXTENSION_RISCV_C`	`MARCH=-march=rv32ic`	
`CPU_EXTENSION_RISCV_M`	`MARCH=-march=rv32im`	
`CPU_EXTENSION_RISCV_C` `CPU_EXTENSION_RISCV_M`	`MARCH=-march=rv32imc`	
`CPU_EXTENSION_RISCV_E`	`MARCH=-march=rv32e`	`MABI = -mabi=ilp32e`
`CPU_EXTENSION_RISCV_E` `CPU_EXTENSION_RISCV_C`	`MARCH=-march=rv32ec`	
`CPU_EXTENSION_RISCV_E` `CPU_EXTENSION_RISCV_M`	`MARCH=-march=rv32em`	

`CPU_EXTENSION_RISCV_E`
`CPU_EXTENSION_RISCV_C`
`CPU_EXTENSION_RISCV_M`
	`MARCH=-march=rv32emc`	

The toolchain always supports the privileged instructions (like `ECALL` or CSR access instructions) regardless of the `MARCH` or `MABI` configuration. However, the compiler will not generate the according instructions by itself. Privileged instructions are only used when explicitly coded as inline assembly or when using according libraries. When the `CPU_EXTENSION_RISCV_Zicsr` extension is not synthesized, all these instructions will behave like NOPs. Instructions returning data will always return zero.

When using the embedded CPU mode (`CPU_EXTENSION_RISCV_E` generic set `true`) a C-library, which was compiled for the `ilp32e` ABI, is required.

The CSR access and the instruction fence extensions (`CPU_EXTENSION_RISCV_Zicsr` and `CPU_EXTENSION_RISCV_Zifencei`) is supported by all toolchain configurations and all ABIs and need no further makefile configuration.

5.9. Building a Non-Volatile Application (Program Fixed in IMEM)

The purpose of the bootloader is to allow an easy and fast update of the application being currently executed. But maybe at some time your project has become mature and you want to actually embed your processor including the application. Of course you can store the executable to the SPI flash and let the bootloader fetch and execute it a system start. But if you don't have an SPI flash available or you want a really fast start of your applications, you can directly implement your executable within the processor internal instruction memory. When using this approach, the bootloader is no longer required. To have your application to permanently reside in the internal instruction memory, follow the upcoming steps.

This works only for the internal instruction memory. Also make sure that the memory components the IMEM is mapped to support an initialization via the bitstream.

1. At first, compile your application code by running the `make install` command (the memory utilization is not shown again when your code has already been compiled):

```
neorv32/sw/example/blink_led$ make compile
Memory utilization:
   text    data     bss     dec     hex filename
    852       0       0     852     354 main.elf
Executable (neorv32_exe.bin) size in bytes:
864
Installing application image to ../../../rtl/core/neorv32_application_image.vhd
```

2. The `install` target has created an executable, too, but this time in the form of a VHDL memory initialization file. At synthesis, this initialization will become part of the final FPGA bitstream, which in terms initializes the IMEM's blockram.

3. You need the processor to directly execute the code in the IMEM. Deactivate the implementation of the bootloader via the top entity's generic:

```
BOOTLOADER_USE => false, -- implement processor-internal bootloader?
```

4. When the bootloader is deactivated, the according ROM is removed and the CPU will start booting at the base address of the instruction memory space. Thus, the CPU directly executed your application code after reset.

5. The IMEM could be still modified, since it is implemented as RAM. This might corrupt your executable. To prevent this and to implement the IMEM as true ROM (and eventually saving some more hardware resources), active the IMEM as ROM feature using the processor's top entity generic:

```
MEM_INT_IMEM_ROM => true, -- implement processor-internal instruction memory as ROM
```

6. Perform a synthesis and upload your new bitstream. Your application code resides now unchangeable in the processor's IMEM and is directly executed after reset.

5.10. Re-Building the Internal Bootloader

If you have modified any of the configuration parameters of the default bootloader (in `sw/bootloader/bootloader.c`), if you have added additional features or if you have implemented your own bootloader, you need to re-compile and re-install the bootloader.

1. The NEORV32 default bootloader uses 4kB of boot ROM space. This is also the default boot ROM size. If your new/modified bootloader exceeds this size, you need to modify the boot ROM configurations.

2. Open the processor's main package file `rtl/core/neorv32_package.vhd` and edit the `boot_size_c` constant according to your requirements. The boot ROM size **must not exceed 32kB** and should be a power of two (for optimal hardware mapping).

```
-- Bootloader ROM --
constant boot_size_c : natural := 4*1024; -- bytes
```

3. Now open the bootloader linker script `sw/common/bootloader_neorv32.ld` and adapt the `LENGTH` parameter of the `bootrom` according to your new memory size. `boot_size_c` and `LENGTH` have to be always identical.

```
MEMORY
{
  bootrom  (rx) : ORIGIN = 0xFFFF0000, LENGTH = 4*1024
}
```

4. Compile and install the bootloader using the explicit `bootloader` makefile target. This target uses the bootloader-specific start-up code and linker script instead of the regular application files.

```
neorv32/sw/bootloader$ make bootloader
```

5. Now perform a new synthesis / HDL compilation to update the bitstream with the new bootloader image.

The bootloader is intended to work regardless of the actual NEORV32 hardware configuration – especially when it comes to CPU extensions. Hence, the bootloader should be build using the minimal `rv32i` ISA only (`rv32e` would be even better).

See chapter 4.5. Bootloader for more information regarding the bootloader.

5.11. Programming the Bootloader SPI Flash

1. At first, reset the NEORV32 processor and wait until the bootloader start screen appears in your terminal program.

2. Abort the auto boot sequence and start the user console by pressing any key.

3. Press `u` to upload the program image, that you want to store to the external flash:

```
CMD:> u
Awaiting neorv32_exe.bin...
```

4. Send the binary in raw binary via your terminal program. When the uploaded is completed and `OK` appears, press `p` to trigger the programming of the flash (do not execute the image via the `e` command as this might corrupt the image):

```
CMD:> u
Awaiting neorv32_exe.bin... OK
CMD:> p
Write 0x000013FC bytes to SPI flash @ 0x00800000? (y/n)
```

5. The bootloader shows the size of the executable and the base address inside the SPI flash where the executable is going to be stored. A prompt appears: Type `y` to start the programming or type `n` to abort.

```
CMD:> u
Awaiting neorv32_exe.bin... OK
CMD:> p
Write 0x000013FC bytes to SPI flash @ 0x00800000? (y/n) y
Flashing... OK
CMD:>
```

6. If `OK` appears in the terminal line, the programming process was successful. Now you can use the auto boot sequence to automatically boot your application from the flash at system start-up without any user interaction.

See chapter 4.5. Bootloader for more information regarding the bootloader.

5.12. Simulating the Processor

The NEORV32 project features a simple testbench (`sim/neorv32_tb.vhd`) that can be used to simulate and test the processor and the CPU itself. This testbench features a 100MHz clock and enables all optional peripheral devices and all optional CPU extensions (but not the embedded CPU mode).

Please note that the true-random number generator (TRNG) **CANNOT** be simulated due to its combinatorial oscillator architecture.

The simulated NEORV32 does not use the bootloader and directly boots the current application image (from the `rtl/core/neorv32_application_image.vhd` image file). Make sure to use the `all` target of the makefile to **install** your application as VHDL image after compilation:

```
sw/example/blink_led$ make clean_all all
```

Simulation Console Output

Data written to the NEORV32 UART transmitter is send to a virtual UART receiver implemented within the testbench. This receiver uses the default (bootloader) UART configuration. Received chars are send to the simulator console and are also stored to a file (`neorv32.testbench_uart.out`) in the simulator home folder.

Faster Simulation Console Output

When printing data via the UART the communication will always be based on the configured BAUD rate. For a simulation this will take a very long time. To have a faster output you can send data to the `DEVNULL` device (see chapter 3.13. Dummy Device (DEVNULL)). ASCII data written to this device will be immediately printed to the simulator console. Additionally, the ASCII data is logged in a file (`neorv32.devnull.out`) in the simulator home folder. All written data is also dumped as 32-bit hexadecimal value into a file called `neorv32.devnull.data.out` in the simulation home folder.

You can also redirect all data written to the UART transmitter for sending directly to the `DEVNULL` simulation output. Hence, the UART transmitter is not used at all. To enable this redirection just compile and install your application and add `DEVNULL_UART_OVERRIDE` to the compiler `USER_FLAGS` variable (do not forget the `-D` suffix flag):

```
sw/example/blink_led$ make USER_FLAGS+=-DDEVNULL_UART_OVERRIDE clean_all all
```

The DEVNULL simulation output (to file and to screen) outputs “complete lines” at once. A line is completed with a line feed (newline, ASCII `\n` = 10).

Simulation with Xilinx Vivado

The project features a Vivado simulation waveform configuration in `sim/vivado`.

Simulation with GHDL

To simulate the processor using **GHDL** navigate to the `sim` folder and run the provided shell script. The simulation time can be configured in the script via the `--stop-time=4ms` argument.

```
neorv32/sim$ sh ghdl_sim.sh
```

5.13. Continuous Integration

This project uses continuous integration provided by Travis CI. The project includes a `.travis.yml` file for configuring Travis CI. This configuration file uses the continuous integration scripts located in `.ci`.

What the continuous integration does so far:

- Builds the doxygen-based software documentation and deploys it to GitHub pages
- Downloads, unpacks and installs the pre-built GCC toolchain
- Test the toolchain
- Compile all example projects from the `sw/example` folder
- Compile the bootloader from the `sw/bootloader` folder
- Compile and install the CPU test code from the `sw/bootloader/cpu_test` folder, the generated executable uses the DEVNULL simulation output
- Simulate the processor using its default testbench (`sim/neorv32_tb.vhd`) using GHDL
- The DEVNULL output is searched for a reference string; if the string is found the test was successful

6. Troubleshooting

If your setup does not work as expected, scroll through the following point. Maybe you have missed something during setup. If you are still encountering problems, open a new issue on GitHub or contact me.

- Check the correct installation of the toolchain with a `$ make check`.
- Check the synthesis tool for errors and warnings. Double-check the timing report.
- Does the processor simulate correctly?
- Synthesis tools can be a little bit obscure sometimes. Use the default synthesis options and do not start with a target frequency of 800MHz for your first setup.
- If your application does not run, make a clean rebuild: `$ make clean_all compile`
- Always use the debug feature of the NEORV32 runtime environment.
- Make sure your hardware configuration (like memory sizes, CPU extensions,...) is always sync with the toolchain (linker script configuration, targeted architecture (`march`), ABI (`mabi`),...).
- Make sure to have the latest version of the project (do a `git pull`) or a stable release.
- More to come...

7. Change Log

Date (DD.MM.YYYY)	HW version	Modifications
23.06.2020	`0.0.2.3`	Publication
25.06.2020	`0.0.2.5`	Added DEVNULL device; added chapter regarding processor simulation; fixed/ added links; fixed typos; added FPGA implementation results for iCE40 UP
05.07.2020	`1.0.0.0`	New CPU architecture: Fetch and execute engines; increased CPI; timer and counter CSRs are now all 64-bit wide; fixed CSR access errors; fixed C.LW decompression logic; `misa` flags C and M are now r/w – compressed mode and multiplier/divider support can be switched on/off during runtime; PC(0) is now always zero; fixed bug in multiplier/divider co-processor; renamed SPI signals; added RISC-V compliance check information – **processor now passes the official RISC-V compliance tests**
06.07.2020	`1.0.1.0`	Added missing `fence` instruction; added new generic to enable optional `Zifencei` CPU extension for instruction stream synchronization
09.07.2020	`1.0.5.0`	`X` flag of `misa` CSR is zero now; the default SPI flash boot address of the bootloader is now `0x0080000`; new exemplary FPGA utilization results for Intel, Lattice and Xilinx; `misa` CSR is read-only again, switching compressed extension on/off is pretty bad for the fetch engine; `mtval` and `mcause` CSRs now allow write accesses and are finally RISC-V-compliant; time low and high registers of MTIME peripheral can now also be written by user; MTIME registers only allow full-word write accesses
10.07.2020	`1.0.6.0`	Non-taken branches are now 1 cycle faster; the `time[h]` CSR now correctly reflects the system time from the MTIME unit; fixed `WFI` instruction permanently stalling the CPU; `[m]cycle[h]` counters now stop counting when CPU is in sleep mode; `minstret[h]` and `mcycle[h]` now also allow write-access
14.07.2020	`1.1.0.0`	Added `fence_o` and `fencei_o` signals to top entity to show if a `fence` or `fencei` instruction is executed; added `mvendorid` and `marchid` CSRs (both are always zero); ALU shift unit is faster now; two lowest bits of `mtvec` are always zero; fixed wrong instruction exception priority; removed HART_ID generic – `mhartid` CSR is always read as zero; performance counters (`[m]cycle[h]`, `[m]instret[h]` and `time[h]`) are also available in embedded mode – but can be explicitly disabled via the CSR_COUNTERS_USE generic; `mcause` CSR only allows write access to bit 31 and bits 3:0; updated synthesis reports
19.07.2020	`1.2.0.0`	CPU bus unit now has independent busses for instruction fetch and data access – merged into single processor bus via new bus switch unit; doubled speed of ALU shifter unit again; all bits of `mcause` CSR can now be modified by application program (full RISC-V-compliant); performance counters CSRs `[m]cycleh` and `[m]instreth` are only 20-bit wide; removed NEORV32-specific custom CSRs – all processor-related information can be obtained from the new SYSINFO IO module (CPU is now more independent from processor configuration); changed IO address of DEVNULL; fixed bug in bootloader's trap handler; added USER_CODE generic to assign a custom user code that can

Date (DD.MM.YYYY)	HW version	Modifications
		be read by software (from SYSINFO)
20.07.2020	`1.2.0.5`	Less penalty for taken branches and jumps (2 cycles faster)
21.07.2020	`1.2.0.6`	Added section regarding the CPU's data and instruction interfaces; optimized CPU fetch engine; updated iCE40 synthesis results
25.07.2020	`1.3.0.0`	`mcause` CSR is read-only now!; removed CLIC, added 4 fast IRQ channels to CPU with according flags in `mie` and `mip` and trap IDs; updated core libraries; updated NEORV32 RTE; highly reworked this document; updated synthesis and performance results
29.07.2020	`1.3.5.0`	Added *user privilege level*, enabled via new `CPU_EXTENSION_RISCV_U` generic; fixed error in `mstatus(mpie)` logic; implemented RISC-V spec.-compliant *Physical Memory Protection* (PMP); allows up to 8 regions but only `NAPOT` mode is supported yet
30.07.2020	`1.3.5.1`	Fixed bug(s) in PMP mask generation; `misa(Z)` is not yet defined by the RISC-V specs., hence it is read-only and read as zero