VLSI IA2

Q1) Indicate and draw design rules for diffusion layers and metal layers

Design Rules for Diffusion Layers (Active Layers)

Diffusion layers (often referred to as “active” layers) define the regions where transistors are formed and where interconnect diffusion occurs. These design rules ensure proper transistor formation and avoid unintended shorts.

Key Rules:

- **Minimum width:** 4λ (lambda-based rules) or 0.10 µm (micron rule for 65 nm).
- **Minimum spacing between diffusion regions:** 4λ or 0.12 µm.
- **Minimum spacing between opposite-type diffusions (e.g., n-diff and p-diff):** 0.25 µm.
- **Extension of active beyond poly gate (to define source/drain):** 2λ or 0.10 µm.
- **Polysilicon to diffusion spacing where no transistor is desired:** 1λ or 0.07 µm.

These rules help ensure that gates form correctly where poly crosses diffusion, and that no unintended transistors form elsewhere.

Design Rules for Metal Layers

Metal layers are used for routing interconnects. Each metal layer has specific width and spacing rules to ensure signal integrity, avoid shorts, and prevent issues like electromigration.

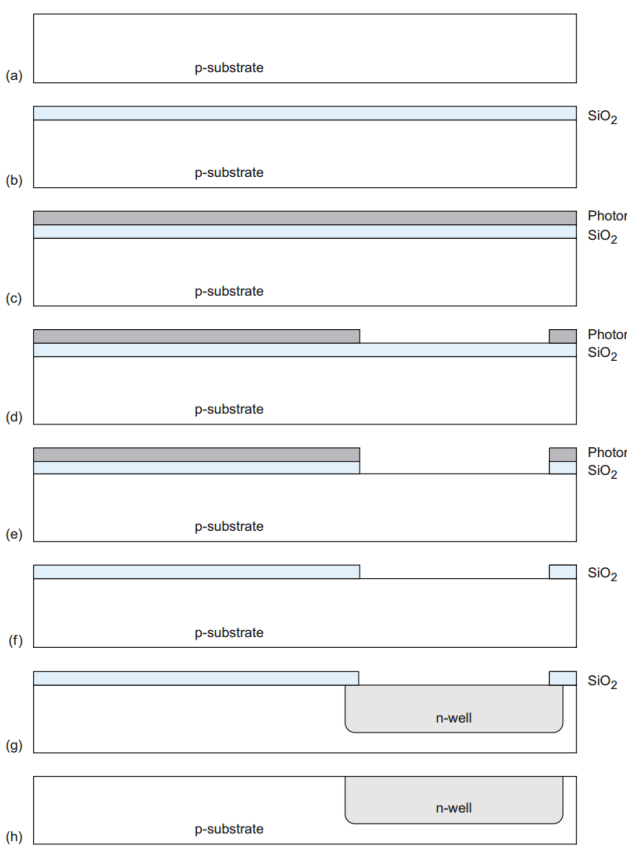
Key Rules for Metal Layers:

- **Minimum width and spacing:** 4λ each or about 0.13 µm (for Metal1).
- **Minimum width of upper-level metals (e.g., Metal3):** 6λ or wider, with increased spacing.
- **Metal slotting rule (for wide wires >10–40 µm):** Slots must be added to reduce stress and risk of electromigration.
- **Fat-metal rules:** Wider wires need greater spacing due to etching effects.
- **Electromigration rule:** Avoid long narrow metal wires carrying high current; use multiple vias and wider traces where possible.

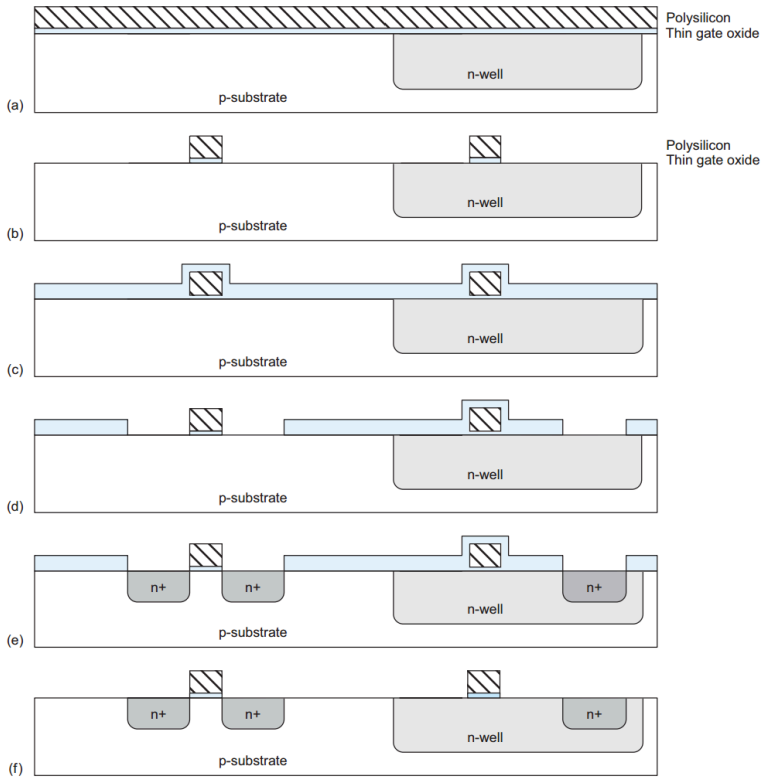
Q2) Explain nMOS fabrication process with diagram

Steps in nMOS Fabrication Process:

1. **Starting Substrate:**
   - Begin with a p-type silicon wafer.
2. **Formation of n-Well (optional for CMOS):**
   - Not required for nMOS-only processes, but used in CMOS.
   - A protective oxide is grown and patterned, and n-type dopants are implanted.
3. **Field Oxide Formation:**
   - Thick oxide is grown in isolation regions to prevent leakage between devices.
4. **Gate Oxide and Polysilicon Gate:**
   - Thin SiO_2 gate oxide is grown.
   - Polysilicon is deposited and patterned to form gate electrodes.
5. **n+ Source and Drain Formation:**



- Protective oxide is applied and patterned using n-diffusion mask.
- n+ regions are created using ion implantation.
- Self-aligned process ensures alignment of source/drain to gate.



6. **Contact Cuts and Metallization:**
    - Contacts are etched through oxide where metal will touch diffusion or poly.
    - Metal layer (usually aluminum) is deposited and patterned.
7. **Final Steps:**
    - A passivation layer is added for protection.
    - The wafer is then diced into individual chips.

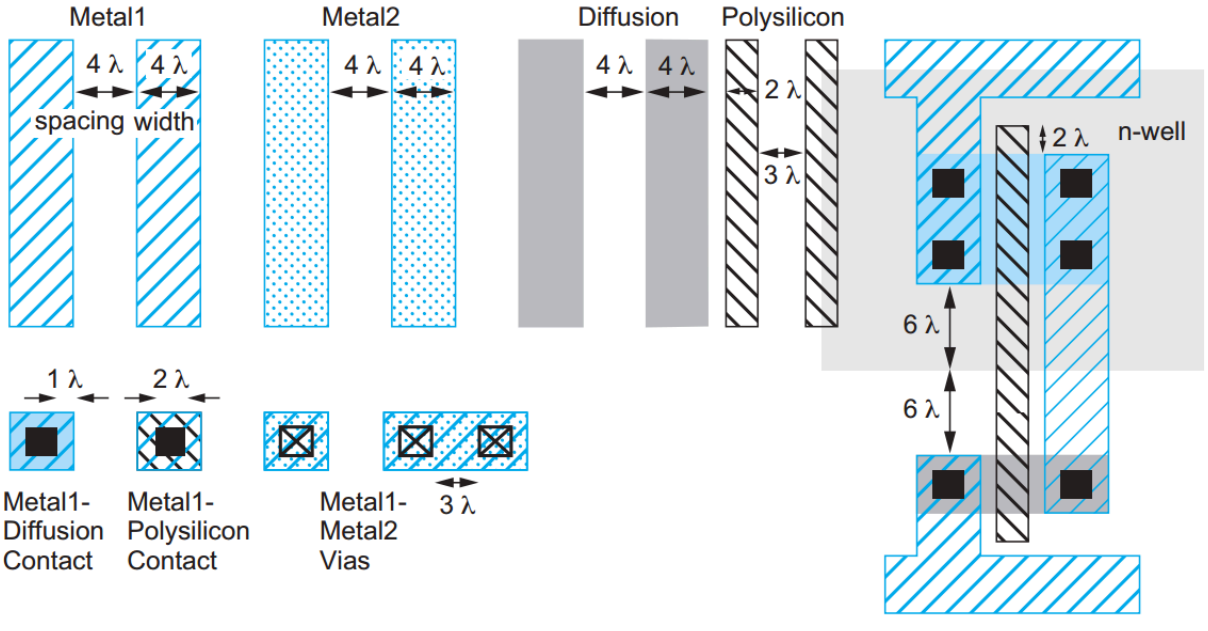
Q3) With neat diagram explain the lambda based design rules for pMOS or nMOS

Key Lambda-Based Rules:

Lambda (λ) rules simplify layout across different technology nodes by expressing distances and sizes as multiples of a single parameter λ (usually λ = 0.3 µm for educational 0.6 µm processes).

Layer	Minimum Width	Minimum Spacing
Diffusion	4λ	4λ
Polysilicon	2λ	2λ–3λ
Metal1	4λ	4λ
Metal2	4λ–6λ	4λ
Contact (to poly or diffusion)	2λ × 2λ	—
Poly to active (no transistor)	—	1λ
N-well to pMOS	—	6λ

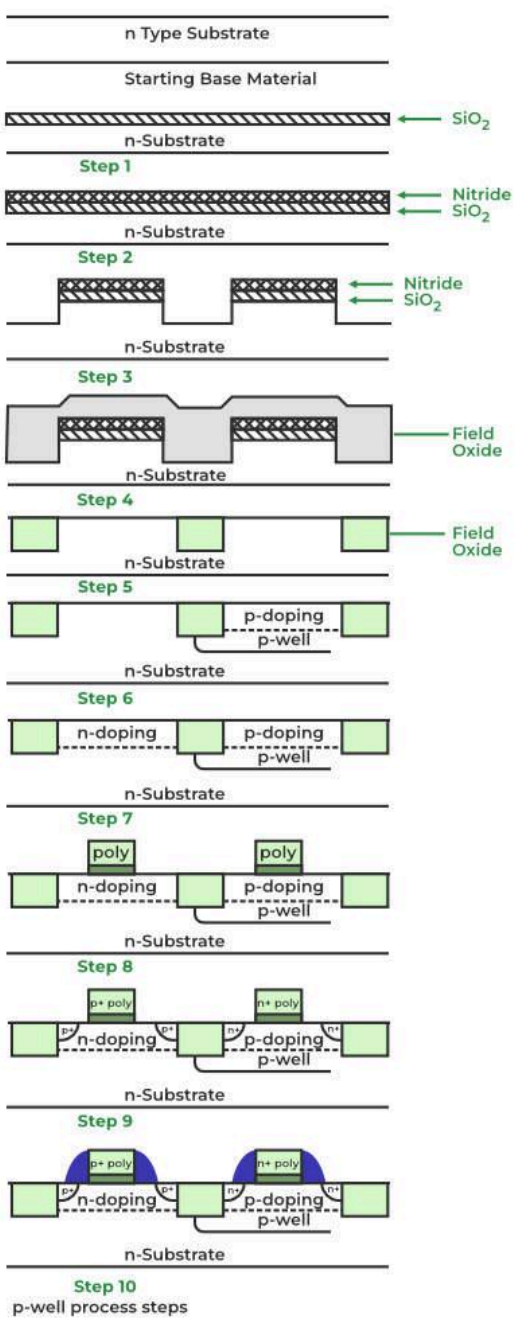
- **Transistor Gat e:** Formed where polysilicon crosses diffusion.
- **Poly overlap over diffusion (gate):** 2λ
- **N-well surrounds pMOS:** 6λ clearance



Q4) Explain the steps involved in fabrication of p-well cMOS transistor with the help of diagram

Fabrication Steps in p-well CMOS Process:

1. **Start with an n-type substrate.**
2. **Form the p-well:**
   - Grow a protective oxide layer.
   - Apply photoresist and use a p-well mask to expose desired p-well regions.
   - Etch the oxide and implant acceptor ions (e.g., boron) to form p-well regions.
3. **Field Oxide Formation:**
   - Grow thick field oxide to isolate active regions.
4. **Gate Oxide and Polysilicon Deposition:**
   - Grow thin gate oxide.
   - Deposit and pattern polysilicon to form transistor gates.
5. **n+ and p+ Source/Drain Implantation:**
   - Use separate masks to define nMOS (in p-well) and pMOS (in n-substrate) source/drain regions.
   - Perform ion implantation for n+ and p+ doping.



- This will also form n+ polysilicon gate and p+ polysilicon gate for NMOS and PMOS transistors respectively. Hence this process is called as self aligned process.

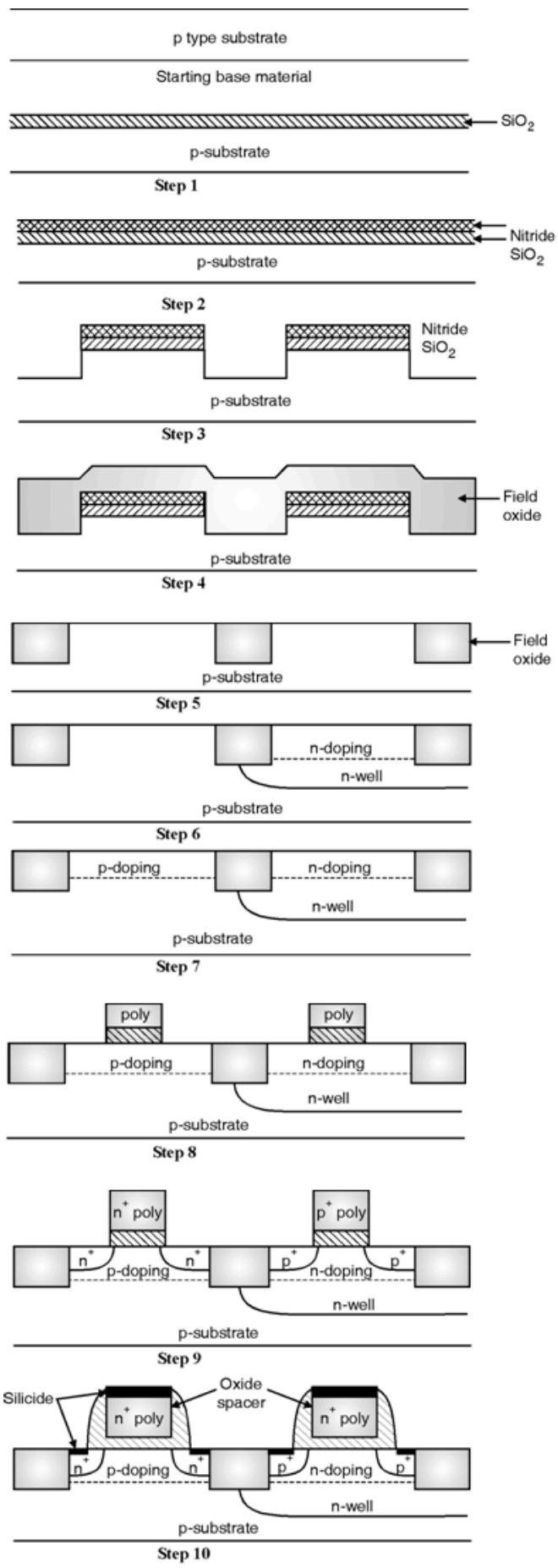
6. **Contact Formation:**
   - Etch contact holes through oxide.
   - Deposit metal (usually aluminum) and pattern to form interconnects.
7. **Final Passivation:**
   - Deposit passivation oxide for protection.

- Open pads for bonding as needed.

Q5) Explain the steps involved in fabrication of n-well cMOS transistor with the help of diagram

Fabrication Steps in n-well CMOS Process:

1. **Start with a p-type substrate.**
   - This forms the base on which NMOS and PMOS transistors will be built.
2. **Form the n-well:**
   - Grow a protective oxide layer.
   - Apply photoresist and use an n-well mask to expose desired n-well regions.
   - Etch the oxide and implant donor ions (e.g., phosphorus or arsenic) to form n-well regions.
   - Perform a high-temperature drive-in to diffuse dopants and form the well.
3. **Field Oxide Formation:**
   - Grow thick field oxide to isolate active regions.
4. **Gate Oxide and Polysilicon Deposition:**
   - Grow thin gate oxide.
   - Deposit and pattern polysilicon to form transistor gates.
5. **n+ and p+ Source/Drain Implantation:**
   - Use separate masks to define nMOS (in p-substrate) and pMOS (in n-well) source/drain regions.
   - Perform ion implantation for n+ and p+ doping.
   - This will also form n+ polysilicon gate and p+ polysilicon gate for NMOS and PMOS transistors respectively. Hence this process is called as self aligned process.



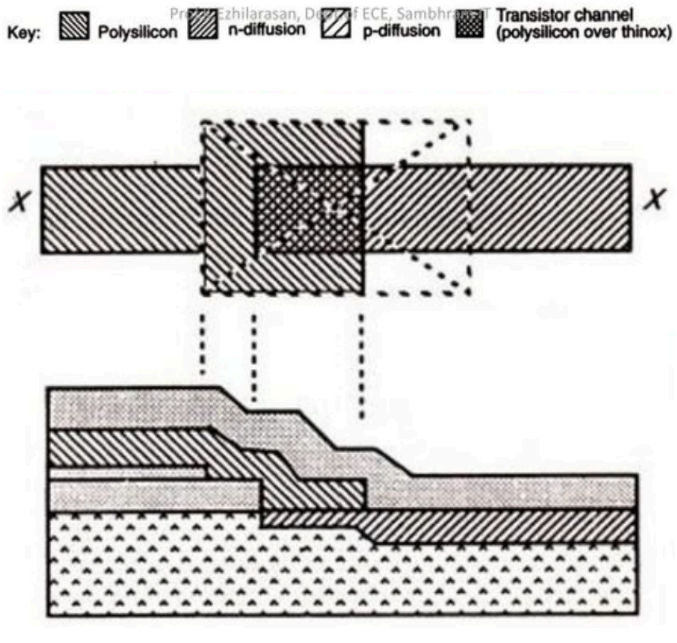
n-well process steps

6. **Contact Formation:**
   - Etch contact holes through oxide.
   - Deposit metal (usually aluminum) and pattern to form interconnects.
7. **Final Passivation:**
   - Deposit passivation oxide for protection.
   - Open pads for bonding as needed.

Q5) Draw the cross-section of buried contact. What are the advantages of lamda based design rules?

Advantages of Lambda-Based Design Rules:

1. **Scalability Across Technologies:**
   - Lambda rules scale easily by redefining λ for each technology node.
2. **Simplicity and Ease of Learning:**
   - Ideal for educational and academic projects where uniform rules help learning.
3. **Technology Independence:**
   - Removes process-specific dimensions; enables cross-process layout reuse.



Buried contact

4. **Compact and Conservative:**
   - While conservative, they ensure high manufacturing yield with fewer design violations.
5. **Quick Prototyping:**
   - Useful in early-stage design and teaching for rapid layout generation without in-depth process calibration.

> "Lambda-based rules round dimensions to multiples of λ for simplicity and layout portability, making them highly effective for teaching and prototyping"

Q6) With neat diagram explain the lamda-based design rules for contact cuts and vias

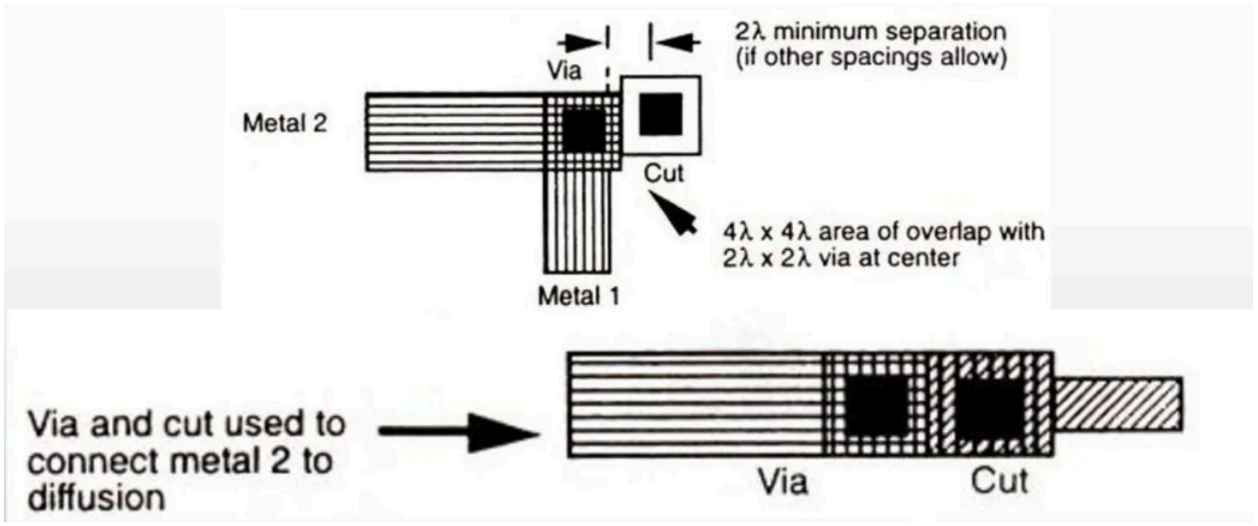
Lambda-Based Rules for Contacts:

Feature	Lambda Rule
Contact Size	2λ × 2λ
Contact Surround by Poly/Active	1λ overlap on all sides
Contact to Gate Spacing	2λ
Contact spacing	2λ between adjacents

Lambda-Based Rules for Vias:

Feature	Lambda Rule
Via Size	2λ × 2λ
Via Spacing	3λ between adjacent vias
Overlap by Metal Layer	1λ minimum
Use of Via Arrays	Recommended for high reliability

> Larger connections are built using arrays of 2λ × 2λ vias to improve yield and prevent current crowding.



Q7) List the colour, stick encoding, mask layout encoding, layers for a simple metal nMOS process

Layer	Mask Layout Encoding
Thinox	
Polysilicon	
Metal1	
Contact cut	
Overglass	
Implant	
Buried contact	

Layer	Mask Layout Encoding
P-Diffusion	
P+ Mask	
Metl2	
VIA	
P-Well	

Color and Stick Encoding (Stick Diagram Convention):

Layer	Stick Color	Stick Type / Pattern
Polysilicon	Red	Solid line (vertical lines for gates)
n-diffusion	Green	Solid horizontal lines
p-diffusion	Yellow	Solid horizontal lines
Metal1	Blue	Solid lines (horizontal or vertical)
Contact (to metal)	Black square	Box over junction
Vias	Black square	Between metal layers

Mask Layout Encoding (Layer Names and Purpose):

Layer Name	Purpose	Common Alias
Active	Defines diffusion regions	OD, Diff, RX
Poly	Forms transistor gate	PO, PC
Metal1	First metal interconnect layer	M1
Contact	Connects metal to poly or diffusion	CA, CONT
n-select	Defines nMOS regions	n-imp, nplus
p-select	Defines pMOS regions (not used in nMOS-only)	p-imp, pplus
n-well	Used in p-well or CMOS processes	NWELL

Q8) Explain the operation of cMOS dynamic logic. Also discuss the cascading problem of dynamic cMOS logic

Operation of CMOS Dynamic Logic:

Dynamic CMOS logic uses a clock to control logic evaluation through two phases:

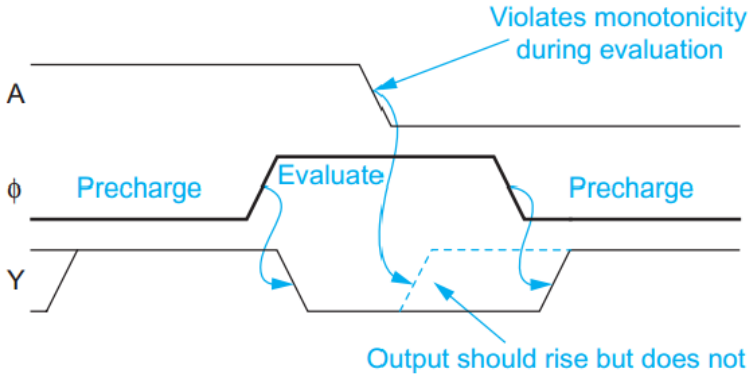
1. **Precharge Phase (Clock = LOW):**
   - A **pMOS precharge transistor** is ON, charging the output node to HIGH.
   - The **evaluation nMOS network** is OFF, so output remains undisturbed.
2. **Evaluation Phase (Clock = HIGH):**
   - The **pMOS precharge transistor** turns OFF.
   - The **nMOS evaluation network** turns ON.
   - Depending on the input combination, the output either discharges to LOW or remains HIGH.
   - No static power consumption; only dynamic power is used during transitions.

> Dynamic gates are fast and area-efficient but sensitive to noise and require careful clocking.

Cascading Problem in Dynamic CMOS Logic:

The **monotonicity problem** occurs when chaining multiple dynamic gates:

- Dynamic gates **assume inputs rise monotonically** during evaluation.
- However, a dynamic gate's output **falls during evaluation**, which **violates this assumption** for the next stage.



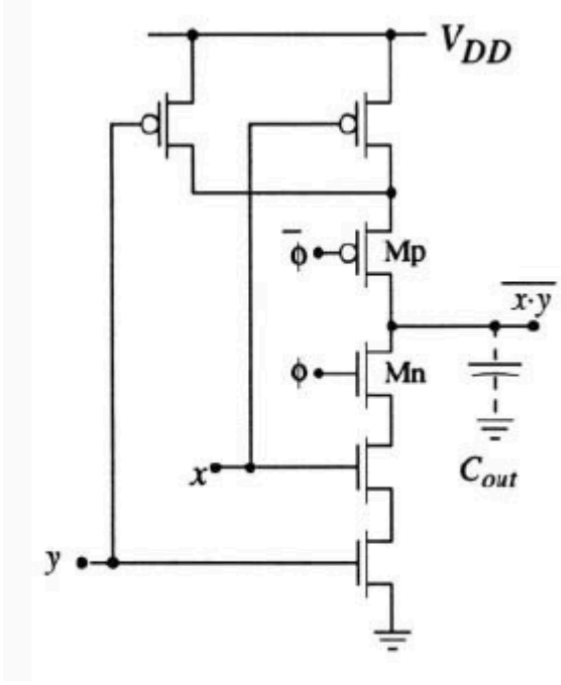
Optional - Monotonicity problem

Q9) Realize a 2-input NAND gate for a clocked cMOS logic and also for cMOS domino logic

Clocked CMOS Logic (C^2MOS) NAND Gate

Implementation Overview:

- A **2-input NAND gate** can be built using two cascaded **clocked CMOS inverters**.
- Each inverter is gated by the clock:
  - **PMOS gated by φ̄ (clock low)** for precharge
  - **NMOS gated by φ (clock high)** for evaluation
- The logic evaluation occurs only during the **clock high (φ = 1)** phase.



Clocked CMOS Logic (C²MOS) NAND Gate

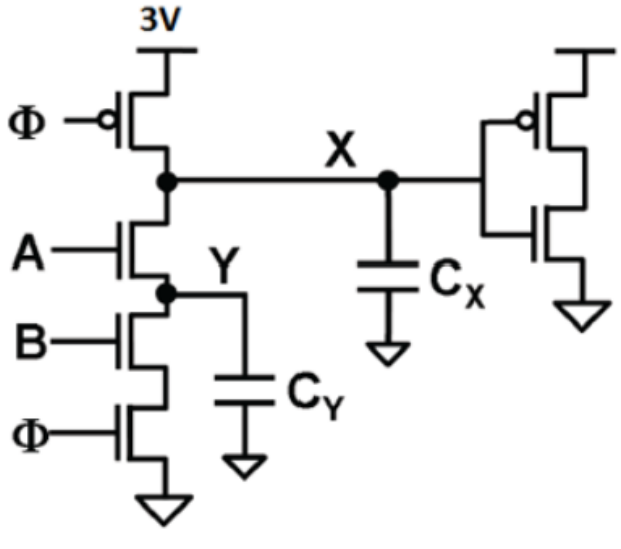
Key Idea:

Use two stages of clock-controlled inverters where the input NMOS logic network forms the NAND function, and the result is passed through the gated inverters.

CMOS Domino Logic NAND Gate

Implementation Steps:

1. **Precharge Phase (φ = 0):**
   - The output node is precharged high by a **PMOS transistor**.
2. **Evaluation Phase (φ = 1):**
   - A 2-input NAND pull-down path is made using **two NMOS transistors in series**.
   - If **A = B = 1**, the output node is pulled low.



2-input domino cMOS NAND logic

3. **Inverter Output:**
   - The dynamic low output is inverted by a static inverter, producing the correct **NAND output** (i.e., high when A and/or B is low).

Important Notes:

- Domino logic gates cannot produce **inverting logic directly**—you must use the inverter.
- Timing is critical; only **monotonically rising logic** is allowed between stages.

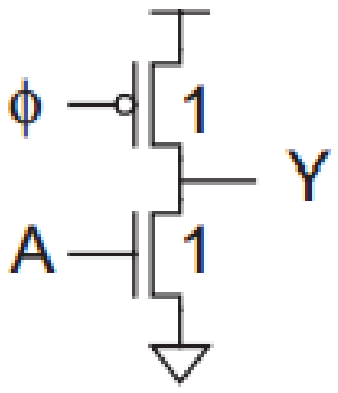
Q10) Explain the working principle of dynamic cMOS logic and clocked cMOS logic

Dynamic CMOS Logic

Working Principle:

Dynamic CMOS logic operates in two phases controlled by a clock signal: **precharge** and **evaluation**.

- **Precharge Phase ($\phi = 0$):**
  - A **PMOS transistor** (called the precharge transistor) is turned ON.
  - The output node is precharged to a high voltage (logic ‘1’).
  - The NMOS evaluation network is OFF, so no discharge occurs.



Dynamic cMOS

- **Evaluation Phase ($\phi = 1$):**
  - The precharge transistor is OFF.
  - The **NMOS pull-down network** is now active.
  - If the NMOS path conducts, it pulls the output to ground (logic ‘0’).
  - If the NMOS path does not conduct (i.e., at least one input is ‘0’), the precharged output remains at logic ‘1’.

Key Notes:

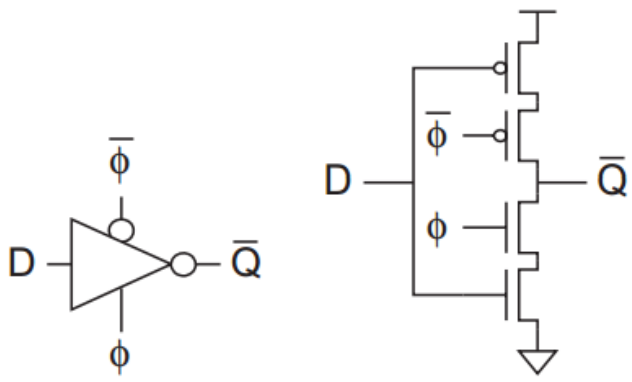
- Only **one type of logic (NMOS or PMOS)** is used in the evaluation path.
- No static power dissipation (only during switching).
- Faster than static CMOS but susceptible to charge leakage and noise.

Clocked CMOS Logic

Clocked CMOS logic (e.g., **Domino logic**) is a special case of dynamic CMOS with some enhancements:

Working Principle:

- **Similar two-phase operation** (precharge and evaluation), but with **buffering** to ensure only non-inverting logic is used.
- **Precharge Phase:**
  - PMOS is ON → output node charges to HIGH.
  - NMOS evaluation transistor is OFF → prevents output from being discharged.



Clocked CMOS

- **Evaluation Phase:**
  - NMOS evaluation transistor is ON.
  - Depending on the inputs, the output node may discharge → logic 0.
  - PMOS is OFF, preventing contention.

Advantages:

- Provides **non-overlapping, glitch-free pipelining**.
- Ensures **monotonic logic transitions**.
- Better suited for **synchronous systems**.

Q11) Explain Domino cMOS logic with neat circuit

Domino CMOS logic is a **dynamic logic family** that combines:

- A **dynamic logic gate** (using nMOS pull-down network and clocked precharge pMOS)
- Followed by a **static CMOS inverter**

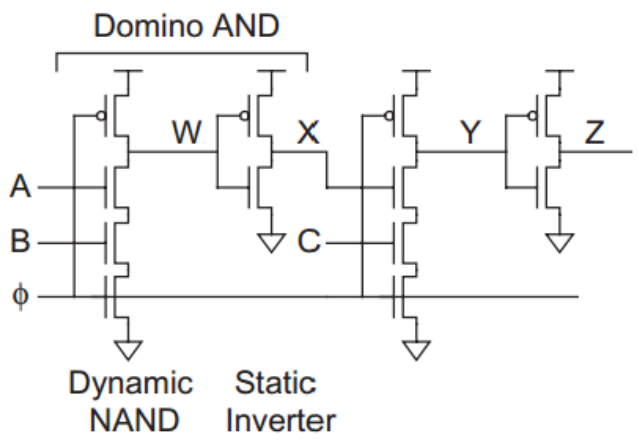
This configuration resolves the **monotonicity problem** found in dynamic logic. During operation:

- **Precharge phase (φ = 0):** The output node is charged high.
- **Evaluate phase (φ = 1):** The output may be pulled low depending on input conditions.
- The **static inverter** converts this falling output into a **rising output**, making it suitable to drive subsequent domino stages.

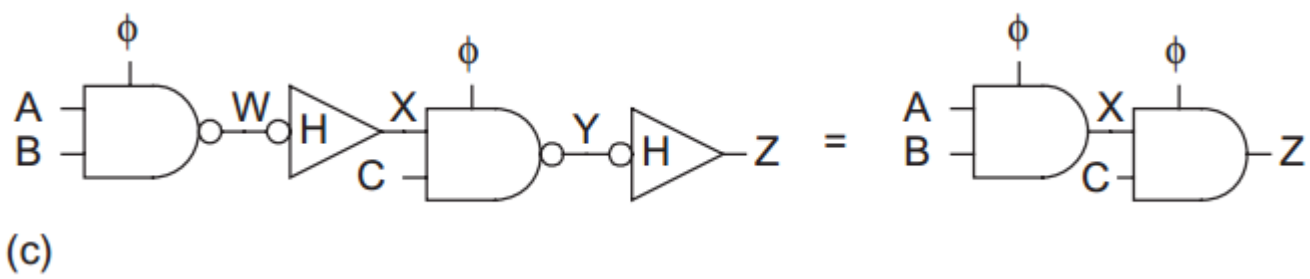
The gates "fall like dominos" in sequence as evaluation progresses.

Key Characteristics:

- **Noninverting logic only:** Domino gates produce only positive logic outputs.
- **Monotonically rising outputs:** Safe for chaining multiple stages.
- **Faster than static CMOS** in critical paths due to use of nMOS-only logic for evaluation.
- **Requires clock signal** for precharge and evaluation phases.



Basic structure of Domino gate



Domino gates symbols AND and NAND

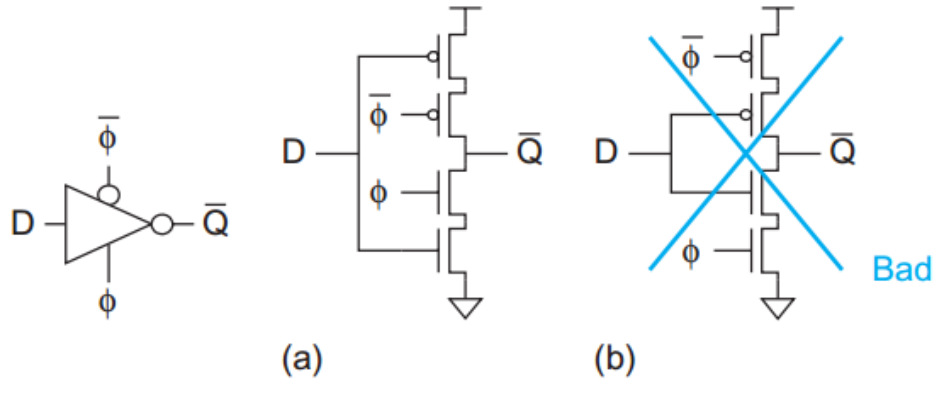
Q12) What is clocked cMOS gate? Where is it preferred?

A **clocked CMOS gate**, often referred to as **C²MOS**, is a type of **dynamic logic gate** that uses **clock-controlled transistors** (typically transmission gates or tristate inverters) to control the timing of signal evaluation and storage.

- In a C²MOS latch, the **pull-up or pull-down paths are gated by the clock**.
- The output switches only when the clock is in a specific state.
- C²MOS improves energy efficiency by eliminating always-on transistors, thereby reducing **static power consumption**.

Typical structure:

It consists of two inverting stages where either the nMOS or pMOS transistor is gated by the clock signal to control when evaluation happens.



Clocked CMOS

Where is C²MOS Preferred?

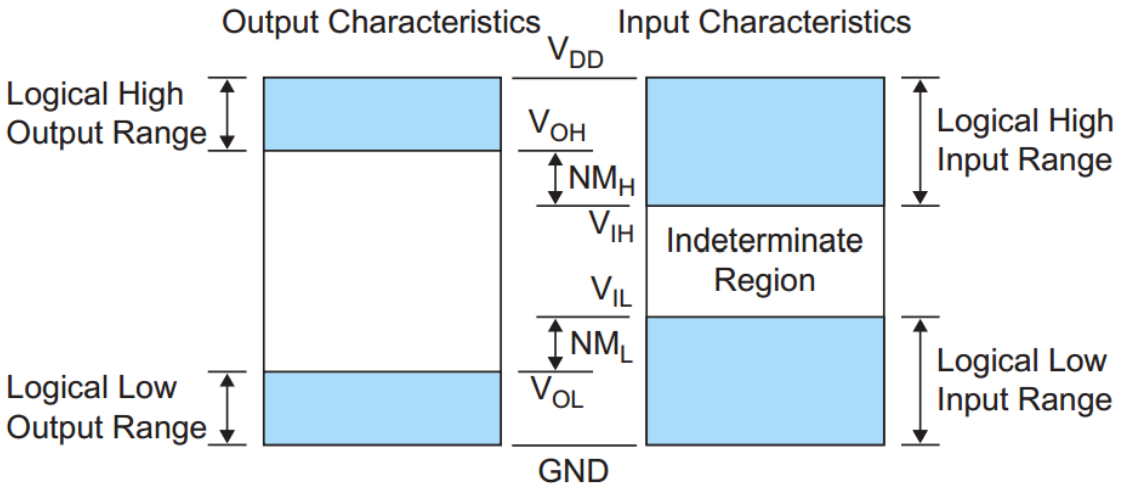
1. **Sequential Circuits:**
   - Used in **dynamic latches and flip-flops** such as the **C²MOS latch** and **C²MOS-based flip-flop**.
2. **Performance-Critical Paths:**
   - It offers **low latency** by enabling signal propagation through a single conducting path.
3. **Low-Power Applications:**
   - Because it avoids static current flow, it's ideal for **low-power digital designs**.
4. **Clock-Driven Designs:**
   - Where clock signals are used to control the timing of logic gate evaluation for **pipeline stages**, **register files**, and **memory elements**.

Q13) Explain noise margin with relevant equations

Noise Margin is a critical parameter that quantifies the **tolerance to noise**—i.e., the unwanted voltage variations that can cause logic level errors. It defines how much noise a logic gate can tolerate without misinterpreting a logic '0' or '1'.

In CMOS logic, we define:

- V_{OH}: Minimum output voltage for logic HIGH
- V_{OL}: Maximum output voltage for logic LOW
- V_{IH}: Minimum input voltage recognized as logic HIGH
- V_{IL}: Maximum input voltage recognized as logic LOW



Noise margin definitions

Noise Margins

There are **two types** of noise margins:

(i) Noise Margin High (NM_H)

Tells how much noise the HIGH level can tolerate before being misread as LOW.

$$\boxed{NM_H = V_{OH} - V_{IH}}$$

(ii) Noise Margin Low (NM_L)

Tells how much noise the LOW level can tolerate before being misread as HIGH.

$$\boxed{NM_L = V_{IL} - V_{OL}}$$

Ideal CMOS Case

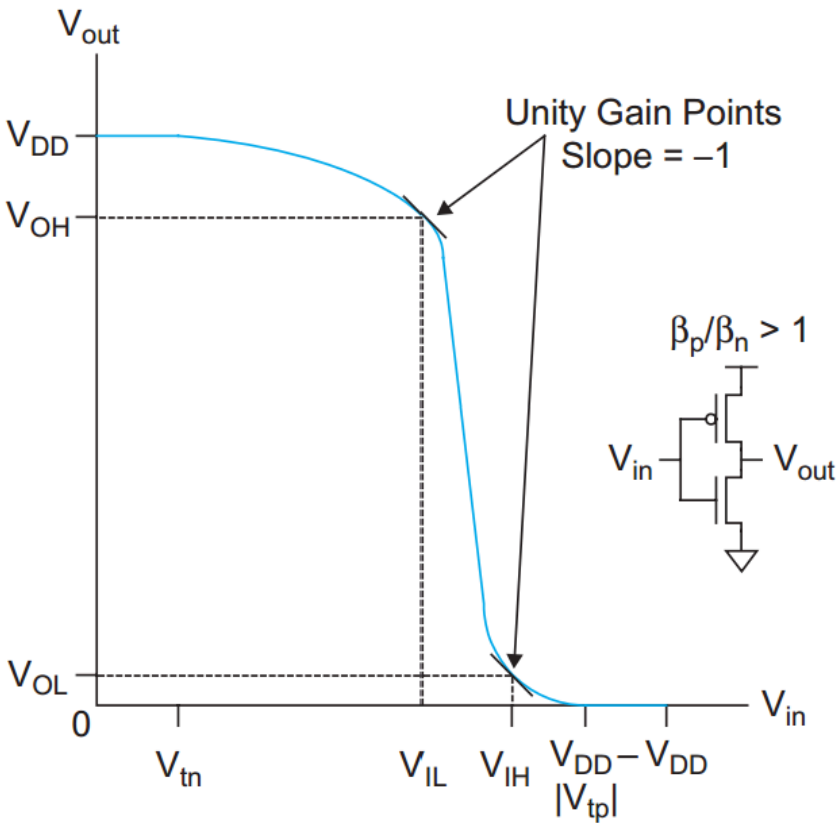
In ideal CMOS circuits:

- $V_{OH} = V_{DD}$
- $V_{OL} = 0$
- V_{IH} and V_{IL} are derived from the **VTC (Voltage Transfer Characteristic)** of the inverter

Typically, CMOS is designed so that:

$NM_H \approx NM_L$

This ensures symmetric noise tolerance.



CMOS inverter noise margin (DIA)

Q14) Explain Latch-up in CMOS

Latch-up is a **parasitic phenomenon** in CMOS circuits where a low-impedance path forms between the power supply (V_{DD}) and ground (GND), causing excessive current flow and potentially destroying the chip.

Cause:

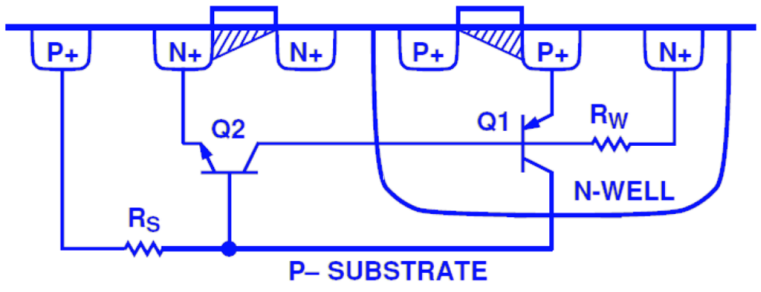
In CMOS technology, both **NMOS and PMOS transistors** are fabricated on a single silicon substrate, leading to the formation of two **parasitic bipolar transistors**:

- A **pnp** transistor formed by the p-substrate, n-well, and p+ diffusion.
- An **npn** transistor formed by the n-well, p-substrate, and n+ diffusion.

These transistors form a **Silicon Controlled Rectifier (SCR)** structure. If triggered (e.g., by a voltage spike or ionizing radiation), the SCR enters a conducting state, creating a **feedback loop** that keeps both transistors on, shorting VDD to GND.

Effects:

- High current flow
- Potential thermal damage
- Malfunction or destruction of the IC



Latch-up CMOS

Prevention Techniques:

- **Guard rings**: Place p+ and n+ diffusions around transistors to sink injected carriers.
- **Well and substrate contacts**: Reduce resistance to quickly remove excess charge.
- **Latch-up resistant CMOS processes**: Use insulating substrates like SOI (Silicon on Insulator).
- **Design rules adherence**: Ensure proper spacing and isolation.

Q15*) Transmission gate DC characteristics

A **Transmission Gate** is a bidirectional analog switch using complementary MOSFETs (nMOS + pMOS) connected in parallel. The gate enables efficient transmission of logic levels (0 to V_{DD}) without significant loss.

DC Characteristics:

Condition	Behavior
ON State	Both nMOS and pMOS ON; acts as a low-resistance path. Passes full V_{in} without threshold voltage drop.
OFF State	Both OFF; open circuit; no path between input and output.
Resistance	Varies withV_{in}, V_out, and device sizes. Lower than single-transistor pass gates due to parallel path.
VTC Behavior	Output voltage follows input almost exactly when ON; no V_t loss due to complementary action.
Leakage	Minimal leakage current in OFF state, but depends on technology node.

Key Observations:

- nMOS passes strong '0' but weak '1'.
- pMOS passes strong '1' but weak '0'.
- Together, a transmission gate **passes both 0 and 1 strongly**.
- This is why it's **preferred** over single nMOS/pMOS pass transistors.

Important Equations:

- Combined ON resistance: $R_{on,total} = \left(\frac{1}{R_{on,nMOS}} + \frac{1}{R_{on,pMOS}} \right)^{-1}$
- Voltage transfer is nearly linear when ON.

********** EOF **********