Lecture 3

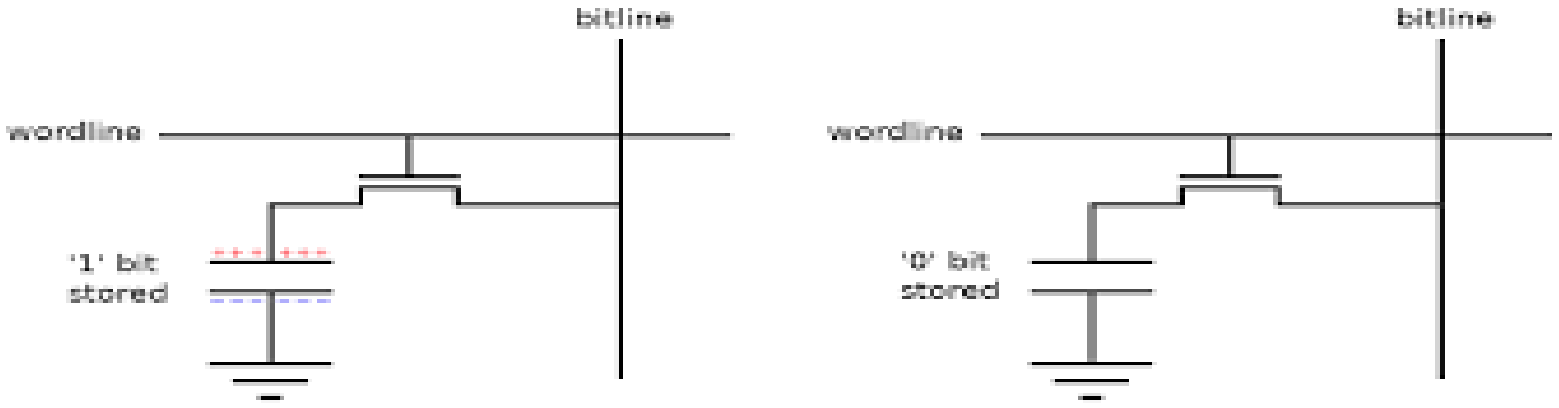
- **Dynamic RAM (DRAM)**
- **Memory Refreshment**

Introduction

- Because of its ability to provide high storage capacity at low cost, dynamic RAM (DRAM) dominates the high-capacity memory applications, including the primary RAM in computers.
- Further, as the name “dynamic” implies, the storage of information is inherently only temporary.
- This need for refresh is the primary logical difference in the behavior of DRAM compared to SRAM.
- We explore this logical difference by examining the dynamic RAM cell, the logic required to perform the refresh operation, and the impact of the need for refresh on memory system operation.

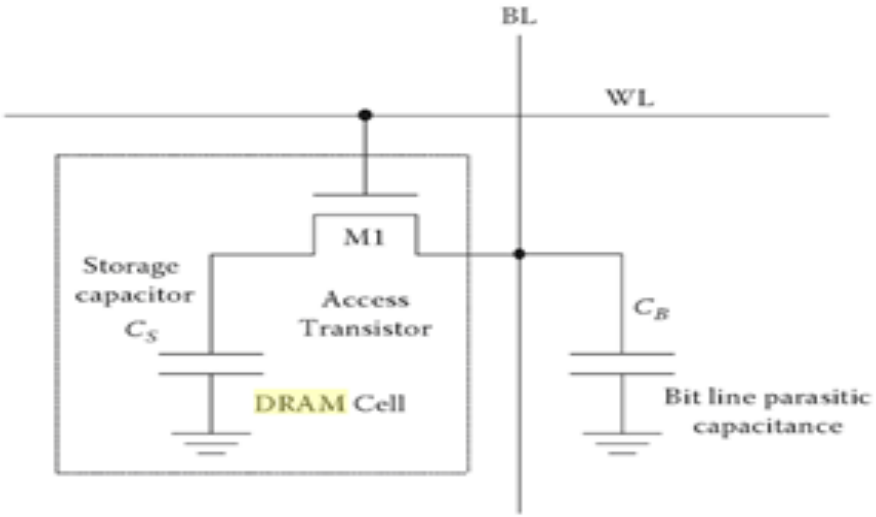
DRAM Cell

- The dynamic RAM cell circuit is shown in Figure.
- It consists of a capacitor C and a transistor T.
- If sufficient charge is stored on the capacitor, it can be viewed as storing a logical 1, else a logical 0.
- The transistor acts much like a switch.



Cont.,

- When the switch is “open,” the charge on the capacitor roughly remains fixed—in other words, is stored.
- But when the switch is “closed,” charge can flow into and out of the capacitor from the external Bit (B) line.
- This charge flow allows the cell to be written with a 1 or 0 and to be read.



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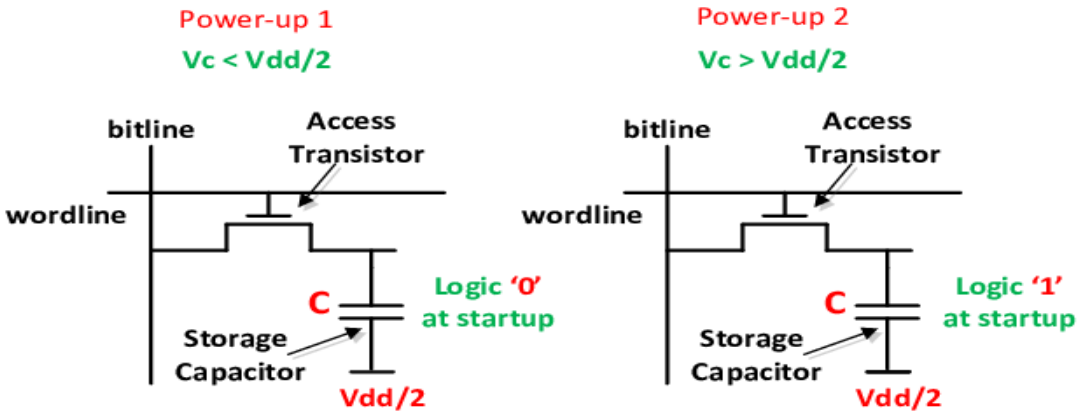
- To reduce the time and power associated with moving charges from storage capacitor (Cs) to Bit-line capacitor (CBL), the CBL is charged to VDD/2.
- If Vc> VDD/2 □ Logic 1 was stored ,and vice versa.
- Sense amplifier

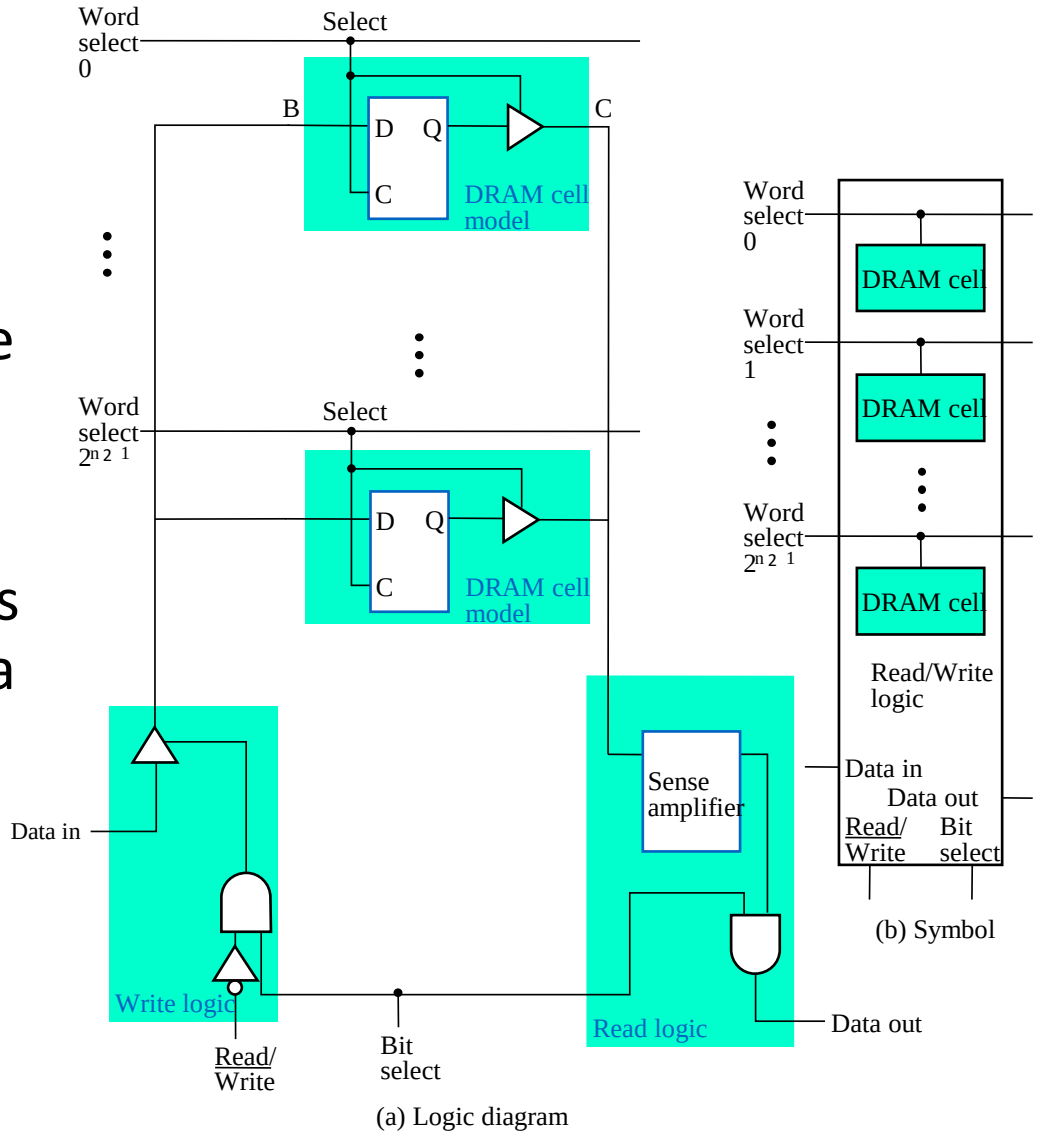


Destructive & Non Destructive Memory Readout

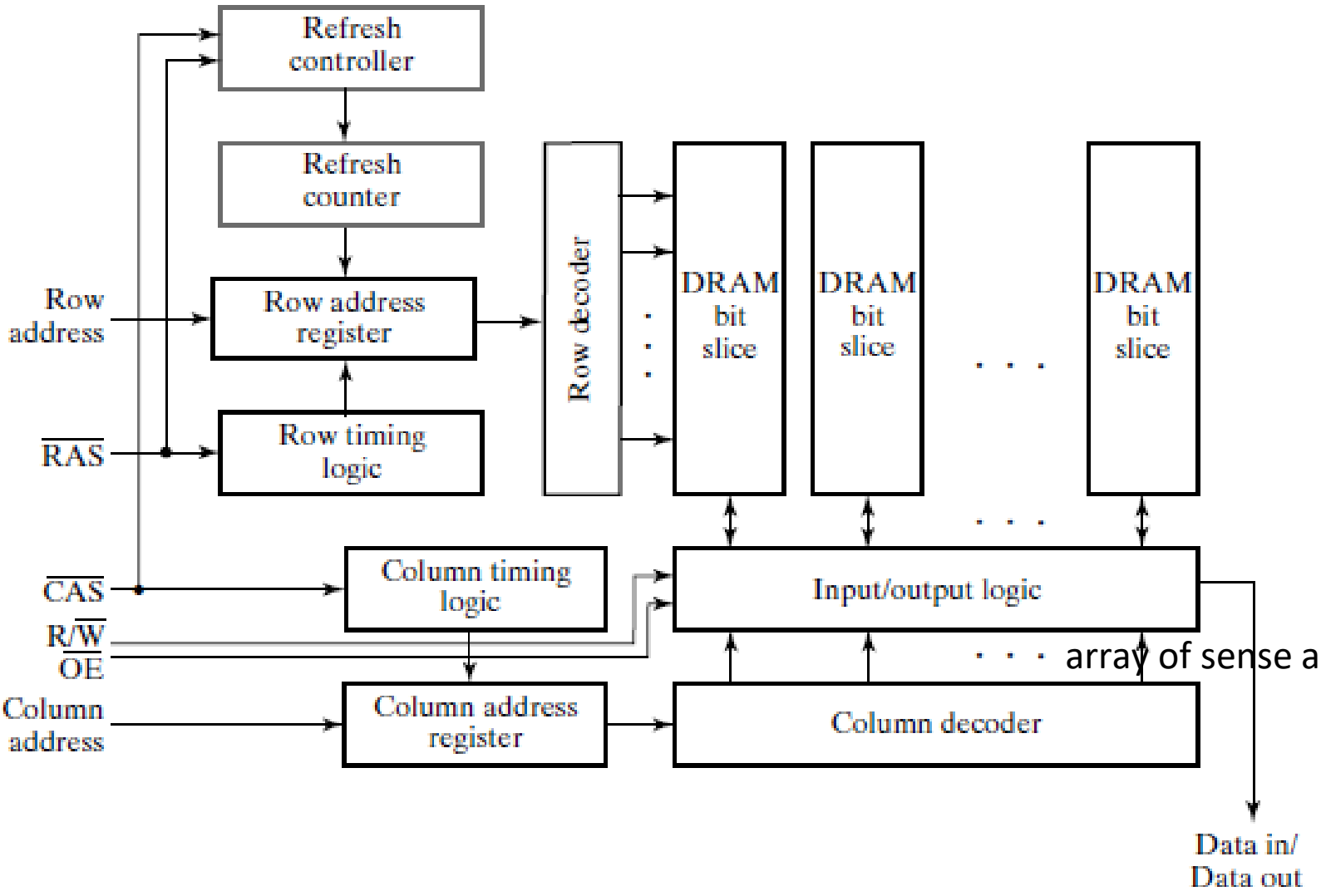
- A read operation that alters the contents of the accessed memory location and must be immediately followed by a rewriting of the contents in order to preserve them.
- If the data in a memory is not destroyed in the reading process, the system has nondestructive readout.
- A flip-flop is an example of nondestructive readout.
- Sensing the output voltage (reading) from a given side of a flip-flop generally does not change the state of the flip-flop and the stored data is retained.

Dynamic RAM - Bit Slice Model

- C is driven by Tri-state drivers
- Sense amplifier is used to measure the minute change in voltage on the Bit-line.
- Rewrite after Reading.
- Array of sense amplifiers acts as a temporary data storage (Row Buffer).



Block Diagram of a DRAM



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How to handle addressing in DRAMs

- To reduce the number of pins, the DRAM address is split to roughly halve the large number of address pins on the typical RAM IC.
- The row address first is used to select the row of cells to be read within the memory.
- The column address secondly is used to select the word to be placed on the output from the data read from the row of cells.

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- This can be done since the row address, which performs the row selection, is actually needed before the column address, which reads out the data from the row selected.
- In order to hold the row address throughout the read or write cycle, it is stored in a register.
- The column address is also stored in a register.

Control signals

- The load signal for the row address register is (Row Address Strobe RAS^{-}), and for the column addresses is (Column address strobe CAS^{-}).
- R/ $W^{-}$and Output enable (OE^{-}).
- Note that this design uses signals active at the LOW (0) level.

Handle Row Address

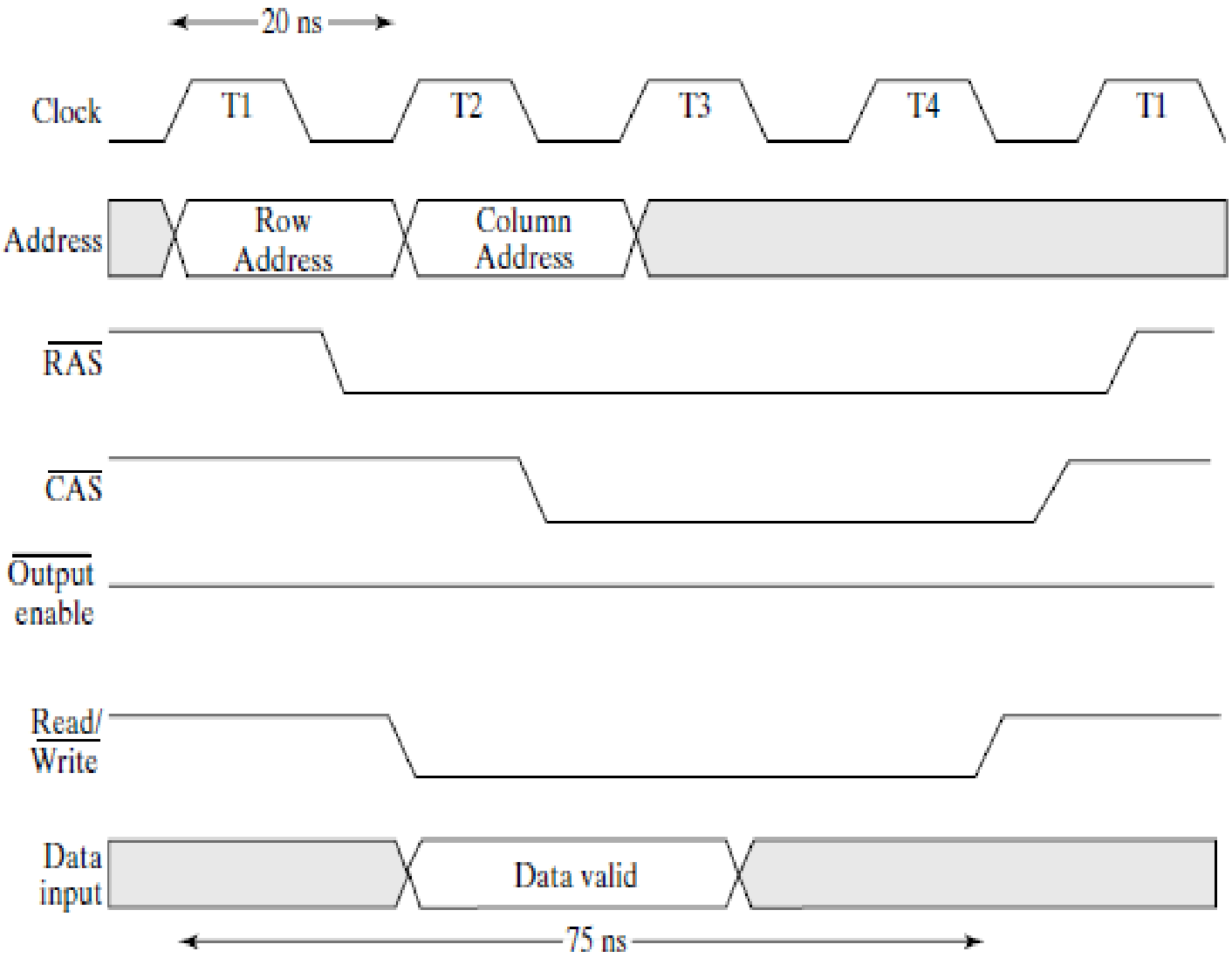
- The row address is applied to the address inputs.
- RAS changes from 1 to 0,
- loading the row address into the row address register.
- This address is applied to the row address decoder and selects a row of DRAM cells.

Handle Column Address

- The column address is applied,
- Then CAS changes from 1 to 0, loading the column address into the column address register.
- This address is applied to the column address decoder, which selects a set of columns of the RAM array of size equal to the number of RAM data bits.

For Write Operation

- The input data with R/ $\overline{W}$ = 0 is applied over a time interval similar to that for the column address.
- The data bits are applied to the set of bit lines selected by the column address decoder, which in turn apply the values to the DRAM cells in the selected row, writing the new data into the cells.
- When CAS and RAS return to 1, the write cycle is complete and the DRAM cells store newly written data.
- Note that the stored data in all of the other cells in the addressed row has been restored.

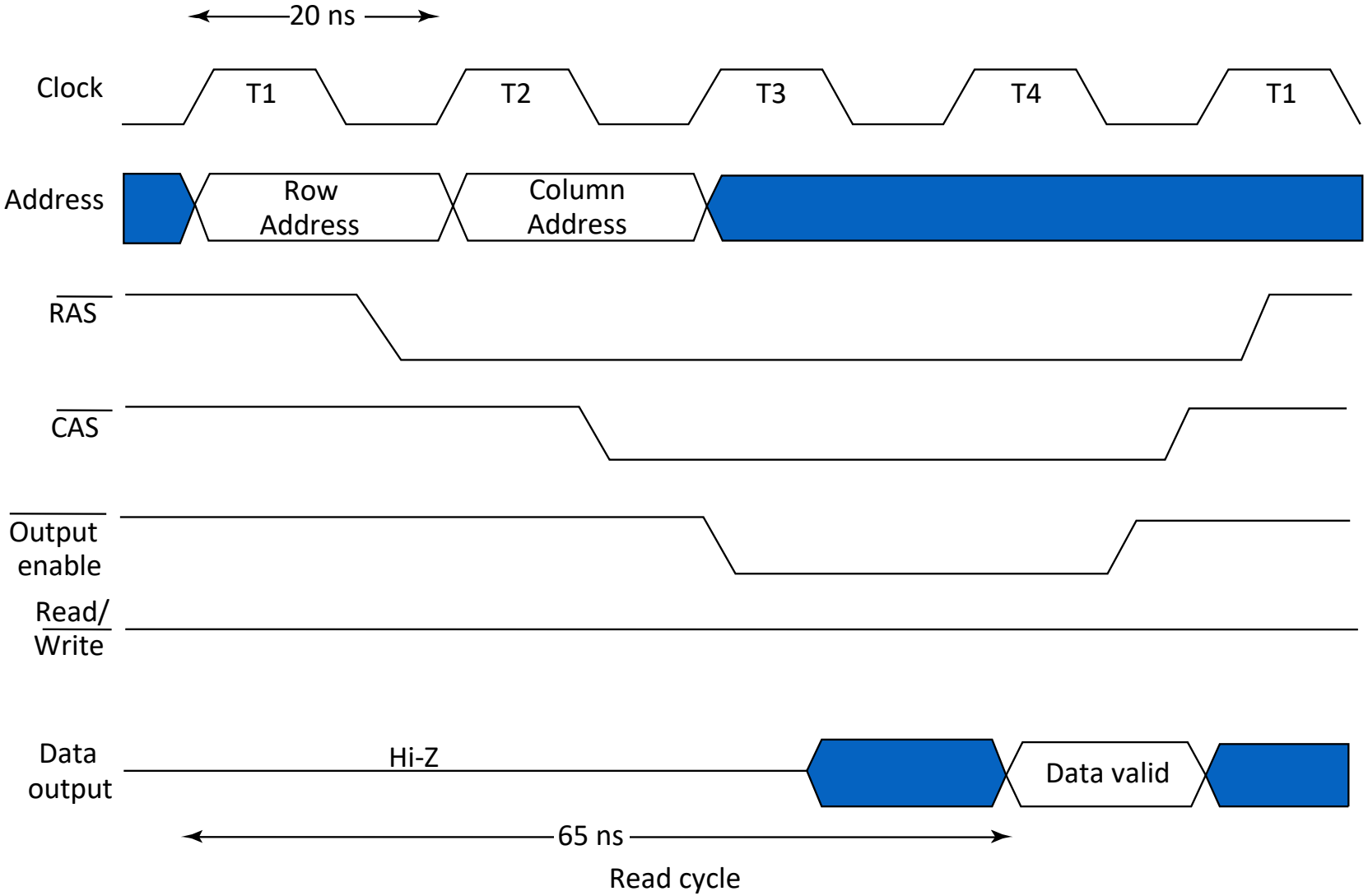


(a) Write cycle

For READ Operation

- The input data with R/ $\overline{W}$ = ‘1’ is applied over a time interval similar to that for the column address.
- Data values in the DRAM cells in the selected row are applied to the bit lines and sensed by the sense amplifiers.
- The column address selects the values to be sent to the data output, which is enable by the OE.
- During the READ operation, all values in the addressed row are restored.

Dynamic RAM Read Timing



Memory Refresh

- Is the process of periodically reading information from an area of computer memory and immediately rewriting it to the same area without modification.
- Each memory refresh cycle refreshes a succeeding area of memory cells, and repeatedly refreshing all the cells in a consecutive cycles.
- The refreshment process is conducted automatically.

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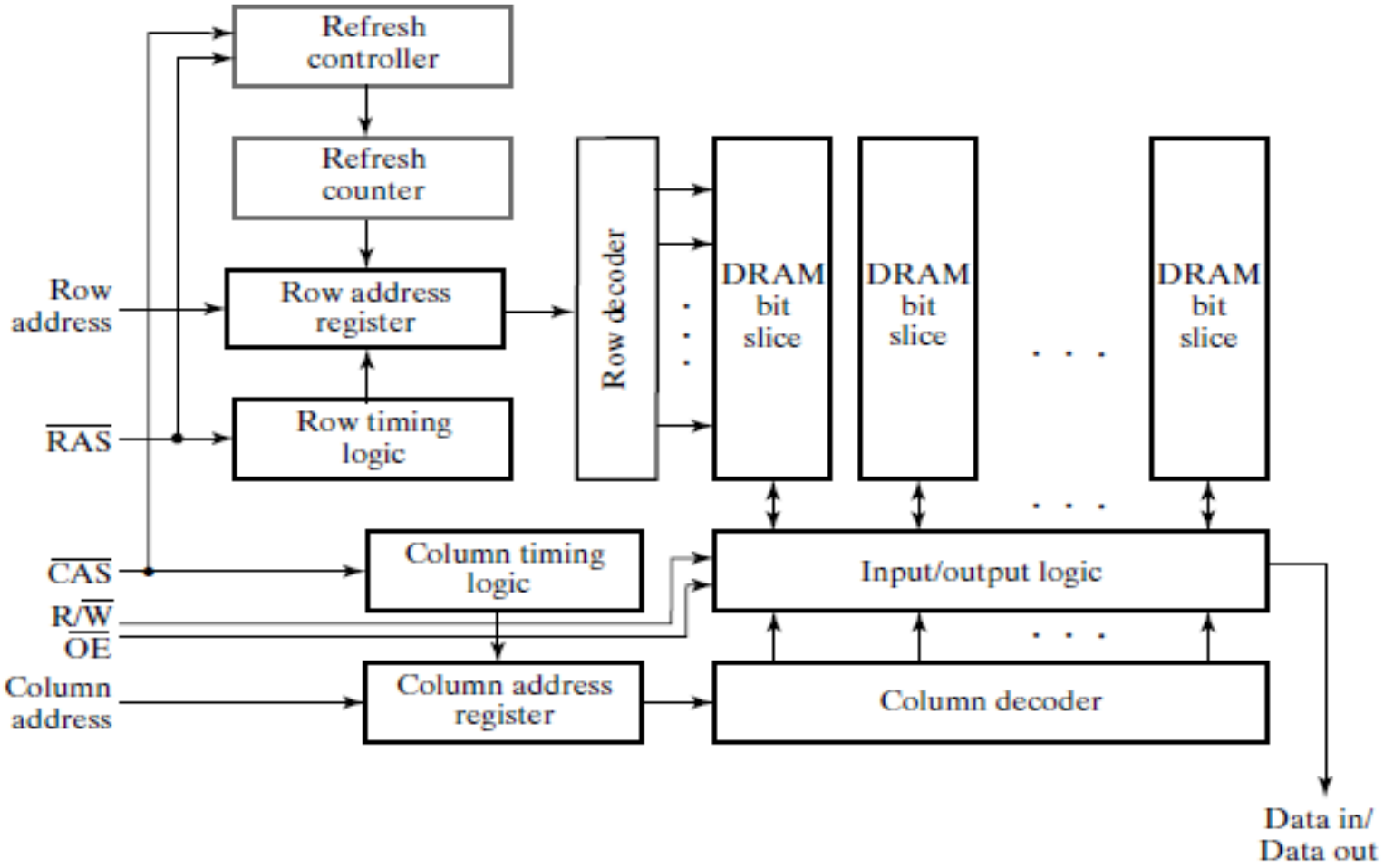
- While a refresh cycle is occurring, the memory is not available for normal READ & WRITE operations.
- In modern memories, this overhead time is not large enough.
- **Conclusion**: each memory cell must be refreshed repetitively within a maximum interval between refreshes specified by the manufacture.

Block Diagram of a DRAM Including Refresh Logic



How Refresh Works?

1- Refresh cycles are generated by refresh counter(either a refresh counter; as a part of the memory **or** external counter as a part of DRAM controller), which contains the address of the row to be refreshed.

2- The row address is applied to the row address lines.

3- The refresh cycle can be triggered by one of the following ways: **RAS-only refresh, CAS-before-RAS refresh, or Hidden refresh.**

The standard triggering ways

- **RAS-only refresh**. A row address is placed on the address lines and RAS is changed to 0. In this case, the refresh addresses must be applied from outside the DRAM chip, typically by an IC called a DRAM controller.

- **CAS-before-RAS refresh**. The CAS is changed from 1 to 0 followed by a change from 1 to 0 on RAS.
- It appears as an illegal operation. In this case, the incoming external row address will be discard , and the memory will use its internal refresh counter.
- Additional refresh cycles can be performed by changing RAS by the internal counter without changing CAS.

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- **Hidden refresh.** Following a normal read or write, CAS is left at 0 and RAS is cycled, effectively performing a CAS-before-RAS refresh. During a hidden refresh, the output data from the prior read remains valid. Thus, the refresh is hidden. Unfortunately, the time taken by the hidden refresh is significant, so a subsequent read or write operation is delayed.
- In all cases, note that the initiation of a refresh is controlled externally by using the RAS and CAS signals.

Refreshing Types

- Refreshes may be performed at evenly spaced points in the refresh time, an approach called **distributed refresh.**
- Alternatively, all refreshes may be performed one after the other, an approach called **burst refresh**

Example

- A 4M × 4 DRAM has a refresh time of 64 ms and the length of time to perform a single refresh per row is 60 ns?
- What is the refreshment time in case of distributed or burst refreshment.
- What is the time for Read & Write.
- **Solution:**

- no. of rows = 4096 rows to be refreshed.

A- Burst Refreshment:

- A total time out for refresh = 4096 x 60 ns = 0.25 ms

- The rest time for R/W = 64ms – 0.25 ms = 63.75 ms

The DRAM controller must initiate 4096 refreshes sequentially every 64 ms for burst refresh.

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B- Distributed Refreshment

- the refresh interval for distributed refresh = 64 ms/4096 = 15.6 microseconds (µs).
- Time R/W = 15.6 µs – 60 ns
- The DRAM controller must initiate a refresh every 15.6 µs for distributed refresh

Since use of burst refresh would halt computer operation for a fairly long period, distributed refresh is more commonly used.

Assignment

- The refresh cycle is similar to READ cycle, but executing faster, Why?

Sheet

- Text book