The AT89S52 is an 8-bit microcontroller based on the **Intel 8051** architecture & developed by Microchip Technology.It is widely used in embedded systems due to its simplicity, availability, and robust features. Here’s a comprehensive overview of the AT89S52 microcontroller:

**1. Features of AT89S52**

* **CPU**: 8-bit 8051-compatible CPU.
* **Clock Speed**: Supports up to **33 MHz**.
* **ROM (Program Memory)**:
  + **8 KB of In-System Programmable (ISP) Flash Memory**.
  + Can be reprogrammed multiple times.
* **RAM (Data Memory)**:
  + **256 bytes** of internal RAM.
  + Divided into:
    - General-purpose memory.
    - Special Function Registers (SFRs).
    - Bit-addressable area.
* **EEPROM**: None internally. External EEPROM can be interfaced.

**2. Pin Configuration**

The AT89S52 has **40 pins**, with functions divided as follows:

| **Pin Group** | **Pin Numbers** | **Description** |
| --- | --- | --- |
| **Port 0 (P0)** | 32–39 | 8-bit bi-directional I/O (open-drain). Used as lower address/data bus during external memory access. |
| **Port 1 (P1)** | 1–8 | 8-bit bi-directional I/O (internally pull-up). |
| **Port 2 (P2)** | 21–28 | 8-bit bi-directional I/O. Used as high-order address bus in external memory mode. |
| **Port 3 (P3)** | 10–17 | Multi-function I/O pins (e.g., serial, interrupts, control signals). |
| **RST** | 9 | Reset input (active HIGH). |
| **XTAL1, XTAL2** | 18, 19 | Connections for external crystal oscillator. |
| **PSEN** | 29 | Program Store Enable. Used for external program memory. |
| **ALE** | 30 | Address Latch Enable. Helps separate address and data buses. |
| **EA** | 31 | External Access Enable (LOW for external memory). |

**3. Special Features**

**Timers**

* **3 Timers**: Timer0, Timer1 (16-bit), and Timer2 (16-bit, auto-reload or capture mode).
* Used for:
  + Delay generation.
  + Event counting.
  + PWM generation (using Timer2).

**Interrupts**

* **6 interrupt sources**:
  1. External Interrupt 0 (INT0)
  2. Timer 0 Overflow
  3. External Interrupt 1 (INT1)
  4. Timer 1 Overflow
  5. Serial Port Interrupt
  6. Timer 2 Overflow (or Capture Mode)

**Serial Communication**

* **UART:** Full-duplex serial communication.
* Baud rate can be set using Timer1.

**I/O Pins**

* 32 general-purpose I/O pins.
* Supports bit-addressable operations.

**Power-Saving Modes**

* **Idle Mode**: CPU stops; peripherals continue.
* **Power-Down Mode**: All system clocks are stopped; minimal power consumption.

**4. Memory Organization**

**Internal Memory**

* **Program Memory (ROM)**: 8 KB Flash memory.
* **Data Memory (RAM)**:
  + 256 bytes total:
    - 128 bytes of General-purpose RAM (00H to 7FH).
    - 128 bytes for Special Function Registers (SFRs) (80H to FFH).

**External Memory**

* Supports **64 KB** of external program memory.
* Supports **64 KB** of external data memory.

**5. Registers in 8051**

### ****General-Purpose Registers:****

* The **8051 architecture** uses **32 general-purpose registers**, labeled **R0 to R7** for each of the **4 register banks** (a total of **128 bytes** of RAM for general-purpose use).
  + These 32 registers are used for data manipulation and are located in the **internal RAM**.
  + The active register bank is selected via the **RS1** and **RS0** bits in the **PSW** (Program Status Word) register.

**Special Function Registers (SFRs):**

* These are 8-bit registers, located in the address range 0x80 to 0xFF. Some are bit-addressable for bit-level manipulation.

| **Register** | **Address** | **Description** |
| --- | --- | --- |
| **Accumulator (A)** | 0xE0 | General-purpose register for arithmetic and logic operations. |
| **B Register (B)** | 0xF0 | Used during multiplication and division instructions. |
| **Program Status Word (PSW)** | 0xD0 | Contains flags like Carry, Auxiliary Carry, and Parity. |
| **Stack Pointer (SP)** | 0x81 | Points to the top of the stack (default = 0x07). |
| **Data Pointer (DPTR)** | 0x82/0x83 | 16-bit register for external memory addressing. Consists of DPL (low byte) and DPH (high byte). |
| **Port Registers (P0–P3)** | 0x80, 0x90, 0xA0, 0xB0 | Used for GPIO operations on Ports 0, 1, 2, and 3. |
| **Timer Control (TCON)** | 0x88 | Controls timers and external interrupts. |
| **Timer Mode (TMOD)** | 0x89 | Configures the timer modes (Timer 0 and Timer 1). |
| **Timer 0 Registers (TH0, TL0)** | 0x8C, 0x8A | High and low bytes for Timer 0. |
| **Timer 1 Registers (TH1, TL1)** | 0x8D, 0x8B | High and low bytes for Timer 1. |
| **Timer 2 Registers (TH2, TL2)** | 0xCD, 0xCC | High and low bytes for Timer 2. |
| **Timer 2 Control (T2CON)** | 0xC8 | Controls Timer 2 and its operation. |
| **Interrupt Enable (IE)** | 0xA8 | Enables or disables interrupts. |
| **Interrupt Priority (IP)** | 0xB8 | Sets interrupt priority levels. |
| **Serial Control (SCON)** | 0x98 | Configures the UART for serial communication. |
| **Serial Buffer (SBUF)** | 0x99 | Holds data for UART transmission and reception. |
| **Power Control (PCON)** | 0x87 | Controls power-saving modes (idle and power-down). |
| **Watchdog Timer (WDTRST, WDTCON)** | 0xA6, 0xA7 | Controls the watchdog timer functionality. |

**Bit-Addressable Registers:**

* Certain registers are bit-addressable, allowing bit-level manipulation. These include:

**PSW (Program Status Word) – 0xD0**

| **Bit** | **Name** | **Description** |
| --- | --- | --- |
| D0 | P (Parity) | Set if the accumulator has an odd number of 1s. |
| D1 | — | Reserved. |
| D2 | OV (Overflow) | Set during signed arithmetic overflow. |
| D3 | RS0 | Register bank select bit 0. |
| D4 | RS1 | Register bank select bit 1. |
| D5 | F0 (Flag 0) | User-defined general-purpose flag. |
| D6 | AC (Aux. Carry) | Set during BCD addition. |
| D7 | CY (Carry) | Set during addition, subtraction, or shift. |

**TCON (Timer Control) – 0x88**

| **Bit** | **Name** | **Description** |
| --- | --- | --- |
| TCON.0 | IT0 | External interrupt 0 edge type (0 = low, 1 = edge). |
| TCON.1 | IE0 | External interrupt 0 flag. |
| TCON.2 | IT1 | External interrupt 1 edge type. |
| TCON.3 | IE1 | External interrupt 1 flag. |
| TCON.4 | TR0 | Timer 0 run control (1 = start timer). |
| TCON.5 | TF0 | Timer 0 overflow flag. |
| TCON.6 | TR1 | Timer 1 run control. |
| TCON.7 | TF1 | Timer 1 overflow flag. |

**SCON (Serial Control) – 0x98**

| **Bit** | **Name** | **Description** |
| --- | --- | --- |
| SCON.0 | RI | Receive interrupt flag (set when a byte is received). |
| SCON.1 | TI | Transmit interrupt flag (set when a byte is sent). |
| SCON.2 | RB8 | Ninth bit received in 9-bit mode. |
| SCON.3 | TB8 | Ninth bit to transmit in 9-bit mode. |
| SCON.4 | REN | Enable serial reception. |
| SCON.5 | SM2 | Multiprocessor communication mode. |
| SCON.6 | SM1 | Serial mode bit 1. |
| SCON.7 | SM0 | Serial mode bit 0. |

**6. Electrical Characteristics**

* **Operating Voltage**: 4.0V to 5.5V.
* **Operating Frequency**: Up to 33 MHz.(Standard Clock Frequency:: 11.0592 MHz)
* **I/O Pin Current**:
  + Maximum 15 mA per pin.
  + Total 71 mA across all pins.

**7. Advantages**

* Simple architecture and easy to learn.
* Abundance of learning resources and tools.
* Wide community support.
* System Programming feature for convenient reprogramming.

**8.Limitations**

* No built-in ADC (Analog-to-Digital Converter).
* No internal EEPROM (requires external EEPROM for non-volatile storage).
* Only 256 bytes of internal RAM.

**9. Programming the AT89S52**

* **Keil uVision IDE** (8051 development).
* **IAR Embedded Workbench** (supporting 8051).
* **SDCC (Small Device C Compiler)** **+ Eclipse/Sublime Text**:Compiler for 8051.
* **Programmer**: Use an ISP programmer to upload code to flash memory.

### ****10. Some Systems and Hardware Programming Language****

* Typically programmed in **Assembly**.
* C
* C++
* Rust
* D
* Zig
* Ada
* VHDL
* Verilog
* Embedded C