Nintendo Entertainment System

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A bit of history

The NES came to the market during unsure times following the home video game crash of 1983. The initial release was limited to Japan until 1985 when the North American version was announced at CES. Media outlets doubted the success of the NES as the North American video game market was all but dead.

The NES proved itself by separating the brand from older low quality systems. Nintendo enforced strict standards for games released for the system and made use of lockout technology that existed both on the console and the game cartridges.

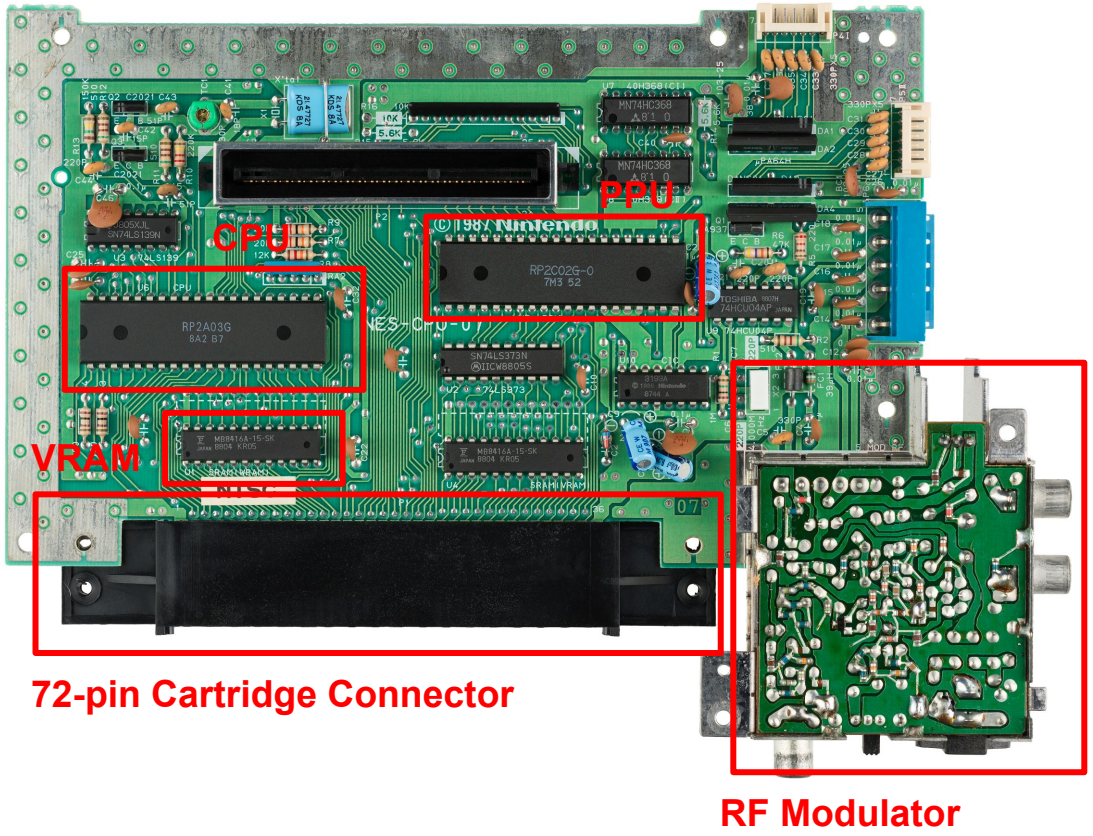
By 1989 the system had sold over 7 million copies and by 1990 the system had outsold all previously released consoles on the market.

The system wasn't officially retired in Japan until 2003 and has left a lasting legacy. In 2016 Nintendo released a palm sized ARM based NES remake preloaded with many popular classics in order to bring the system back to the home without having to maintain the old hardware.

Although decades old, the NES has a legacy that continues to today.

Overview of the system

- Custom 6502 CPU(2A03)
- Ricoh RP2C02 PPU
- Name-Table VRAM
- 72-pin Cart Connection
- Video output via RF modulator.

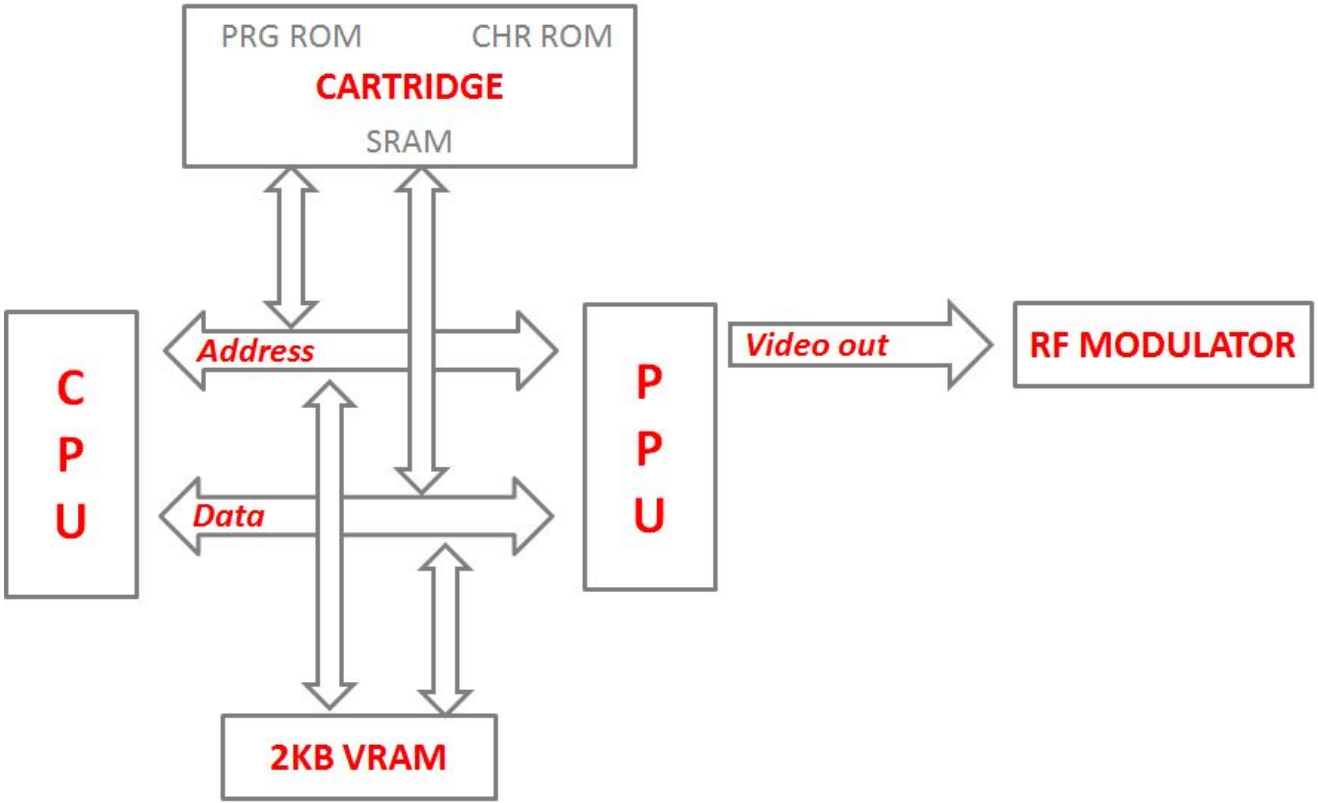


Overview of Cartridge

Technology within the Cartridges vary depending on requirements of the game. Larger games with save states like “The Legend of Zelda” would include a small battery for an additional SRAM cell.

Most games will include program ROM, which when connected to the system is mapped to the CPU, and a CHR ROM which is mapped to the PPU for mapping sprites and graphical elements of games.

NES Architecture



Description of CPU

The NES used a dated(at the time) 8 bit microcontroller from MOS Technology, referred to as the 6502. It was originally released in 1975 as an inexpensive full featured alternative to far more expensive processors.

The 6502 used a single 8 bit accumulator register and two 8 bit index registers. Along with an 8 bit stack pointer, 8 bit status register, and a 16 bit program counter.

This Processor supports several addressing modes, including implied, absolute, indexed absolute, indexed zero paged, relative, indirect(using x or y registers), and immediate. The 6502 also supported a fast zero page mode using a single byte address to reduce cycles needed to fetch the full address.

CPU continued

Two types of interrupts are used within the 6502, NMI edge sensitive interrupts and IRQ level sensitive interrupts. There exists a hardware edge detector and hardware level detector for each interrupt accordingly.

The output of each detector is polled during the final cycle of an instruction before the opcode fetch of the next instruction. These are used for I/O interaction for user input for the system.

The CPU has access to 2KB internal RAM and has the ability to address registers and memory space used by the PPU, APU, I/O, and Cartridge ROM and RAM.

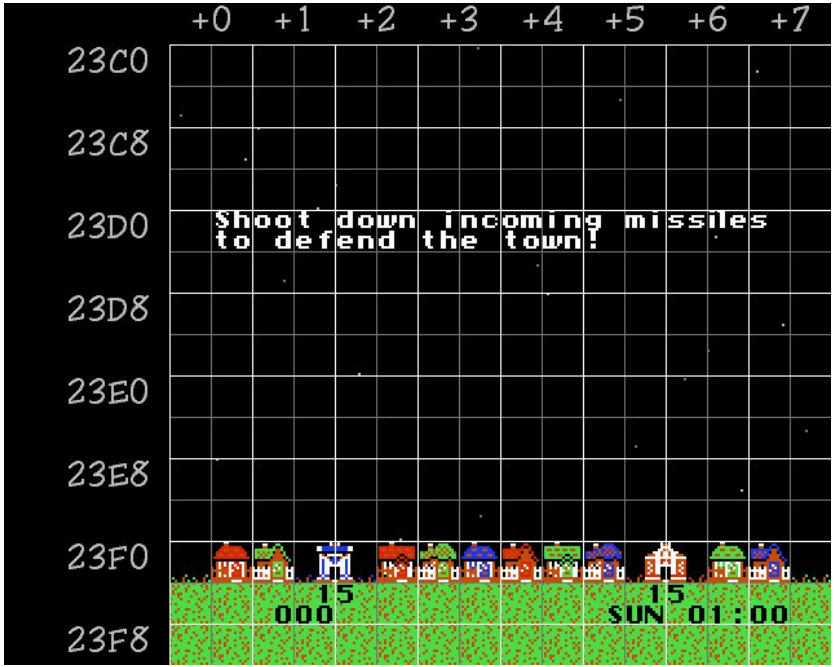
Operation of PPU

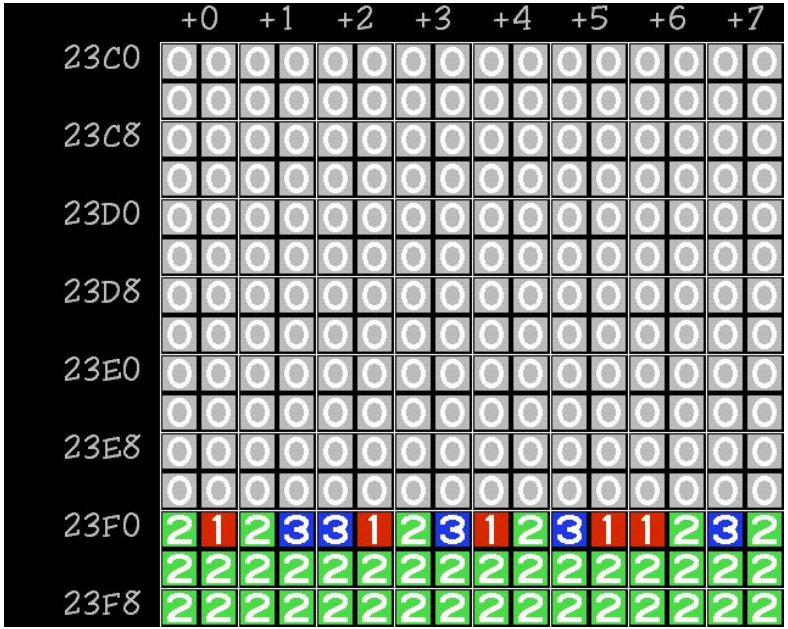
The PPU, or Picture Processing Unit, was a relatively advanced graphics unit, especially in comparison to the older 6502. The PPU had its own addressing space which had a total of 10 KB of memory. 8KB of this memory was mapped to the ROM of the game cartridge and the other 2KB was used to store mapping data, color palettes, and dynamic memory for keeping track of the position, color, and orientation of sprites being drawn to the screen.

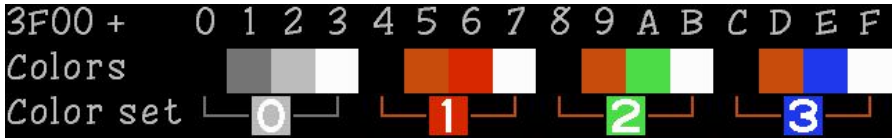
In order to draw the background, pattern tables stored in ROM would be mapped via name tables which keeps track of the pallets needed to make up the the background. Attribute tables at the end of each name table keeps track of where each pallet is displayed on the screen.

In order to draw sprites over the background, Object Attribute Memory from within the PPU keeps track of up to 64 sprites. Each sprite uses 4 bytes of memory to store x and y position, tile index, and rendering attributes.

PPU Continued







Audio control

The APU, or Audio Processing Unit, was implemented within the 6502(2A03). The APU used registers mapped to certain channels, each providing certain wave generators for sound effects. There was a total of five channels implemented, two pulse wave generators, a triangle wave generator, a noise generator, and a delta modulation channel for DPCM samples. Each channel is equipped with a variable rate timer and modulators driven by low-frequency clocks.

The APU also contains it’s own status register, allowing channels to be enabled and disabled.

Memory Mapping

The NES has limited system memory but has the ability to address various hardware registers and cartridge memory. This allows for direct access to hardware, in game programming, and the ability to expand based on the hardware contained within the cartridge.

Mirrors on the main memory exist due to cost saving measures for hardware address decoding. It is cheaper hardware wise to only check the lower bits of the address than to build hardware to check the higher bits first.

Mirrors for the PPU registers can be enabled for graphics wrapping or for drawing status bars over scrolling graphics. An example is the life and score bar used in “Super Mario Bros”.

Address Range	Size	Description
$0000-$07FF	$0800	2KB internal RAM
$0800-$0FFF	$0800	Mirrors of $0000-$07FF
$1000-$17FF	$0800	
$1800-$1FFF	$0800	
$2000-$2007	$0008	PPU registers
$2008-$3FFF	$1FF8	Mirrors of PPU registers
$4000-$4017	$0018	APU and IO registers
$4018-$401F	$0008	Disabled APU and IO functionality
$4020-$FFFF	$BFE0	Cartridge space

Conclusion

The Nintendo Entertainment System has been a lasting design in the realm of computer games. It's timeless design and memorable titles continue to today to bring returning players back and draw new players in. It's simple but clever design has also brought many developers to emulate the system to continue the legacy and make the system more accessible.

The NES continues to inspire, with indie titles and genres of music that attempt to emulate the feel and experience of the system that revitalized the home video game market.

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