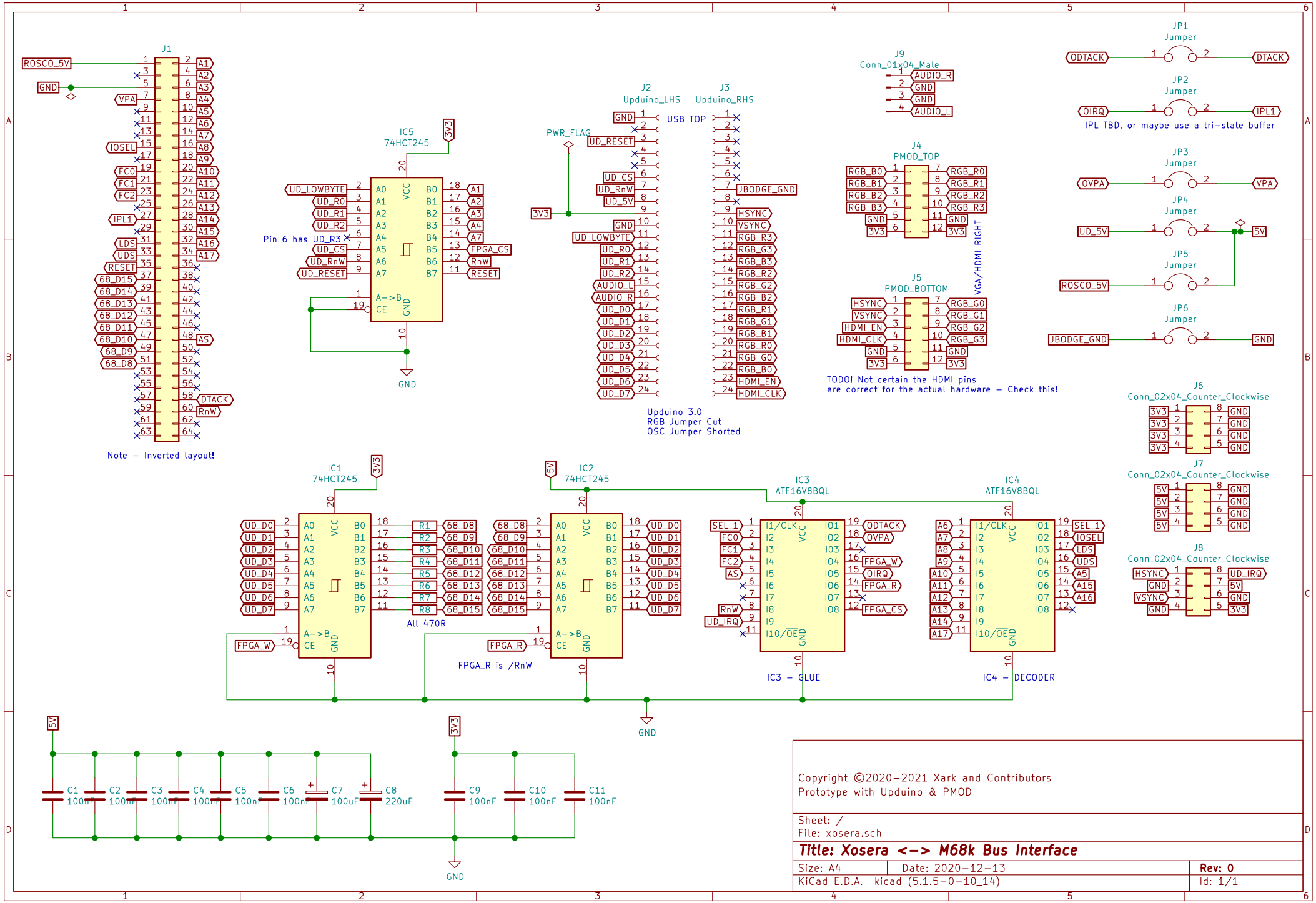
J1
ROSCO_5V
GND
VPA
IOSEL
FC0
FC1
FC2
IPL1
LDS
UDS
RESET
68_D15
68_D14
68_D13
68_D12
68_D11
68_D10
68_D9
68_D8
AS
DTACK
RnW
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17
Note – Inverted layout!
IC5
74HCT245
3V3
UD_LOWBYTE
UD_R0
UD_R1
UD_R2
Pin 6 has UD_R3
UD_CS
UD_RnW
UD_RESET
A0 A1 A2 A3 A4 A5 A6 A7
A–>B
CE
VCC
GND
B0 B1 B2 B3 B4 B5 B6 B7
FPGA_CS
RnW
RESET
J2
Upduino_LHS
J3
Upduino_RHS
USB TOP
PWR_FLAG
JBODGE_GND
HSYNC
VSYNC
RGB_R3
RGB_G3
RGB_B3
RGB_R2
RGB_G2
RGB_B2
RGB_R1
RGB_G1
RGB_B1
RGB_R0
RGB_G0
RGB_B0
HDMI_EN
HDMI_CLK
AUDIO_L
AUDIO_R
UD_D0
UD_D1
UD_D2
UD_D3
UD_D4
UD_D5
UD_D6
UD_D7
Upduino 3.0
RGB Jumper Cut
OSC Jumper Shorted
J9
Conn_01x04_Male
AUDIO_R
GND
GND
AUDIO_L
J4
PMOD_TOP
RGB_B0
RGB_B1
RGB_B2
RGB_B3
GND
3V3
RGB_R0
RGB_R1
RGB_R2
RGB_R3
GND
3V3
VGA/HDMI RIGHT
J5
PMOD_BOTTOM
HSYNC
VSYNC
HDMI_EN
HDMI_CLK
GND
3V3
RGB_G0
RGB_G1
RGB_G2
RGB_G3
GND
3V3
TODO! Not certain the HDMI pins
are correct for the actual hardware – Check this!
JP1
Jumper
ODTACK
DTACK
JP2
Jumper
OIRQ
IPL1
IPL TBD, or maybe use a tri-state buffer
JP3
Jumper
OVPA
VPA
JP4
Jumper
UD_5V
5V
JP5
Jumper
ROSCO_5V
JP6
Jumper
JBODGE_GND
GND
J6
Conn_02x04_Counter_Clockwise
3V3 3V3 3V3 3V3
GND GND GND GND
J7
Conn_02x04_Counter_Clockwise
5V 5V 5V 5V
GND GND GND GND
J8
Conn_02x04_Counter_Clockwise
HSYNC
GND
VSYNC
GND
UD_IRQ
5V
GND
3V3
IC1
74HCT245
3V3
UD_D0
UD_D1
UD_D2
UD_D3
UD_D4
UD_D5
UD_D6
UD_D7
FPGA_W
R1 R2 R3 R4 R5 R6 R7 R8
68_D8
68_D9
68_D10
68_D11
68_D12
68_D13
68_D14
68_D15
All 470R
IC2
74HCT245
5V
FPGA_R
FPGA_R is /RnW
IC3
ATF16V8BQL
SEL_1
FC0
FC1
FC2
A5
RnW
UD_IRQ
I1/CLK
I10/OE
ODTACK
OVPA
FPGA_W
OIRQ
FPGA_R
FPGA_CS
IC3 – GLUE
IC4
ATF16V8BQL
A6
A7
A8
A9
A10
A11
A12
A13
A14
A17
SEL_1
IOSEL
LDS
UDS
A5
A15
A16
IC4 – DECODER
GND
C1 100nF
C2 100nF
C3 100nF
C4 100nF
C5 100nF
C6 100nF
C7 100uF
C8 220uF
C9 100nF
C10 100nF
C11 100nF
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Prototype with Upduino & PMOD
Sheet: /
File: xosera.sch
Title: Xosera <–> M68k Bus Interface
Size: A4
Date: 2020–12–13
Rev: 0
KiCad E.D.A. kicad (5.1.5–0–10_14)
Id: 1/1