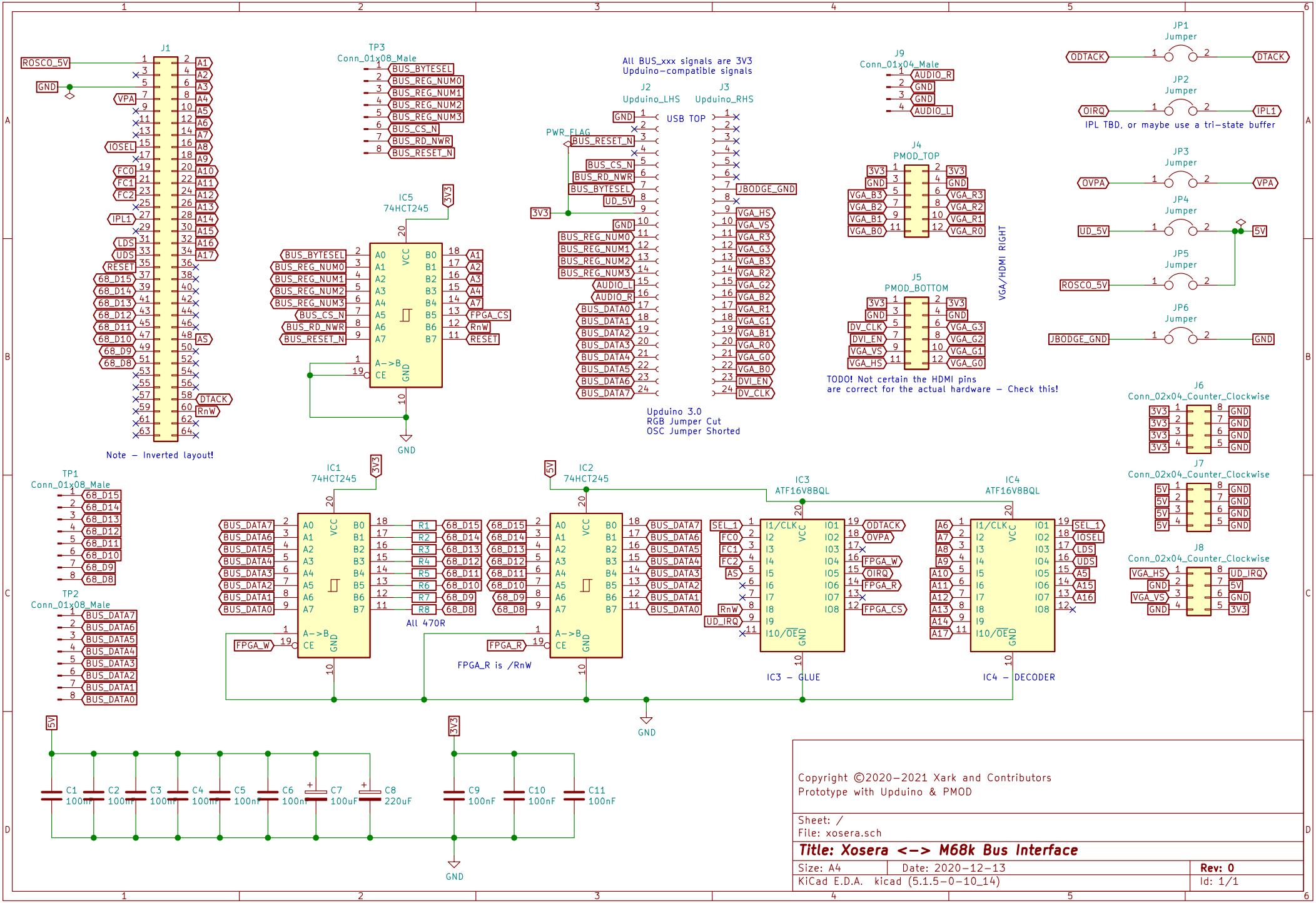
J1
ROSCO_5V
GND
VPA
IOSEL
FC0
FC1
FC2
IPL1
LDS
UDS
RESET
68_D15
68_D14
68_D13
68_D12
68_D11
68_D10
68_D9
68_D8
AS
DTACK
RnW
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
Note – Inverted layout!
TP3
Conn_01x08_Male
BUS_BYTESEL
BUS_REG_NUM0
BUS_REG_NUM1
BUS_REG_NUM2
BUS_REG_NUM3
BUS_CS_N
BUS_RD_NWR
BUS_RESET_N
IC5
74HCT245
3V3
VCC
A–>B
CE
GND
FPGA_CS
All BUS_xxx signals are 3V3
Upduino–compatible signals
J2
Upduino_LHS
J3
Upduino_RHS
USB TOP
PWR_FLAG
JBODGE_GND
UD_5V
AUDIO_L
AUDIO_R
BUS_DATA0
BUS_DATA1
BUS_DATA2
BUS_DATA3
BUS_DATA4
BUS_DATA5
BUS_DATA6
BUS_DATA7
VGA_HS
VGA_VS
VGA_R3
VGA_G3
VGA_B3
VGA_R2
VGA_G2
VGA_B2
VGA_R1
VGA_G1
VGA_B1
VGA_R0
VGA_G0
VGA_B0
DVI_EN
DV_CLK
Upduino 3.0
RGB Jumper Cut
OSC Jumper Shorted
J9
Conn_01x04_Male
J4
PMOD_TOP
J5
PMOD_BOTTOM
VGA/HDMI RIGHT
TODO! Not certain the HDMI pins
are correct for the actual hardware – Check this!
JP1
Jumper
JP2
Jumper
IPL TBD, or maybe use a tri–state buffer
JP3
Jumper
JP4
Jumper
JP5
Jumper
JP6
Jumper
J6
Conn_02x04_Counter_Clockwise
J7
Conn_02x04_Counter_Clockwise
J8
Conn_02x04_Counter_Clockwise
TP1
Conn_01x08_Male
TP2
Conn_01x08_Male
IC1
74HCT245
IC2
74HCT245
5V
R1
R2
R3
R4
R5
R6
R7
R8
All 470R
FPGA_W
FPGA_R
FPGA_R is /RnW
IC3
ATF16V8BQL
IC4
ATF16V8BQL
SEL_1
IC3 – GLUE
IC4 – DECODER
C1
100nF
C2
100nF
C3
100nF
C4
100nF
C5
100nF
C6
100nF
C7
100uF
C8
220uF
C9
100nF
C10
100nF
C11
100nF
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Prototype with Upduino & PMOD
Sheet: /
File: xosera.sch
Title: Xosera <–> M68k Bus Interface
Size: A4
Date: 2020–12–13
Rev: 0
KiCad E.D.A. kicad (5.1.5–0–10_14)
Id: 1/1