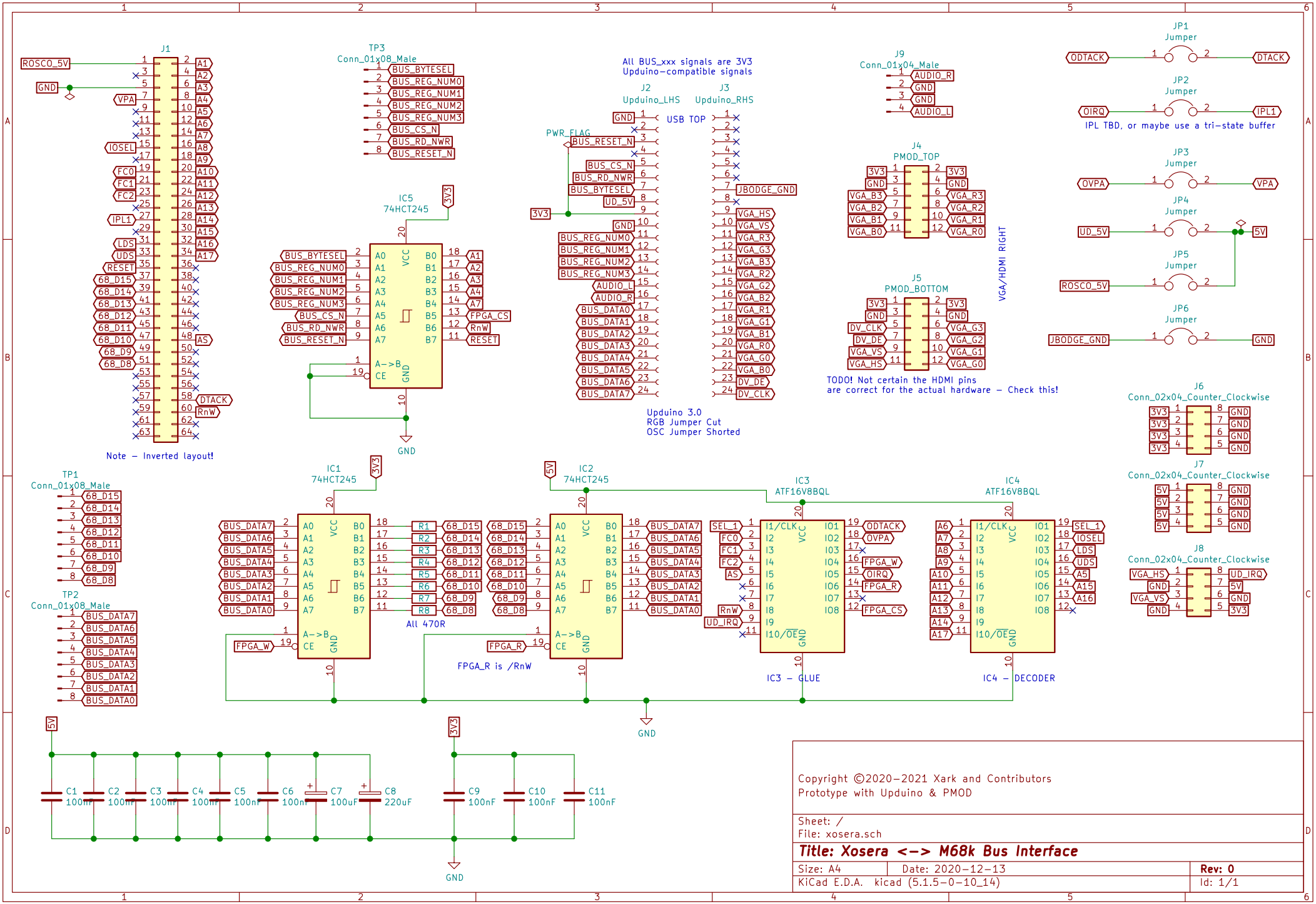
J1
Note – Inverted layout!
TP3
Conn_01x08_Male
IC5
74HCT245
All BUS_xxx signals are 3V3
Upduino-compatible signals
J2
Upduino_LHS
J3
Upduino_RHS
USB TOP
PWR_FLAG
Upduino 3.0
RGB Jumper Cut
OSC Jumper Shorted
J9
Conn_01x04_Male
J4
PMOD_TOP
J5
PMOD_BOTTOM
VGA/HDMI RIGHT
TODO! Not certain the HDMI pins
are correct for the actual hardware – Check this!
JP1
Jumper
JP2
Jumper
IPL TBD, or maybe use a tri-state buffer
JP3
Jumper
JP4
Jumper
JP5
Jumper
JP6
Jumper
J6
Conn_02x04_Counter_Clockwise
J7
Conn_02x04_Counter_Clockwise
J8
Conn_02x04_Counter_Clockwise
TP1
Conn_01x08_Male
TP2
Conn_01x08_Male
IC1
74HCT245
All 470R
IC2
74HCT245
FPGA_R is /RnW
IC3
ATF16V8BQL
IC3 – GLUE
IC4
ATF16V8BQL
IC4 – DECODER
C1 100nF
C2 100nF
C3 100nF
C4 100nF
C5 100nF
C6 100nF
C7 100uF
C8 220uF
C9 100nF
C10 100nF
C11 100nF
GND
Copyright ©2020-2021 Xark and Contributors
Prototype with Upduino & PMOD
Sheet: /
File: xosera.sch
Title: Xosera <-> M68k Bus Interface
Size: A4
Date: 2020-12-13
Rev: 0
KiCad E.D.A. kicad (5.1.5-0-10_14)
Id: 1/1