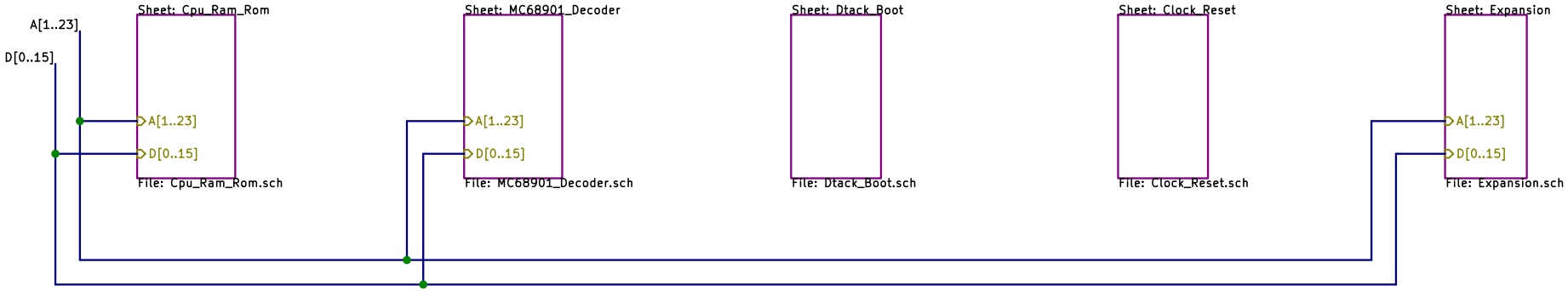
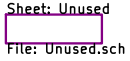
2020-02-25
Double click to enther a Hierarchical sheet.
(RMB & select from sub menu to turn back).



2020-02-25
Address and data busses are routed through the hierarchical schematic.
The Control bus is still routed via global labels, because separately named signals in busses are not implemented yet (Expected in KiCad V6)

Because the Controll bus still uses global labels, all the blue bus lines of that bus is just eye candy. KiCad just relies on the global labels.

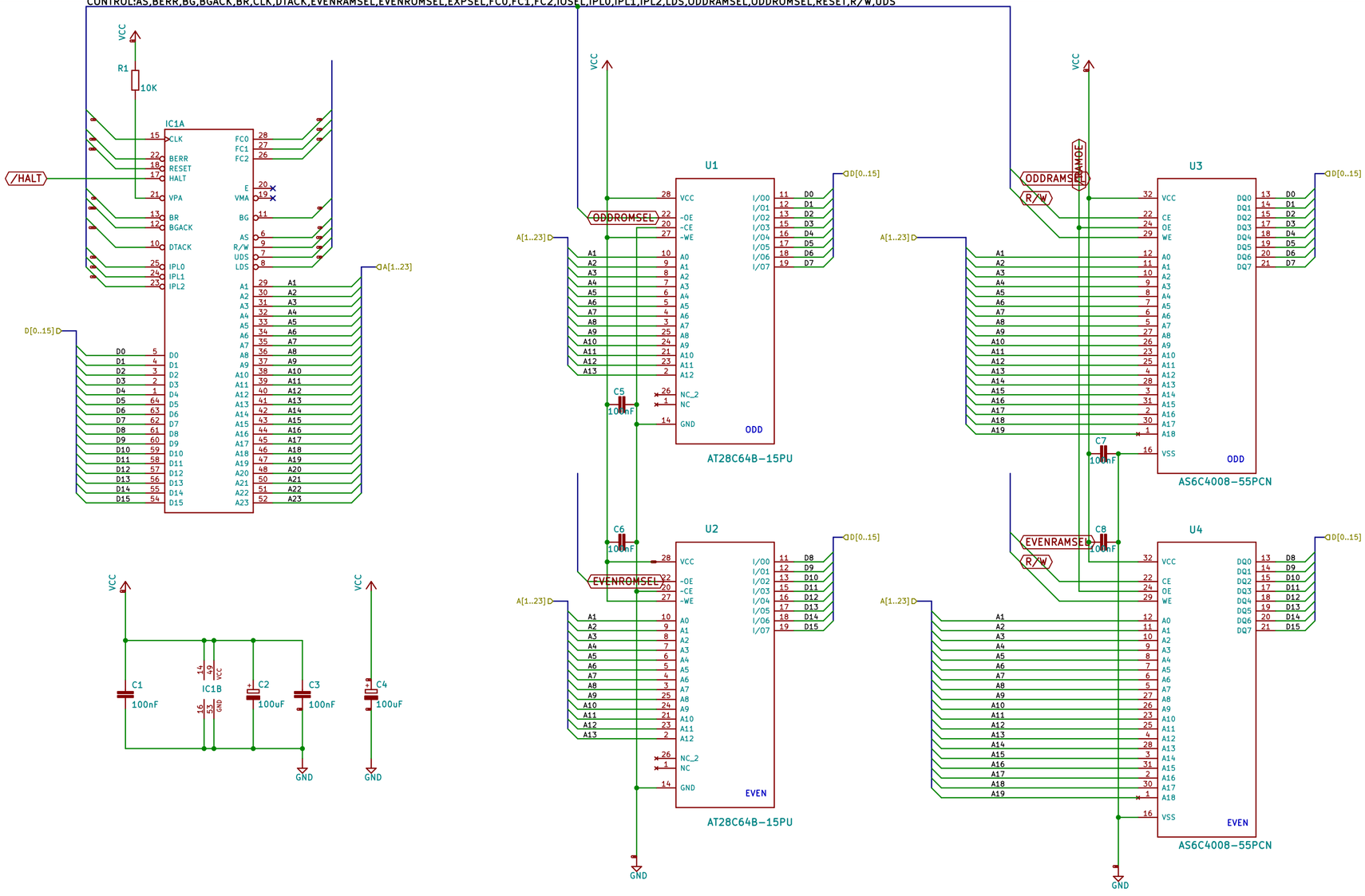
2020-02-25
ERC in EEschem still generates a bunch of errors.
These errors are from faults in symbols, for example 2 ouput pins of different IC's connected together.



2020-02-25
After all the changes I made (and intermediate) I checked the generated connectivity from the schematic with the PCB.
I have not touched the PCB (after automatic conversion) and DRC does not give errors or unrouted connections, which almost guarantees I did not add errors to the schematic.

Sheet: / File: rosco_m68k.sch		
Title:		
Size: A4	Date: 2020-02-25	**Rev:**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 1/7

CONTROL:AS,BERR,BG,BGACK,BR,CLK,DTACK,EVENRAMSEL,EVENROMSEL,EXPSEL,FC0,FC1,FC2,IOSEL,IPL0,IPL1,IPL2,LDS,ODDRAMSEL,ODDROMSEL,RESET,R/W,UDS

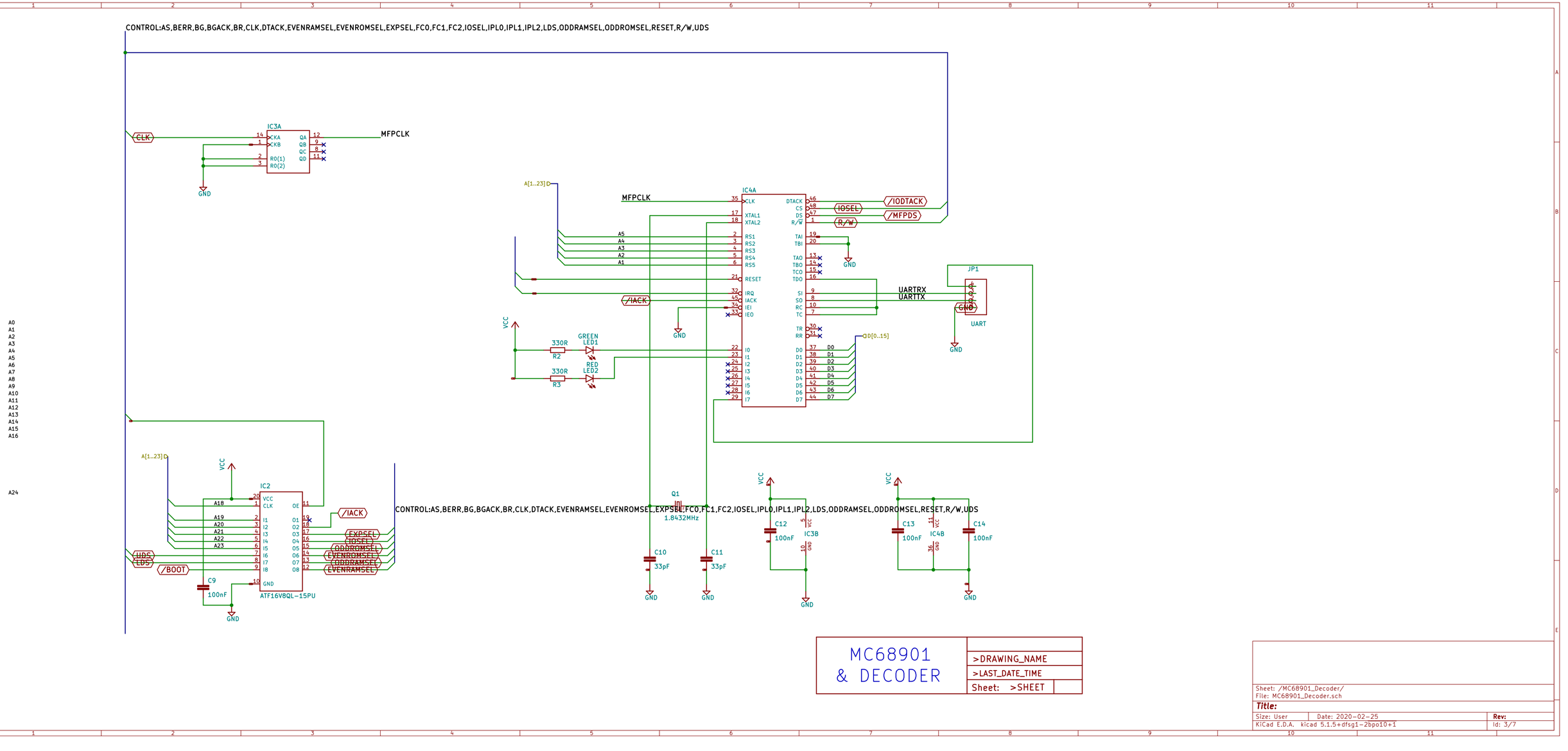


CPU, RAM & ROM	>DRAWING_NAME
	>LAST_DATE_TIME
	Sheet: >SHEET

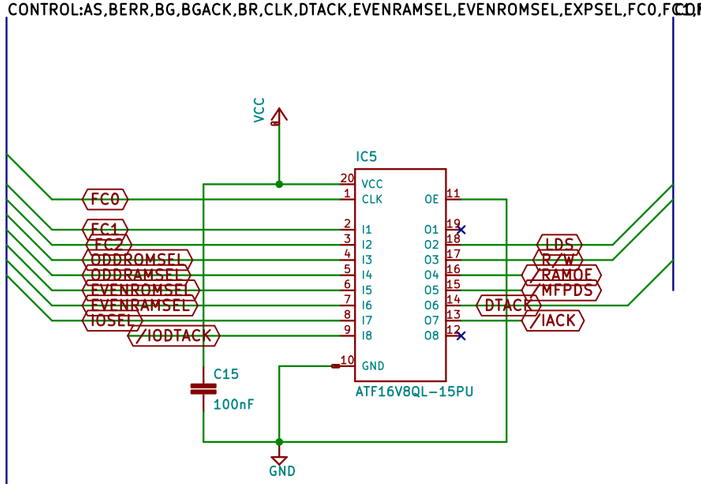
Sheet: /Cpu_Ram_Rom/
File: Cpu_Ram_Rom.sch

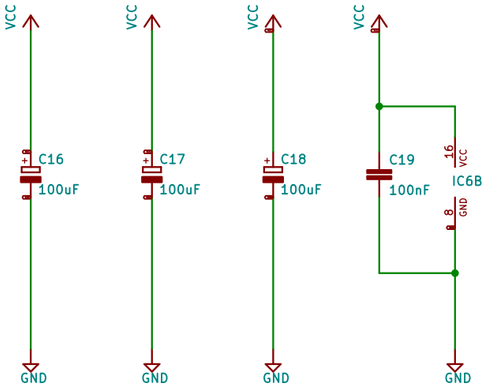
Title:

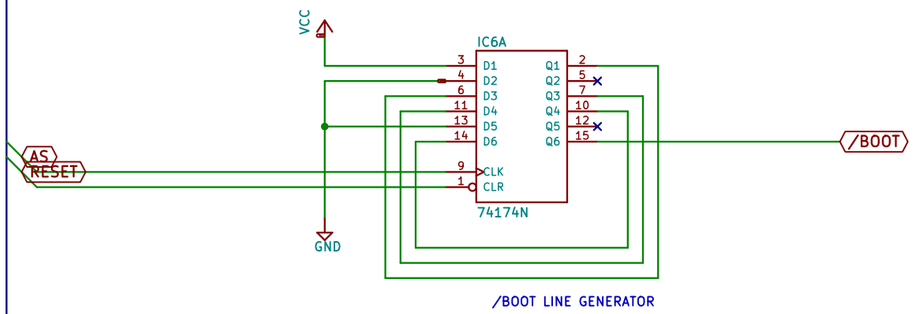
Size: User	Date: 2020-02-25	**Rev:**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 2/7


CONTROL:AS,BERR,BG,BGACK,BR,CLK,DTACK,EVENRAMSEL,EVENROMSEL,EXPSEL,FC0,FC1,FC2,IOSEL,IPL0,IPL1,IPL2,LDS,ODDRAMSEL,ODDROMSEL,RESET,R/W,UDS
IC3A
CLK
MFPCLK
GND
A[1..23]
MFPCLK
IC4A
/IODTACK
IOSEL
/MFPDS
R/W
/IACK
UARTRX
UARTTX
JP1
UART
GND
VCC
330R
R2
GREEN LED1
330R
R3
RED LED2
D[0..15]
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A24
IC2
ATF16V8QL-15PU
/BOOT
UDS
LDS
EXPSEL
IOSEL
ODDROMSEL
EVENROMSEL
ODDRAMSEL
EVENRAMSEL
C9
100nF
Q1
1.8432MHz
C10
33pF
C11
33pF
C12
100nF
IC3B
C13
100nF
IC4B
C14
100nF
CONTROL:AS,BERR,BG,BGACK,BR,CLK,DTACK,EVENRAMSEL,EVENROMSEL,EXPSEL,FC0,FC1,FC2,IOSEL,IPL0,IPL1,IPL2,LDS,ODDRAMSEL,ODDROMSEL,RESET,R/W,UDS
MC68901
& DECODER
>DRAWING_NAME
>LAST_DATE_TIME
Sheet: >SHEET
Sheet: /MC68901_Decoder/
File: MC68901_Decoder.sch
Title:
Size: User
Date: 2020-02-25
Rev:
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1
Id: 3/7

CONTROL:AS,BERR,BG,BGACK,BR,CLK,DTACK,EVENRAMSEL,EVENROMSEL,EXPSEL,FC0,FC1,FC2,IOSEL,IPL0,IPL1,IPL2,LDS,ODDRAMSEL,ODDROMSEL,RESET,R/W,UDS







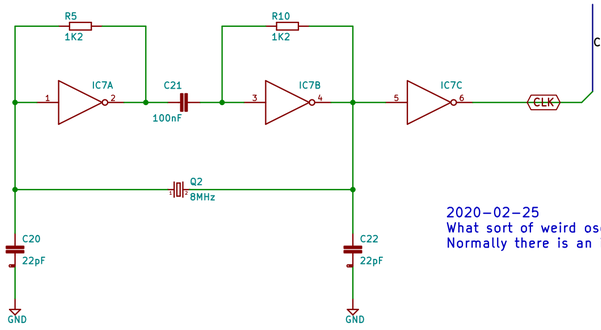
	>DRAWING_NAME
	>LAST_DATE_TIME
	Sheet: >SHEET

DTACK & BOOT

Sheet: /Dtack_Boot/
File: Dtack_Boot.sch

Title:

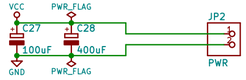
Size: User	Date: 2020-02-25	**Rev:**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 4/7



CONTROL:AS,BERR,BG,BGACK,BR,CLK,DTACK,EVENRAMSEL,EVENROMSEL,EXPSEL,FC0,FC1,FC2,IOSEL,IPL0,IPL1,IPL2,LDS,ODDRAMSEL,ODDROMSEL,RESET,R/W,UDS

2020-02-25
What sort of weird oscillator is this?
Normally there is an inverting amplifier across the Xtal.

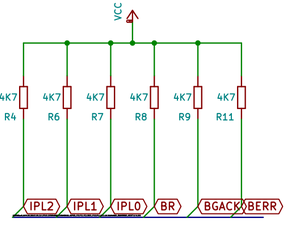
2020-02-25
These 2 Vcc and GND symbols are from KICad's own library.
These symbols have internal Vcc and GND labels, and
If you use these throughout your schematic, you can omit the Vcc
and GND labels generated by the Eagle -> KICad conversion.

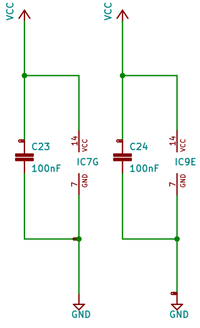


2020-02-25
Personally I would add an Inductor or ferrite core right after the power
connector. (And use a bigger connector with screw terminals).

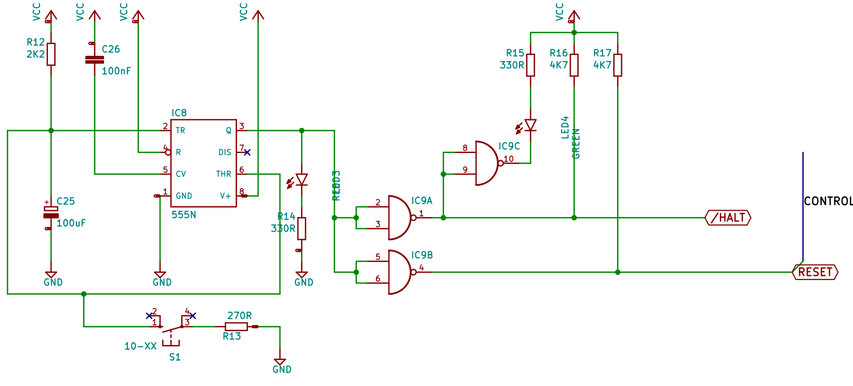
2020-02-25
These "PWR_FLAG" symbols are to indicate that these wires are "Power" connections.
IC normally have Power inputs, and ERC will generate errors if any of
the "power connections" of a component is not connected to these
"PWR_FLAG" symbols.

SYSTEM CLOCK CIRCUIT





RESET CIRCUIT



CONTROL:AS,BERR,BG,BGACK,BR,CLK,DTACK,EVENRAMSEL,EVENROMSEL,EXPSEL,FC0,FC1,FC2,IOSEL,IPL0,IPL1,IPL2,LDS,ODDRAMSEL,ODDROMSEL,RESET,R/W,UDS

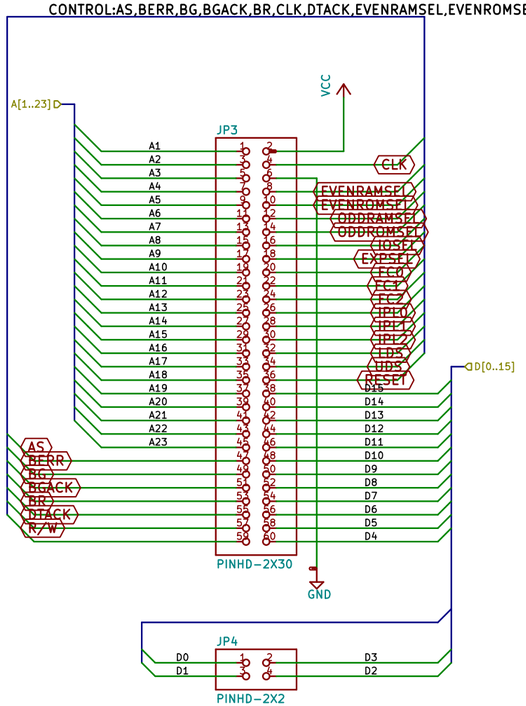
CLOCK & RESET	
	>DRAWING_NAME
	>LAST_DATE_TIME
	Sheet: >SHEET

Sheet: /Clock_Reset/
File: Clock_Reset.sch

Title:

Size: User	Date: 2020-02-25	**Rev:**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 5/7

CONTROL:AS,BERR,BG,BGACK,BR,CLK,DTACK,EVENRAMSEL,EVENROMSEL,EXPSEL,FC0,FC1,FC2,IOSEL,IPL0,IPL1,IPL2,LDS,ODDRAMSEL,ODDROMSEL,RESET,R/W,UDS



EXPANSION

>DRAWING_NAME	
>LAST_DATE_TIME	
Sheet: >SHEET	

Sheet: Expansion.sch
File: Expansion.sch

Title:

Size: User	Date: 2020-02-25	**Rev:**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 6/7

In KiCad, unused pins must have the "No Connect" flag.
If the do not have this "cross", then ERC will generate errors.

H1
MountingHole

H2
MountingHole

H3
MountingHole

H4
MountingHole

2020-02-25
I've added some mounting holes here.
Add them to the PCB if you like ...

	>DRAWING_NAME
	>LAST_DATE_TIME
	Sheet: >SHEET

UNUSED GATES

Sheet: /Unused/
File: Unused.sch

Title:

Size: User	Date: 2020-02-25	**Rev:**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 7/7