Adeeb_B190737CS_Q01_TB.v ×   Adeeb_B190737CS_Q01.v   Adeeb_B190737CS_TB_Q08.v

D: > Adeeb > NITC > 2nd Year > Sem3 > Logic Design > Lab > Assignment > Adeeb_b190737CS_A02_Eval_R >   Adeeb_B190737CS_Q01_TB.v

```verilog
326        or_gate_16 or1(w1,x,16'b0000_1000_0000_0000);
327
328        mux_16_2x1 mux1(out,w0,w1,f1);
329
330    endmodule
331
332
333    module circuitll_tb();
334
335        reg[31:0] x;
336        reg zx,nx,zy,ny,f,f1,no;
337        wire[15:0] out;
338        wire zr,ng;
339
340
341        initial
342        begin
343            zx=1;nx=0;zy=1;ny=0;f=1;no=0;
344            x=0;
345            f1= 0;
346        end
347
348        always
349        begin
350            #5 zx=1;nx=1;zy=0;ny=1;f=1;f1=0;no=0;
351            #5 zx=0;nx=0;zy=0;ny=1;f=1;f1=0;no=1;
352            #5 zx=0;nx=1;zy=0;ny=1;f=0;f1=0;no=1;
353            #5 zx=0;nx=0;zy=1;ny=1;f=1;f1=0;no=0;
354            #5 zx=0;nx=1;zy=0;ny=0;f=1;f1=0;no=1;
355            #5 zx=0;nx=0;zy=0;ny=0;f=0;f1=1;no=0;
```