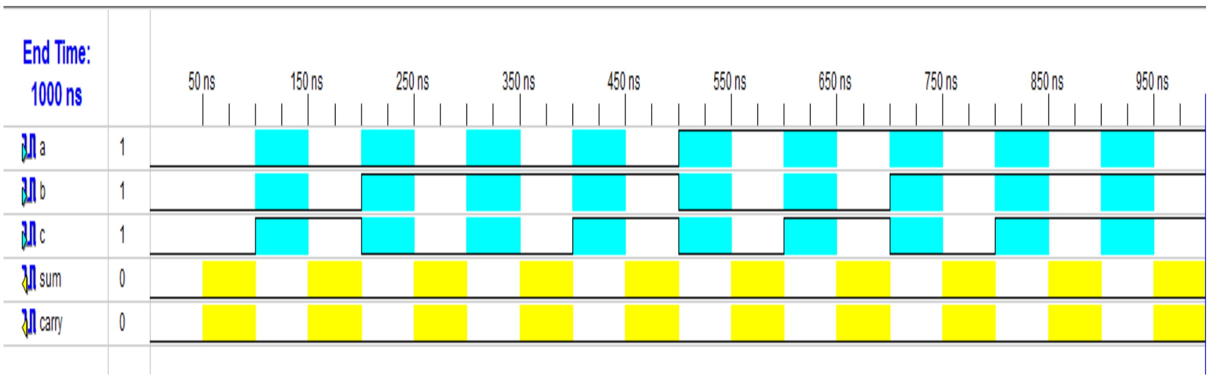
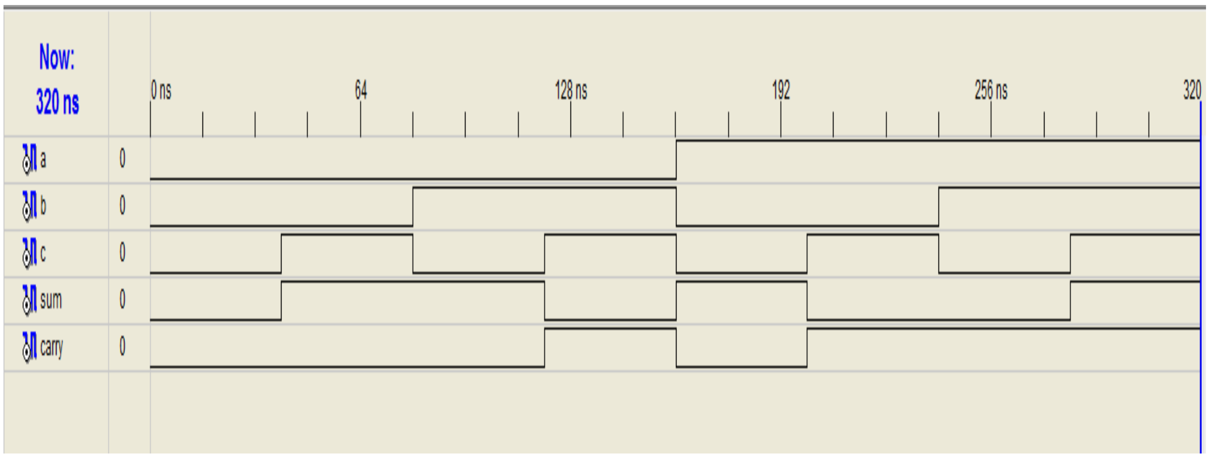
FULL ADDER

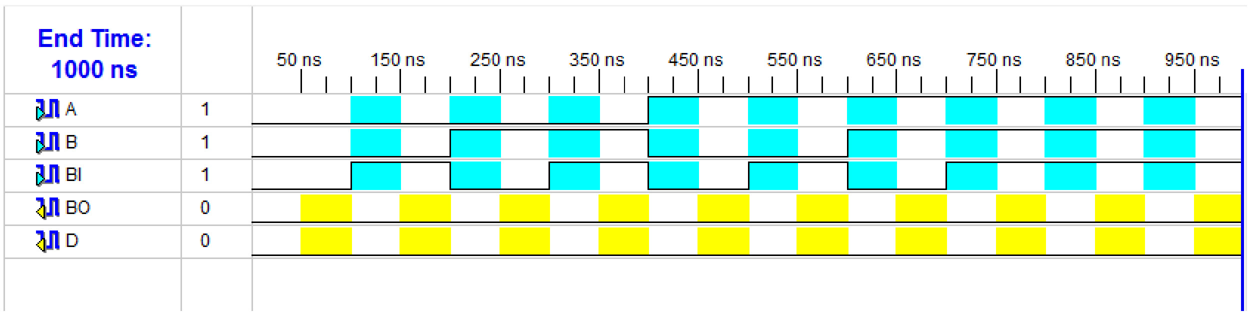
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity fulladder is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           c : in  STD_LOGIC;
           sum : out  STD_LOGIC;
           carry : out  STD_LOGIC);
end fulladder;

architecture Behavioral of fulladder is

begin
sum<=a xor b xor c;
carry<=((a and B) or (a and C) or (b or c));

end Behavioral;
```

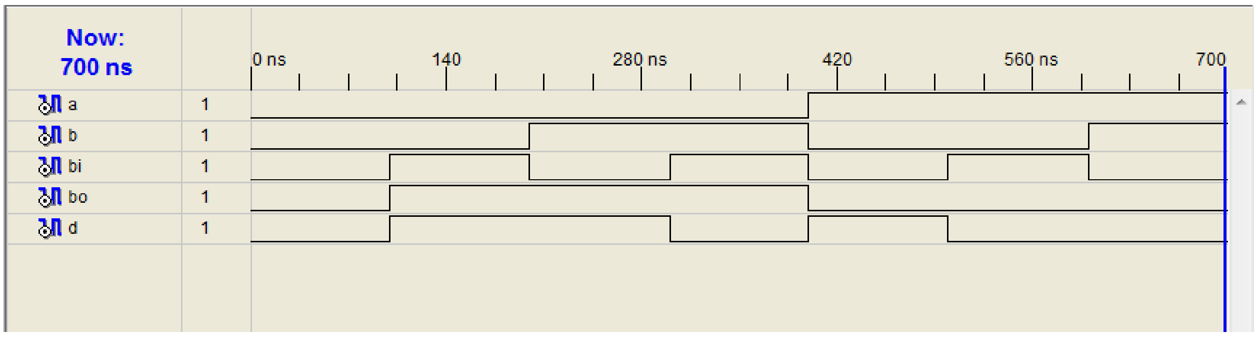




HALF SUBTRACTOR

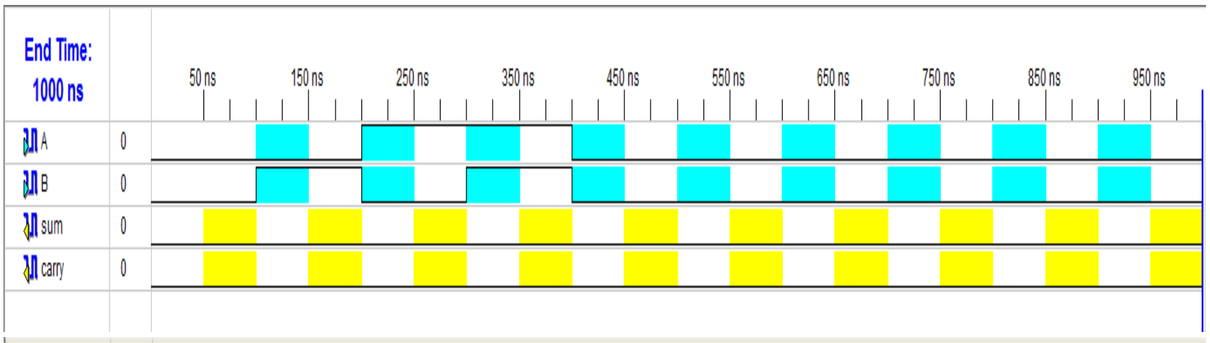
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity fulsubtractor is
    Port ( A : in  STD_LOGIC;
           B : in  STD_LOGIC;
           BI : in  STD_LOGIC;
           BO : out STD_LOGIC;
           D : out  STD_LOGIC);
end fulsubtractor;

architecture Behavioral of fulsubtractor is

begin
D<=A XOR B XOR BI ;
BO<=(((Not A) and B) OR ((Not A) and BI) OR(B and BI));

end Behavioral;
```

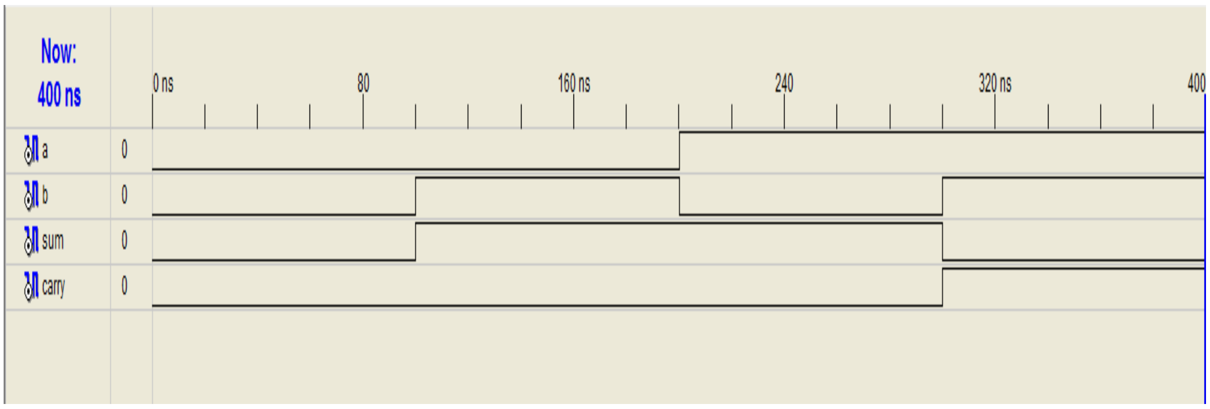




HALF ADDER

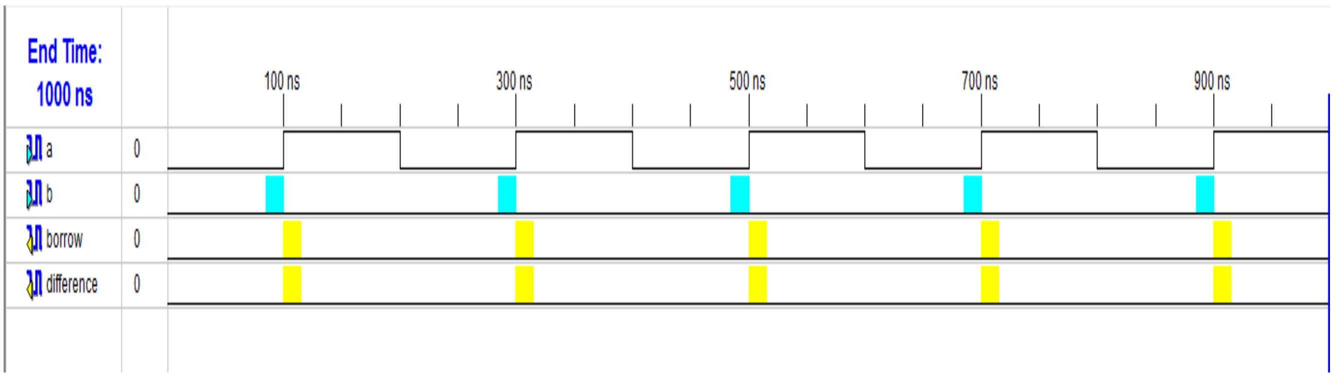
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity halfadder is
    Port ( A : in  STD_LOGIC;
          B: in  STD_LOGIC;
           sum : out  STD_LOGIC;
           carry : out  STD_LOGIC);
end halfadder;

architecture Behavioral of halfadder is

begin
sum<= ((not a) and B)or(a and (not B));
carry<= a and B;
end Behavioral;
```

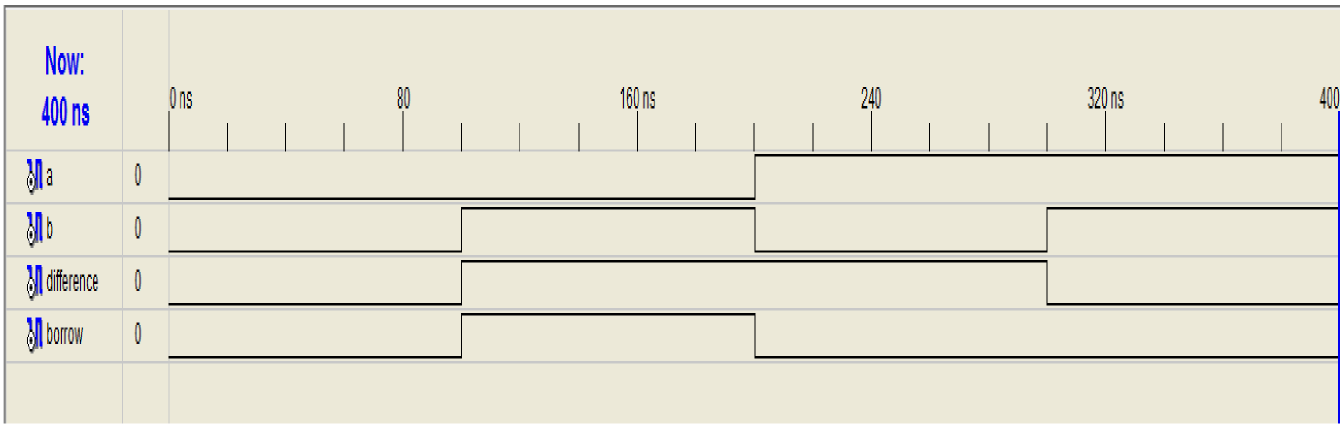




HALF SUBTRACTOR

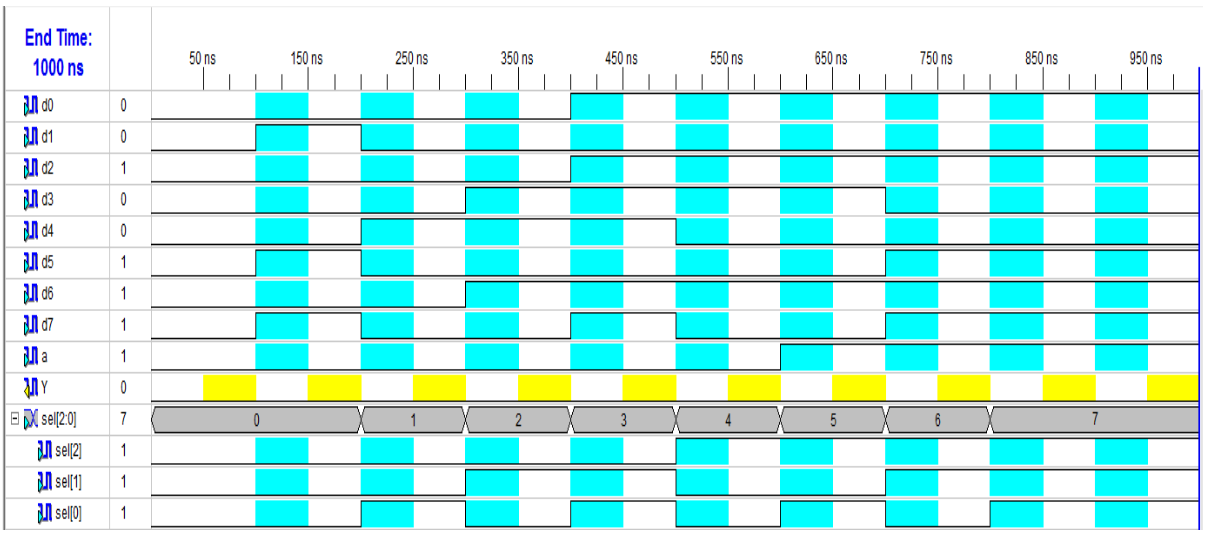
```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity halfsubtracter is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           difference  : out  STD_LOGIC;
           borrow : out  STD_LOGIC);
end halfsubtracter;

architecture Behavioral of halfsubtracter is

begin
difference<=(a xor b);
borrow<=((not a)and b);

end Behavioral;
```

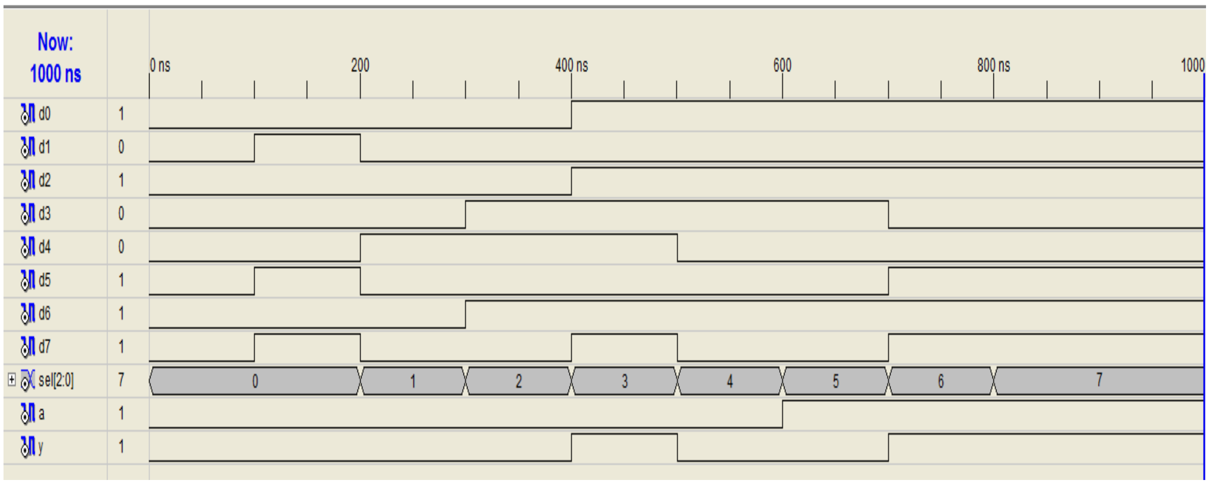




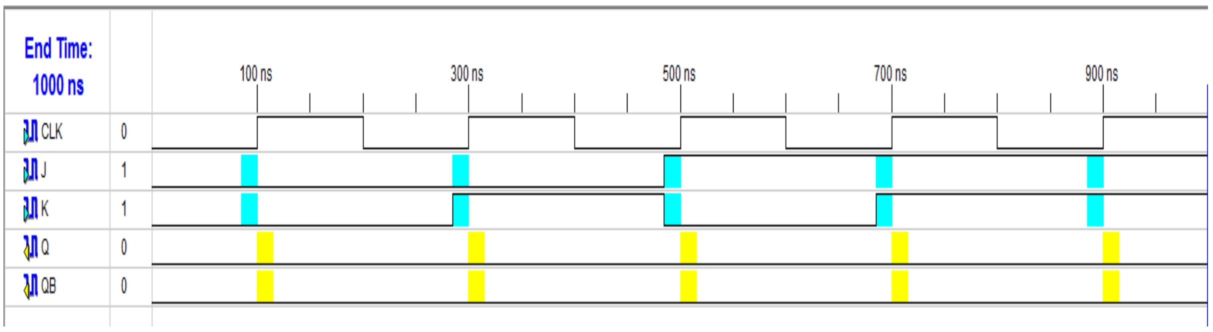
8:1 MUX

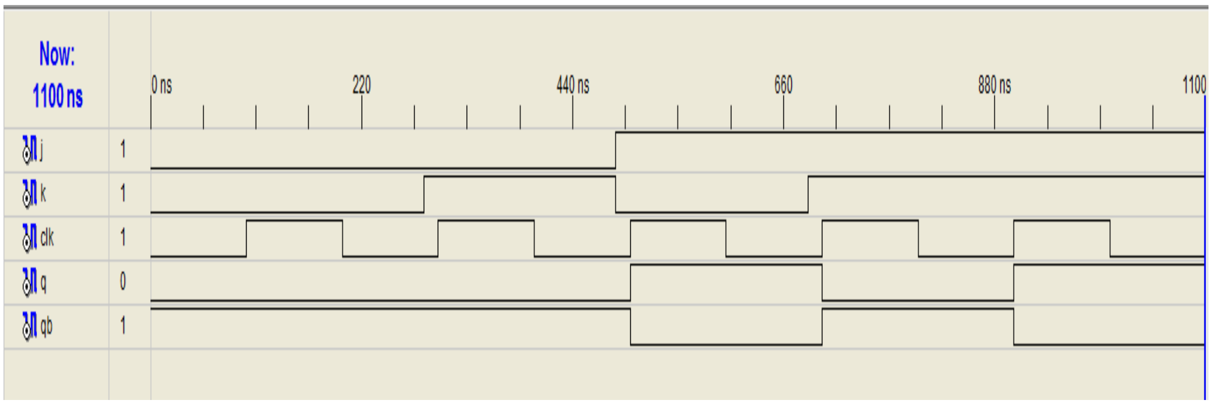
```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity mm is
    Port ( d0 : in  STD_LOGIC;
           d1 : in  STD_LOGIC;
           d2 : in  STD_LOGIC;
           d3 : in  STD_LOGIC;
           d4 : in  STD_LOGIC;
           d5 : in  STD_LOGIC;
           d6 : in  STD_LOGIC;
           d7 : in  STD_LOGIC;
           sel : in  STD_LOGIC_VECTOR (2 downto 0);
           a : in  STD_LOGIC;
           Y : out  STD_LOGIC);
end mm;

architecture Behavioral of mm is

begin
Y<=d0 when sel="000" else
d1 when sel="001" else
d2 when sel="010" else
d3 when sel="011" else
d4 when sel="100" else
d5 when sel="101" else
d6 when sel="110" else
d7;
end Behavioral;
```



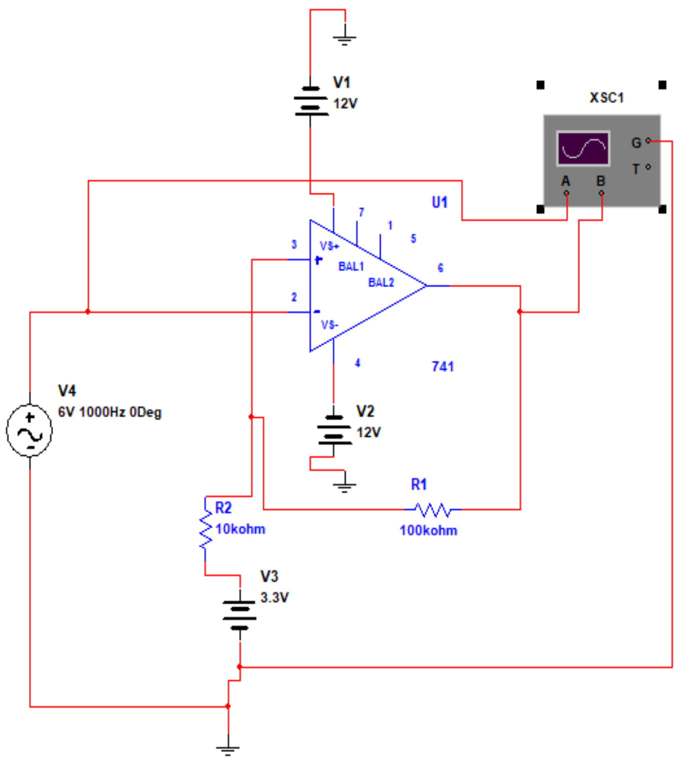


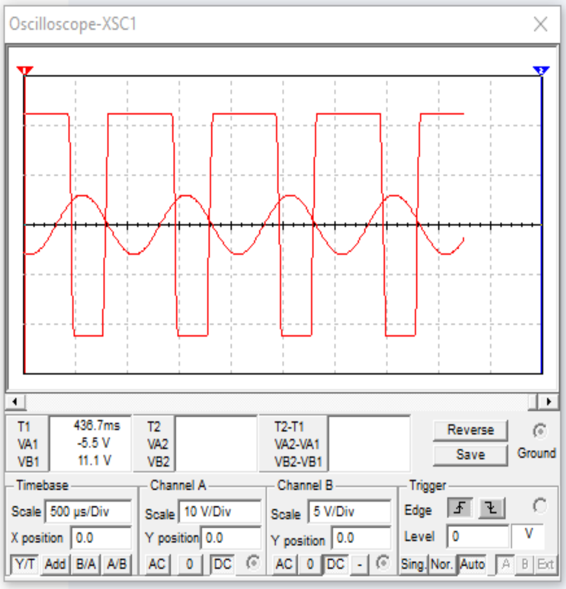
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity JKFF is
Port ( J, K, CLK : in STD_LOGIC;
Q, QB : out STD_LOGIC);
end JKFF;
architecture Behavioral of JKFF is
begin
process (CLK)
variable TEMP: STD_LOGIC := '0';
begin
if (CLK = '1') then
if (J = '0' and K = '0') then TEMP := TEMP;
elsif (J = '1' and K = '1') then TEMP := not TEMP;
elsif (J = '0' and K = '1') then TEMP := '0';
else TEMP := '1';
end if;
end if;
Q <= TEMP;
QB <= not TEMP;
end process;
end Behavioral;
```





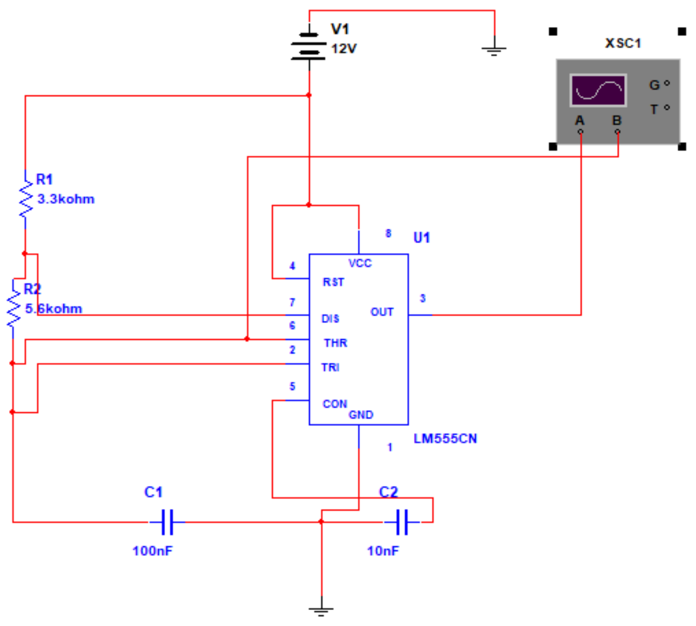
Window comparator

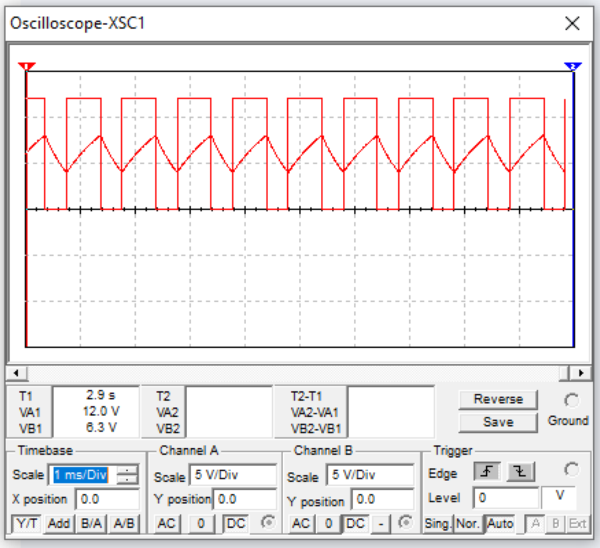



Oscilloscope-XSC1

```
T1     436.7ms   T2          T2-T1
VA1    -5.5 V    VA2         VA2-VA1
VB1    11.1 V    VB2         VB2-VB1

Timebase              Channel A              Channel B              Trigger
Scale 500 µs/Div      Scale 10 V/Div         Scale 5 V/Div          Edge
X position 0.0        Y position 0.0         Y position 0.0         Level 0 V
```

Astable Multivibrator

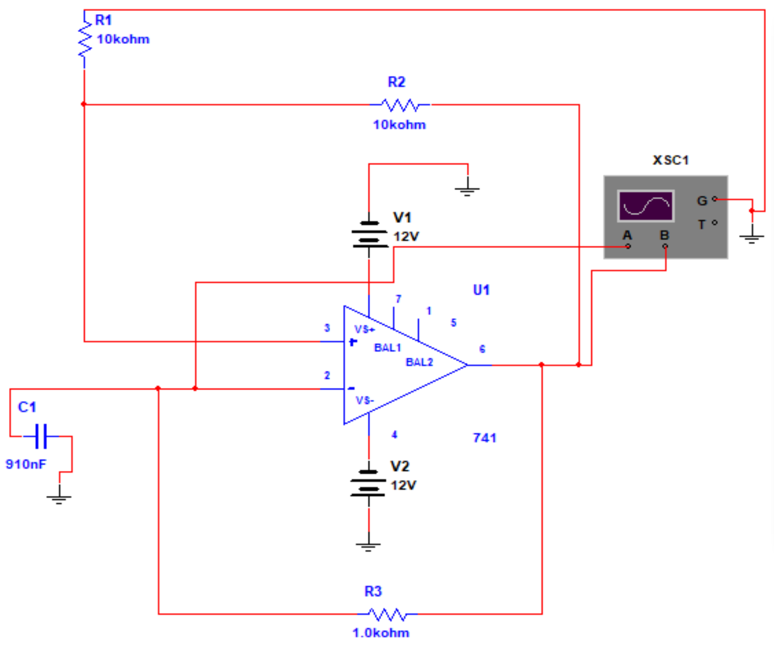


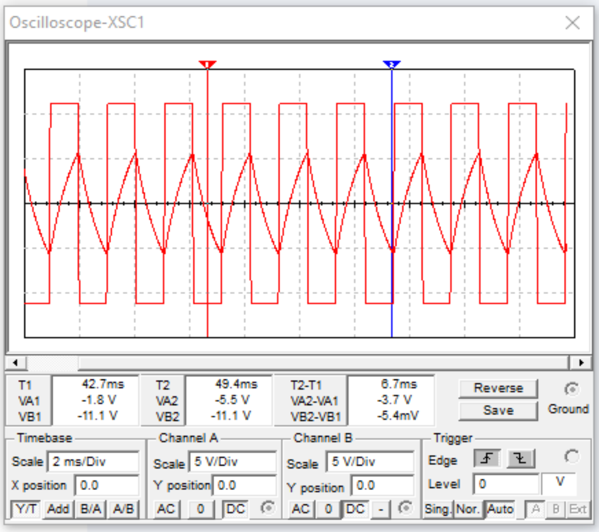

Oscilloscope-XSC1

```
T1      2.9 s     T2      T2-T1
VA1     12.0 V    VA2     VA2-VA1
VB1     6.3 V     VB2     VB2-VB1
```

Timebase: Scale 1 ms/Div, X position 0.0, Y/T
Channel A: Scale 5 V/Div, Y position 0.0, DC
Channel B: Scale 5 V/Div, Y position 0.0, DC
Trigger: Edge, Level 0 V, Auto

Relaxation Oscillator




Oscilloscope-XSC1

```
T1      42.7ms    T2      49.4ms    T2-T1     6.7ms
VA1     -1.8 V    VA2     -5.5 V    VA2-VA1   -3.7 V
VB1     -11.1 V   VB2     -11.1 V   VB2-VB1   -5.4mV
```

Timebase: Scale 2 ms/Div, X position 0.0, Y/T
Channel A: Scale 5 V/Div, Y position 0.0, DC
Channel B: Scale 5 V/Div, Y position 0.0, DC
Trigger: Edge, Level 0 V, Auto