MODULE – 1

ANALOG ELECTRONIC CIRCUITS

OPTOELECTRONIC DEVICES

Optoelectronic Devices is the field that deals with study of devices that emit, detect and control light in the wavelength spectrum ranging from ultraviolet to far infrared. They include electrical-to-optical (convert electrical energy into light energy) and optical-to-electrical (convert light energy into electrical energy) transducers. Optocouplers also come in this broad category.

PHOTODIODES:

Photodiode is a light detector semiconductor device that converts light energy into electric current or voltage which depends upon the mode of operation.

The upper cut-off wavelength of a photodiode is given by; $\lambda_{cc} = \frac{1240}{EE_{gg}}$

where, $\lambda\lambda_{cc}$ is the cut-off wavelength in nm and EE_{gg} is the bandgap energy in eV.

A normal p-n junction diode allows a small amount of electric current, under reverse bias, due to minority charge carriers. To increase the electric current under reverse bias condition, we need to generate more minority carriers. The external reverse voltage applied to the p-n junction diode will supply energy to the minority carriers, but it will not increase the population of minority charge carriers.

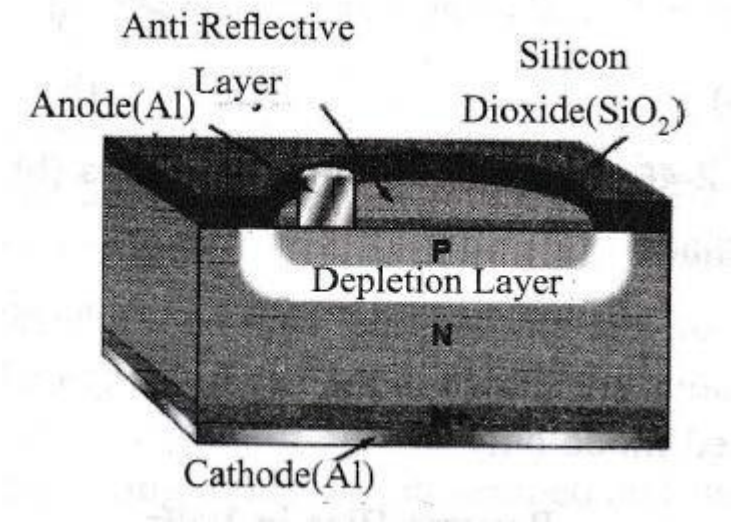
A small number of minority carriers are generated due to external reverse bias voltage. The minority carriers generated at n-side or p-side will recombine in the same material, before they cross the junction. As a result, no electric current flows due to these charge carriers. For example, the minority carriers generated in the p-type material experience a repulsive force from the external voltage and try to move towards n-side. However, before crossing the junction, the free electrons recombine with the holes within the same material. As a result, no electric current flows.

To overcome this problem, we need to apply external energy directly to the depletion region to generate more charge carriers. A special type of diode called photodiode is designed to generate more number of charge carriers in depletion region. In photodiodes, we use light or photons as the external energy to generate charge carriers in depletion region.

Construction:

The typical construction of a photodiode is illustrated in the following Figure. This example uses a construction technique called *ion implantation* where the surface of a layer of N-type is bombarded with P- type silicon ions to produce a P-type layer of about 1 µm (micrometre) thick. During the formation of the diode, excess electrons move from N-type towards P-type and excess holes move from P-type towards

N-type; this process is called *diffusion*, resulting in the removal of free charge carriers close to the PN-junction, so creating a depletion layer as shown in the following Figure.

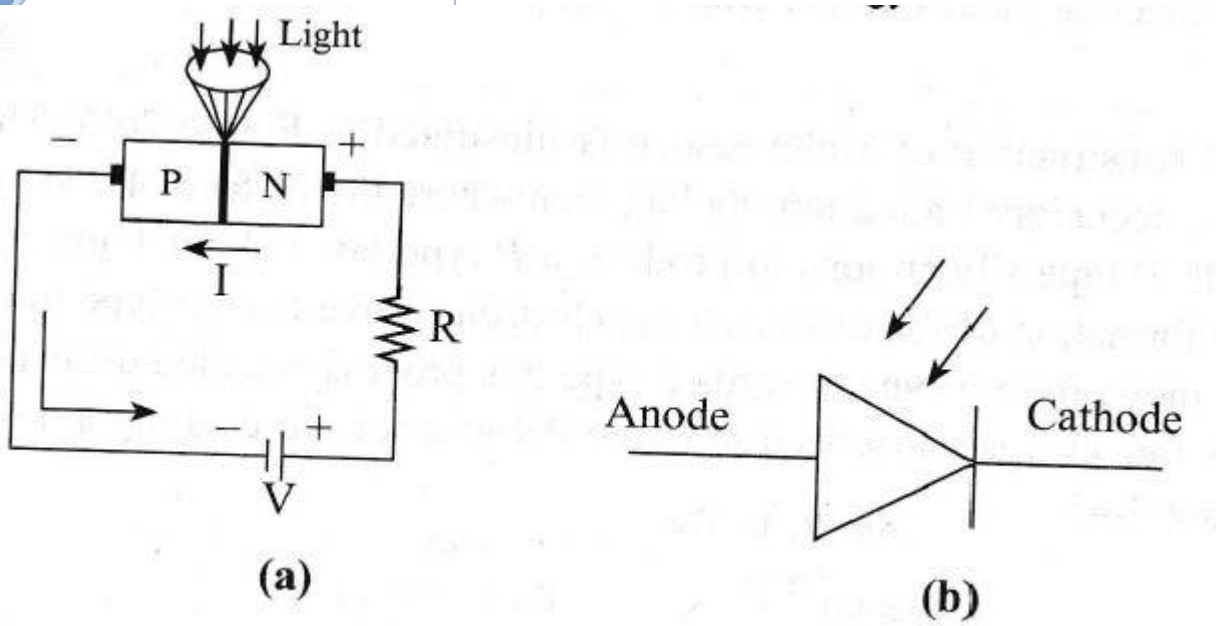


The (light facing) top of the diode is protected by a layer of Silicon Dioxide (SiO_2) in which there is a window for light to shine on the semiconductor. This window is coated with a thin anti-reflective layer of Silicon Nitride (SiN) to allow maximum absorption of light and an anode connection of aluminium (AI) is provided to the P-type layer. Beneath the N-type layer, there is a more heavily doped N+ layer to provide a low resistance connection to the cathode.

Working Principle:

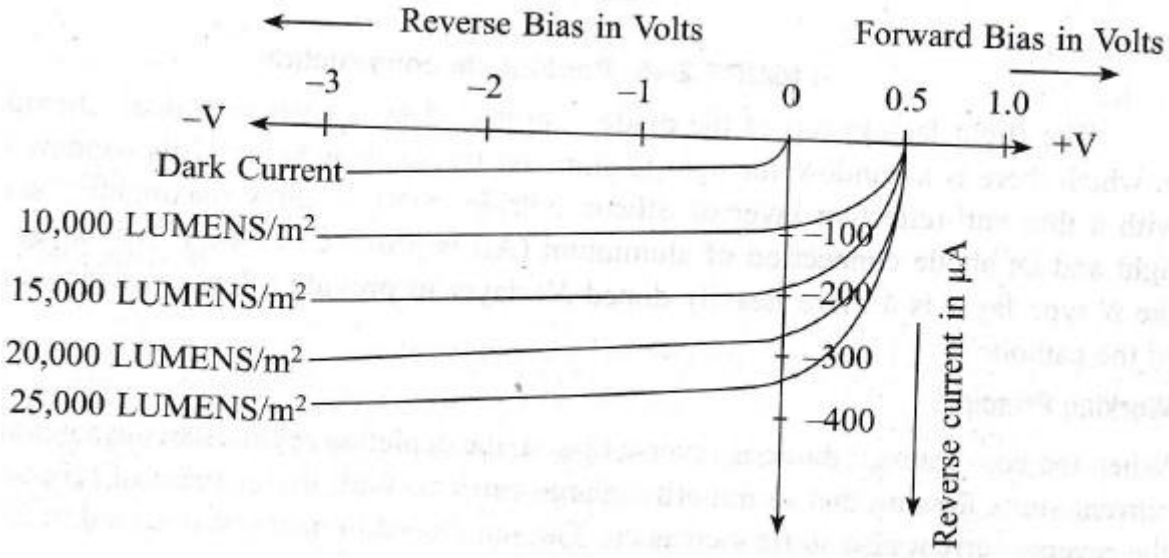
When the conventional diode is reverse biased, the depletion region starts expanding and the current starts flowing due to minority charge carriers. With the increase of reverse voltage, the reverse current also starts increasing. The same condition can be obtained in photodiode without applying reverse voltage.

The following Figure shows photo diode bias symbol. The junction of Photodiode is illuminated by the light source; the photons strike the junction surface. The photons impart their energy in the form of light to the junction. Due to which electrons from valence band get the energy to jump into the conduction band. This leaves positively charged holes in the valence band, so producing 'electron-hole pairs' in the depletion layer. Some electron-hole pairs are also produced in P and N layers, but apart from those produced in the diffusion region N layers, most will be re-absorbed within the P and N materials as heat. The electrons in the depletion layer are then swept towards the positive potential on the cathode, and the holes swept towards the negative potential on the anode, so creating a photo current. In this way, the photodiode converts light energy into electrical energy.



V-I Characteristics of Photodiode:

The characteristics curve of the photodiode can be understood with the help of the following Figure. The characteristics are shown in the negative region because the photodiode can be operated in reverse biased mode only.



The reverse saturation current in the photodiode is denoted by I_0, It varies linearly with the intensity of photons striking the diode surface. The current under large reverse bias is the summation of reverse saturation current and short circuit current.

$$II = II_{sscc} + II_0\ (1 - ee^{VV/\Delta VVV})$$

Where I_{sc} is the short circuit current, V is positive for forward voltage and negative for reverse bias, V_t is volt equivalent for temperature, Δ is unity for germanium and, 2 for silicon.

Applications:

- Photodiodes are used in consumer electronics devices like smoke detectors, compact disc players, and televisions and remote controls in VCRs.
- In other consumer devices like clock radios, camera light meters, and street lights, photoconductors are more frequently used rather than photodiodes.
- Photodiodes are frequently used for exact measurement of the intensity of light in science and industry. Generally, they have an enhanced, more linear response than photoconductors.

LIGHT EMITTING DIODE (LED):

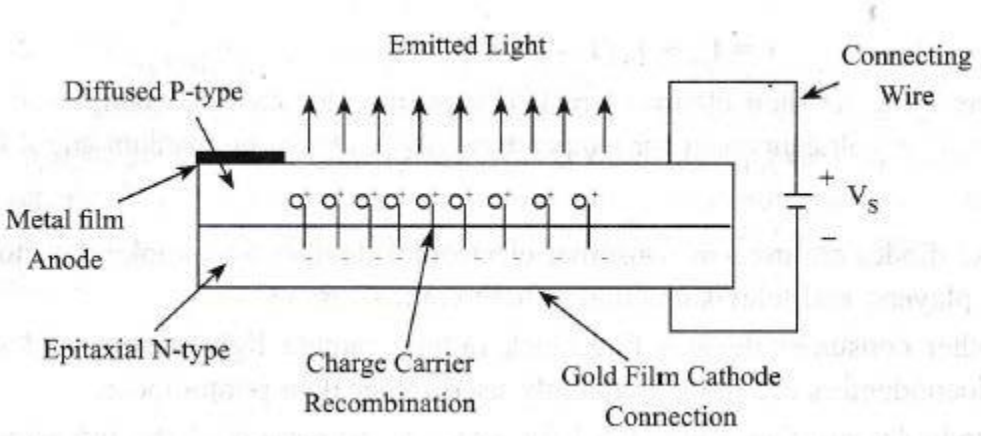
The LED is a PN-junction diode which emits light when an electric current passes through it in the forward direction. A P-N junction can convert absorbed light energy into a proportional electric current. The same process is reversed here (i.e. the P-N junction emits light when electrical energy is applied to it). This phenomenon is generally called *Electroluminescence*.

Electroluminescence is the properly of the material to convert electrical energy into light energy and later it radiates this light energy. Different sizes of light emitting diodes are available in market form lmm^2 to onward.

Construction:

The semiconductor material used in LED is *Galliurn Arsenide (GaAs)*, *Gallium phosphide (GaP)* or *Gallium Arsenide Phosphide (GaAsP)*. Any of the above-mentioned compounds can be used for the construction of LED, but the color of radiated light changes with the change in material (for example, GaP material gives green/red color with forward voltage of 2.2V).

The semiconductor layer of *P-type* is placed above *N-type* because the charge carrier recombination occurs in *P-type*. Besides, it is the surface of the device, and thus, the light emitted can be easily seen on the surface. If *P-type* is placed below the *N-type*, the emitted light cannot be seen. The following Figure shows cross sectional view of diffused LED.

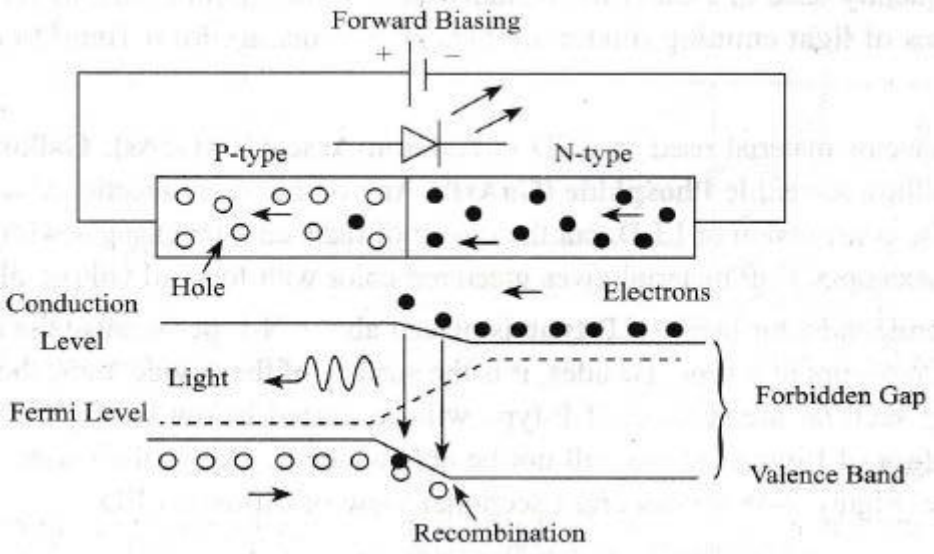


The *P-type* layer is formed from diffusion of semiconductor material. On the other side, in *N-type* region, the epitaxial layer is grown on *N-type* substrate. The metal film is used on the *P-type* layer to provide anode connection to the diode. Similarly, Gold-film layer is coated on *N-type* to provide cathode connection. The Gold-film layer on N-type also provides reflection from the bottom surface of the diode. If any significant part of radiated light tends to hit bottom surface then that will be reflected from the bottom surface to the device top surface. This increases LED's efficiency.

Working Principle:

The charge carriers recombine in a forward-biased P-N junction as the electrons cross from the N-region and recombine with the holes existing in the P-region. Free electrons are in the conduction band of energy levels, while holes are in the valence energy band. Thus the energy level of the holes is less than the energy levels of the electrons. Some portion of the energy must be dissipated to recombine the electrons and the holes. This energy is emitted in the form of heat and light.

The working of the LED depends on the quantum theory. The quantum theory states that, when the energy of electrons decreases from the higher level to lower level, it emits energy in the form of photons. The energy of the photons is equal to the gap between the higher and lower level, as shown in the following Figure.



The LED is forward biased, which allows the current to flow in the forward direction. The flow of current is because of the movement of electrons in the opposite direction. The recombination shows that the electrons move from the conduction band to valence band and they emit electromagnetic energy in the form of photons. The energy of photons is equal to the gap between the valence and the conduction band. Color of light can be determined by the band gap of semiconductor material.

Applications:

- LEDs are used in remote control systems such TV or LCD remote.
- Used in traffic signals for controlling the traffic crowds in cites.
- Used in digital computers for displaying the computer data.
- Used in electronic calculators for showing the digital data.
- Used in digital watches and automotive heat lamps.

PHOTOCOUPLER:

Photocoupler or Optocoupler is a device that transfers electrical signals between two isolated circuits by using light.

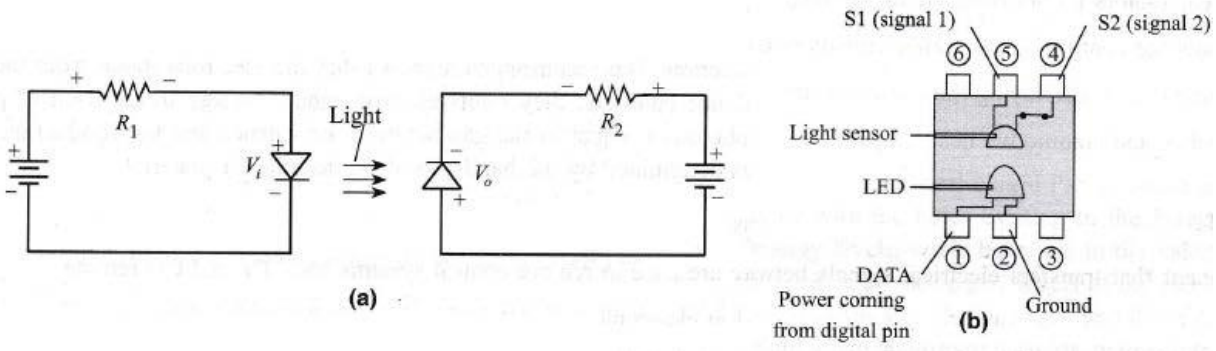
Photocouplers are used in many functions: they can be used to link data across two circuits; they can be used within optical encoders, where the optocoupler provides a means of detecting visible edge transitions on an encoder wheel to detect position, etc., and they can be used in many other circuits where optical links and transitions are needed. As a result, optical couplers or photocouplers are found in many circuits.

Construction:

All optocouplers consist of two elements: a light source (a LED) and a photosensor (a photoresistor, photodiode, phototransistor, silicon-controlled rectifier (SCR), or triac); which are separated by a dielectric (non-conducting) barrier.

Working Principle:

When input current is applied to the LED, it switches ON and emits infrared light; the photosensor then detects this light and allows current to flow through the output side of the circuit; conversely, when the LED is off, no current will flow through the photosensor. By this method, the two flowing currents are electrically isolated. It consists of LED and photodiode; where the circuits are isolated electrically. In the following Figure, LED is forward biased, photodiode is reverse biased and output exists across R_2.



The Figure (a) describes the basic operation of an optocoupler. When current is not being applied via Pin 1, the LED is off, and the circuit connected to Pins 4 and 5 is experiencing no current flow. When power is applied to the input circuit, the LED switches on, the sensor detects the light, closes the switch and initiates current flow in the output circuit, as shown in the Figure (b).

Applications:

- Input and output switching in electronically noisy environments.
- Controlling transistors and triacs.
- Switch-mode power supplies.
- PC/ Modem communication.
- Signal isolation.
- Power control.

BJT BIASING

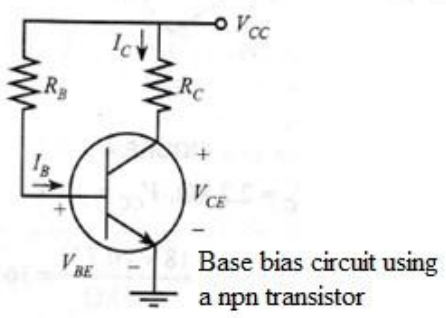
A *transistor* (*Bipolar Junction Transistor-BJT*) is a sandwich of one type of semiconductor (P-type or N-type) between two layers of other type. Transistors are of two types: *p-n-p transistor* and *n-p-n transistor*. There are three distinct regions (hence, terminals) in a transistor: *Emitter*, *Base*, and *Collector*.

For any circuit, four-terminals would be required: two-input-terminals and two-output-terminals. Hence, for a transistor, one of the three terminals will be common to both input and output in a circuit. Thus, there are three different modes of operation for a transistor: *Common-Base Connection (CB)*, *Common Emitter Connection (CE)*, and *Common Collector Connection (CC)*.

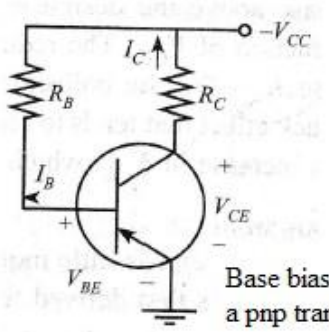
Transistor Biasing is the establishment of suitable dc-values such as I_C, V_{CE}, I_B, etc., by using a dc-source. When BJT is properly biased, amplification of signal takes place. There are mainly three types of biasing a transistor: *Base bias* or *Fixed bias*, *Collector-to-Base bias*, *Voltage-divider bias*.

BASE BIAS or FIXED BIAS:

Base biasing configuration is given in the following Figure. A base resistance R_B is used between V_{CC} and base to establish the base current I_B. Since V_{CC} and R_B are fixed quantities, I_B remains fixed.



Base bias circuit using a npn transistor



Base bias circuit using a pnp transistor

Applying Kirchoff's Voltage Law (KVL) to the base circuit;

$V_{CC} - I_B R_B - V_{BE} = 0$

Or, $I_B = (V_{CC} - V_{BE})/R_B$ ---------- *(1)*

V_{BE} is 0.7 V for Silicon and 0.3 V for Germanium transistor.

Applying the KVL to the collector circuit;

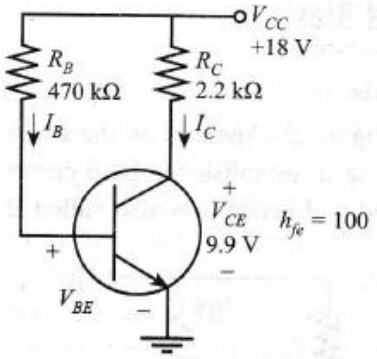
$V_{CC} - I_C R_C - V_{CE} = 0$

Or, $V_{CE} = V_{CC} - I_C R_C$ ---------- *(2)*

Note that, the voltage and current polarities are reversed in base bias circuits of npn- and pnp-transistors; but, the same KVL equations are applicable.

Example 1:

The base bias circuit is shown in Figure for the values indicated calculate I_B, I_C and V_{CE}.



Given: $R_B = 470\ \text{k}\Omega$, $R_C = 2.2\ \text{k}\Omega$, $V_{CC} = 18\ \text{V}$

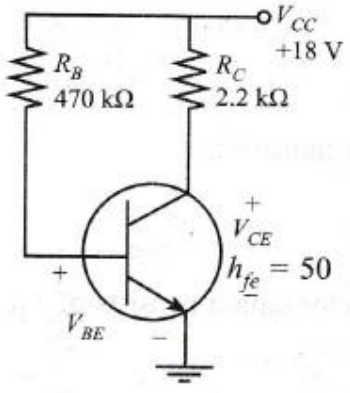
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\ \text{V} - 0.7\ \text{V}}{470\ \text{k}\Omega} = 36.8\ \mu\text{A}$$

$$I_C = h_{fe} I_B = 100 \times 36.8\ \mu\text{A} = 3.68\ \text{mA}$$

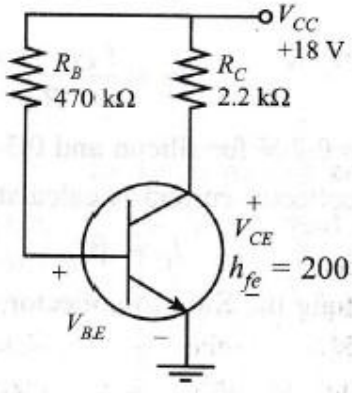
$$V_{CE} = V_{CE} - I_C R_C = 18\ \text{V} - (3.68\ \text{mA} \times 2.2\ \text{k}\Omega) = 9.9\ \text{V}$$

Example 2:

Calculate the maximum and minimum levels of I_C and V_{CE} for the base bias circuit in Figure (a), when $h_{fe(\text{min})} = 50$ and $h_{fe(\text{max})} = 200$.



(a): Conditions for $h_{fe(\text{min})}$



(b): Conditions for $h_{fe(\text{max})}$

Given: $h_{fe(\min)} = 50$, $h_{fe(\max)} = 200$,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega} = 36.8\,\mu\text{A}$$

Case i:

$$h_{fe(\max)} = 200$$

$$I_C = h_{fc} I_B = 200 \times 36.8\,\mu\text{A} = 7.36\text{ mA}$$

$$V_{CE} = V_{CE} - I_C R_C = 18\text{ V} - (7.36\text{ mA} \times 2.2\text{ k}\Omega) = 1.8\text{ V}$$

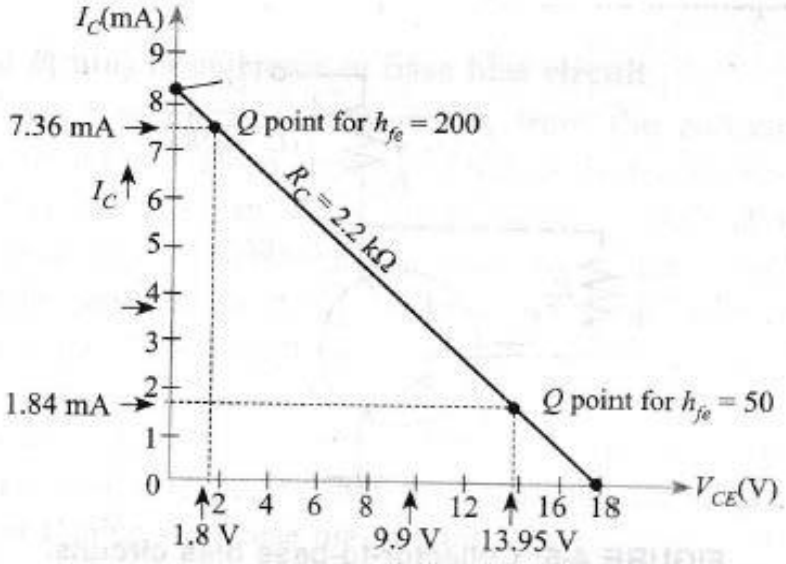
Case ii:

$$h_{fe(\min)} = 50$$

$$I_C = h_{fe} I_B = 50 \times 36.8\ \mu\text{A} = 1.84\text{ mA}$$

$$V_{CE} = V_{CE} - I_C R_C = 18 - (1.84\text{ mA} \times 2.2\text{ k}\Omega) = 13.95\text{ V}$$

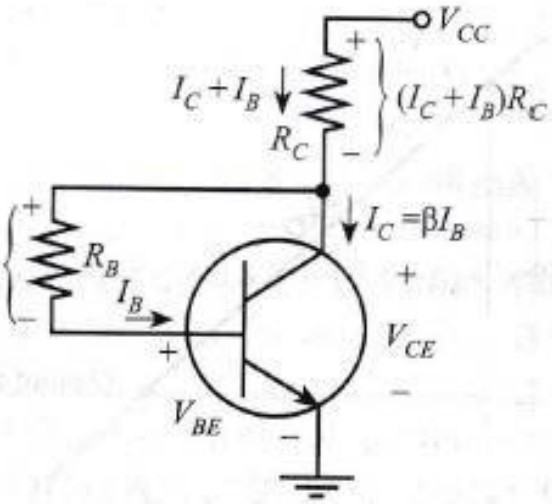
Two Q points in Figure (c) for a Transistor of a given type number always have a wide range of h_{fe} values (the h_{fe} spread). So $h_{fe(\max)}$ and $h_{fe(\min)}$ should always be used for practical circuit analysis. The base bias circuit is rarely employed because of the uncertainty of the Q point. More predictable results can be obtained with other types of bias circuit.



(c): The transistor h_{fe} value has a major effect on the Q point for a base bias circuit.

COLLECTOR-TO-BASE BIAS CIRCUIT:

The collector-to-base bias circuit shown in the following Figure, has the base resistor R_B connected between the transistor collector and base terminals. This circuit has significantly improved bias stability for h_{fe} changes compared to base bias.



Applying KVL to the outer loop;

$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$ Or, $V_{CE} = V_{CC} - (I_C + I_B) R_C$---------- *(3a)*

Applying KVL to the loop V_{CE}, I_BR_B, and V_{BE};

$V_{CE} - V_{BE} - I_BR_B = 0$ Or, $V_{CE} = V_{BE} + I_BR_B$---------- *(3b)*

Equating equations 3a and 3b;

$V_{CC} - (I_C + I_B) R_C = V_{BE} + I_BR_B$

Or, $(I_C + I_B) R_C + I_BR_B = V_{CC} - V_{BE}$ i.e., $I_B (R_C + R_B) + I_CR_C = V_{CC} - V_{BE}$

Substituting $I_C = \beta I_B$ in above equation, we get;

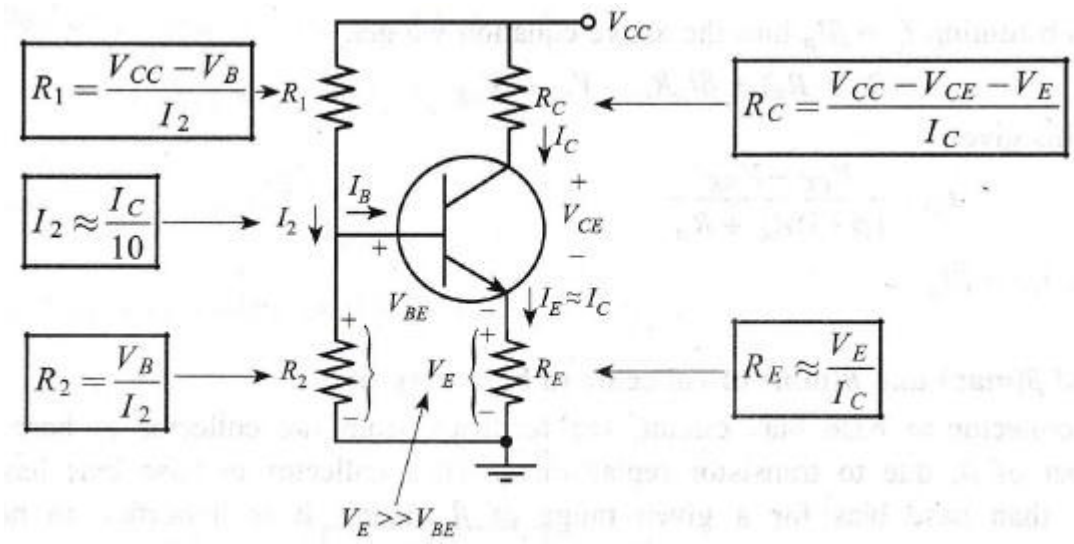
$I_B (R_C + R_B) + \beta I_BR_C = V_{CC} - V_{BE}$ Gives, $I_B = (V_{CC} - V_{BE})/(\beta+1)R_C + R_B$---------- *(4)*

Effect of I_C or ß: Any changes in V_{CE} changes I_B, the change in I_B causes I_C to change. If I_C increases above the design level, there is an increased voltage drop across R_C; resulting in reduction of V_{CE}. The reduced V_{CE} causes I_B to be lower. If I_B decreases, I_C also decreases, as $I_C = \beta I_B$. Similarly, a reduction in I_C produces an increase in V_{CE}, which increase I_B, thus tending to increase I_C back to the original level. Thus an increase/ decrease in I_C produces a feedback effect that tends to return I_C toward its original level.

In the collector-to-base bias circuit, the feedback from the collector-to-base reduces the effect of β (due to transistor replacement). Thus collector-to-base bias has greater stability than base bias, for a given range of β values.

VOLTAGE DIVIDER (EMITTER CURRENT) BIAS CIRCUIT:

Voltage divider bias is the most stable of the three basic transistor biasing circuits. A voltage divider circuit is shown in the following Figure.



There is an emitter resistor R_E connected in series with Emitter terminal, so that the total dc load in series with the transistor is ($R_C + R_E$). Resistors R_1 and R_2 constitutes a voltage V_B.

Applying KVL to the loop V_{CC}, R_1, and R_2, we get;

$V_{CC} - I_1R_1 - I_2R_2 = 0$ Or, $I_1R_1 + I_2R_2 = V_{CC}$ ----------(5)

We have; $I_1 = I_2 + I_B$

Voltage divider bias circuits are normally designed to have a voltage divider current I_2 very much greater than transistor base current I_B. i.e., $I_2 >> I_B$. Hence, $I_1 \approx I_2$ ---------- (6)

Using 6 in 5; $I_2R_1 + I_2R_2 = V_{CC}$ *i.e.,* $I_2 (R_1 + R_2) = V_{CC}$ Or, $\boldsymbol{I_2 = (V_{CC}) / (R_1 + R_2)}$

V_B is the voltage across R_2. i.e., $V_B = I_2R_2$ Or, $\boldsymbol{V_B = (V_{CC} * R_2) / (R_1 + R_2)}$

V_E is the voltage across R_E. i.e., $\boldsymbol{V_E = I_ER_E}$

Applying KVL to the base-emitter loop; $V_B - V_{BE} - V_E = 0$ i.e., $\mathbf{V_{BE} = V_B - V_E}$

Or, $V_E = V_B - V_{BE}$ i.e., $I_ER_E = V_B - V_{BE}$ Hence, $\boldsymbol{I_E = (V_B - V_{BE}) / R_E}$

Applying KVL to the collector-emitter loop; $V_{CC} - I_CR_C - V_{CE} - I_CR_E = 0$ $[I_E \approx I_C]$

i.e., $\boldsymbol{V_{CE} = V_{CC} - I_C (R_C + R_E)}$

ANALOG AND DIGITAL ELECTRONICS

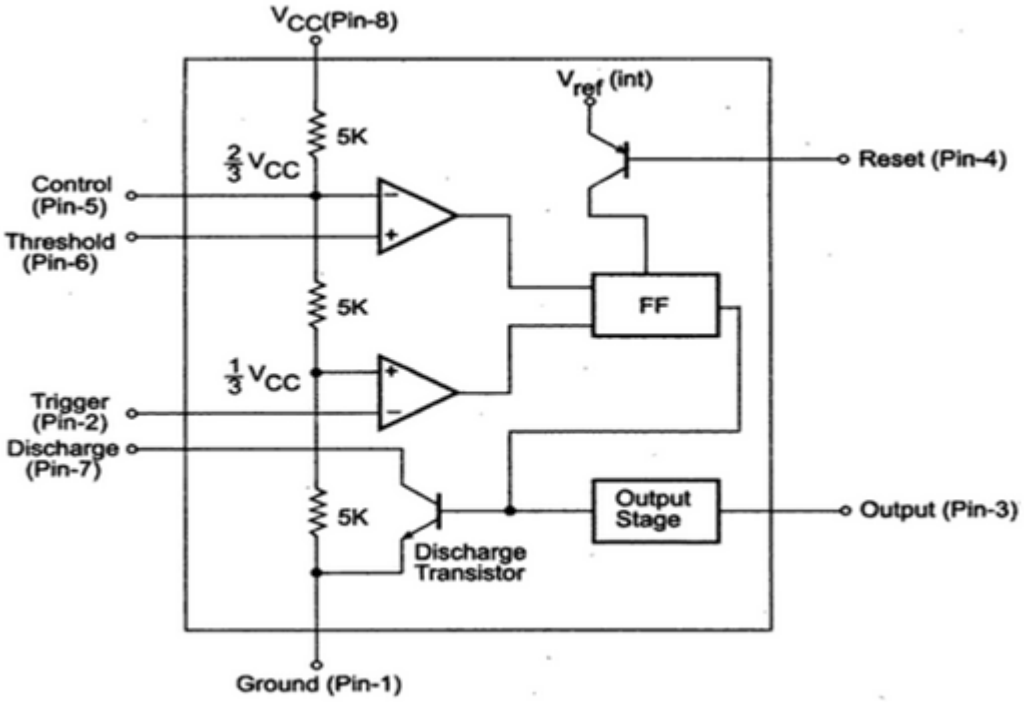
MULTIVIBRATORS USING IC-555

A multivibrator (like an oscillator) is a circuit with regenerative feedback, which produces a pulsed output. There are three basic types of multivibrator circuits:

- *Astable* – has no stable states, but switches continuously between two states. This action produces a train of square wave pulses at a fixed frequency.
- *Monostable* – one of the states is stable, but the other state is unstable (transient).
- *Bistable* – the circuit is stable in either state.

Timer IC-555:

Timer IC-555 is the one of the most commonly used general-purpose linear integrated circuits.

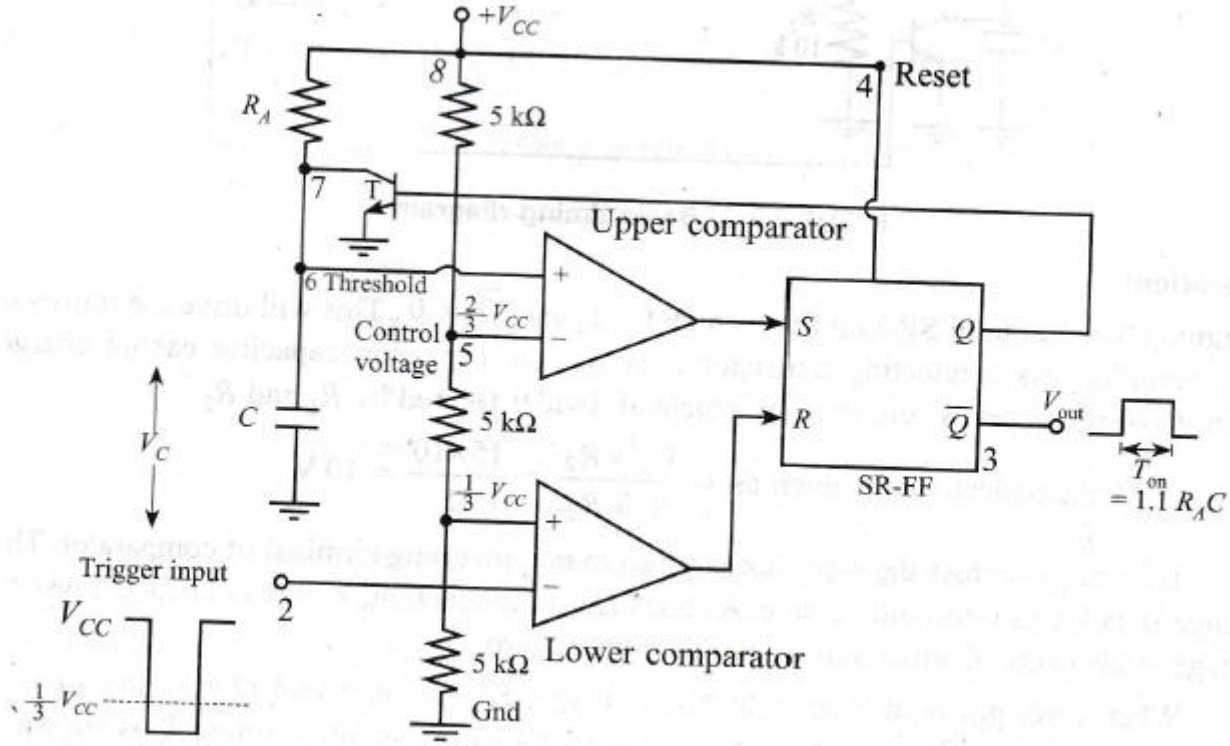


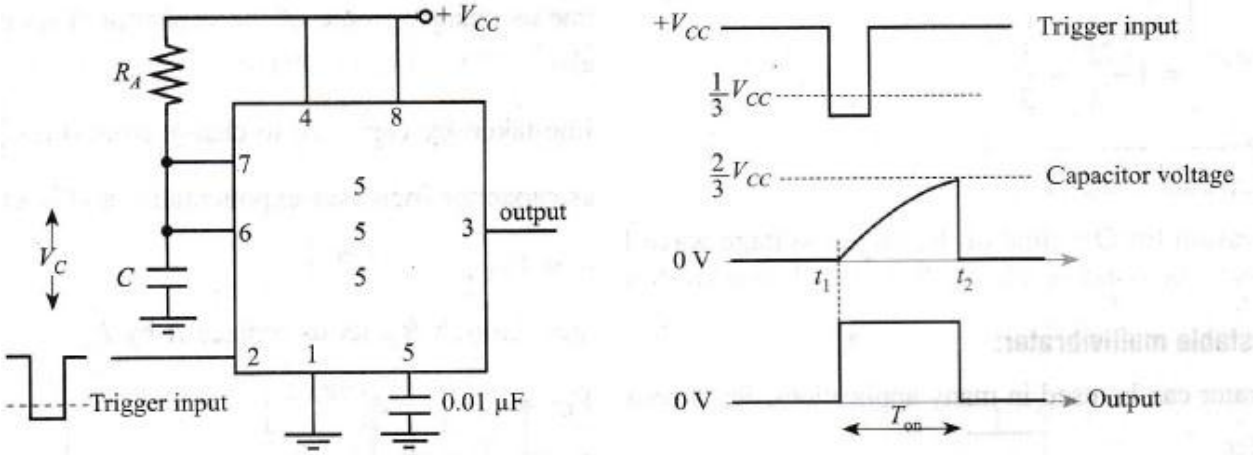
Internal Schematic of Timer IC-555

The Timer IC 555 comprises two Op-Amp comparators, a flip-flop, a discharge transistor, a reset transistor, three identical resistors and an output stage. The resistors set the reference voltage levels at the non-inverting input of the lower comparator and inverting input of the upper comparator at $+V_{CC}/3$ and $2V_{CC}/3$, respectively. The output of two comparator feed SET and RESET inputs of the Flip-Flop. This decided the logic state of its output and subsequently the final output. The Flip-Flops complementary outputs feed the output stage and the base of the discharge transistor. Hence, when the output is HIGH, the discharge transistor is OFF and when the output is LOW, the discharge transistor is ON.

MONOSTABLE MULTIVIBRATOR:

Monostable multivibrator using 555 timer IC is as shown in the following Figure. This 555 timer is called monostable multivibrator because it has only one stable state. Resistor R_A and capacitor C are components connected externally to the IC-555. Threshold voltage (6) and discharge (7) pins are connected to each other.





- Initially the SR-FF is set ($Q = 1$); transistor T is driven into saturation, and the capacitor is by passed by the transistor. Therefore, the capacitor voltage $V_C = 0$, and also the output voltage $Vout = 0$ (as $Q = 1$).

- When the negative going trigger pulse (which should be more than *1/3* V_{CC}) is applied at trigger input of lower comparator, the comparator output goes high; and SR-FF is reset ($Q = 0$), forcing $\bar{Q}$ to go high and transistor *T* turns off.
- As *T* is off, capacitor starts charging through R_A. Now, the output will remain high (from t_1 to t_2, in waveform shown).
- At time t_2; the voltage across the capacitor V_{CC} becomes more than *2/3* V_{CC} and upper comparator output goes high. This will set the SR-FF ($Q = 1$).
- Since, SR-FF output Q = 1; transistor T is ON, and hence, capacitor discharges, and also output goes low. The output remains low till the next trigger pulse is applied.

From the waveform of monostable multivibrator, it is clear that, the ON time T_{ON} of the output voltage is same as charging time of the capacitor.

Therefore, T_{ON} → is the time taken by capacitor to charge from 0 to *2/3* V_{CC}.

The voltage across capacitor increases exponentially and is given by; $V_C = V_{CC}[1 - e^{-t/RC}]$

As capacitor charges through R_A; let us replace *R* by R_A: Hence, $V_C = V_{CC}[1 - e^{-t/R_A C}]$

At $t = t_2$ (T_{ON}), the capacitor voltage (V_C) reaches *2/3* V_{CC}:

Therefore, $\frac{2}{3}V_{CC} = V_{CC}[1 - e^{-T/R_A C}]$ Or, $e^{-T/R_A C} = 1 - 2/3 = 1/3$

Therefore, $\boldsymbol{T_{ON} = 1.1\, R_A C}$

Applications:

A monostable multivibrator can be used in many applications, few important applications are

1. Frequency divider
2. Missing pulse detector
3. Pulse width modulator
4. Pulse position modulator etc.

Example 1:

For a monostable muitivibrator time delay $T = 100$ ms and resistance $R = 105$ kΩ. Calculate the capacitor value.

Given: $T = 100$ ms, $R = 105$ kΩ

We knew that the pulse width *W* is given by

$$W = 1.1RC = T_{on}\,(\text{time delay})$$

$$C = \frac{T_{on}}{1.1R} = \frac{100\text{ ms}}{1.1\times 105\text{ k}}$$

$$\boxed{C = 0.865\,\mu\text{F}}$$

Example 2:

Design a monostable multivibrator circuit using 555 timer to produce an output pulse of 20sec width.

The output pulse [T_{on}] is given as

$$T_{on} = 20 \text{ sec}$$

WKT $T_{on} = 1.1RC$ Assuming $C = 150\ \mu F$

$$20 = 1.1\ R \times 150\ \mu F$$

$$R = \frac{20}{1.1\times150\times10^{-6}} = 121.21\,k\Omega$$

$$\boxed{R = 121.21\,k\Omega}$$

Example 3:

Find the resistive element value to generate $T = 10$ ms time delay, using 555 timer as a monostable multivibrator Assume $C = 0.47\ \mu F$.

The on period of pulse is given by

$$T_{on} = 1.1RC$$

$$10 \times 10^{-3} = 1.1 \times R \times 0.47 \times 10^{-6}$$

$$R = \frac{10\times10^{-3}}{1.1\times0.47\times10^{-6}} = 19.34\,k\Omega$$

$\boxed{R = 19.34\,k\Omega}$ We can choose standard value as 18 kΩ.

Example 4:

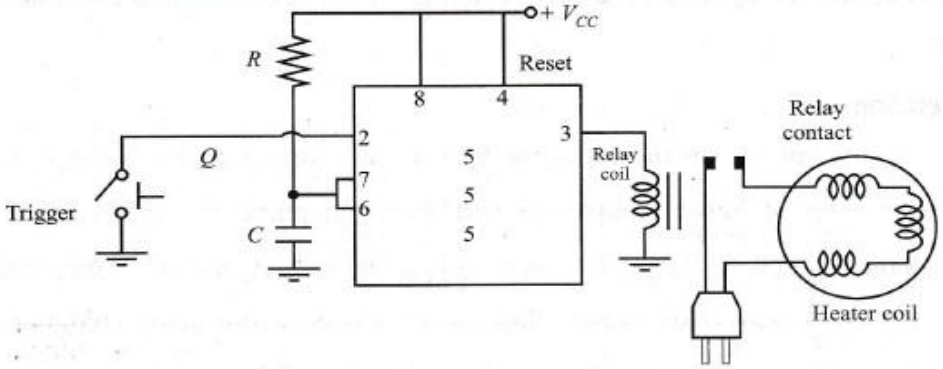
Design a timer that can turn on a heater immediately after pressing the button, and it should hold the heater in on-state for 10 seconds.

The relay coil should be energized for 10 seconds to hold heater on so T_{on} is 10 seconds and choosing $C = 47\ \mu F$.

WKT $T_{on} = 1.1RC$

$10 = 1.1RC$

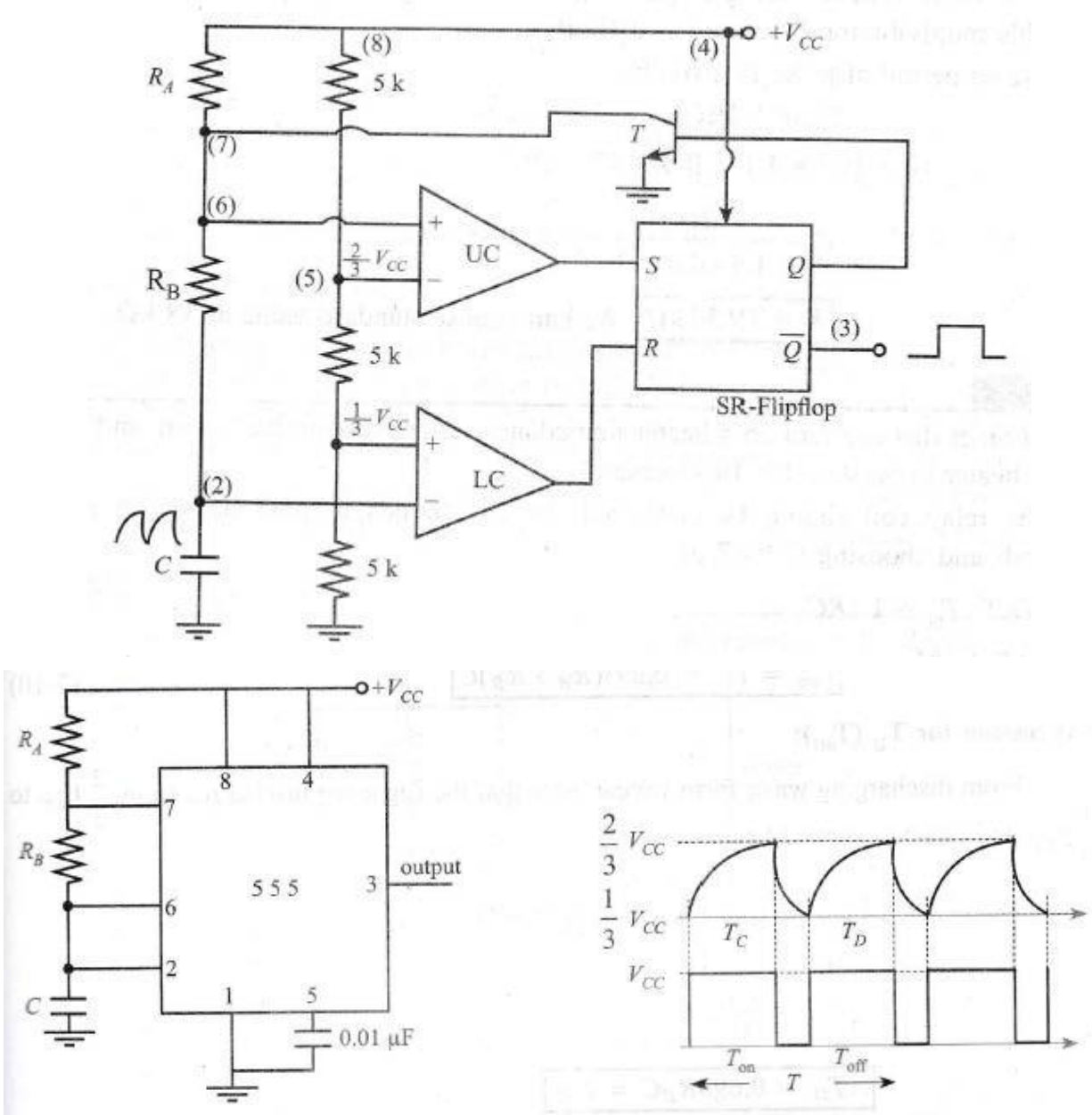
$$\boxed{R = \frac{10}{1.1\times47\times10^{-6}} = 193.42\,k\Omega}$$



Monostable multivibrator used to turn–on relay

ASTABLE MULTIVIBRATOR:

An *astable multivibrator* does not have any stable state; it keeps changing its state from low to high and high to low. This multivibrator is also called *free running multivibrator* or *rectangular wave generator* circuit. *Astable multivibrator* does not require an external trigger pulse to change the state of the output. The circuit configuration of an astable rnultivibrator is as shown in the following Figure.



To understand the operation, let us divide the circuit operation into two time interval T_{ON} and T_{OFF}.

ON time operation:

- At $t = 0$, the voltage on the capacitor $V_{CC} = 0$, the same capacitor voltage is applied to both trigger point of lower comparator and threshold point of upper comparator. As capacitor voltage $V_C = 0$, which is less $1/3\ V_{CC}$, the output of lower comparator goes high ($QQ\text{-}= 1$) and $Q = 0$. This

causes T to go off and capacitor starts charging through series resistors R_A and R_B. When capacitor voltages reaches *2/3* V_{CC}, on time is terminated.

OFF time operation:

- As soon as V_C exceeds *2/3* V_{CC}, the upper comparator output goes high and it will set the SR FF. i.e., $S = 1$ and $R = 0$ and $Q = 1$ and $QQ\text{\textregistered} = 0$. This will turn on transistor T, and output at pin (3) goes low.
- Now, the capacitor discharges through R_B, and through transistor T. The discharge time (also called off time (T_D); and it depends on the values of R_B and C. When capacitor voltage is $V_C = 1/3$ V_{CC}, lower comparator output goes high.
- This process of charging and discharging is continuous and hence circuit oscillates. The schematic diagram and waveforms are as shown in the Above Figure.

The output voltage waveform is the sum of charging and discharging periods (T_C, and T_D) of the capacitor.

.'. Period of one cycle $T = T_C + T_D$.

Frequency can be written as $ff = \frac{1}{TT} = \frac{1}{TT_{CC} + TT_{DD}}$

Voltage across charging capacitor is given by (initial voltage on capacitor is zero);

$$VV_{CC} = VV_{CCCC}[1 - ee^{\frac{-W}{RRCC}}]$$

If there is some initial voltage present, the voltage expression for capacitor changes, and is given by;

$$W_{CC} = W_{FF} + (W_{ii} - W_{FF})ee^{\frac{-W}{RRCC}}$$

Where V_F - final voltage capacitor can reach, and V_i - is Initial voltage on capacitor.

During charging time T_C, the initial voltage on the capacitor is $V_i = 1/3$ V_{CC}, and the final voltage is $V_F = V_{CC}$. Also as charging takes place through both R_A and R_B, the above expression becomes;

$$\frac{2VV_{CC}}{3} = VV_{CCCC} + (\frac{1}{3}W_{CCCC} - W_{CCCC})ee^{-\frac{TT_{CC}}{\text{\textregistered}R_{AA}+RR_{BB}\text{\textregistered}C}}$$

$$\frac{1}{3}VV_{CCCC} = (\frac{2}{3}W_{CCCC})ee^{-\frac{TT_{CC}}{\text{\textregistered}R_{AA}+RR_{BB}\text{\textregistered}C}}$$

Therefore, $\boldsymbol{T_{ON} = T_C = 0.693\ (R_A + R_B)\ C}$

From discharging waveform; we can note that, the capacitor discharges from *2/3* V_{CC} to *1/3* V_{CC}; and can be expressed as:

$$\frac{1}{3}VV_{CCCC} = 0 + (\frac{2}{3}W_{CCCC} - 0)ee^{-\frac{TT_{DD}}{RR_{BB}\text{\textregistered}C}}$$

Or, $$\frac{1}{3}VV_{CCCC} = (\frac{2}{3}W_{CCCC})ee^{-\frac{TT_{DD}}{RR_{BB}CC}}$$

Therefore, $\boldsymbol{T_{OFF} = T_D = 0.693\ R_B\ C}$

Hence, Total period, $T = T_{ON} + T_{OFF} = 0.693\,(R_A + 2R_B)\,C$

Frequency, $ff = \frac{11}{TT} = \frac{11.4444}{(RR_{AA}+22RR_{BB})CC}$

Duty Cycle, %D = [(on time) / (total time)]*100

$$\%\,DD = \frac{(RR_{AA}+RR_{BB})}{(RR_{AA}+22RR_{BB})} * 111111$$

Applications:

A nastable multivibrator can be used in many applications, few important applications are

1. Square-wave oscillator/ generator
2. Schmitt trigger using IC-555
3. Voltage controlled oscillator.

Example 1:

For an astable circuit $R_1 = 22\ k\Omega$, $R_2 = 30\ k\Omega$ and $C = 0.5\ \mu F$ Find on and off period of the output wave form shown in Figure 7-17.

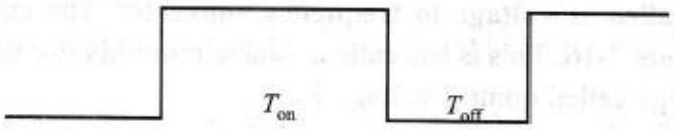


FIGURE 7-17

The on period corresponds to charging period of a capacitor and charging takes place through resistors R_1 and R_2.

$$\therefore T_C = T_{on} = 0.693(R_1 + R_2)C$$

$$= 0.693(22+30)\times10^3\times0.5\times10^{-6}$$

$$\boxed{T_{on} = 18\ \text{msec}}$$

The off period corresponds to discharging time (T_D) of the capacitor and discharging taken place through R_2 only.

$$\therefore T_D = T_{off} = 0.693R_2C$$

$$= 0.693\times30\times10^3\times0.5\times10^{-6}$$

$$\boxed{T_{off} = 10.395\ \text{msec}}$$

Example 2:

A 555 timer is configured to operate in astable mode with R_A = 5 kΩ, R_B = 5 kΩ and C = 0.01 μF, Determine the frequency of the output and duty cycle.

Given: R_A = 5 kΩ, R_B = 5 kΩ, C = 0.01 μF

Frequency of oscillation for astable multivibrator is given by

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} = \frac{1.45}{(5\,\text{k} + 2(5\,\text{k}))0.01\,\mu\text{F}}$$

$$= \frac{1.45}{5\times10^3 + 2(5\times10^3)\times0.01\times10^{-6}}$$

$$\boxed{f = 10.357\,\text{kHz}}$$

and Duty cycle $D = \frac{R_A + R_B}{R_A + 2R_B} = \frac{5\times10^3 + 5\times10^3}{5\times10^3 + 2(5\times10^3)}$

$$D = \frac{10\times10^3}{15\times10^3} = 66.66\%$$

$$\boxed{D = 66.66\%}$$

Example 3:

Design an astable multivibrator using 555 timer for a frequency of 2 kHz and a duty cycle of 75% Assume C_1 = 0.1 μF.

Given: f = 2 KHz, duty cycle = 75%, C = 0.1 μF

The on period $T_{on} = 0.693\,(R_A + R_B)\,C$.

The off period $T_{off} = 0.693 R_B\,C$

Total period $T = T_{on} + T_{off} = 0.693(R_A + R_B)\,C$

∴ Duty cycle D is given by

$$D = \frac{T_{on}}{T_{on} + T_{off}} = \frac{T_{on}}{T} = \frac{0.693\,(R_A + R_B)C}{0.693\,(R_A + 2R_B)C}$$

$$D = \frac{R_A + R_B}{R_A + 2R_B} = \frac{3}{4} = 0.75$$

$$\therefore 3\,(R_A + 2\,R_B) = 4\,(R_A + R_B)$$

$$3R_A + 6R_B = 4\,R_A + 4R_A + 4R_B$$

$$2R_B = R_A \qquad \text{Or,} \quad R_B = \tfrac{1}{2}R_A$$

Substituting for R_B in expression for T

$$\therefore T = 0.693(R_A + R_B)C$$

$$T = 0.693\left(R_A + \frac{1}{2}R_A\right)\times0.1\times10^{-6}$$

$$T = 0.693\left(\frac{3}{2}R_A\right)\times0.1\times10^{-6}$$

$$\boxed{f = \frac{1}{T}}$$

$$1\times10^3 = f = \frac{1}{T} = \frac{1}{0.693(1.5R_A)\times0.1\times10^{-6}}$$

$$R_A = \frac{1}{0.693(1.5)0.1\times10^{-6}\times10^3}$$

$$\boxed{R_A = 9.6\,\text{k}\Omega}$$

$$R_B = \frac{1}{2}R_A$$

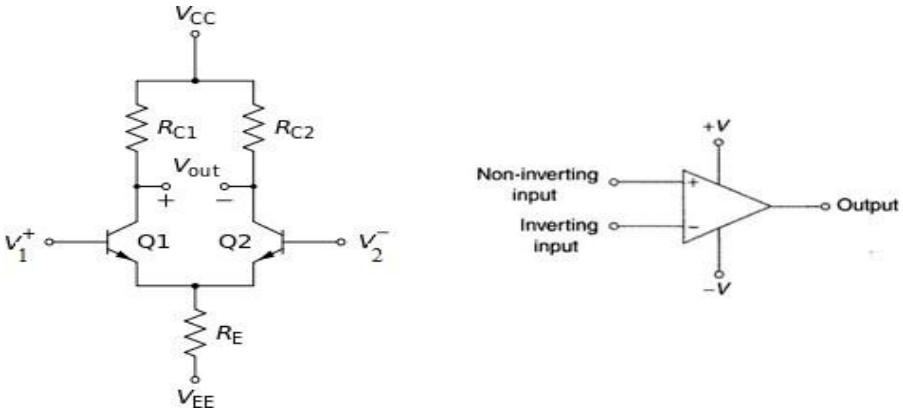
$$= \frac{1}{2}\times9.6\times10^3$$

$$\boxed{R_B = 4.8\,\text{k}\Omega}$$

ANALOG AND DIGITAL ELECTRONICS

OPERATIONAL AMPLIFIER (OP-AMP) APPLIATION CIRCUITS

An **Op-Amp** is a direct-coupled high gain, high bandwidth differential amplifier with very high value of input impedance and very low value of output impedance.



Basic Differential Amplifier & Circuit Representation of an OP-Amp

The ideal Op-Amp model was derived to simplify circuit calculations. The ideal Op-Amp model makes three assumptions:

1. Input resistance (impedance), $R_i = \infty$
2. Output resistance (impedance), $R_o = 0$
3. Open-loop (differential voltage) gain, $A_d = \infty$

Ideal Op-Amp	Practical Op-Amp
Internal Impedance is infinite	Input Impedance range 100KΩ to 1000MΩ
Output Impendence is zero	Output impedance range from 10Ω to 100Ω
Open loop differential voltage gain is infinite	Open loop gain is in the range of 10,000 to 100,000
Bandwidth is infinite	Bandwidth is limited
DC input and output offset voltage is zero	Finite DC input and output offset voltage
Input differential voltage is zero	Finite differential voltage is finite

Based on these three assumptions,

other assumptions can be derived:

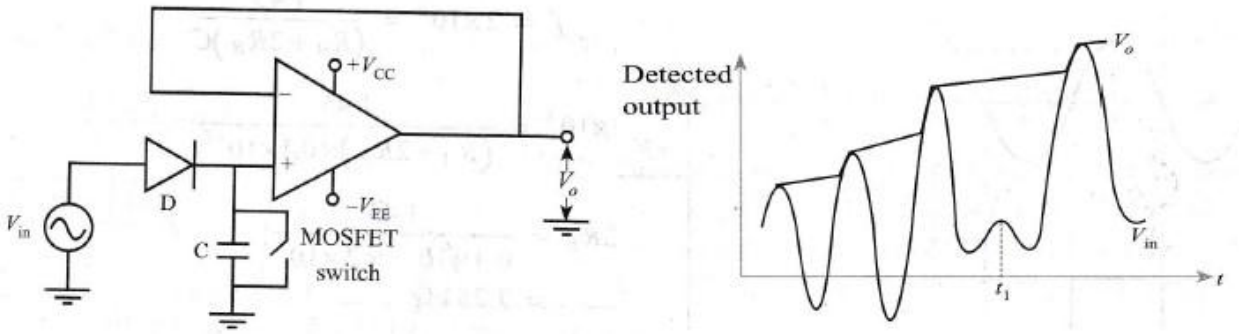
1. Since $R_i = \infty$, $I_i = I_{ni} = 0$
2. Since $R_o = 0$, $V_o = A_d * V_d$
3. Zero DC input and output offset voltages
4. Bandwidth and slew rate are also infinite, as no frequency dependencies are assumed.
5. Drift is also zero, as there is no changes in performance over time, temperature, power supply variations, and so on
6. Since output voltage depends only on differential input voltage, it rejects any voltage common to both inputs. Hence, common mode gain = 0

Open-loop gain is the differential voltage gain in the absence of any positive or negative feedback. Practical Op-Amps have –

1. Input impedance can vary from hundred of kilo-ohms (for some low-grade Op-Amps) to tera-ohms (for high grade Op-Amps).
2. Output impedance may be in the range of 10 to 100 Ω
3. Open-loop gain in the range of 10,000 to 1, 00,000
4. Bandwidth is limited and is specified by gain-bandwidth product
5. There may be some finite DC output (referred to as output offset voltage), even when both the inputs are grounded.

PEAK DETECTORS:

Peak detector detects holds the most positive value attained by the input signal. The following Figure shows peak detector circuit.

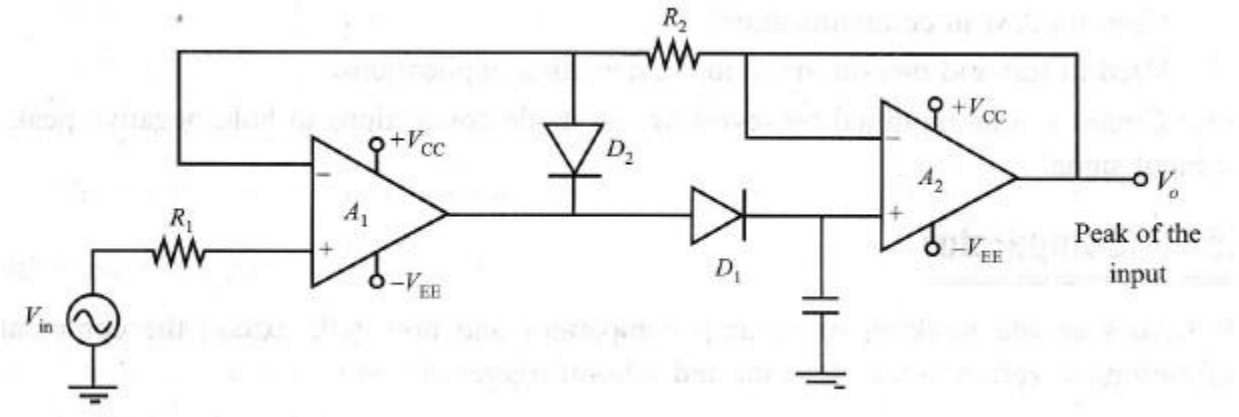


During positive half cycle of the input, D-conducts and capacitor charges to peak (highest) value of the input. Capacitor retains its charged value unless and until it discharges with a help of switch.

The op-amp is connected as a voltage follower and its output voltage will be equal the drop across capacitor which is positive peak value of the applied voltage and will remain that for long periods until next more higher peak occurs at the input. For negative cycle of input, the diode is reverse biased and capacitor retains its value.

Modified Peak Detector:

More sophisticated peak detector that buffers the signal source from the capacitor is shown in the following Figure.



As Op-Amp (A_1) is connected as voltage follower, the circuit presents very high impedance to the signal source. Op-Amp (A_2) acts as a buffer between the capacitor and the load. Output (V_0) at any given time is equal to the voltage on the capacitor which is nothing but, the peak value of the input occurred up to that time.

Whenever the input signal has higher peak than the present one, the capacitor charges up to new high input level. Whenever input level gets dropped, then capacitor retains the peak value of input, as

diode D_1 gets reverse biased and diode D_2 prevents amplifier A_1 output from going into negative saturation.

To hold the negative peak of the input signal, reverse the diode connections in the above Figure.

Applications:

- Used for AM in communication
- Used in test and measurement instrumentation applications.

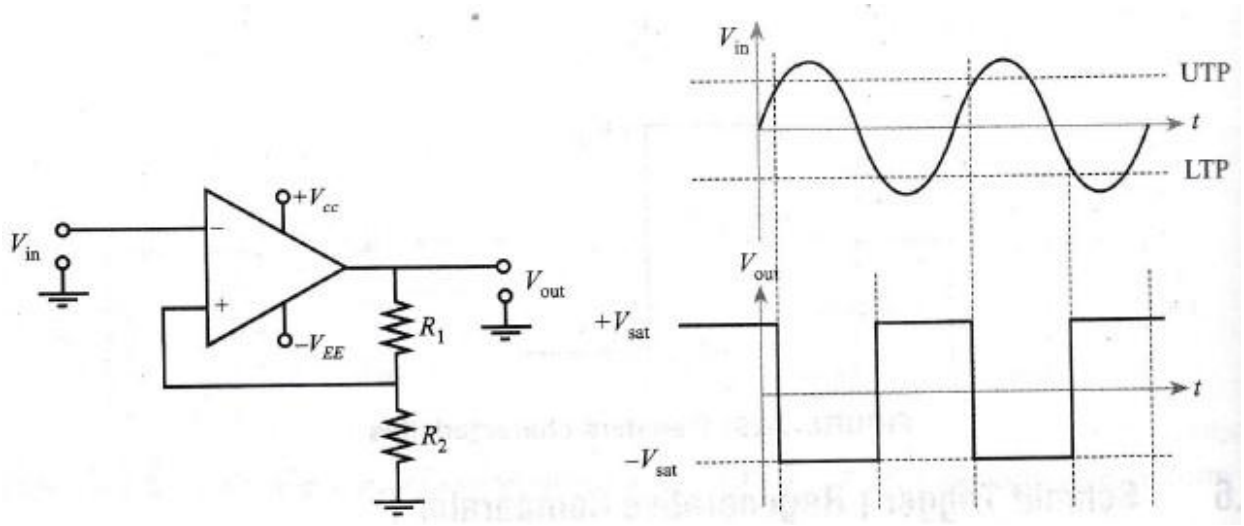
SCHMITT TRIGGER (REGENERATIVE) COMPARATOR:

A Schmitt trigger is a fast-operating voltage level detector.

Inverting Schmitt Trigger:

The input voltage V_{in} is applied to the inverting input terminal and the feedback voltage goes to the non-inverting terminal. This means, the circuit uses positive voltage feedback (i.e., feedback voltage aids the input voltage).

If the input voltage at the inverting terminal is slightly positive than feedback voltage at the non-inverting terminal, the output voltage will be negative (negative saturation, $-V_{sat}$); and if the input voltage more negative than the reference feedback voltage, the output will be positive (positive saturation, $+V_{sat}$).



Hence, the voltage at the output switches from $+V_{sat}$ to $-V_{sat}$ or vice-versa; are called *Upper Trigger Point (UTP)* and *Lower Trigger Point (LTP)*. The difference between two trigger points is called *Hysteresis*.

The upper and lower trigger points can be written as;

$$UUTTUU = \frac{RR_2}{(RR_1+RR_2)} VV_{sssVV} \qquad LLTTUU = \frac{RR_2}{(RR_1+RR_2)} (-VV_{sssVV})$$

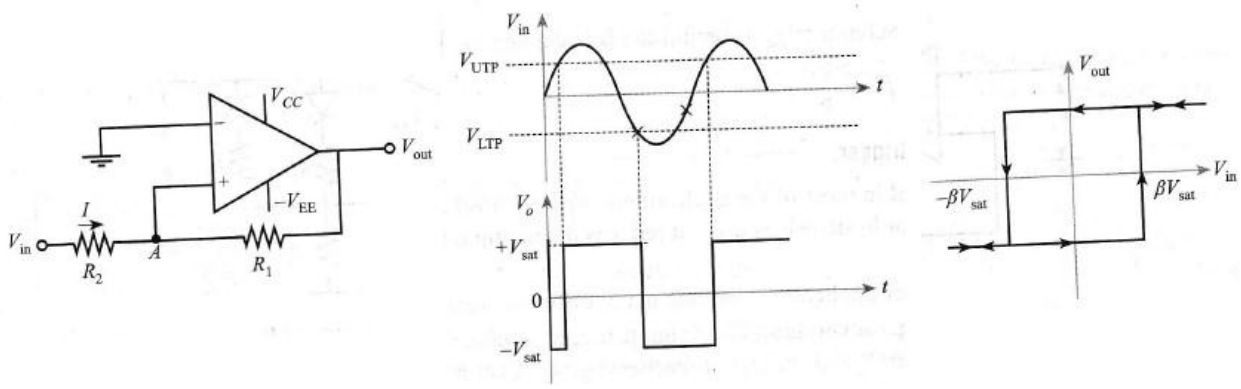
$$VV_{hyyss} = UUTTUU - LLTTUU = \frac{RR_2}{(RR_1+RR_2)} VV_{sssVV} - \frac{RR_2}{(RR_1+RR_2)} (-VV_{sssVV}) = 2\left(\frac{RR2}{RR_1+RR_2}\right) VV_{sssVV} = 2\beta\beta VV_{sssVV}$$

$$\beta\beta = \frac{RR2}{RR_1+RR_2}$$

Non-Inverting Schmitt Trigger:

The input voltage V_{in} is applied to the non-inverting input terminal and the feedback voltage also goes to the non-inverting terminal. The inverting terminal is grounded..

Initially, assume that the output is in the negative saturation ($-V_{sat}$). Then the feedback voltage is also negative. This feedback voltage will hold the output in negative saturation, until the input voltage becomes positive enough to make voltage positive.



Let V_A is the voltage at point A. Hence, $V_A = IR_2$.

Since no current passes through the Op-Amp, entire current flows through R_1.

$$\text{Therefore, } II = \frac{VV_0}{RR_1} = \frac{+VV_{ssssVV}}{RR_1}$$

When V_{in} becomes positive and its magnitude becomes greater than $(R_2/R_1)V_{sat}$, then the output switches to $+V_{sat}$. Therefore, the UTP at which the output switches to $+V_{sat}$ is given by;

$$UUTTUU = \frac{RR_2W_{ssssVV}}{RR_1}$$

Similarly, when V_{in} becomes negative and its magnitude becomes greater than $(R_2/R_1)V_{sat}$, then the output switches to $-V_{sat}$. Therefore, the LTP at which the output switches to $-V_{sat}$ is given by;

$$LLTTUU = -\frac{RR_2W_{ssssVV}}{RR_1}$$

$$W_{hyyss} = UUTTUU - LLTTUU = 2\frac{RR2}{RR_1}W_{ssssVV} = 2\beta\beta W_{ssssVV}$$

$$\beta\beta = \frac{RR2}{RR_1}$$

Applications of Schmitt Trigger:

Schmitt trigger is used in many applications, where level needs to be sensed. Hysteresis is used to reduce the multiple transitions that can occur around.

- Digital to analog conversion
- Level detection
- Line reception.

Example 2:

Design a Schmitt trigger whose threshold voltages are ± 5 V. Draw its wave forms.

Choosing op-amp with $V_{sat} = \pm 13.5$ V with supply ± 15 V.

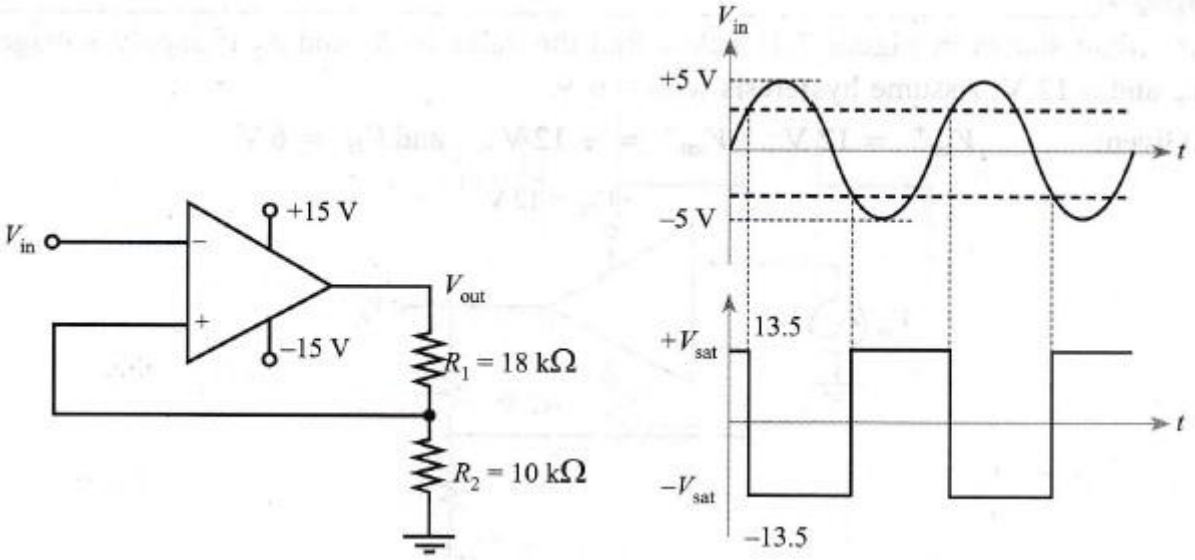
$$V_{UTP} = +5\text{ V}$$

$$\text{Now } V_{UTP} = \frac{R_2}{R_1 + R_2}.V_{sat} \quad \text{i.e., } 5 = \frac{R_2}{R_1 + R_2} \times 13.5$$

$$\therefore R_1 + R_2 = 2.7\,R_2 \quad \text{i.e. } R_1 = 1.7\,R_2$$

$$\text{Choose } R_2 = 10\,\text{k}\Omega \quad \therefore R_1 = 17\text{k}\Omega\,(\text{Use } 18\,\text{k}\Omega)$$

The designed circuit with waveform are shown below.



Example 3:

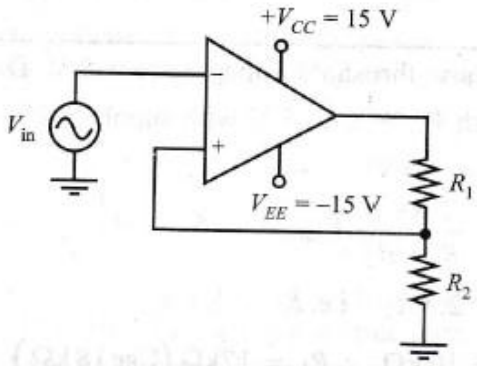
For the circuit shown, $R_2 = 120\ \Omega$ and $R_1 = 51\ \text{k}\Omega$ Determine the threshold voltages, if power supply applied to the op-amps are +15 V and −15 V.

Given

$$V_{sat}^{+} = +V_{CC} = +15\text{ V}.$$

$$V_{sat}^{-} = -V_{EE} = -15\text{ V}.$$

$$R_1 = 51\,\text{k}\Omega,\ R_2 = 120\,\Omega$$



WKT

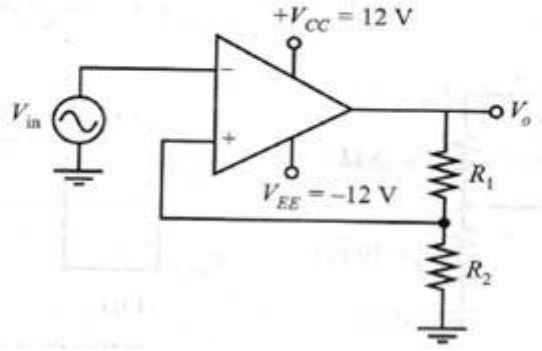
$$V_{UTP} = \frac{V_{sat}^{+}\,R_2}{R_1 + R_2} = \frac{15 \times 120}{51 \times 10^3 + 120} = 35.2\text{ mV}.$$

$$V_{LTP} = \frac{V_{sat}^{-}\,R_2}{R_1 + R_2} = \frac{-15 \times 120}{51 \times 10^3 + 120} = -35.2\text{ mV}$$

Example 4:

For the circuit shown in Figure below find the value of R_1 and R_2 if supply voltages are +12 and – 12 V. Assume hysteresis with = 6 V.

Given: $V_{sat}^{+} = 12\,V$; $V_{sat}^{-} = -12\,V$; and $V_H = 6\,V$



Hysteresis is given by

$$V_H = \frac{R_2 V_{sat}^{+}}{R_1 + R_2} - \frac{R_2 V_{sat}^{-}}{R_1 + R_2} = \frac{R_2}{R_1 + R_2}\left[V_{sat}^{+} - V_{sat}^{-}\right]$$

$$\therefore \frac{R_2}{R_1 + R_2} = \frac{V_H}{\left[V_{sat}^{+} - V_{sat}^{-}\right]}$$

$$\therefore \frac{R_2}{R_1 + R_2} = \frac{6}{12 - [-12]} \qquad \therefore \frac{R_2}{R_1 + R_2} = 0.25$$

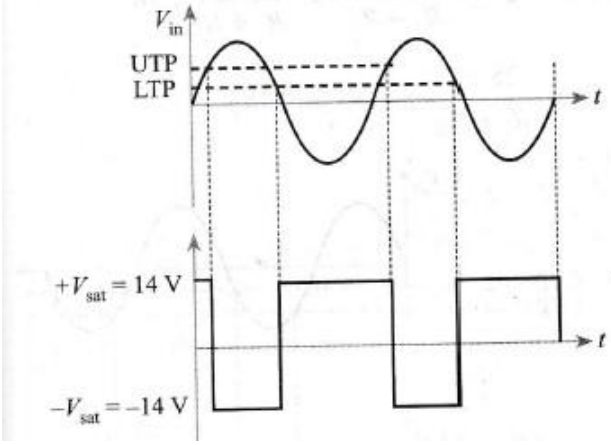
$$\therefore R_2 = 0.25\,R_1 + 0.25\,R_2 \qquad \therefore 0.75\,R_2 = 0.25\,R_1$$

$$\frac{R_2}{R_1} = \frac{0.25}{0.75} \qquad \text{Assuming } \boxed{\begin{array}{l} R_2 = 10\,k\Omega \\ R_1 = 30\,k\Omega \end{array}}$$

Example 5:

Design Schmitt trigger circuit with UTP = 4 and LTP = 2 V [both positive] Assume V_{sat} = 14 V.

Given: $V_{sat} = 14\,V$, UTP = 4 and LTP = 2 V.



WKT

$$V_{UTP} = \frac{R_2}{R_1 + R_2}.V_{sat}$$

$$V_{LTP} = \frac{R_2}{R_1 + R_2}.V_{sat}^{(-)}$$

$$V_H = V_{UTP} - V_{LTP} = 2.V_{sat}.\frac{R_2}{R_1 + R_2}$$

$$= 4 - 2 = 2 \times 14 \times \frac{R_2}{R_1 + R_2}$$

$$2 = 28\frac{R_2}{R_1+R_2} \qquad 28R_2 = 2R_1+2R_2 \qquad 26R_2 = 2R_1 \qquad \text{i.e., } \boxed{R_1 = 13R_2}$$

Let $\boxed{R_2 = 10\,\text{k}\Omega}$ $\qquad R_1 = 13\times10\,\text{k} = 130\,\text{k}\Omega$

Example 6:

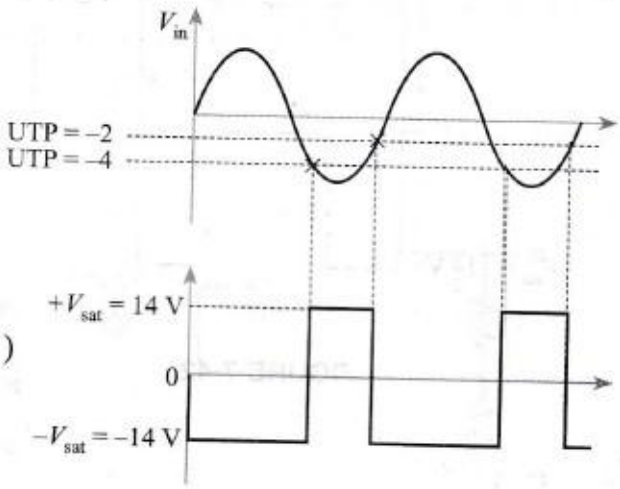
Design schmitt trigger circuit with UTP = – 2 and LTP = – 4 V. V_{sat} = 14 V.

We have, $\text{UTP} - \text{LTP} = \dfrac{2R_2}{R_1+R_2}V_{sat}$

$$-2+4 = 2 = \frac{2R_2V_{sat}}{R_1+R_2} = \frac{2R_2}{R_1+R_2}\times14$$

$$2 = \frac{28R_2}{R_1+R_2} \Rightarrow R_1 = 13R_2$$

Let $R_2 = 10\,\text{k}$ $\qquad \therefore R_1 = 130\,\text{k}\Omega\,(120\,\text{k std})$



Also WKT

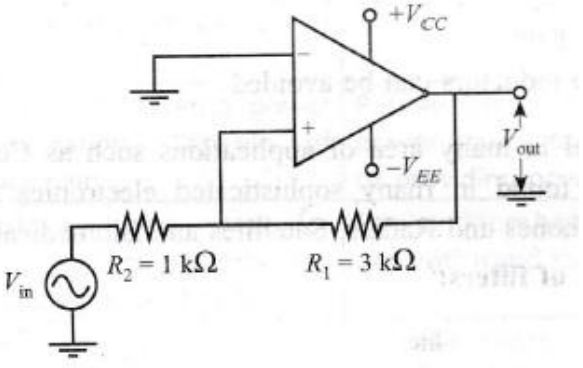
$$\text{UTP} + \text{LTP} = \frac{2R_1.V_{Ref}}{R_1+R_2}$$

$$V_{Ref} = \frac{(R_1+R_2)(\text{UTP}+\text{LTP})}{2R_1} \qquad V_{Ref} = 3.27\,\text{V}.$$

Example 7:

For the schmitt trigger R_1 = 3 kΩ and R_2 = 1 kΩ calculate the V_{UTP}, V_{LTP} and V_H. Assume saturation voltages as ± 12 V.

Given: $V_{sat}^{+} = 12\,\text{V}$; $V_{sat}^{-} = -12\,\text{V}$; $R_1 = 2\,\text{k}\Omega$; $R_2 = 3\,\text{k}\Omega$



WKT

$$V_{UTP} = \frac{(V_{sat}^{+})R_1}{R_2} = \frac{(12)\times1\,\text{k}}{3\,\text{k}} = 4\,\text{V}$$

$$V_{LTP} = \frac{-(V_{sat}^{-})R_1}{R_2} = \frac{-(12)\times1\,\text{k}}{3\,\text{k}} = -4\,\text{V}$$

The hysteresis width is given by

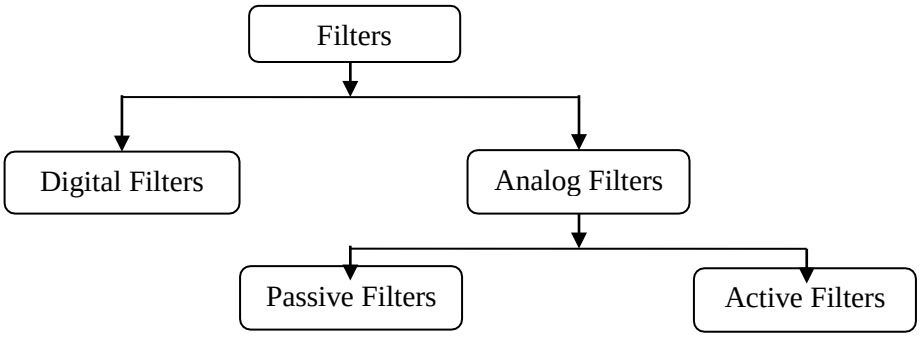
$$V_H = \frac{R_1}{R_2}\left[V_{sat}^{+} - V_{sat}^{-}\right] = \frac{1\,\text{k}}{3\,\text{k}}\left[12-(-12)\right] = \frac{24}{3} = 8\,\text{V}.$$

ACTIVE FILTERS:

Filter is a frequency selective circuit commonly used in signal processing that passes signal of specified range of frequencies and blocks the signals of frequencies outside the band. Active filters are attractive due to their –

- Flexibility in gain control
- Small component size
- No loading problem
- Pass band gain
- Use of the inductors can be avoided

Filters are useful in many areas of applications, such as Communication and Signal Processing. They are found in electronic systems like Radio, Television, Telephones, Radars, satellites, and Biomedical instruments.



Broader Classification of Filters

Passive filters work for high frequencies; but at audio frequencies, the inductors become problematic, as they are large, heavy, high power dissipation, and expensive.

Active filters use Op-Amp as the active element, resistors and capacitors as passive elements.

SNo.	Passive Filters	Active Filters
1	Filters with only components like resistors, capacitors, and inductors are known as passive filters.	Filters with components such as Op-Amps, transistors, and other active elements are known as active filters.
2	Passive filters do not require an external power source for operation; incapable of providing power gain.	Active filters require an external power supply for operation; capable of providing power gain.
3	Better stability and can withstand large currents.	Oscillations and noise will be generated due to feedback loops.
4	A passive filter has no frequency	Due to active elements, active filters have

	limitations.	frequency limitations.
5	Passive filters circuits are bulky/ heavy due to the presence of inductors; they consume more power and operate with limited speed.	Active filters circuits are more compact, less heavy; and operate with high speed.
6	Difficult to fabricate in IC form and usually designed using discrete components.	Can be fabricated in IC form and usually designed using discrete components.

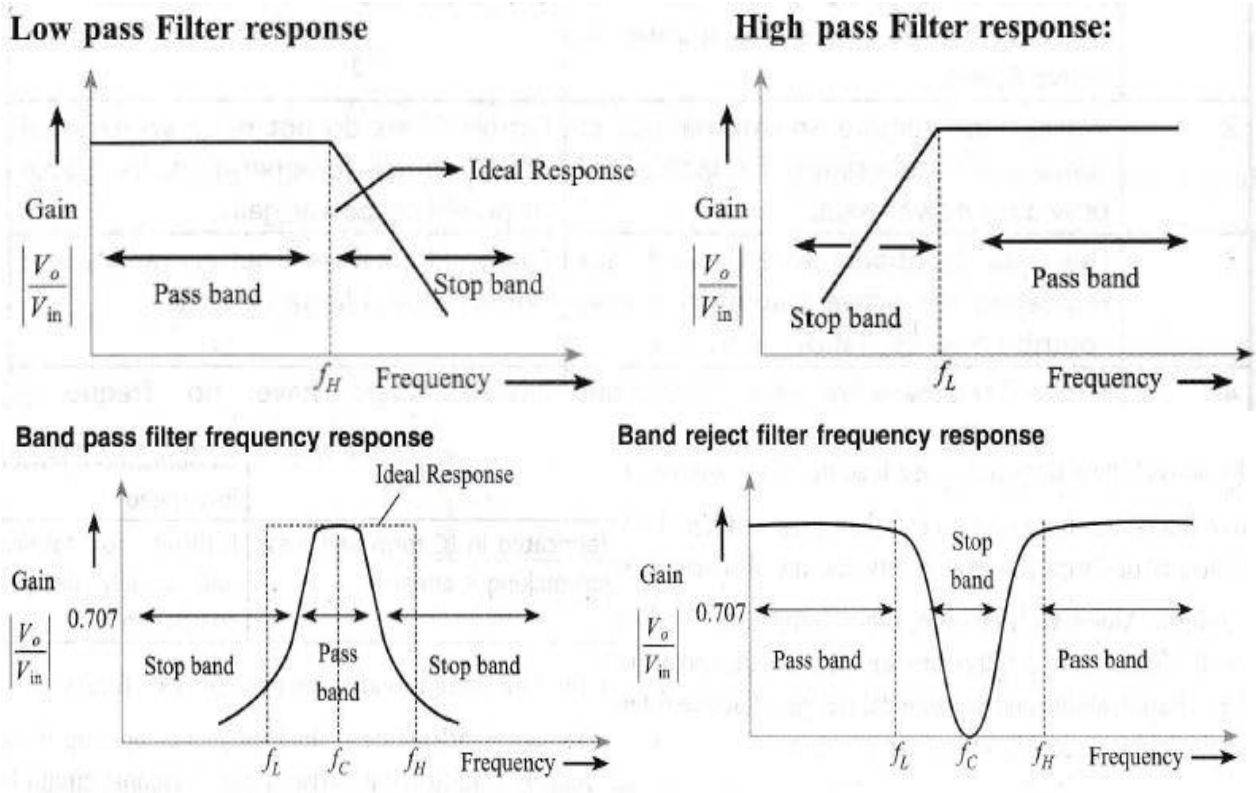
Active filters offer the following advantages over Passive filters:

- Gain and frequency adjustment flexibility
- No loading problem & No insertion loss
- Size and weight
- Cost.

Most commonly used active filters are –

- Low-pass filter, High-pass filter, Band-pass filter, Band-stop filter (Band-reject filter), and All-pass filter.

Frequency Response:

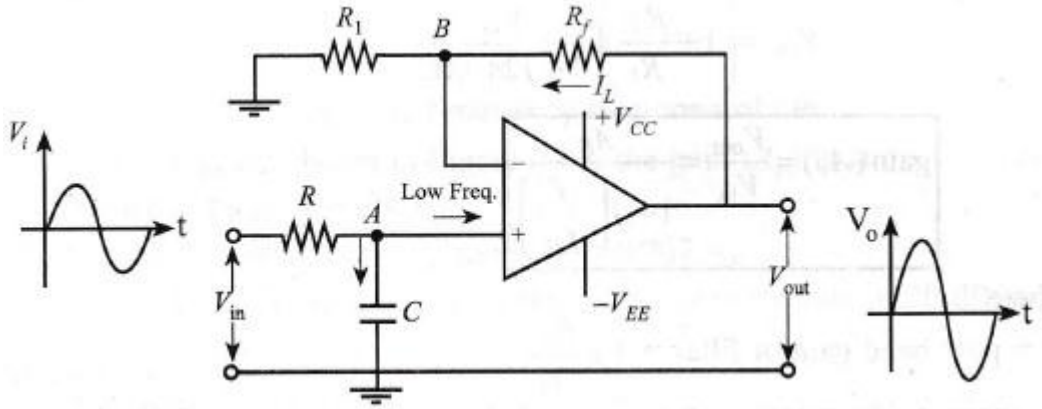


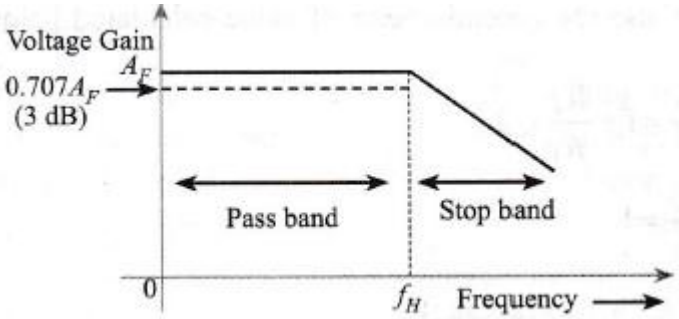
Design:

An active filter generally uses Op-Amp. Op-Amp has very high input impedance and low output impedance. The gain is determined by the resistive network in the feedback loop.

First Oder Active Low-Pass Filter (LPF):

The first-order low-pass butter worth filter consists of a single RC filter stage, providing a low frequency path to the non-inverting input of an Op-Amp. The circuit diagram and the frequency response of the circuit is given below:





- From the graph; the gain (A_F) is almost constant for the frequency range: $0 < f < f_H$.
- At cut-off frequency, $f = f_H$, the gain is $0.707A_F$.
- After cut-off frequency f_H, the gain decreases at the rate of 20 dB/decade.
- The cut-off frequency is given by: $ff_{HH} = \frac{1}{2\pi RRCC}$
- Pass band gain is given by: $AA_{FF} = 1 + \frac{RR_{ff}}{RR_1}$

Some applications of low-pass filters are –

- Low-pass filters are used in Audio amplifiers
- LPFs are used in equalizers or speakers to reduce the high frequency noise.

Example 1:

Design a first order low pass filter with cut-off frequency of 2.2 kHz and with pass band gain of 2.

Given: cut-off frequency f_H = 2.2 KHz.

Let us choose C = 0.01 μF.

WKT $f_H = \frac{1}{2\pi RC}$

$$\Rightarrow \quad R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi \times 2.2\times10^{3}\times0.01\times10^{-6}}$$

$$R = 7.233 k\Omega$$

For frequency scaling, use the potentiometer of value calculated below.

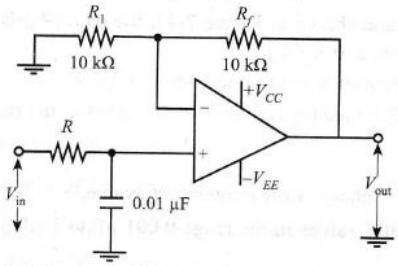
W.K.T

$$A_F = 1 + \frac{R_f}{R_1} = 2$$

$$\frac{R_f}{R_1} = 1$$

Therefore $R_f = R_1$ = 10 kΩ(Take).

The low pass filter circuit with designed values is as follows:



Example 2:

Determine the value of the resistance required for the low pass filter with cut-off frequency 30 k rad/sec and capacitor value = 0.001 μF.

Given ω_H = 30k rad/sec and C = 0.001 μF.

WKT $\omega_H = 2\pi f_H$

and $f_H = \frac{1}{2\pi RC}$

$$\therefore \quad \omega_H = \cancel{2\pi} \times \frac{1}{\cancel{2\pi} R\times0.001\times10^{-6}} = 30\times10^{3}$$

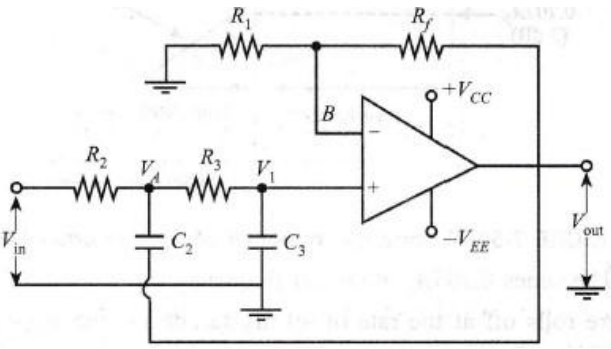
$$R = \frac{1}{30\times10^{3}\times0.001\times10^{-6}}$$

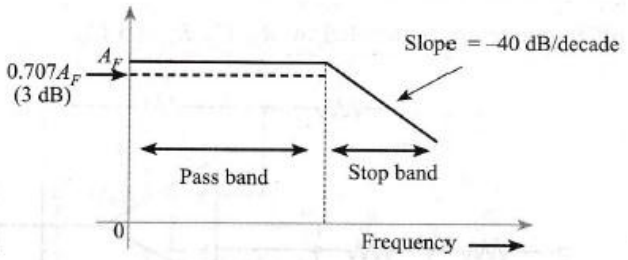
$$= \frac{1}{30\times\cancel{10^{3}}\times\cancel{10^{-3}}\times10^{-6}} = 0.33\times10^{+5}$$

$$\boxed{R = 33\ k\Omega}$$

Second Order Low-Pass Filter:

First order filter can be converted to second order filter by adding an extra RC-network, as shown in the following Figure. The frequency response of second order low-pass filter is same as the first order low-pass filter except that the gain at the stop band rolls off at the rate of 40 dB/decade.





- After cut-off frequency f_H, the gain decreases at the rate of 40 dB/decade.
- The cut-off frequency is given by: $ff_{HH} = \frac{1}{2\pi\sqrt{RR_3CC_2CC_3}}$.
  - If $R_2 = R_3 = R$ & $C_2 = C_3 = C$; then $ff_{HH} = \frac{1}{2\pi RRCC}$
- Pass band gain is given by: $AA_{FF} = 1 + \frac{RR_{ff}}{RR_1}$

Example 1:

Determine the values of Resistance required for second order low pass Butter worth filter having cut-off frequency as 15 k rad/sec with capacitor value as 0.01 µF.

Given: ω_H = 15 k rad/sec, C = 0.01 F.

From equation (7.38)

$$f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$$

But $R_2 = R_3 = R$ and $C_2 = C_3 = C$ and C as 0.01 µF

$$f_H = \frac{1}{2\pi\sqrt{(R)^2\times(0.01\times10^{-6})^2}} = \frac{1}{2\pi\times R\times0.01\times10^{-6}} \quad (*)$$

and $\omega_H = 2\pi f_H$ = 15 k rad/sec $= 2\pi \times f_H = 15 \times 10^3$ $f_H = \frac{15\times10^3}{2\pi}$ =2.3870 kHz

on substituting f_H in equation(*), it becomes

$$2.3870\times10^3 = \frac{1}{2\pi\times R\times0.01\times10^{-6}} \qquad R = 6.67\ \text{k}\Omega \qquad R_2 = R_3 = 6.67\ \text{k}\Omega$$

Example 2:

Design a second order low pass filter with cut-off frequency of 10 kHz and unity gain at low frequency. Also calculate the voltage transfer function magnitude at 15 kHz for the filter.

Given: Cut-off frequency $f_H = \frac{1}{2\pi RC}$

$$\therefore \quad RC = \frac{1}{2\pi f_H} = \frac{1}{2\pi\times10\times10^3} = 15.92\times10^{-6}$$

Let R = 100 kΩ, then $C = \frac{15.92\times10^{-6}}{100\times10^3}$ = 0.159 pF

Therefore C_2 = 0.159 pF and C_3 = 0.159 pF

The voltage transfer function is given by

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^4}} = \frac{1}{\sqrt{1+\left(\frac{15\times10^3}{10\times10^3}\right)}} = 0.406$$

Example 3:

Design a second order low pass butter worth filter for the cut-off frequency $f_H = 200$ Hz and draw the circuit diagram.

Given : $f_H = 200$ Hz.

Choose $R_2 = R_3 = R$ and $C_2 = C_3 = C = 0.1$ μF

Now, let us find value of R

$$f_H = \frac{1}{2\pi RC}$$

$$200 = \frac{1}{2\pi \times R \times 0.1 \times 10^{-6}}$$

$$\boxed{R = 7.96\ \text{k}\Omega.}$$

For second order filter

$$R_f = 0.586R,$$

i.e $$A_F = 1 + \frac{R_f}{R_1} = 1.586.$$

choosing $R_1 = 10\ \text{k}\Omega$

$$1 + \frac{R_f}{R_1} = 1.586$$

$$1 + \frac{R_f}{10\ \text{k}\Omega} = 1.586$$

$$\frac{R_f}{10\ \text{k}\Omega} = 0.586$$

$$R_f = 5.86\ \text{k}\Omega$$

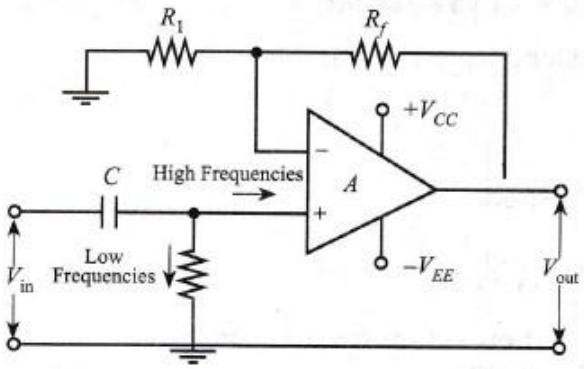
For adjustment use 10 kΩ pot.

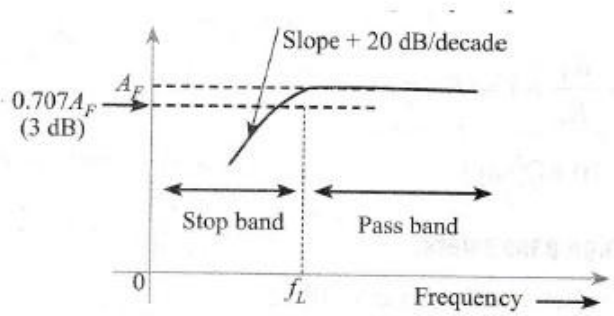
High-Pass Butter Worth Filter:

High-pass filters passes higher frequency signals, attenuating all signals below cut-off frequency, f_L.

First Order High-Pass Butter Worth Filter:

The filter circuit consists of a passive filter followed by a non-inverting amplifier.





- At low frequency: $f < f_L$, $\frac{V_0}{V_{in}} < A_F$. A_F increases at the rate of 20 dB/decade till $f = f_L$
- At cut-off frequency, $f = f_L$, the gain is $0.707A_F$.
- At very high frequency $f > f_L$, $\frac{V_0}{V_{in}} = A_F$ is constant.
- The cut-off frequency is given by: $f_L = \frac{1}{2\pi RC}$
- Pass band gain is given by: $A_F = 1 + \frac{R_f}{R_1}$

Example 1:

Design a first order high pass filter with a cut-off frequency of 10 kHz with pass band gain of 2.

Given: f_L = 101 kHz (given)

Choose $C < 1$ μF.

Let $C = 0.01$ μF

Calculate $R = \dfrac{1}{2\pi fc}$

$$R = \frac{1}{2\pi \times 10 \times 10^3 \times 0.01 \times 10^{-6}}$$

$$\boxed{R = 1.5913\ \text{k}\Omega}$$

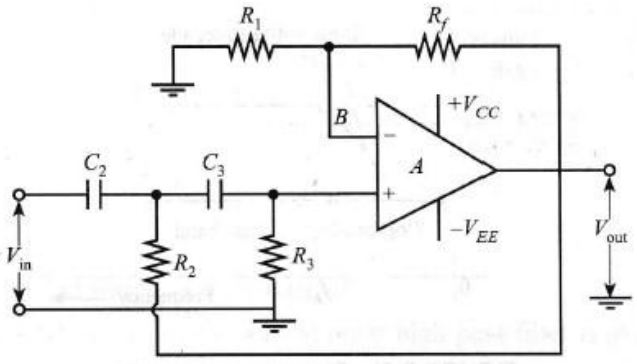
Step 4: Gain $A_F = 2 = 1 + \dfrac{R_f}{R_1}$

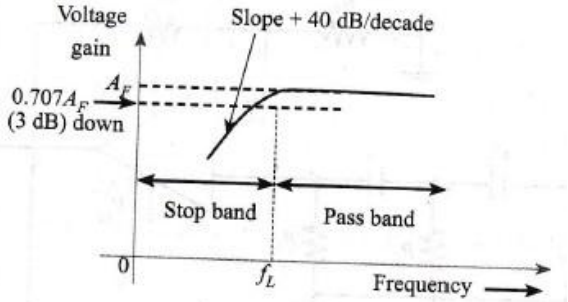
$$\therefore \quad \frac{R_f}{R_1} = 1 \Rightarrow R_f = R_1$$

Choosing R_1 = 10 kΩ(say).

Second Order High-Pass Filter:

A first order high-pass filter can be converted into a second order high-pass filter by using an extra RC-network in the input side. The frequency response of second order high-pass filter is same as the first order high-pass filter except that the gain at the stop band rolls off at the rate of 40 dB/decade.

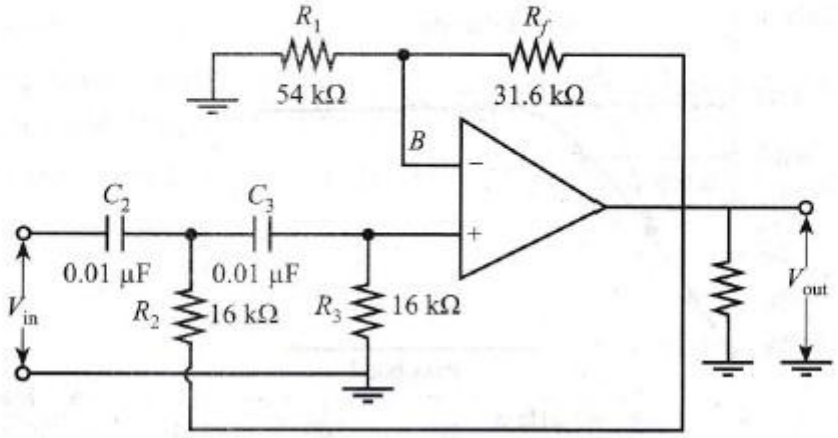




- The cut-off frequency is given by: $ff_{LL} = \dfrac{1}{2\pi \sqrt{2} RR_3 CC_2 CC_3}$.
  - If $R_2 = R_3 = R$ & $C_2 = C_3 = C$; then $ff_{LL} = \dfrac{1}{2\pi RRCC}$
- Pass band gain is given by: $AA_{FF} = 1 + \dfrac{RR_{ff}}{RR_1}$

Example 1:

For the circuit shown in Figure find (a) lower cut-off frequency (b) pass band gain



Given: $R_2 = R_3 = 16\ \text{k}\Omega$ and $C_2 = C_3 = 0.01\ \mu\text{F}$

(a) The lower cut-off frequency for second order high pass filter is given by

$$f_L = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}} = \frac{1}{2\pi\sqrt{\left(16\times10^3\right)^2\left(0.01\times10^{-6}\right)^2}} = 1\,\text{kHz}$$

$$\boxed{f_L = 1\,\text{kHz}}$$

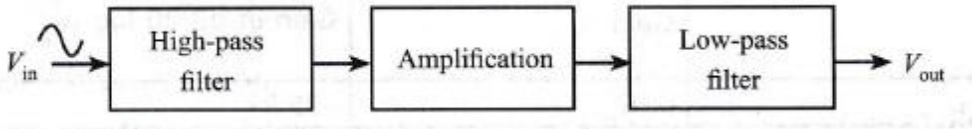
b) The pass band gain is

$$A_F = 1 + \frac{R_f}{R_1} = 1 + \frac{31.6\times10^3}{54\times10^3} = 1.586$$

$$\boxed{A_F = 1.586}$$

Active Band-Pass Filter:

Active band-pass filters provide an effective means of making a filter to pass only a given band of frequencies. An active band-pass filter can be constructed by cascading a single low-pass filter with a single high-pass filter, as shown below:



The cut-off frequency of the low-pass filter is higher than the cut-off frequency of the high-pass filter; and the difference between these frequencies at the –3dB point will give the '*bandwidth*' of the band-pass filter. A band-pass filter can be characterized by Quality factor (Q). The relation between Q, 3dB bandwidth, and the centre frequency, f , is given by; $QQ = \_\frac{ff_{CC}}{}$

$\frac{}{ff_{CC}}$

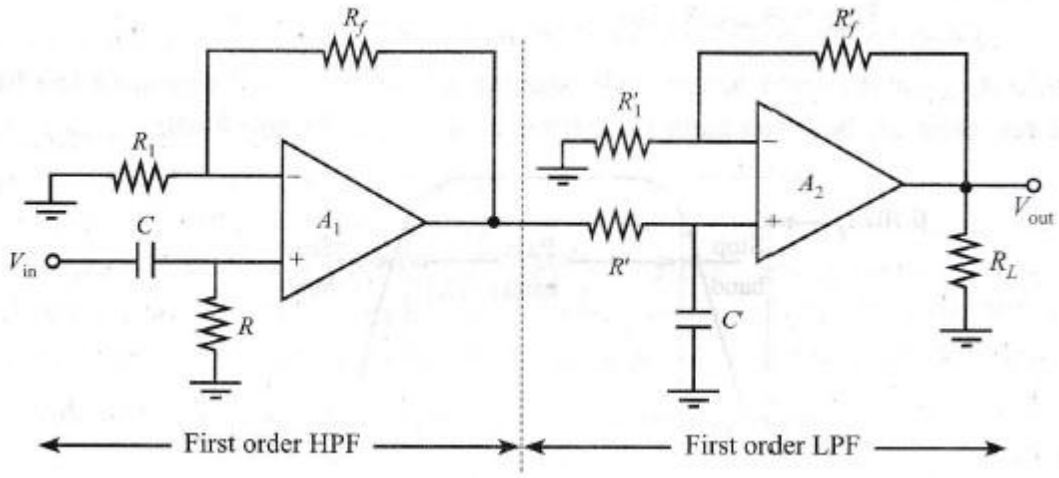
C

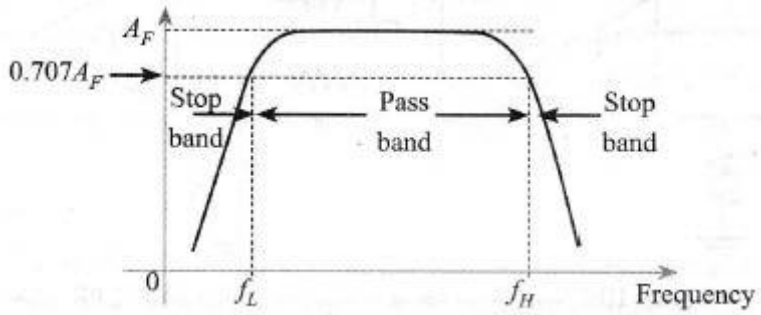
B

BBB $ff_{HH} - ff_{LL}$

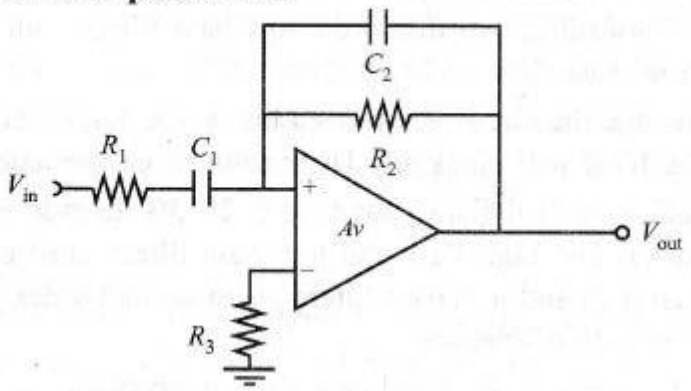
Wide Band-Pass Filter:

A low *Q*-filter will have a wide-pass-band; i.e., with $Q < 10$. It has wide flat response over the range of frequencies and bandwidth is large.





Single stage first order Bandpass filter:

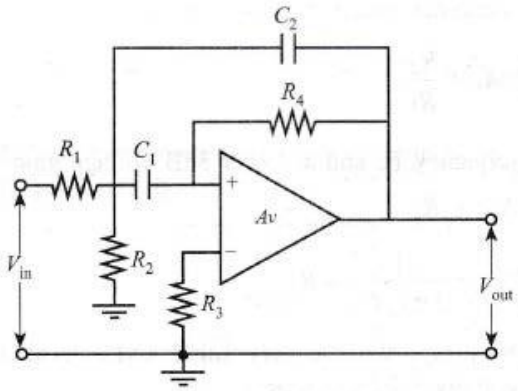


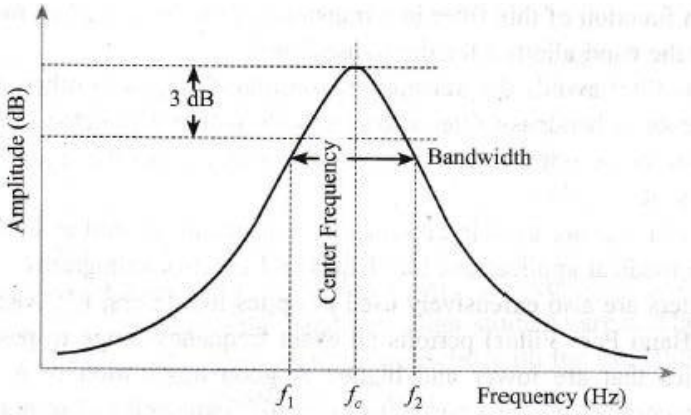
Narrow Band-Pass Filter:

A high *Q*-filter will have a narrow-pass-band; i.e., with $Q > 10$. It has a sharp bell type response, with high gain and high selectivity.

- $ff_{\alpha} = \frac{1}{2\pi \blacksquare_1 RR_2 CC_1 CC_2}$.
- $QQ_{BBUU} = \frac{ff_{\alpha\ c}}{BBBB_{3ddBB}} = \frac{\frac{RR_1}{2}}{\blacksquare RR_2}$

- Maximum Gain, $AA_{vv} = -\frac{RR_2}{2RR_1} = -2QQ^2$





Applications of Band-Pass Filters (BPF):

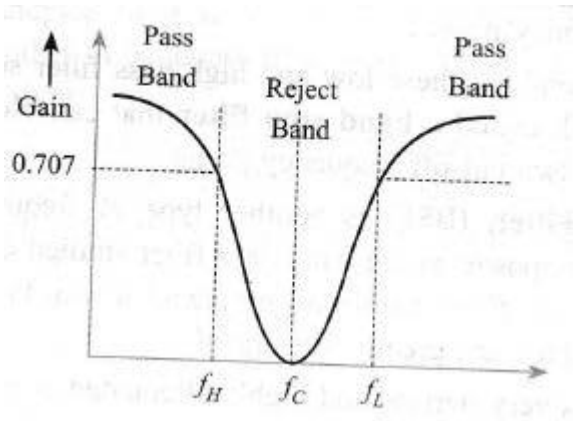
- BPFs are also used in optics like Lasers, LIDARS, etc.
- BPFs are extensively used in wireless transmitters and receivers.
- BPFs are used in electronic devices like Sonar, Seismology; and medical applications like ECG, and electrocardiograms.
- BPFs are extensively used for Audio signal processing, where a particular range of frequencies of sound is required while removing the rest.

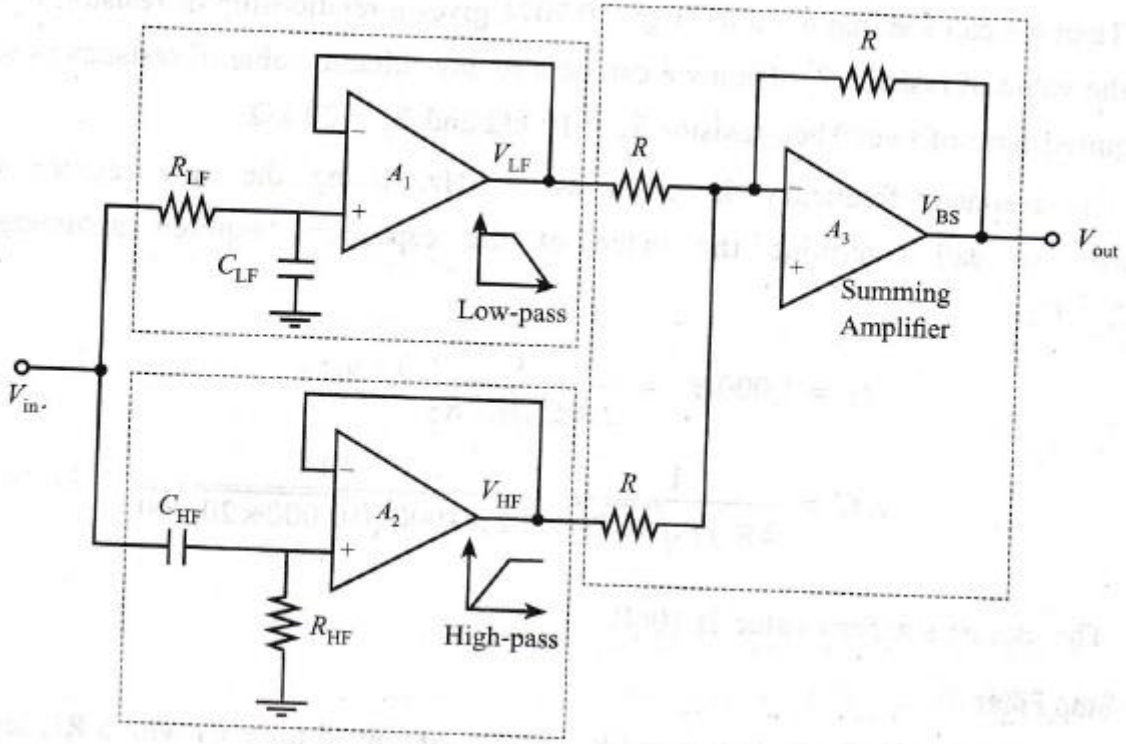
Band-Stop Filter (Band-Reject Filter):

Band-Stop Filer (BSF) is another type of frequency selective circuit that functions in exactly opposite to the band-pass filter. BSF passes all frequencies with the exception of those within a specified stop band, which are attenuated. If this stop band is very narrow and highly attenuated over a few hertz, then the band-stop filter is referred as a *notch filter*.

Wide Band-Reject Filter:

The frequency response curve and the circuit diagram of a wide band-reject filter is given below.





Example 2:

Design a basic wide-band, RC band stop filter with a lower cut-off frequency of 200Hz and a higher cut-off frequency of 800Hz. Find the geometric center frequency, –3dB bandwidth and Q of the circuit.

Given: $f_L = 200$ Hz, $f_H = 800$ Hz

We have

$$f = \frac{1}{2\pi RC} Hz$$

The upper and lower cut-off frequency points for a band stop filter can be found using the same formula as that for both the low and high pass filters.

Assuming a capacitor, C value for both filter sections of 0.1 uF, the values of the two frequency determining resistors, R_L and R_H are calculated as follows.

High Pass Filter Section

$$f_L = \frac{1}{2\pi R_L C} = 200\,\text{Hz} \quad \text{and} \quad C = 0.1\,\mu\text{F}$$

$$\therefore R_L = \frac{1}{2\pi \times 200 \times 0.1 \times 10^{-6}} = 7958\,\Omega \text{ or } 8\,\text{k}\Omega$$

Low Pass Filter Section

$$f_H = \frac{1}{2\pi R_H C} = 800\,\text{Hz} \quad \text{and} \quad C = 0.1\,\mu\text{F}$$

$$\therefore R_H = \frac{1}{2\pi \times 800 \times 0.1 \times 10^{-6}} = 1990\,\Omega \text{ or } 2\,\text{k}\Omega$$

From this, we can calculate the geometric center frequency, f_C as:

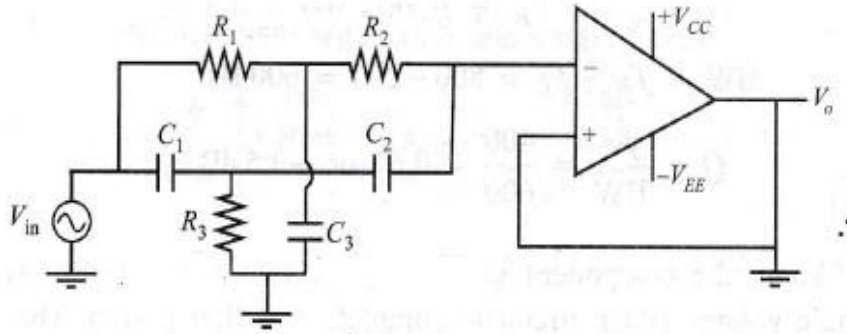
$$f_C = \sqrt{f_L \times f_H} = \sqrt{200 \times 800} = 400 \text{ Hz}$$

$$\text{BW} = f_H - f_L = 800 - 200 = 600 \text{ Hz}$$

$$Q = \frac{f_C}{\text{BW}} = \frac{400}{600} = 0.67 \text{ or } -3.5 \text{ dB}$$

Narrow Band-Stop Filter (Notch Filter):

Notch filters are highly selective, high-*Q* form of band-stop filter, which can be used to reject a single or very small band of frequencies. The most common notch filter design is the twin-T notch filter network (shown below).

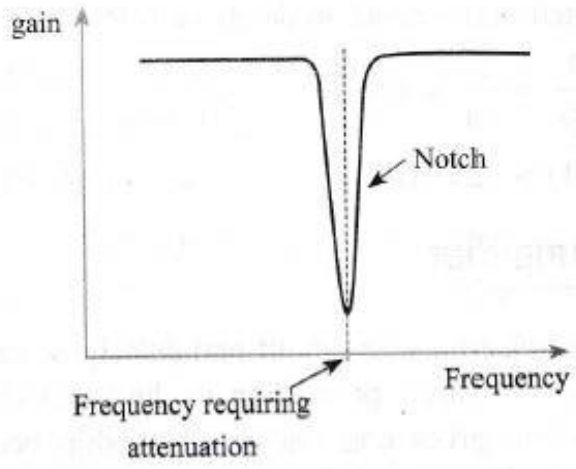


$$R_1 = R_2 = 2(R_3)$$

$$C_2 = C_3 = (0.5)C_1$$

$$\therefore f_N = f_{\text{notch}} = \frac{1}{4\pi R_3 C_3}$$

A twin-T network offers very high reactance at the resonance frequency and very low reactance at frequency off-resonance. In the circuit diagram, very low frequency signals find their way to the output via low-pass filter (formed by $R_1 - R_2 - C_3$); and very high frequency signals find their way to the output via high-pass filter (formed by $C_1 - C_2 - R_3$). Hence, in an intermediate band of frequencies, both filters pass signals to the output; due to cancellation of +ve phase shift of high-pass filter with the –ve phase shift of the low-pass filter.



Example 1:

Design a two op-amp narrow-band, RC notch filter with a center notch frequency, f_N of 1 kHz and a –3dB bandwidth of 100 Hz. Use 0.1 μF capacitors in your design and calculate the expected notch depth in decibels.

Given: $f_N = 1000$ Hz, BW = 100 Hz and $C = 0.1$ uF.

1. Calculate value of R for the given capacitance of 0.1 uF

$$R = \frac{1}{4\pi f_N C} = \frac{1}{4\pi \times 1000 \times 0.1 \times 10^{-6}}$$

$$\therefore \quad R = 795\ \Omega \text{ or } 800\ \Omega$$

2. Calculate value of Q

$$Q = \frac{f_N}{BW} = \frac{1000}{100} = 10$$

3. Calculate value of feedback fraction k

$$K = 1 - \frac{1}{4Q} = 1 - \frac{1}{4 \times 10} = 0.975$$

4. Calculate the values of resistors R_3 and R_4

$$K = 0.975 = \frac{R_4}{R_3 + R_4}$$

Assume $R_4 = 10$ kΩ, then R_3 equals:

$$R_3 = R_4 - 975\ R_4 = 10000 - 0.975 \times 10000,$$

$$\therefore \quad R_3 = 250\ \Omega$$

5. Calculate expected notch depth in decibels, (dB)

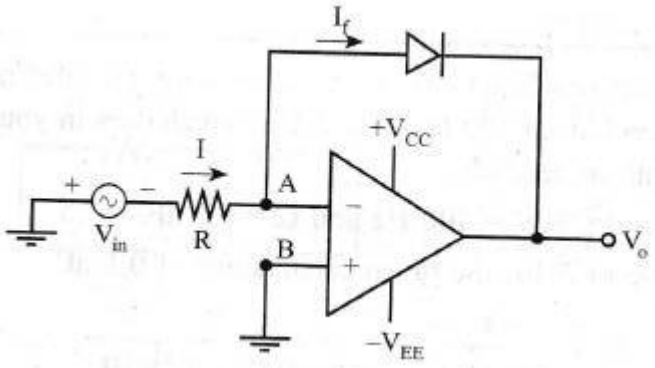
$$\frac{1}{Q} = \frac{1}{10} = 0.1$$

$$f_{N(\text{d B})} = 20 \log (0.1) = -20 \text{ dB}$$

NON LINEAR AMPLIFIER:

Non linearity is the behavior of a circuit, particularly an amplifier, in which the output signal strength do not vary in direct proportion to the input signal strength. A non-linear amplifier in as circuit which gives non linear relationship between its input and output signals.

The Non linear amplification can be achieved in a simple way by just connecting a non-linear device such as PN-junction diode in the feedback path. In the circuit shown is the following Figure, large change in input voltage causes small change in the output voltage. This circuit is a log amplifier, hence the output voltage is logarithm of the input voltage.



The above Figure shows a non-linear amplifier, where diode '*D*' is used in negative feedback path. By virtual ground concept; as node *B* is grounded, node *A* will be virtually grounded. Therefore, $V_A = 0$.

We have; $I = \frac{V_{in} - V_A}{R} = \frac{V_{in}}{R}$ since $V_A = 0$.

Let I_f be the current through the diode. The voltage across diode is $V_A - V_0$. Since, $V_A = 0$, the voltage across diode is $-V_0$.

Diode equation: $-V_0 = \eta V_T \ln \left(\frac{I_f}{I_r}\right)$

Where, V_T – Voltage equivalent of Temperature

I_f – Diode forward current

I_r – Diode reverse saturation current.

Since, current through the Op-Amp is negligible; $I = I_f$

Therefore, $I_f = I = \frac{V_{in}}{R}$

Gives, $V_0 = \eta V_T \ln \left(\frac{V_{in}}{I_r R}\right) = \eta V_T \ln \left(\frac{V_{in}}{V_{ref}}\right)$ $I_r R = V_{ref}$ is a constant.

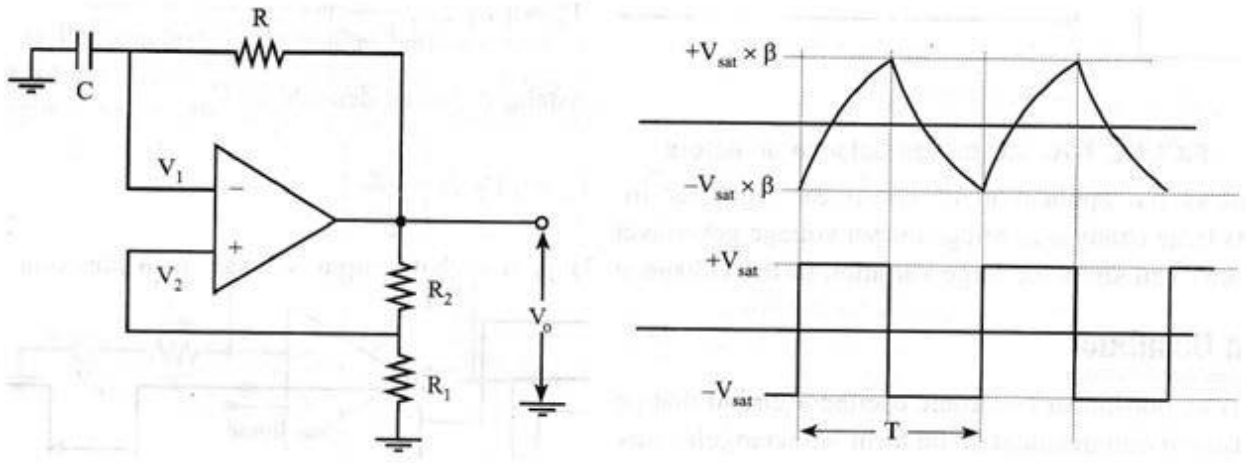
The above equation shows that, the output voltage is a logarithmic function of input voltage.

Applications: Non-linear Amplifiers are used in AC bridge balance detectors.

RELAXATION OSCILLATOR:

Relaxation oscillator is a non-linear electronic oscillator circuit that generates a continuous non-sinusoidal output signal in the form of rectangular wave, triangular wave or a saw-tooth wave. The time period of non-sinusoidal output depends on the charging time of the capacitor connected in the oscillator circuit.

The relaxation oscillator basically contains a feedback loop that has a switching device in the form of transistor, relays, operational amplifiers, comparators, or a tunnel diode that charges a capacitor through a resistance till it reaches a threshold level then discharges it again. The following Figure shows the basic circuit of an Op-Amp based relaxation oscillator.



Assume that, the output is initially in positive saturation. As a result, voltage at non-inverting input of Op-Amp is $+V_{SAT} * R_1 / (R_1 + R_2)$. This force the output to stay in positive saturation as the capacitor C is initially in fully discharged state. Capacitor C starts charging towards $+V_{SAT}$ through R. The moment the capacitor voltage exceeds the voltage appearing at the non-inverting input, the output switches to $-V_{SAT}$.

Now, the voltage appearing at the non-inverting input changes to $-V_{SAT} * R_1 / (R_1 + R_2)$. The capacitor starts discharging and after reaching zero, it begins to discharge towards $-V_{SAT}$. Again, as soon as it becomes more negative than the voltage appearing at the non-inverting input of the Op-Amp, the output switches back to $+V_{SAT}$.

The expression for the time period of the output rectangular waveform is given by; $TT = 2\,RRCC \ln(\frac{1+\beta\beta}{1-\beta\beta})$

In the above equation; the natural logarithm is used, which is logarithm to base *e*. By varying the value of resistor R, the time period of the output waveform can be varied.

β is the feedback fraction/ factor and is given by $\beta = R1/(R1+R2)$

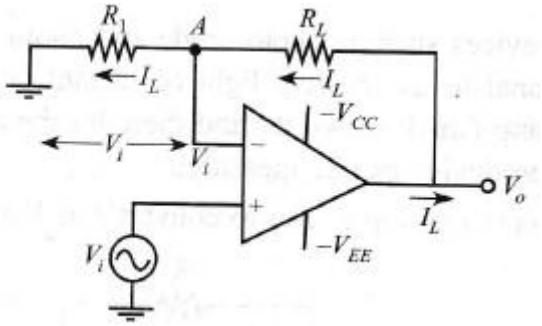
When the output voltage V_0 is at at $+V_{SAT}$ the feedback voltage is known as upper threshold voltage V_{UTP} and is given by $+V_{SAT} \times R1/(R1+R2)$

When the output voltage V_0 is at at $-V_{SAT}$ the feedback voltage is known as lower threshold voltage V_{LTP} and is given by $-V_{SAT} \times R1/(R1+R2)$

VOLTAGE TO CURRENT (V TO I) CONVERTER:

In many applications, we have to convert a voltage to a proportionate current. These voltage-to-current converter circuits can be of *two types*:

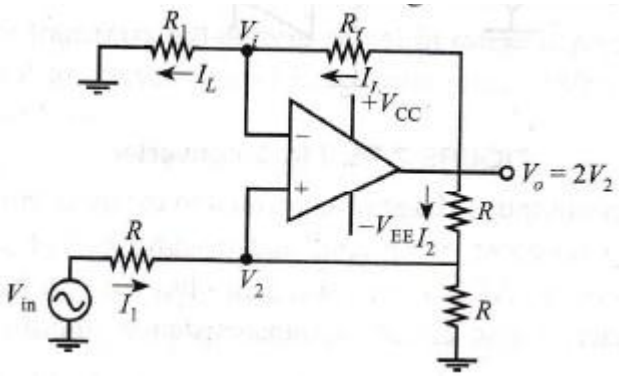
a) **Voltage to Current Converter with Floating Load:** The circuit is shown in the following Figure, where R_L is the floating load.



Since, voltage at node A is V; $= II RR$ Or, $II = \frac{VV_{ii}}{RR_1}$

i.e., input voltage V_i is converted into and output current.

b) **Voltage to Current Converter with Grounded Load:** The circuit is shown in the following Figure.



$$II_1 = \frac{VV_{iii\,i} - VV_2}{RR} \qquad II_2 = \frac{VV_0 - VV_2}{RR}$$

The load current is given by; $I_L = I_1 + I_2$

Therefore, $II_{LL} = \frac{VV_{iii\,i} - VV_2}{RR} + \frac{VV_0 - VV_2}{RR} = \frac{VV_{iii\,i} + VV_0 - 2VV_2}{RR}$

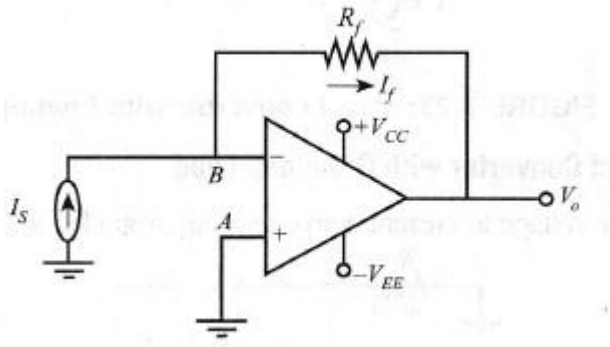
For a non-inverting amplifier, we know that; $AA = 1 + \frac{RR}{W} = 2 \quad SSSS, \quad = 2VV_{vv}$

Therefore, $II_{LL} = \frac{VV_{iiii} + 2VV_2 - 2VV_2}{RR} \quad 00rr, \quad = \frac{VV_{iiii}}{RR}$

Thus, the current I_L is proportionate to voltage.

CURRENT TO VOLTAGE (C TO V) CONVERTER:

Consider the simple Op-Amp circuit to convert *I* to *V*, as shown in the following Figure.



Since, current through the Op-Amp is negligible; $I_S = I_f$

$$II_{ss} = II_{ff} = \frac{W_{BB} - W_0}{RR_{ff}}$$

By virtual ground concept; as node *A* is grounded, node *B* will be virtually grounded. Therefore, $V_B = 0$. Therefore,

$$II_{ss} = \frac{-W_0}{RR_{ff}} \quad 00rr, \quad W_0 = II_{SS}RR$$

Thus, output is proportional to the input current I_S, and the circuit works as *I* to *V* converter.

ANALOG AND DIGITAL ELECTRONICS

VOLTAGE REGULATORS

All electronic systems that we use daily, requires a stable power supply voltage source; and voltage regulators accomplish that. *Voltage regulator* is a circuit that keeps the output voltage constant under all operating conditions. *Voltage regulation* is the process of keeping a voltage steady under conditions of changing applied voltage, changing load and temperature.

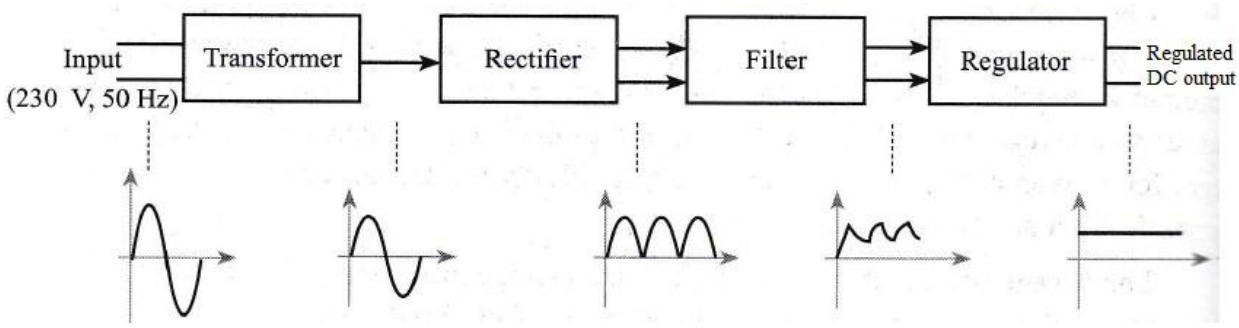
There are *two types* of voltage regulators: *shunt* and *series*.

Need for Regulators:

In ordinary power supplies, the voltage regulation is very poor. The DC output voltage changes appreciably with change in load current. The output voltage also changes due to fluctuations in the input AC supply. This is due the following reasons:

1. In practice, there are considerable fluctuations in line voltage caused by external factors. This changes the DC output voltage. Most of the electronic circuits will refuse to work satisfactorily on such output voltage fluctuations. Hence, regulated power supply is the solution.
2. The internal resistance of ordinary power supply is relatively large (> 30 Ω). Therefore, output voltage is affected by the amount of load current drawn from the supply. These variations in DC voltage may cause erratic operation of circuits. Without stable potentials, circuit performance degrades and if the variations are large enough, the components may get destroyed. In order to avoid this, regulated power supply is used.

Input to the voltage regulator is unregulated pulsating DC obtained from filter rectifier. Its output is constant DC voltage which is almost ripple free. The following Figure shows block diagram of regulated power supply.



The *transformer* provides voltage transformation and electrical isolation between the input power supply (AC mains) and the DC output. The *rectifier circuit* changes the AC voltage appearing across the transformer secondary to DC (unidirectional output). The rectifier circuit always has some AC content known as ripple. The *filter circuit* smoothens the ripple of the rectifier circuit. The *regulator* is a type of feedback circuit that ensures that the output DC voltage does not change from its nominal value due to change in line voltage or load current.

Factors Affecting the Load Voltage:

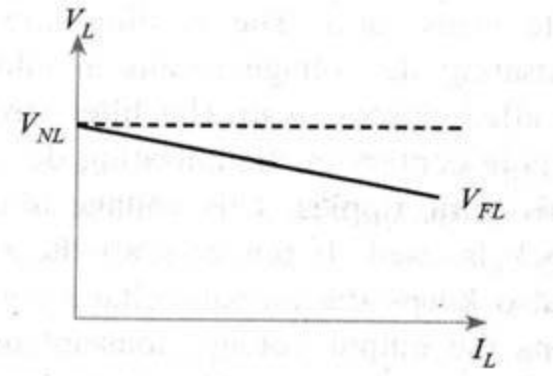
The variables affecting the load voltage in a power supply are given below:

1. ***Load current (I_L):*** Ideally the output voltage should remain constant in-spite of changes in the load current, but practically the power supply without regulator, the load voltage decreases as load current, I_L, increases. For practical power supply regulator, the load voltage must be constant through load to full load condition.
2. ***Line voltage:*** The input to the rectifier is AC (230 V) is the line voltage. This input decides the output voltage level. If input changes, output also changes. So this affects the performance of power supply. So ideally voltage must remain constant irrespective of any changes in the line voltage.
3. ***Temperature:*** In the power supply, the rectifier unit is used which uses PN-junction diode. As the diode characteristics are temperature dependent, the overall performance of the power supply is temperature dependent.

Performance Parameters of a Power Supply:

The power supply is judged by some parameters, called as *performance parameters*. These performance parameters are explained below:

1. ***Line Regulation:*** If the input to the rectifier unit i.e. 230 V changes, the output DC of rectifier will also change and since the output of rectifier is applied to the regulator, the output of regulator will also vary. Thus the source causes the change in output. This is as *source regulation* or *line regulation*. It is defined as the change in regulated DC output for a given change in input (line) voltage. Ideally the source regulation should be zero and practically it should be as low as possible.
2. ***Load Regulation:*** *Load regulation* is defined as the change in the regulated output voltage when load current is changed from zero (no load) to maximum value (full load). The load regulation ideally should be zero, but practically it should be as small as possible. The following Figure shows the load regulation characteristics. Percentage load regulation = $\left(\frac{VV_{OOL\ L} - VV_{FFLL}}{VV_{FFLL}}\right) * 100$



3. ***Voltage Stability factor (S_V):*** *Voltage stability factor* shows the dependency of output voltage on the input line voltage. *Voltage stability factor* is defined as the percentage change in the output voltage which occurs per volt change in input voltage, where load current and temperature are assumed to be constant. Smaller the value of this factor, better is the performance of power supply.
4. ***Temperature Stability Factor (S_r):*** As in the chain of power supply we are using semiconductor devices (diodes in rectifier block) the output voltage is temperature dependent. Thus the *temperature stability* of the power supply will be determined by temperature coefficients of various temperature sensitive semiconductor devices. So, it is better to choose the low temperature coefficient devices to keep output voltage constant and independent of temperature. S_r must be as small as possible, and ideally it should it should be zero for a power supply.
5. ***Ripple Rejection Factor (RR):*** The output of rectifier and filter consists of ripples. *Ripple rejection* is defined as a factor which shows how effectively the regulator rejects the ripples and attenuates it from input to output. As ripples in the output are small compared to input, the *RR* is very small and in dB, it is in negative value. Ripple rejection factor = $\frac{VV_{RRIIUUUULLE\ E}(OOUUTTUUUUTT)}{VV_{RRIIUUUULLEE}(IIOOUUUUTT)}$

When expressed in decibels, ripple rejection equals $20\log\frac{VV_{RRIIUUUULLE\ E}(OOUUTTUUUUTT)}{VV_{RRIIUUUULLEE}(IIOOUUUUTT)}$ dB

Also, $VV_{RRIIUUUULLEE}(SSooWWoooo WW) = \frac{VV_{RRIIUUUULLE\ E}(IIOOUUUUTT)}{1+LLSSSSoo\ GGssiiii}$

Example: *Two power supplies A and B are available in the market. Power supply A has no-load and full-load voltages of 40 V and 30 V respectively; whereas these values are 30 V and 28 V for power supply B. Which one do you think is better power supply?*

Supply A: V_{NL} = 40 V, V_{FL} = 30 V

% Voltage regulation = $[(V_{NL} - V_{FL})/V_{FL}]*100$ = [(40 – 30)/30]*100 = 33 %.

Supply B: V_{NL} = 30 V, V_{FL} = 28 V

% Voltage regulation = $[(V_{NL} - V_{FL})/V_{FL}]*100$ = [(30 – 28)/28*]*100 = 7 %.

Conclusion: The power supply which has lower voltage regulation is better. Hence, power supply *B* is between than power supply *A*.

Example: *A regulated power supply operates from 220 ± 20 VAC. It produces a no-load regulated output voltage of 24 ± 0.5 VDC. Also, the regulated output voltage falls from 24 VDC to 23.8 VDC as the load changes from no-load to full-load condition for the nominal value of input voltage. Determine (a) line regulation and (b) load regulation.*

Line regulation = (24.5 – 23.5)/24 = 1/24 = 0.0417 = 4.17%

Load regulation = (24 – 23.8)/23.8 = 0.2/23.8 = 0.0084 = 0.84%.

Example: *A regulated power supply provides a ripple rejection of –80dB. If the ripple voltage in the unregulated input were 2V, determine the output ripple.*

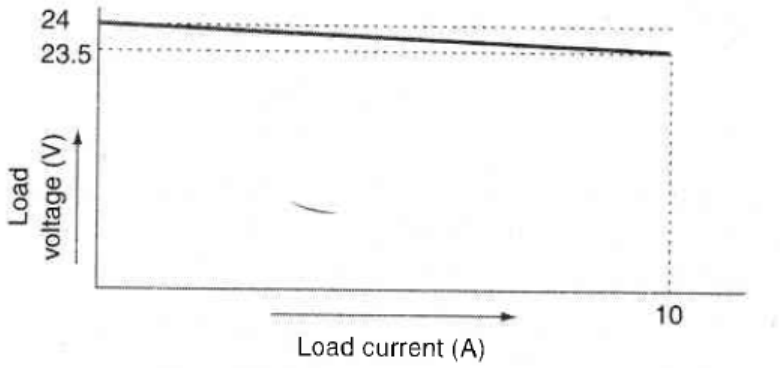
Ripple rejection in dB is given by; $20 \log \left(\frac{V_{RIPPLE\ (OUTPUT)}}{V_{RIPPLE\ (INPUT)}} \right) \text{dB} = -80\text{dB}$

Or $\log \left(\frac{V_{RIPPLE\ (OUTPUT)}}{V_{RIPPLE\ (INPUT)}} \right) = -4$

Or $\left(\frac{V_{RIPPLE\ (OUTPUT)}}{V_{RIPPLE\ (INPUT)}} \right) = 10^{-4}$

Therefore, output ripple = $2 * 10^{-4}$ V = 0.2mV

Example: *The following Figure shows load voltage versus load current characteristics of a regulated power supply. Determine the output impedance of the power supply.*



Output impedance is given by ratio of change in the output voltage for known change in the load current. From the given characteristic curve, output impedance = (24 – 23.5)/((10 – 0) = 0.5/10 = 0.05Ω = 50mΩ.

Three-Terminal Regulators:

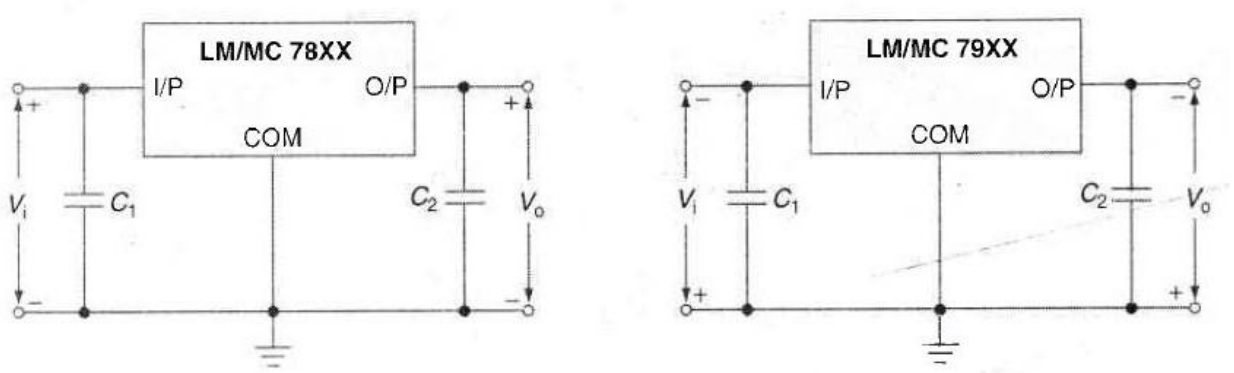
Three-terminal regulators require no external components. These are available in fixed output voltage (positive and negative) as well as adjustable output voltage (positive and negative) types with current rating 100mA, 500mA, 1.5A and 3.0A.

- LM/MC 78XX-series and LM 140XX/340XX-series are the popular three-terminal positive output voltage regulators.
- LM/MC 79XX-series and LM 120XX/320XX-series are the popular three-terminal negative output voltage regulators.
- LM 117/217/317 is common adjustable positive output voltage regulators.
- LM 137/237/337 is common adjustable negative output voltage regulators.
    - ✓ A two-digit number in place of "XX" indicates the regulated output voltage.

The minimum unregulated input to regulated output differential voltage required for the regulator to produce the intended regulated output voltage is known as *dropout voltage*. For example, consider a 5V regulator with a 2V dropout voltage; for this to give a regulated output, the input voltage must be least

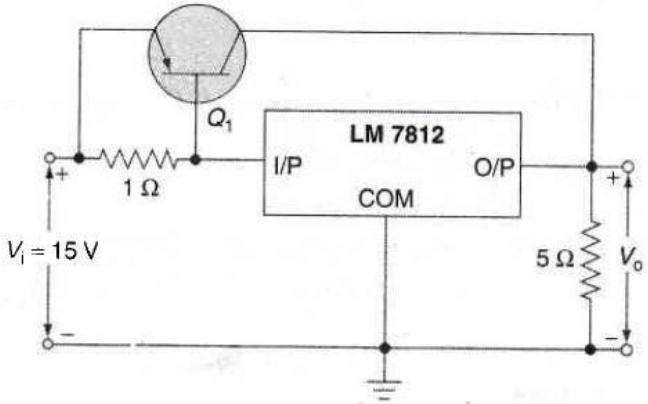
equal to the output voltage (5V) plus the dropout voltage (2V), which is 7V; any input below 7V will result into unregulated voltage output.

The following Figures show the basic application circuits using LM/MC 78XX-series and Lm/MC 79XX-series three-terminal regulators.



Basic Application Circuits using Three-Terminal Regulators

Example: *Refer three-terminal regulator circuit of following Figure. Determine (a) load current; (b) current through LM 7812; (c) current through external transistor; (d) power dissipated in LM 7812. Take* V_{BE} *(*Q_1*) = 0.7V.*



(a) Load current = 12/5 = 2.4A

(b) Current through regulator = 0.7/1 = 0.7A

(c) Current through external transistor = 2.4 – 0.7 = 1.7A

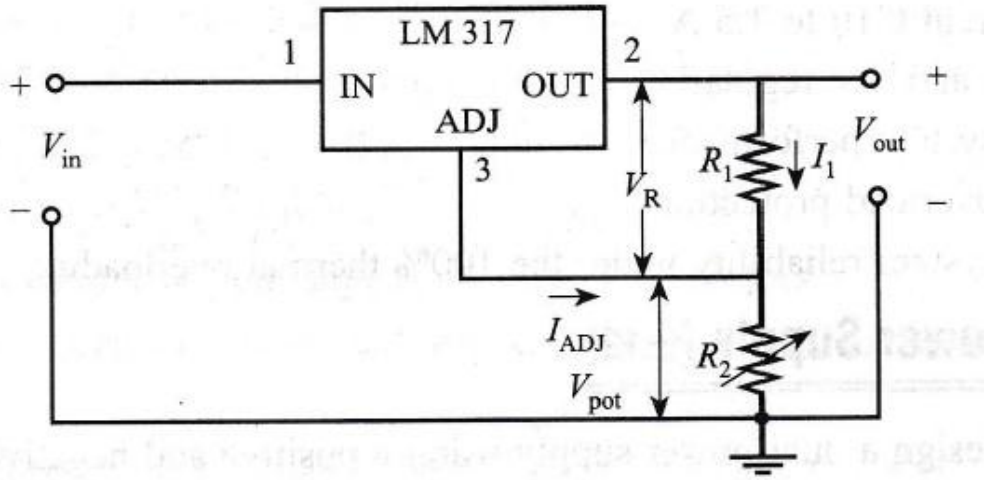
(d) Voltage appearing at regulator input = 15 – 0.7 = 14.3V

(e) Power dissipated in the regulator = (14.3 – 12) * 0.7 = 1.61W.

Adjustable Voltage Regulator:

An adjustable voltage regulator is a kind of regulator, whose regulated output voltage can be varied over a range. There are positive adjustable voltage regulators and negative adjustable regulators in practice.

LM317 is a classic example of positive adjustable voltage regulator, whose output voltage can be varied over a range of 1.2 V to 57 V. LM337 is an example of negative adjustable voltage regulator. LM337 is actually a compliment of LM317 which are similar in operation and design with the only difference being polarity of regulated output voltage.



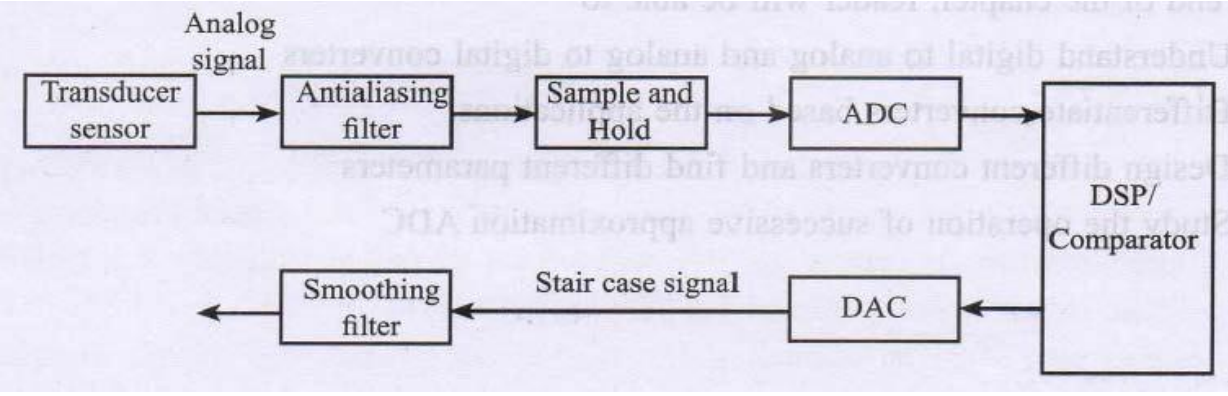
Connection of LM317 Adjustable Voltage Regulator

The resistors R_1 and R_2 determine the output voltage V_{out}. The resistor R_2 can be adjusted to get the output voltage in the range of 1.21 V to 57 V. The output voltage is given by;

$$V_{out} = V_R\,(1 + R_2/R_1) + I_{ADJ}R_2$$

D TO A & A TO D CONVERTERS

The digital system such as computers also need to communicate with physical processes and with people through analog signals. So there is a need of digital to analog converters.



Typical A/D and D/A Converter

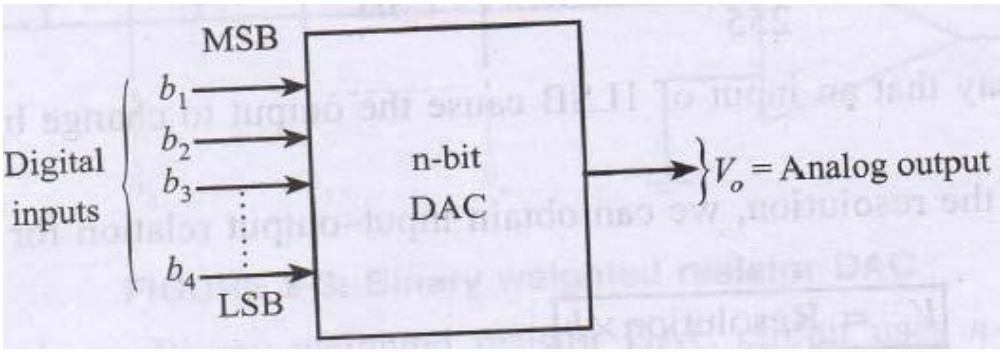
Naturally available signal is analog in form, and may be obtained from *sensor or transducer*. This analog signal is band limited by *anti-aliasing filter*. The signal is then *sampled* at a frequency rate, more than twice the maximum frequency of the band limited signal. The sampled signal is held constant by *hold*

circuit while conversion is taking place. The discrete signal from the sample and hold circuit is fed to analog to digital converter (ADC). The *ADC* gives digital output signal that can be easily processed, stored, or transmitted by digital systems or computer system.

The digital signal is converted back to by *digital to analog converter* (DAC). The output of DAC is usually stair-case waveform, which is passed through smoothing filter to reduce the quantization noise. The diagram shown in the above Figure can be used in the applications such as digital signal processing, digital audio mixing, music and video synthesis, data acquisition, pulse code modulation, and microprocessor instrumentation.

BASIC DAC TECHNIQUES:

The DAC converts digital or binary data into its equivalent analog value. The symbolic representation of an n-bit DAC is given below:



n-bit DAC

The DAC output can either be a voltage or current signal. For a voltage output DAC, the conversion characteristic can be expressed by;

$$W_0 = kkW_{FSS}(bb_1 2^{-1} + bb_2 2^{-2} + bb_3 2^{-3} + \ \ldots\ bb_{ii} 2^{-ii})$$

Where, V_0 – Output voltage

V_{FS} – Full scale output voltage

k – Scaling factor (usually 1)

$b_1 . . ., b_n$ – n-bit binary fractional word with decimal point located at the left

b_1 – MSB with a weight = $V_{FS}/2$

b_n – LSB with a weight = $V_{FS}/2^n$

Performance Parameters of DAC:

1. **Resolution:** *Resolution* is the number of various analog output values that is provided by a DAC.

   For n-bit DAC; $Resolution = 2^n$

   Resolution can also be defined as the ratio of change in output voltage resulting from a change of LSB at the digital input. For n-bit DAC; $Resolution = V_{OFS}/2^n - 1$

Where, V_{OFS} – Full scale output voltage.

If we know the resolution, we can obtain input-output relation for DAC:

$$V_0 = Resolution\ x\ b$$

Where, b – Decimal values of digital input.

For example, in a 4-bit system, using ladder, the LSB has a weight of $\frac{1}{16}$. This means that, the smallest increment in the output voltage is $\frac{1}{16}$ of the input voltage. If we assume that, this 4-bit system has input voltage levels of +16 V; (since has a weight of $\frac{1}{16}$) a change in LSB results in a change of 1 V in the output. Thus, the output voltage changes in steps of 1 V.

Hence, this converter can be used to represent analog voltages from 0 to +15 V in 1-V increments. But, this converter cannot be used to resolve voltages into increments smaller than 1V. If we desire to produce +4.2 V, using this converter, the actual output voltage would be +4.0 V. This converter is not capable of distinguishing voltages finer than 1 V, which is the resolution of the converter.

If we want to represent voltages to a finer resolution, we would have to use a converter with more input bits. For example, the LSB of a 10-bit converter has a weight of 1/1024. If this converter has a +10 V full-scale output, the resolution is approximately, +10 * $\frac{1}{1024}$ = 10 mV.

Problem: *What is the resolution of a 9-bit D/A converter which uses a ladder network? What is the resolution expressed as a percentage? If the full-scale output voltage of this converter is +5 V, what is resolution in volts?*

Solution: The LSB in a 9-bit D/A converter has a weight of $\frac{1}{512}$. Thus, this converter has a resolution of 1 part in 512.

The resolution expressed in percentage is $\frac{1}{512}$ * 100 percent = 0.2 %.

The voltage resolution is obtained by multiplying the weight of the LSB by the full-scale output voltage. Thus, the resolution in volts is: $\frac{1}{512}$ * 5 = 10 mV.

Problem: *How many bits are required at the input of a converter, if it is necessary to resolve voltage to 5 mV and the ladder has +10 V full-scale?*

Solution: The LSB of an 11-bit D/A converter has a resolution of $\frac{1}{2048}$. This would provide a resolution at the output of $\frac{1}{2048}$ * 10 = +5 mV.

2. **Accuracy:** The *accuracy of the D/A converter* is primarily a function of the accuracy of the precision resistors used in the ladder and the precision of the reference voltage supply used. *Accuracy* is a measure of how close the actual output voltage is to the theoretical output value.

$$AAccccoorrssccyy = \frac{VV_{SSFFSS}}{(2^{ii} - 1)2}$$

Problem: *Calculate the accuracy of a 8-bit DAC, if the full scale output voltage is 10.0 V?*

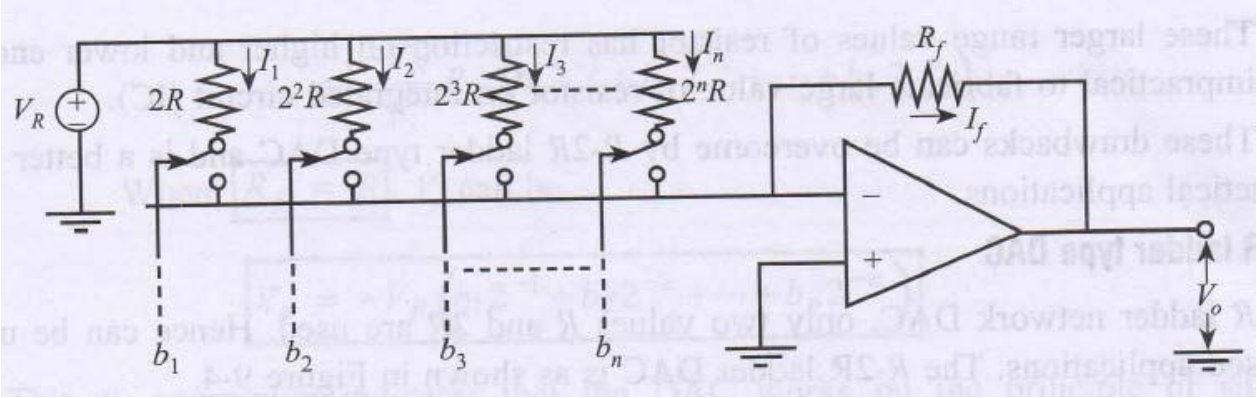
Solution: $AAccccoorrssccyy = \frac{VV_{SSFFS\ S}}{(2^{ii}-1)2} = \frac{10.0}{(2^{8}-1)2} = 19.8\ mmVV.$

3. **Setting Time:** *Setting time* is the time required for a DAC output to settle within $\pm\ ^{1}_{2}\ LLSSBB$ of final value for a given digital input.

4. **Stability:** The performance of a DAC is not *stable* due to the parameters such as temperature, power supply variations, and ageing.

Binary Weighted Resistor DAC:

The following Figure shows binary weighted resistor DAC circuit using *n*-electronic switches to control the binary inputs $b_1, b_2, \ldots, b_n$.



When the switch is ON; $II = \frac{VV_{RR}}{RR}$ When the switch is OFF; I = 0.

Due to very high input impedance of Op-Amp, the total current *I* will flow through R_f. The total current through R_f is; $ll = ll_1 + ll_2 + ll_3 + \ldots + ll_{ii}$

$$= \frac{VV_{RR}}{2^1 RR} bb_1 + \frac{VV_{RR}}{2^2 RR} bb_2 + \frac{VV_{RR}}{2^3 RR} bb_3 + \ldots + \frac{VV_{RR}}{2^{ii} RR} bb_{ii}$$

$$= \frac{VV_{RR}}{RR} [bb_1 2^{-1} + bb_2 2^{-2} + bb_3 2^{-3} + \ldots + bb_{ii} 2^{-ii}]$$

The output voltage is; $V_0 = -I_f R_f$

$$ii.ee., VV_0 = \frac{-VV_{RR}}{RR} RR_{ff} [bb_1 2^{-1} + bb_2 2^{-2} + bb_3 2^{-3} + \ldots + bb_{ii} 2^{-ii}]$$

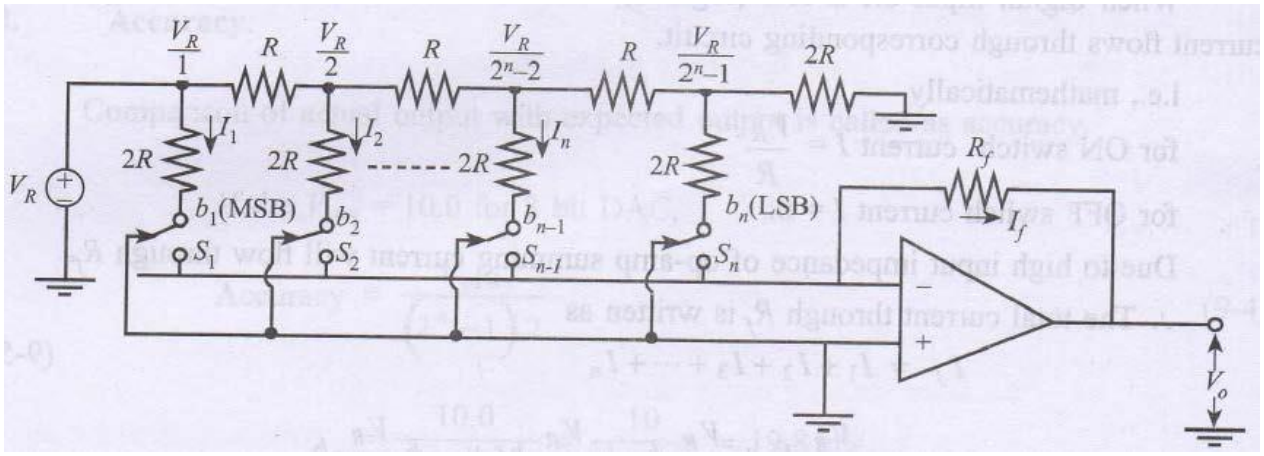
If $R_f = R$; Or, $VV_{11} = -VV_{RR}\blacklozenge bb_{11}22^{-11} + bb_{22}22^{-22} + bb_{33}22^{-33} + \ldots + bb_{mm}22^{-mm}\blacklozenge$

Drawbacks: (1) Large range of resistor values are required, as resistance values increases like $2^1R, 2^2R, 2^3R, \ldots, 2^nR$.

(2) Practically it's difficult to fabricate large values of resistors on IC.

R-2R Ladder type DAC:

In R-2R ladder, only two values, R and 2R are used. The circuit diagram is given below:



Each binary bit connects switch either to ground (non-inverting input) or to the inverting terminal of Op-Amp. Due to virtual ground, both the positions of the switches are at ground potential, and currents through the resistances are constant.

The current flowing through each of 2R resistances;

$$II_1 = \frac{VV_{RR}}{2RR} \qquad II_2 = \frac{VV_{RR}/2}{2RR} = \frac{VV_{RR}}{4RR} \qquad II_3 = \frac{VV_{RR}/4}{2RR} = \frac{VV_{RR}}{8RR} \qquad II_{ii} = \frac{VV_{RR}/(2^{ii}-1)}{2RR}$$

$$\text{But, } W_0 = -I_{ff}RR_{ff} = -RR_{ff}(II_1 + II_2 + \ldots + II_{00})$$

$$ii.ee., VV_0 = -RR_{ff}\left[\frac{VV_{RR}}{2RR}bb_1 + \frac{VV_{RR}}{4RR}bb_2 + \ldots + \frac{VV_{RR}}{2^{ii}RR}bb_{ii}\right]$$

$$\text{Or, } VV_0 = -\frac{VV_{RR}}{RR}RR_{ff}[bb_1 2^{-1} + bb_2 2^{-2} + \ldots + bb_{ii}2^{-ii}]$$

If $R_f = R$; $\qquad VV_{11} = -VV_{RR}[b_{11}22^{-11} + bb_{22}22^{-22} + \ldots + bb_{nn}22^{-nn}]$

Advantages: (1) As it requires only two types of resistors, fabrication and accurate value of R-@R can be designed.

(2) Node voltage remains constant, and hence, slow down effect can be avoided.

Example 1:

The digital input for a 4 bit DAC is $D = 0111$. Calculate its output voltage take $V_{oFS} = 15$ V.

$$\text{Resolution} = \frac{V_{oFS}}{2^n - 1} = \frac{15}{2^4 - 1} = 1\text{ V/LSB}$$

$$\therefore V_o = \text{Resolution} \times D$$

$$D = \text{Decimal values } (0111) = 7$$

$$V_o = \frac{1\text{ V}}{\text{LSB}} \times 7 = 7\text{ V}$$

$$\therefore \boxed{V_o = 7\text{ V}}$$

Example 2:

A 8 bit DAC having resolution of 22mv/LSB. Calculate V_{oFS} and output if the input is $(10000000)_2$.

Given: resolution = 22 mV, Input = $(1000000)_2$

$$\text{Resolution} = \frac{V_{oFS}}{2^n - 1}$$

$$22mv = \frac{V_{oFS}}{2^8 - 1}$$

$$V_{oFS} = 5.6 \text{ V}$$

D = equivalent of $(10000000)_2 = 128$

$V_o = 22 \times 10^{-3} \times 128 = 2.8$ V.

Example 3:

Calculate output voltage produced by DAC, when output range is between 0 and 10 V for input binary number.

a) 10 (2 bit DAC) b) 0011

a) From equation (9-7) we can write,

$$V_o = 10\text{ V}\left(1\times\frac{1}{2}+0\times\frac{1}{4}\right) = 5\text{ V}$$

b) From equation (9-7) we can write,

$$V_o = 10\text{ V}\left(0\times\frac{1}{2}+0\times\frac{1}{4}+1\times\frac{1}{8}+1\times\frac{1}{16}\right)$$

$= 1.875$ volts.

Example 4:

Calculate the values of the LSB and full scale output for 4 bit DAC for 0 to 10 V range.

We have,

$$\text{LSB} = \frac{1}{2^4} = \frac{1}{16}$$

For 10 V range,

$$\text{LSB} = \frac{10\text{ V}}{16} = 625\text{ mV}$$

and

$$\text{MSB} = \left(\frac{1}{2}\right)\text{Fullscale}$$

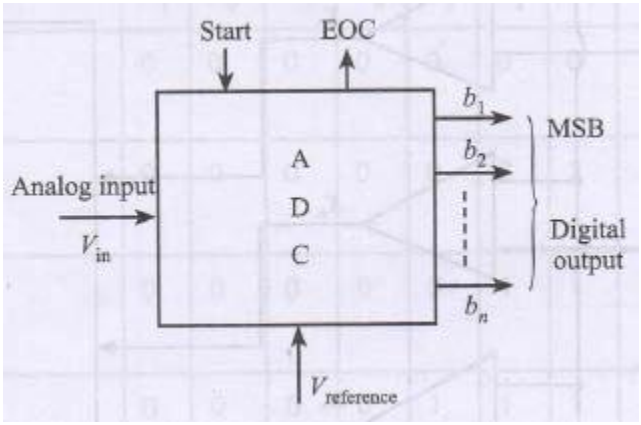
$$= \frac{1}{2}\times 10 = 5\text{ V}$$

Full scale output = Full scale voltage – 1 LSB

$$= 10 - 625\text{ mV} = 9.375\text{ V}$$

A-D CONVERTERS:

ADC takes the analog signal as input and converts into digital output. The functional diagram of DAC is given below:

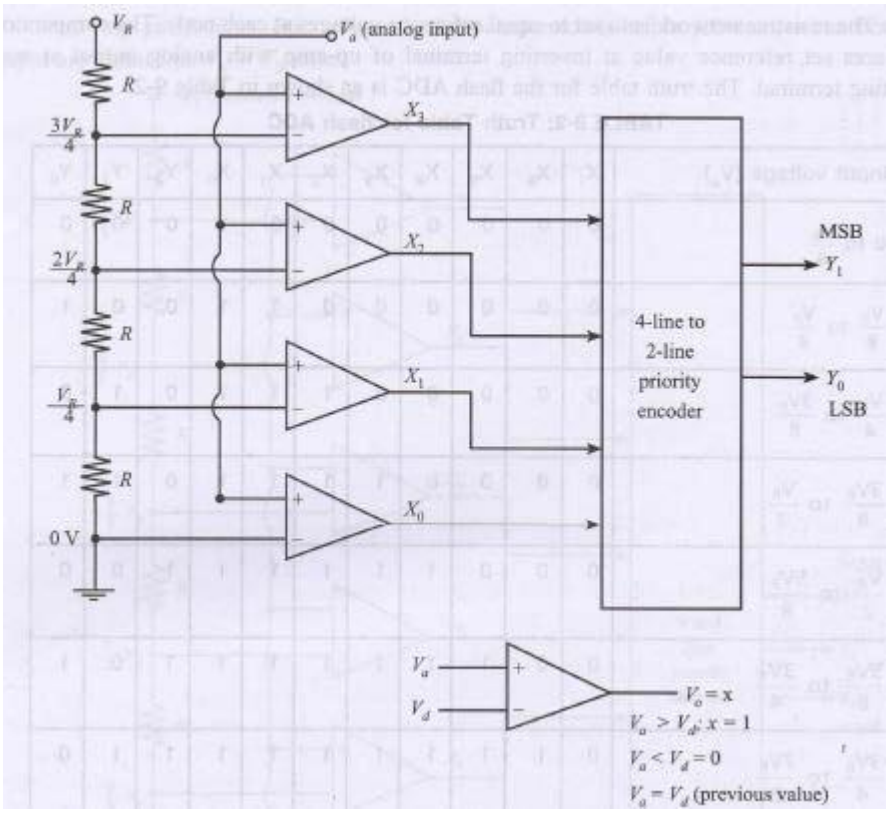


ADC is provided with two control inputs *start* (input to initiate the conversion) and *end of conversion* (output to indicate the end of conversion). *Direct type ADCs* and *Integrated type ADCs* are the two types of ADCs available.

Flash (Comparator/ Parallel) type ADC:

A simple, fast, but most expensive conversion technique.

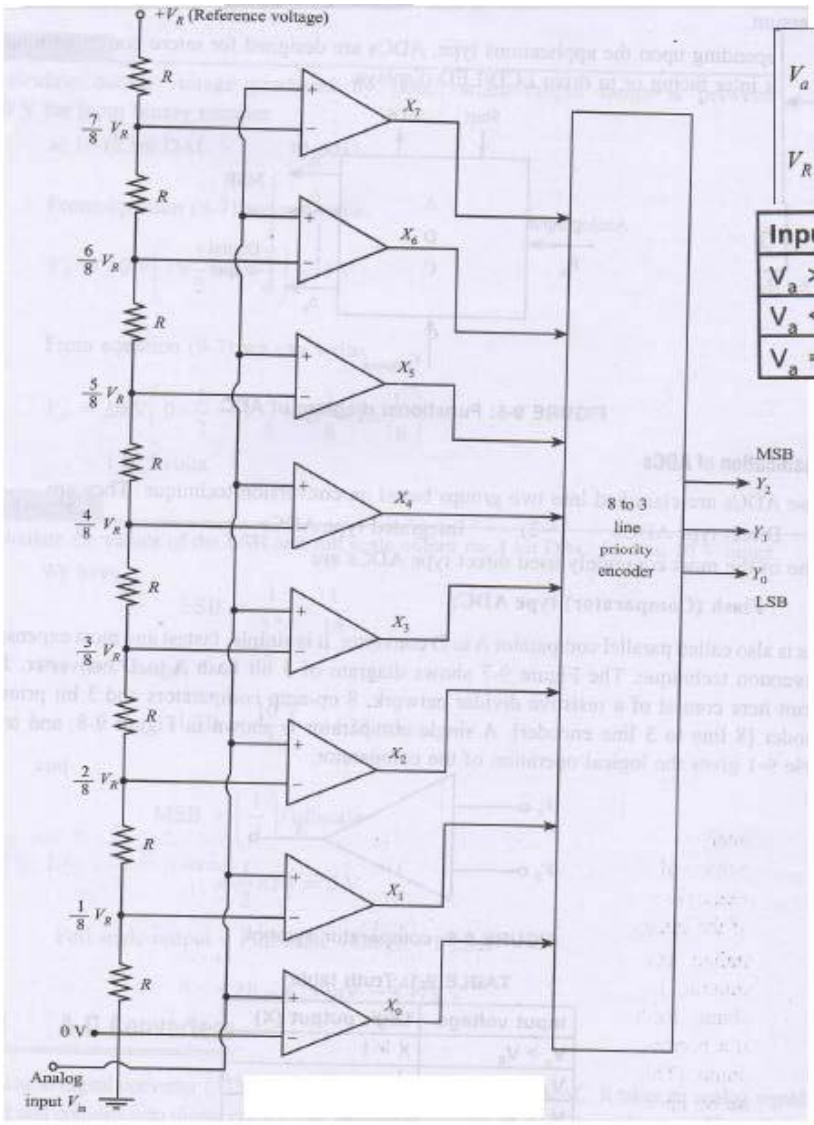
A 2-bit Flash ADC:

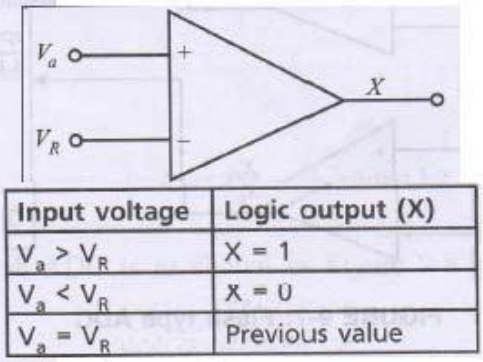


ANALOG AND DIGITAL ELECTRONICS

Analog input voltage (V_a)	X_3	X_2	X_1	X_0	Y_1	Y_0
0 to $\frac{V_R}{4}$	0	0	0	1	0	0
$\frac{V_R}{4}$ to $\frac{2V_R}{4}$	0	0	1	1	0	1
$\frac{2V_R}{4}$ to $\frac{3V_R}{4}$	0	1	1	1	1	0
$\frac{3V_R}{4}$ to V_R	1	1	1	1	1	1

A 3-bit Flash ADC:





Input voltage	Logic output (X)
$V_a > V_R$	X = 1
$V_a < V_R$	X = 0
$V_a = V_R$	Previous value

The resistive network is to set to equal reference voltages at each node. The comparactor compares set reference value at inverting terminal of Op-Amp with analog output at non-inverting terminal. The truthtable for ADC is given below:

Input voltage (V_a)	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $\frac{V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8}$ to $\frac{V_R}{4}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{V_R}{4}$ to $\frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8}$ to $\frac{V_R}{2}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{V_R}{2}$ to $\frac{5V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V_R}{8}$ to $\frac{3V_R}{4}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{3V_R}{4}$ to $\frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8}$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Advantages:

1. High speed

Disadvantages:

1. Number of comparators required is almost double for each added bit

   Eg.: For 2-bit ADC; No. of Comparators = 4 (2^2)

   For 3-bit ADC; No. of Comparators = 8 (2^3)

Successive Approximation type ADC:

The following Figure shows successive approximation ADC.

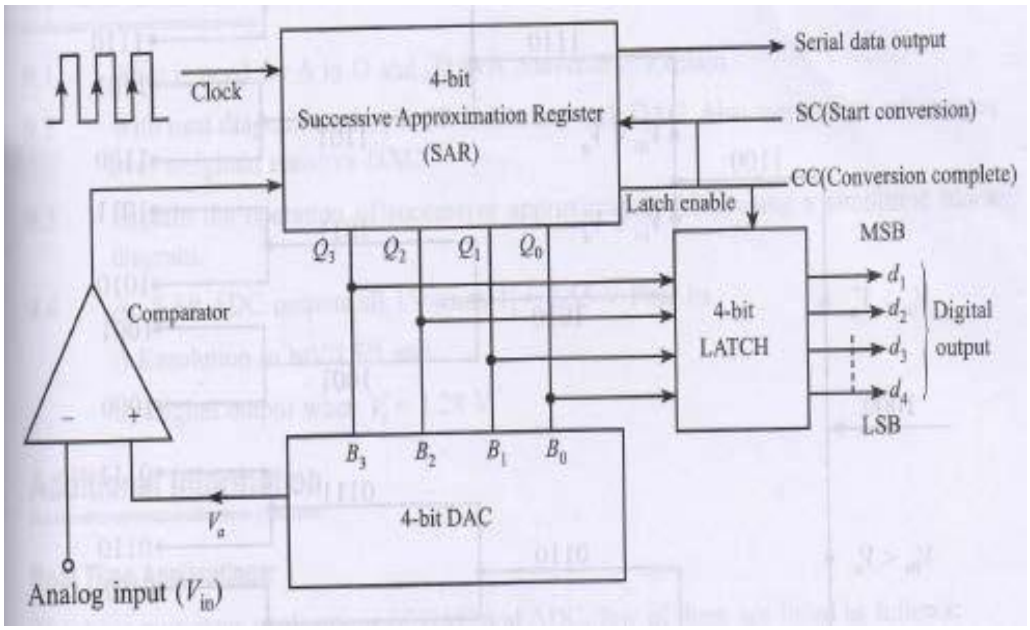
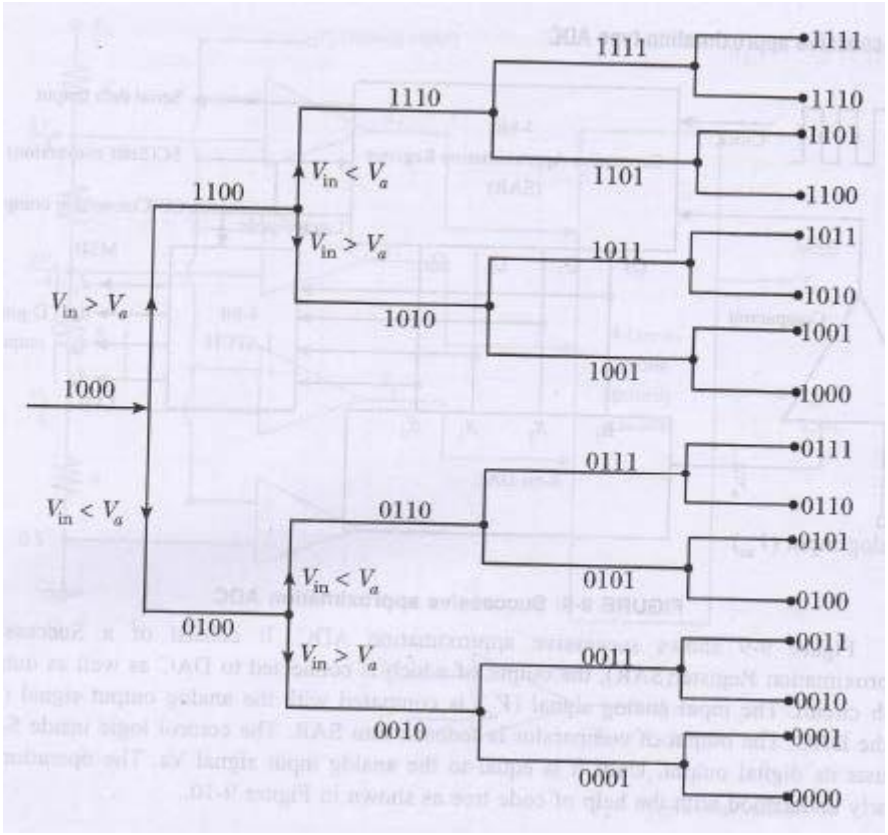


Figure shows a successive approximation register (SAR), the output of which is connected to DAC and output latch circuit. The input signal (V_{in}) is compared with the analog output signal (V_a) of the DAC. Output of the comparator is feedback into SAR. The control logic inside SAR adjusts its digital output; until it is equal to the analog input signal. The operation could be understood by the code tree given below.

At the start of conversion cycle, start conversion terminal is made high. On the first clock pulse, the output of the SAR is made 1000. The DAC produces an analog voltage (V_a) proportional to 1000. This analog voltage is compared with input analog signal (V_{in}).

If $V_{in} > V_a$, the comparator output will be high and SAR keeps Q3 high. On the other hand, if $V_{in} < V_a$, then the comparator output becomes low and SAR resets Q3 to low. If $V_{in} > V_a$, SAR follows the upward path in code tree and if $V_{in} < V_a$, SAR follows downward path.



The conversion time for *n*-bit successive approximation ADC is (*n* + *2*) clock periods.

Advantages:

1. Considerably good speed
2. Good resolution.