# Package Co-Design of a Fully Integrated Multimode 76-81GHz 45nm RFCMOS FMCW Automotive Radar Transceiver

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***Abstract* — The successful implementation, adoption, and proliferation of mmWave radar sensing technologies, to enabling future ADAS (advanced driver-assisted system) safety features, will require highly-integrated, high performance, and cost-effective packaged SoC (system on chip) solutions. This paper presents the co-design/simulation and measured results of a fully integrated 76-81GHz 45nm RFCMOS automotive transceiver packaged in a 0.65-mm pitch, 161-pin 10.4 mm × 10.4 mm flip chip BGA. Due to the complex process integration and mmWave operational frequency, electromagnetic interactions at system-level (viz. Silicon + Package + PCB) are exacerbated with potential impact to performance and functionality. We detail how package technology selection, via optimization of the package and system, was achieved through a coupled circuit-to-electromagnetic co-design modeling and simulation methodology. Laboratory measurements on TI AWR1243(TM), a fully integrated 76-81GHz FMCW (frequency modulated continuous wave) automotive transceiver, are presented that validate the integrity of the co-design modeling and simulation methodology.**

***Keywords – Automotive Radar; RFCMOS; IC Packaging; Co-Design Modeling and Simulation.***

## I. INTRODUCTION

Advanced driver assistance systems (ADAS) are generally defined as vehicle-based intelligent systems that provide assistance to the driver and improve driving experience [1]. Automotive radar sensor is a key technology for enabling future ADAS safety features. Collision detection, collision avoidance, warning, and mitigation, blind spot monitoring and detection, lane change assistance, lane departure warming system, are some of the safety features of ADAS (Figure 1). The ADAS automotive market was estimated at $32 billion in 2017 and is expected to reach around $60 billion in 2025 [2]. While the market forecast is very promising, the technical challenges are expected to be numerous and complex. A key requirement to the successful proliferation of radar sensing technologies, for automotive high volume manufacturing (HVM), is a highly-integrated, high performance, low power, and cost-effective transceiver packaged solutions.

The growing demand for safety-critical Advanced Driver Assistance Systems for pedestrian detection/avoidance, lane departure warning/correction, traffic sign recognition, surround view, drowsiness monitoring and other applications, is requiring a new class of system on chip (SoC) automotive radar. Typically, a complete mmWave radar SoC system includes transmit (TX) and receive (RX) radio frequency (RF) components; analog components such as clocking; and digital components such as analog-to-digital converters (ADCs), microcontrollers (MCUs) and digital signal processors (DSPs). Traditionally, these systems were implemented with discrete components, which increased power consumption and overall system cost. System design is challenging due the complexity and high frequencies.

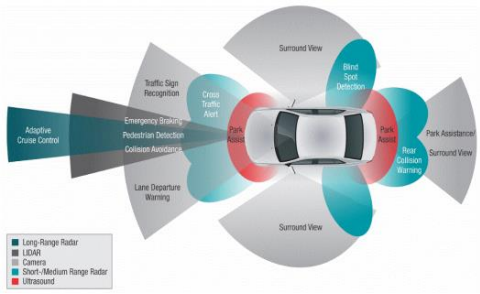


Fig. 1. Features of ADAS for Automotive Safety.

Texas Instruments, Inc. RFCMOS mmWave sensors differentiate themselves from traditional SiGe-based solutions [3-4] by enabling flexibility and programmability in the mmWave RF front-end and the MCU, hardware accelerator (HWA), and DSP processing back-end. CMOS front-ends offer tight integration with the baseband and microcontroller components which result in small-form-factor, low-power, low-cost architectures [5-6]. Another crucial element in a low-cost millimeter-wave radar solution is the IC packaging technology. While there have been many claims for optimal packaging solutions – ranging from traditional QFN [7], wire-bond BGA [8], and to fan-out WLP [9-10], the solutions are either too cost prohibitive and/or fall short of the desired electrical/thermal/reliability requirements. The requirements for packaging are numerous and complex – these include excellent RF isolation and controlled impedance, minimum attenuation/dispersion, good thermal performance at 125°C, good signal integrity of I/O to enable optimal fan-out for PCB routing, 1000+ cycles for solder join reliability, meet/exceed automotive safety requiring AEQ-100 G1 reliability, and provisioning for a highly scalable solution for future integration of passive and antenna, among others.

After a brief overview of the AWR1243™ device in Section II, the electrical co-design methodology developed for electrical performance assessment of the packages and system are presented in Section III. Selection of the optimal packaging technology, based off electrical comparative study of cost-effective packaging technologies, is detailed in Section IV. Measurements and system characterization details of the AWR1243™ device is discussed in Section V.

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## II. TRANSCEIVER DESCRIPTION

A comprehensive technical description of the automotive radar transceiver platform design is provided in [11]. We summarize here the main functional building blocks and provide a high-level overview of the functionalities of each block. The AWR1243$^{TM}$ device is a single-chip highly integrated radar transceiver and front end that includes three transmit and four receive chains (Figure 2). The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, power amplifier (PA), low-noise amplifier (LNA), mixer, intermediate frequency (IF), and analog-to-digital (ADC). This subsystem also includes the crystal oscillator and temperature sensors. The three transmit channels can be operated up to a maximum of two at a time (simultaneously) for transmit beamforming purpose as required; whereas the four receive channels can all be operated simultaneously.

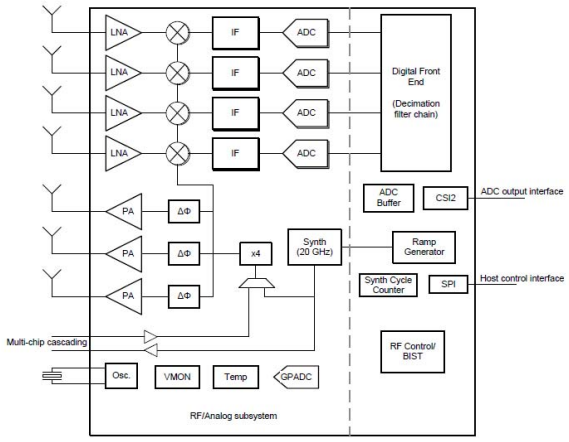



Fig. 2. Functional subsystem of the AWR1243$^{TM}$ transceiver.

The clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal. It has a built-in oscillator circuit followed by a clean-up phase-lock loop (PLL) and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76- to 81-GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation. The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

The device transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. A maximum of two transmit chains can be operational at the same time. However, all three chains can be operated together in a time-multiplexed fashion. The device supports binary phase modulation for MIMO radar and interference mitigation. Each transmit chain can deliver a maximum of 12 dBm at the antenna port on the PCB. The transmit chains also support programmable backoff for system optimization. Figure 3 depicts the transmit subsystem components. Also shown are the package and PCB interfaces.

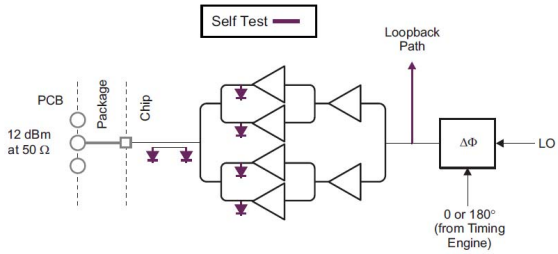



Fig. 3. Transmit subsystem of the AWR1243$^{TM}$ transceiver.

The device receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, A2D conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization. Unlike conventional real-only receivers, the AWR1243 device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The AWR1243 is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies that is above 350 kHz and can support bandwidths up to 15 MHz.

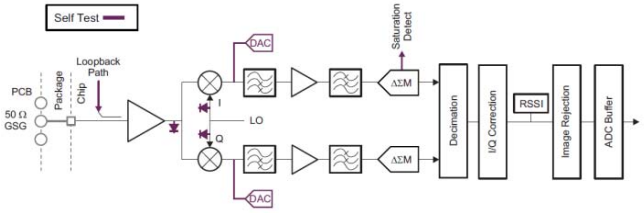



Fig. 4. Receive subsystem of the AWR1243$^{TM}$ transceiver.

The clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal. It has a built-in oscillator circuit followed by a clean-up phase-lock loop (PLL) and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an x4 multiplier to create the required frequency in the 76- to 81-GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation. The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Other subsystem of interests are the control interfaces. The device is controlled from external processor via the serial perpipheral interface. SPI is a high-speed synchronous serial input/output port that allows a serial bit stream to be shifted into and out of the device at a programmed bit-transfer rate. Additionally, the device uses MIPI D-PHY / CSI2-based format to transfer the raw A2D samples to the external MCU. The CSI is a MIPI D-PHY compliant interface for connecting the device to a camera receiver module. This interface is made of four differential lanes; each lane is configurable for carrying data or clock.

## III. Electrical Co-Design Modeling Methodology

To assess the electrical performance of the different packaging technologies and their impact to the system, a coupled circuit-to-electromagnetic methodology was developed. Figure 3 below shows the high-level modeling flow for the assessment of the packages performance. As per the flow, the package is designed with inputs from manufacturing/assembly rules and engineering/customer specs. S-parameters extractions for RF channels were extracted using a full-wave 3D electromagnetic solver. RLGC parasitics for power integrity analysis of the digital/analog supply/ground networks were performed using 3D quasi-static electromagnetic solver. Simulation to measurement correlations of these solvers were previously demonstrated in [12-13].

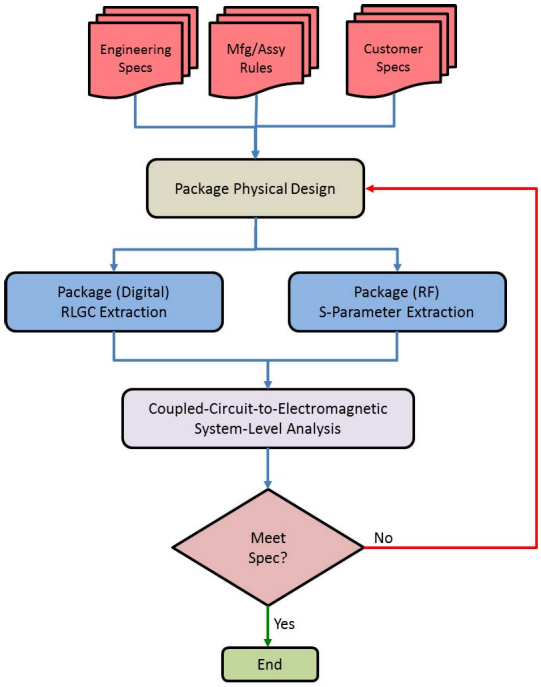



Fig. 5. Package Co-Design and Co-Analysis Methodology

The extracted models are then pushed through to the system-level circuit analysis step. In the system-level circuit analysis step, the time and frequency domain models of the package are coupled to the silicon transistor spice netlist and transient analysis performed. If the requirements are met for the investigated figure of merits (FOMs – viz. insertion loss, return loss, crosstalk, supply inductance, jitter, among others), the flow is exited. If the requirements are not met, then it iteratively looped back to the package and chip floorplanning step and re-designs until requirements are met or exceeded. The impact of PCB on system performance can also be assessed via the same flow.

Due to the complex process integration and mmWave operational frequency, electromagnetic interactions at system-level (viz. Silicon + Package + PCB) are exacerbated. As such it is critical that good physical and electrical co-design techniques are employed. The physical co-design involved the optimization of the SoC floorplanning, package and PCB routing. Apart from physical design optimization for routability and manufacturability, it is critical to making sure that electrically there is no performance decay through the system (viz. chip + package + PCB) transitions. Traditional approach to electrical co-analysis focused on electromagnetic extractions of each component separately and cascading the models during the system-level analysis. This approach cannot be applied to mmWave frequency extractions due to the high electromagnetic interactions at each transition. The classical approach of concatenating each model to represent the complete 3D behavior can lead to inaccurate modeling at even lower frequency. The authors know at first hand a signal integrity issue that was observed, modeled, and characterized on a 12.5Gbps SFF-8431 link at the package to PCB transition/interface [14]. A "phantom" capacitance was observed during time domain reflectometry (TDR) measurement at the package to PCB transition – i.e. the BGA balls. This capacitive dip was not observed in the modeling via the classical approach – where package and PCB models were extracted separately and concatenated for system-level analysis. When the correct 3D co-design approach was employed, in which the physical design of the package was merged to the physical design of the PCB and 3D full-wave extraction performed on the merged coupled structure, only then the capacitive dip was observed (Figure 4). The cause was later determined to be an increase in the ball-to-ball capacitive coupling due to BGA balls collapsing phenomenon observed during manufacturing process. The detail phenomenon, the simulations methodologies, and silicon measurement to modeling correlation and characterization are fully detailed in [14].

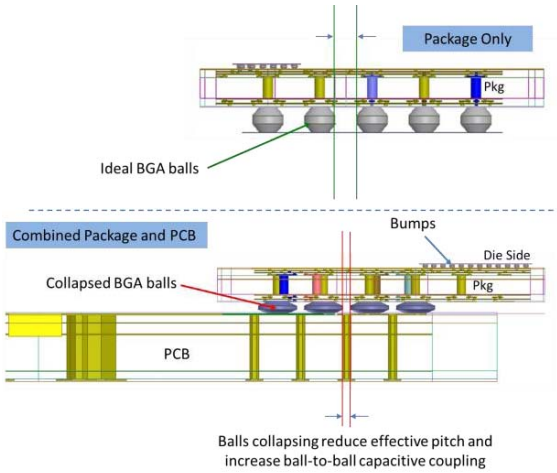



Fig. 6. Electromagnetic interactions at Package + PCB interface.

For improved accuracy and integrity of models, the co-design and co-analysis developed here comprehends the electromagnetic interactions at the interface of die bump to package and package BGA ball to PCB. In the next section we detail how package technology selection was achieved using the flow developed here.

## IV. Package Technologies for Automotive mmWave

As discussed above, ccontinued advances in semiconductor manufacturing technologies in recent years have made it possible to develop mm-wave monolithic integrated circuits (MMICs) using standard CMOS processes at a relatively low cost. However, it remains a challenge to develop suitable and affordable techniques for interconnects and packaging of these MMICs, especially for low cost commercial systems such as automobile radars. Packaging solution for these MMICs needs to provide adequate system level performance while withstanding harsh environmental loads such as moisture, chemicals, and wild temperature swings [15]. In the sub-sections that follow, an electrical assessment of cost-effective packaging technologies are undertaken using the co-design methodology described in Section III.

Like most high speed interconnection designs, the primary goal of mm-wave package transition design is to ensure maximum RF transmit and receive power transfer from die through package to PCB. As such one of the most critical electrical performance parameter, or figure of merit (FOM), is insertion loss (IL), which is often expressed in dB as:

$$IL(dB) = 10\log_{10}\frac{P_T}{P_R} \qquad (1)$$

where $P_T$ is the power inserted at one point and $P_R$ is the power received at the other point. For common cases where same reference impedance is used both ends, the insertion loss is related to the scattering parameters with the equation

$$IL = -20\log_{10}|S_{21}|dB \qquad (2)$$

It should be noted that the mm-wave transceivers under consideration have a fairly narrow signal bandwidth compared to the carrier frequency, *i.e.*, 76GHz to 81GHz, instead of spreading all the way from DC to several harmonics of the data rates as for most digital signals. Therefore, we only need to design the package structure such that it provides good signal propagation within this relatively narrow band of interest without paying much attention to its behavior outside of the band.

Three widely used packaging technologies, QFN, nFBGA, and FCBGA, are evaluated for their ability to support high-fidelity power transfer for mm-wave applications as detailed below.

### *4.1 QFN Package*

QFN (Quad Flat No-leads) package is a near Chip Scale Package (CSP) made with a planar copper lead frame substrate [16]. It is a mature packaging technology with very low manufacturing cost. While the exposed thermal pad offers extremely low thermal resistance to the PCB, the relatively long bondwire connection and large separation between signal and ground bondwires limited its application at higher frequencies. Table 1 below shows a number of GSG configurations attempted and their corresponding simulated insertion loss performances.

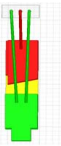
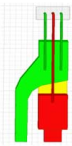
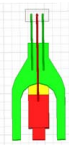
| Bondwire Configurations | Qfn_11 | Qfn_11_no_stub | Qfn_13 | Qfn_13_no_stub | Qfn_14 |
|---|---|---|---|---|---|
| |  |  |  |  |  |
| Insertion Loss @77GHz | -7.6dB | -4.4dB | -7.64dB | -10.45dB | -13.6dB |

TABLE I. Simulated QFN package designs

In the bondwire configurations depicted above, the green copper plates and bondwires are for GND connection while the red ones are for signaling. The best IL performance, at nominal condition, was seen with the configuration of no plating stub on the signal plate (there is a small cost adder compared to the normal configuration with stub) at 77GHz, but -4.4dB is not enough to meet the link budget for the package transition for most applications. It is clear from the resulted that QFN is not the packaging technology of choice.

### *4.2 nFBGA Package*

nFBGA packages are a family of laminate-based CSP's that use bond wire as the interconnect between die and the package substrate while connections between the package substrate and the board are made with alloy balls [17]. The nFBGA family comes in a range of solder ball pitch, and can accommodate various stacked die configurations, with as many as three die housed in each package. It has been fully qualified in numerous applications and is being used extensively in mobile phones, laptops, modems, handheld devices, and automotive environment.

A channel in an nFBGA package consists of bond wires, package traces, vias, and solder balls, as shown in Figure 7 below.

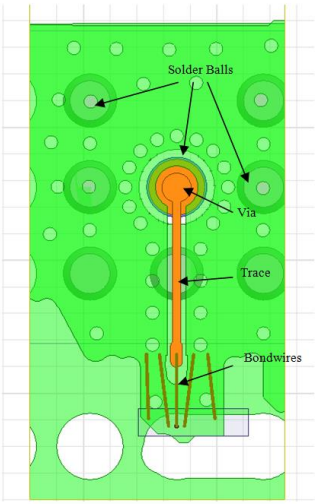



Fig. 7. nFBGA package connection (top down view)

While package traces are uniform transmission lines with well controlled impedance over a wide frequency range, bondwires, vias and solder balls can all cause impedance discontinuities. Even with minimum pitch between a signal bondwire and its nearby ground, the characteristic impedance of the line is still well above 50 Ohms. So, bondwires are usually regarded as an inductive region of the channel. In contrast, vias and solder balls are normally capacitive impedance discontinuities.

Due to the above mentioned impedance discontinuities along the channel, nFBGA packages are typically used for low or mid speed applications. Recently, 40Gbps digital signal transmission with a similar packaging technology has been achieved by minimizing the impacts of each individual impedance discontinuity along the signal propagation path [18]. However, it is very difficult, if not impossible, to expand the frequency range from DC to 80GHz with the same or similar techniques. On the other hand, it is possible to achieve good signal propagation along the channel within the relatively narrow bandwidth of 76GHz to 81GHz as discussed earlier.

Simulated insertion loss of a receiver pair under nominal manufacturing process parameters is shown in Figure 8. There is clearly a peak at around 80GHz and insertion loss greater than -2dB has been achieved in the band of 76GHz to 84GHz. However, at such high frequencies, the usually hard to control small variations in bondwire geometries in the manufacturing process can lead to significant changes in the impedance matching condition and may be of concern for large volume production.

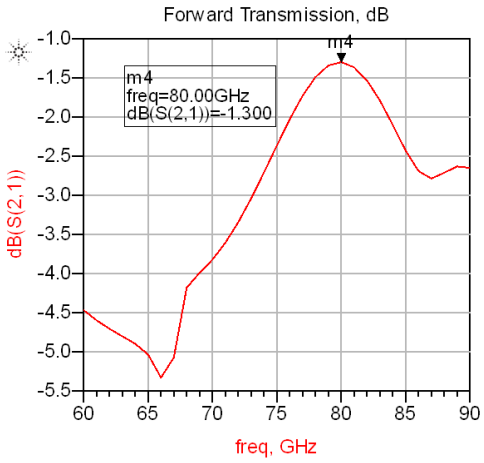



Fig. 8. nFBGA IL simulation results

### *4.3 Flip chip BGA (FCBGA) Package*

Flip chip packages use conductive alloy "bumps" placed directly on the die surface to connect to the package carrier (substrate) [19]. As such, the bumped die needs to be "flipped over" and placed face down. A typical channel in an FCBGA package consists of solder bumps, package traces, vias, and solder balls, as shown in Figure 9 below.

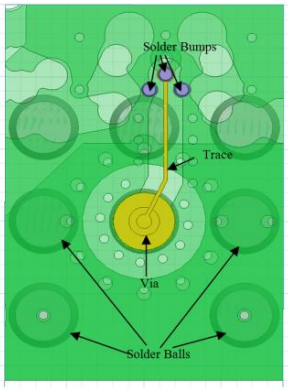



Fig. 9. FCBGA package connection (top down view)

Compared to nFBGA packages, the solder balls and the trace routing on the FCBGA packages have the same constructions/characteristics, but the bump connections between the die and the substrate are much shorter in length and thus bring about much smaller inductance than the bondwires. As a result, insertion losses for connections made through FCBGA packages usually do not typically show sharp resonant behaviors as those with nFBGA packages. The simulated insertion losses over a FCBGA package transition for the automotive radar application under nominal process/environmental conditions are shown in Figure 10. The peak insertion loss within the operating frequency range is below -0.8dB.

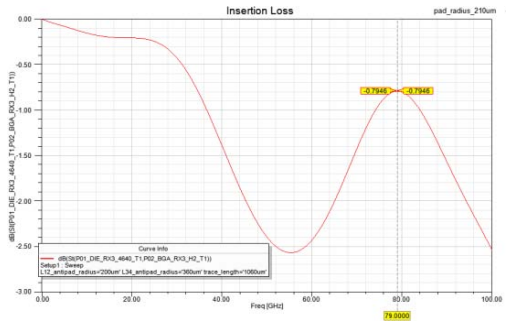



Fig. 10. Insertion loss of a channel on FCBGA design (package only)

In addition, manufacturing process variations in solder bump geometry are usually smaller than those with bondwires. So, FCBGA is the package technology selected for the automotive radar transceiver design.

### *4.4 Package Co-Design FOM Parametric Study*

As mentioned earlier, bondwires, vias, solder bumps, and solder balls on the package can all cause impedance discontinuity and thus make it almost impossible to achieve the insertion loss target of greater than -2dB from DC to 80GHz. However, it is possible to achieve the goal within a relatively narrow bandwidth. The key here is to recognize and take advantage of the resonance phenomenon that occurs naturally between the bondwire inductance and via/ball capacitance.

As shown in Figure 11, the signal propagation path on a nFBGA or a FCBGA package can be conceptually divided into three regions: the transmission line segment formed by the trace routing on the substrate, the capacitive region formed by the (stacked) vias and the solder ball, and finally the inductive region coming from the bondwires(nFBGA) or solder bumps(FCBGA). As per complex conjugate impedance matching theory, when the length of the transmission line segment is equal to multiples of the guided wavelength at the center frequency, the inductance and the capacitance "cancel" each other and maximal insertion loss along the path is achieved. So, in addition to minimizing bondwire length and optimizing via/ball transitions, a critical design parameter that needs to be controlled precisely is the length of the trace between the bond finger and the through hole via on the package such that it is roughly equal to multiples of the guided wavelength at about 80GHz.

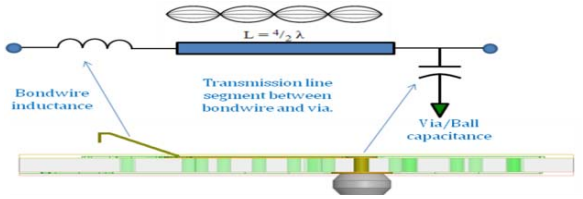



Fig. 11. Controlling resonant frequency of a FCBGA signal channel.

In practice, the optimal value of the trace length can be determined through parametric studies in simulation where the trace length on the package is parameterized and swept across a range and insertion loss of the channel is monitored. Sample results from such a study are shown in Figure 12. Trace length that gives the highest insertion losses in the frequency band of interest is then used in preliminary package routing.

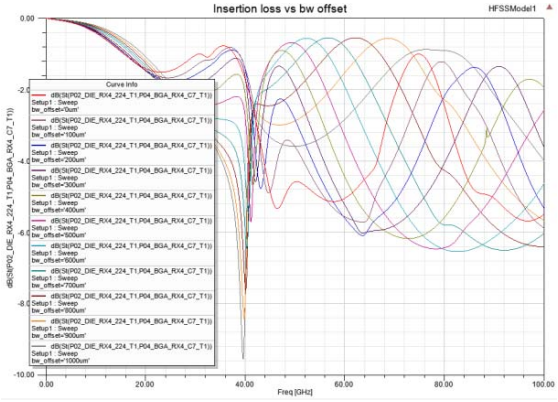



Fig. 12. Parametric studies of resonant frequency vs. package trace length.

### *4.5 Power Integrity/Coupling Analysis*

As mentioned in Section III, extraction and optimization of the parasitics for critical power/gnd supplies network were performed. These include the analog and digital supplies. Additionally, intra- and inter-coupling between the serial interfaces/clocks were modeled, using methodology developed in [20], and optimized to achieve desired requirements. Figure 13 below shows the original and improve package routing design and their corresponding coupling performance.

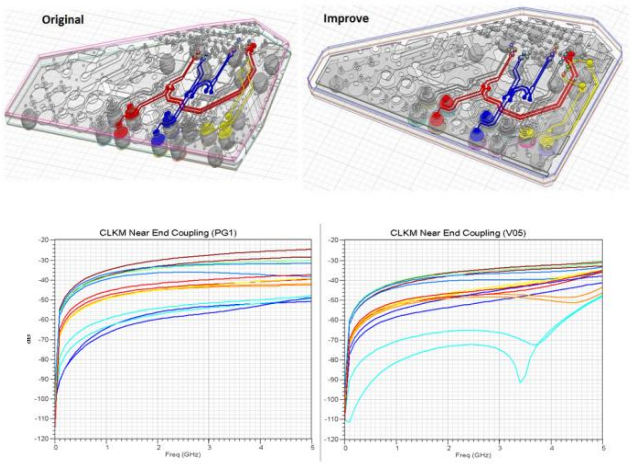



Fig. 13. Design improvement via co-design to reduce coupling.

### *4.6 System-Level Transition Modeling*

As mentioned earlier, bondwires, vias, solder bumps, and solder balls on the package can all cause impedance discontinuity and thus make it almost impossible to achieve the insertion loss target of greater than -2dB from DC to 80GHz. However, it is possible to achieve the goal within a relatively narrow bandwidth. The key here is to recognize and take advantage of the resonance phenomenon that occurs naturally between the bondwire inductance and via/ball capacitance. After the preliminary package routing for the mmWave section is finished, we connect the package with relevant structures on die and the PCB to evaluate the IL, RL, and crosstalk over the whole signaling path. The simulation result for the FCBGA package with on-die structure and a small transmission line segment on PCB is shown in Figure 14.

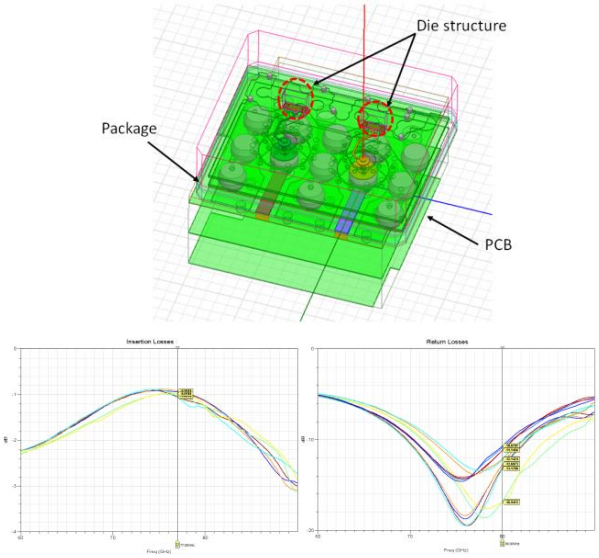



Fig. 14. Insertion/Return Loss of System (Die + Pkg+ PCB).

To assess the impacts of many manufacturing/assembling process variations, we also perform a large number of Design of Experiment (DOE) simulations where many geometric features of the package and PCB are parameterized and varied. One typical set of such results are shown in Table II. When the complete die, package and PCB layouts are optimized, final transient system-level analyses were performed.

| | | Design Parameters | | | | Insertion Loss @80GHz | | MAG @80GHz | |
|---|---|---|---|---|---|---|---|---|---|
| | | Nominal Values | Min | Max | Sweep Step | Min (dB) | Max (dB) | Min (dB) | Max (dB) |
| Package | | | | | | | | | |
| | Mold Compound Loss Tangent | 0.014 | 0.01 | 0.02 | 0.002 | -2.78 | -2.75 | -1.52 | -1.52 |
| | Trace width | 25um | 20um | 30um | 2um | -2.84 | -2.68 | -1.54 | -1.51 |
| | Buildup layer thickness | 20um | 10um | 30um | 2um | -2.93 | -2.73 | -1.66 | -1.51 |
| | Core dielectric layer thicknes | 150um | 130um | 170um | 10um | -3.06 | -2.49 | -1.54 | -1.51 |
| | Solder bump height/deformation | 80um | 72um | 96um | df (0.9~1.2) | -2.80 | -2.70 | -1.65 | -1.46 |
| | Solder ball height/deformation | 300um | 270um | 350um | df (0.9~1.2) | -2.77 | -2.73 | -1.57 | -1.50 |
| | die/package alignment(offset) | 0um/0um (X/Y) | -10um/-10um | 10um/10um | 4um/4um | -2.80 | -2.70 | -1.54 | -1.50 |
| PCB | | | | | | | | | |
| | Trace width/GND Gap | 200um | 180um | 220um | 10um | -2.82 | -2.72 | -1.54 | -1.52 |
| | Rogers buildup layer thicknes | 127um | 119um | 135um | 2um | -2.85 | -2.65 | -1.53 | -1.51 |
| | BGA Pad radius | 165um | 160um | 200um | 10um | -3.52 | -2.67 | -1.60 | -1.51 |
| | BGA Antipad radius | 400um | 300um | 400um | 20um | -2.84 | -2.75 | -1.53 | -1.51 |
| | bottom layout cutout radius | 160um | 100um | 200um | 20um | -3.09 | -2.54 | -1.54 | -1.51 |
| | Back material dk | 3 | 2 | 5 | 0.2 | -2.80 | -2.70 | -1.52 | -1.52 |
| | package/PCB alignment(offset) | 0um/0um (X/Y) | -40um/-40um | 40um/40um | 20um/20um | -3.56 | -3.32 | -1.57 | -1.51 |

TABLE II. DOE RESULTS OF MM-WAVE TRANSITION OVER FCBGA PACKAGE

## V. MEASUREMENT DETAILS

Performance of full RF transition model (silicon + package + PCB) can be tested and verified by measuring RF parameters of the AWR1243$^{TM}$ device. A characterization board is designed and manufactured to enable measuring RF ports of the FCBGA device through G-S-G probe measurements. The characterization board and the measurement setup are shown in Figure 15.


Fig. 15. Probe measurement setup

GGB G-S-G probes are connected to WR-12 waveguide output of the frequency extenders. TRL calibration structures are implemented on the board to enable de-embedding GCPW line section from measurements.

Figure 16 shows measured return loss on the board. There is good correlation between simulated and measured return loss.

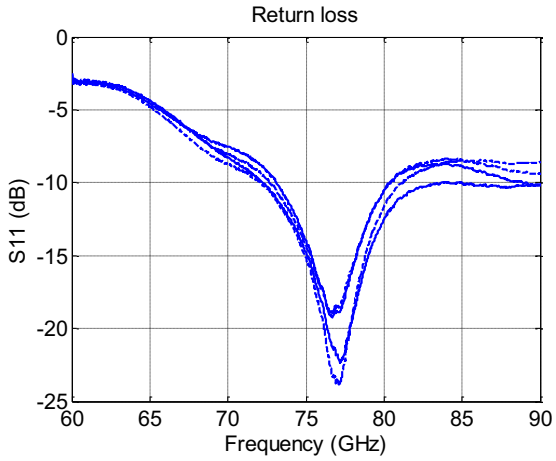



Fig. 16. Measured return loss

While there is no direct method to measure insertion loss of the package on the function device, it can be indirectly verified from other RF parameter measurements. Comparison between TX output power and RX noise figure measurements on silicon die probe modules and on the characterization board show good correlation with assumed simulated package insertion numbers.

## VI. CONCLUSIONS

As discussed, a critical requirement to the successful proliferation of radar sensing technologies, for automotive high volume manufacturing (HVM), is a highly-integrated, high performance, low power, and cost-effective transceiver packaged solutions. A number of HVM packaging technologies were evaluated and contrasted to assess their potential adoption for mmWave automotive applications – namely QFN, nFBGA, and FCBGA. While other technologies have been proposed in the literature (e.g. eWLB), their adoptions have been hampered either with poor performance at mmWave frequency and/or too costly for HVM manufacturing. We have presented considerations on die, package and board co-design and co-simulation for signal and power integrity of the mixed-mode (viz. Analog, RF, and digital) design. As demonstrated the electromagnetic interactions at the interfaces can impact performance significantly. To that end, we have shown that the comprehensive modeling/analysis co-design methodology can be successfully applied to characterize the performance of the device early in the design phase. Additionally the methodology provides the ability to perform parametric sweeping of the key performance figure of merits under manufacturing/assembly process variations. From characterization data obtained on the AWR1243$^{TM}$ evaluation module, we have validated the flow by demonstrating good correlation between the modeling methodology and silicon measurements.

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